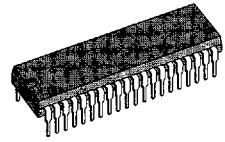
CMOS 16 X 8 CROSSPOINT WITH CONTROL MEMORY

- LOW ON RESISTANCE (typ. 60 Ω at V_{DD} = 10 V)
- INTERNAL CONTROL LATCHES
- ANALOG SIGNAL SWING CAPABILITY EQUAL TO POWER SUPPLY VOLTAGE APPLIED
- LESS THAN 1 % TOTAL DISTORT. AT 0 dBm
- LESS THAN – 95 dB CROSS-TALK AT 1 KHz 1 V_{pp}
- VERY LOW POWER CONSUMPTION



DIP40

ORDERING NUMBER : M3494 B1

DESCRIPTION

The M3494 contains a 16 x 8 array of crosspoint together with a 7 to 128 line decoder and latch circuits. Anyone of the 128 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is set at logical one.

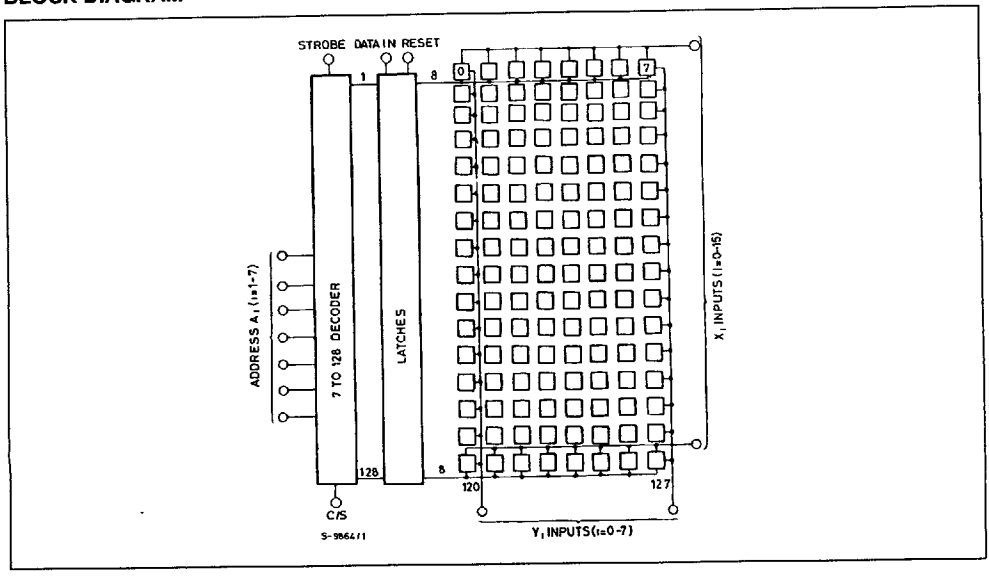
The input pin V_G shifts the logic level of the digital inputs. It allows one M3494 supplied between V_{BB} and V_{DD} to have input logic levels equal to V_G and V_{DD}.

M3494 can handle analog signals with an amplitude equal to the voltage power supply.

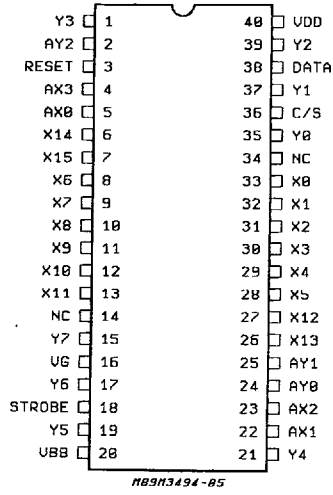
The C/S allows the control inputs of different devices to be connected in parallel in multiple chip system. Each device is selected when its own C/S input pin is high level.

M3494 is available in 40 lead dual in-line plastic.

BLOCK DIAGRAM



PIN CONNECTION (top view)



INPUT/OUTPUT DESCRIPTION

I/O	Symbol	Pin	Description
POWER			
I	V_{DD}	40	Positive Power Supply
I	V_{SS}	20	Negative Power Supply
I	V_G	16	Digital Signal Ground
ADDRESS			
I	AX0-AX3	4, 5, 22, 23	X Address Lines. These 4 pins are used to select one of the 16 rows of switches. Refer to the truth table for legal address.
I	AY0-AY2	2, 24, 25	Y Address Lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table for legal address.
CONTROL			
I	DATA	38	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
I	STROBE	18	This pin enables whatever action is selected by the ADDRESS and DATA pins. When the STROBE pin is held low, no switch openings or closings take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin)
I	RESET	3	Master Reset. This pin turns off (opens) all 128 switches. The states of the above control lines are irreleant. This pin is active high.
I	C/S	36	Chip Select. This pin allow the input control lines of different M3494's to be connected in parallel in multiple chip system. This pin is active high. Each device is selected by its own C/S input pin.
DATA			
I/O	X0-X11	6-13, 26-33	Analog Input/Outputs. These pins are connected to the Y0-Y7 pins in according to the truth table.
I/O	Y0-Y7	1,15,17,19,21 35,37,39	Analog Input/Outputs. These pins are connected to the X0-X15 pins in according to the truth table.

TRUTH TABLE

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0<0> -<0>Y0
1	0	0	0	0	0	0	X1<0> -<0>Y0
0	1	0	0	0	0	0	X2 <0>-<0>Y0
1	1	0	0	0	0	0	X3 <0>-<0>Y0
0	0	1	0	0	0	0	X4 <0>-<0>Y0
1	0	1	0	0	0	0	X5 <0>-<0>Y0
0	1	1	0	0	0	0	X12 -<0>Y0
1	1	1	0	0	0	0	X13 -<0>Y0
0	0	0	1	0	0	0	X6 <0>-<0>Y0
1	0	0	1	0	0	0	X7 <0>-<0>Y0
0	1	0	1	0	0	0	X8 <0>-<0>Y0
1	1	0	1	0	0	0	X9<0> -<0>Y0
0	0	1	1	0	0	0	X10 -<0>Y0
1	0	1	1	0	0	0	X11 -<0>Y0
0	1	1	1	0	0	0	X14 -<0>Y0
1	1	1	1	0	0	0	X15 -<0>Y0
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ <0> ↓
1	1	1	1	1	0	0	X15 - Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	1	0	X15 - Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	1	0	X15 - Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	0	1	X15 - Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	0	1	X15 - Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	1	1	X15 - Y6
0	0	0	0	1	1	1	X0 - Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	1	1	X15 - Y7

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (V_{BB} = 0)	– 0.5 to 14	V
V_{IN}	Input Voltage Range	V_G – 0.5 to V_{DD} + 0.5	V
P_{tot}	Power Dissipation	1	W
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 50 to 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltages	V_G = 0+ 5 ± 10 %	V
V_{BB}		– 5 ± 10 %	V
T_{op}	Operating Temperature	0, + 70	°C
V_{IN}	(logic signal)	V_G, V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{DD} = +5V, V_G = 0V, V_{BB} = -5V unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Supply Current	Reset = V_{DD}			1	mA
CROSSPOINT						
	On Resistance	V_{IDC} = 0.75V, V_{ODC} = 0.5V, See Figure 1		60	100	Ω
	On Resistance Variation			6	10	Ω
	Off-leakage *	All switches off V_{OS} = V_{IS} = V_{BB} to V_{DD}			± 3	µA
CONTROLS						
V_{IL}					0.8	V
V_{IH}			2.4			V
	Input Leakage *	V_{IN} = V_G to V_{DD}			± 3	µA

* The device is guaranteed with such limits up to 70°C. At 25°C these limits become ± 100nA.

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, C_L = 50pF all input square wave rise and fall times = 10ns, V_{DD} = 10V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
CROSSPOINT							
t_{PHL}, t_{PLH}	Propagation Delay Time (switch on) Signal Input to Output	R_L = 1kΩ		30	100	ns	2
	Frequency Response (any switch on) 20 log (V_{OS}/V_{IS}) = -3dB	R_L = 91Ω, V_{IS} = 2V_{PP}, C_L = 3pF		50		MHz	
	Sine Wave Distortion	f_i = 1kHz, R_L = 0.6kΩ, V_{IS} = 8V_{PP}			1	%	
	Feedthrough (any switches off)	f_i = 10kHz, R_L = 1kΩ, V_{IS} = 2V_{PP}	-80			dB	3
	Frequency for Signal Crosstalk Attenuation of 40dB Attenuation of 110dB	V_{IS} = 1V_{PP}	 1 5			 MHz kHz	4
C	Capacitance Xn to V_{BB} Yn to V_{BB} Feedthrough	 f_i = 1MHz, V_{IS} = 0.1V_{PP}	 15		 15 0.4	pF	
C	Capacitance Logic Input to V_G	f_i = 1MHz, V_{IS} = 0.1V_{PP}	5			pF	
CONTROLS (t_r, t_f = 10ns) (V_{DD} = +5V, V_G = 0V, V_{BB} = -5V)							
t_{PSN}	Propagation Delay Time Strobe to Output (switch turn-on to high level)	R_L = 1kΩ, C_L = 50pF		150	200	ns	5
t_{PZH}	Data-in to Output (turn-on to high level)			150	200	ns	6
t_{PAN}	Address to Output (turn-on to high level)			150	200	ns	7
t_{PSF}	Propagation Delay Time Strobe to Output (switch turn-off)			150	200	ns	5
t_{PZL}	Data-in to Output (turn-on to low level)			150	200	ns	6
t_{PAF}	Address to Output (turn-off)			150	200	ns	7
t_S	Set-up Time Data-in to Strobe or C/S		40			ns	5 10
t_H	Hold Time Data-in to Strobe or C/S		120			ns	5 10
t_O	Switching Frequency			1		MHz	
t_W	Strobe Pulse Width C/S Pulse Width		100			ns	10
t_{WR}	Reset Pulse Width		150			ns	9
t_{PHZ}	Reset Turn-off to Output Delay			150	200	ns	9
t_{AS}	Address Set-up Time Address to Strobe or C/S		120			ns	10
t_{AH}	Address Hold Time Address to Strobe or C/S		120			ns	10
	Control Crosstalk Data-in, Address or Strobe to Output	Square wave input, V_{IN} = 3V, R_L = 10kΩ		75		mV	8

TEST CIRCUITS

Figure 1 : RON Measurement.

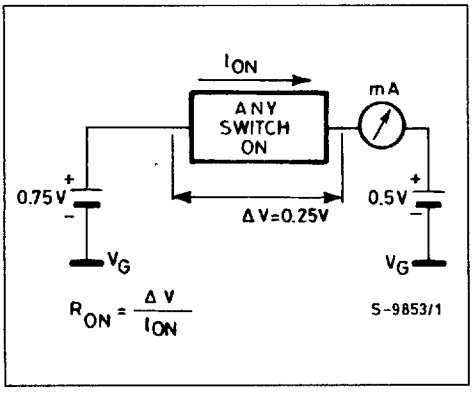


Figure 2 : Propagation Delay Time and Waveforms (signal input to signal output switch ON).

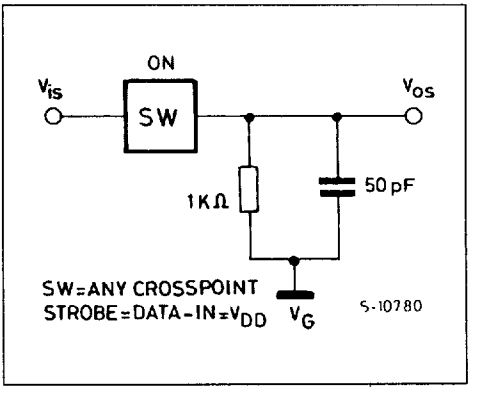
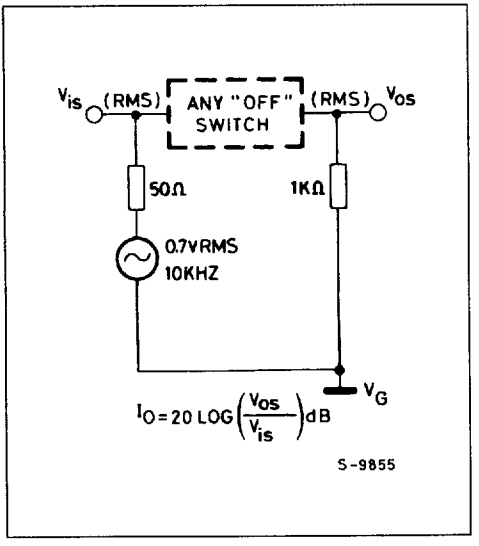


Figure 3 : Off Isolation Measurement (Feed through).



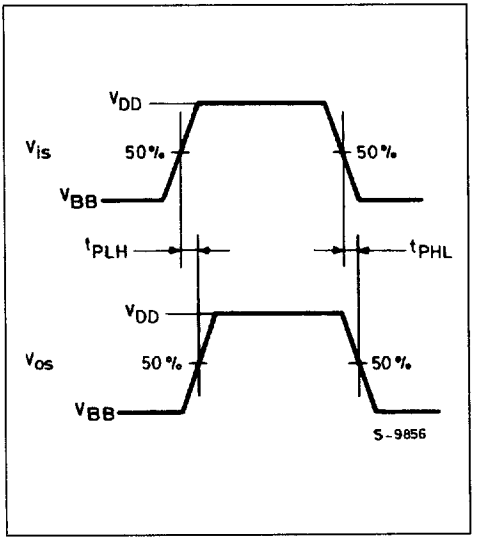


Figure 4 : Crosstalk Measurements.

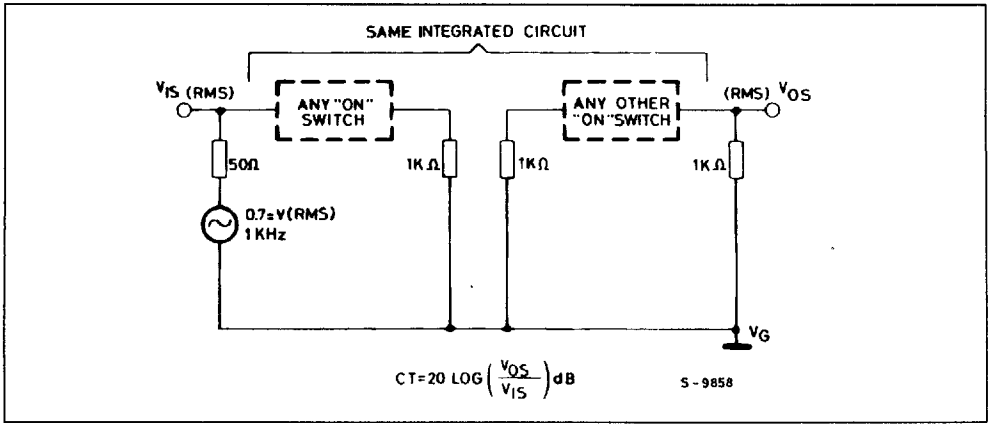


Figure 5 : Propagation Delay Time and Waveforms (strobe to signal output switch Turn-ON or Turn-OFF).

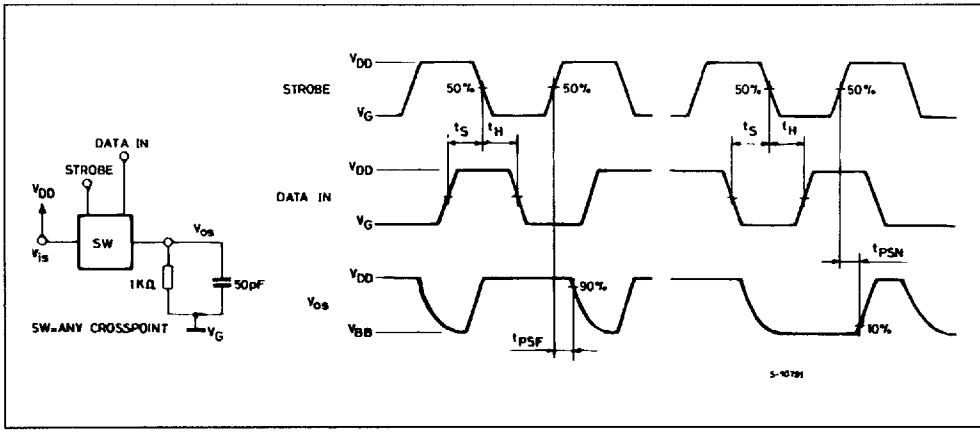


Figure 6 : Propagation Delay Time and Waveforms (data-in signal output, switch Turn-ON to high or low level).

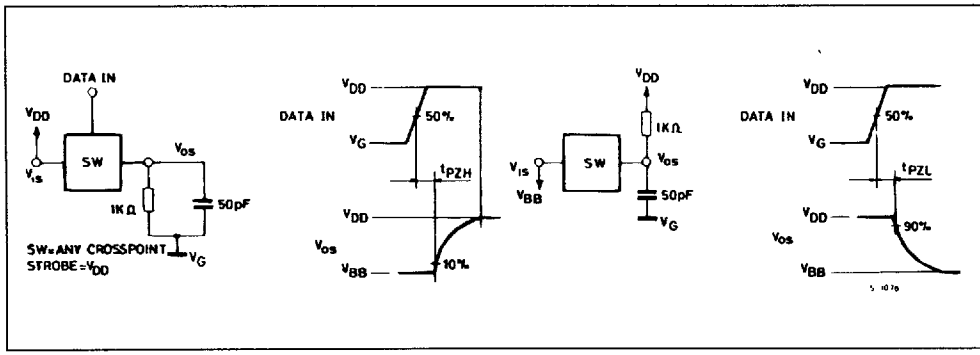


Figure 7 : Propagation Delay Time and Waveforms (address to signal output switch Turn-ON or Turn-OFF).

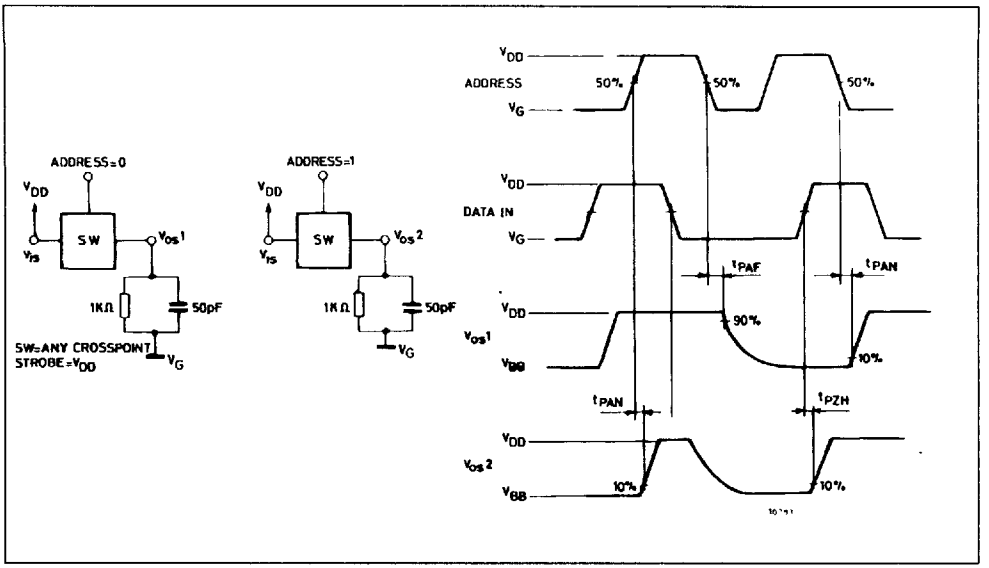


Figure 8 : Waveforms for Crosstalk (control input to signal output).

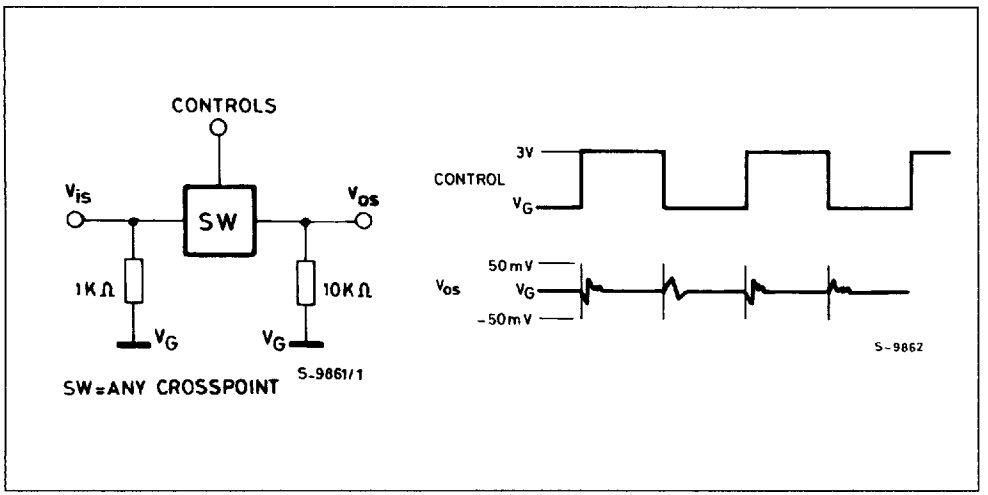


Figure 9 : Propagation Delay Time and Waveforms (reset to output delay).

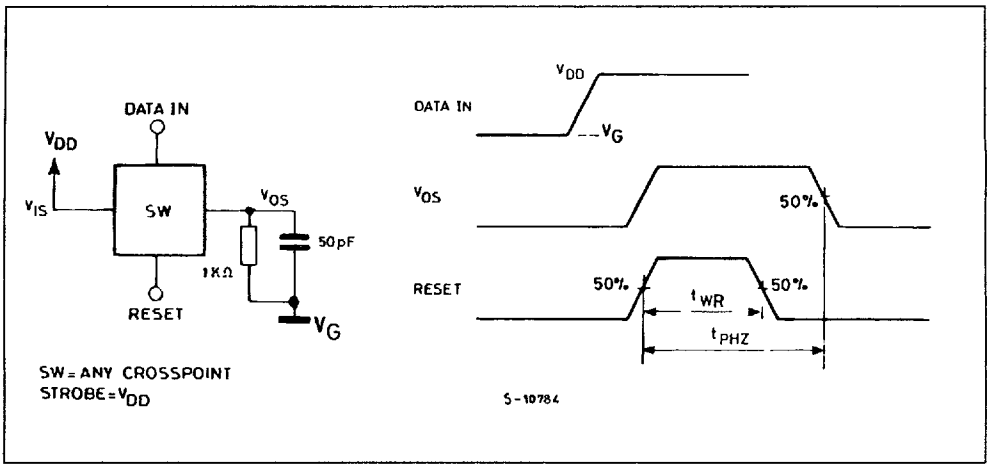


Figure 10 : Propagation Delay Time and Waveforms (Strobe and C/S to signal output switch).

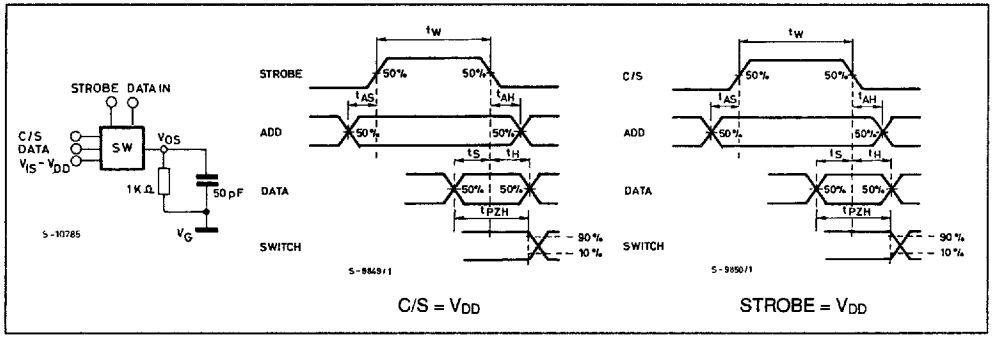


Figure 11 : Typical R_{ON} versus V_{IS}.

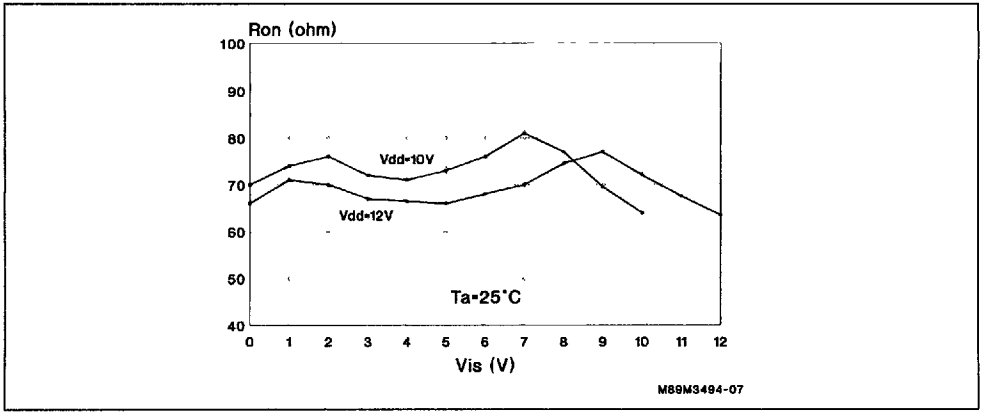


Figure 12 : Peak to Peak Voltage Capability versus Total Harmonic Distortion.

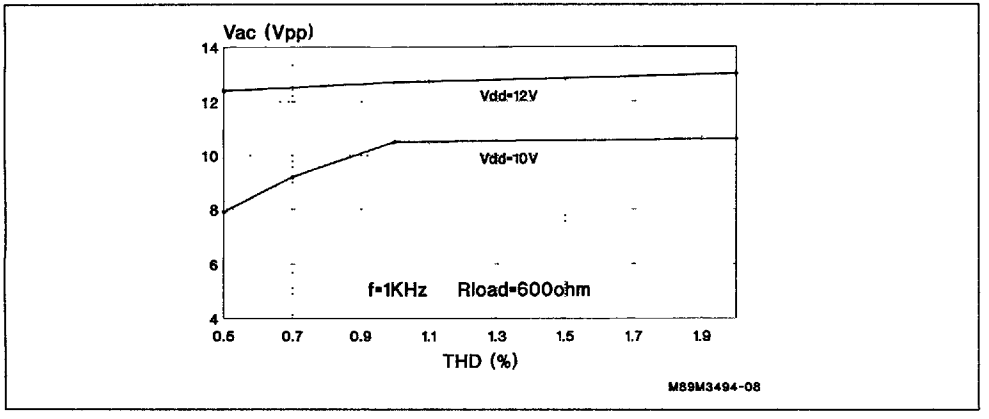
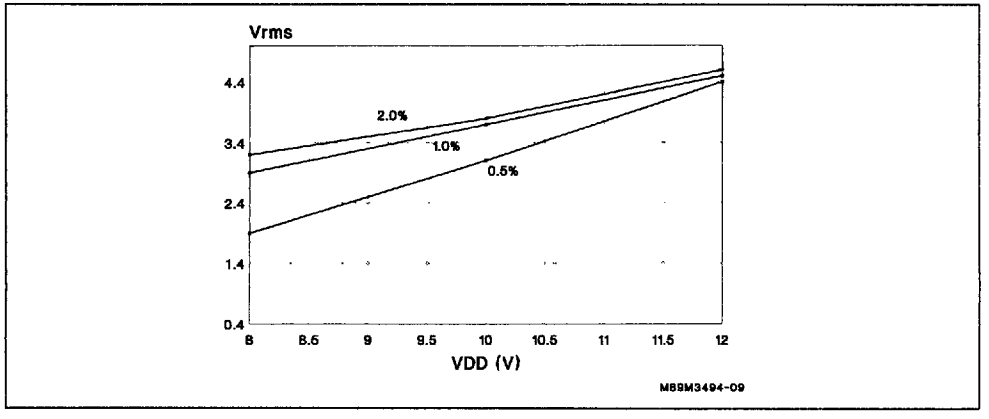


Figure 13 : V_{RMS} Capability versus V_{DD}.



TYPICAL APPLICATIONS

The figures 14, 15 and 16 show the system configuration for expanded matrices (16 x 16, 8 x 64, 32 x 32).

Figure 14 : (16 x 16 non blocking matrix).

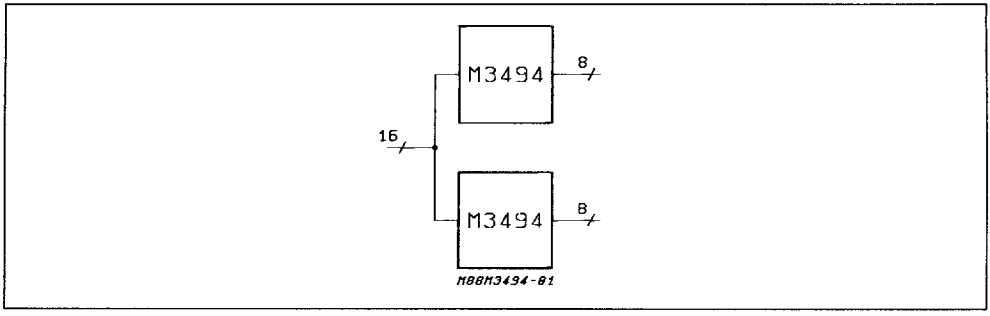


Figure 15 : (8 x 64 matrix).

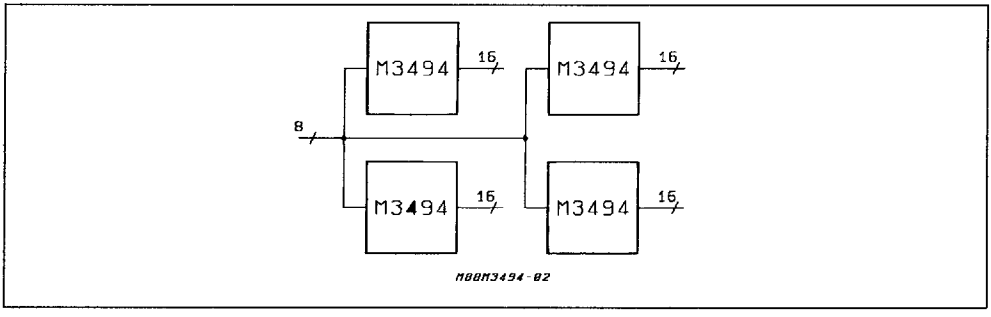
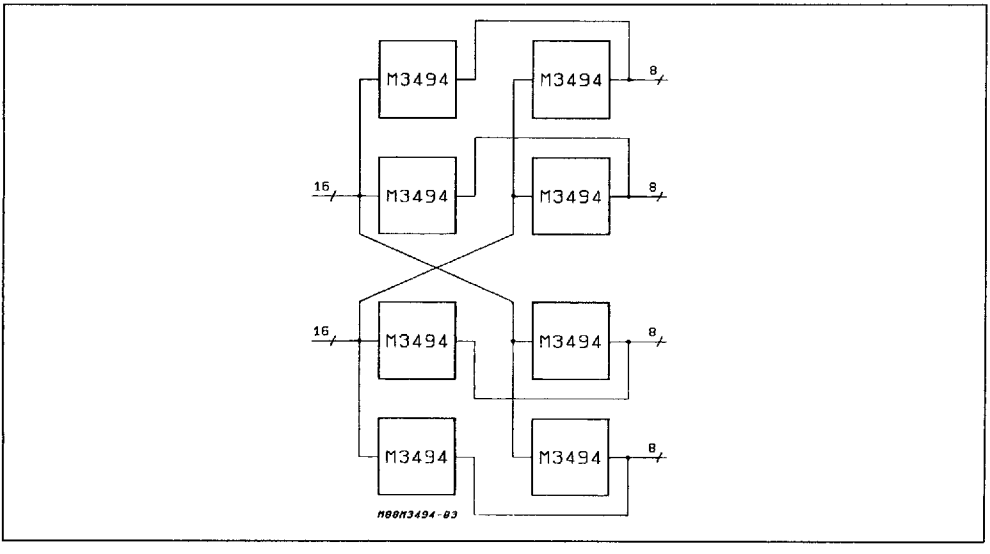


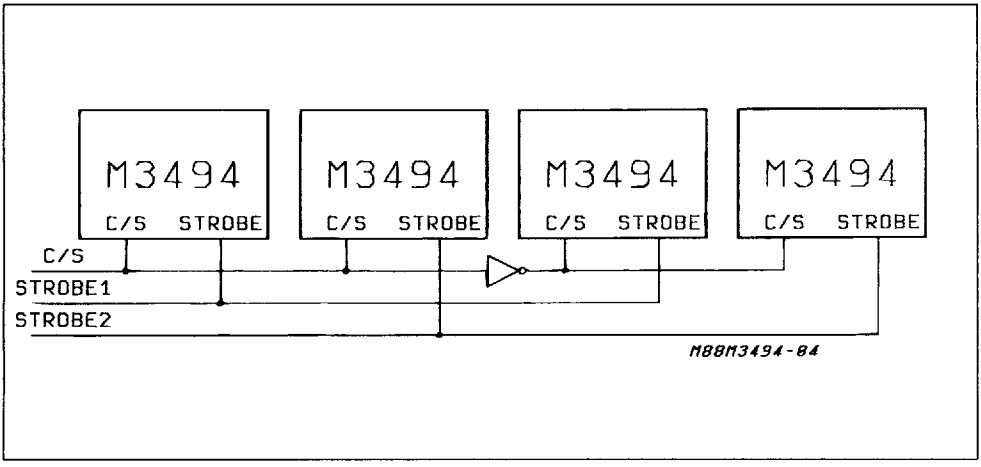
Figure 16 : (32 x 32 non blocking matrix).



The availability of the C/S input in addition of the STROBE input aids the addressing circuit for expanded matrices.

Fig. 17 shows an example, the selection circuit for a matrix with 4 x M3494 that implement this function with only one extenal inverter.

Figure 17.



Note : The Reset, Data and Address inputs are connected in parallel.