YAMAHA

YDA131

D-1

STEREO 2.5W DIGITAL AUDIO POWER AMPLIFIER

■Outline

The YDA131 is the high efficient digital audio power amplifier IC that operates on a single 5V power supply.
This IC is capable of providing output power of 2.5W/channel, which is at the highest level as a device on a single 5V power supply. By adopting Yamaha's proprietary modulation system, the device provides low distortion and high signal to noise ratio at the highest level among digital amplifiers in the equivalent class.
This IC accepts analog signal, converts it into digital pulse by the digital modulation circuitry and outputs the signal from the large current capacity buffers. The digital pulse signal that is outputted from the output buffer is converted into audio signal through an external low pass filter, and sent to the speakers.
This IC has the overcurrent detection function that detects short-circuiting of speaker terminal end and the high temperature detection function that detects abnormal high temperature.
With the overcurrent detection function, this IC generates a warning signal when the current that flows in the output buffers of left and right channels exceeds a fixed value. With the high temperature detection function, this IC generates a warning signal when the junction temperature becomes abnormal.
Furthermore, this IC builds in function that mute an audio output and shut off all functions of the IC. By this function, power consumption is restrained at the minimum.

■Features

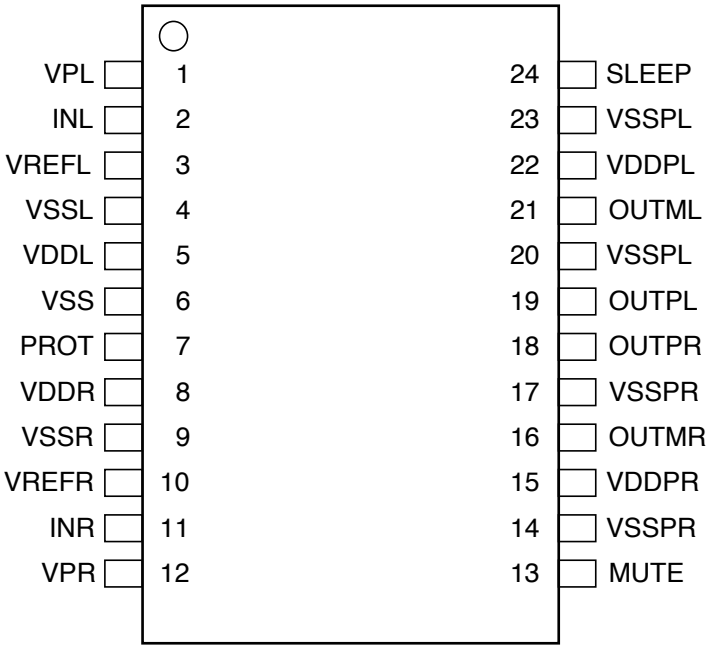
- High output power
  2.5 W VDD=5.0V, 4Ω (THD+N<10%)
- High efficiency operation
  85 % VDD=5.0V, R_L=8Ω
  75 % VDD=5.0V, R_L=4Ω
- Low distortion(THD+N)
  0.018 % Po=1.0W, 1kHz, R_L=4Ω
- High signal to noise ratio
  103dB VDD=5.0V, Input sensitivity =1.0V, R_L=4Ω
  97dB VDD=5.0V, Input sensitivity=150mV, R_L=4Ω
- Low consumption current
  14.0 mA VDD=5.0V, no signal(no filter)
  7.0 mA VDD=5.0V, at mute
  1 μA VDD=5.0V, at sleep
- Channel separation
  80dB 1kHz
- Any gain setting by external resistor
- Any setting of starting time by VREF capacitor
- Sleep function by SLEEP terminal
- Output mute function by MUTE terminal
- Over current detection function of speaker terminal end (Ground short-circuiting, Load short-circuiting)
- High temperature detection function
- Pop noise suppression function at turn-on and turn-off
- Analog input/BTL(Bridge-Tied Load)output
- 24-pin plastic SSOP (YDA131-E)

YAMAHA CORPORATION

YDA131CATALOG
CATALOG No.:LSI-4DA131A3
2003.1

■ Terminal configuration

YDA131-E



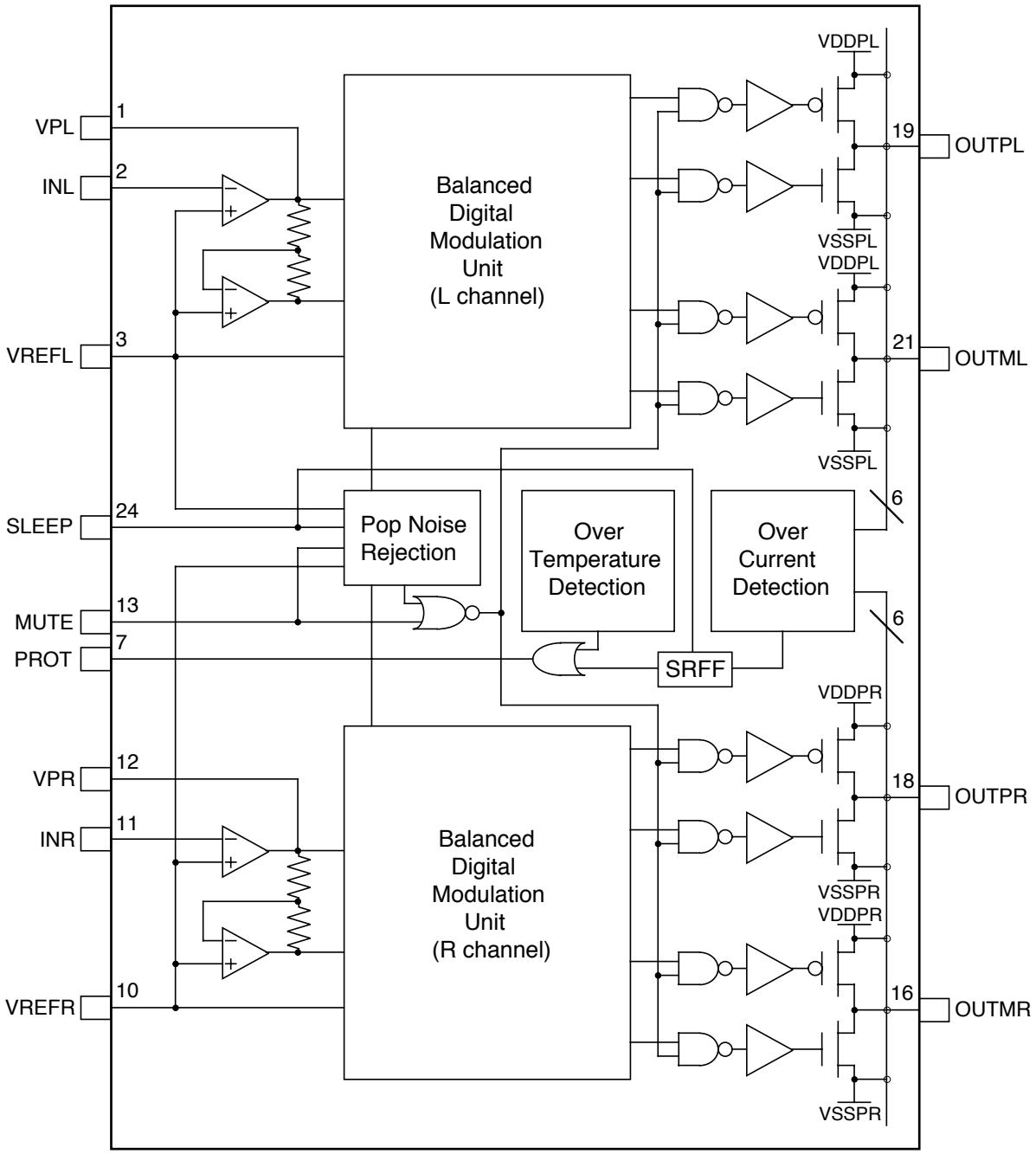
＜24 pin SSOP Top View＞

■ Terminal functions

No.	Name	I/O	Function
1	VPL	AO	Lch gain control
2	INL	AI	Lch audio input
3	VREFL	AO	Lch voltage reference
4	VSSL	—	VSS for analog circuit of Lch
5	VDDL	—	VDD for analog circuit of Lch
6	VSS	—	VSS for control circuit and protection circuit
7	PROT	O	Warning output for protection function
8	VDDR	—	VDD for analog circuit of Rch
9	VSSR	—	VSS for analog circuit of Rch
10	VREFR	AO	Rch voltage reference
11	INR	AI	Rch audio input
12	VPR	AO	Rch gain control
13	MUTE	I	Output shut off control
14	VSSPR	—	VSS for output buffer of Rch
15	VDDPR	—	VDD for output buffer of Rch
16	OUTMR	O	Negative output of Rch
17	VSSPR	—	VSS for output buffer of Rch
18	OUTPR	O	Positive output of Rch
19	OUTPL	O	Positive output of Lch
20	VSSPL	—	VSS for output buffer of Lch
21	OUTML	O	Negative output of Lch
22	VDDPL	—	VDD for output buffer of Lch
23	VSSPL	—	VSS for output buffer of Lch
24	SLEEP	I	Operation shut off control

Note. A: Analog terminal

■ Internal block diagram



■ Description of terminal functions

VDDPL, VSSPL, VDDPR, VSSPR (Terminal No.22, 20&23, 15, 14&17)
These are the power supply and ground terminals for the output buffers.
VDDPL and VSSPL are the power supply and ground terminals for the left channel, and VDDPR and VSSPR are the power supply and ground terminals for the right channel.
There are two VSSPL terminals and two VSSPR terminals, both of which are to be connected with similar impedance (length of patterns on the printed circuit board).

OUTPL, OUTML, OUTPR, OUTMR (Terminal No.19, 21, 18, 16) [Digital-OUT]
These are the output buffer terminals and output digital pulse signal that has been modulated by PWM system.
OUTPL and OUTML are the output buffer terminals for the left channel, OUTPL is the positive terminal and OUTML is the negative terminal.
OUTPR and OUTMR are the output buffer terminals for the right channel, OUTPR is the positive terminal and OUTMR is the negative terminal.
Since both channels are BTL (Bridge-Tied Load) output, the minus terminal is not at the ground potential.
Connect the IC with the speakers through an LC filter as shown in the "Application circuit" for the purpose of removing the carrier frequency signal.

VDDL, VSSL, VDDR, VSSR (Terminal No.5, 4, 8, 9)
These are the power supply and ground terminals for the circuitries other than the output buffers.
VDDL and VSSL are the power supply and ground terminals for the left channel circuit.
VDDR and VSSR are the power supply and ground terminals for the right channel circuit.

VSS (Terminal No.6)
This is the ground terminal for the protection circuitry and the control circuitry.
Connect VSS to the left-channel analog ground near the terminal.

INL, VPL, INR, VPR (Terminal No.2, 1, 11, 12) [Analog]
These are the audio signal input and gain adjustment terminals.
INL and VPL are the audio signal input and gain adjustment terminals for the left channel.
INR and VPR are the audio signal input and gain adjustment terminals for the right channel.
The terminals are connected respectively to the inversion input and output of the first stage inversion operational amplifiers. The amplifier gain is set by connecting an input resistor and a feedback resistor to both terminals as shown the "Application circuit". The use of this inversion operational amplifier allows making a simple filter.
For the details, refer to "Gain setting" on page 6.

VREFL, VREFR (Terminal No.3, 10) [Analog]
These are reference voltage output terminals.
VREFL is the reference voltage output terminal for the left channel, and VREFR is the reference voltage output terminal for the right channel. Connect the same capacitors to these terminals. The starting time is set by changing the capacitance connected to VREFL and VREFR terminals.
For the details, refer to "Pop noise reduction function" on page 9.

SLEEP (Terminal No.24) [Digital-IN]
This is the operation shut off control terminal.
The terminal controls both channels at the same time. When SLEEP terminal is set at "H" level, all of the internal circuits are placed in the shut off state, output is placed in the muted state, and the IC is placed in the sleep state. At this time the power consumption is minimized, and warning signal (PROT terminal output) is set at "L" level.
When SLEEP terminal is set at "L" level, this IC goes into normal operation after sufficient time (starting time) to make each reference voltage reaches a fixed potential.

MUTE (Terminal No.13) [Digital-IN]
This is the output shut-off control terminal.
The terminal controls both channels at the same time. When MUTE terminal is set at "H" level, all of the output buffer terminals, OUTPL, OUTML, OUTPR and OUTMR output "L" level, and this IC changes in mute state.
When MUTE terminal is set at "L" level, all of the output buffer terminals, OUTPL, OUTML, OUTPR and OUTMR output the digital pulse signal.

PROT (Terminal No.7) [Digital-OUT]
This is the warning signal output terminal for both overcurrent detection and high temperature detection.
PROT terminal outputs "H" level when either of those detection circuitries detects a hazardous state.
For the method of controlling MUTE terminal and SLEEP terminal by using PROT terminal, refer to "Overcurrent detection function and high temperature detection function" on page 7.

■ Description of operation functions

Refer to "Connection circuit example" on page 11, when reading the following descriptions.

■ Gain setting

This IC consists of the first stage inversion operational amplifier, and the fixed-gain digital power amplifier.
The gain of the digital power amplifier is fixed at 8 dB.
The gain of the first stage inversion operational amplifier is set with the resistance values of the input resistor (R_I) and feedback resistor (R_F) as described by "Formula 1". To reduce pop noise, it is necessary to observe the restrictions described in "Pop noise reduction function" on page 9. Use the feedback resistor (R_F) of 10kΩ or higher, because the driving capability of the operational amplifier is limited.
In "Application circuit", input resistor (R_I)=7.5kΩ and feedback resistor (R_F)=47kΩ and the gain of the first stage inversion operational amplifier is set at 16 dB, as described in "Figure 1: First stage inversion operational amplifier input circuit example". Therefore, the total gain at this case is given as described below.

8dB (fixed gain of the digital power amplifier) + 16dB (gain of the first stage inversion operational amplifier) = 24dB

In the "Application circuit", low pass filter capacitor (C_F) is added to limit the band width of the input signal, as described in "Figure 1: First stage inversion operational amplifier input circuit example", whereby the value can be adjusted as necessary. To limit the input DC current, DC cutting capacitor (C_I) is added, whereby this capacitor and input resistor (R_I) constitute a high pass filter.
The cut off frequency fc of this high pass filter is set as necessary, and can be decided by "Formula 2".

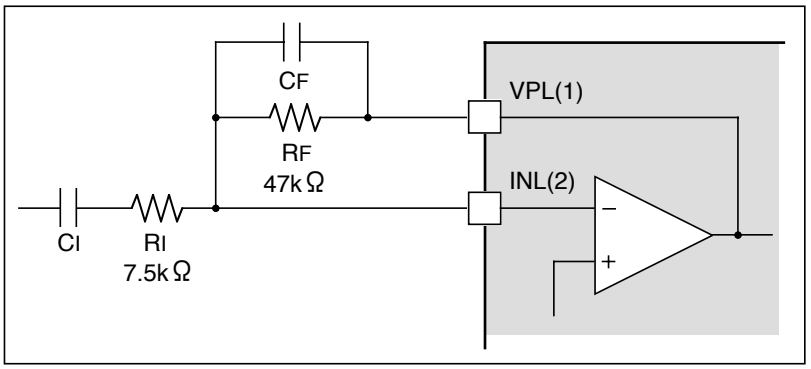


Figure 1: First stage inversion operational amplifier input circuit example

Formula 1: Gain of first stage inversion operational amplifier Av(dB) = 20*log(R_F/R_I)

Formula 2: Cut off frequency fc(Hz) = 1/(2*π*R_I*C_I)

When low band boost function is needed due to a reason such as small diameter speaker, the low boost function can be realized by making the circuit of the first stage operational amplifier as shown in "Figure 2: Low band boost circuit example". For this circuit, the gain is increased by +3dB at the frequency fb of "Formula 3", and the low band boost quantity Ab is decided by "Formula 4". At this time, the frequency characteristic is as shown in "Figure 3: Frequency characteristic at low band boost".

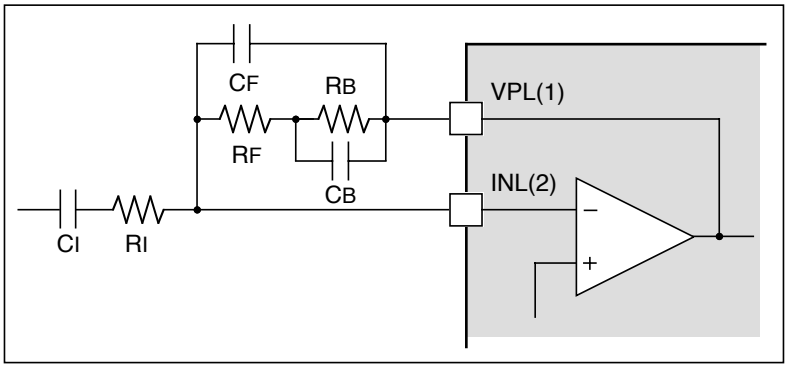


Figure 2: Low band boost circuit example

Formula 3: Frequency at which the gain increased by +3dB fb(Hz) = 1/(2*π*R_F*C_B)

Formula 4: Boost quantity Ab(dB) = 20*log((R_F+R_B)/R_F)

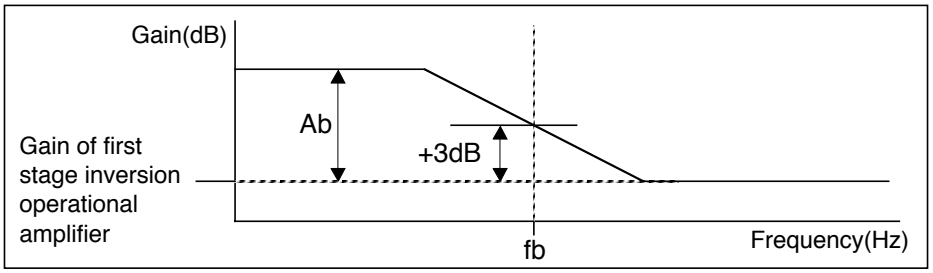


Figure 3: Frequency characteristic at low band boost

■ Mute function

When MUTE terminal is set at "H" level, all of the output buffer terminals, OUTPL, OUTML, OUTPR and OUTMR, output "L" level, and this IC changes into mute state. When MUTE terminal is set at "L" level, all of the output buffer terminals, OUTPL, OUTML, OUTPR and OUTMR, output digital pulse signal.
This IC includes a pop noise reduction function circuitry in both cases the mute control is enabled and disabled.
In the mute mode, the overcurrent detecting function is disabled. However, all the output buffers outputting "L" level, the electric current is at a safe level even if the buffer terminals are short-circuited.

■ Sleep function

When SLEEP terminal is set at "H" level, all of the internal circuitries are placed in the shut-off state, output is placed in the mute state, and this IC is placed in the sleep state. In this state, the power consumption is minimized, overcurrent detection function and high temperature detection function are disabled, and warning signal (PROT terminal output) is set at "L" level.
When SLEEP terminal is set at "L" level, this IC goes into normal operation state after sufficient time (starting time) to make each reference voltage reaches an established potential.
This IC includes a pop noise reduction function in both cases the sleep control is enabled and disabled.

■ Overcurrent detection function and high temperature detection function

This IC includes the output buffer overcurrent detection function and high temperature detection function. When either detection circuit detects an abnormality, warning signal (PROT terminal) output is set at "H" level.

Overcurrent detection function

When either of four speakers terminal end (between LC filter and speaker) short-circuits with VSS terminal or reverse polarity speaker terminal end, this IC determines that the overcurrent state has occurred and outputs warning signal (PROT terminal ="H" level).
When a warning is signaled, MUTE terminal or SLEEP terminal should be controlled externally to place this IC in the muted state or sleep state immediately to protect this IC.
And it does not cope with over current protection that short-circuiting of output terminals (OUTPL, OUTML, OUTPR, OUTMR) and VSS terminal, and short-circuiting between each output terminal.
When the warning signal (PROT terminal ="H" level) is outputted due to overcurrent detection, this IC keeps the warning signal output after the current return to normal state.
The warning signal is cancelled by changing the state of SLEEP terminal as "L" level, "H" level and "L" level in this order or by turning on the power supply again.

When this IC is used with application that speaker terminal is likely to short-circuit during operation, use the following over current detection and protection circuit.

(1) Connecting PROT terminal output to MUTE terminal.
When an overcurrent is detected, the output goes into mute state. In this case, warning signal output and mute state cannot be cancelled unless otherwise the power supply is turned on again or the state of SLEEP terminal is changed as "L" level, "H" level and "L" level in this order.

(2) Attaching a fall delay circuit to PROT terminal, and connecting it to SLEEP terminal.
For the connection, refer to "Figure 4: PROT terminal output connection circuit example" in the following "Restrictions" section.
When overcurrent is detected, this IC goes into sleep state, and the output goes into mute state, and warning signal output is cancelled. The sleep state is cancelled after the elapse of the fall delay time, and return to normal operation.
If the overcurrent state remains even after the restart, the sleep and start are repeated.

(3) If the current capacity of used power supply exceeds 1.5A, connect shottkey-diode between output terminals (OUTPL, OUTML, OUTPR, OUTMR) and VSS, and connect between PROT and MUTE terminal or SLEEP terminal as (1), (2).

■ High temperature detection function

When this IC operates with its internal temperature exceeding the maximum rating (junction temperature), it determines itself as a high temperature state, and outputs the warning signal (PROT terminal ="H" level).
When a warning is signaled, MUTE terminal or SLEEP terminal should be controlled externally to place this IC in muted state or sleep state immediately to protect this IC. If the internal overheating is due to the overload output, the temperature rise is avoided by aforesaid control.
When the warning signal is generated due to the high temperature detection, and then, the temperature is reduced sufficiently by the protection action with the control of MUTE terminal or SLEEP terminal, this IC cancels the warning signal. The warning signal is also cancelled by setting the state of SLEEP terminal at "L" level or by turning on the power supply again.
The control through the use of PROT terminal, MUTE terminal or SLEEP terminal is made also for the case of high temperature detection like the case of the overcurrent detection.
In case of high temperature detection, this IC cancels the warning signal if the temperature is reduced sufficiently. Thus, this IC can return to the normal operation even if PROT terminal and MUTE terminal are connected.

■ Restrictions

A pulse as short as about 1μs may be outputted from PROT terminal when the power supply is turned on or the state of SLEEP terminal is changed from "H" level to "L" level.
When this IC is controlled using SLEEP terminal and PROT terminal, connect an LPF (low pass filter) that can cut pulse about 10μs to PROT terminal.
"Figure 4: PROT terminal output connection circuit example" is the connection circuit example for the case LPF (low pass filter) and fall delay circuit are attached to PROT terminal and connected to SLEEP terminal.

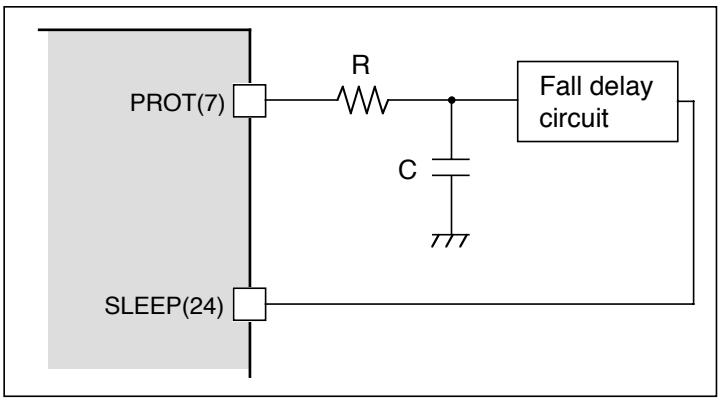


Figure 4: PROT terminal output connection circuit example

■ Pop noise reduction function

This IC includes pop noise reduction function that works when turning on and shutting off the power supply, and controlling the mute or sleep functions.

When turn on the power supply

This IC is in mute state immediately after turning on the power supply.
The starting process is performed at the power on (sleep cancellation), and after the internal operation stabilizes, the mute state is cancelled. This operation minimizes the generation of pop noise at turning on the power supply.
To make this function operate effectively, it is necessary to use the input resistor "RI" of the first stage inversion operational amplifier, the input AC coupling capacitor "CI" of the first stage inversion operational amplifier, and reference voltage stabilizing capacitor "CR1" under the following condition.
These values must be same for both channels.

Condition: CR1 > (RI * CI)/5000

To make the pop noise reduction function operate effectively when turning on the power supply, the capacitors (CR1) of VREFL and VREFR terminals must be discharged sufficiently before turning on the power supply again. If you turn on the power supply again without discharged sufficiently these capacitors, this function does not operate effectively, and there is a possibility that pop noise generates.

Starting time

Starting time is a period for each reference voltage to reach the specified potential (for charging capacitors (CR1) of VREFL and VREFR terminals) when the power supply is turned on or is turned on again. This period varies in relation to the capacitance (CR1) of VREFL and VREFR terminals.
The table of starting time is as follows:

Table: Starting time

CR1capacitor(μF)	Starting time (sec)
2	0.13
10	0.33
30	0.85
50	1.40

When shutting off the power supply

This IC performs muting processing internally when the power supply voltage has changed by more than10% in a very short period or when the power supply voltage is reduced below 3.0V to reduce the pop noise when the IC is shut off.
To make this function operate efficiently, it is necessary to fall the power voltage quickly when shutting off the power supply.
When the power is supplied to the IC through a voltage regulator and a large capacitance is connected after the regulator, such as the case shown in "Figure 5: Power supply fall acceleration circuit example", the voltage of VDD can be reduced quicker if a diode is connected to it.

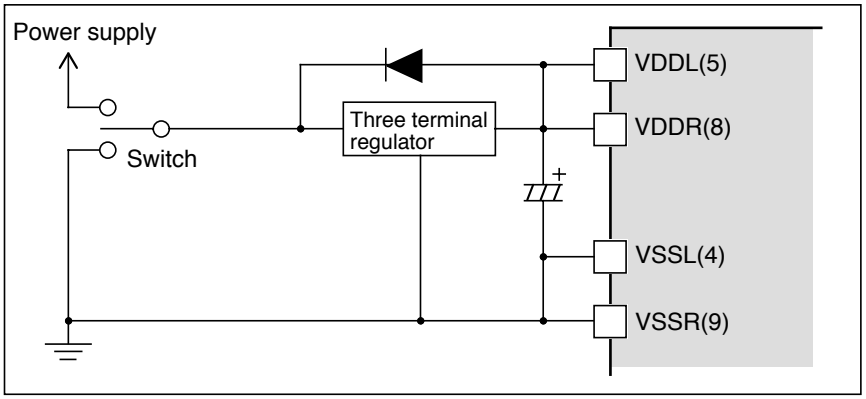


Figure 5: Power supply fall acceleration circuit example

If power supply voltage changes exceeding 10% in a very short period, this IC may go into mute state internally due to the pop moise reduction function described before. Therefore, it is recommended to use this IC in normal operation so that the change of power supply voltage in a very short period wouldn't exceed 10%.
This IC may also go into mute state internally when the power supply voltage is reduced temporarily below 3.0V. Therefore, it is recommended to use this IC in normal operation so that the power supply voltage wouldn't fall below 3.0V.

■ Power consumption

This IC is capable of outputting up to 5W in total, or 2.5W per one channel. Digital amplifiers can be used without heat sink because their operation efficiency is higher than conventional linear amplifiers.
When using this IC, ensure that the power consumption does not exceed the maximum allowable loss that is defined as the absolute maximum rating.
The power consumption of this device can be obtained by using "Formula 5".
In the following formula, P_D represents the power consumption, Po represents average output power, R_L represents the output load impedance, and Pic represents the internal control circuit loss.

Formula 5: $P_D(W) = Po(W) * 1.05 / R_L(\Omega) + Pic(W)$

$Pic = 0.09W$ (VDD=5.0V)
$Pic = 0.04W$ (VDD=3.3V)

The maximum allowable loss $P_D max$ is obtained by using "Formula 6" based on the absolute maximum rating of the junction temperature of this IC.
In the following formula, Tjmax represents the absolute maximum rating of the junction temperature, θja represents thermal resistance of SSOP24 package, and Ta represents the ambient temperature.

Formula 6: $P_D max(W) = (Tjmax(°C) - Ta(°C)) / \theta ja$

$\theta ja = 96.7°C/W$
$Tjmax = 125$

For example, when VDD=5.0V, output load=4Ω, and 2.5W X 2ch is outputted continuously, the maximum allowable loss is exceeded. However, this IC can deal with reproduction of normal music signal sources sufficiently because it is believed to be sufficient that average output power of the normal music signal sources is estimated at 1/8 of the maximum output.

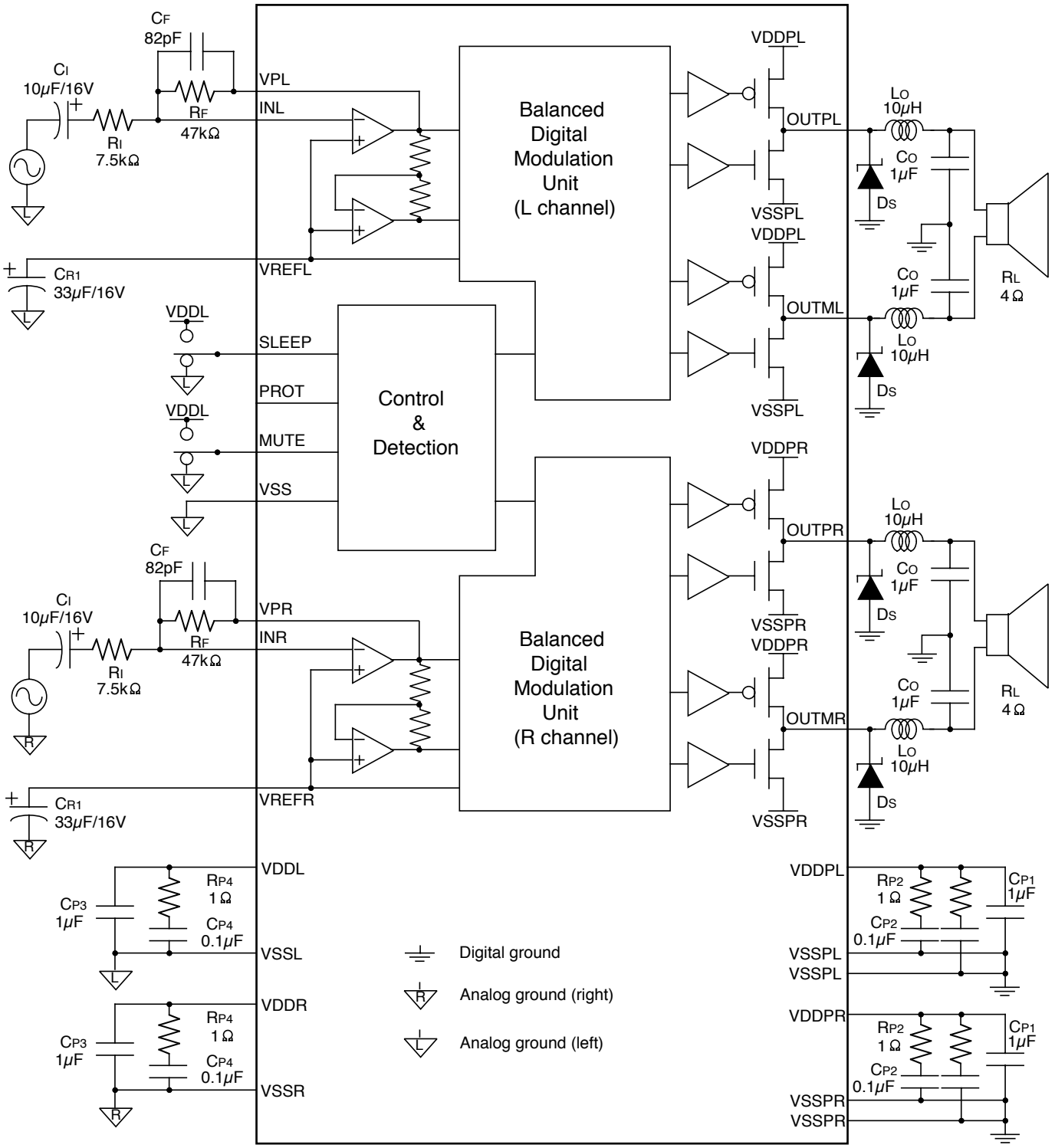
■ Load impedance and filter constant

The speaker that is connected to this IC is to have the load impedance (R_L) of 4Ω or higher.
Typical filter constants for load impedance (R_L) when the cut-off frequency is set at 50kHz are as shown in the following table.

Table: Filter constant example

Load impedance R_L	L	C
4Ω	10μH	1μF
8Ω	22μH	0.47μF
16Ω	39μH	0.27μF

■ Application circuit



Outline of components that are connected externally to this IC.

C_{P1}, C_{P3}	Capacitors for stabilization of the power supply
C_{P2}, C_{P4}, R_{P2}, R_{P4}	Capacitors and resistors for stabilization of the power supply (snubber)
C_{R1}	Capacitor for stabilization of reference voltage, and capacitor for stabilization of starting.
C_I	Input AC coupling capacitor: R_I and C_I form a high pass filter.
R_I	Inversion input resistor that determines the gain.
R_F	Feedback resistor for determining the gain.
C_F	Capacitor for input low pass filter.
L_O	Output inductance: Being combined with C_O, the component forms the secondary filter that removes the high frequency and delivers an amplified audio signal to the load.
C_O	Output capacitor
D_S	Shottkey-diode for terminal protection (equivalent to 11EQS04)

■ Electrical characteristics

1. Absolute maximum rating

Item	Symbol	Rating	Unit
VDD terminal power supply voltage *1	V_{DD}	V_{SS} -0.5~V_{SS} +6.0	V
Digital input terminal voltage	V_{DIN}	V_{SS} -0.5~V_{DD}+0.5	V
Analog input terminal voltage	V_{AIN}	V_{SS} -0.5~V_{DD}+0.5	V
Storage temperature	T_{STG}	-50~125	°C
Maximum allowable loss (Ta=70°C)	P_{D70}	568	mW
Maximum allowable loss (Ta=25°C)	P_{D25}	1034	mW
Junction temperature	T_{jmax}	125	°C

Note. *1:V_{DD} covers all of VDD terminals, including VDDPL, VDDPR, VDDL and VDDR.
V_{SS} covers all of VSS terminals, including VSSPL, VSSPR, VSSL, VSSR and VSS.

2. Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.15	5.0	5.25	V
Operating ambient temperature (ambient temperature Ta)	T_{OP}	0	25	70	°C
Output load impedance	R_L	4			Ω

3. DC characteristics (V_{DD}=5V±0.25V, Ta=0~70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage "H" level	V_{OH}	I_{OH}= -80μA、PROT terminal	V_{DD}-1.0			V
Output voltage "L" level	V_{OL}	I_{OH}= 1.6mA、PROT terminal			V_{SS}+0.4	V
Input voltage "H" level	V_{IH}	SLEEP, MUTE terminal	3.5			V
Input voltage "L" level	V_{IL}	SLEEP, MUTE terminal			1.0	V
Consumption current 1	I_{DD1}	at SLEEP mode		1		μA
Consumption current 2	I_{DD2}	at MUTE mode		7		mA
Consumption current 3	I_{DD3}	no signal, no filter		14		mA

Note. These values do not guarantee the characteristics at V_{DD}=3.3V±0.15V.

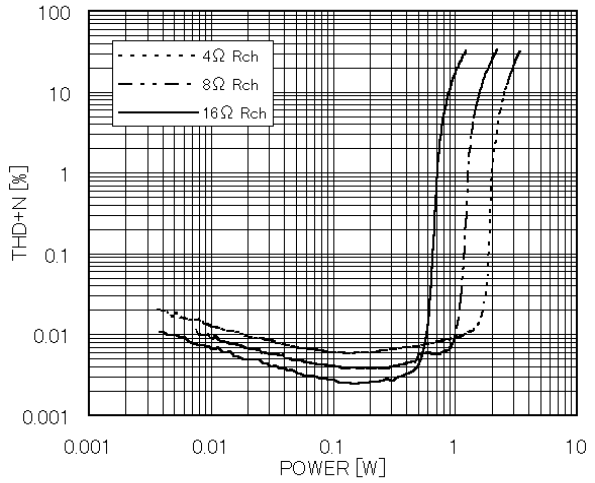
4. Analog characteristics（V_{DD}=5.0V, Ta=25°C, Frequency=1kHz）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum output	P_O	THD+N=10%, R_L=4Ω		2.5		W
Voltage gain (R_I=7.5kΩ, R_F=47kΩ)	A_V	R_L=4Ω		24		dB
Total harmonic distortion (20kHz Band Width)	THD+N	R_L=4Ω, Po=1.0W		0.018		%
Signal/noise ratio (A-Filter)	SNR	Input sensitivity 1.0V R_L=4Ω Input sensitivity 150mV R_L=4Ω		103 97		dB dB
Channel separation	CS	R_L=4Ω		80		dB
Maximum efficiency	η	R_L=8Ω R_L=4Ω		85 75		% %
Output offset voltage	V_O	R_L=4Ω		6		mV

Note. All the analog characteristics shown above are the values obtained on the DMB-D1, Yamaha's YDA131 evaluation board.
The characteristics may vary according to the coils and capacitors that are used, pattern layout and other factors.
These values do not guarantee the characteristics at V_{DD}=3.3V±0.15V.

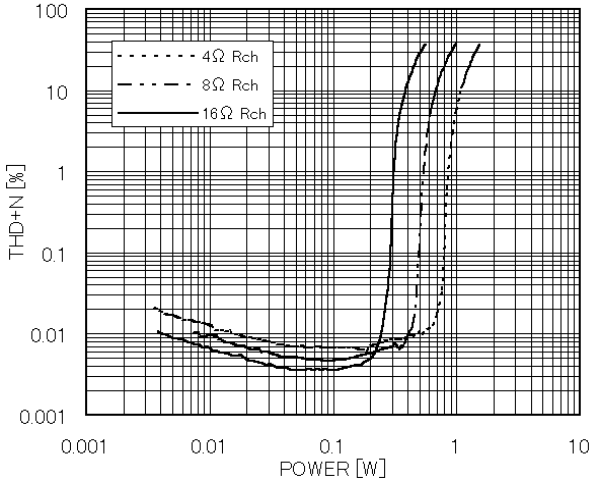
■ Characteristics example

POWER - THD+N (VDD=5.0V)



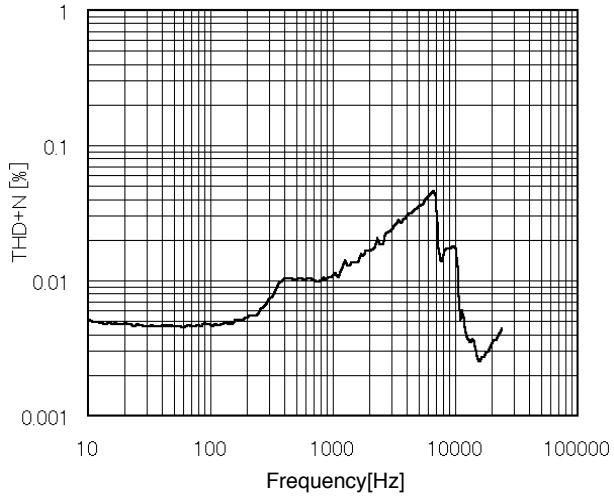
f=1kHz RI=22kΩ RF=22kΩ 20kHzLPF

POWER - THD+N (VDD=3.3V)



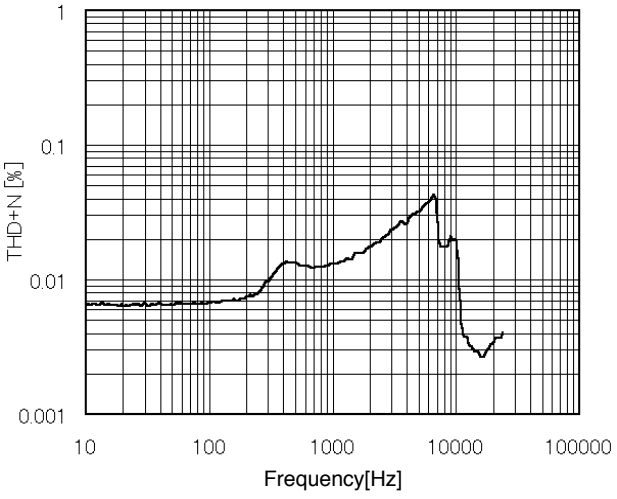
f=1kHz RI=22kΩ RF=22kΩ 20kHzLPF

Frequency - THD+N (VDD=5.0V)



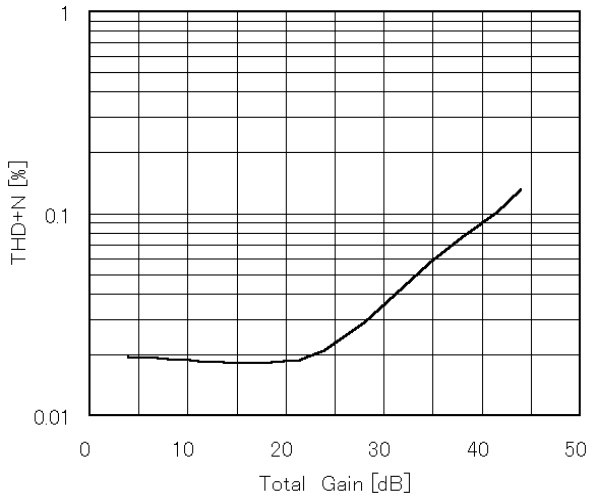
PO=1.0W RI=22kΩ RF=22kΩ RL=4Ω 20kHzLPF

Frequency - THD+N (VDD=3.3V)



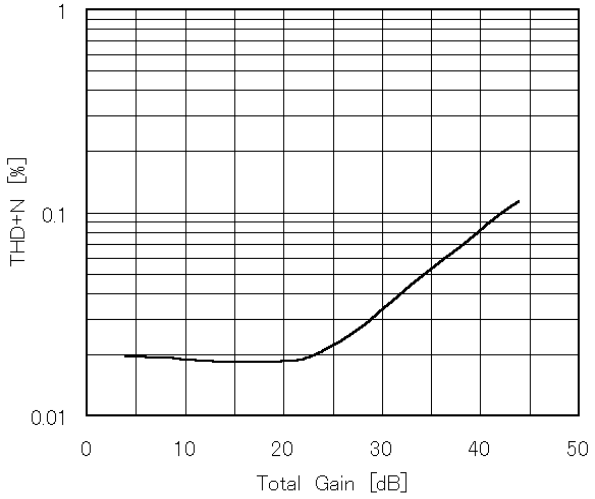
PO=0.5W RI=22kΩ RF=22kΩ RL=4Ω 20kHzLPF

Gain - THD+N (VDD=5.0V)



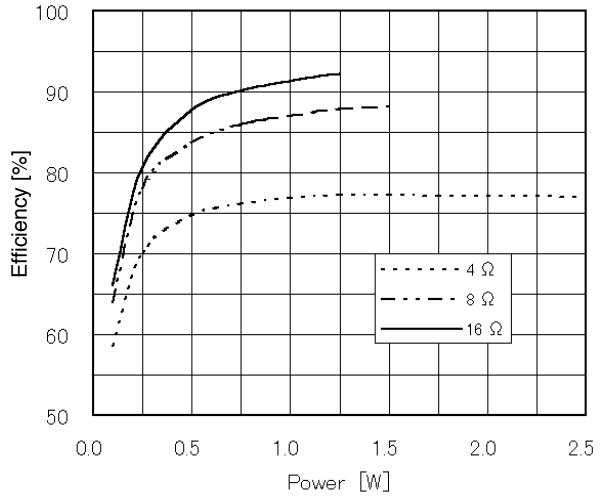
PO=1.0W f=1kHz RL=4Ω 20kHzLPF

Gain - THD+N (VDD=3.3V)



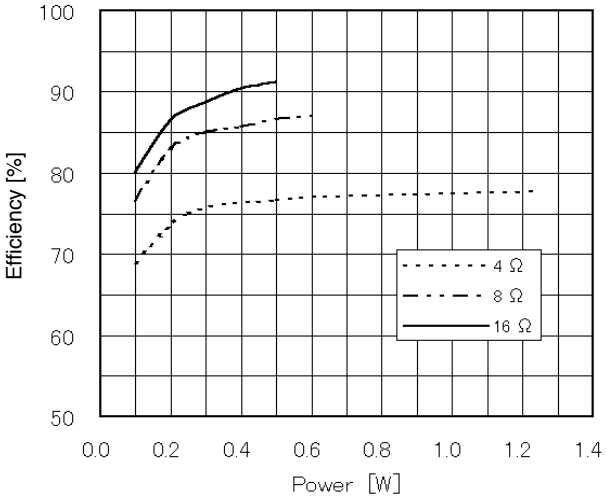
PO=0.5W f=1kHz RL=4Ω 20kHzLPF

Efficiency - Power [VDD=5.0V]



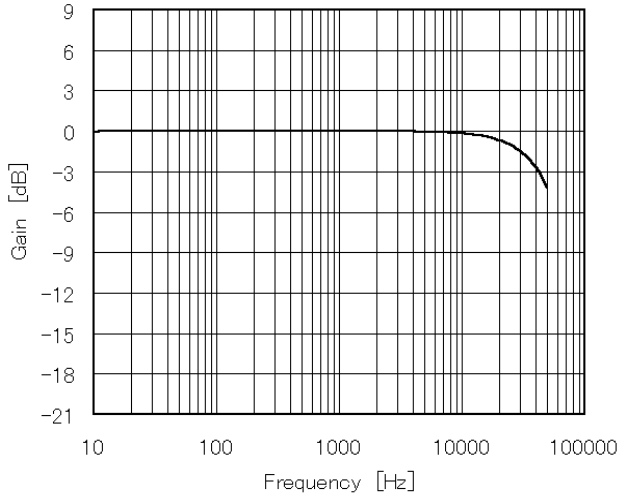
f=1kHz VDD=5.0V

Efficiency - Power [VDD=3.3V]



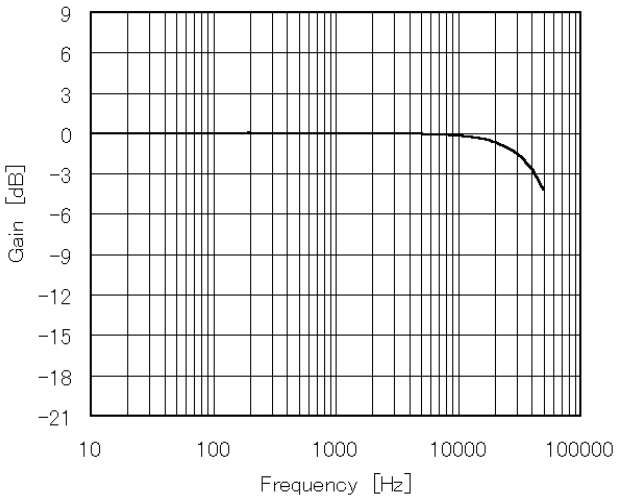
f=1kHz VDD=3.3V

Frecuency characteristics [VDD=5.0V]



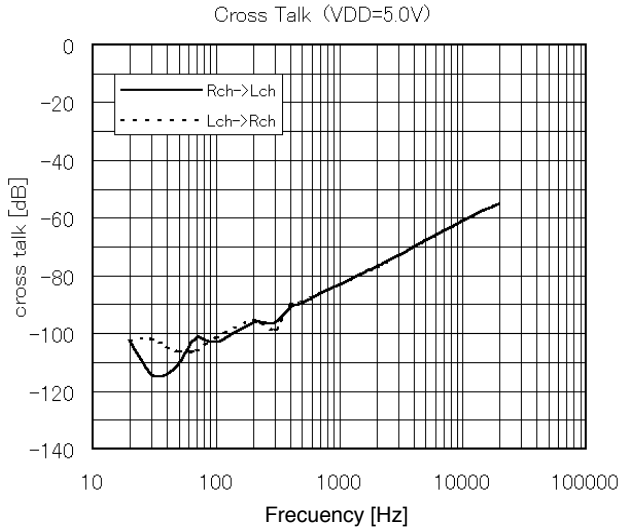
Lo=10μH Co=1μF RL=4Ω VDD=5.0V

Frecuency characteristics [VDD=3.3V]



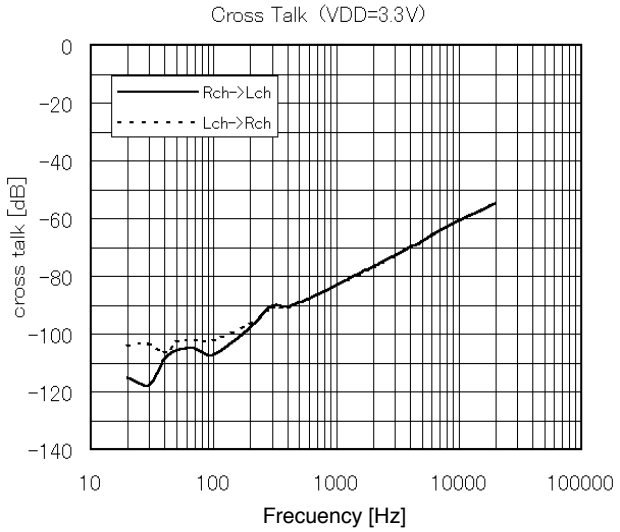
Lo=10μH Co=1μF RL=4Ω VDD=3.3V

Cross Talk (VDD=5.0V)



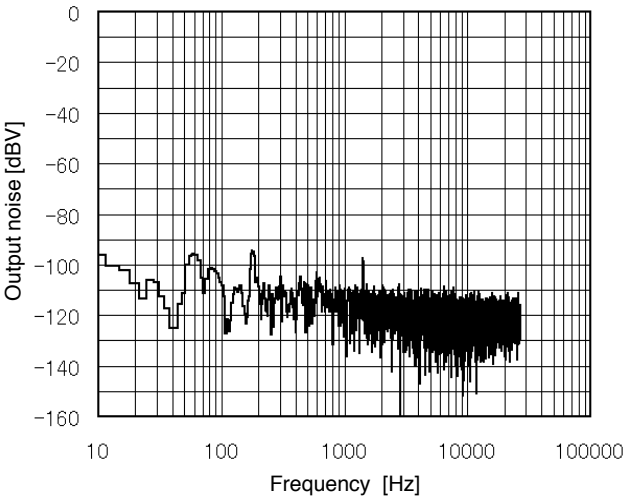
RI=22kΩ RF=22kΩ Po=0.1W RL=4Ω VDD=5.0V

Cross Talk (VDD=3.3V)



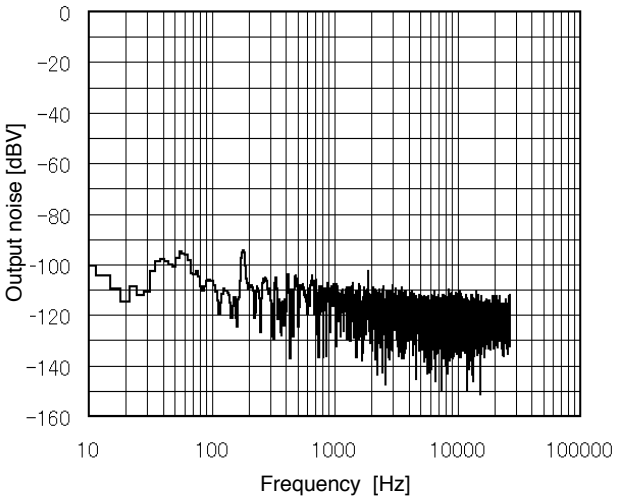
RI=22kΩ RF=22kΩ Po=0.1W RL=4Ω VDD=3.3V

Output noise spectrum



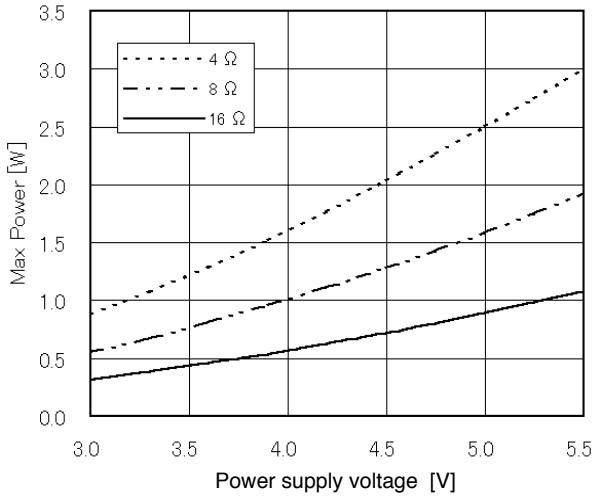
RI=7.5kΩ RF=47kΩ VDD=5.0V

Output noise spectrum



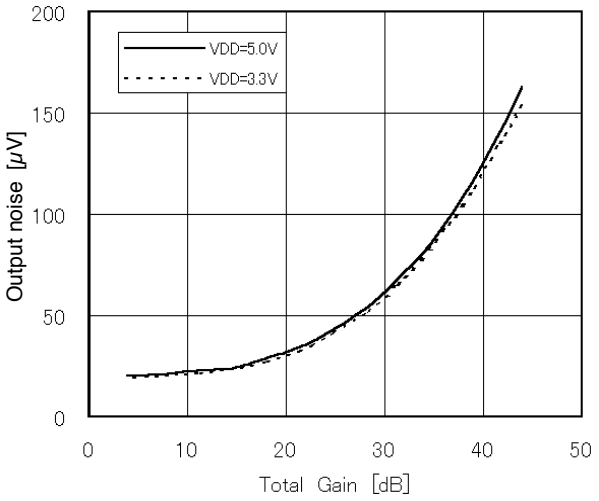
RI=7.5kΩ RF=47kΩ VDD=3.3V

Max power - Power supply voltage



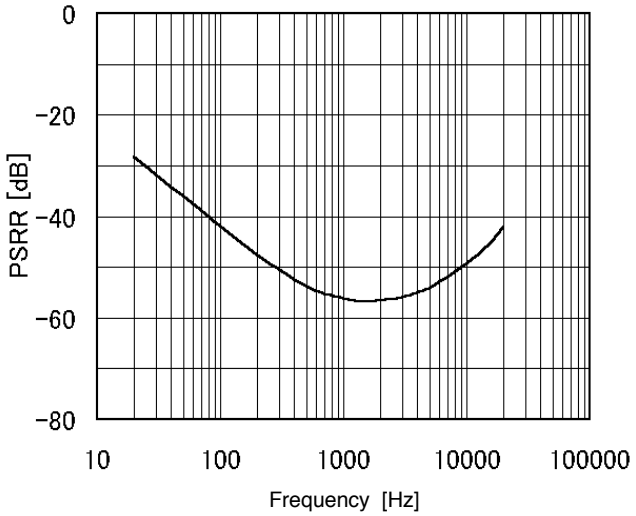
THD=10% f=1kHz

Output noise - Gain



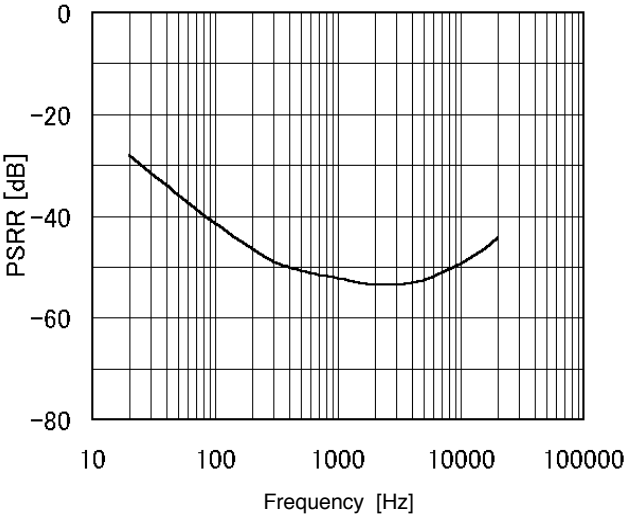
IHF-A + 20kHzLPF RL=4Ω

PSRR (VDD=5.0V)



VDD=5.0V±500mVpp CR1=33μF RL=4Ω

PSRR (VDD=3.3V)



VDD=3.3V±300mVpp CR1=33μF RL=4Ω

■ Recommended parts

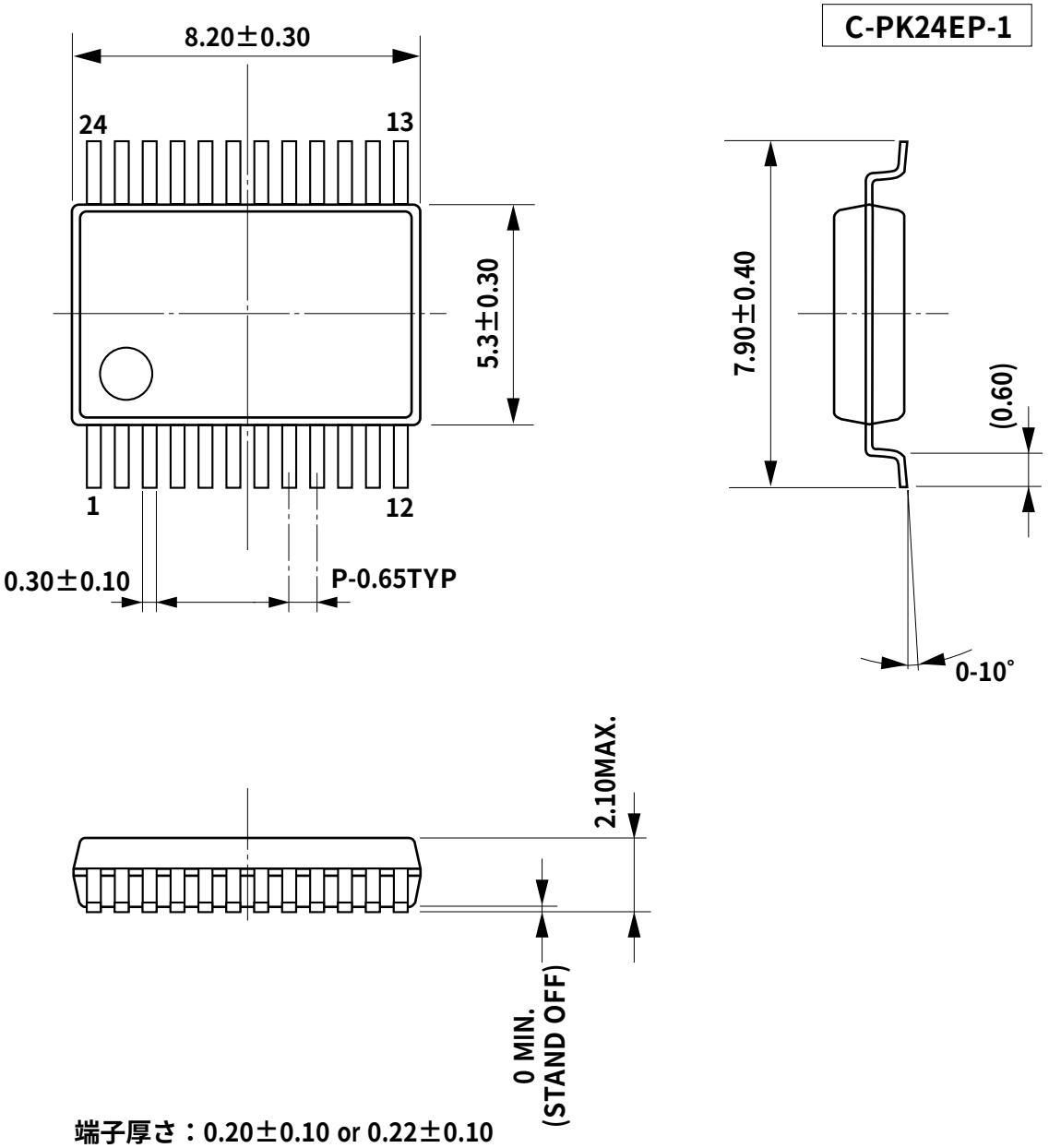
Information about recommended output inductors is as follows.

Manufacturers	Contacts	Model numbers
TOKO, Inc.	http://www.toko.com/	D62LCB / A918CY-100M D53LC / A915AY-100M
FDK CORPORATION	http://www.fdk.co.jp/company_e/han_w_point-e.html For inquiries: Hamagomu Bldg. 5-36-11,Shinbashi,Minato-ku, Tokyo, 105-8677,Japan Mr.Hirofumi Hoshino Manager, Sales Section Electroic Materials Sales Dept. Electroic Sales Div. E-MAIL:hoshino@fdk.co.jp Tel:(81)-3-5473-4662, Fax:(81)-3-3431-9436	CD-C-0506A-100 CD-C-0506C-100 [Trial product]
MITSUMI ELECTRIC CO., LTD.	http://www.mitsumi.co.jp/english/Support/index.html	C5-K1.8L / R-12 A088 EA C5-K2L / R-12 A077 EA

■ External dimensions of package

YDA131-E

C-PK24EP-1



端子厚さ：0.20±0.10 or 0.22±0.10
(LEAD THICKNESS)

カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT) : mm (millimeters)

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注）表面実装 LSI は保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。

Note:The LSIs for surface mount need special consideration on storage and soldering conditions.
For detailed information, please contact your nearest Yamaha agent.

IMPORTANT NOTICE

1. Yamaha reserves the right to make changes to its Products and to this document without notice. The information contained in this document has been carefully checked and is believed to be reliable. However, Yamaha assumes no responsibilities for inaccuracies and makes no commitment to update or to keep current the information contained in this document.

2. These Yamaha Products are designed only for commercial and normal industrial applications, and are not suitable for other uses, such as medical life support equipment, nuclear facilities, critical care equipment or any other application the failure of which could lead to death, personal injury or environmental or property damage. Use of the Products in any such application is at the customer's sole risk and expense.

3. YAMAHA ASSUMES NO LIABILITY FOR INCIDENTAL, CONSEQUENTIAL, OR SPECIAL DAMAGES OR INJURY THAT MAY RESULT FROM MISAPPLICATION OR IMPROPER USE OR OPERATION OF THE PRODUCTS.

4. YAMAHA MAKES NO WARRANTY OR REPRESENTATION THAT THE PRODUCTS ARE SUBJECT TO INTELLECTUAL PROPERTY LICENSE FROM YAMAHA OR ANY THIRD PARTY, AND YAMAHA MAKES NO WARRANTY OR REPRESENTATION OF NON-INFRANGIMENT WITH RESPECT TO THE PRODUCTS. YAMAHA SPECIALLY EXCLUDES ANY LIABILITY TO THE CUSTOMER OR ANY THIRD PARTY ARISING FROM OR RELATED TO THE PRODUCTS' INFRINGEMENT OF ANY THIRD PARTY'S INTELLECTUAL PROPERTY RIGHTS, INCLUDING THE PATENT, COPYRIGHT, TRADEMARK OR TRADE SECRET RIGHTS OF ANY THIRD PARTY.

5. EXAMPLES OF USE DESCRIBED HEREIN ARE MERELY TO INDICATE THE CHARACTERISTICS AND PERFORMANCE OF YAMAHA PRODUCTS. YAMAHA ASSUMES NO RESPONSIBILITY FOR ANY INTELLECTUAL PROPERTY CLAIMS OR OTHER PROBLEMS THAT MAY RESULT FROM APPLICATIONS BASED ON THE EXAMPLES DESCRIBED HEREIN. YAMAHA MAKES NO WARRANTY WITH RESPECT TO THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR USE AND TITLE.

Note) The specifications of this product are subject to change without notice.

Agency

YAMAHA CORPORATION

Semiconductor Sales & Marketing Department

■ Head Office 203, Matsunokijima, Toyooka-mura, Iwata-gun, Shizuoka-ken, 438-0192, Japan
Tel. +81-539-62-4918 Fax. +81-539-62-5054

■ Tokyo Office 2-17-11, Takanawa, Minato-ku, Tokyo, 108-8568, Japan
Tel. +81-3-5488-5431 Fax. +81-3-5488-5088

■ Osaka Office 3-12-12, Minami Senba, Chuo-ku Osaka City, Osaka, 542-0081, Japan
Tel. +81-6-6252-6221 Fax. +81-6-6252-6229

 Printed in Japan