YAMAHA LSI

Preliminary

YGV605

PVDC (Pattern mode Video Display Controller)

■ OUTLINE

PVDC is a VDP for controlling the display screens of various display equipment (Consumer TVs, various CRT monitors, liquid crystal TVs, liquid crystal panels, etc.).
It's extensive functions include: a pattern graphics plane, a sprite plane, a ROM data transfer function, and an external synchronization function. It is an optimum display control, used mainly for game equipment.

■ FEATURES

- Consists of a one pattern graphic plane (scroll screen), and 64 sprite planes (movable screens).
- Because parameters are used to set the synchronous frequency and resolution of the display screen, the PVDC can be used with a variety of display equipment systems. (NTSC and PAL TV, various CRTs, liquid crystal TV, liquid crystal panels, etc.)
- Because the PVDC incorporates VRAM, an externally attached video memory can be constructed using only a pattern ROM. (Reduced system cost and lower programming requirements)
- Because data can be transferred to the built-in VRAM, color pallet, and register directly from the externally attached ROM, the initial VDP setup is easy.
- Scrolling of a divided screen is possible.
- Built-in color pallet that simultaneously displays 16 colors, with 4096 colors to choose from.
- Linear RGB output by built-in DAC
- Superimpose or multiple VDP construction is made possible by the external synchronization function.
- Pattern size is 8 × 8 dots. Color can be specified in dot units.
- Sprite size is 8 × 8 dots or 16 × 16 dots. Color can be specified in dot units.
- Maximum number of sprites that can be displayed on one screen is 64, with a maximum of 16 sprites on one horizontal line.
- 80-pin plastic QFP, CMOS, 5V single power supply.

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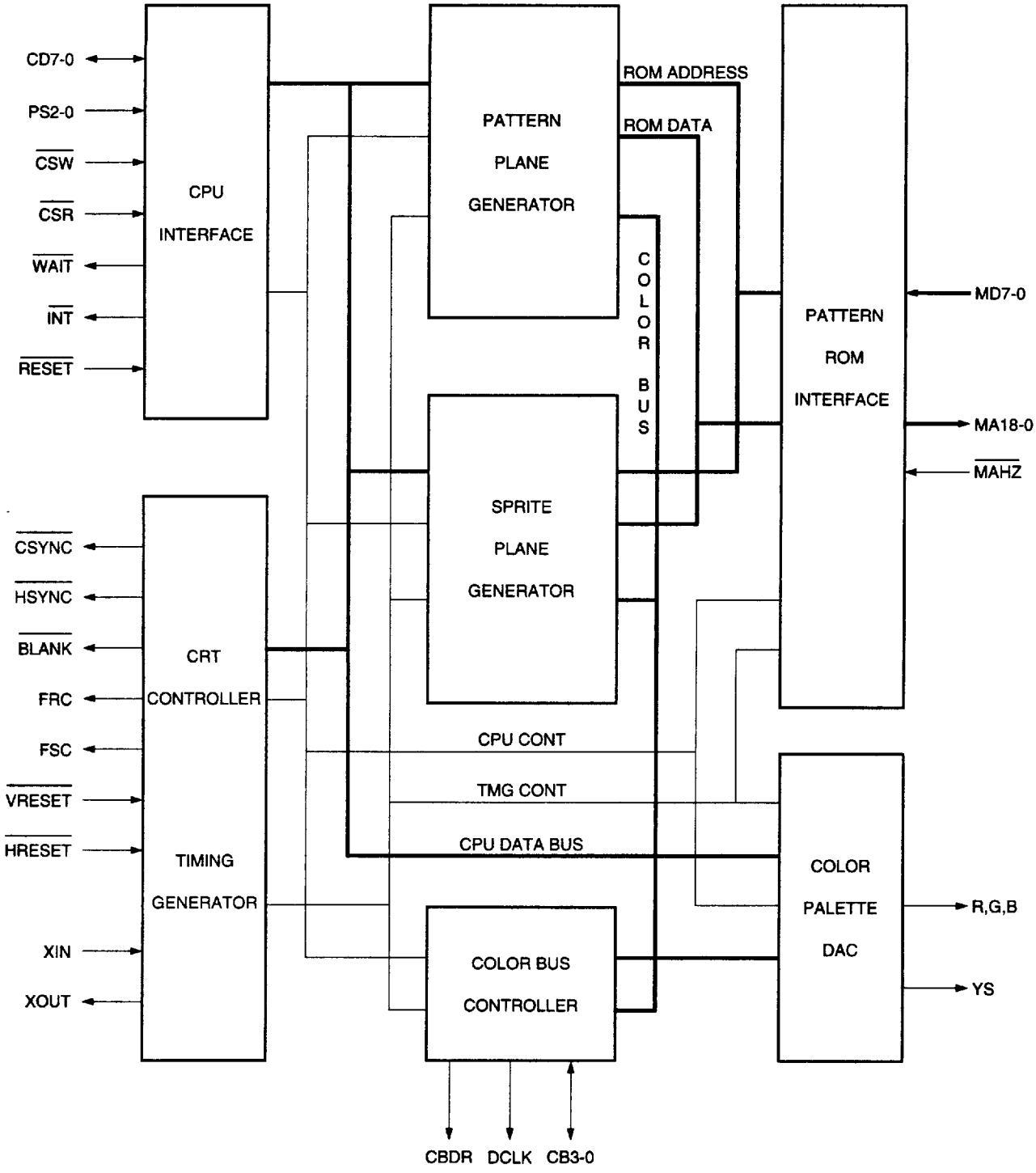
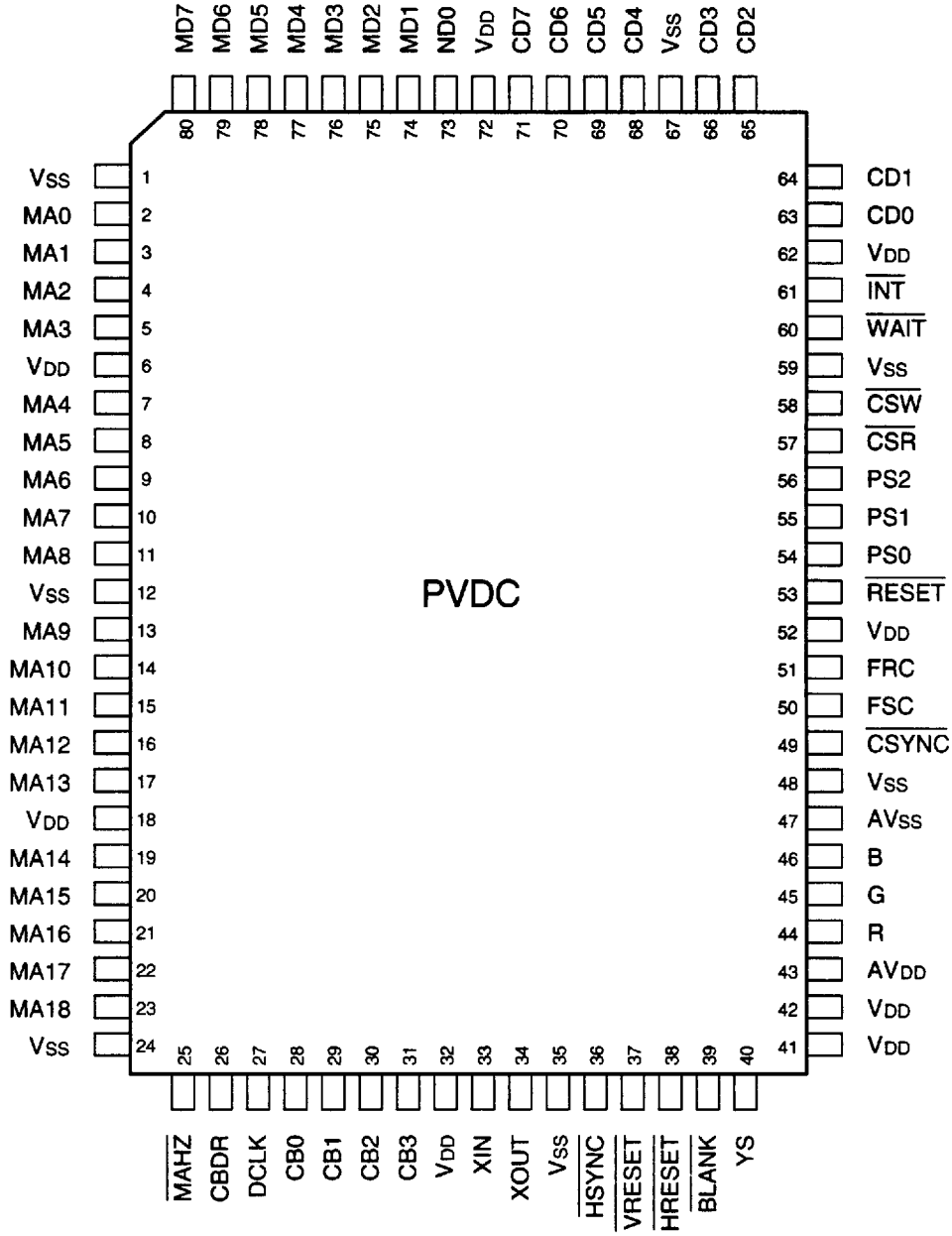
YGV605 CATALOG
CATALOG No.: LSI-4GV6050
1992. 9

■ BLOCK DIAGRAM



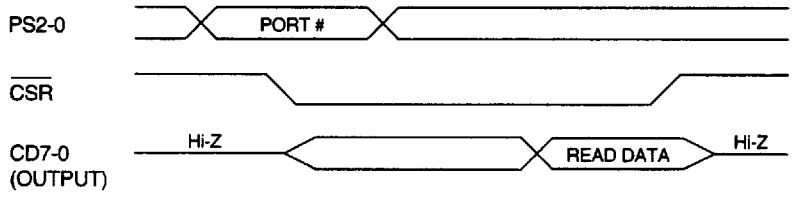
■ PIN ASSIGNMENT



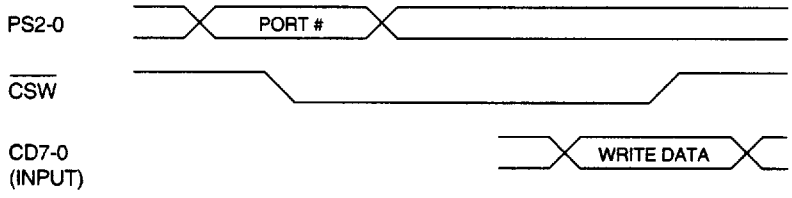
■ TERMINAL FUNCTION

1) CPU interface

- CD7-0 (I/O)
  CPU 8-bit bi-directional data bus.
- PS2-0 (I)
  Input/Output port no. input. PVDC P#0 ~ P#7 selection.
- $\overline{CSR}$ (I)
  Strobe input for PVDC data read out from the CPU.
- $\overline{CSW}$ (I)
  Strobe input for PVDC data write from the CPU.



CPU-PVDC READ CYCLE



CPU-PVDC WRITE CYCLE

- $\overline{WAIT}$ (O: Open drain output)
  Output of wait signal to the CPU.
- $\overline{INT}$ (O: Open drain output)
  Output of the interruption request signal to the CPU.
- $\overline{RESET}$ (I)
  Power on reset input. PVDC is initialized during low level.

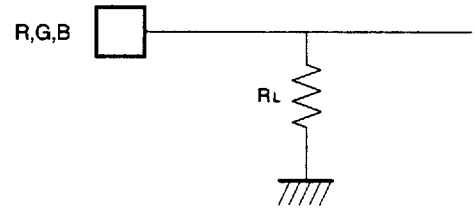
2) ROM interface

- MD7-0 (I)
  ROM data bus.
- MA18-0 (O: 3 state output)
  ROM address bus.
- $\overline{MAHZ}$ (I)
  Make terminal MA18-0 high impedance during low level.

3) Display monitor interface

- $\overline{CSYNC}$ (O)
  Combined synchronous signal or vertical synchronous signal.
- $\overline{HSYNC}$ (O)
  Horizontal synchronous signal.

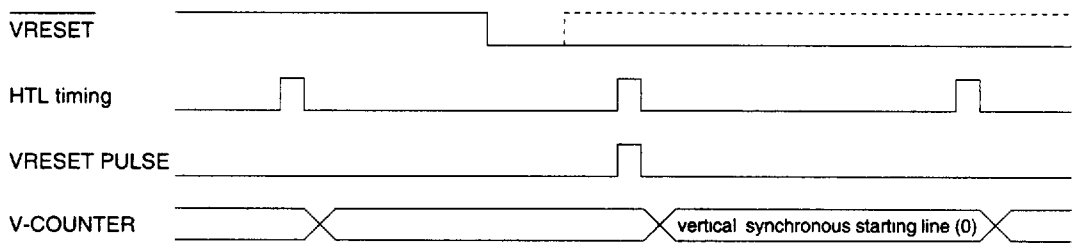
• R, G, B (O: Analog output)
Linear RGB output.



• FSC (O)
Output of sub-carrier clock for video encoder.

• FRC (O)
Frame clock output. A 2-frame cycle clock is used to make the panel AC conversion.

• $\overline{\text{VRESET}}$ (I)
Vertical timing reset input. The input signal to this terminal is sampled with the dot clock, then a fall from high level to low level is detected, and the internal V counter is reset to the vertical synchronous starting line at the next HTL timing (HSYNC start timing).
When reset input is made during the vertical display interval, the display data of the next one field is not guaranteed.



• $\overline{\text{HRESET}}$ (I)
Horizontal timing reset input. The input signal to this terminal is sampled with the main clock, then a fall from high level to low level is detected, and the internal H counter is reset to the horizontal synchronous starting position.
When reset input is made during the horizontal display interval, the display data of the next one line is not guaranteed.

• YS (O)
Superimpose timing signal. It becomes high level during PVDC data display timing.

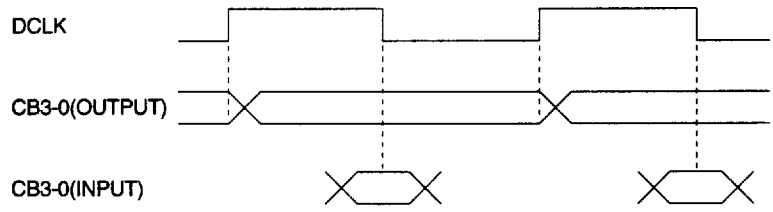
• $\overline{\text{BLANK}}$ (O)
Retrace line blanking interval. Its output timing is 3-dots earlier than the linear RGB and SYNC output.

• CB3-0 (I/O)
Color bus terminal. Display color code output from PVDC, or display color code input to PVDC. Its output timing is 3-dots earlier than the linear RGB and SYNC output.

• DCLK (O)

Dot clock output.

Input/output of the terminal CB3-0 synchronizes this clock.



• CBDR (O)

This shows the input/output status of the CB3-0 terminal.

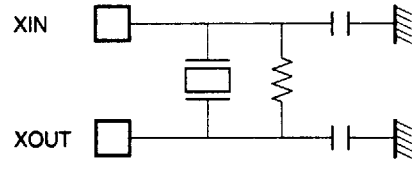
When the CBDR is low level, the CB3-0 becomes an input terminal.

When it is high level, the CB3-0 becomes an output terminal.

4) Others

• XIN (I), XOUT (O)

Crystal oscillator connection terminal for the main clock. External clock input should be input to the XIN terminal.



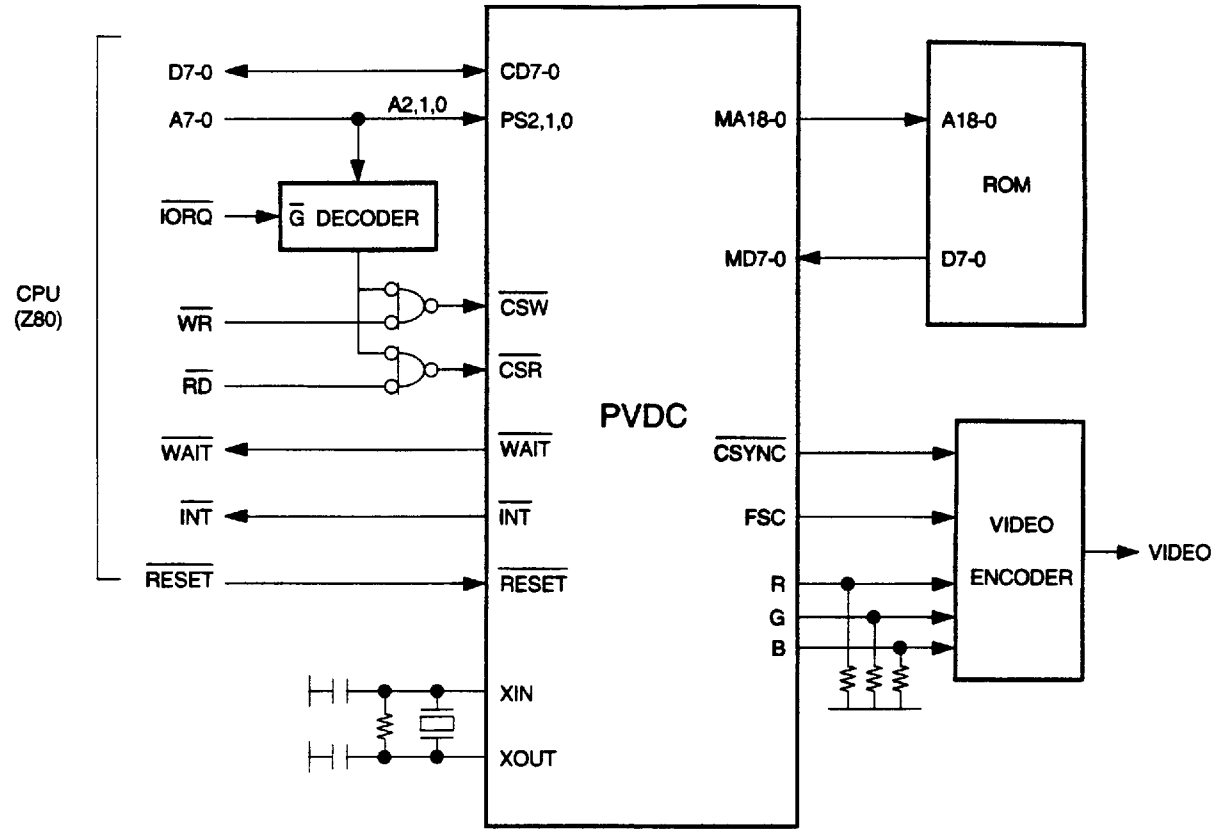
• AVDD, AVSS (I)

Analog power supply input for RGB.

• VDD, VSS (I)

Digital power supply input.

■ SYSTEM CONFIGURATION EXAMPLE



■ ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5~+7.0	V
Input terminal voltage	V_I	–0.5~V_{DD}+0.5	V
Output terminal voltage	V_O	–0.5~V_{DD}+0.5	V
Output terminal current	I_O	–20~+20	mA
Storage temperature	Tstg	–50~+125	°C

• Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Supply voltage	V_{SS}		0		V
Low-level Input voltage (except for the XIN terminal)	V_{IL}	–0.3		0.8	V
High-level Input voltage (except for the XIN terminal)	V_{IH}	2.0		V_{DD}+0.3	V
Low-level Input voltage (the XIN terminal)	V_{IL}	–0.3		1.5	V
High-level Input voltage (the XIN terminal)	V_{IH}	3.5		V_{DD}+0.3	V
Ambient operating temperature	Top	0		70	°C

• Electrical Characteristics Under Recommended Operating Conditions

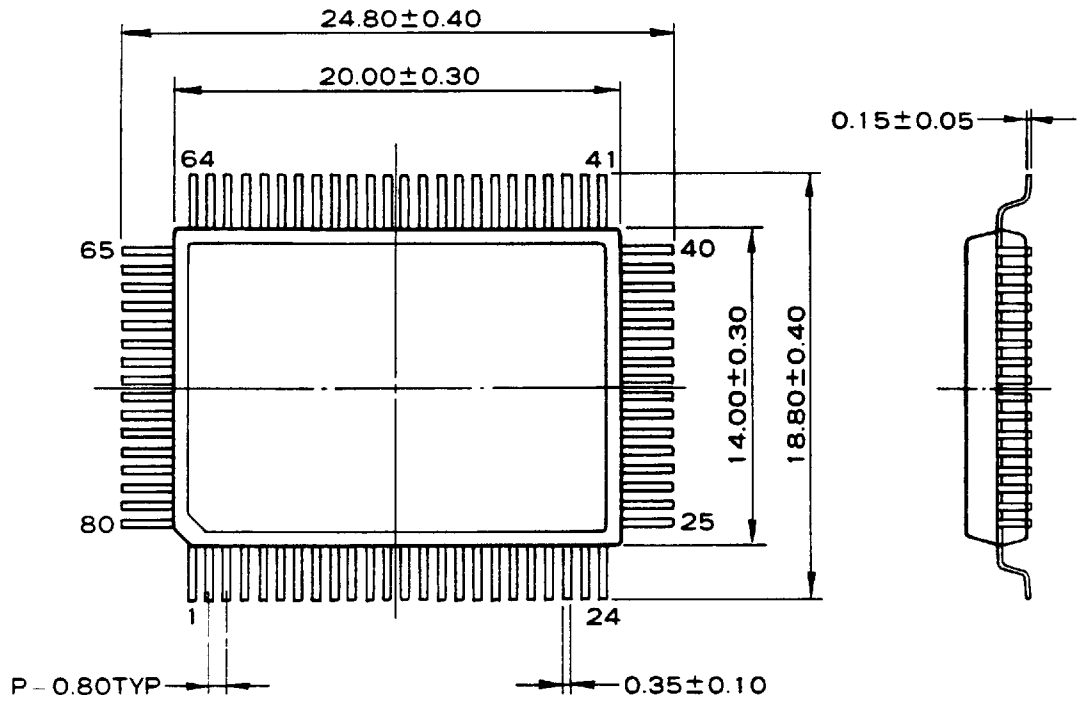
• DC Characteristics

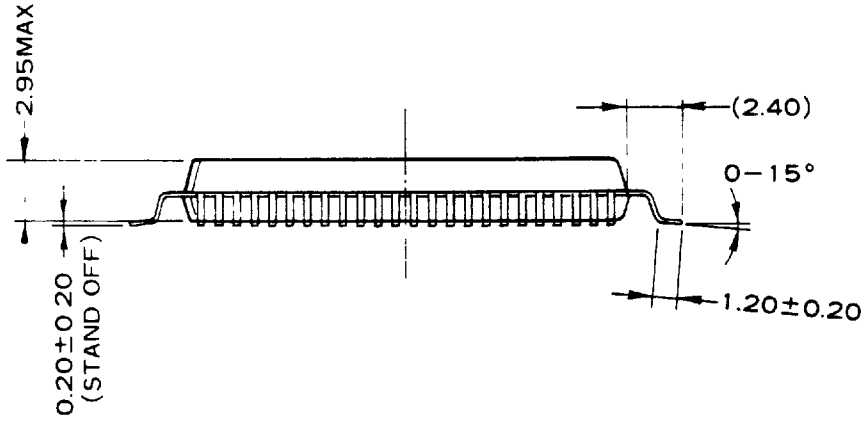
Item	Symbol	Measuring conditions	Min.	Typ.	Max.	Unit
Low-level output voltage (except for the OPEN DRAIN terminal)	V_{OL}	I_{OL}=1.6 mA			0.4	V
Low-level output voltage (the OPEN DRAIN terminal)	V_{OL}	I_{OL}=3.2 mA			0.4	V
High-level output voltage (except for the OPEN DRAIN terminal)	V_{OH}	I_{OH}=–0.4 mA	4.0			V
Input leakage current	I_{LI}				10	µA
Output leakage current	I_{LO}				25	µA
Power consumption	I_{DD}			60		mA

• Terminal capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input terminal capacity	C_I			8	pF
Output terminal capacity	C_O			10	
Input/Output terminal capacity	C_{IO}			12	

■ EXTERNAL DIMENSION





UNIT: mm

The specifications of this product are subject to improvement changes without prior notice.

AGENCY

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0.3K-0920 Printed in Japan 92.8