COS/MOS INTEGRATED CIRCUIT

4517B

HCC/HCF 4517B

DUAL 64-STAGE STATIC SHIFT REGISTER

- CLOCK FREQUENCY 12 MHz (TYP.) AT V_{DD}= 10V
- SCHMITT TRIGGER CLOCK INPUTS ALLOW OPERATION WITH VERY SLOW CLOCK RISE AND FALL TIMES
- THREE-STATE OUTPUTS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4517B** (extended temperature range) and **HCF 4517B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.

The **HCC/HCF 4517B** dual 64-stage static shift register consists of two independent registers each having a clock, data, and write enable input and outputs accessible at taps following the 16th, 32nd, 48th, and 64th stages. These taps also serve as input points allowing data to be inputted at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low-to-high transition. The truth table indicates how the clock and write enable inputs control the operation of the **HCC/HCF 4517B**. Inputs at the intermediate taps allow entry of 64 bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

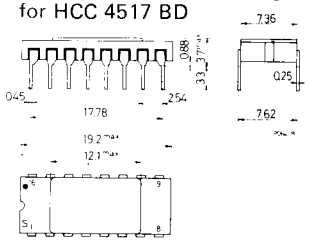
* All voltages are with respect to V_{SS} (GND).

ORDERING NUMBERS:

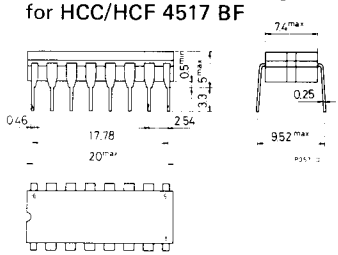
HCC 4517 BD for dual in-line ceramic package
HCC 4517 BF for dual in-line ceramic package, frit seal
HCC 4517 BK for ceramic flat package
HCF 4517 BE for dual in-line plastic package
HCF 4517 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

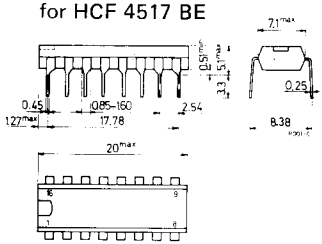
Dual in-line ceramic package for HCC 4517 BD



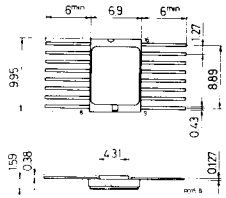
Dual in-line ceramic package for HCC/HCF 4517 BF



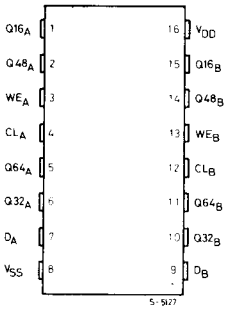
Dual in-line plastic package for HCF 4517 BE



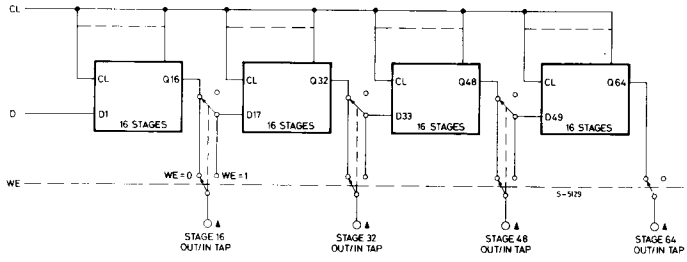
Ceramic flat package for HCC 4517 BK



PIN CONNECTIONS



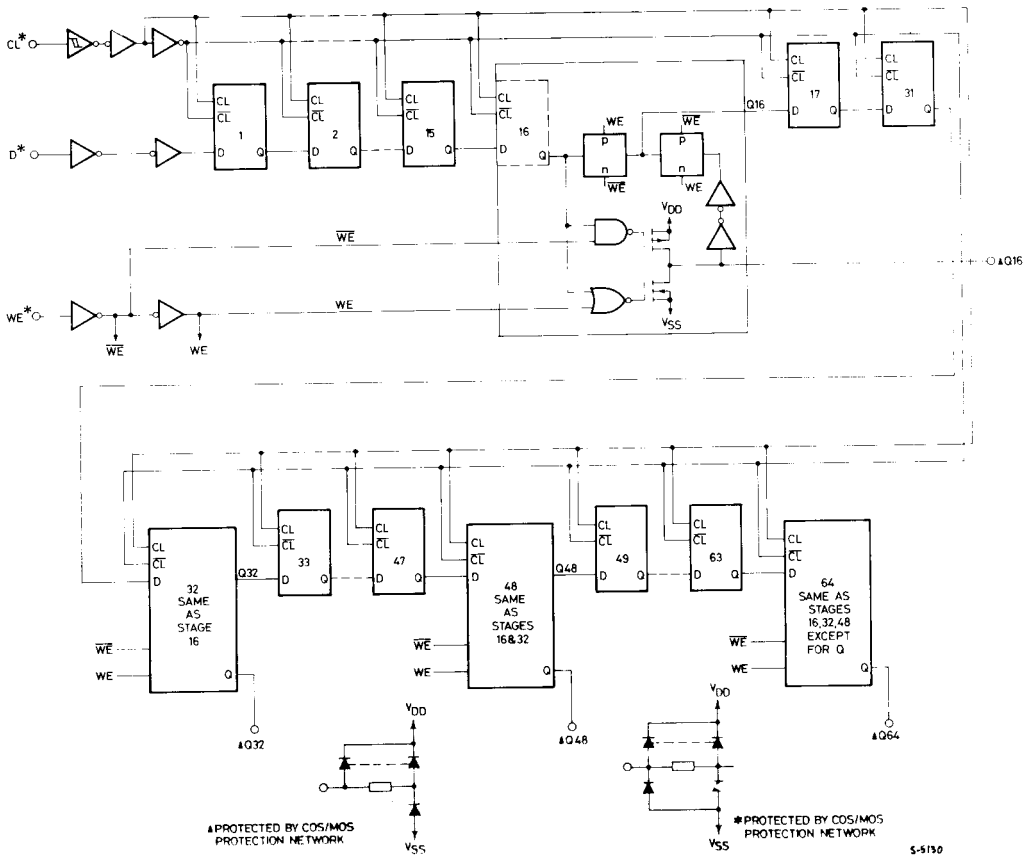
FUNCTIONAL DIAGRAM (one half)



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC DIAGRAM AND TRUTH TABLE



Clock	Write Enable	Data	Stage 16 Tap	Stage 32 Tap	Stage 48 Tap	Stage 64 Tap
0	0	X	Q16	Q32	Q48	Q64
0	1	X	Z	Z	Z	Z
1	0	X	Q16	Q32	Q48	Q64
1	1	X	Z	Z	Z	Z
⌐	0	DI In	Q16	Q32	Q48	Q64
⌐	1	Di In	D17 In	D33 In	D49 In	Z
⌐	0	X	Q16	Q32	Q48	Q64
⌐	1	X	Z	Z	Z	Z

X = Don't Care Z = High Impedance

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		± 1	
I_{OH}, I_{OL}	3-state output leakage current	HCC types	0/18			18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
		HCF types	0/15			15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	
C_I	Input capacitance			Any input						5	7.5			pF

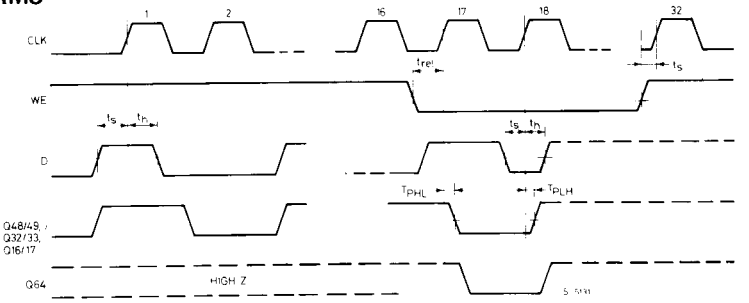
* T_{Low} = − 55°C for **HCC** device: −40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ)

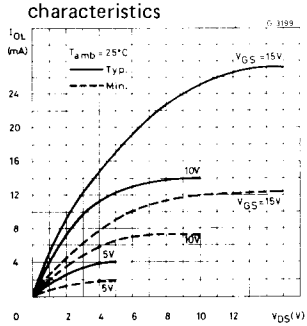
Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation delay time: CL to Bit 16 Tap	5		200	400	ns
		10		110	220	
		15		90	180	
t_{PLZ}, t_{PHZ} t_{PZL}, t_{PZH}	3-state output WE to Bit 16 Tap (see note)	5		75	150	ns
		10		40	80	
		15		30	60	
t_{THL}, t_{TLH}	Output transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_{setup}	Write enable-to-clock	5	-100	-50		ns
		10	-50	-25		
		15	-30	-15		
t_{setup}	Data-to-clock	5	-100	-50		ns
		10	-60	-30		
		15	-30	-15		
	Write enable-to-clock Release time	5		50	100	ns
		10		25	50	
		15		20	40	
t_{hold}	Data-to-clock	5		100	200	ns
		10		50	100	
		15		25	50	
t_W	Minimum clock pulse width	5		90	180	ns
		10		40	80	
		15		25	50	
f_{CL}	Maximum clock input frequency	5	3	6		MHz
		10	6	12		
		15	8	15		
t_f, t_r	Maximum clock input rise or fall time	5	UNLIMITED			μs
		10				
		15				

Note: Measured at the point of 10% change in output with an output load of 50 pF, RL= 1 kΩ to V_{DD} for t_{PZL}, t_{PLZ} and R_L= 1 kΩ to V_{SS} for t_{PHZ}.

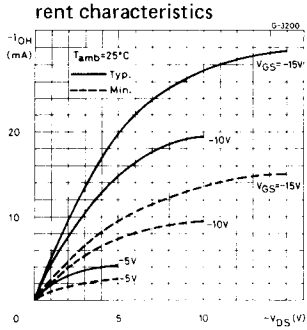
WAVEFORMS



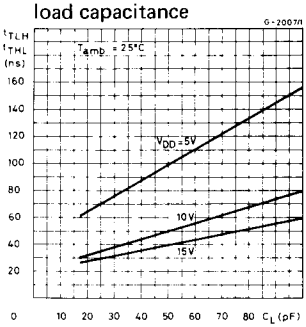
Output low (sink) current characteristics



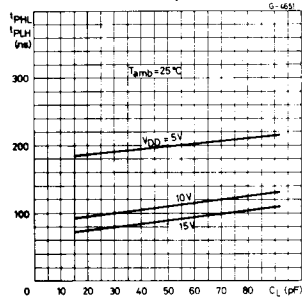
Output high (source) current characteristics



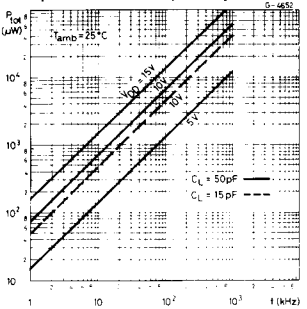
Typical transition time vs. load capacitance



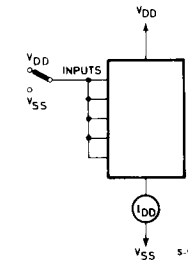
Typical propagation delay time vs. load capacitance



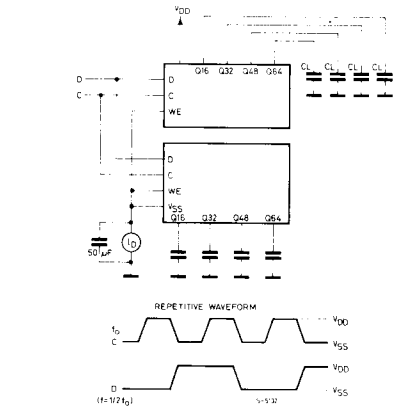
Typical dinamic power dissipation vs. frequency

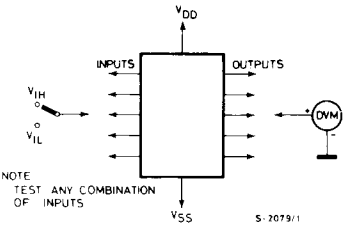


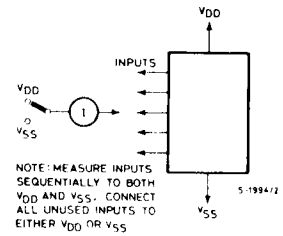
TEST CIRCUITS

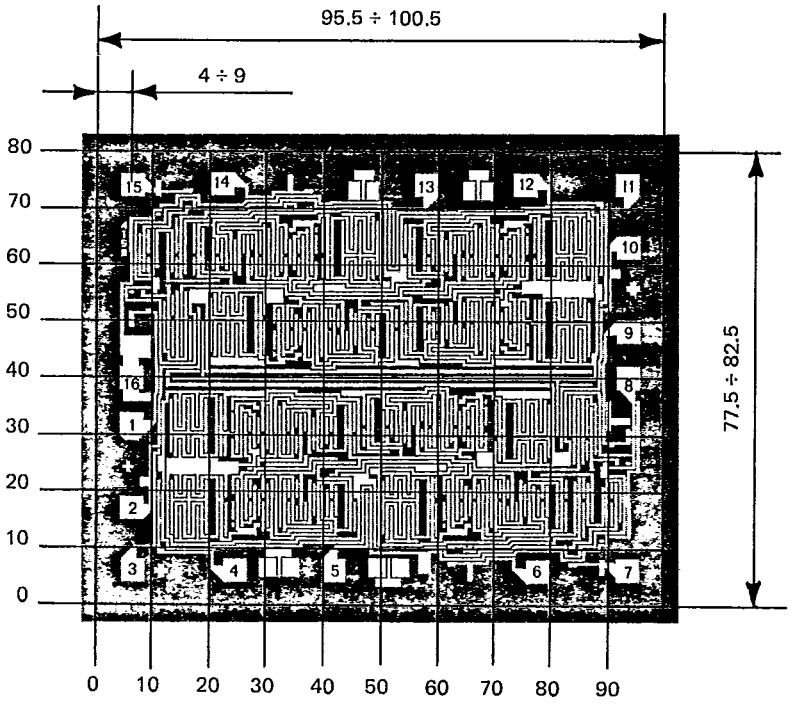


Dynamic power dissipation and waveforms









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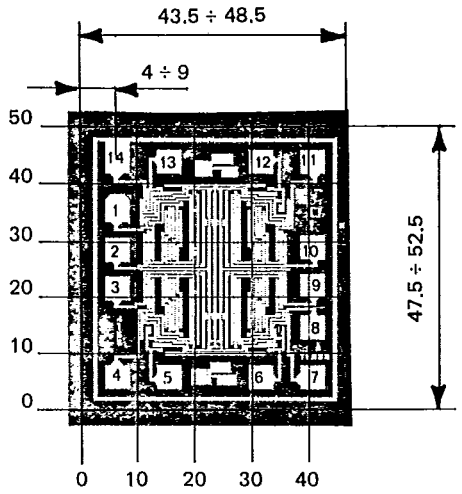

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