

**OKI Semiconductor****FEDD51V17805F-02**  
Issue Date: Aug. 16, 2002**MSM51V17805F****2,097,152-Word × 8-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO****DESCRIPTION**

The MSM51V17805F is a 2,097,152-word × 8-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM51V17805F achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM51V17805F is available in a 28-pin plastic TSOP.

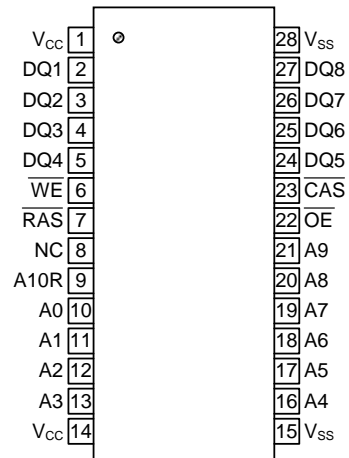
**FEATURES**

- 2,097,152-word × 8-bit configuration
- Single 3.3V power supply, ±0.3V tolerance
- Input : LVTTL compatible, low input capacitance
- Output : LVTTL compatible, 3-state
- Refresh : 2048 cycles/32ms
- Fast page mode with EDO, read modify write capability
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
- Packages  
28-pin 400mil plastic TSOP (TSOPII28-P-400-1.27-K) (Product : MSM51V17805F-xxTS-K)  
xx indicates speed rank.

**PRODUCT FAMILY**

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>		Operating (Max.)	Standby (Max.)
MSM51V17805F	50ns	25ns	13ns	13ns	84ns	360mW	1.8mW
	60ns	30ns	15ns	15ns	104ns	324mW	
	70ns	35ns	20ns	20ns	124ns	288mW	

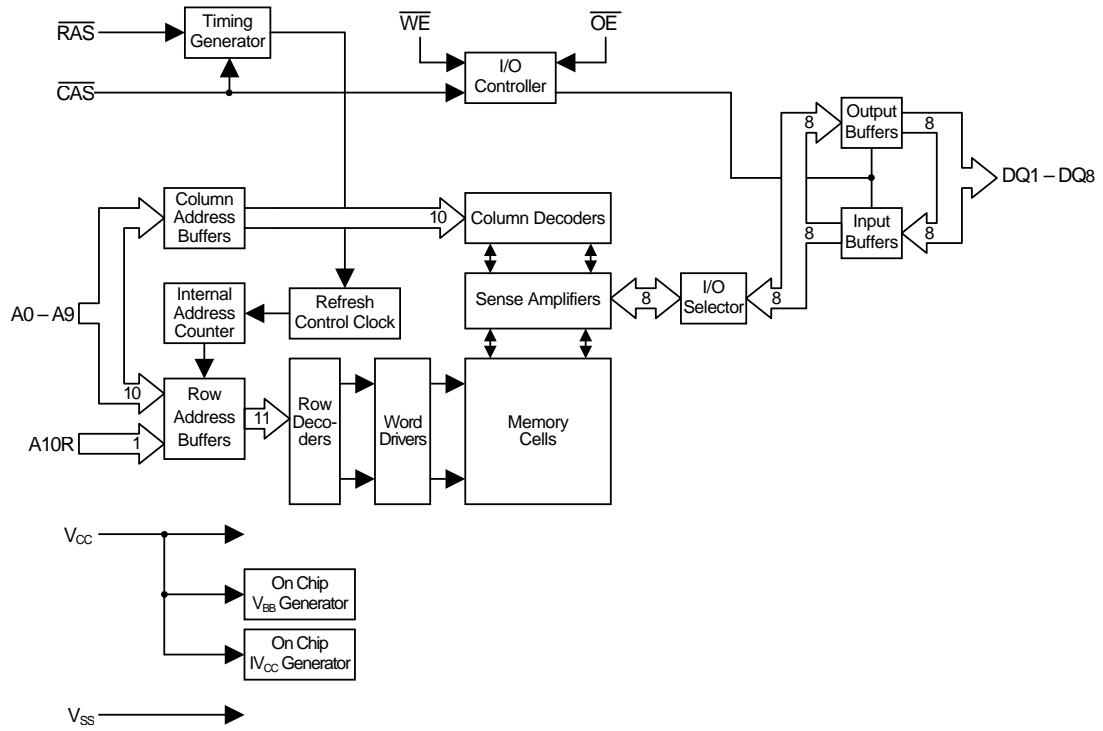
## PIN CONFIGURATION (TOP VIEW)

28-Pin Plastic TSOP  
(K Type)

Pin Name	Function
A0–A9, A10R	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
DQ1–DQ8	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$V_{\text{CC}}$	Power Supply (3.3V)
$V_{\text{SS}}$	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every  $V_{\text{CC}}$  pin, and the same GND voltage level must be provided to every  $V_{\text{SS}}$  pin.

**BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS****ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage $V_{CC}$ Supply relative to $V_{SS}$	$V_T$	-0.5 to 4.6	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_{D^*}$	1	W
Operating Temperature	$T_{opr}$	0 to 70	°C
Storage Temperature	$T_{stg}$	-55 to 150	°C

\*:  $T_a = 25^{\circ}\text{C}$ **RECOMMENDED OPERATING CONDITIONS** $(T_a = 0 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	3.0	3.3	3.6	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3^{*1}$	V
Input Low Voltage	$V_{IL}$	$-0.3^{*2}$	—	0.8	V

Notes: \*1. The input voltage is  $V_{CC} + 1.0\text{V}$  when the pulse width is less than 20ns (the pulse width is with respect to the point at which  $V_{CC}$  is applied).

\*2. The input voltage is  $V_{SS} - 1.0\text{V}$  when the pulse width is less than 20ns (the pulse width respect to the point at which  $V_{SS}$  is applied).

**PIN CAPACITANCE** $(V_{CC} = 3.3\text{V} \pm 0.3\text{V}, T_a = 25^{\circ}\text{C}, f = 1 \text{ MHz})$ 

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 – A9, A10R)	$C_{IN1}$	—	5	pF
Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$C_{IN2}$	—	7	pF
Output Capacitance (DQ1 – DQ8)	$C_{I/O}$	—	7	pF

## DC CHARACTERISTICS

(V<sub>CC</sub> = 3.3V ± 0.3V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM51V17805 F-50		MSM51V17805 F-60		MSM51V17805 F-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.0mA	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I <sub>LI</sub>	0V ≤ V <sub>I</sub> ≤ V <sub>CC</sub> +0.3V; All other pins not under test = 0V	- 10	10	- 10	10	- 10	10	μA	
Output Leakage Current	I <sub>LO</sub>	DQ disable 0V ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	- 10	10	- 10	10	- 10	10	μA	
Average Power Supply Current (Operating)	I <sub>CC1</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling, t <sub>RC</sub> = Min.	—	100	—	90	—	80	mA	1,2
Power Supply Current (Standby)	I <sub>CC2</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$ , $\overline{\text{CAS}} \geq V_{CC} - 0.2V$	—	0.5	—	0.5	—	0.5		
Average Power Supply Current ( $\overline{\text{RAS}}$ -only Refresh)	I <sub>CC3</sub>	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ , t <sub>RC</sub> = Min.	—	100	—	90	—	80	mA	1,2
Power Supply Current (Standby)	I <sub>CC5</sub>	$\overline{\text{RAS}} = V_{IH}$ , $\overline{\text{CAS}} = V_{IL}$ , DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I <sub>CC6</sub>	$\overline{\text{RAS}} =$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	100	—	90	—	80	mA	1,2
Average Power Supply Current (Fast Page Mode)	I <sub>CC7</sub>	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ cycling, t <sub>HPC</sub> = Min.	—	100	—	90	—	80	mA	1,3

- Notes: 1. I<sub>CC</sub> Max. is specified as I<sub>CC</sub> for output open condition.  
2. The address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .  
3. The address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .

## AC CHARACTERISTICS (1/3)

 $(V_{CC} = 3.3V \pm 0.3V, T_a = 0 \text{ to } 70^\circ\text{C})$  Note1,2,3

Parameter	Symbol	MSM51V17805 F-50		MSM51V17805 F-60		MSM51V17805 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	$t_{RC}$	84	—	104	—	124	—	ns	
Read Modify Write Cycle Time	$t_{RWC}$	110	—	135	—	160	—	ns	
Fast Page Mode Cycle Time	$t_{HPC}$	20	—	25	—	30	—	ns	
Fast Page Mode Read Modify Write Cycle Time	$t_{HPRWC}$	58	—	68	—	78	—	ns	
Access Time from $\overline{RAS}$	$t_{RAC}$	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{CAS}$	$t_{CAC}$	—	13	—	15	—	20	ns	4,5
Access Time from Column Address	$t_{AA}$	—	25	—	30	—	35	ns	4,6
Access Time from $\overline{CAS}$ Precharge	$t_{CPA}$	—	30	—	35	—	40	ns	4
Access Time from $\overline{OE}$	$t_{OEA}$	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{CAS}$	$t_{CLZ}$	0	—	0	—	0	—	ns	4
Data Output Hold After $\overline{CAS}$ Low	$t_{DOH}$	5	—	5	—	5	—	ns	
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	$t_{CEZ}$	0	13	0	15	0	20	ns	7,8
$\overline{RAS}$ to Data Output Buffer Turn-off Delay Time	$t_{REZ}$	0	13	0	15	0	20	ns	7,8
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	$t_{OEZ}$	0	13	0	15	0	20	ns	7
$\overline{WE}$ to Data Output Buffer Turn-off Delay Time	$t_{WEZ}$	0	13	0	15	0	20	ns	7
Transition Time	$t_T$	1	50	1	50	1	50	ns	3
Refresh Period	$t_{REF}$	—	32	—	32	—	32	ms	
$\overline{RAS}$ Precharge Time	$t_{RP}$	30	—	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	$t_{RAS}$	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode with EDO)	$t_{RASP}$	50	100,000	60	100,000	70	100,000	ns	
$\overline{RAS}$ Hold Time	$t_{RSH}$	7	—	10	—	13	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	$t_{ROH}$	7	—	10	—	13	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode with EDO)	$t_{CP}$	7	—	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	$t_{CAS}$	7	10,000	10	10,000	13	10,000	ns	
$\overline{CAS}$ Hold Time	$t_{CSH}$	35	—	40	—	45	—	ns	

## AC CHARACTERISTICS (2/3)

(V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>a</sub> = 0 to 70°C) Note1,2,3

Parameter	Symbol	MSM51V17805 F-50		MSM51V17805 F-60		MSM51V17805 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
CAS to RAS Precharge Time	t <sub>CRP</sub>	5	—	5	—	5	—	ns	
RAS Hold Time from CAS Precharge	t <sub>RHCP</sub>	30	—	35	—	40	—	ns	
OE Hold Time from CAS (DQ Disable)	t <sub>CHO</sub>	5	—	5	—	5	—	ns	
RAS to CAS Delay Time	t <sub>RCD</sub>	11	37	14	45	14	50	ns	5
RAS to Column Address Delay Time	t <sub>RAD</sub>	9	25	12	30	12	35	ns	6
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	7	—	10	—	10	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	
Column Address Hold Time	t <sub>CAH</sub>	7	—	10	—	13	—	ns	
Column Address to RAS Lead Time	t <sub>RAL</sub>	25	—	30	—	35	—	ns	
Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	0	—	ns	
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	0	—	ns	9
Read Command Hold Time referenced to RAS	t <sub>RRH</sub>	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	0	—	ns	10
Write Command Hold Time	t <sub>WCH</sub>	7	—	10	—	13	—	ns	
Write Command Pulse Width	t <sub>WP</sub>	7	—	10	—	10	—	ns	
WE Pulse Width (DQ Disable)	t <sub>WPE</sub>	7	—	10	—	10	—	ns	
OE Command Hold Time	t <sub>OEH</sub>	7	—	10	—	13	—	ns	
OE Precharge Time	t <sub>OEP</sub>	7	—	10	—	10	—	ns	
OE Command Hold Time	t <sub>OCH</sub>	7	—	10	—	10	—	ns	
Write Command to RAS Lead Time	t <sub>RWL</sub>	7	—	10	—	13	—	ns	
Write Command to CAS Lead Time	t <sub>CWL</sub>	7	—	10	—	13	—	ns	
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	0	—	ns	11
Data-in Hold Time	t <sub>DH</sub>	7	—	10	—	13	—	ns	11
OE to Data-in Delay Time	t <sub>OED</sub>	13	—	15	—	20	—	ns	
CAS to WE Delay Time	t <sub>CWD</sub>	30	—	34	—	44	—	ns	10
Column Address to WE Delay Time	t <sub>AWD</sub>	42	—	49	—	59	—	ns	10
RAS to WE Delay Time	t <sub>RWD</sub>	67	—	79	—	94	—	ns	10
CAS Precharge WE Delay Time	t <sub>CPWD</sub>	47	—	54	—	64	—	ns	10

## AC CHARACTERISTICS (3/3)

 $(V_{CC} = 3.3V \pm 0.3V, T_a = 0 \text{ to } 70^\circ\text{C})$  Note1,2,3

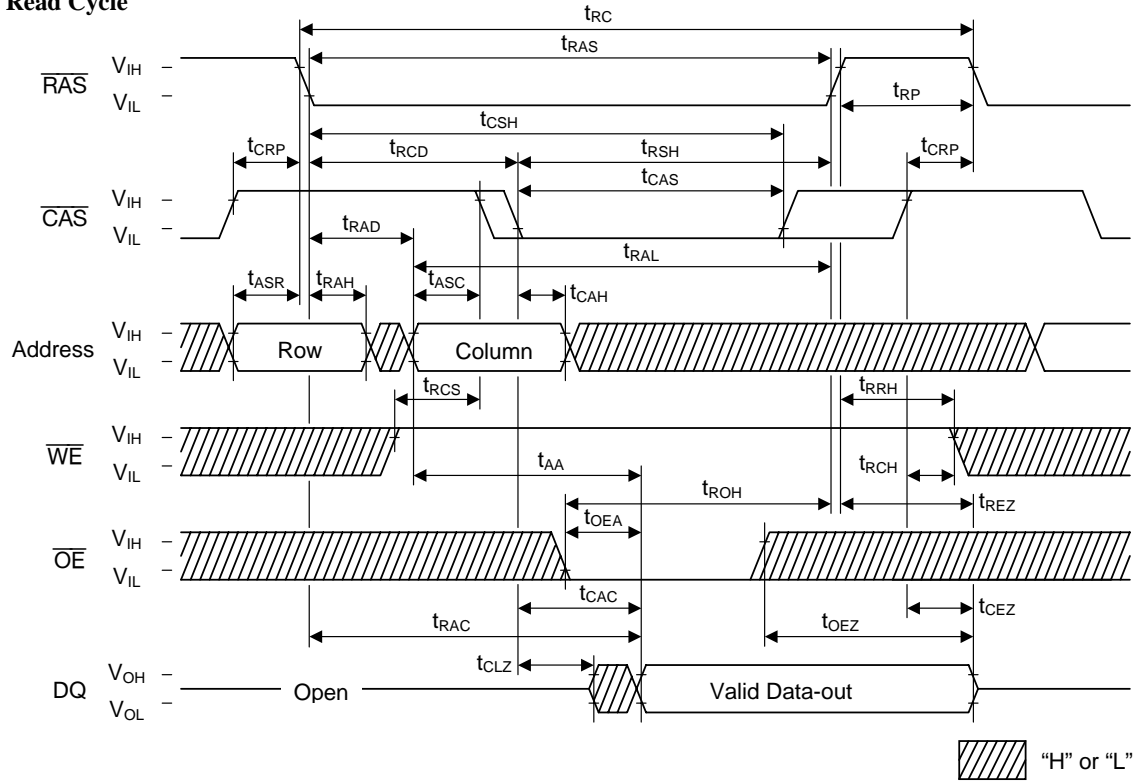
Parameter	Symbol	MSM51V17805 F-50		MSM51V17805 F-60		MSM51V17805 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	$t_{RPC}$	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	$t_{CSR}$	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	$t_{CHR}$	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	$t_{WRP}$	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	$t_{WRH}$	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time	$t_{WTS}$	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time	$t_{WTH}$	10	—	10	—	10	—	ns	



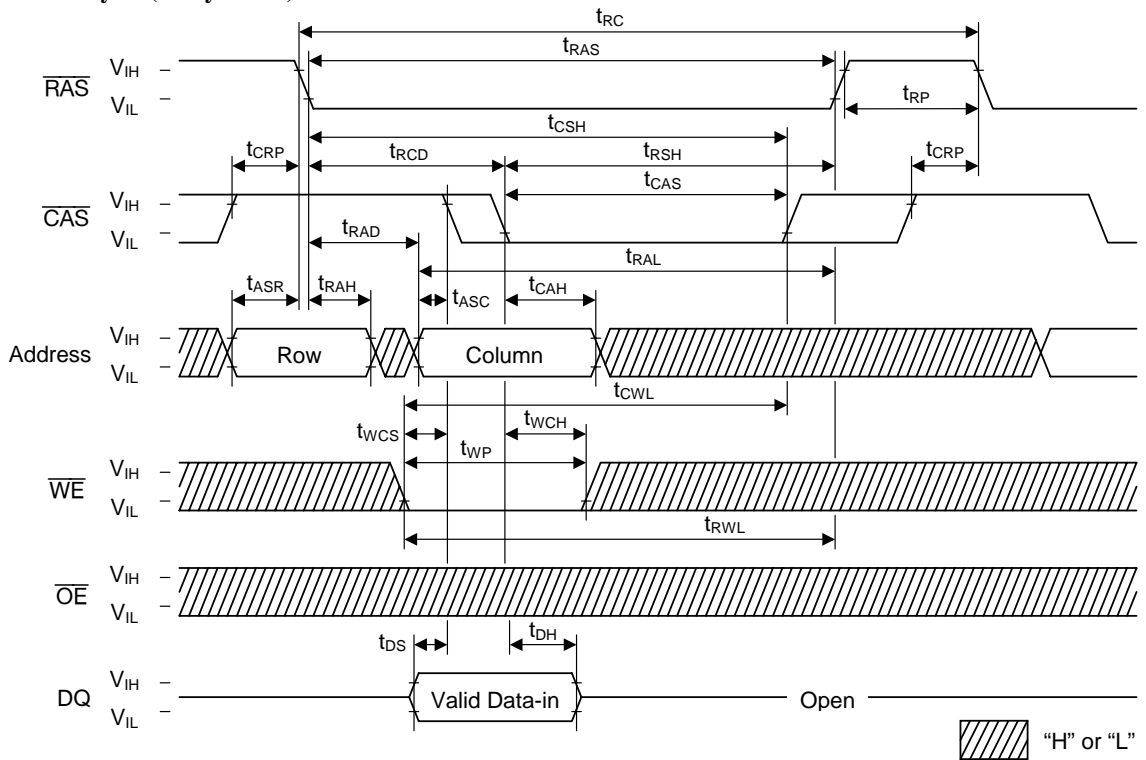
- Notes:
1. A start-up delay of 200 $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 2\text{ns}$ .
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. -50 is measured with a load circuit equivalent to 1 TTL load and 50pF, and -60/-70 is measured with a load circuit equivalent to 1 TTL load and 100pF.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, then the access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, then the access time is controlled by  $t_{AA}$ .
  7.  $t_{CEZ}$  (Max.),  $t_{REZ}$  (Max.),  $t_{WEZ}$  (Max.), and  $t_{OEZ}$  (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{CEZ}$ , and  $t_{REZ}$  must be satisfied for open circuit condition.
  9.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  10.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}$  (Min.),  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{AWD} \geq t_{AWD}$  (Min.) and  $t_{CPWD} \geq t_{CPWD}$  (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
  11. These parameters are referenced to the  $\overline{\text{CAS}}$ , leading edges in an early write cycle, and to the  $\overline{\text{WE}}$  leading edge in an  $\overline{\text{OE}}$  control write cycle, or a read modify write cycle.

**TIMING CHART**

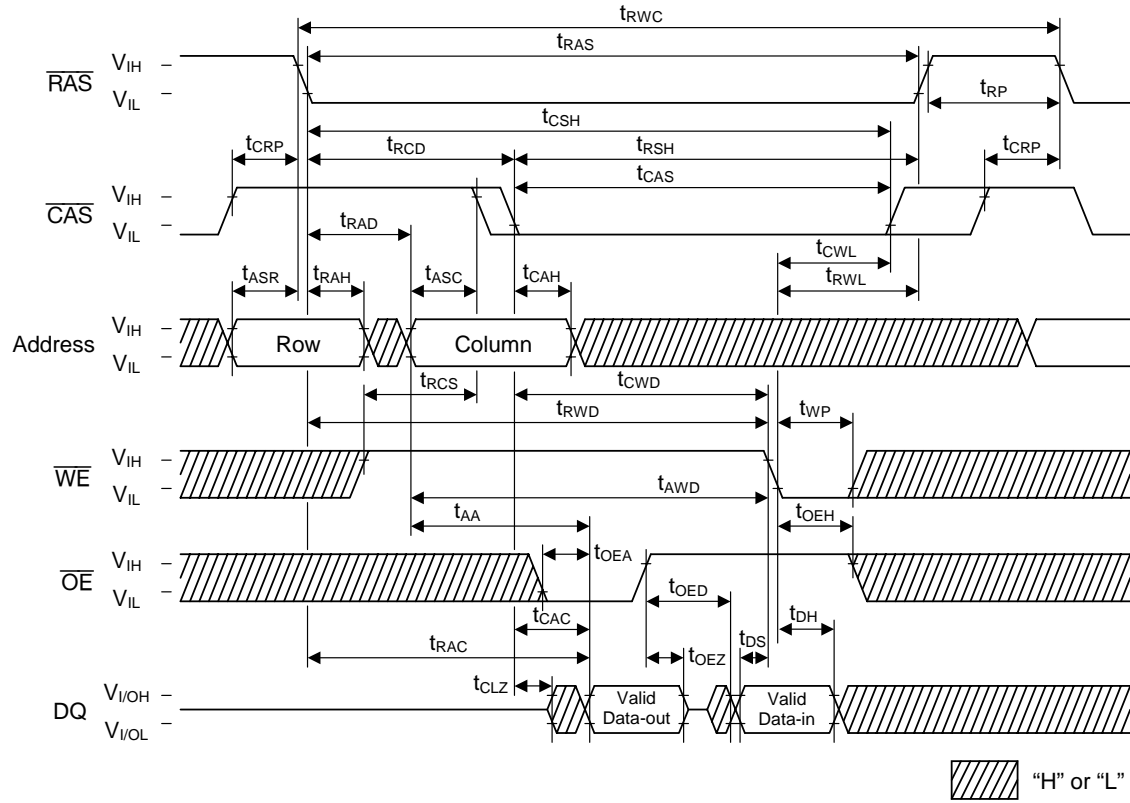
**Read Cycle**



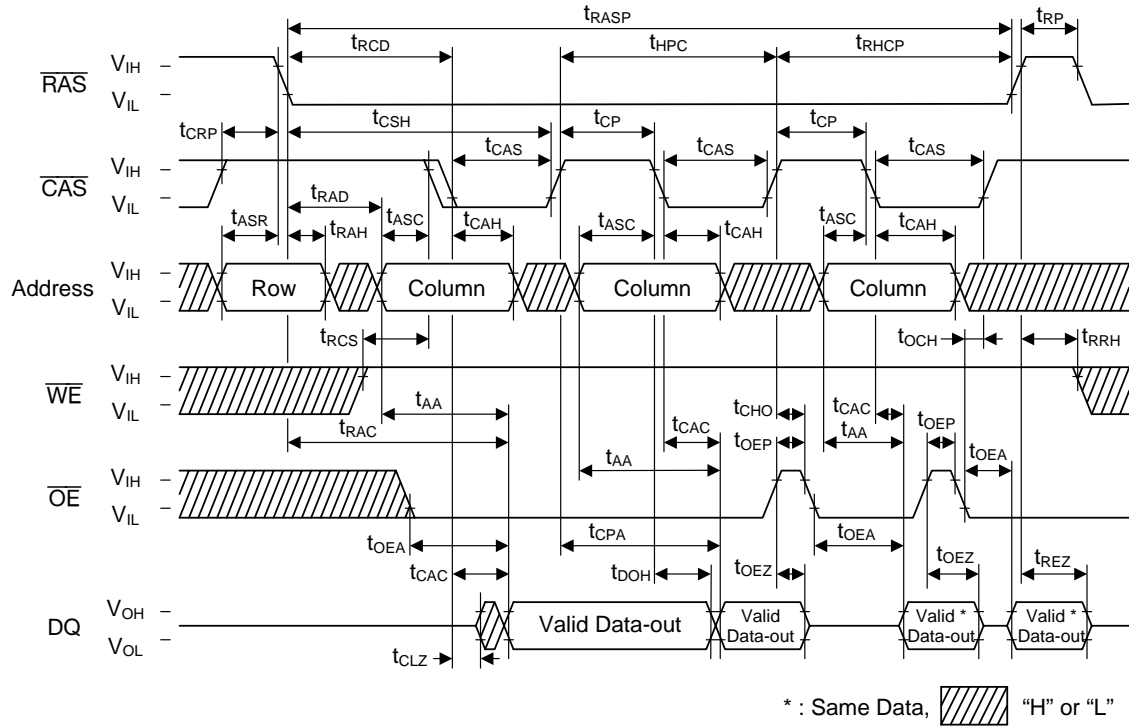
**Write Cycle (Early Write)**



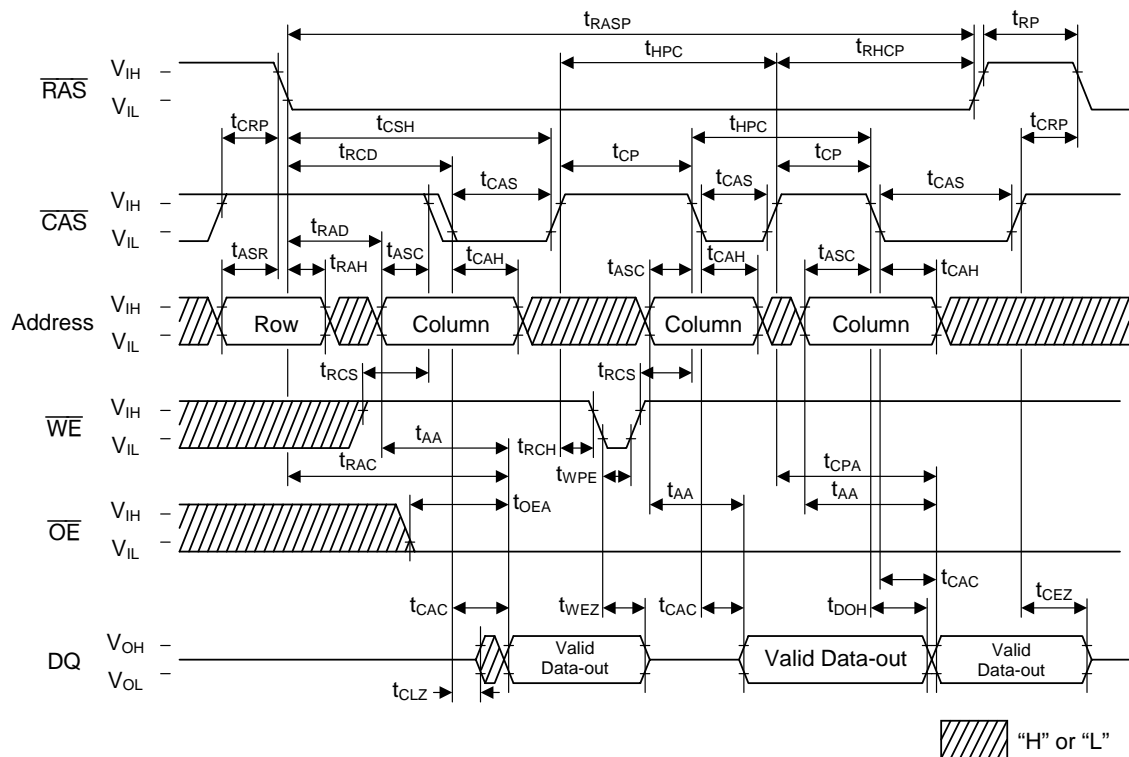
**Read Modify Write Cycle**



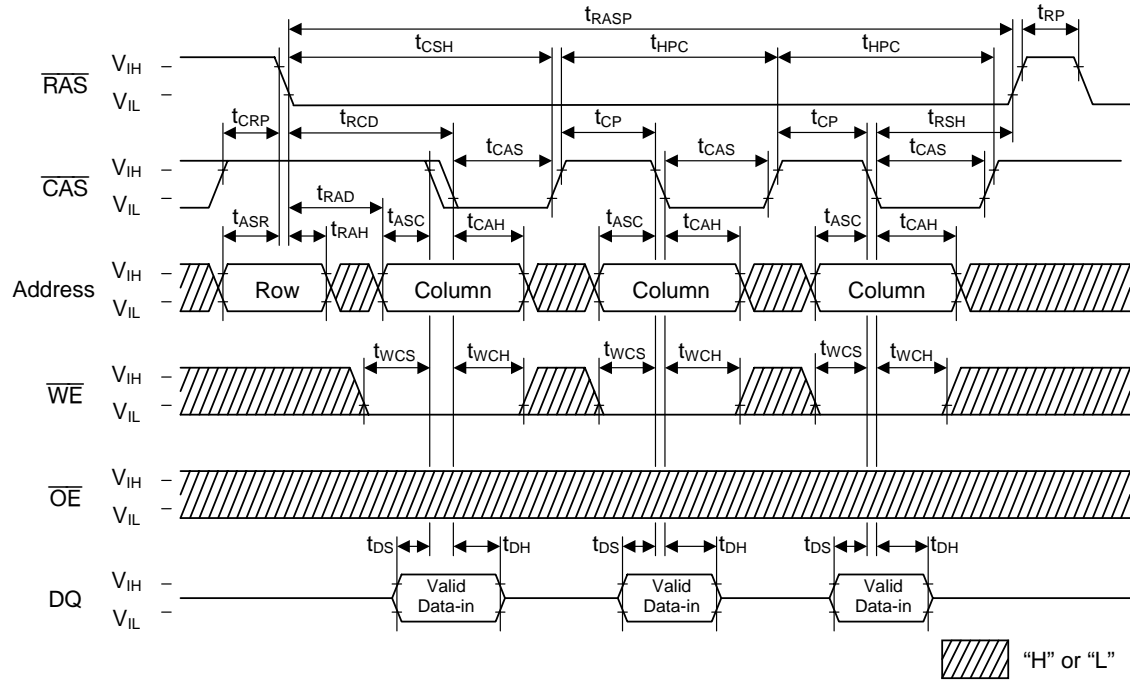
**Fast Page Mode Read Cycle (Part-1)**



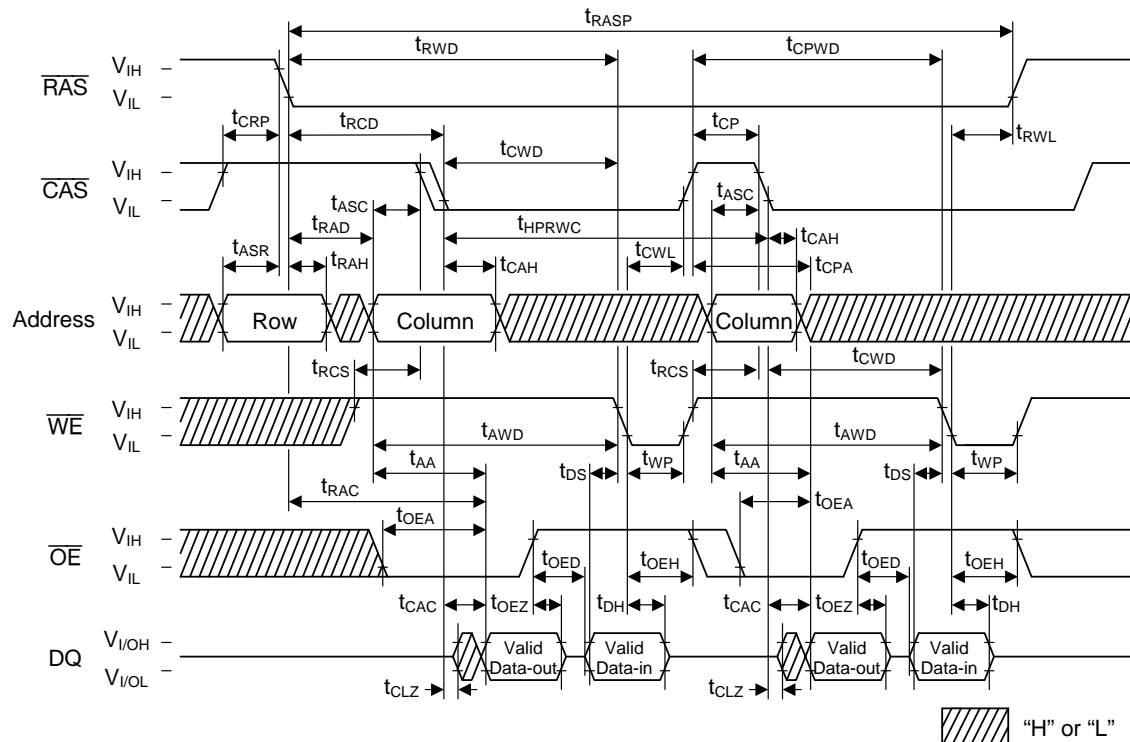
**Fast Page Mode Read Cycle (Part-2)**



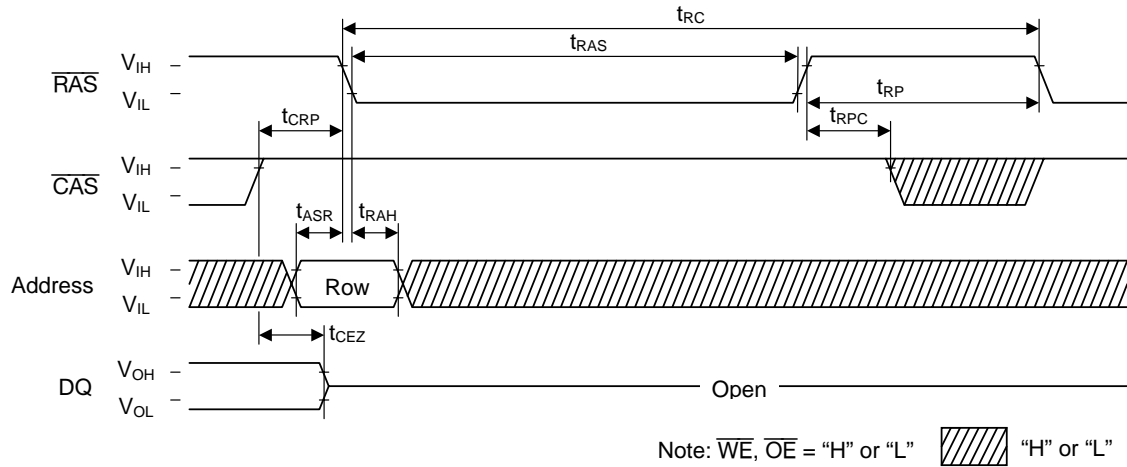
## Fast Page Mode Write Cycle (Early Write)



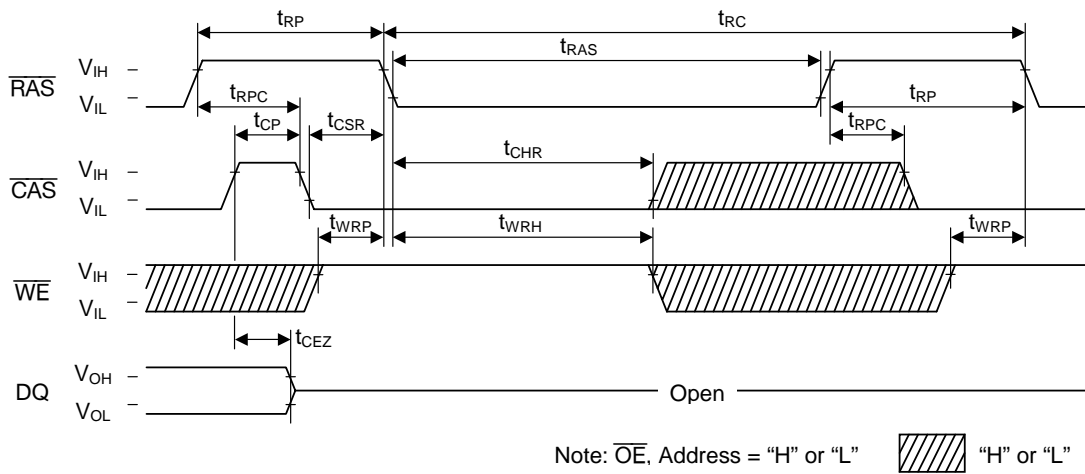
## Fast Page Mode Read Modify Write Cycle



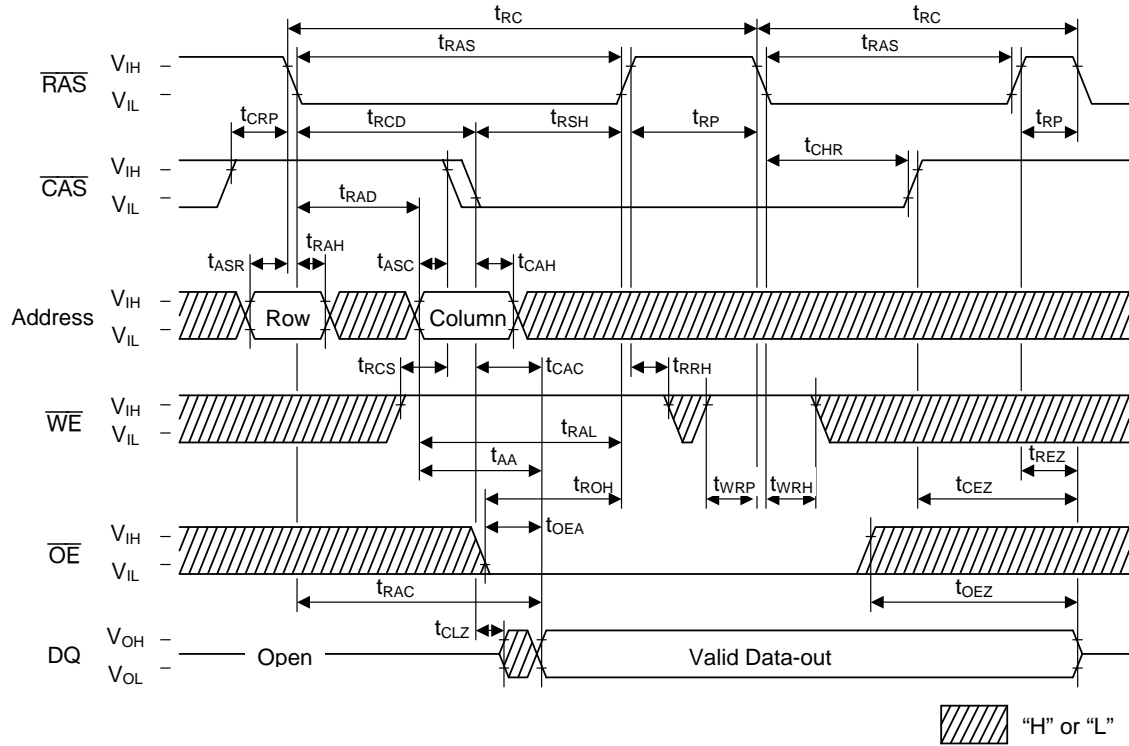
**RAS-only Refresh Cycle**



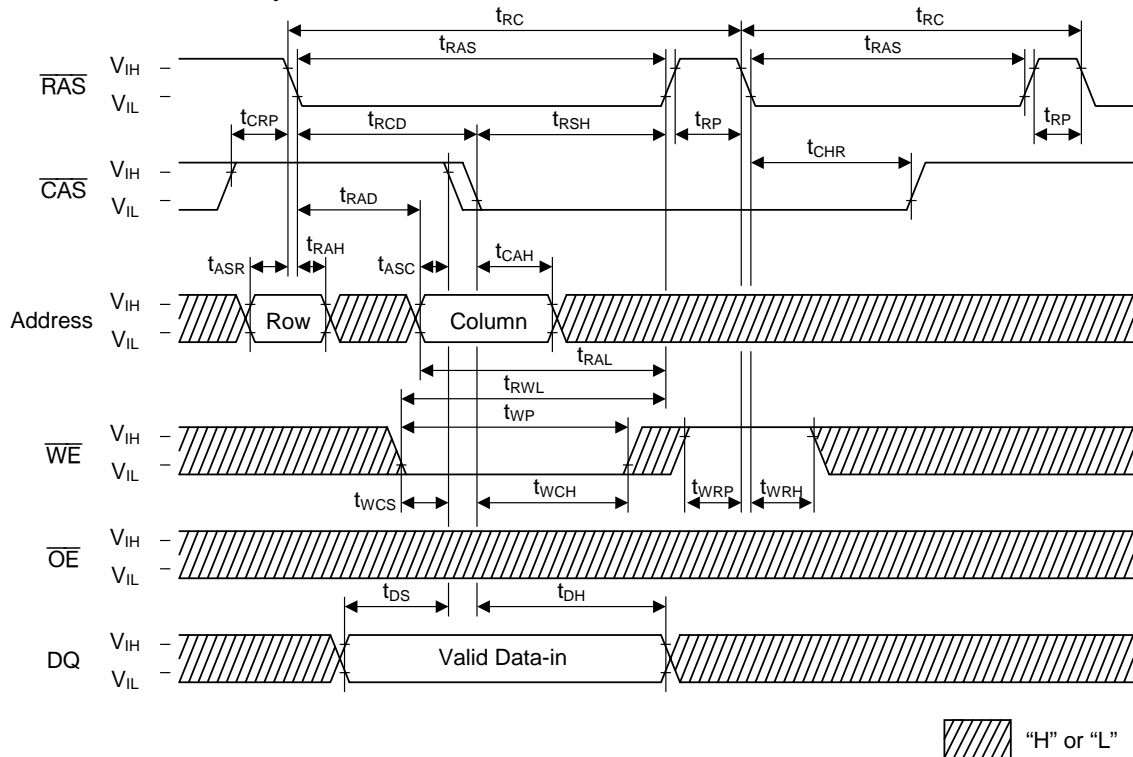
**CAS before RAS Refresh Cycle**



**Hidden Refresh Read Cycle**



**Hidden Refresh Write Cycle**



**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDD51V17805F-01	Dec, 2000	–	–	Final edition 1
FEDD51V17805F-02	Aug, 2002	1, 2	1, 2	Deleted SOJ package



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