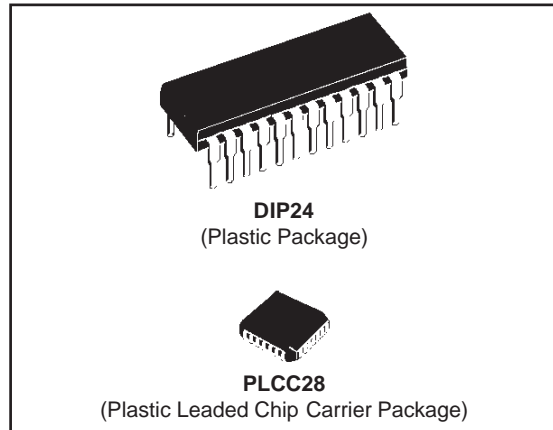


PROGRAMMABLE V.23 MODEM WITH DTMF

- PROGRAMMABLE MODES :
 - Modem 75bps transmit, 1200bps receive
 - Modem 1200bps transmit, 75bps receive
 - DTMF dialing
 - Call status tone detection
 - Auxiliary analog transmit input
 - Analog test loopback
- PROGRAMMABLE FUNCTIONS :
 - Transmission level
 - Hysteresis and detection level
 - Filters (reception and transmission)
 - Line monitoring and buzzer
 - DTMF frequencies
- FIXED COMPROMISE LINE EQUALIZER
- AUTOMATIC BIAS ADJUSTMENT
- INTEGRATED DUPLEXER
- STANDARD LOW COST CRYSTAL (3.579MHz)
- TAX TONE REJECTION
- POWER-UP INITIALIZATION OF REGISTERS
- OPERATES FROM $\pm 5V$
- CMOS



on a 4-wire line. Its programming concept makes it the ideal component to design low-cost intelligent modems, featuring auto dialing and auto answering. The TS7514 conforms to CCITT V.23 recommendation. The chip incorporates DTMF dialing, line monitoring, tone and dialing detection.

DESCRIPTION

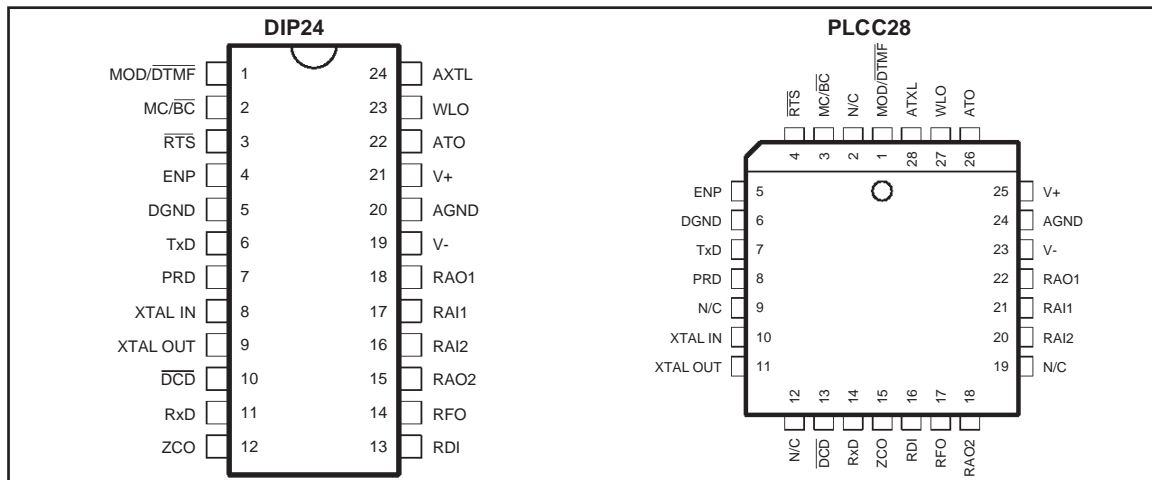
The TS7514 is an FSK modem which can be programmed for asynchronous half-duplex voice-band communications on a 2-wire line or full duplex

ORDER CODES

Part Number	Temperature Range	Package
TS7514CP	0 to 70°C	DIP24
TS7514CFN	0 to 70°C	PLCC28

7514-01.TBL

PIN CONNECTIONS



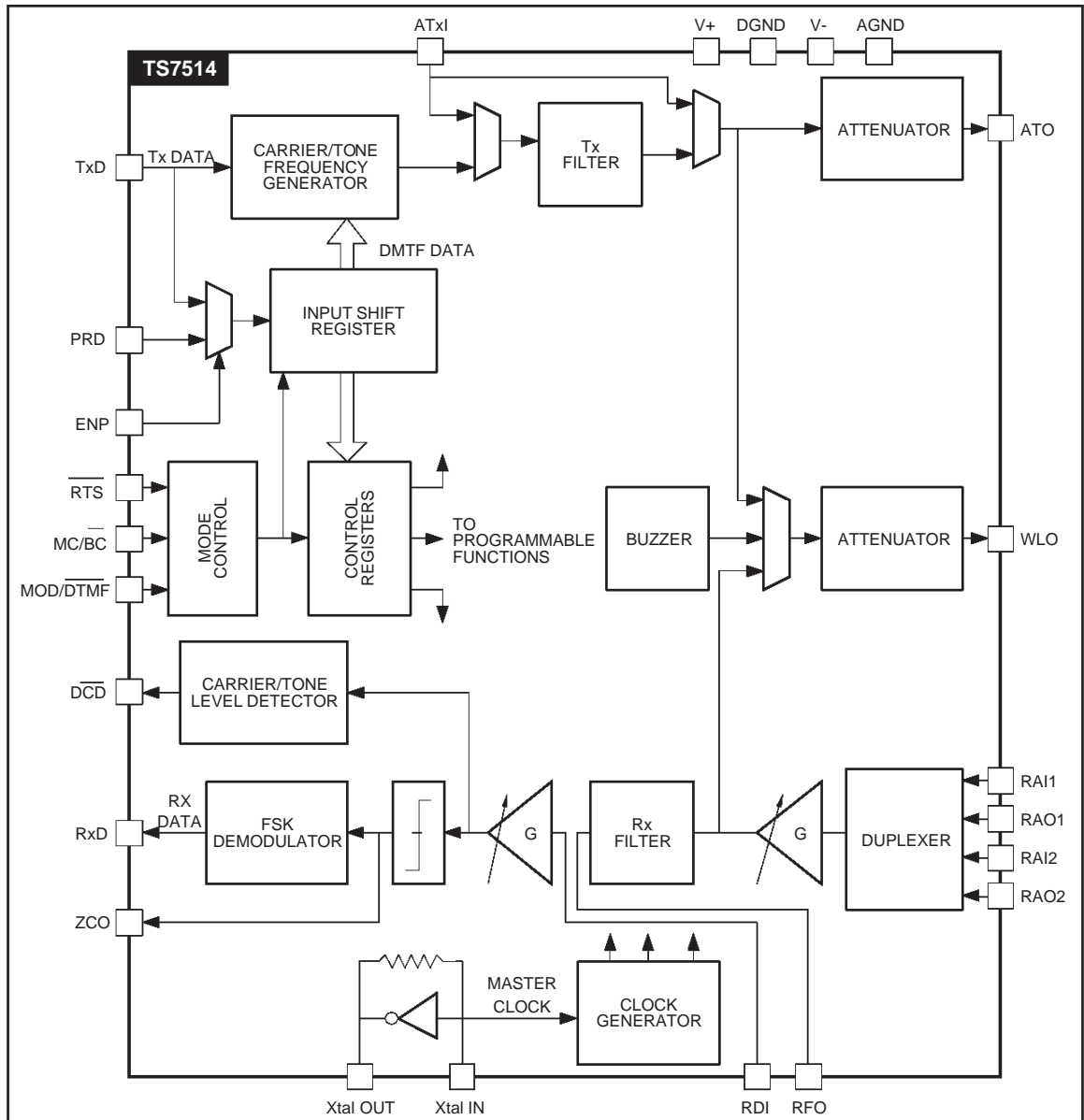
7514-01.EPS / 7514-02.EPS

PIN DESCRIPTION

Name	Pin Number		Description
	DIP24	PLCC28	
MOD/DMTF	1	1	MODEM or DMTF Operating Mode Selection. Also controls write operations to control registers (if MOD/DMTF = 0 and MC/BC = 0).
MC/BC	2	3	Digital Control Input. In MODEM mode, it sets transmission mode to main or back channel. It also permits selection of dialing or control registers programming.
RTS	3	4	Request to Send. When RTS = 0, the circuit sends an analog signal to the ATO output. The signal depends on the operating mode selected. When RTS = 1, the signal sent to ATO is suppressed after its first zero crossing. When MOD/DMTF = 0 and MC/BC = 0, the RTS pin acts as a clock for serial data loading into the input register.
ENP	4	5	Serial Register Write Select Input. When ENP = 0, the serial register input is connected to TxD. When ENP = 1, the register input is connected to PRD.
DGND	5	6	Digital Ground = 0V. All digital signals are referenced to this pin.
TxD	6	7	Digital Input for Transmit or Control Data
PRD	7	8	Digital Input for Control Data. Selected through ENP
XtalIN	8	10	Crystal Oscillator Input. Can be tied to an external clock generator. f _{QUARTZ} = 3.579MHz.
XtalOUT	9	11	Crystal Oscillator Output
DCD	10	13	Data Carrier Detect Output
RxD	11	14	Digital Receive Data Output
ZCO	12	15	Zero Crossing Rx Digital Output (ringing detection)
RDI	13	16	Analog Output for the Receive Signal after Filtering or Analog Input for the Amplifier-limiter.
RFO	14	17	Analog Receive Filter Output
RAO2	15	18	A2 Amplifier Output
RAI2	16	20	A2 Amplifier Inverting Input
RAI1	17	21	A1 Amplifier Inverting Input
RAO1	18	22	A1 Amplifier Output
V-	19	23	Negative Supply Voltage : - 5V ±5%
AGND	20	24	Analog Ground = 0 V. Reference Pin for Analog Signals
V+	21	25	Positive Supply Voltage : + 5V ±5%
ATO	22	26	Analog Transmit Output
WLO	23	27	Analog Output for Line Monitoring and Buzzer
ATxl	24	28	Direct Analog Input Transmit Filter

7514-02.TBL

Figure 1 : Simplified Block Diagram



7514-03.EPS

FUNCTIONAL DESCRIPTION

The TS7514 circuit is an FSK modem for half-duplex, voice-band asynchronous transmissions on a 2-wire line according to CCITT recommendation V.23 or full duplex on 4 wire-line.

The circuit features DTMF dialing, call status tone detection and line monitoring in both dialing and automatic answer modes. A signalling frequency is available at the line monitoring output (buzzer).

Ring detection is possible by using the signal detection function and bypassing the receive filter. The receive signal at ZCO output can be filtered in the associated microprocessor.

The TRANSMIT channel (Tx) includes :

- Two programmable frequency generators.
- One switched capacitor filter (SCF) with low-pass or bandpass configuration and its associated propagation delay corrector.
- One continuous time low-pass smoothing filter.
- One attenuator, programmable from 0 to + 13dB by 1dB steps.
- One programmable analog input.

The RECEIVE channel (Rx) includes :

- Two operational amplifiers for duplexer implementation.
- One continuous time low-pass anti-aliasing filter.
- One programmable gain amplifier.
- One linear compromise equalizer.
- One switched capacitor band pass filter (can be set to either main or back channel).
- One continuous time low pass smoothing filter.
- One limiting amplifier.
- One correlation demodulator.
- One programmable level signal detector.

The LINE MONITORING channel includes :

- One buzzer.
- One 3-channel multiplexer to select between :
 - Transmit channel monitoring.
 - Receive channel monitoring.
 - Buzzer.
- One programmable attenuator

Internal Control

Power-up Initialization

The TS7514 includes power-up initialization of control registers. This system sets the ATO transmission output to an infinite attenuation position, leaving time for the microprocessor to set up the RPROG input on power up. Control registers are also initialized when V+ is lower than 3V or V- greater than -3V.

Registers

Write access to the DTMF data register and to other control registers is achieved in serial mode through TxD input or PRD input. Addressing of these 4 bit registers is indirect. They are accessed through an 8 bit shift register addressed when MOD/DTMF = 0 and MC/BC = 0. Data sent to the TxD input is strobed on the RTS signal trailing edge.

Serial data is sent to the TxD input, with Least Significant Bit (LSB) first. The 4 Most Significant Bits (MSB) contain the control register address while the 4 LSB contain associated data.

Data transfer from the input register to the control register (addressed by the MSB's) is started by the operating mode (MODEM or DTMF) selection (MOD/DTMF = 1 or MC/BC = 1).

Figure 2 : Internal Control Register

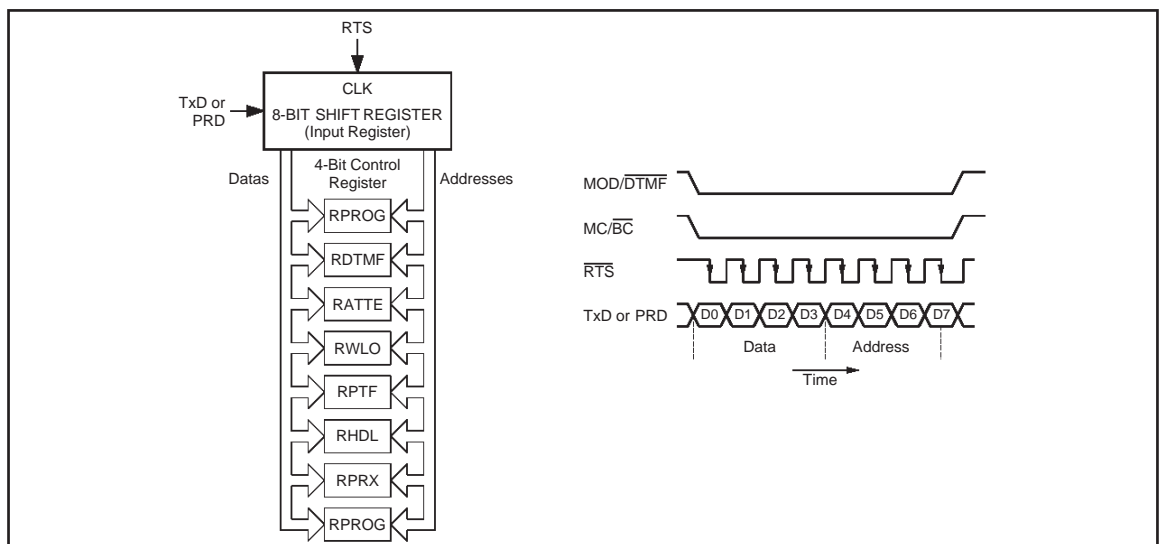
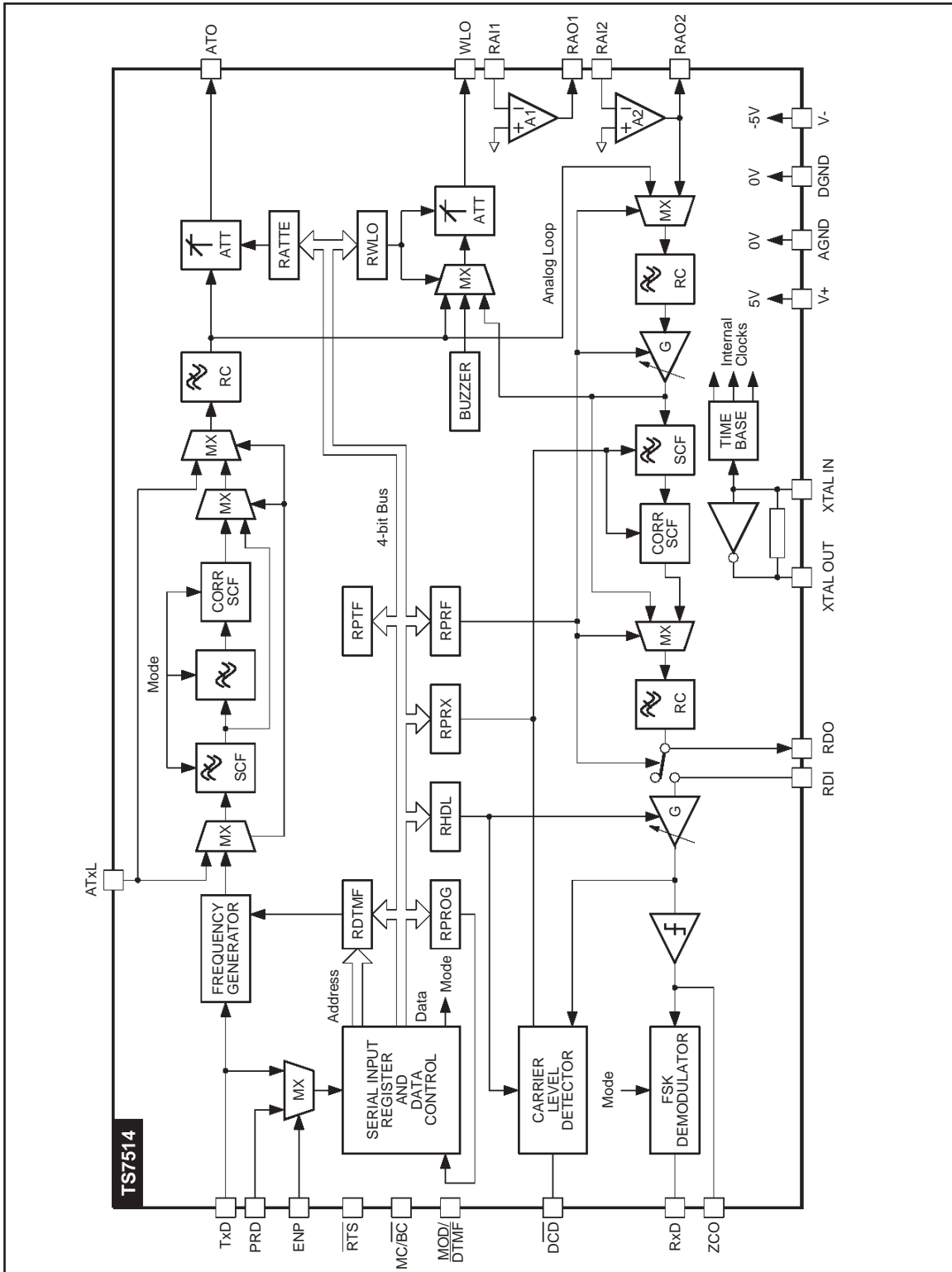


Figure 3 : Detailed Block Diagram



7514-05.EPS

OPERATING MODES

The various operating modes are defined by MC/BC and MOD/DTMF inputs, and by the content of a control register RPROG.

The TS7514 includes 8 control registers. Access to each control register is achieved through an auxiliary 8-bit shift register (input register). The input of that shift register is connected either to TxD or PRD, depending upon the status of the ENP control pin (ie when ENP = 0 and ENP = 1 respectively). In both cases, the RTS input receives the shift clock and sequentially transfer is controlled by setting simultaneously MOD/DTMF and MC/BC to 0. The

previous internal status and data are memorized during loading of the input register so that transmission continues properly. That feature allows the user to modify transmission level or line monitoring selection during transmission. The transmit channel operating mode (Modem main or back channel, DTMF) can only be modified when RTS = 1. When RTS = 0, the ATO transmit output is enabled and the preselected operating mode is activated. When RTS returns to 1, Modem or DTMF transmission is inhibited after the first zero crossing of the generated signal.

MOD/DTMF	MC/BC	Transmission (ATO)	Reception (RxD, DCD)
1	1	MODEM, Main Channel	MODEM, Back Channel
1	0	MODEM, Back Channel	MODEM, Main Channel
0	1	DTMF	DCD= Active Tone Detection (270 -500Hz) if RTS = 1... DCD = 1 if RTS = 0
0	0	If RTS = 0 when that configuration occurs, transmission and reception are not modified. If RTS = 1 (no signal sent on the line), transmission is not modified and reception is set up to detect 2100Hz tone (note 1).	

Note 1 : The decision threshold of the demodulator output is shifted, so that RxD changes from 0 to 1 at 1950Hz instead of 1700Hz.

MODEM TRANSMISSION FREQUENCIES

Modulation Rate	TxD	CCITT R35 AND V.23 Recommendations (Hz)	Frequency Generated with Xtal at 3.579MHz (Hz)	Error (Hz)
75bps	1	390 ±2	390.09	+0.09
	0	450 ±2	450.45	+0.45
1200bps	1	1300 ±10	1299.76	-0.24
	0	2100 ±10	2099.12	-0.88

DTMF TRANSMISSION FREQUENCIES

	Specifications DTMF (Hz)	Frequency Generated with Xtal at 3.579MHz (Hz)	Dividing Ratio	Error (%)
f1	697 ±1.8%	699.13	5120	+0.31
f2	770 ±1.8%	771.45	4640	+0.19
f3	852 ±1.8%	853.90	4192	+0.22
f4	941 ±1.8%	940.01	3808	-0.10
f5	1209 ±1.8%	1209.31	2960	+0.03
f6	1336 ±1.8%	1335.65	2680	-0.03
f7	1477 ±1.8%	1479.15	2420	+0.15
f8	1633 ±1.8%	1627.07	2200	+0.36

CARRIER LEVEL DETECTOR

- Output Level Detection conditions

The DCD signal detector output is set to logic state 0 if the RMS value of the demodulator input signal is greater than N1. The DCD output has logic state 1 if the RMS value is less than N2.

The detector has an hysteresis effect : N1 - N2.

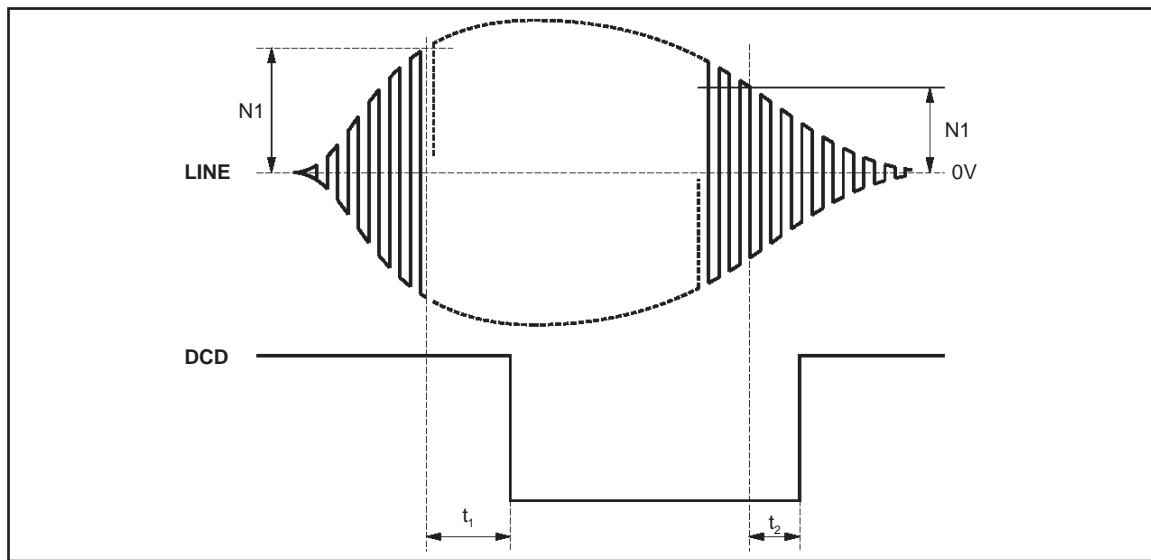
- Timing Detection Requirements

Signal detection time constants at the DCD output comply with CCITT Recommendation V.23.

Modulation Ratio	DCD Transition	CCITT V.23 (min)	Min.	Max.	CCITT V.23 (max)	Unit
1200bps	t1	10	10	20	20	ms
	t2	5	5	15	15	ms
75bps (Note 1)	t1	0	15	40	80	ms
	t2	15	15	40	80	ms

Note 1 : wide band Rx filter used (see Figure 7c).

Figure 4 : Signal Detection Time Out



Note : When delays are bypassed (see RPRX register programming) response time ranges from 0 to 5ms in receive mode at 1200bps, and from 0 to 10ms at 75bps.

PROGRAMMING REGISTER (RPROG)

Address				Data				Selected Mode (note 1)
D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	0 0	X X	0 1	0 1	The most significant bit (D7) is not used when decoding control register addresses.
				0	X	0	1	Control register addressing is enabled when D7 = 0 (see note 2).
				0	X	1	0	Control register addressing is enabled when D7 = 1 (see note 2).
				0	0	X	X	Reception positioned in the channel opposite to the transmission channel controlled by MC/BC
				0	1	X	X	Reception positioned in the same channel as transmission (see note 3).
				1	X	X	X	Programming inhibited in normal operating mode. This mode is used for testing purposes.

Notes : 1. RPROG is set to 0000 on power-up.
 2. Excepted for RPROG register whose address is always 000, regardless of D0 and D1.
 3. This mode allows either full duplex operation on a 4-wire line, or circuit testing with external Tx/Rx loopback.

DTMF DIALING DATA REGISTER (RDTMF REGISTER)

Address				Data				Tone Frequency (Hz)	
D7	D6	D5	D4	D3	D2	D1	D0	Low	High
P	0	0	1	X	X	0	0	697	X
				X	X	0	1	770	X
				X	X	1	0	852	X
				X	X	1	1	941	X
				0	0	X	X	X	1209
				0	1	X	X	X	1336
				1	0	X	X	X	1477
				1	1	X	X	X	1633

Notes : This register is not initialized on power-up.
 X : don't care value.
 P : 1,0 or X depending upon RPROG content.

DATA REGISTER FOR THE TRANSMISSION ATTENUATOR (RATE REGISTER)

Address				Data				Attenuation (dB)	Output Transmit Level (dBm)	On Line Level (dBm) Coupler Gain (- 6dB)
D7	D6	D5	D4	D3	D2	D1	D0			
P	0	1	0	0	0	0	0	0	+ 4	- 2
				0	0	0	1	1		+ 3
				0	0	1	0	2	+ 2	- 4
				0	0	1	1	3	+ 1	- 5
				0	1	0	0	4	0	- 6
				0	1	0	1	5	- 1	- 7
				0	1	1	0	6	- 2	- 8
				0	1	1	1	7	- 3	- 9
				1	0	0	0	8	- 4	- 10
				1	0	0	1	9	- 5	- 11
				1	0	1	0	10	- 6	- 12
				1	0	1	1	11	- 7	- 13
				1	1	0	0	12	- 8	- 14
				1	1	0	1	13	- 9	- 15
				1	1	1	0	Infinite	< - 64	< - 70
				1	1	1	1	Infinite*	< - 64 *	< - 70 *

* Power-up configuration.

LINE MONITORING PROGRAMMING REGISTER (RWLO REGISTER)

Address				Data				Line Monitoring In Transmit Mode Relative Level (dB)	Line Monitoring In Receive Mode Relative Level (dB)
D7	D6	D5	D4	D3	D2	D1	D0		
P	0	1	1	0	0	0	0	- 10	
				0	0	0	1	- 20	
				0	0	1	0	- 31	
				0	0	1	1	- 42	
				0	1	0	0		0
				0	1	0	1		- 10
				0	1	1	0		- 20
				0	1	1	1		- 31
				1	0	0	0		0.42 V _{PP}
				1	0	0	1		- 10dB
				1	0	1	0		- 20dB
				1	0	1	1		- 31dB
				1	1	X	X		< - 60dB*

* Power-up configuration.
Note : Signaling frequency is a square wave signal at 2982Hz.



RECEIVE FILTER SELECTION AND GAIN PROGRAMMING REGISTER (RPRF REGISTER)

Address				Data				Reception Gain (dB) (note 1)	Comments
D7	D6	D5	D4	D3	D2	D1	D0		
P	1	0	1	X	X	0	0	0	
				X	X	0	1	+ 6 *	
				X	X	1	0	+ 12	
				X	X	1	1	0	Rx Channel Band = Tx Channel B and Tx to Rx Loopback – 33dBm ≤ Rx Level ≤ 40dBm
				X	0	X	X	X	Receive Filter Selected
				X	1	X	X	X	Receive Filter Disabled
				1	X	X	X	X	Receive Filter Disconnected from RDI Output and from Demodulator. Offset Disabled.

* Power-up configuration.

Note 1 : Depending on the line length, the received signal can be amplified. Programmable reception gain allows a level close to +3dBm at the filter input to take benefit of the maximum filter dynamic range (S/N ratio). The following requirement must be met : max. line level + prog. gain ≤ +3dBm.

TRANSMISSION FILTER PROGRAMMING REGISTER (RPTF REGISTER)

Address				Data				ATO Transmission
D7	D6	D5	D4	D3	D2	D1	D0	
P	1	0	0	0	0	0	0	MODEM or DTMF Signal*
				0	0	0	1	ATxI via Smoothing Filter and Attenuator
				0	0	1	0	ATxI via Low-pass Filter and Attenuator
				0	0	1	1	ATxI via Band-pass Filter and Attenuator
				0	1	0	0	In DTMF Mode, Transmission of High Tone Frequency
				1	0	0	0	In DTMF Mode, Transmission of Low Tone Frequency

* Power-up configuration.

HYSTERESIS AND SIGNAL DETECTION LEVEL PROGRAMMING REGISTER (RHDL REGISTER)

Address				Data				N2 (dBm) (note 1) See Figure 4	N1/N2 (dB)
D7	D6	D5	D4	D3	D2	D1	D0		
P	1	1	0	X	0	0	0	- 43 *	X
				X	0	0	1	- 41	X
				X	0	1	0	- 39	X
				X	0	1	1	- 37	X
				X	1	0	0	- 35	X
				X	1	0	1	- 33	X
				X	1	1	0	- 31	X
				X	1	1	1	- 29	X
				0	X	X	X	X	3 *
				1	X	X	X	X	3.5

* Power-up configuration.

Note 1 : Detection low level measured at the demodulator input. The line signal detection level is obtained by reducing the gain at the filter.

RECEIVE CHANNEL PROGRAMMING REGISTER (RPRX REGISTER)

Address				Data				Configuration
D7	D6	D5	D4	D3	D2	D1	D0	
P	1	1	1	X	X	0	X	Low Frequency Wide Band Selected (Figure 7b) (Note 1)
				X	X	1	X	Low Frequency Narrow Band Selected (Figure 7c)
				X	X	X	0	Carrier Level Detector Delay Enabled*
				X	X	X	1	Carrier Level Detector Delay Disabled.

Note 1 : In active tone detection mode (MOD/DTMF = 0, MC/BC = 1, RTS = 1 see op. modes), The low frequency wide band is automatically selected for the receive channel, whatever the RPRX register programming value. After a switch back to modem mode (MOD/DTMF = 1, MC/BC = 0 or 1) the RPRX register indicates again the value programmed before the active tone detection mode.

INPUT SHIFT REGISTER ACCESS

Figure 5 : 1st Case : Programmation without Data Transmission

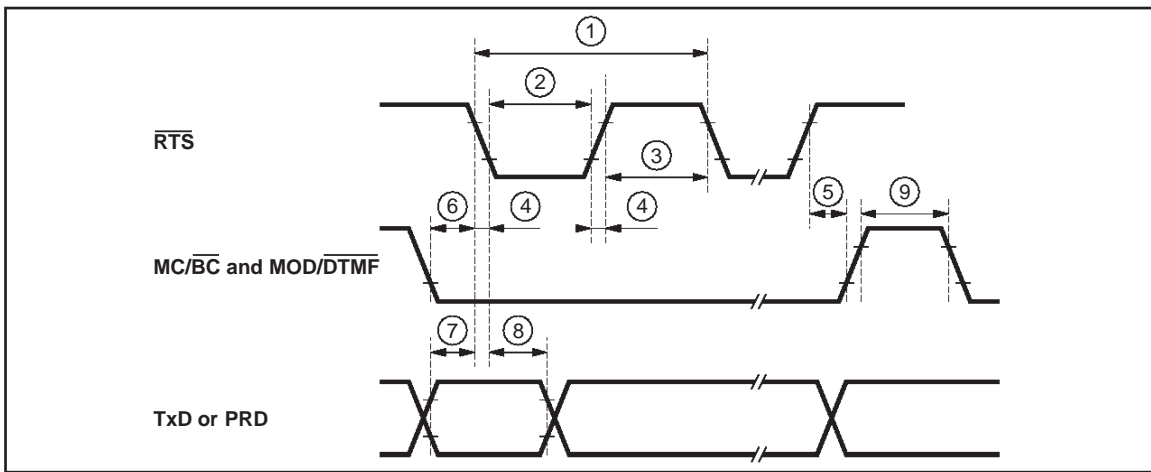
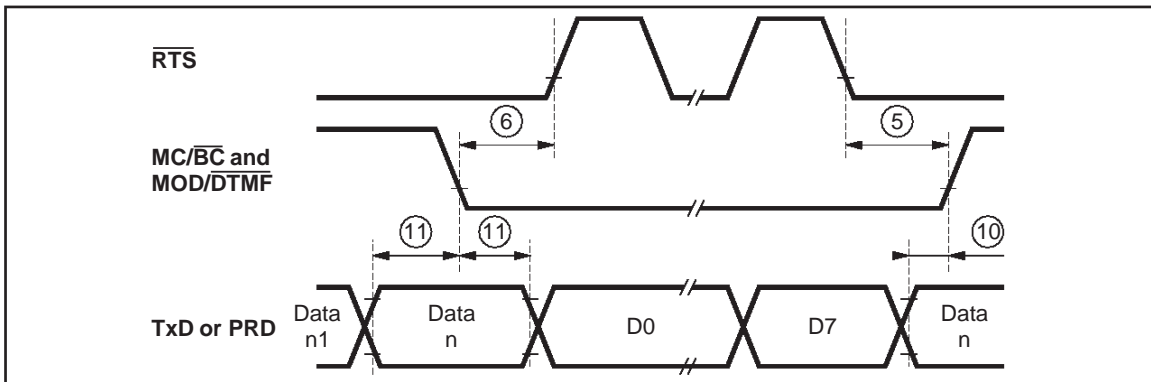


Figure 6 : 2nd Case : Programmation with TxD During Data Transmission



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
DGND	DGND (digital ground) to AGND (analog ground)	- 0.3, + 0.3	V
V+	Supply Voltage V+ to DGND or AGND	- 0.3, + 7	V
V-	Supply Voltage V- to DGND or AGND	- 7, + 0.3	V
V _I	Voltage at any Digital Input	DGND - 0.3, V+ + 0.3	V
V _{in}	Voltage at any Analog Input	V- 0.3, V+ + 0.3	V
I _o	Current at any Digital Output	- 20, + 20	mA
I _{out}	Current at any Analog Output	- 10, + 10	mA
P _{tot}	Power Dissipation	500	mW
T _{op}	Operating Temperature	0, + 70	°C
T _{stg}	Storage Temperature	- 65, + 150	°C
T _{lead}	Lead Temperature (soldering, 10s)	+ 260	°C

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If the Maximum Ratings are exceeded, permanent damage may be caused to the device. This is a stress rating only, and functional operation of the device under these or any other conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to the device.

ELECTRIC OPERATING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V+	Positive Supply Voltage	4.75	5	5.25	V
V-	Negative Supply Voltage	- 5.25	- 5.0	- 4.75	V
I+	V+ Operating Current	-	10	15	mA
I-	V- Operating Current	- 15	- 10	-	mA

7514-04.TBL

DC AND OPERATING CHARACTERISTICS

Electrical characteristics are guaranteed over the complete temperature range, with typical load unless otherwise specified. Typical values are given for : V⁺ = +5V, V⁻ = -5V and room temperature = 25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE (MOD/DTMF, RTS, DCD, RxD, ZCO, TxD, MC/BC, ENP, PRD)						
V _{IL}	Input Voltage, Low Level		-	-	0.8	V
V _{IH}	Input Voltage, High Level		- 2.2	-	-	-
I _{IL}	Input Current, Low Level	DGND < V _I < V _{IL} (max)	- 10	-	10	μA
I _{IH}	Input Current, High Level	V _{IH} (min) < V _I < V+	- 10	-	10	μA
I _{OL}	Output Current, Low Level	V _{OL} = 0.4V	1.6	-	-	mA
I _{OH}	Output Current, High Level	V _{OH} = 2.8V	-	-	- 250	μA

ANALOG INTERFACE-PROGRAMMABLE (ATxI)

V _{in}	Input Voltage Range		- 1.8	-	+ 1.8	V
I _{in}	Input Current (filter output selected)		- 10	-	+ 10	μA
C _{in}	Input Capacitance (ATT output selected)		-	-	20	pF
R _{in}	Input Resistance (ATT output selected)		100	-	-	kΩ

ANALOG INTERFACE - TRANSMIT OUTPUT (ATO) (load conditions R_L = 560Ω, C_L = 100pF)

V _{OS}	Output Offset Voltage		- 250	-	+ 250	mV
C _L	Load Capacitance		-	-	100	pF
R _L	Load Resistance		-	560	-	Ω
V _{out}	Output Voltage Swing		- 1.8	-	+ 1.8	V
R _{out}	Output Resistance		10	-	25	Ω
-	ATO Attenuation Ratio when RTS = 1		70	-	-	dB

7514-05.TBL

DC AND OPERATING CHARACTERISTICS (continued)

Electrical characteristics are guaranteed over the complete temperature range, with typical load unless otherwise specified. Typical values are given for : $V^+ = +5V$, $V^- = -5V$ and room temperature = 25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ANALOG INTERFACE - LINE MONITORING (WLO (load conditions , $R_L = 10k\Omega$, $C_L = 50pF$))						
V_{OS}	Output Offset Voltage		- 250	-	+ 250	mV
C_L	Load Capacitance		-	-	100	pF
R_L	Load Resistance		10	-	-	k Ω
V_{out}	Output Voltage Swing		- 1.8	-	+ 1.8	V
R_{out}	Output Resistance		-	-	15	Ω
-	WLO Attenuation Ratio		70	-	-	dB

ANALOG INTERFACE - DUPLEXER (RAI+, RAI-, RA0)

V_{in}	Input Voltage Range RAI+, RAI-		-2	-	+2	V
I_{in}	Input Current RAI+, RAI-		-10	-	+10	μA
C_{in}	Input Capacitance RAI+, RAI-		-	-	10	pF
V_{off}	Input Offset Voltage RAI+, RAI-		-20	-	+20	mV
V_{out}	Output voltage Swing, RA0	$C_L = 100pF$ $R_L = 300 \Omega$	-1.8 -0.9	$R_L = 600\Omega$ -	+1.8 +0.9	V V
C_L	Load Capacitance RA01	$C_L = 100pF$	-	-	100	pF
R_L	Load Resistance RA01		300	-	-	Ω
G	DC voltage Gain in Large Signals, RA01	$C_L = 100pF$, $R_L = 300\Omega$	60	-	-	dB
CMRR	Common Mode Rejection Ratio, RA01, RA02		60	-	-	dB
PSRR	Supply Voltage Rejection Ratio, RA01, RA02		60	-	-	dB
V_{out}	Output Voltage Swing, RA02	$C_L = 50pF$, $R_L = 10k\Omega$	-2.5	-	2.5	pF
C_L	Load Capacitance, RA02		-	-	50	pF
R_L	Load Resistance, RA02		10	-	-	k Ω
AV_O	DC Voltage Gain in Large Signals, RA02		-	-	-	dB

ANALOG INTERFACE-RECEIVE FILTER OUTPUT (RFO)
Amplifier Limiter Input (RDI)

V_{in}	Input Voltage Range (RPRF = 1 xxx)		- 2.2	-	+ 2.2	V
R_{in}	Input Resistance (RPRF = 1 xxx)		1.5	-	-	k Ω
C_{in}	Input Capacitance (RPRF = 1 xxx)		-	-	20	pF
C_L	Load Capacitance (RPRF = 1 xxx)		-	-	50	pF
R_L	Load Resistance		1.5	-	-	k Ω
V_{out}	Output Voltage Swing	$C_L = 50pF$, $R_L = 1.5k\Omega$	- 1.8	-	+ 1.8	V
R_{out}	Output Resistance		-	-	15	Ω

DYNAMIC CHARACTERISTICS FOR PROGRAMMING REGISTER ACCESS (see Figures 5 and 6)

t_{CYC} (1)	Cycle Time		600	-	-	ns
P_{wel} (2)	Pulse Width, \overline{RTS} Low		300	-	-	ns
P_{Weh} (3)	Pulse Width, \overline{RTS} High		300	-	-	ns
t_r , t_f (4)	\overline{RTS} Rise and Fall Times		-	-	50	ns
t_{HCE} (5)	Control Input Holding Time		100	-	-	ns
t_{SCE} (6)	Control Input Setup Time		300	-	-	ns
t_{SDI} (7)	TxD or PRD Input Setup Time		200	-	-	ns
t_{HDI} (8)	TxD or PRD Input Hold Time		100	-	-	ns
t_{WW} (9)	TWW Input Writing Impulsion Width (high level)		300	-	-	ns
t_{BD} (10)	TxD Input Setup Time		100	-	-	ns
t_{HD} (11)	TxD Input Hold Time		100	-	-	ns

7514-06.TBL

DC AND OPERATING CHARACTERISTICS (continued)

Electrical characteristics are guaranteed over the complete temperature range, with typical load unless otherwise specified. Typical values are given for : $V^+ = +5V$, $V^- = -5V$ and room temperature = 25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TRANSMIT FILTER TRANSFER FUNCTION (load conditions : $R_L = 560\Omega$, $C_L = 100pF$)						
G_{AR}	Absolute Gain at 2100Hz		-	0	-	dB
G_{HH}	Gain Relative to Gain at 1700Hz	Band-pass < 390Hz = 390Hz = 450Hz = 1100Hz Band-pass or Low-pass 1100Hz to 2300Hz 3300Hz 5800Hz > 16000Hz	- - - -0.5 -0.5 - - -	- - - - - -3 - -	-30 -35 -35 +0.5 +0.5 - -15 -35	dB dB dB dB dB dB dB dB
D_{AR}	Group Delay (modem transmission) Main Channel : from 380 to 460Hz Back Channel : from 1100 to 2300Hz		90 1.04	- -	110 1.08	μs ms

ATTENUATOR TRANSFER FUNCTION

A_{TT}	Absolute Gain for 0dB Programmed		0.3	0	0.3	dB
R_{AT}	Attenuation Relative to Programmed Value Attenuation for Programmed Value = ∞		-0.5 70	- -	+0.5	dB dB
R_{LT}	Relative Attenuation between two Consecutive Steps		0.8	-	1.2	dB

TRANSMIT GENERAL CHARACTERISTICS

	Modem Amplitude (Att = 0dB)	390Hz 450Hz 1300Hz 2100Hz	+3.5 +3.5 +3.5 +3.5	- - - -	+4.5 +4.5 +4.5 +4.5	dBm dBm dBm dBm
	DTMF Amplitude (Att = 0dB) - Low Frequency Group - Low Frequency Group versus Low Frequency Group		-3 +1.5	- -	-1.5 +2.5	dBm dB
	Psophometric Noise		-	-	250	μV

RECEIVE FILTER TRANSFER FUNCTION

G_{AR}	Absolute Gain at 1100Hz - Main Channel (0dB programmed)		-0.5	-	+0.5	dB
G_{RR}	Gain Relative to the Gain at 1300Hz (0dB programmed)	< 150Hz 150Hz to 450Hz 1300Hz 2100Hz 2300Hz 5500Hz to 10000Hz > 10000Hz	- - -0.5 1.1 - - -	- - - 1.8 - - -	-60 -50 0.5 2.3 2.7 -50 -60	dB dB dB dB dB dB dB
G_{AR}	Absolute Gain at 420Hz (back channel - narrow band) (0dB programmed)		0.5	-	+0.5	dB
G_{RR}	Gain Relative to Gain at 420Hz (0dB programmed)	< 150Hz 380Hz 400Hz to 440Hz 460Hz 1100Hz to 10000Hz > 10000Hz	- - -0.5 - - -	- - - - - -	-50 +0.5 +0.5 +0.5 -50 -60	dB dB dB dB dB dB
G_{AR}	Absolute Gain at 425Hz (tone detection or back channel wide band) (0dB programmed)		-0.5	-	+0.5	dB
G_{RR}	Gain Relative to Gain at 425Hz (0dB programmed)	< 112Hz 275Hz 300Hz to 525Hz 575Hz 1375Hz to 10000Hz > 10000Hz	- - -0.5 - - -	- - - - - -	-50 +0.5 +0.5 +0.5 -50 -60	dB dB dB dB dB dB
	Psophometric Noise		-	-	300	μV

7514-07.TBL

DC AND OPERATING CHARACTERISTICS (continued)

Electrical characteristics are guaranteed over the complete temperature range, with typical load unless otherwise specified. Typical values are given for : $V^+ = +5V$, $V^- = -5V$ and room temperature = $25^{\circ}C$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

RECEIVE TRANSFER - GENERAL CHARACTERISTICS

	Absolute Filter Gain for : 0dB programmed 6dB programmed 12dB programmed		- 0.5 + 5.5 + 11.5	- - -	+ 0.5 + 6.5 12.5	dB
R _{DS}	Signal Detection Level Relative to Programmed Value		- 0.5	-	+ 0.5	dB
R _{HY}	Hysteresis Value		- 2	-	-	dB
	Signal Level (loop 3) at Reception Input		- 40	- 35	- 33	dBm

LINE MONITORING - GENERAL CHARACTERISTICS (load conditions : $R_L = 10k\Omega$, $C_L = 50pF$)

A _{TT}	Absolute Gain for 0dB Programmed		-	0	-	dB
R _{AT} -	Attenuation Relative to Programmed Value Attenuation for Programmed Value		- 1 70	- -	+ 1	dB dB
FS	Buzzer Signalling Frequency		-	2982	-	Hz
	Signalling Frequency Amplitude at 0.42V _{PP} Programmed		0.38	0.42	0.46	V _{PP}

7514-08.TBL

Receive Filter Transfer Characteristics

Figure 7a : Main Channel

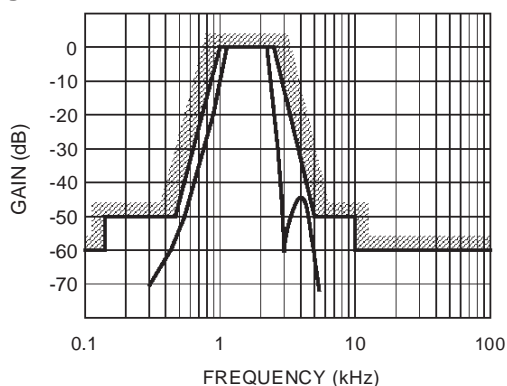


Figure 7b : Back Channel - Narrow Band

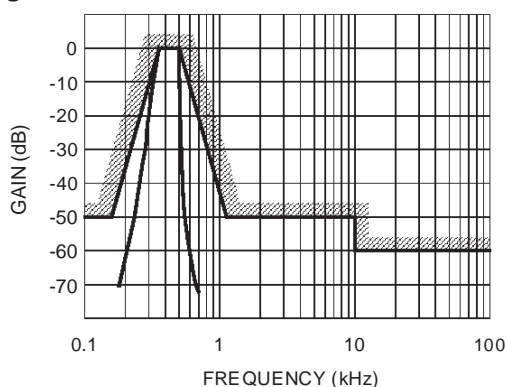
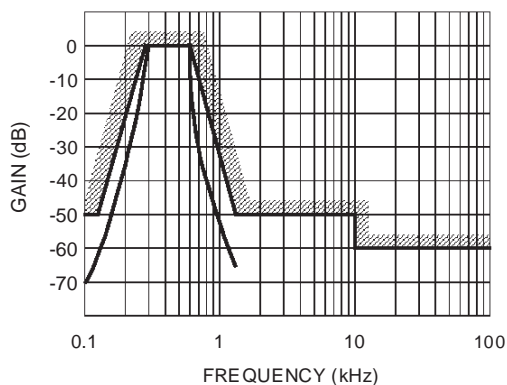
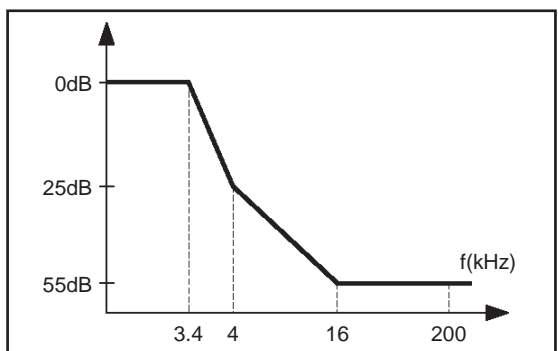


Figure 7c : Basic Channel
Wide band and Tone Detection



Transmission Spectrum

At the ATO output, the out-of-band signal power conforms to the following specifications :



Receiver

Measurement conditions
Local transmit level : -10dBm on lower channel at 75bps.
Receive level : -25dBm, with 511 bit pseudo-random test pattern.
Test equipment : TRT sematest.

Isochronous distortion

The following table shows typical isochronous distortion obtained with the TS7514 circuit :

Line	Reception (1200)	Reception (75)
Line 1 (fiat)	10 %	4 %
Line 2	12 %	4 %
Line 3	18 %	6 %
Line 4	14 %	6 %

Bit error rate

Typical bit error rates versus while noise are as follows (noise and signal levels are measured without weighting on the 300/3400Hz) :

	Reception (1200)		Reception (75)	
	S/N	BER	S/N	BER
Line 1	6 dB	2.10^{-3}	- 3 dB	2.10^{-3}
Line 2	7 dB	2.10^{-3}	- 3 dB	2.10^{-3}
Line 3	8 dB	2.10^{-3}	- 3 dB	2.10^{-3}
Line 4	7 dB	2.10^{-3}	- 3 dB	2.10^{-3}

CHARACTERISTICS OF TEST LINES

Figure 8

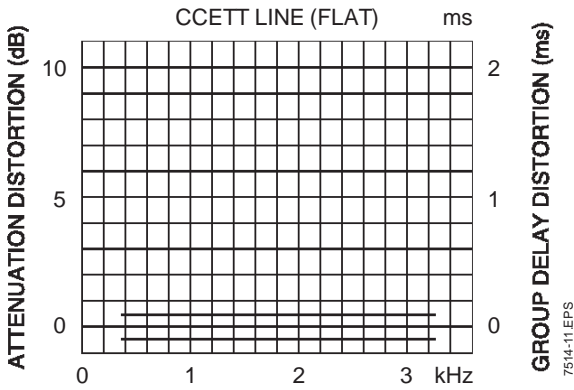


Figure 9

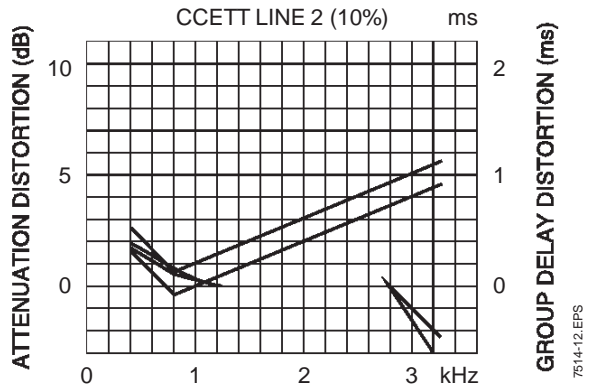


Figure 10

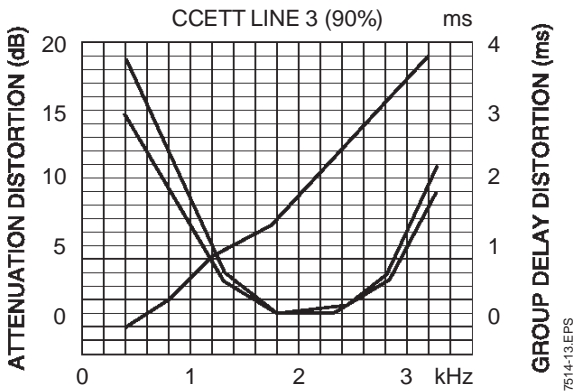
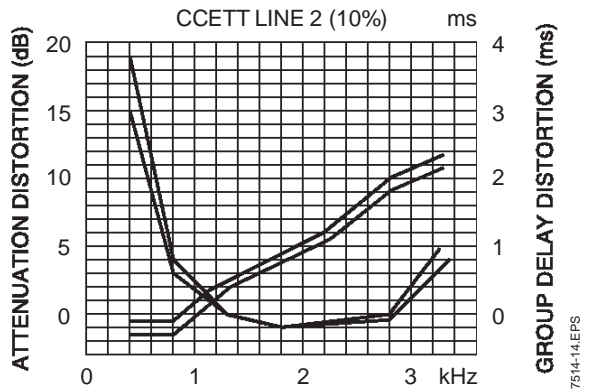
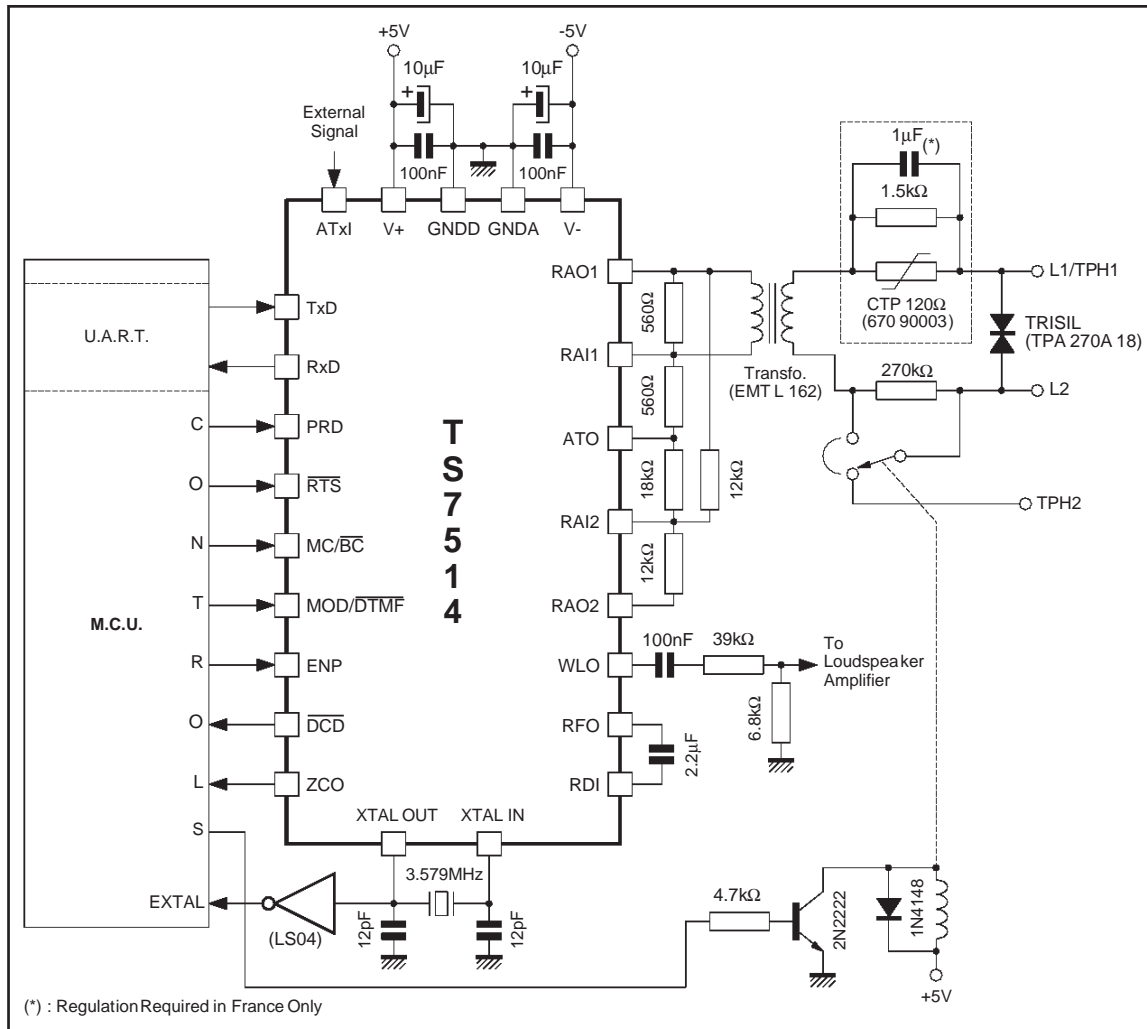


Figure 11



TYPICAL APPLICATION INFORMATION



7514-15.EPS

POWER SUPPLIES DECOUPLING AND LAYOUT CONSIDERATIONS

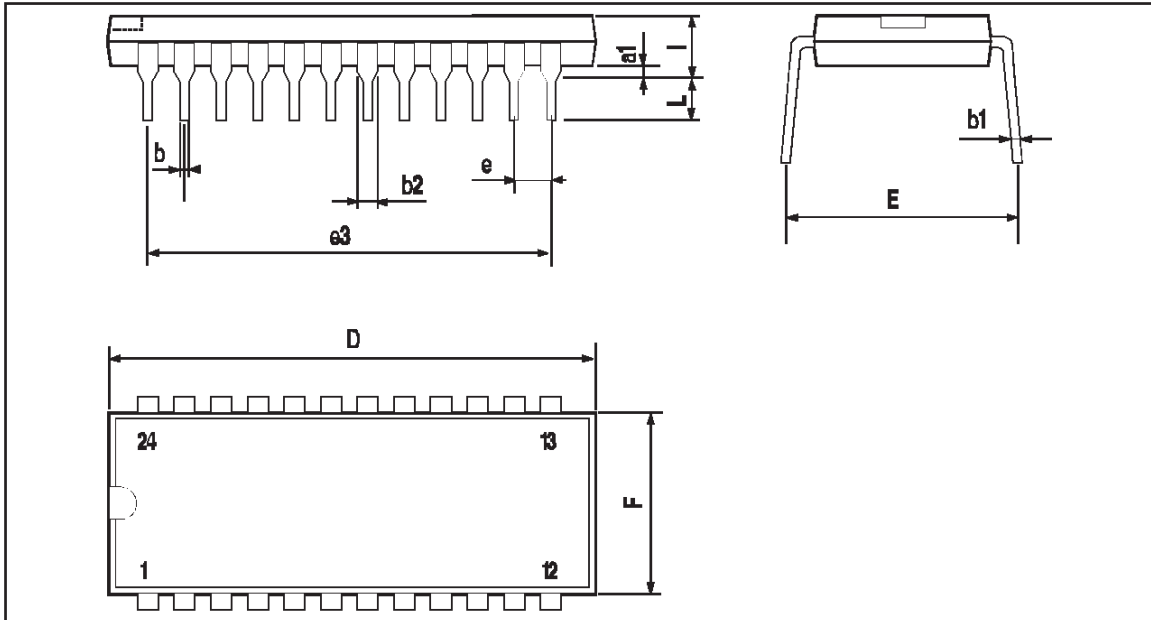
Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performances of the TS7514 operating in close proximity to digital systems, supply and ground noise should be minimized.

This involves attention to power supply design and circuit board layout.

The power supplies should be bypassed with tantalum or electrolytic capacitors to obtain noise free operation. These capacitors should be located close to the TS7514. The electrolytic type capacitors for improved high frequency performance.

Power supplies connections should be short and direct. Ground loops should be avoided.

PACKAGE MECHANICAL DATA
24 PINS - PLASTIC DIP

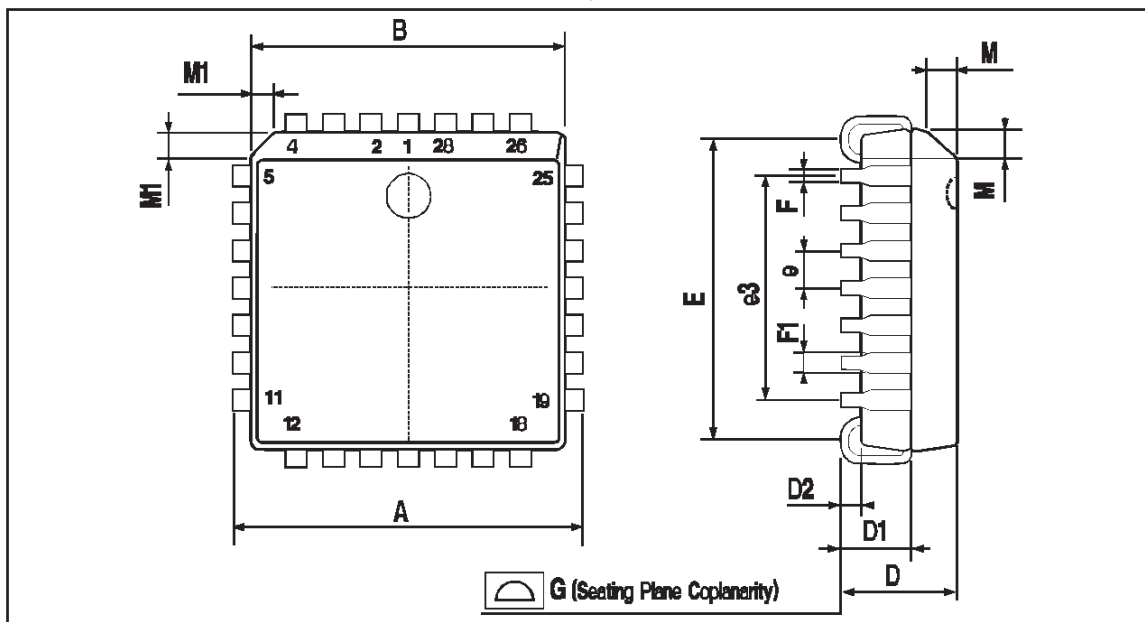


PM-DIP24.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
l		4.445			0.175	
L		3.3			0.130	

DIP24.TBL

PACKAGE MECHANICAL DATA
28 PINS - PLASTIC LEADED CHIP CARRIER PLCC)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

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