

MSM51V18165F

1,048,576-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM51V18165F is a 1,048,576-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM51V18165F achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM51V18165F is available in a 42-pin plastic SOJ or 50/44-pin plastic TSOP.

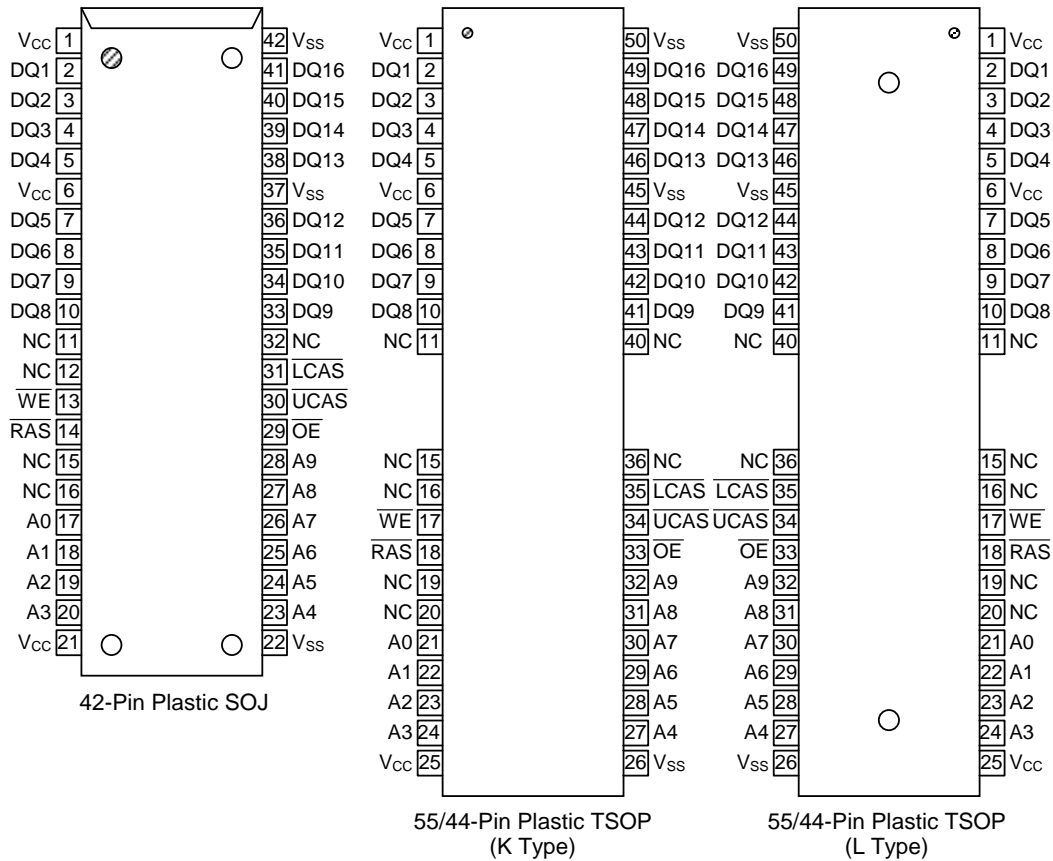
FEATURES

- 1,048,576-word × 16-bit configuration
 - Single 3.3V power supply, ±0.3V tolerance
 - Input : LVTTL compatible, low input capacitance
 - Output : LVTTL compatible, 3-state
 - Refresh : 1024 cycles/16ms
 - Fast page mode with EDO, read modify write capability
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh capability
 - Package options:
 - 42-pin 400mil plastic SOJ (SOJ42-P-400-1.27) (Product : MSM51V18165F-xxJS)
 - 50/44-pin 400mil plastic TSOP (TSOPII50/44-P-400-0.80-K) (Product : MSM51V18165F-xxTS-K)
 - (TSOPII50/44-P-400-0.80-L) (Product : MSM51V18165F-xxTS-L)
- xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MSM51V18165F	50ns	25ns	13ns	13ns	84ns	324mW	1.8mW
	60ns	30ns	15ns	15ns	104ns	288mW	
	70ns	35ns	20ns	20ns	124ns	252mW	

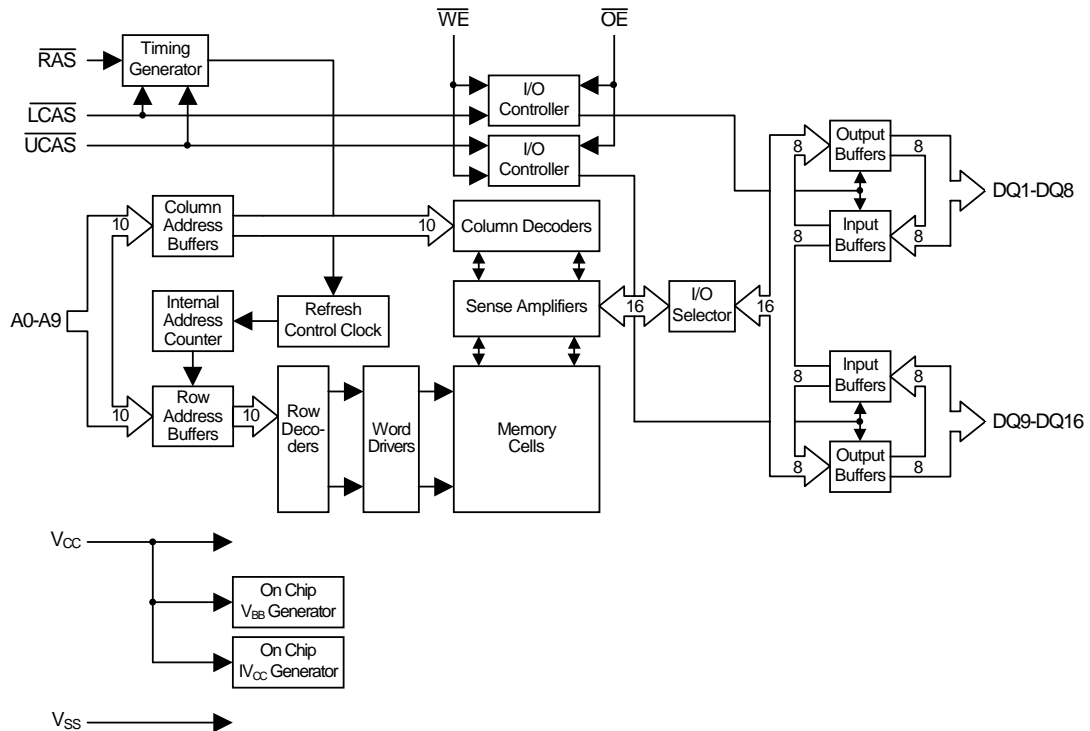
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0–A9	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{LCAS}}$	Lower Byte Column Address Strobe
$\overline{\text{UCAS}}$	Upper Byte Column Address Strobe
DQ1–DQ16	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V_{CC}	Power Supply (3.3V)
V_{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
RAS	LCAS	UCAS	WE	OE	DQ1-DQ8	DQ9-DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D _{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D _{OUT}	Upper Byte Read
L	L	L	H	L	D _{OUT}	D _{OUT}	Word Read
L	L	H	L	H	D _{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D _{IN}	Upper Byte Write
L	L	L	L	H	D _{IN}	D _{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

* : "H" or "L"

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	- 0.5 to $V_{CC} + 0.3$	V
Voltage V_{CC} Supply relative to V_{SS}	V_{CC}	- 0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_{D^*}	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	- 55 to 150	°C

*: $T_a = 25^{\circ}\text{C}$

Recommended Operating Conditions

($T_a = 0^{\circ}\text{C}$ to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC} + 0.3^{*1}$	V
Input Low Voltage	V_{IL}	- 0.3 ^{*2}	—	0.8	V

Notes: *1. The input voltage is $V_{CC} + 1.0\text{V}$ when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is $V_{SS} - 1.0\text{V}$ when the pulse width is less than 20ns (the pulse width respect to the point at which V_{SS} is applied).

Capacitance

($V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $T_a = 25^{\circ}\text{C}$, $f=1\text{MHz}$)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	7	pF

DC Characteristics

($V_{CC} = 3.3V \pm 0.3V$, $T_a = 0^\circ C$ to $70^\circ C$)

Parameter	Symbol	Condition	MSM51V18165 F-50		MSM51V18165 F-60		MSM51V18165 F-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -2.0mA$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 2mA$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	$0V \leq V_I \leq V_{CC}+0.3V$; All other pins not under test = $0V$	- 10	10	- 10	10	- 10	10	μA	
Output Leakage Current	I_{LO}	DQ disable $0V \leq V_O \leq V_{CC}$	- 10	10	- 10	10	- 10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	\overline{RAS} , \overline{CAS} cycling, $t_{RC} = \text{Min.}$	—	90	—	80	—	70	mA	1,2
Power Supply Current (Standby)	I_{CC2}	\overline{RAS} , $\overline{CAS} = V_{IH}$	—	2	—	2	—	2	mA	1
		\overline{RAS} , $\overline{CAS} \geq V_{CC} - 0.2V$	—	0.5	—	0.5	—	0.5		
Average Power Supply Current (\overline{RAS} -only Refresh)	I_{CC3}	\overline{RAS} cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = \text{Min.}$	—	90	—	80	—	70	mA	1,2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current (\overline{CAS} before \overline{RAS} Refresh)	I_{CC6}	$\overline{RAS} = \text{cycling}$, \overline{CAS} before \overline{RAS}	—	90	—	80	—	70	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS} = V_{IL}$, \overline{CAS} cycling, $t_{HPC} = \text{Min.}$	—	90	—	80	—	70	mA	1,3

- Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. The address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. The address can be changed once or less while $\overline{CAS} = V_{IH}$.

AC Characteristic (1/2)

($V_{CC} = 3.3V \pm 0.3V$, $T_a = 0^\circ C$ to $70^\circ C$) Note1,2,3

Parameter	Symbol	MSM51V18165 F-50		MSM51V18165 F-60		MSM51V18165 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	84	—	104	—	124	—	ns	
Read Modify Write Cycle Time	t_{RWC}	110	—	135	—	160	—	ns	
Fast Page Mode Cycle Time	t_{HPC}	20	—	25	—	30	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{HPRWC}	58	—	68	—	78	—	ns	
Access Time from \overline{RAS}	t_{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from \overline{CAS}	t_{CAC}	—	13	—	15	—	20	ns	4,5
Access Time from Column Address	t_{AA}	—	25	—	30	—	35	ns	4,6
Access Time from \overline{CAS} Precharge	t_{CPA}	—	30	—	35	—	40	ns	4,13
Access Time from \overline{OE}	t_{OEA}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from \overline{CAS}	t_{CLZ}	0	—	0	—	0	—	ns	4
Data Output Hold After \overline{CAS} Low	t_{DOH}	5	—	5	—	5	—	ns	
\overline{CAS} to Data Output Buffer Turn-off Delay Time	t_{CEZ}	0	13	0	15	0	20	ns	7,8
\overline{RAS} to Data Output Buffer Turn-off Delay Time	t_{REZ}	0	13	0	15	0	20	ns	7,8
\overline{OE} to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	13	0	15	0	20	ns	7
\overline{WE} to Data Output Buffer Turn-off Delay Time	t_{WEZ}	0	13	0	15	0	20	ns	7
Transition Time	t_T	1	50	1	50	1	50	ns	3
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	
\overline{RAS} Precharge Time	t_{RP}	30	—	40	—	50	—	ns	
\overline{RAS} Pulse Width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
\overline{RAS} Pulse Width (Fast Page Mode with EDO)	t_{RASP}	50	100,000	60	100,000	70	100,000	ns	
\overline{RAS} Hold Time	t_{RSH}	7	—	10	—	13	—	ns	
\overline{RAS} Hold Time referenced to \overline{OE}	t_{ROH}	7	—	10	—	13	—	ns	
\overline{CAS} Precharge Time (Fast Page Mode with EDO)	t_{CP}	7	—	10	—	10	—	ns	15
\overline{CAS} Pulse Width	t_{CAS}	7	10,000	10	10,000	13	10,000	ns	
\overline{CAS} Hold Time	t_{CSH}	35	—	40	—	45	—	ns	
\overline{CAS} to \overline{RAS} Precharge Time	t_{CRP}	5	—	5	—	5	—	ns	13
\overline{RAS} Hold Time from \overline{CAS} Precharge	t_{RHCP}	30	—	35	—	40	—	ns	13

AC Characteristic (2/2)

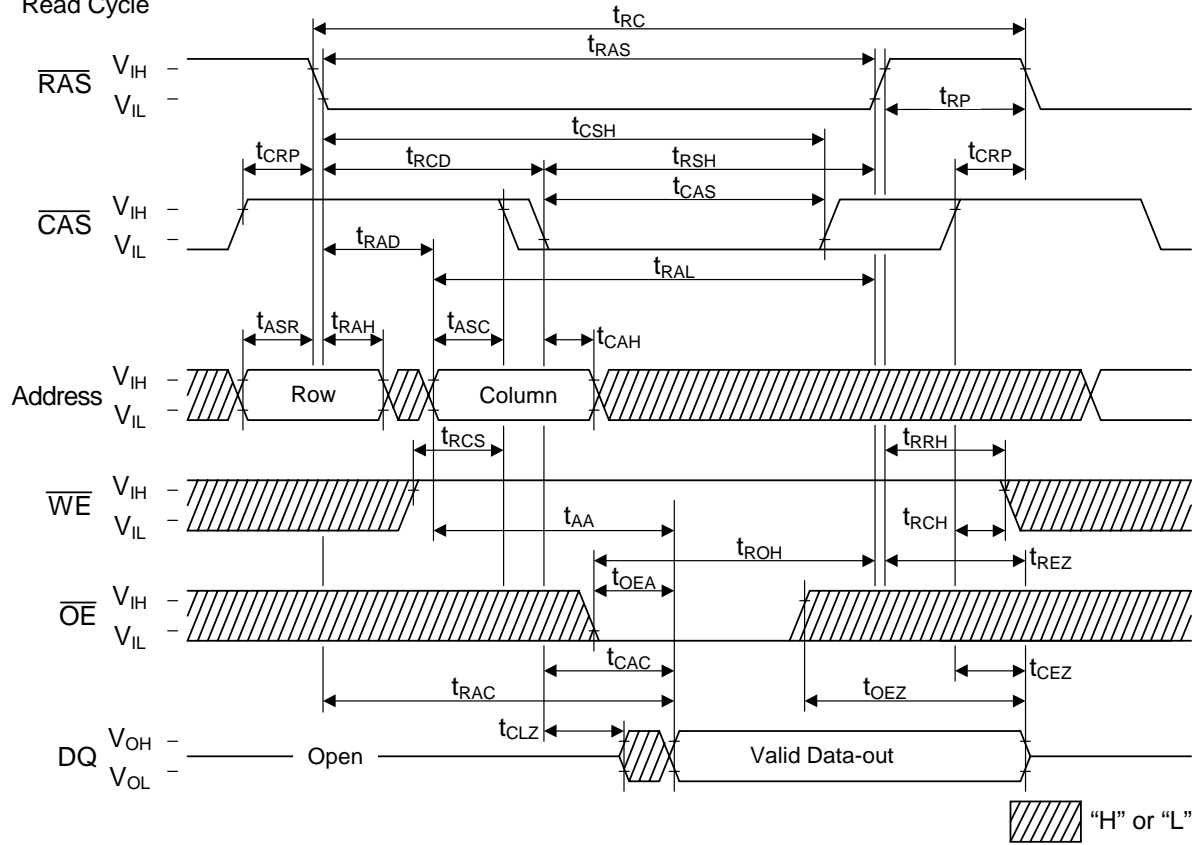
(V_{CC} = 3.3V ± 0.3V, T_a = 0°C to 70°C) Note1,2,3

Parameter	Symbol	MSM51V18165 F-50		MSM51V18165 F-60		MSM51V18165 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{\text{OE}}$ Hold Time from $\overline{\text{CAS}}$ (DQ Disable)	t _{CHO}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	11	37	14	45	14	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	9	25	12	30	12	35	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	12
Column Address Hold Time	t _{CAH}	7	—	10	—	13	—	ns	12
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	25	—	30	—	35	—	ns	
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	12
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	9,12
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	10,12
Write Command Hold Time	t _{WCH}	7	—	10	—	13	—	ns	12
Write Command Pulse Width	t _{WP}	7	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Pulse Width (DQ Disable)	t _{WPE}	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	7	—	10	—	13	—	ns	
$\overline{\text{OE}}$ Precharge Time	t _{OEP}	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OCH}	7	—	10	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	7	—	10	—	13	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	7	—	10	—	13	—	ns	14
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	11,12
Data-in Hold Time	t _{DH}	7	—	10	—	13	—	ns	11,12
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OED}	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	30	—	34	—	44	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	42	—	49	—	59	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	67	—	79	—	94	—	ns	10
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	47	—	54	—	64	—	ns	10
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time (CAS before RAS)	t _{CSR}	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time (CAS before RAS)	t _{CHR}	10	—	10	—	10	—	ns	13

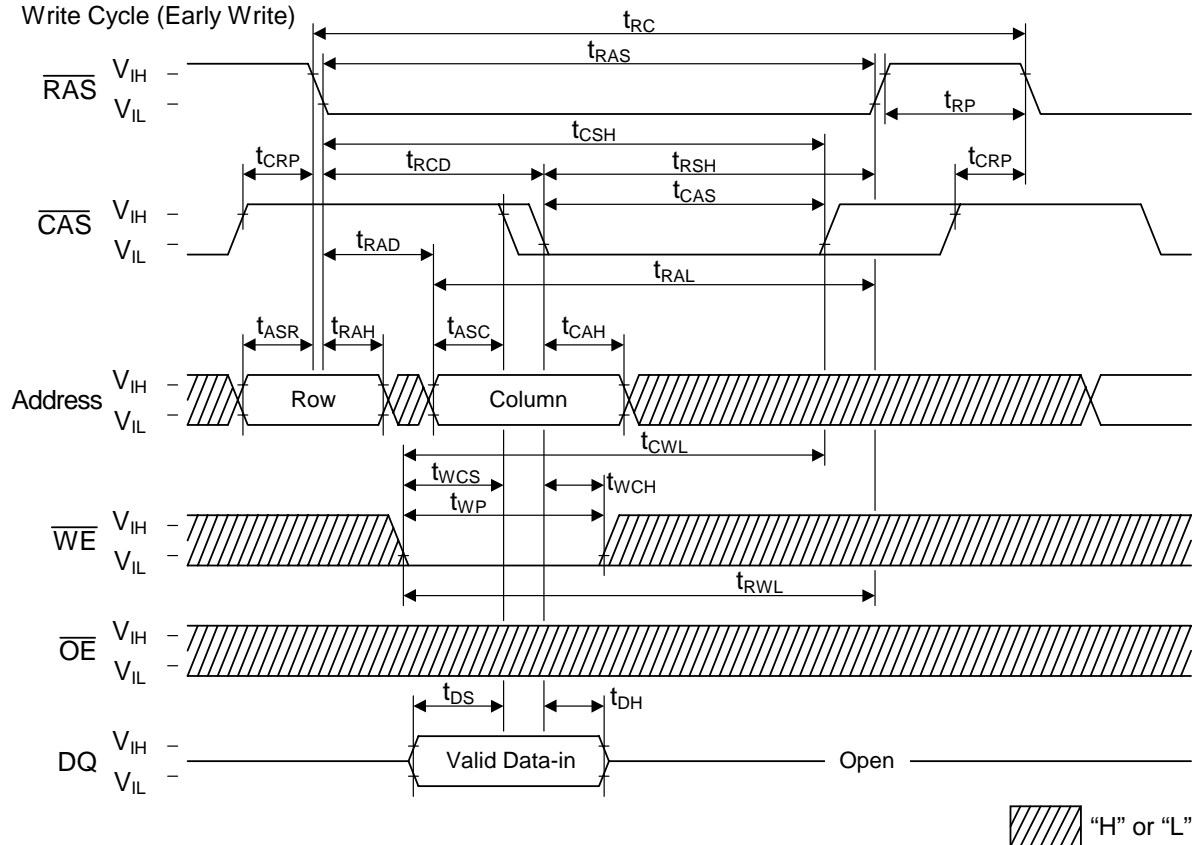
- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 2\text{ns}$.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100pF. The output timing reference levels are $V_{OH} = 2.0\text{V}$ and $V_{OL} = 0.8\text{V}$.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.), and t_{OEZ} (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} , and t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$, leading edges in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.
 12. These parameters are determined by the falling edge of either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, whichever is earlier.
 13. These parameters are determined by the rising edge of either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, whichever is later.
 14. t_{CWL} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
 15. t_{CP} is determined by the time both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.

Timing Chart

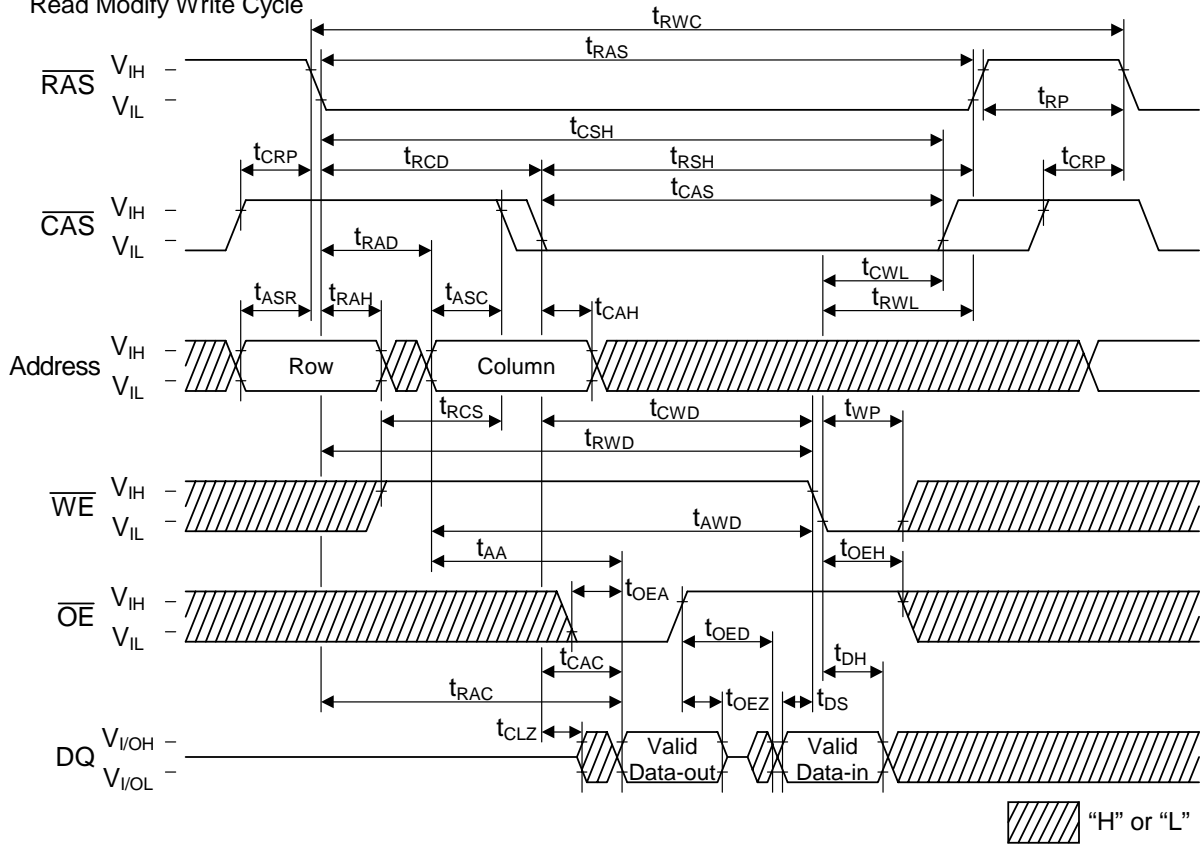
- Read Cycle



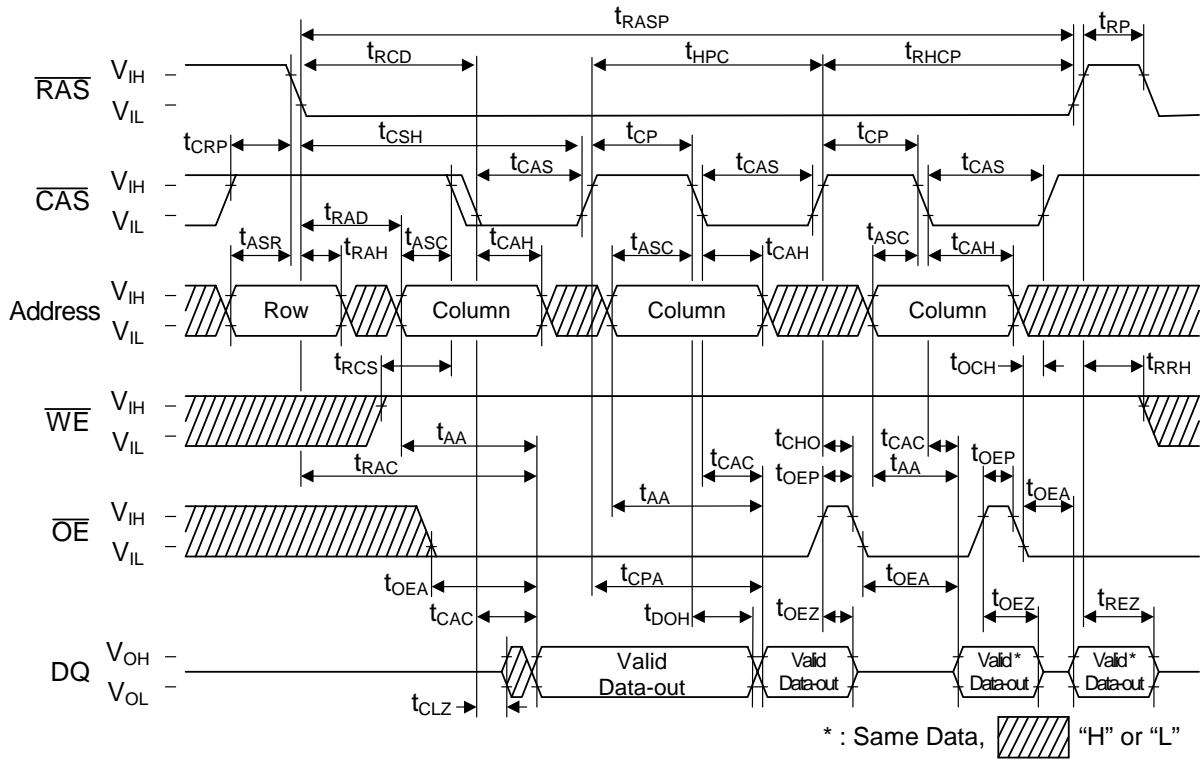
- Write Cycle (Early Write)



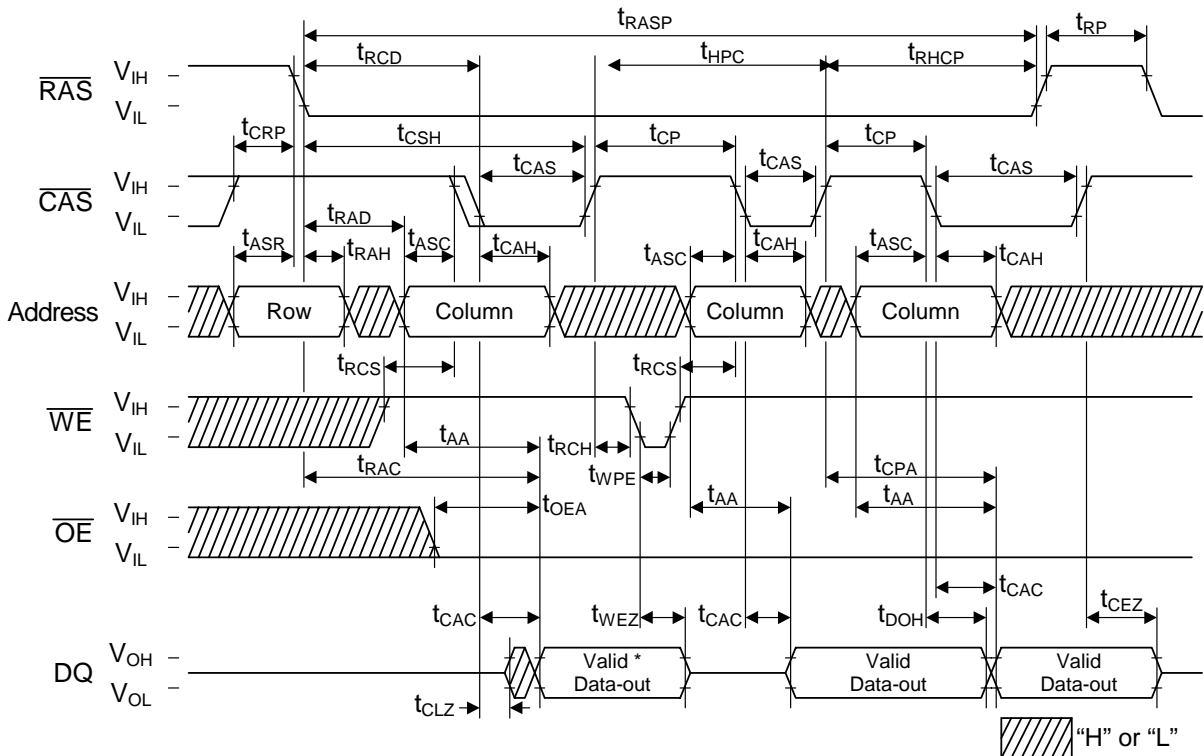
- Read Modify Write Cycle



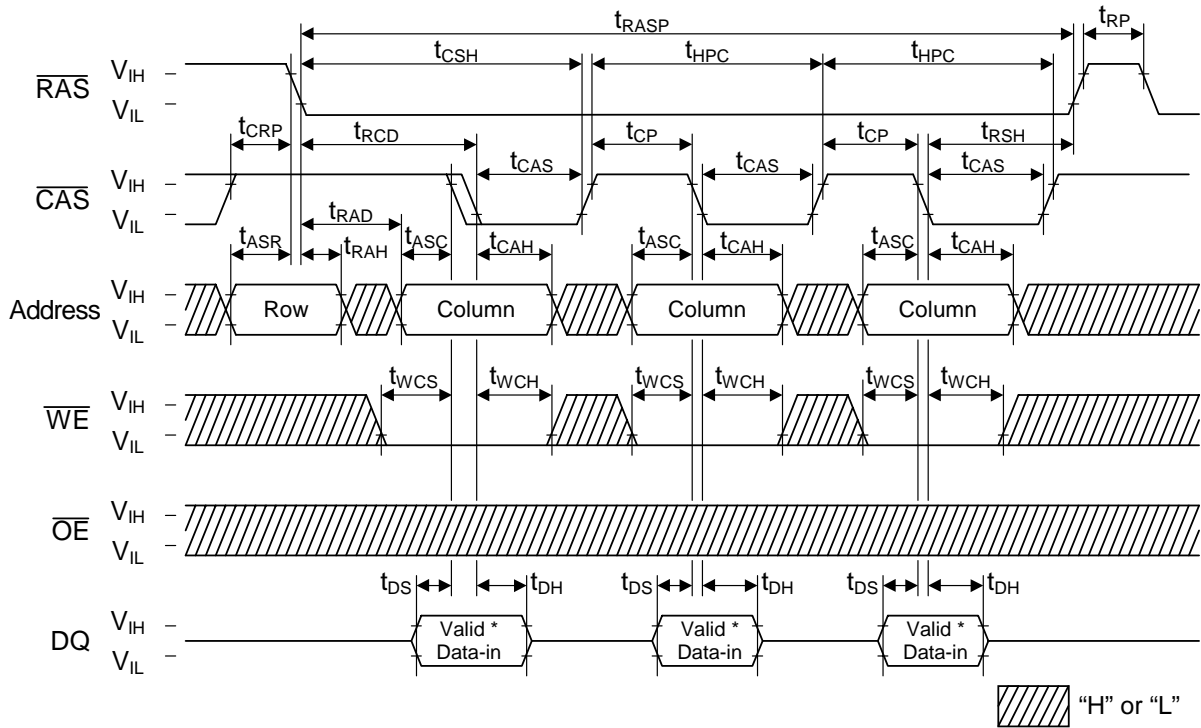
- Fast Page Mode Read Cycle (Part-1)



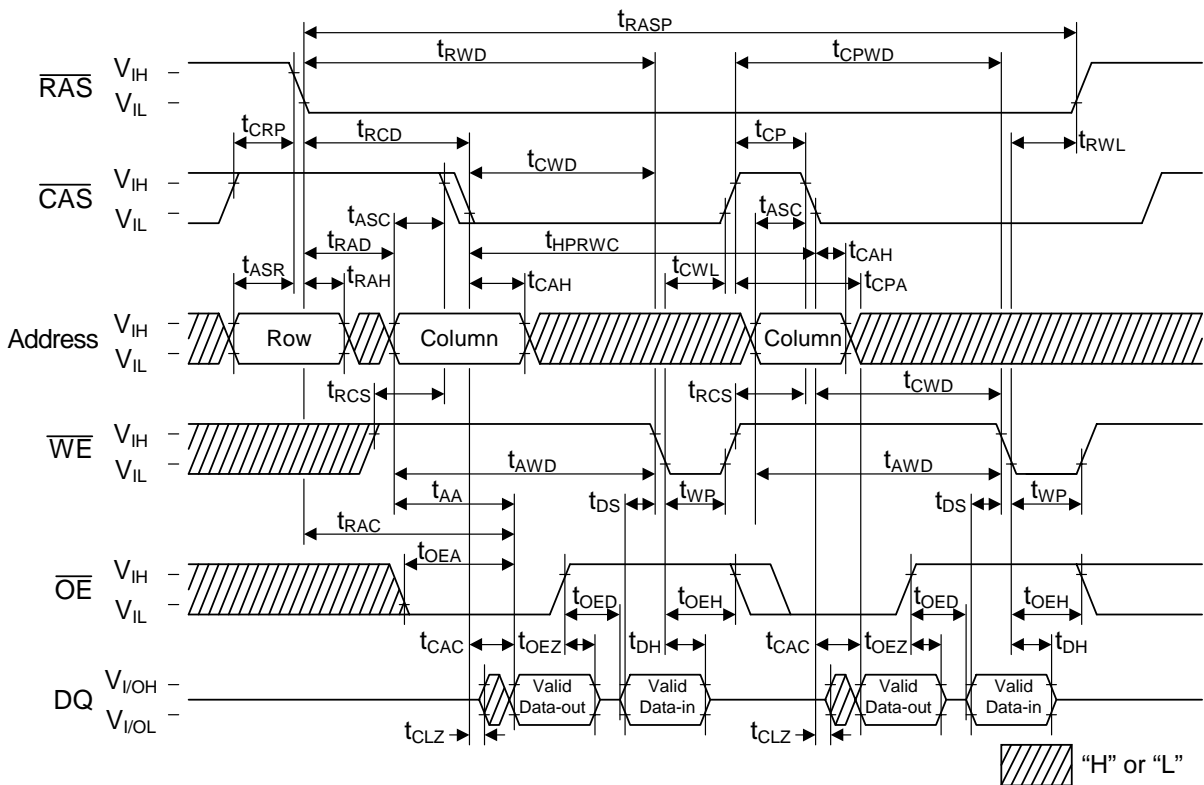
- Fast Page Mode Read Cycle (Part-2)



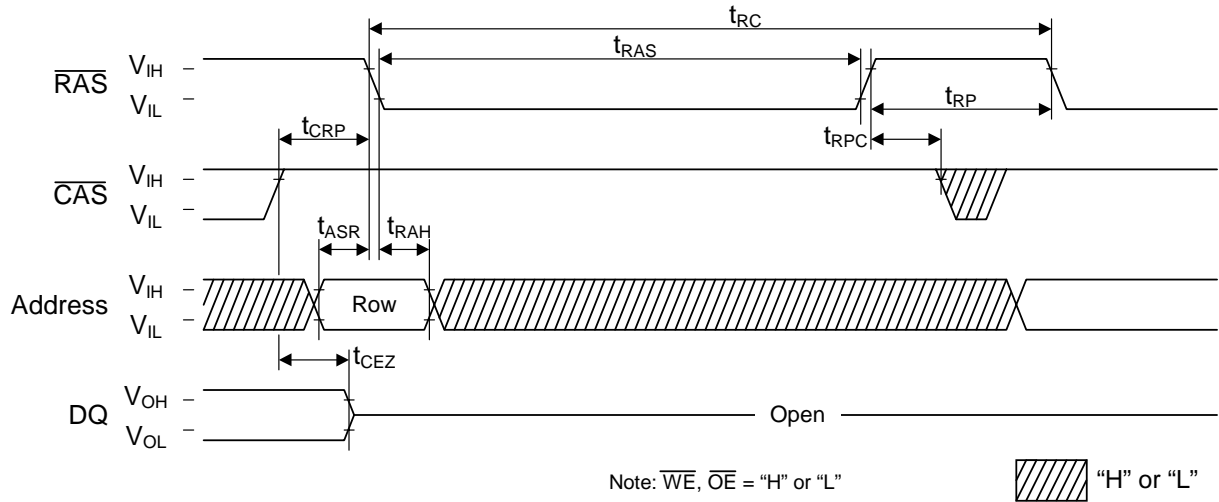
- Fast Page Mode Write Cycle (Early Write)



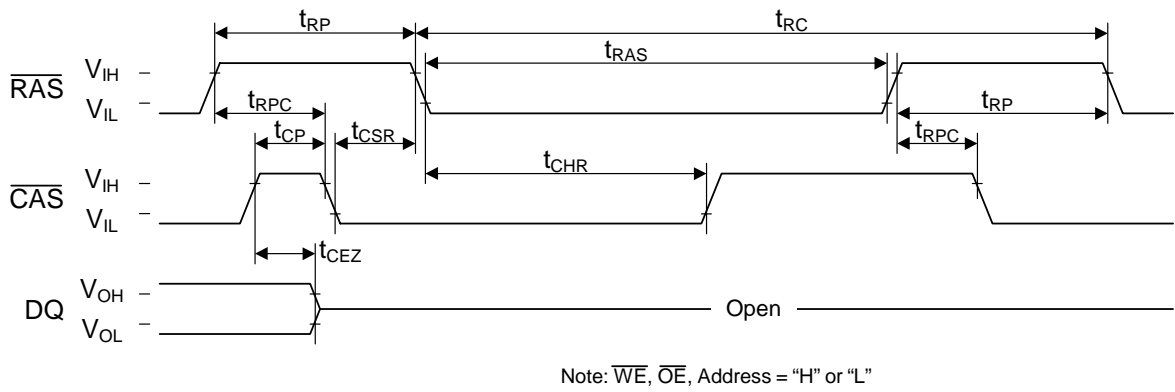
- Fast Page Mode Read Modify Write Cycle



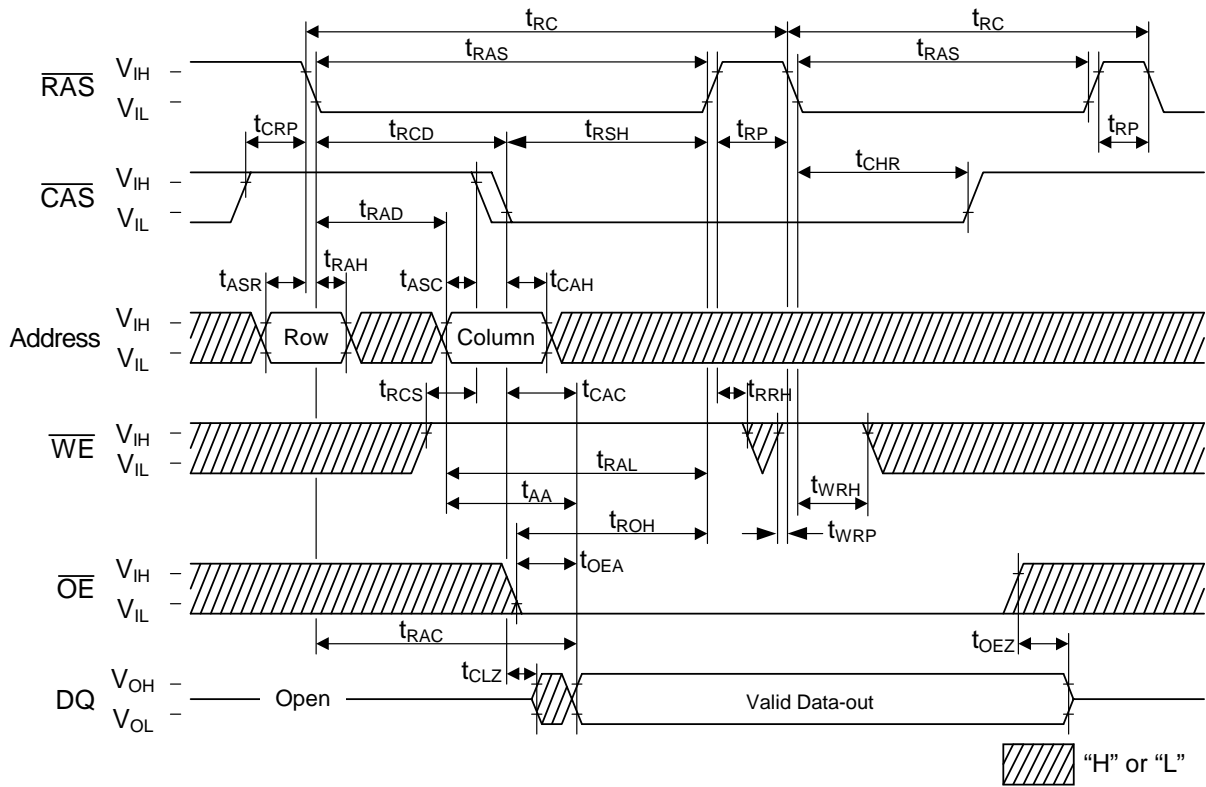
- $\overline{\text{RAS}}$ -Only Refresh Cycle



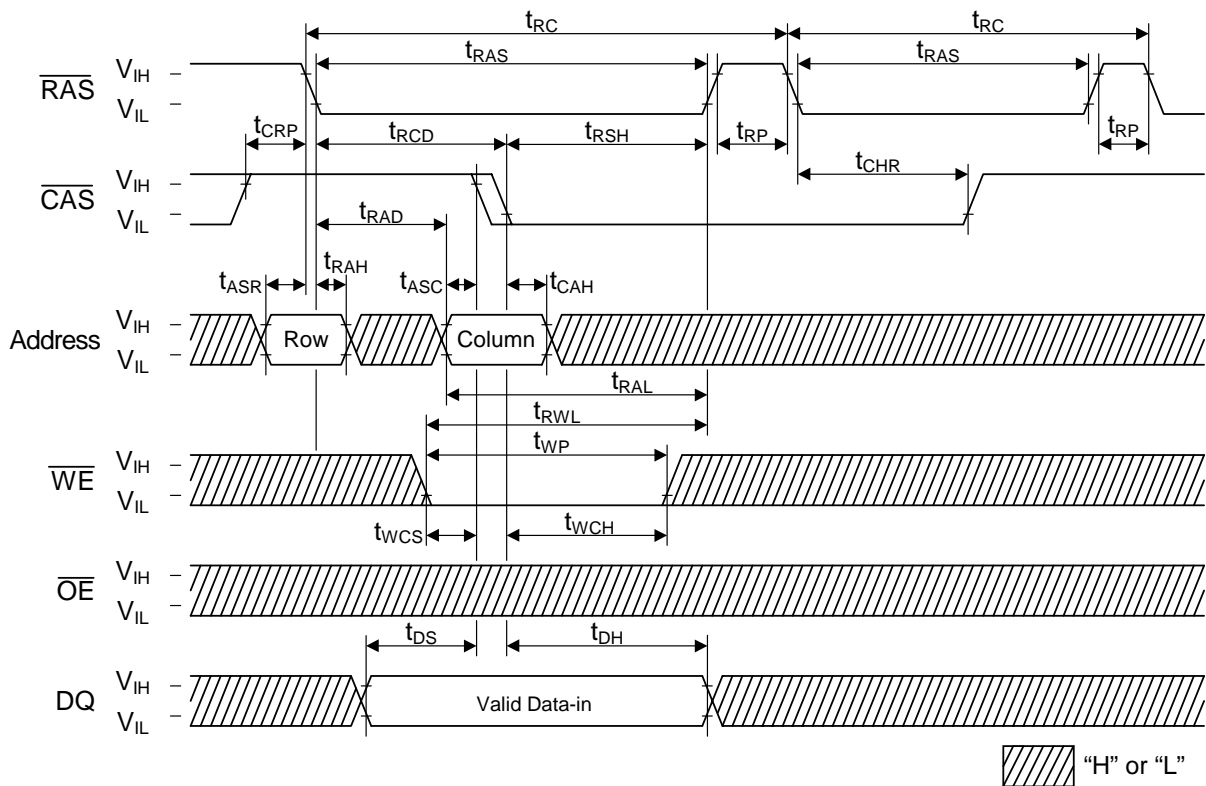
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle



- Hidden Refresh Read Cycle



- Hidden Refresh Write Cycle



NOTICE

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit and assembly designs.
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