

MSM51V17405F**4,194,304-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO****DESCRIPTION**

The MSM51V17405F is a 4,194,304-word × 4-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM51V17405F achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM51V17405F is available in a 26/24-pin plastic SOJ or 26/24-pin plastic TSOP.

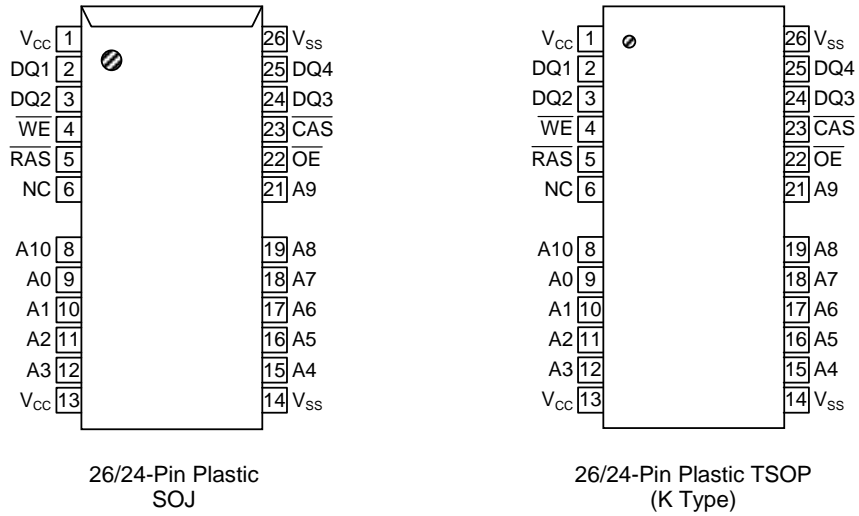
FEATURES

- 4,194,304-word × 4-bit configuration
 - Single 3.3V power supply, ±0.3V tolerance
 - Input : LVTTTL compatible, low input capacitance
 - Output : LVTTTL compatible, 3-state
 - Refresh : 2048 cycles/32ms
 - Fast page mode with EDO, read modify write capability
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
 - Packages
 - 26/24-pin 300mil plastic SOJ (SOJ26/24-P-300-1.27) (Product : MSM51V17405F-xxSJ)
 - 26/24-pin 300mil plastic TSOP (TSOPII26/24-P-300-0.80-K) (Product : MSM51V17405F-xxTS-K)
- xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM51V17405F	50ns	25ns	13ns	13ns	84ns	360mW	1.8mW
	60ns	30ns	15ns	15ns	104ns	324mW	
	70ns	35ns	20ns	20ns	124ns	288mW	

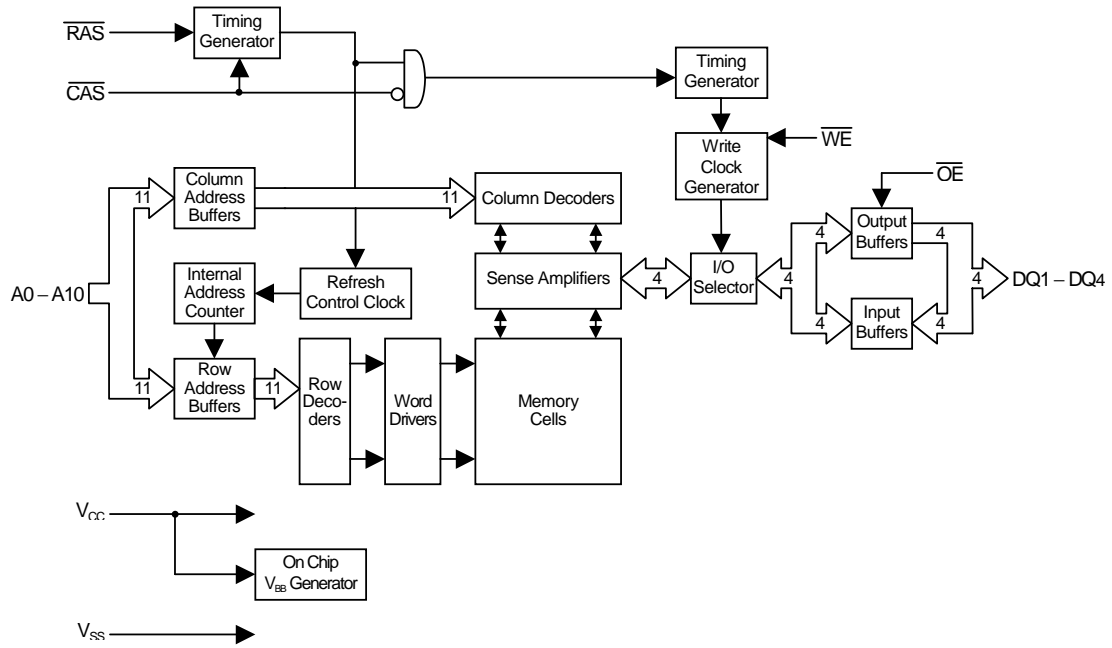
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0–A10	Address Input
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
DQ1–DQ4	Data Input/Data Output
\overline{OE}	Output Enable
\overline{WE}	Write Enable
V_{CC}	Power Supply (3.3V)
V_{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage V_{CC} Supply relative to V_{SS}	V_T	-0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_{D^*}	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: $T_a = 25^{\circ}\text{C}$ **RECOMMENDED OPERATING CONDITIONS** $(T_a = 0 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

Notes: *1. The input voltage is $V_{CC} + 1.0\text{V}$ when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is $V_{SS} - 1.0\text{V}$ when the pulse width is less than 20ns (the pulse width respect to the point at which V_{SS} is applied).

PIN CAPACITANCE $(V_{CC} = 3.3\text{V} \pm 0.3\text{V}, T_a = 25^{\circ}\text{C}, f = 1 \text{ MHz})$

Parameter	Symbol	Min.	Typ.	Min.	Unit
Input Capacitance (A0 – A10)	C_{IN1}	—	—	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{IN2}	—	—	7	pF
Output Capacitance (DQ1 – DQ4)	$C_{I/O}$	—	—	7	pF

DC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM51V17405 F-50		MSM51V17405 F-60		MSM51V17405 F-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V _{OH}	I _{OH} = -2.0mA	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	
Output Low Voltage	V _{OL}	I _{OL} = 2.0mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0V ≤ V _I ≤ V _{CC} +0.3V; All other pins not under test = 0V	- 10	10	- 10	10	- 10	10	μA	
Output Leakage Current	I _{LO}	DQ disable 0V ≤ V _O ≤ V _{CC}	- 10	10	- 10	10	- 10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t _{RC} = Min.	—	100	—	90	—	80	mA	1,2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2V$	—	0.5	—	0.5	—	0.5		
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, t _{RC} = Min.	—	100	—	90	—	80	mA	1,2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	$\overline{\text{RAS}} = \text{cycling}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	100	—	90	—	80	mA	1,2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling, t _{HPC} = Min.	—	100	—	90	—	80	mA	1,3

- Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
3. The address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

AC CHARACTERISTICS (1/3)

(V_{CC} = 3.3V ± 0.3V, T_a = 0 to 70°C) Note1,2,3,12,13

Parameter	Symbol	MSM51V17405 F-50		MSM51V17405 F-60		MSM51V17405 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	84	—	104	—	124	—	ns	
Read Modify Write Cycle Time	t _{RWC}	110	—	135	—	160	—	ns	
Fast Page Mode Cycle Time	t _{HPC}	20	—	25	—	30	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{HPRWC}	58	—	68	—	78	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	13	—	15	—	20	ns	4,5
Access Time from Column Address	t _{AA}	—	25	—	30	—	35	ns	4,6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	30	—	35	—	40	ns	4
Access Time from $\overline{\text{OE}}$	t _{OEa}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
Data Output Hold After $\overline{\text{CAS}}$ Low	t _{DOH}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{CEZ}	0	13	0	15	0	20	ns	7,8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t _{REZ}	0	13	0	15	0	20	ns	7,8
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	13	0	15	0	20	ns	7
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t _{WEZ}	0	13	0	15	0	20	ns	7
Transition Time	t _T	1	50	1	50	1	50	ns	3
Refresh Period	t _{REF}	—	32	—	32	—	32	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode with EDO)	t _{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	7	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	7	—	10	—	13	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode with EDO)	t _{CP}	7	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	7	10,000	10	10,000	13	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	35	—	40	—	45	—	ns	

AC CHARACTERISTICS (2/3)

(V_{CC} = 3.3V ± 0.3V, T_a = 0 to 70°C) Note1,2,3,12,13

Parameter	Symbol	MSM51V17405 F-50		MSM51V17405 F-60		MSM51V17405 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
CAS to RAS Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	30	—	35	—	40	—	ns	
OE Hold Time from CAS (DQ Disable)	t _{CHO}	5	—	5	—	5	—	ns	
RAS to CAS Delay Time	t _{RCD}	11	37	14	45	14	50	ns	5
RAS to Column Address Delay Time	t _{RAD}	9	25	12	30	12	35	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	7	—	10	—	13	—	ns	
Column Address to RAS Lead Time	t _{RAL}	25	—	30	—	35	—	ns	
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	9
Read Command Hold Time referenced to RAS	t _{RRH}	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	7	—	10	—	13	—	ns	
Write Command Pulse Width	t _{WP}	7	—	10	—	10	—	ns	
WE Pulse Width (DQ Disable)	t _{WPE}	7	—	10	—	10	—	ns	
OE Command Hold Time	t _{OEH}	7	—	10	—	13	—	ns	
OE Precharge Time	t _{OEP}	7	—	10	—	10	—	ns	
OE Command Hold Time	t _{OCH}	7	—	10	—	10	—	ns	
Write Command to RAS Lead Time	t _{RWL}	7	—	10	—	13	—	ns	
Write Command to CAS Lead Time	t _{CWL}	7	—	10	—	13	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t _{DH}	7	—	10	—	13	—	ns	11
OE to Data-in Delay Time	t _{OED}	13	—	15	—	20	—	ns	
CAS to WE Delay Time	t _{CWD}	30	—	34	—	44	—	ns	10
Column Address to WE Delay Time	t _{AWD}	42	—	49	—	59	—	ns	10
RAS to WE Delay Time	t _{RWD}	67	—	79	—	94	—	ns	10
CAS Precharge WE Delay Time	t _{CPWD}	47	—	54	—	64	—	ns	10

AC CHARACTERISTICS (3/3)

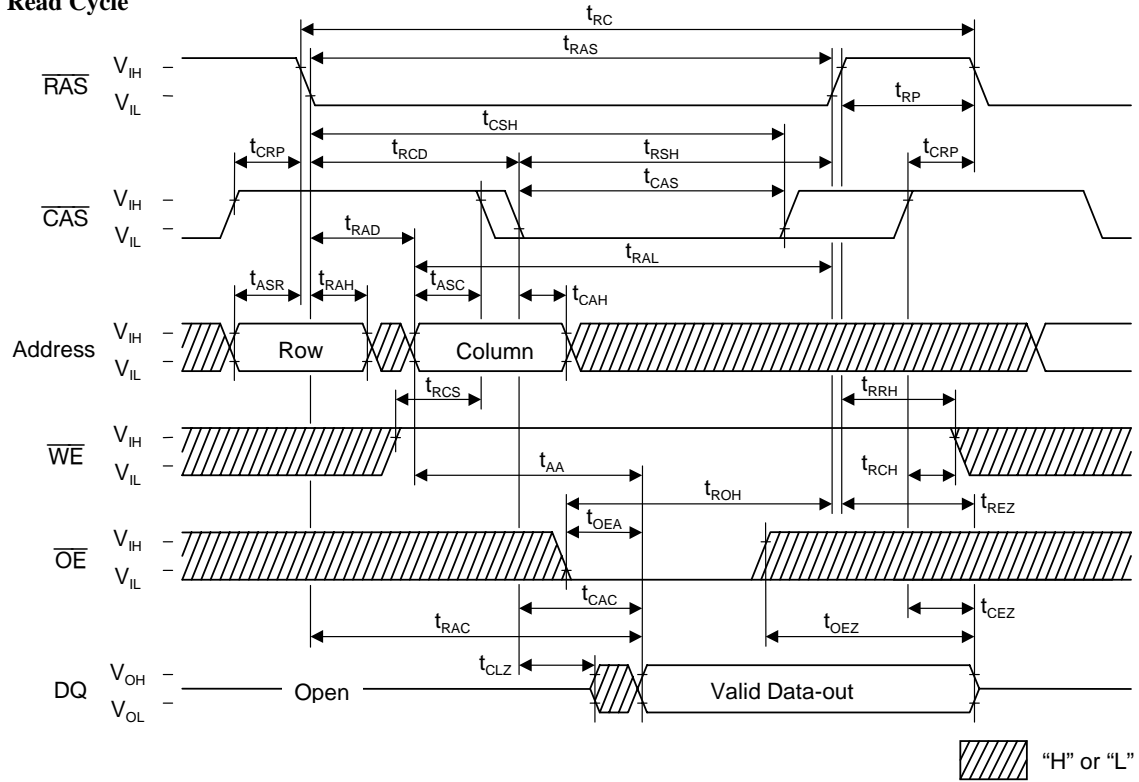
 $(V_{CC} = 3.3V \pm 0.3V, T_a = 0 \text{ to } 70^\circ\text{C})$ Note1,2,3,12,13

Parameter	Symbol	MSM51V17405 F-50		MSM51V17405 F-60		MSM51V17405 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t_{WRP}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)	t_{WTH}	10	—	10	—	10	—	ns	

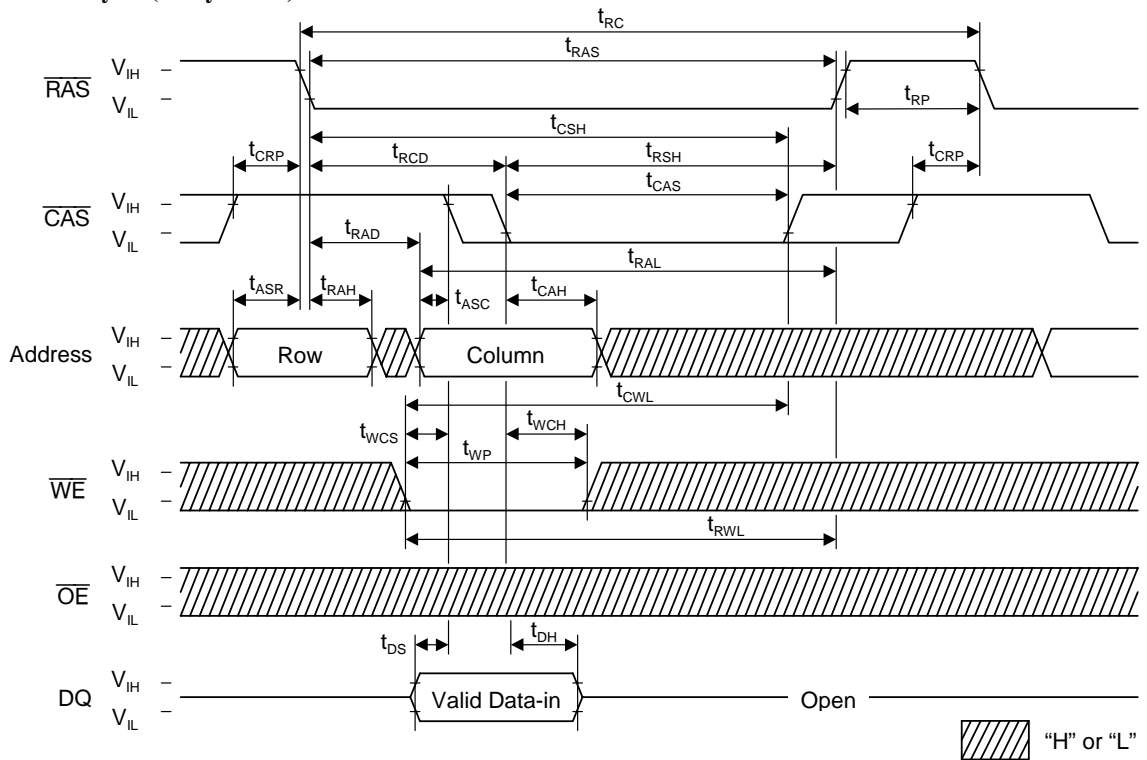
- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 2\text{ns}$.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. -50 is measured with a load circuit equivalent to 1 TTL load and 50pF, and -60/-70 is measured with a load circuit equivalent to 1 TTL load and 100pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.), and t_{OEZ} (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} , and t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to the $\overline{\text{CAS}}$, leading edges in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.
 12. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test CA9 and CA10 are not used and each DQ pin now access 4-bit locations. Since all 4 DQ pins are used, a total 16 data bits can be written in parallel into the memory array. In a read cycle, if 4 data bits are equal, the DQ pin will indicate a high level. If the 4 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 13. In a test mode read cycle, the value of access time parameter is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

TIMING CHART

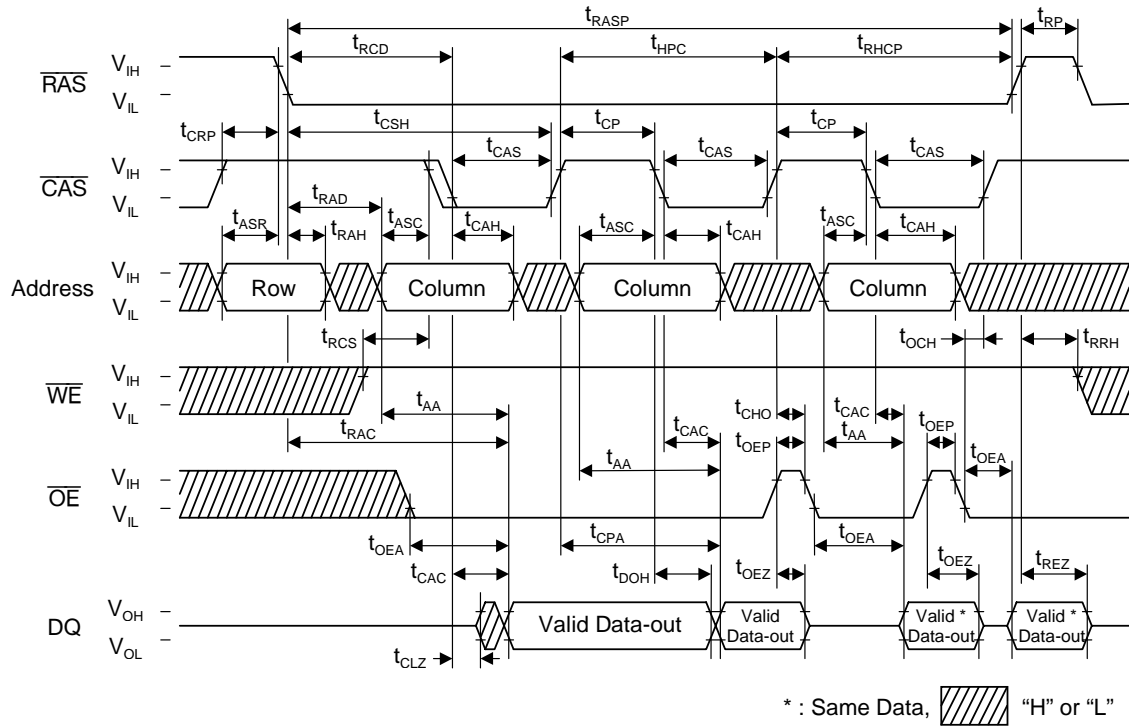
Read Cycle



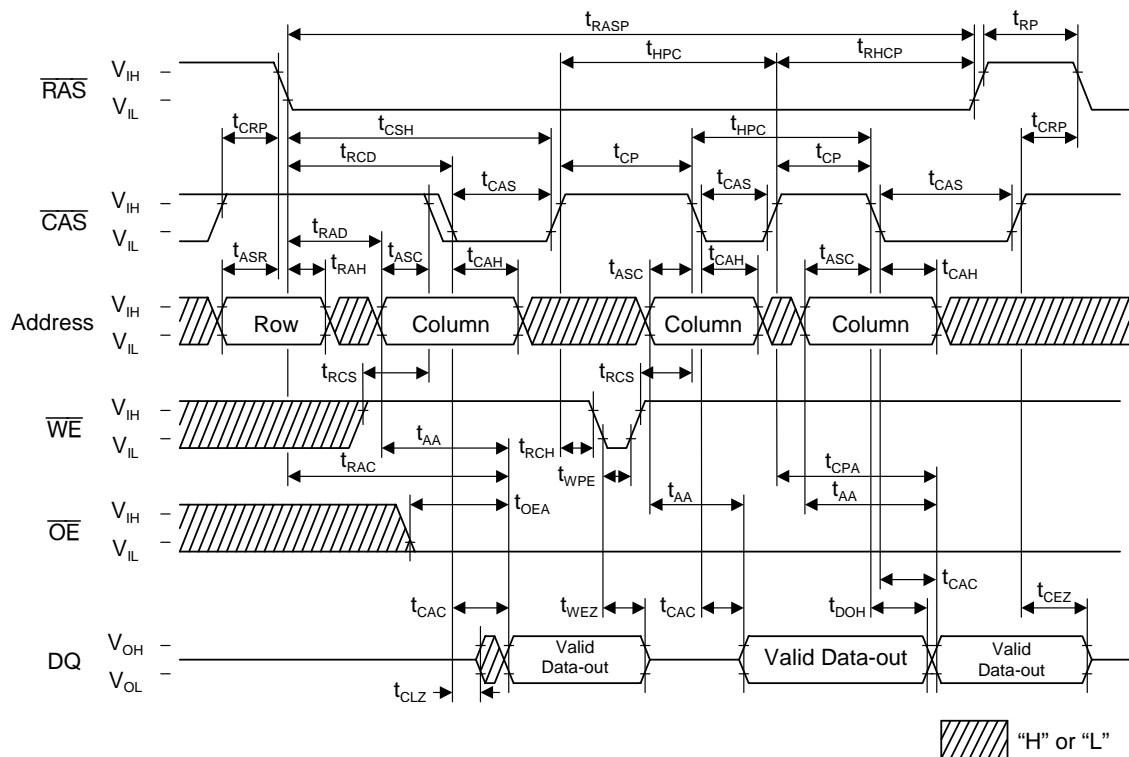
Write Cycle (Early Write)



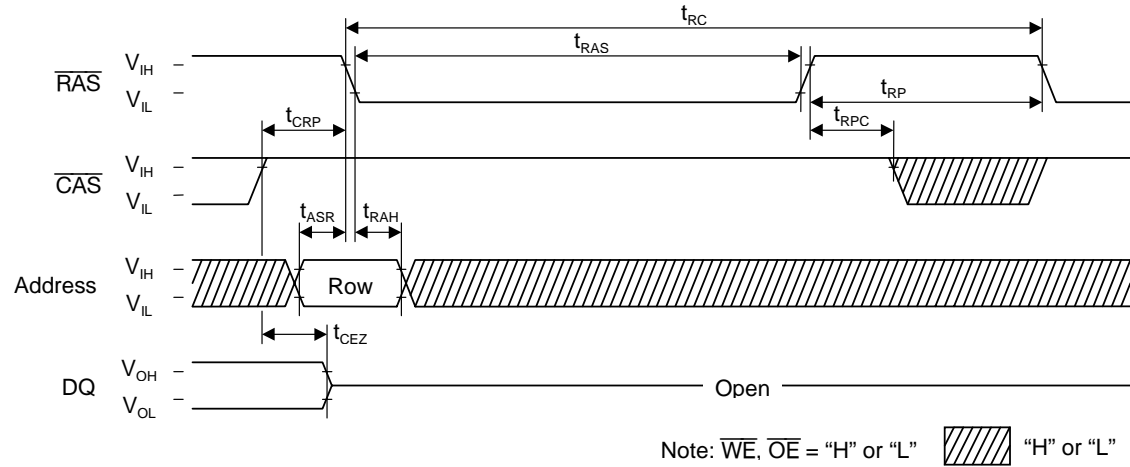
Fast Page Mode Read Cycle (Part-1)



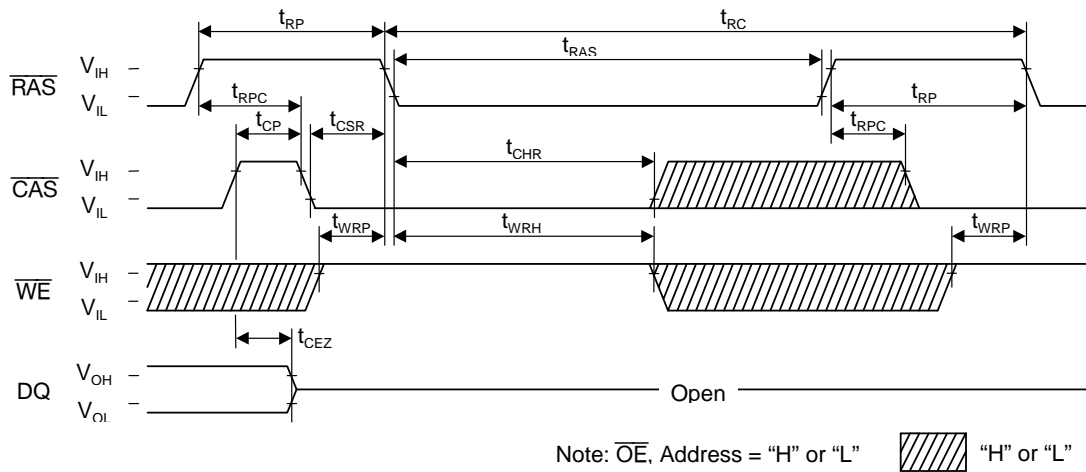
Fast Page Mode Read Cycle (Part-2)



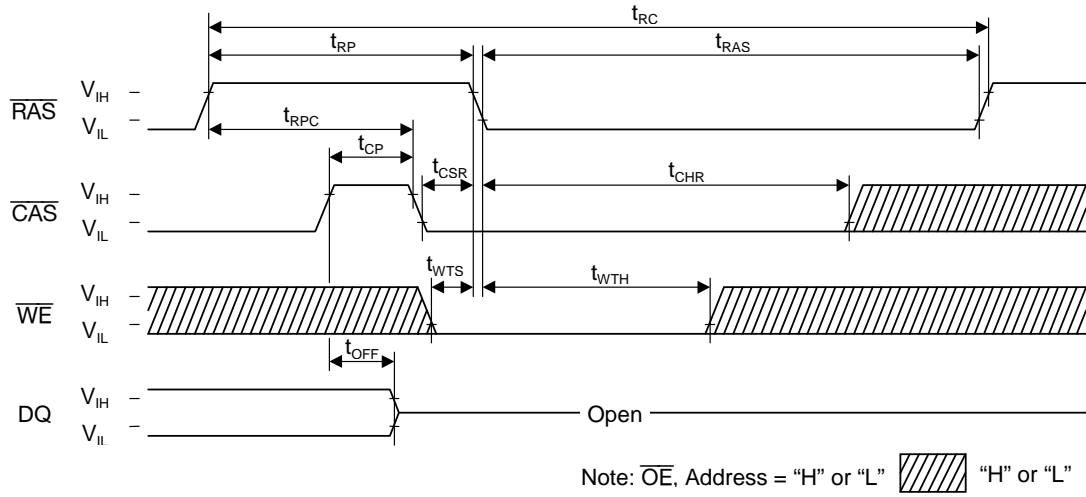
RAS-only Refresh Cycle



CAS before RAS Refresh Cycle



Test Mode-in Cycle



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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
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