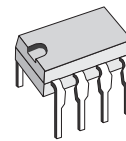


**SWITCH MODE POWER SUPPLY SECONDARY CIRCUIT**

- INTERNAL PWM SIGNAL GENERATOR
- POWER SUPPLY WIDE RANGE 4.5V – 14.5V
- SOFT START
- REFERENCE VOLTAGE  $2V \pm 5\%$
- WIDE FREQUENCY RANGE 250kHz
- MINIMUM OUTPUT PULSE WIDTH 500nS
- MAXIMUM PRESET DUTY CYCLE
- SYNCHRONIZATION WINDOW
- OUTPUT SWITCH
- UNDERVOLTAGE LOCKOUT
- FREQUENCY RANGE WITH SYNCHRONIZATION 64kHz



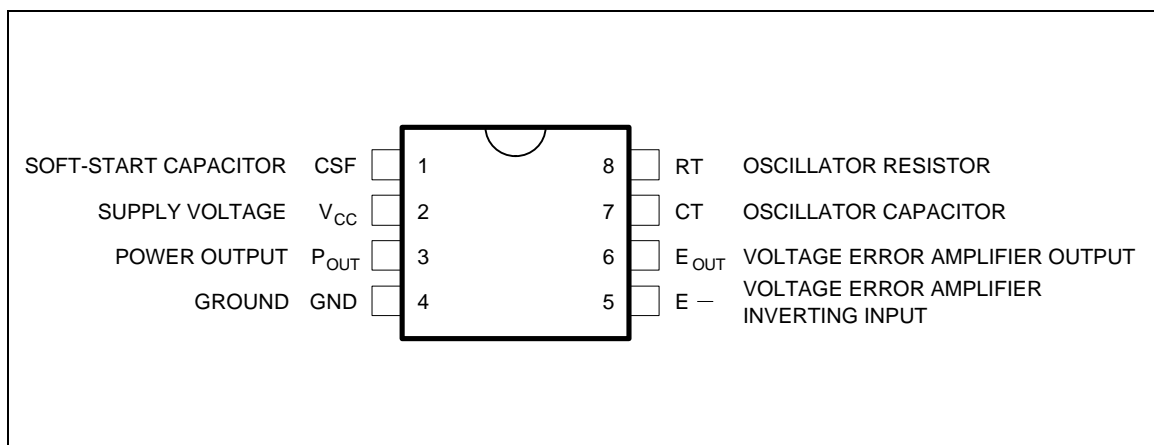
**DIP8**  
(Plastic Package)

**ORDER CODE : TEA5170**

**DESCRIPTION**

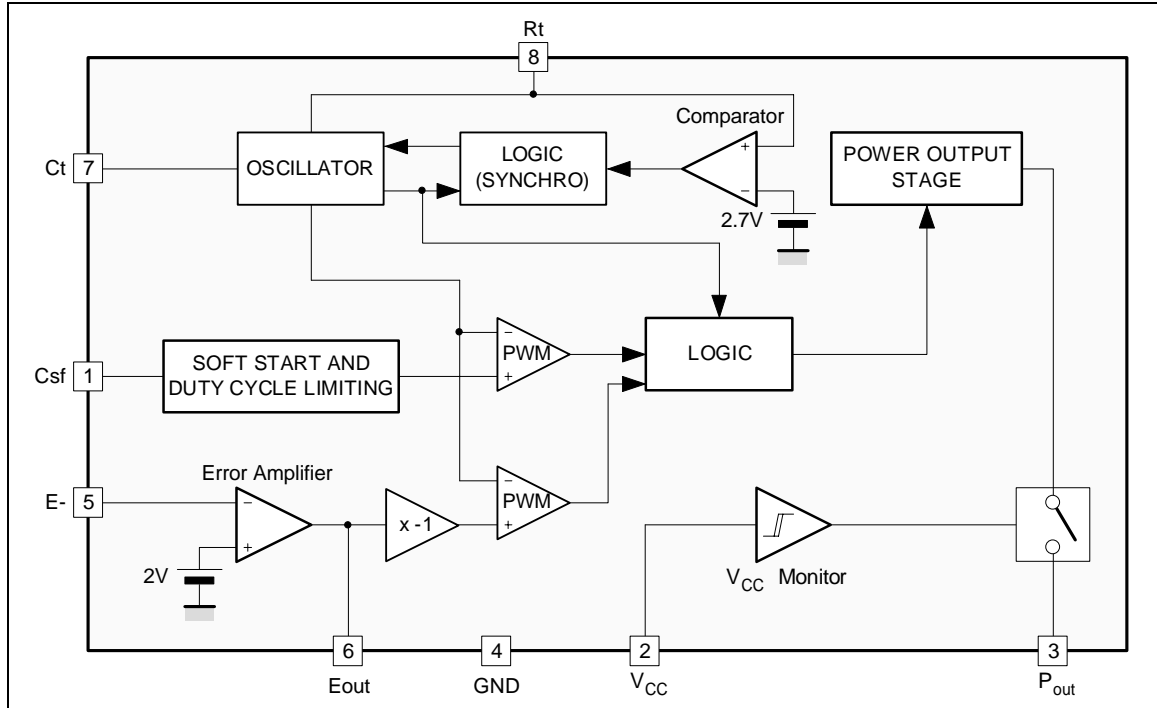
The TEA5170 is designed to work in the secondary part of an off-line SMPS, sending pulses to the slaved TEA2260/61 which are located on the primary side of the main transformer. An accurate regulated voltage is obtained by duty cycle control. The TEA5170 can be externally synchronized by higher or lower frequency signal, then it could be used in applications like TV set ones. For more details, refer to application note AN408/0591.

**PIN CONNECTIONS**



5170-01.EPS

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	15	V
$T_j$	Operating Junction Temperature	150	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	- 40, + 150	$^{\circ}\text{C}$

## THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	90	$^{\circ}\text{C}/\text{W}$

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Power Supply Voltage	5		14	V
RT	Timing Resistor	47		180	$\text{k}\Omega$
CT	Timing Capacitor	0.12		1.8	nF
Fosc	Oscillator Frequency	12		250	kHz
Fsy	Synchro Frequency	12		64	kHz
$T_{amb}$	Operating Ambient Temperature	- 20		70	$^{\circ}\text{C}$
VRT	Voltage on Pin RT (8)			7	Volt
VCT	Current on Pin CT (1)			100	$\mu\text{A}$
ISOURCE	Output Current		30	60	mA

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{V}$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

## OSCILLATOR

TA	Free Period	$R_T = 100\text{k}\Omega \pm 0\%$ $C_T = 1.2\text{nF} \pm 0\%$ , $V_{CC} = 12\text{V}$	60.40	65.60	70.80	$\mu\text{S}$
TB		$R_T = 100\text{k}\Omega \pm 0\%$ $C_T = 560\text{pF} \pm 0\%$ , $V_{CC} = 12\text{V}$	29.18	31.70	34.22	$\mu\text{S}$
$\Delta F_{OSC}(T)$	Frequency drift due to ambient temperature variation from $0^\circ\text{C}$ to $70^\circ\text{C}$ $\frac{F_{OSC}(70^\circ\text{C}) - F_{OSC}(0^\circ\text{C})}{70^\circ\text{C} \times F_{OSC}(25^\circ\text{C})}$	$R_T = 100\text{k}\Omega \pm 0\%$ $C_T = 1.2\text{nF} \pm 0\%$ , $V_{CC} = 12\text{V}$		0.01		$\%/^\circ\text{C}$
$\Delta F_{OSC}(V_{CC})$	Frequency drift due to $V_{CC}$ variation from 5V to 12V $\frac{F_{OSC}(12\text{V}) - F_{OSC}(5\text{V})}{7\text{V} \times F_{OSC}(12\text{V})}$	$R_T = 100\text{k}\Omega \pm 0\%$ $C_T = 1.2\text{nF} \pm 0\%$		0.07		$\%/V$

ERROR VOLTAGE AMPLIFIER ( $V_{CC} = 12\text{V}$ )

I <sub>bias</sub>	Input Bias Current	$E_{in} = 2\text{V}$	0	0.2	1	$\mu\text{A}$
G <sub>vol</sub>	Voltage Gain			80		dB
GB	Gain Bandwidth			2		MHz
	Slew Rate			2		$\text{V}/\mu\text{s}$

## INTERNAL VOLTAGE REFERENCE

V <sub>REF</sub>	Voltage Reference	Using the voltage error amplifier as a follower	1.9	2	2.1	V
$\Delta V_{REF}(V_{CC})$	Line Regulation $\frac{V_{REF}(12\text{V}) - V_{REF}(5\text{V})}{7\text{V}}$	$V_{CC} = 5\text{V}$ to $12\text{V}$	-3	0.4	3	mV/V
$\Delta V_{REF}(T)$	$V_{REF}$ drift with temperature $\frac{V_{REF}(70^\circ\text{C}) - V_{REF}(0^\circ\text{C})}{70^\circ\text{C}}$	$T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$		0.2		mV/ $^\circ$

## TON MIN

T <sub>ONMIN A</sub>	Minimum Duty Cycle	$C_t = 1.2\text{nF} \pm 0\%$ $R_t = 100\text{k}\Omega \pm 0\%$	1.77	2.53	3.29	$\mu\text{s}$
T <sub>ONMIN B</sub>	Minimum Duty Cycle	$C_t = 560\text{pF} \pm 0\%$ $R_t = 100\text{k}\Omega \pm 0\%$	1.04	1.49	1.94	$\mu\text{s}$

## POWER OUTPUT STAGE

V <sub>POUTH</sub>	Output High Level	$I_{load} = 1\text{mA}$	6.3	6.9	7.5	V
V <sub>POUTL</sub>	Output Low Level	$I_{load} = -1\text{mA}$	0.5	0.8	1.1	V
I <sub>SINK</sub>	Sink Current	$V_{POUT} = 3\text{V}$	30	60	190	mA
I <sub>SOURCE</sub>	Source Current	$V_{POUT} = 3\text{V}$	30	110	190	mA

## SYNCHRONISATION

F <sub>trig Max</sub>	Maximum Synchro Frequency		64			kHz
V <sub>trig</sub>	Synchro Triggering Threshold			2.7	3	V
T <sub>trigp</sub>	Synchro Triggering Pulse Width	at $V_{RT} = 2.7\text{V}$ (fig 5)	800			nS
W <sub>trig +</sub>	Positive Triggering Window $\frac{T_{trig+} - T_O}{T_O}$	$C_T = 1.2\text{nF} \pm 0\%$ $R_T = 100\text{k}\Omega \pm 0\%$	25	35	40	%
W <sub>trig -</sub>	Negative Triggering Window $\frac{T_O - T_{trig-}}{T_O}$	$C_T = 1.2\text{nF} \pm 0\%$ $R_T = 100\text{k}\Omega \pm 0\%$	9	29	42	%

## SOFT START

I <sub>csf</sub>	*Csf Load Current	$V_{csf} = 1\text{V}$	2.5	3.7	6	$\mu\text{A}$
Donmax	Maximum Duty Cycle	$V_{CS} > 2.5\text{V}$ , $V_{CC} = 12\text{V}$ $C_T = 1.2\text{nF} \pm 0\%$ $R_T = 100\text{k}\Omega \pm 0\%$	60	78	95	%

\*Csf is a high impedance capacitor

5170-04, TEL

## TEA5170

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 12\text{V}$ , unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>V<sub>CC</sub> MONITOR</b>						
V <sub>START</sub>	Turn-on Threshold		3.60	4	4.40	V
V <sub>HYST</sub>	Hysteresis Voltage		100			mV
V <sub>STOP</sub>	Turn-off Threshold		3.50			V
<b>TOTAL DEVICE</b>						
I <sub>CC</sub>	Supply Current	RT = 100kΩ ± 0%, CT = 1.2nf ± 0% No Load on Pin 3, V <sub>CC</sub> = 12V	7	12	25	mA

### GENERAL DESCRIPTION

The TEA5170 takes place in the secondary part of an isolated off-line SMPS. During normal mode operation, it sends pulses to the slave circuit located in the primary side (TEA2164, TEA2260/61) through a pulse transformer to achieve a very precisely regulated voltage by duty cycle control.

The main blocs of the circuit are :

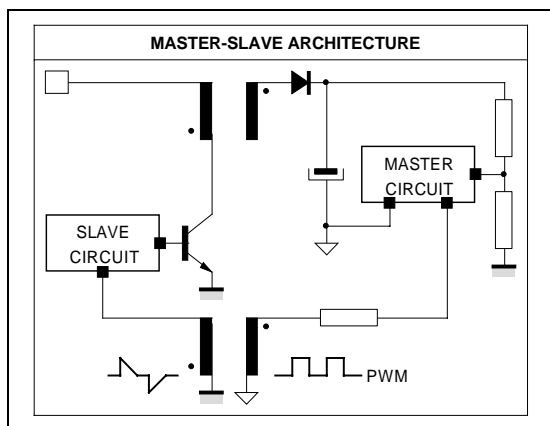
- an error voltage amplifier
- an RC oscillator
- an output stage
- a V<sub>CC</sub> monitor
- a voltage reference bloc
- a pulse width modulator
- two logic blocs
- a soft start and Duty cycle limiting bloc

### PRINCIPLE OF OPERATION

The TEA5170 sends pulses continuously to the slave circuit in order to insure a proper behaviour of the primary side.

- According to this, the output duty cycle is varying between D<sub>ON (min.)</sub> (0.05) and D<sub>ON (max.)</sub> (0.75) : then even in case of open load, pulses are still sent to the slave circuit.

Figure 1 : Basic Concept

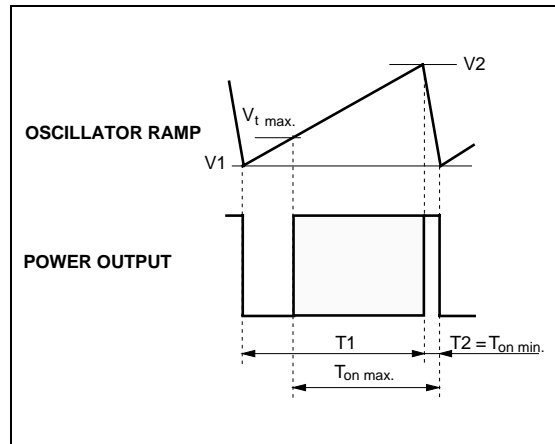


### ASYNCHRONIZED MODE (Figure 2)

The regulated voltage image is compared to 2V voltage reference. The error voltage amplifier output and the RC oscillator voltage ramp are applied to the internal Pulse Width Modulator Inputs.

The PWM logic Output is connected to a logic bloc which behaves like a RS latch, sets by the PWM output and resets when Ct downloading occurs. Finally, the push-pull output bloc delivers square wave signal whom output leading edge occurs during Ct uploading time, and output trailing edge at Ct downloading time end. The duty cycle is limited to 75% of oscillator period as maximum value and to Ct downloading time/oscillator period as minimum value (Figure 2).

Figure 2



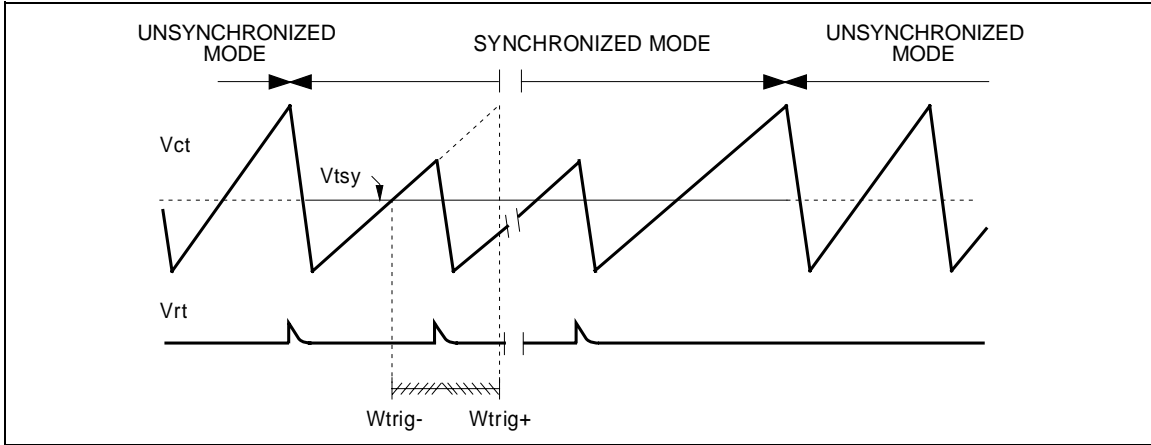
### SYNCHRONIZED MODE (see Figure 3)

The TEA5170 will enter the Synchronized Mode when it receives one pulse through Rt during Ct discharge.

At that time Ct charging current will be multiplied by 0.75 and period will increase up to T<sub>o</sub> x 1.26.

A pulse occurring during the synchro window, commands the Ct downloading. If none, the TEA5170 will return to normal mode at the end of the period.

Figure 3



**Remark :** In case of an application between TEA5170 and TEA2164, to optimize the synchronization windows of these circuits, the following relations have to be used :  $T_m = \frac{T_{SYNC}}{1.06} T_e = \frac{T_m}{1.223}$  with T<sub>e</sub> : Free period of the TEA2164 oscillator, and T<sub>m</sub> : Free period of the TEA5170 oscillator.

**BLOCK DESCRIPTION**

The error voltage amplifier inverting-input and output are accessible to use different feed-back network and allowing parasitic filtering network. The non-inverting input is internally connected to 2V reference voltage.

The RC oscillator is designed to work at high frequency (up to 250kHz). R<sub>T</sub> sets the capacitor charging current I<sub>o</sub> = 2/R<sub>T</sub>.

The capacitor C<sub>T</sub> is loaded from V<sub>1</sub> ≈ 1V to V<sub>2</sub> = 2V during T<sub>1</sub> =  $\frac{C_T R_T}{1.985}$  and then down loaded through an integrated resistor R<sub>2</sub> ≈ 1kΩ during T<sub>2</sub> = 1300 C<sub>T</sub>. The ramp is used to limit the duty cycle. Then the maximum duty cycle is

$$DONMAX = \frac{1}{T_1 + T_2} (0.73 T_1 + T_2)$$

The output level is V<sub>CC</sub> independant when V<sub>CC</sub> is over 8V.

The V<sub>CC</sub> monitoring switches the circuit on when V<sub>CC</sub> is over 4V and switches it off when under 3.8V. This function insures a proper starting procedure (made by the primary side circuit).

**SYNCHRONIZATION**

(see Figures 4 and 5)

Figure 4 : Triggering Schematic

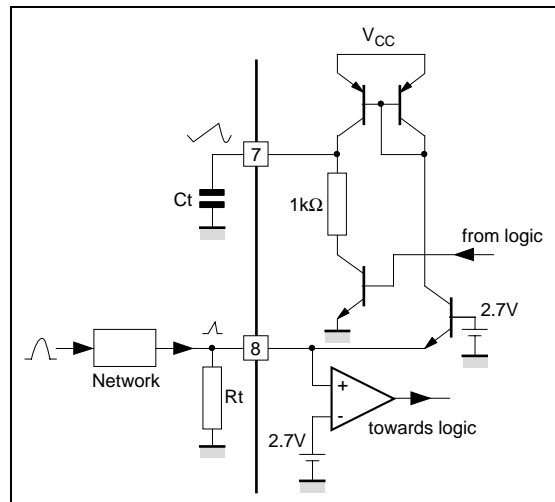
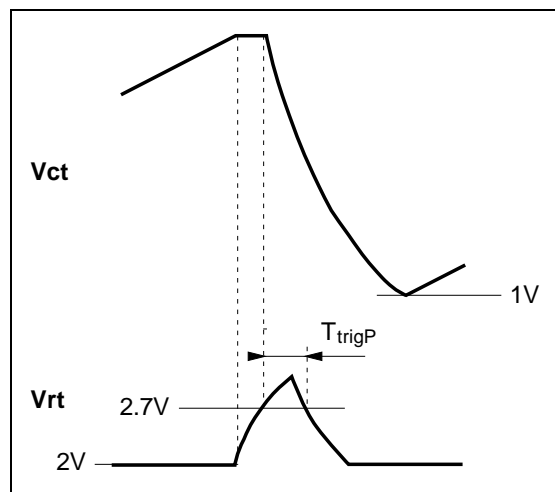


Figure 5 : Typical Waveforms



**STARTING**

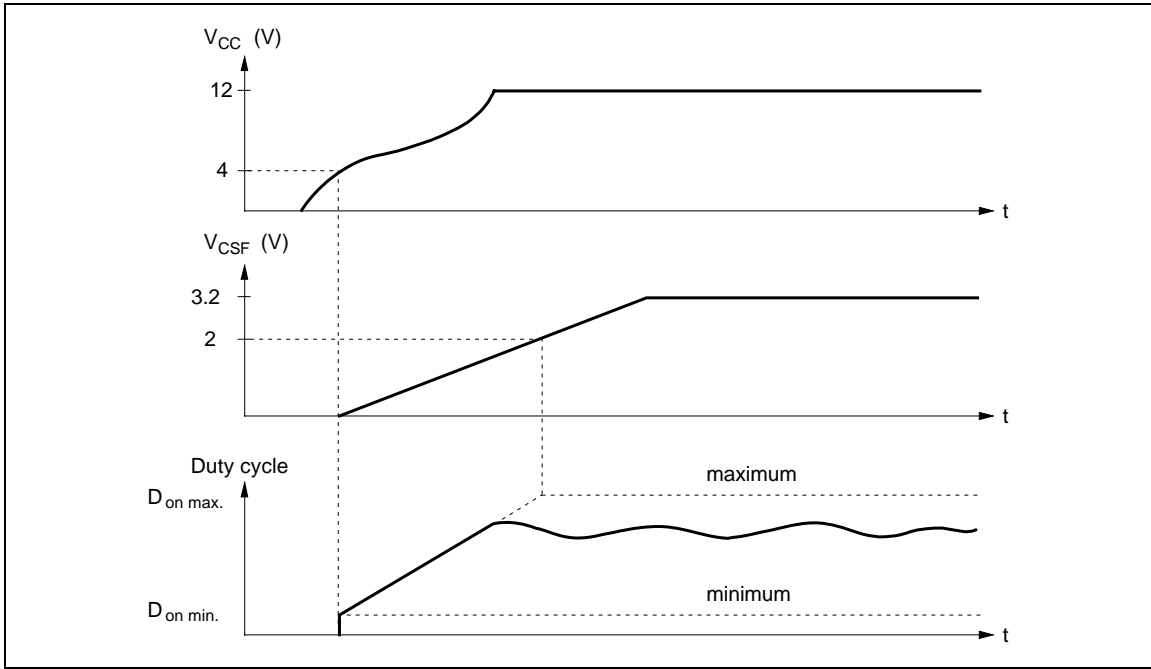
When  $V_{CC}$  is under 4V, output pulses are not allowed and the slave circuit keeps its own mode. When  $V_{CC}$  is going over 4V, output pulses are sent via the pulse transformer (or an optical device) to the slave circuit which is synchronizing and entering the slaved mode. Output pulses can be shut down only if  $V_{CC}$  goes below 3.8 Volt.

**SOFT START**

Using  $C_{sf}$ , it is possible to make a soft start sequence. When  $V_{CC}$  grows from 0V to 4V, voltage on  $C_{sf}$  equals 0V. When  $V_{CC}$  is higher than 4V,  $C_{sf}$  is loaded by a  $3.7\mu A$  current, then  $T_{onMAX}$  ( $V_{csf}$ ) will vary linearly from  $T_{onmin}$  to  $T_{onmax}$  according to  $C_{sfst}$  bias.

When  $V_{CC}$  will go low (3.8 Volt threshold),  $C_{sf}$  will be downloaded by an internal transistor.

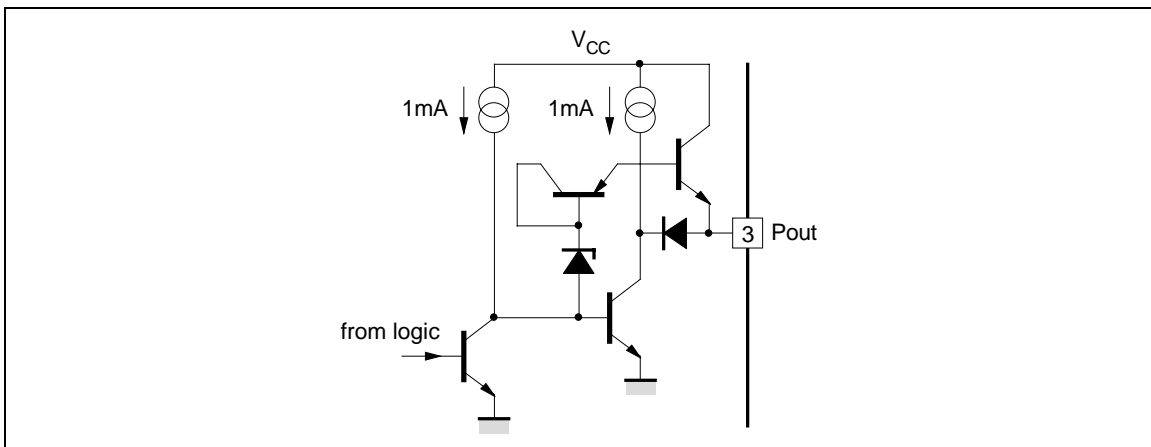
**Figure 6 :** Soft-Start Sequence



5170-08.EPS

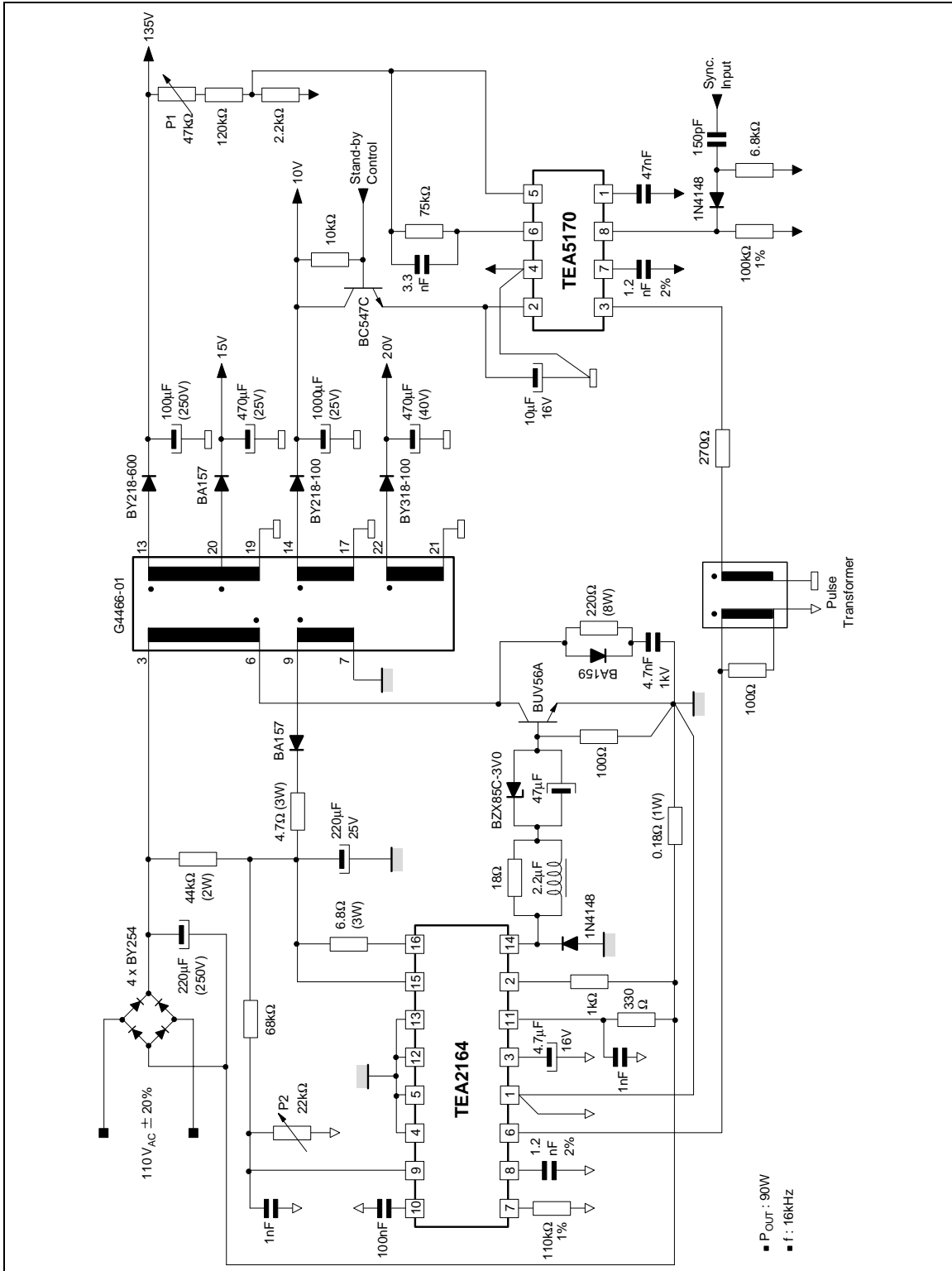
**POWER OUTPUT STAGE**

**Figure 7 :** Electrical Schematic



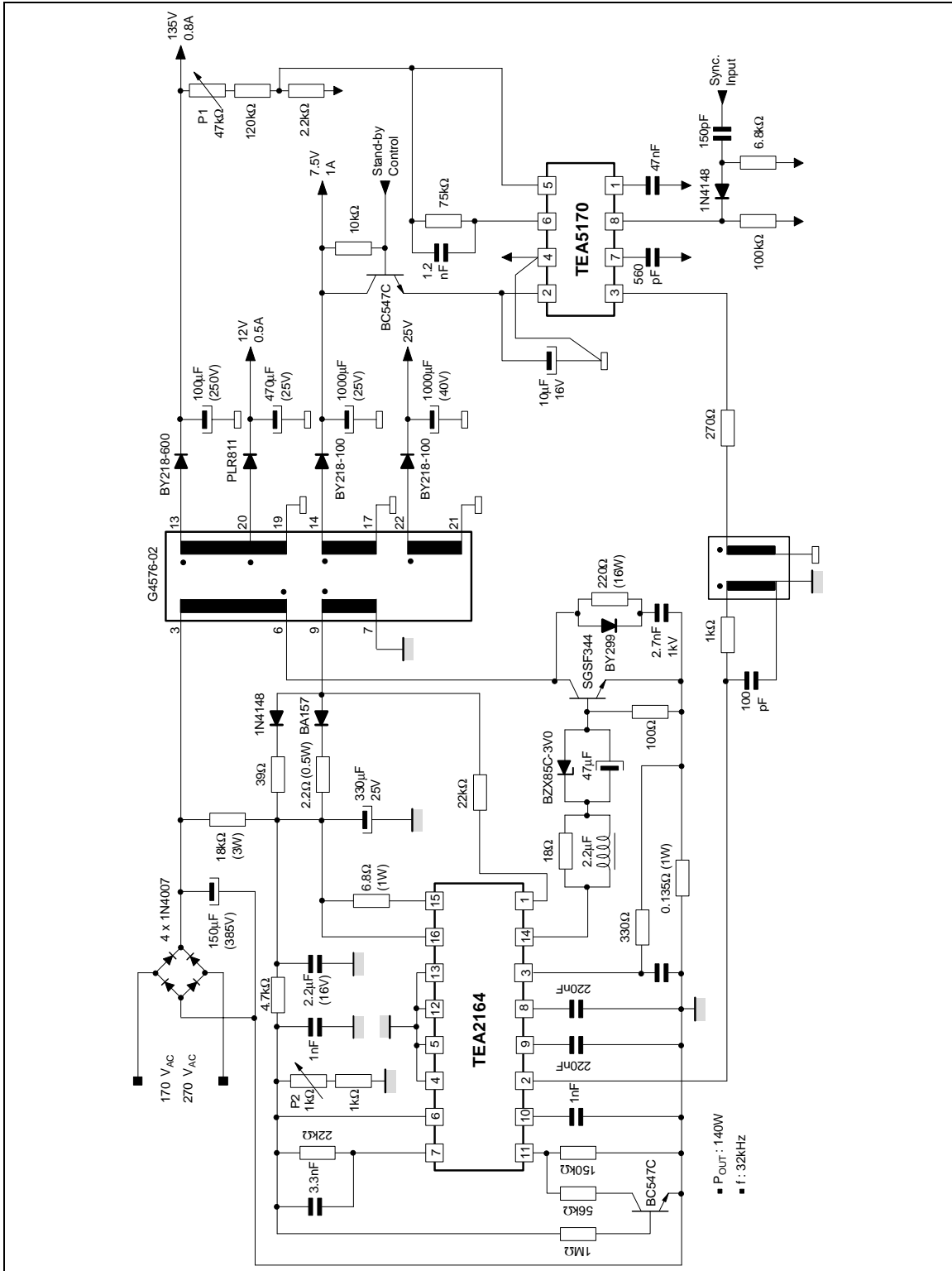
5170-08.EPS

Figure 8



5170-10/EP5

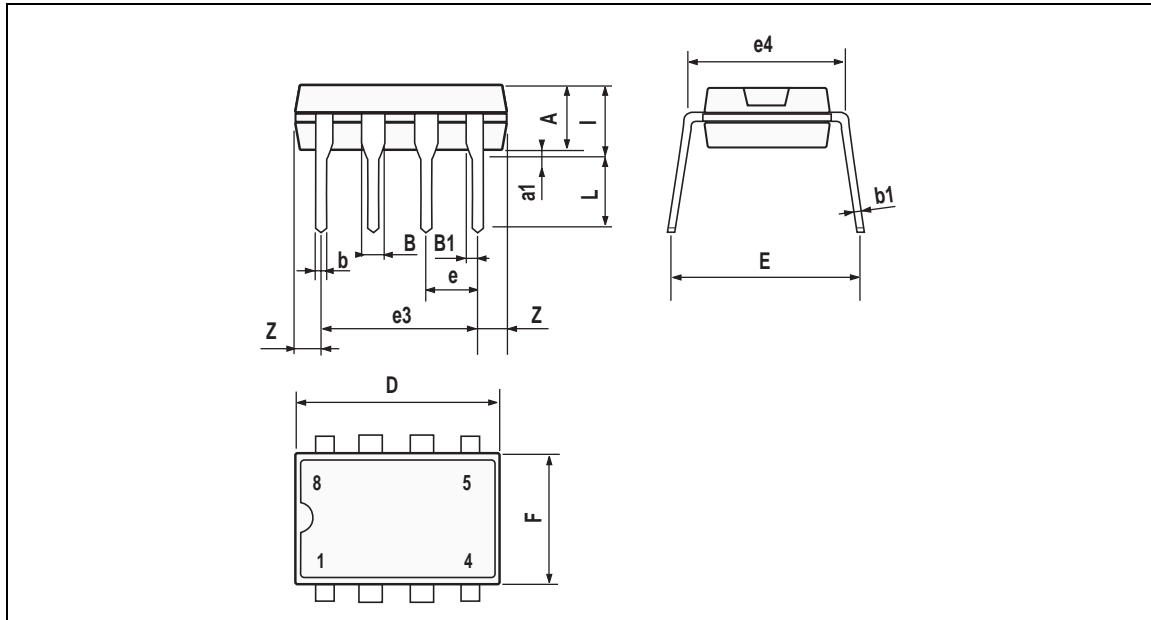
Figure 9



5170-11.EPS



**PACKAGE MECHANICAL DATA**  
8 PINS - PLASTIC DIP



PMDIP8LEPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8 TBL

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No licence is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1994 SGS-THOMSON Microelectronics - All Rights Reserved

Purchase of I<sup>2</sup>C Components of SGS-THOMSON Microelectronics, conveys a license under the Philips I<sup>2</sup>C Patent. Rights to use these components in a I<sup>2</sup>C system, is granted provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.

**SGS-THOMSON Microelectronics GROUP OF COMPANIES**

Australia - Brazil - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco  
The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.