OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM5259

40-DOT SEGMENT DRIVER

GENERAL DESCRIPTION

The MSM5259 is a dot matrix LCD segment driver which is fabricated using low power CMOS metal gate technology. This LSI consists of 40-bit shift register, 40-bit latch and 40-bit 4-level driver.
It converts serial data, which is received from an LCD controller LSI, to parallel data and outputs LCD driving waveforms to LCD.
Expansion of the display can be easily made according to the number and structure of characters. Since the 40-bit shift register of this device consists of two 20-bit shift registers, it is possible to allot bits efficiently according to the number of characters.
The MSM5259 can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source. For static operation only, the device is available with a power supply voltage of 2.5V or more.

FEATURES

- Supply voltage : 3.5 to 6.0V (Dynamic display)
  : 2.5 to 6.0V (Static display)
- LCD driving voltage : 2.5 to 6.0V (Static display)
- Applicable LCD duty : 1/8 to 1/16
- Interface with MSM6222-xx (Dot matrix LCD controller with 16-dot common driver and 40-dot segment driver)
- Bias voltage can be supplied externally.
- Package options:
  56-pin plastic QFP (QFP56-P-910-0.65-K) (Product name : MSM5259GS-K)
  56-pin plastic QFP (QFP56-P-910-0.65-L2) (Product name : MSM5259GS-L2)
  56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name : MSM5259GS-2K)
  56-pin plastic QFP (QFP56-P-910-0.65-2L2) (Product name : MSM5259GS-2L2)

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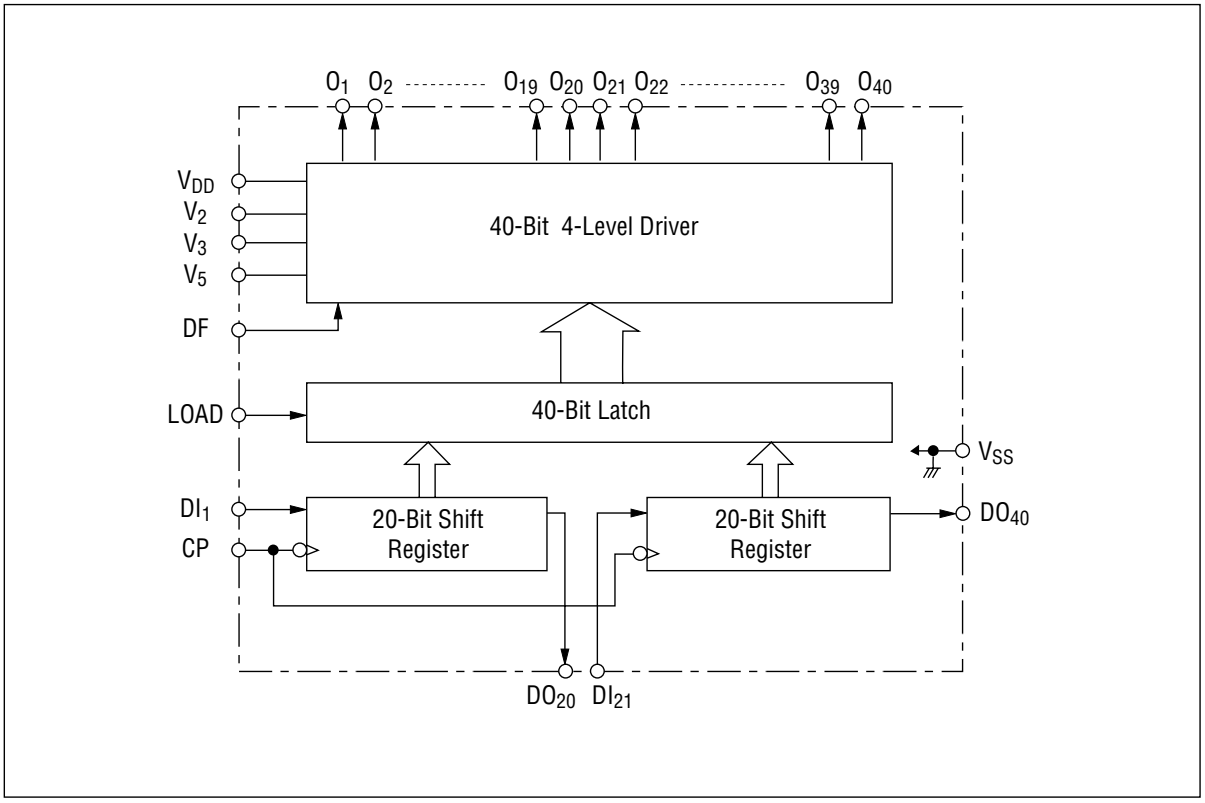
BLOCK DIAGRAM



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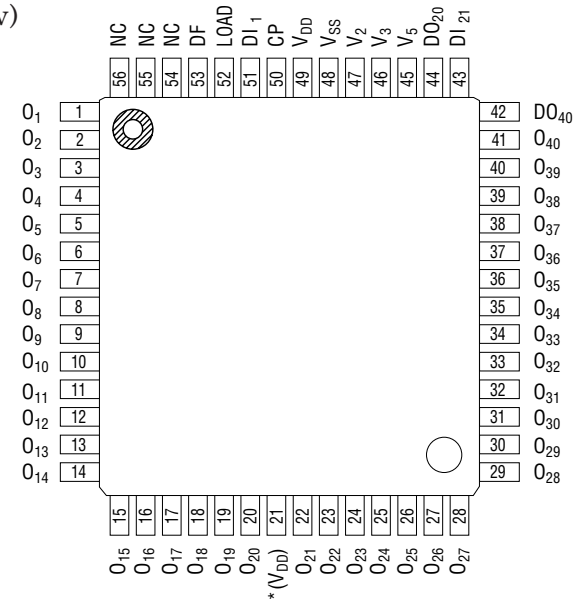
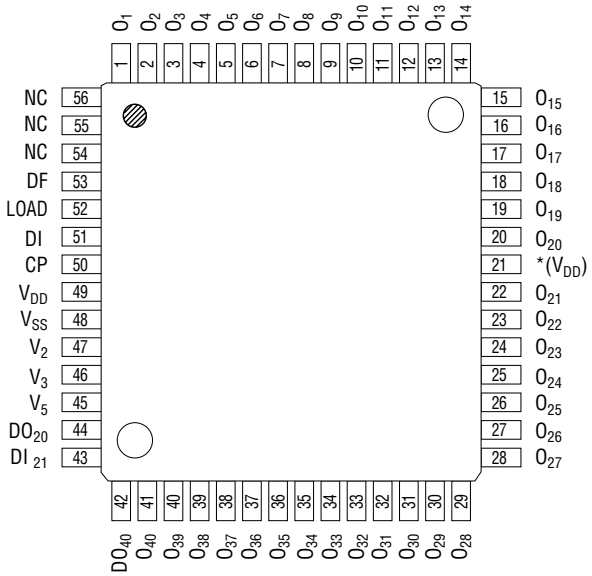
PIN CONFIGURATION

(Top View)



NC : No connection

56-Pin Plastic QFP (Type K)



NC : No connection

56-Pin Plastic QFP (Type L)

* Do not connect pin 21 to the other signal pins, because the pin is internally connected to V_{DD}. Do not use pin 21 as a single V_{DD} signal line. It is permissible to use pin 21 for supplying a higher power of V_{DD}.

Note : The figure for Type L shows the configuration viewed from the reverse side of the package. Pay attention to the difference in pin arrangement.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	Ta = 25°C	–0.3 to +6.5	V
Supply Voltage (2)	$V_{DD} - V_5$ *1		0 to +6.5	V
Input Voltage	V_I		–0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Rnage	Unit
Supply Voltage (1)	V_{DD}	Dynamic	3.5 to 6.0	V
		Static	2.5 to 6.0	
Supply Voltage (2)	$V_{DD} - V_5$ *1	—	2.5 to 6.0 *2	V
Operating Temperature	T_{op}	—	–30 to +85	°C

*1 $V_{DD} > V_2 > V_3 > V_5 > V_{SS}$ (Dynamic display)
$V_{DD} = V_3 > V_2 = V_5 = V_{SS}$ (Static display)
For V_{DD} of less than 3.5V, the device is available only for static operation.

*2 V_{DD} is the reference potential for the LCD driving voltage.
To determine the LCD driving voltage, change the value of V_5. (0V Minimum)

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ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{DD} = 5V±10%, Ta=–30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH} *1	—	0.8V_{DD}	—	V_{DD}	V
"L" Input Voltage	V_{IL} *1	—	0	—	0.2V_{DD}	V
"H" Input Current	I_{IH} *1	$V_{IH} = V_{DD}$	—	—	1	µA
"L" Input Current	I_{IL} *1	V_{IL} = 0V	—	—	–1	µA
"H" Output Voltage	V_{OH} *2	I_O = –40µA	4.2	—	—	V
"L" Output Voltage	V_{OL} *2	I_O = 0.4mA	—	—	0.4	V
ON Resistance	R_{ON} *3	V_{DD}–V_5= 5V $\lvert V_N – V_O \rvert$ = 0.25V *4	—	—	5	kΩ
Supply Current	I_{DD}	f_{CP} = 0Hz, No load	—	—	0.5	mA

*1 Applicable to DF, LOAD, DI_1 and DI_{21}.
*2 Applicable to DO_{20} and DO_{40}.
*3 Applicable to O_1 to O_{40}.

*4 Dynamic display : $V_N = V_{DD}$ to V_5, $V_2 = \frac{2}{3}(V_{DD} - V_5)$, $V_3 = \frac{1}{3}(V_{DD} - V_5)$

Static display : $V_N = V_{DD}$ to V_5, $V_3 = V_{DD}$, $V_2 = V_5 = V_{SS}$

DC Characteristics (2)

(Only for static operation) (V_{DD} = 3V±0.5V, Ta=–30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH} *1	—	0.8V_{DD}	—	V_{DD}	V
"L" Input Voltage	V_{IL} *1	—	0	—	0.2V_{DD}	V
"H" Input Current	I_{IH} *1	$V_{IH} = V_{DD}$	—	—	1	µA
"L" Input Current	I_{IL} *1	V_{IL} = 0V	—	—	–1	µA
"H" Output Voltage	V_{OH} *5	I_O = –40µA	2.2	—	—	V
"L" Output Voltage	V_{OL} *5	I_O = 0.2mA	—	—	0.4	V
ON Resistance	R_{ON} *6	$V_3 = V_{DD}$ = 3V, $V_2 = V_5 = V_{SS}$ = 0V, $\lvert V_N – V_O \rvert$ = 0.25V	—	—	10	kΩ
Supply Current	I_{DD}	f_{CP} = 0Hz, No load	—	—	0.5	mA

*5 Applied to DO_{20} and DO_{40}.
*6 Applied to O_1 to O_{40}.

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Switching Characteristics (1)

(V_{DD} = 5V±10%, Ta=–30 to +85°C, C_L=15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	t_{PLH}, t_{PHL}	—	—	—	250	ns
Clock Frequency	f_{CP}	Duty = 50%	—	—	3.3	MHz
Clock Pulse Width	$t_{W\ (CP)}$	—	125	—	—	ns
Load Pulse Width	$t_{W\ (L)}$	—	125	—	—	ns
Data Set-up Time DI → CP	t_{SETUP}	—	50	—	—	ns
Data Hold Time DI → CP	t_{HOLD}	—	50	—	—	ns
CP → LOAD Set-up Time	t_{CL}	—	250	—	—	ns
LOAD → CP Hold Time	t_{LC}	—	0	—	—	ns
CP Rise/Fall Time	$t_{r(CP)}$, $t_{f(CP)}$	—	—	—	50	ns
LOAD Rise/Fall Time	$t_{r(L)}$, $t_{f(L)}$	—	—	—	1	µs

Switching Characteristics (2)

(Only for static operation) (V_{DD} = 3V±0.5V, Ta=–30 to +85°C, C_L=15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	t_{PLH}, t_{PHL}	—	—	—	800	ns
Clock Frequency	f_{CP}	Duty = 50%	—	—	1.0	MHz
Clock Pulse Width	$t_{W\ (CP)}$	—	300	—	—	ns
Load Pulse Width	$t_{W\ (L)}$	—	300	—	—	ns
DI → CP Set-up Time	t_{SETUP}	—	200	—	—	ns
DI → CP Hold Time	t_{HOLD}	—	200	—	—	ns
CP → LOAD Set-up Time	t_{CL}	—	800	—	—	ns
LOAD → CP Hold Time	t_{LC}	—	0	—	—	ns
CP Rise/Fall Time	$t_{r(CP)}$	—	—	—	1	µs
LOAD Rise/Fall Time	$t_{r(L)}$, $t_{f(L)}$	—	—	—	1	µs

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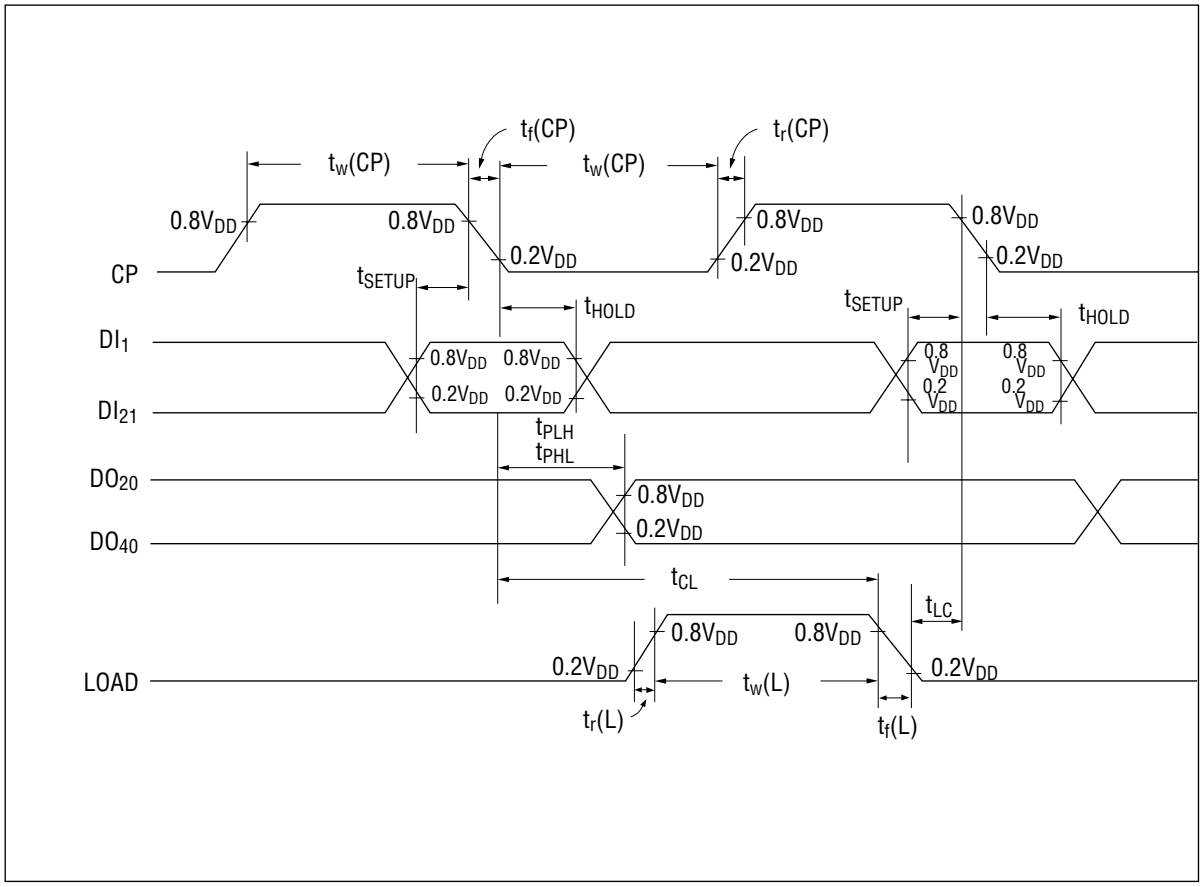

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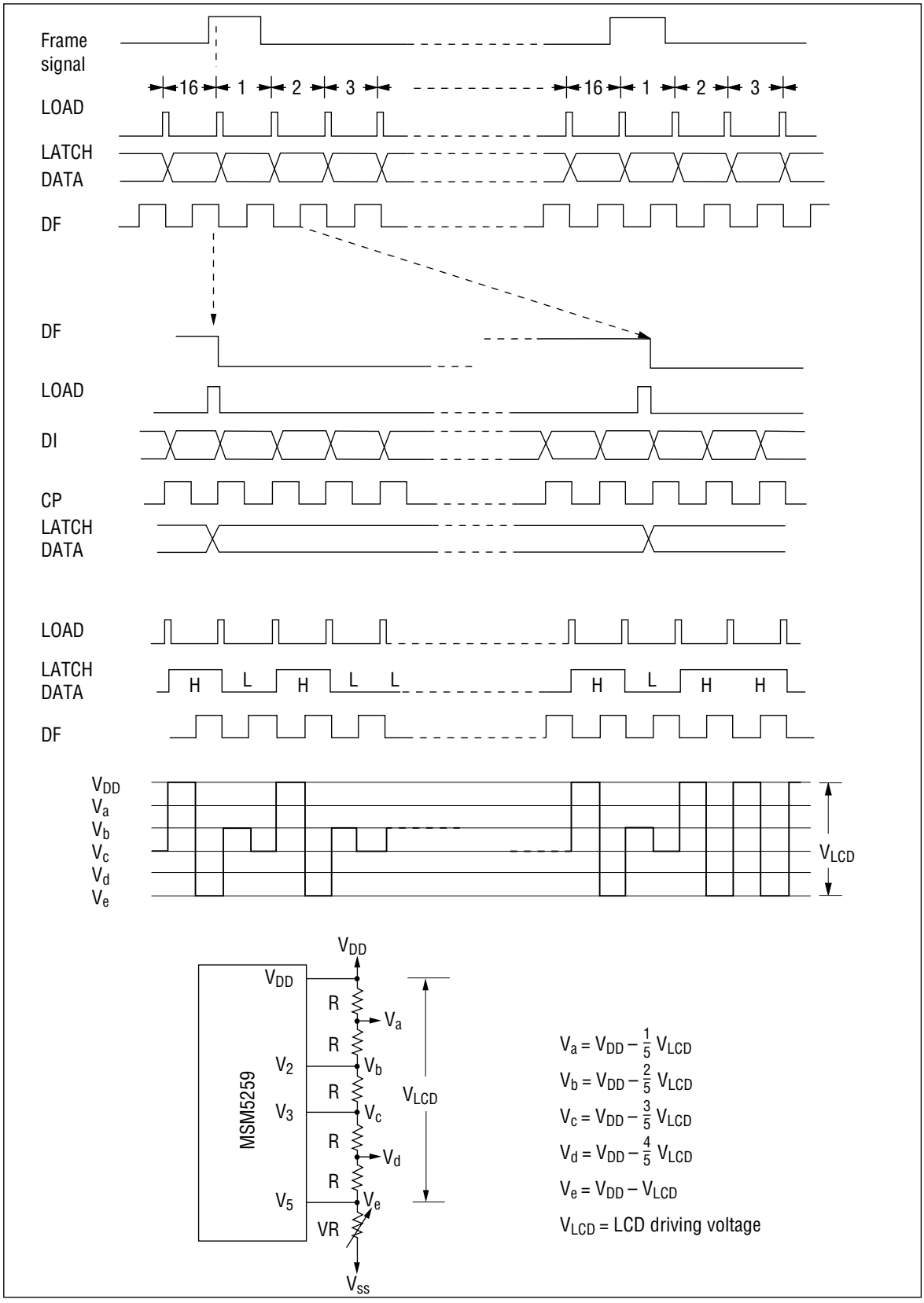
TIMING DIAGRAM

1/5 bias, 1/16 duty



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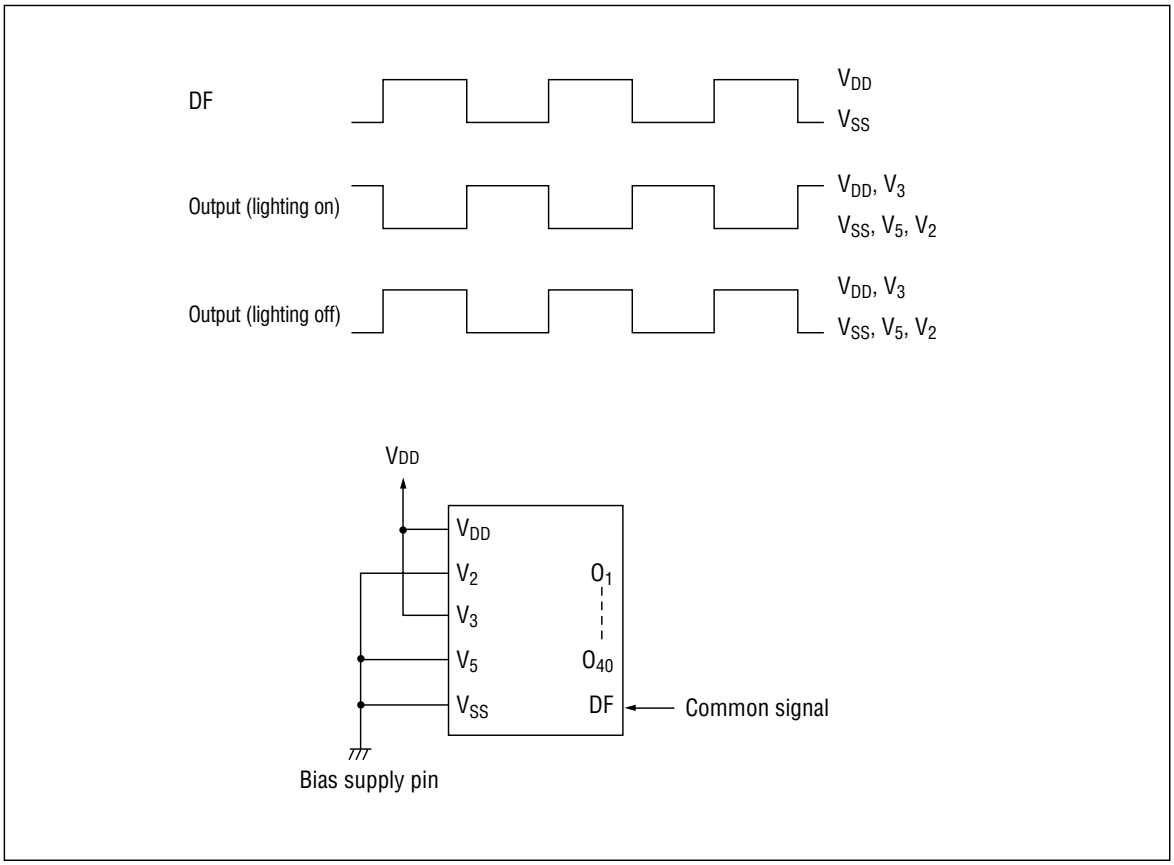
Static Display



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FUNCTIONAL DESCRIPTION

Pin Functional Description

- **DI_1**
  The data (1st to 20th bit) from the LCD controller LSI is input to 20-bit shift register from DI_1. (Positive logic)

- **DI_{21}**
  Data input to the shift register (21st to 41st bit).
  Connecting DO_{20} and DI_{21} allows configuration of a 40-bit register.
  If DI_{21} is not used, connect this pin to V_{SS}.

- **CP**
  Clock pulse input pin for the two 20-bit shift registers. The data is input to the 20-bit shift register at the falling edge of the clock pulse. A data set up time (t_{SETUP}) and data hold time (t_{HOLD}) are required between the DI1 and DI21 signals and a clock pulse.

- **DO_{20}**
  20th bit of the shift register contents is output from DO_{20}. The data which was input from DI_1 is output from this pin with a delay of the number of bits of the shift register (20), synchronized with the clock pulse. By connecting DO_{20} to DI_{21}, two 20-bit shift registers can be used as a 40-bit shift register.

- **DO_{40}**
  40th bit of the shift register contents is output from DO_{40}. The data which was input from DI_{21} is output from this pin with a delay of the number of bits of the shift register (20), synchronized with the clock pulse. By connecting DO_{40} to the next MSM5259's DI_1, this LSI is applicable to a wide screen LCD.
  Refer to the application circuit.

- **DF**
  Alternate signal input pin for LCD driving.

- **LOAD**
  Signal for latching the shift register contents is input from this pin. When the LOAD pin is set at "H" level, the shift register contents are transferred to the 40-bit 4-level driver. When LOAD pin is set at "L" level, the last display output data (O_1 - O_{40}), which was transferred when LOAD pin was at "H" level, is held.

- **V_{DD}, V_{SS}**
  Supply voltage pins.
  V_{DD} is generally set to 4.0 to 6.0V. V_{SS} is a ground pin (V_{SS} = 0V)

- **V_2, V_3, V_5**
  Bias supply voltage pins to drive the LCD. Bias voltage divided by the register is usually used as supply voltage source.
  Refer to the application circuit.
  For static operation, connect V_3 to V_{DD} and also connect V_2, V_5, to V_{SS}.

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- **O_1 to O_{40}**
  Display data output pin which corresponds to each data bit in the latch. One of V_{DD}, V_2, V_3 and V_5 is selected as a display driving voltage source according to the combination of latched data level and DF signal. (Refer to the truth table below.)

Truth Table

Latched data	DF	Driver output level
"H" (Select)	H	V_5
	L	V_{DD}
"L" (Non-select)	H	V_3
	L	V_2

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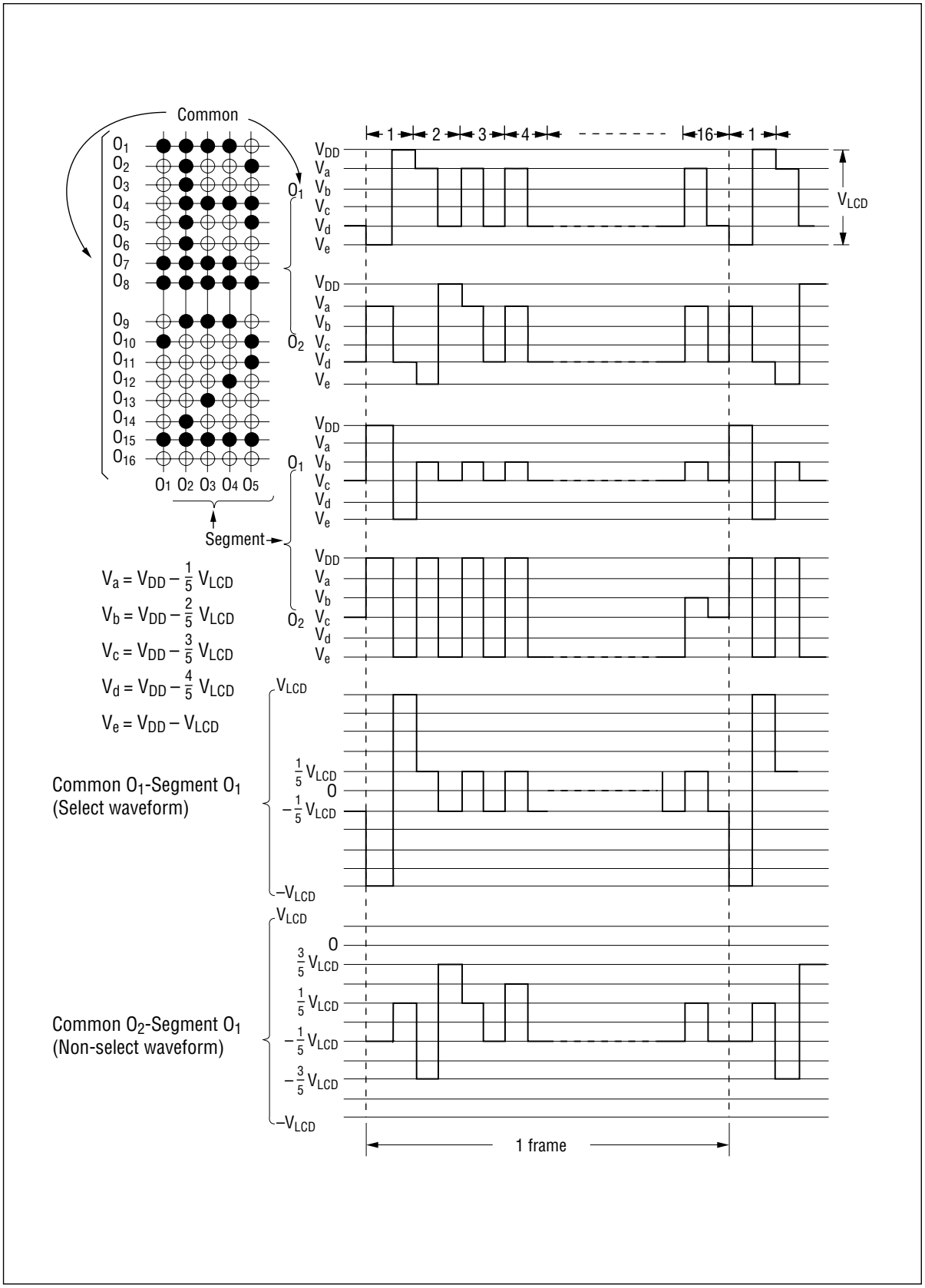
LCD Driving Waveform (1/5 bias, 1/16 duty)



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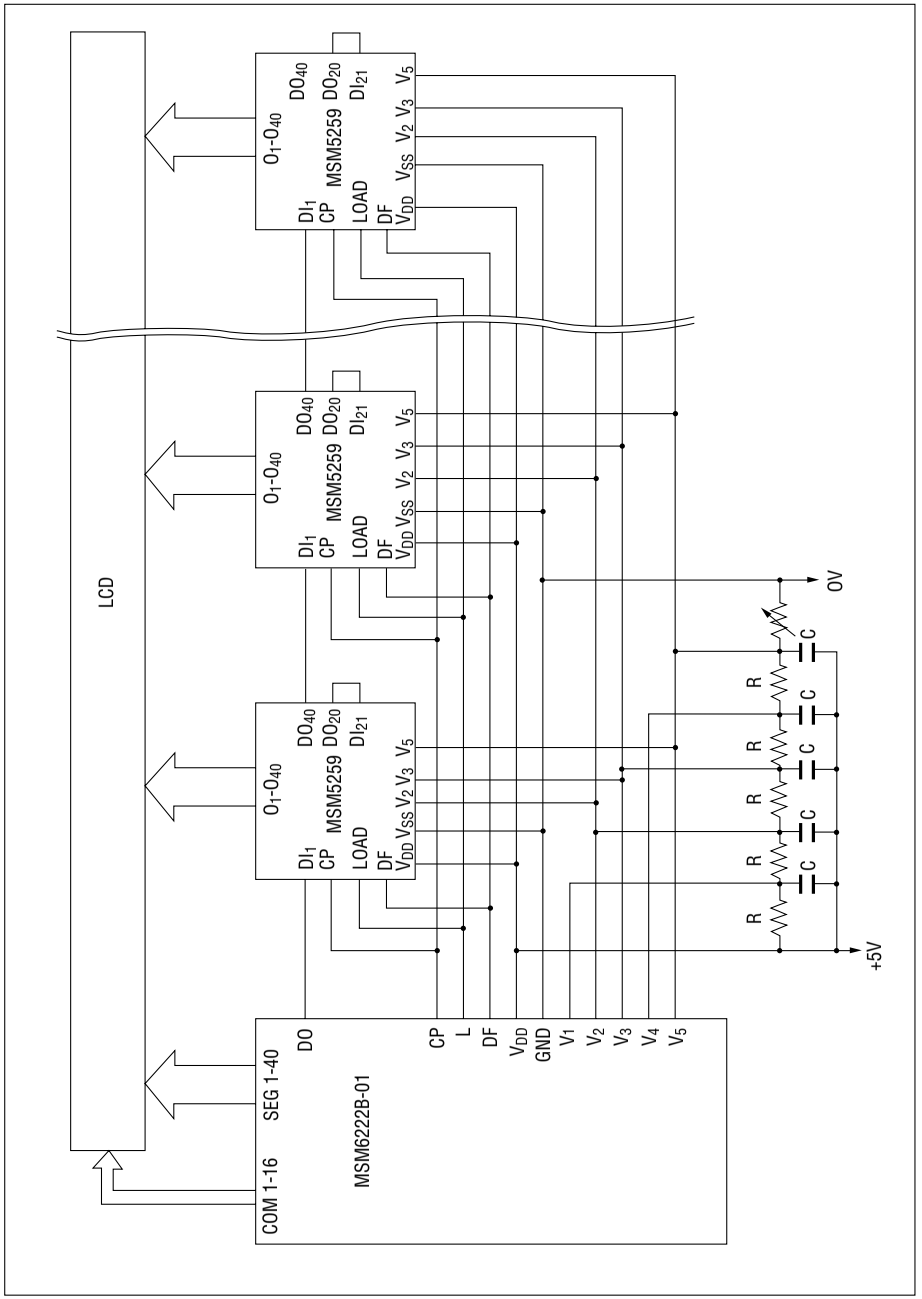
APPLICATION CIRCUITS

(Connected to MSM6222B-01 LCD Controller)



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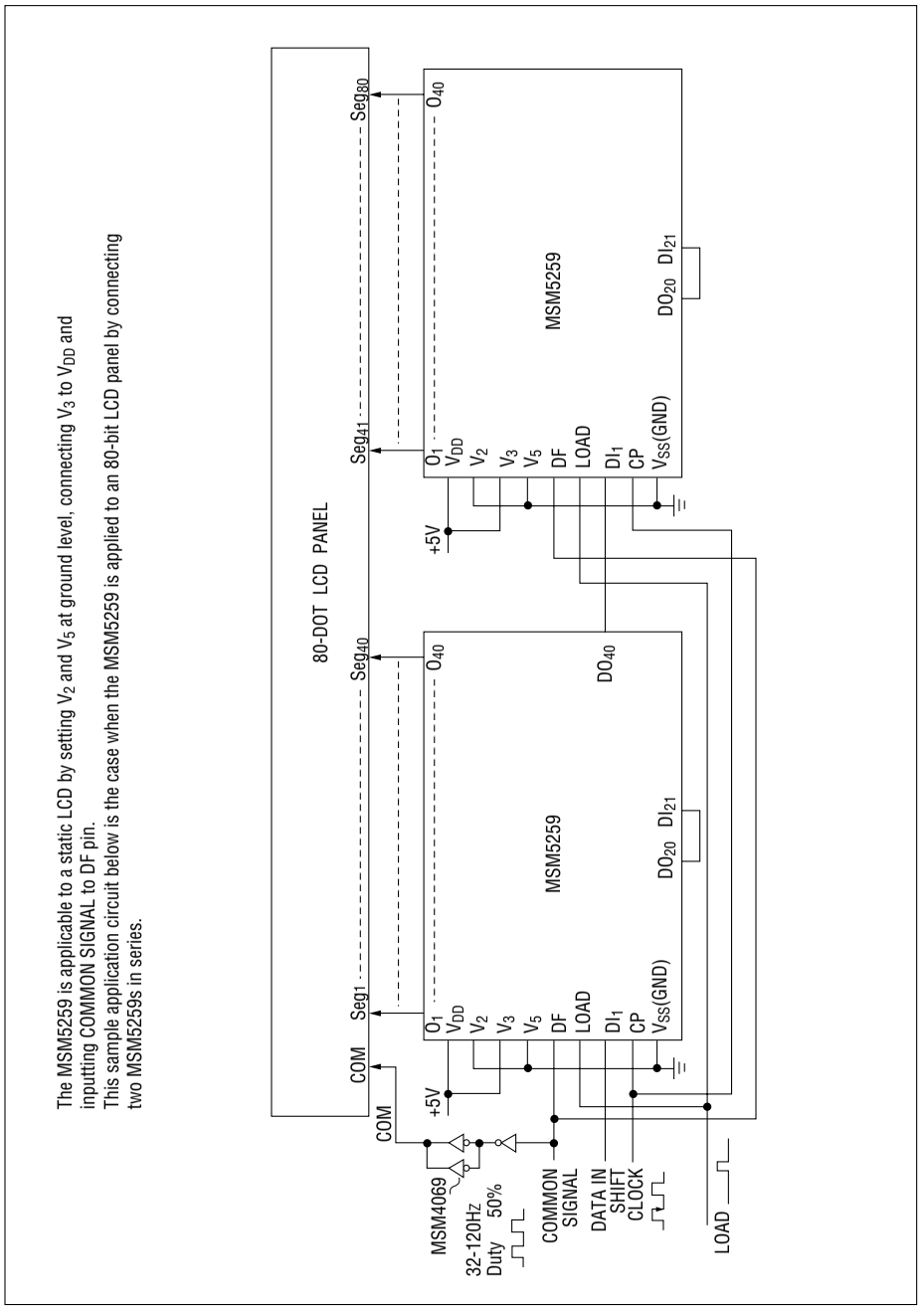
Application Circuit for Static Display

The MSM5259 is applicable to a static LCD by setting V_2 and V_5 at ground level, connecting V_3 to V_{DD} and inputting COMMON SIGNAL to DF pin.
This sample application circuit below is the case when the MSM5259 is applied to an 80-bit LCD panel by connecting two MSM5259s in series.



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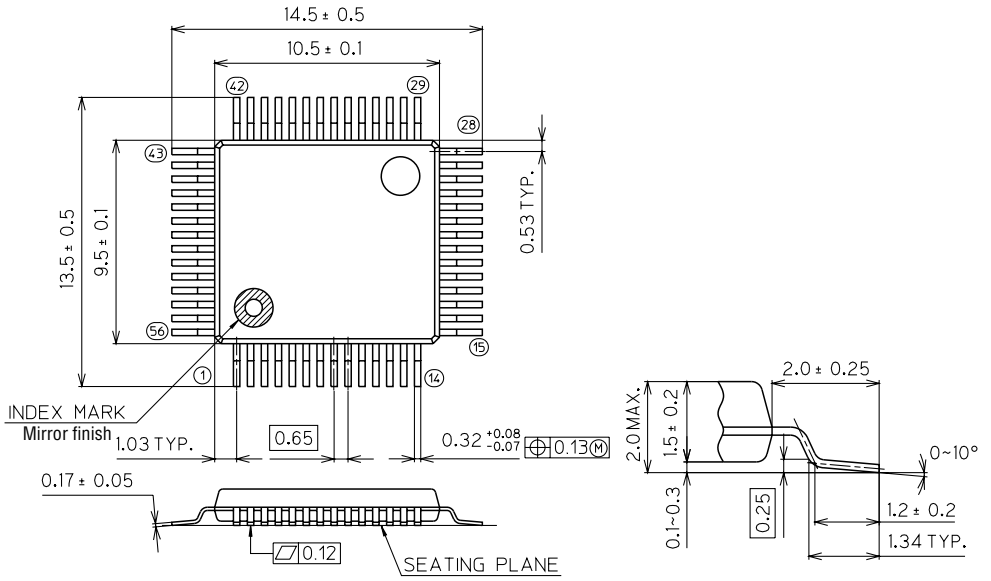
PACKAGE DIMENSIONS

(Unit : mm)

QFP56-P-910-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.36 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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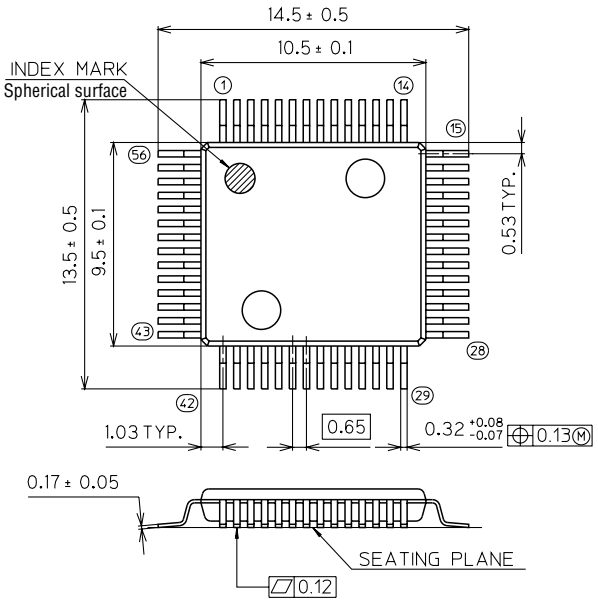
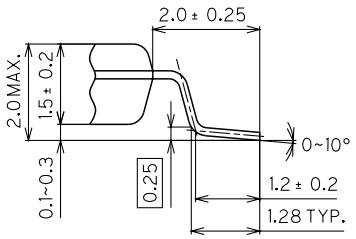
(Unit : mm)

QFP56-P-910-0.65-L2





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.36 TYP.

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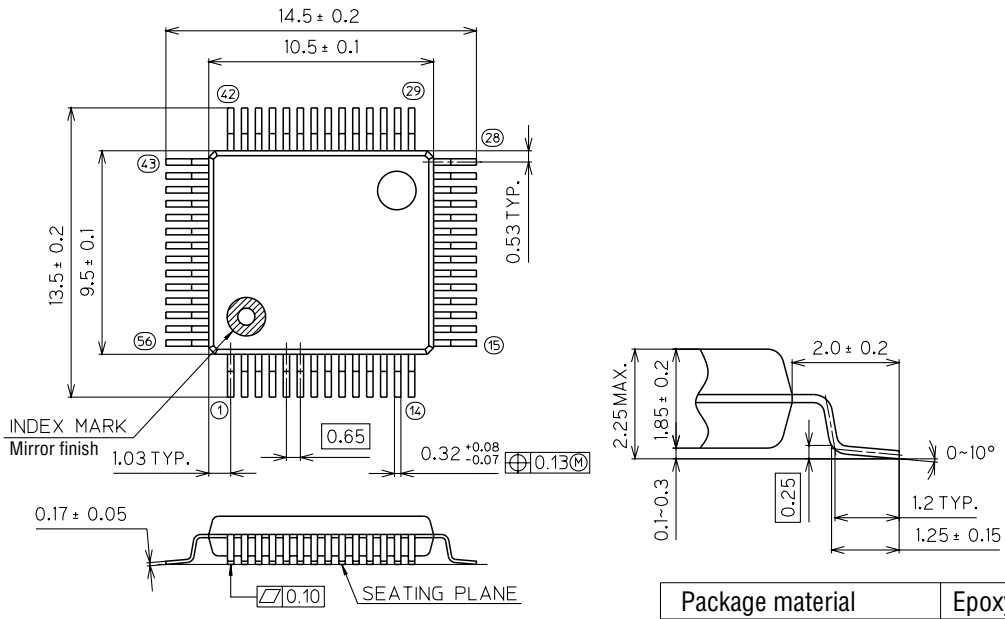
(Unit : mm)

QFP56-P-910-0.65-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mount Type Package

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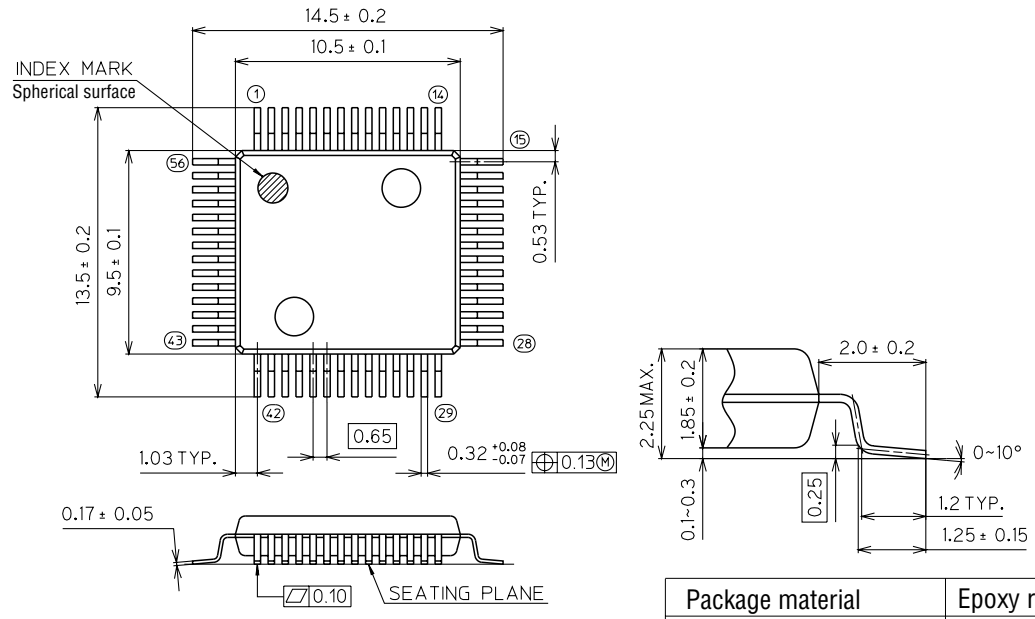
(Unit : mm)

QFP56-P-910-0.65-2L2



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mount Type Package

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