
MSM6606

80-DOT LCD DRIVER WITH KEY MATRIX

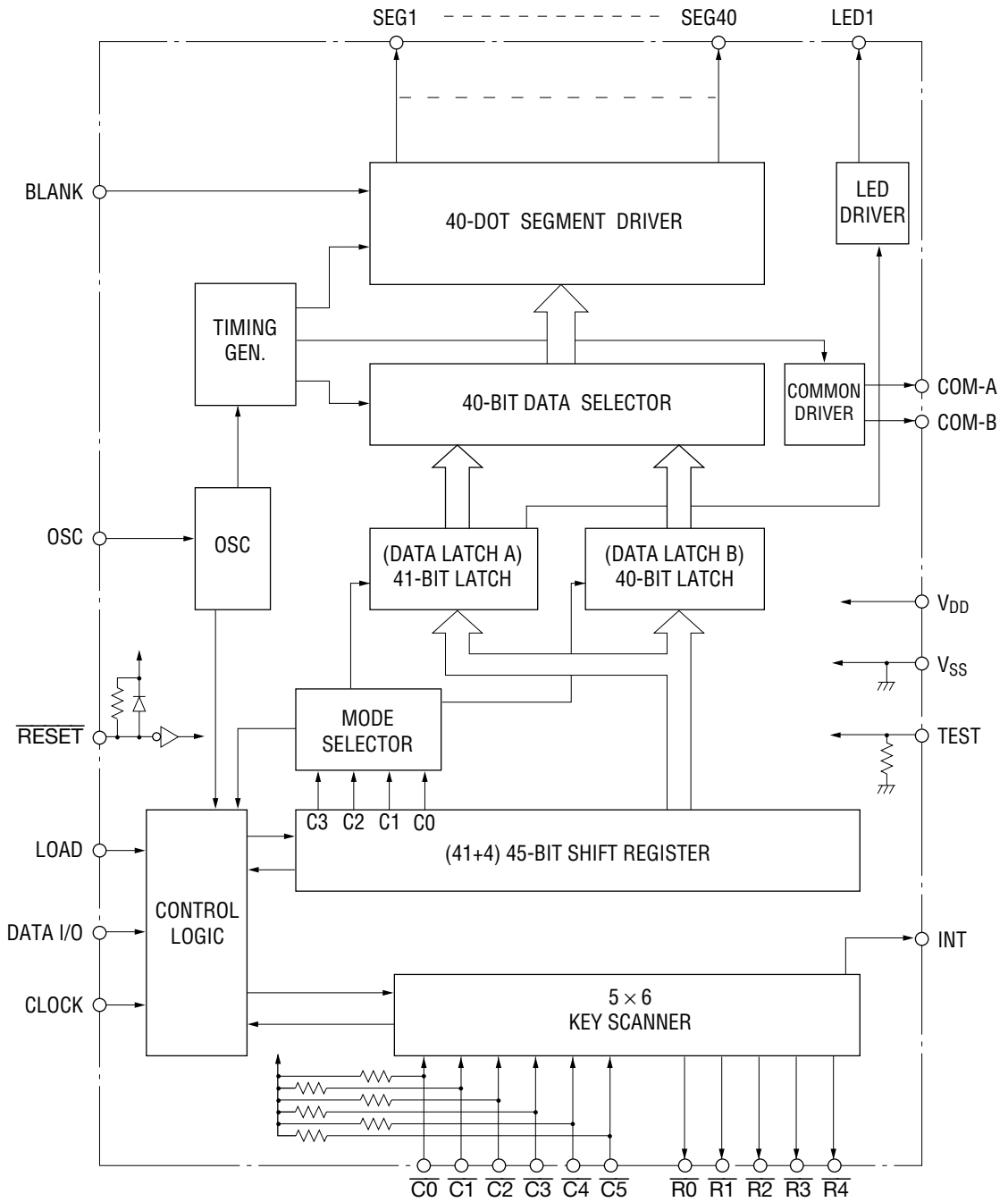
GENERAL DESCRIPTION

The MSM6606 is an LCD driver for a 1/2 duty dynamic display. It can directly drive an LCD of up to 80 segments, and one LED. Keyboard input is now available by the internal 5 x 6 keyscan circuit, and the number of wires between the front panel and the CPU can be minimized.

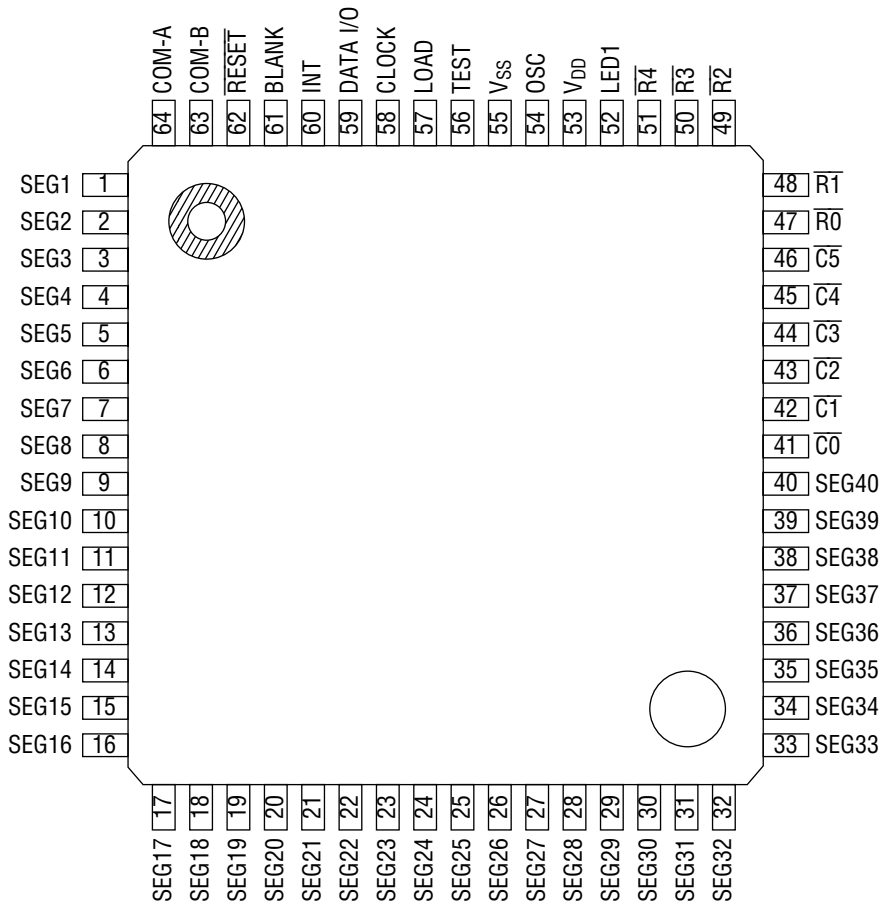
FEATURES

- Power supply voltage : 5V \pm 10%
- Temperature range : -40 to +85°C
- Can display an LCD of up to 80 segments (1/2 duty dynamic drive)
- Can directly drive one LED ($I_O = -15$ mA max.)
- Internal 5 x 6 keyscan circuit allows reading of the status of up to 30 key switches
- A serial interface with the CPU is implemented by LOAD, DATA I/O, and CLOCK
- Built-in RC oscillation circuit for LCD alternating current drive
- Built-in voltage dividing resistor for bias voltage generation
- Package:
64-pin plastic QFP (QFP64-P-1414-0.80-BK) (Product name : MSM6606GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to +6.5	V
Input Voltage	V_I	$T_a = 25^\circ\text{C}$	-0.3 to $V_{DD}+0.3$	V
Output Current	I_O	$T_a = 25^\circ\text{C}$ *1	-20	mA
Storage Temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$

*1 Applicable to LED1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	4.5 to 5.5	V
Operating Temperature	T_{op}	—	-40 to +85	$^\circ\text{C}$

Recommended Oscillation Circuit Conditions

Parameter	Symbol	Condition	Min.	Max.	Unit
Oscillation Resistance	R_O	—	20	120	$\text{k}\Omega$
Oscillation Capacitance	C_O	—	0.01	0.047	μF

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5V ±10%, T_a = -40 to +85°C)

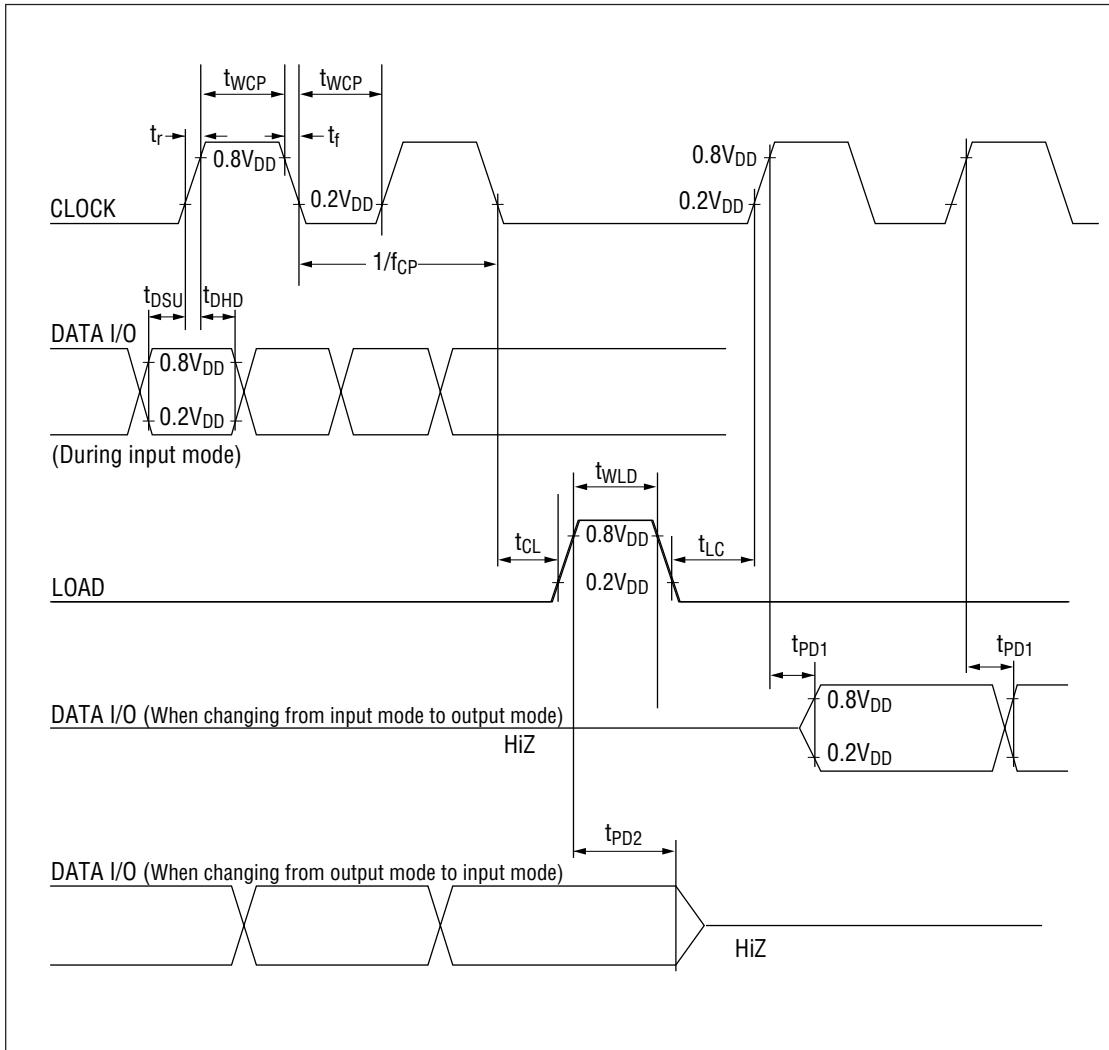
Parameter	Symbol	Condition	Min.	Max.	Unit	Applicable Pin
"H" Input Voltage	V _{IH}	—	0.7V _{DD}	V _{DD}	V	All inputs
"L" Input Voltage	V _{IL}	—	V _{SS}	0.3V _{DD}	V	
"H" Input Current	I _{IH1}	V _{DD} = 5.5V, V _I = V _{DD}	—	1	μA	CLOCK, LOAD BLANK
"L" Input Current	I _{IL1}	V _{DD} = 5.5V, V _I = 0V	—	-1	μA	
"H" Input Current	I _{IH2}	V _{DD} = 5.5V, V _I = V _{DD}	—	10	μA	DATA I/O
"L" Input Current	I _{IL2}	V _{DD} = 5.5V, V _I = 0V	—	-10	μA	
"L" Input Current	I _{IL3}	V _{DD} = 5.0V, V _I = 0V	-0.18	-0.8	mA	$\overline{C0} - \overline{C5}$
"L" Input Current	I _{IL4}	V _{DD} = 5.0V, V _I = 0V	-0.02	-0.1	mA	\overline{RESET}
"H" Output Voltage	V _{OH1}	V _{DD} = 4.5V, I _O = -30μA	4.3	—	V	SEG1 - SEG40
"L" Output Voltage	V _{OL1}	V _{DD} = 4.5V, I _O = 30μA	—	0.2	V	
"H" Output Voltage	V _{OH2}	V _{DD} = 4.5V, I _O = -150μA	4.3	—	V	COM-A COM-B
"L" Output Voltage	V _{OL2}	V _{DD} = 4.5V, I _O = 150μA	—	0.2	V	
"H" Output Voltage	V _{OH3}	V _{DD} = 4.5V, I _O = -15mA	3.0	—	V	LED1
"L" Output Voltage	V _{OL3}	V _{DD} = 4.5V, I _O = 0.1mA	—	0.4	V	
"H" Output Voltage	V _{OH4}	V _{DD} = 4.5V, I _O = -0.4mA	4.1	—	V	DATA I/O INT
"L" Output Voltage	V _{OL4}	V _{DD} = 4.5V, I _O = 0.4mA	—	0.4	V	
"H" Output Voltage	V _{OH5}	V _{DD} = 4.5V, I _O = -50μA	2.5	—	V	$\overline{R0} - \overline{R4}$
"L" Output Voltage	V _{OL5}	V _{DD} = 4.5V, I _O = 1.0mA	—	0.4	V	
"M" Output Voltage	V _{OM}	V _{DD} = 4.5V, I _O = 0mA	2.15	2.35	V	COM-A COM-B
"M" Output Resistance	R _{OM}	V _{DD} = 4.5V, I _O = ±10μA *1	—	100	kΩ	
Supply Current	I _{DD}	V _{DD} = 5.5V, no load *2	—	0.5	mA	V _{DD}

*1 R_{OM} = (V_O - V_{OM})/I_O*2 V_{IH} = V_{DD}, V_{IL} = 0 V, f_{OSC} = 3.2 kHz

Switching Characteristics

 $(V_{DD} = 5V \pm 10\%, T_a = -40 \text{ to } +85^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Frequency	f_{CP}	—	—	2.0	MHz
Clock Pulse Width	t_{WCP}	—	200	—	ns
Rise/Fall Time	t_r, t_f	—	—	50	ns
Data Setup Time	t_{DSU}	—	100	—	ns
Data Hold Time	t_{DHD}	—	100	—	ns
Load Pulse Width	t_{WLD}	—	200	—	ns
Clock→Load Time	t_{CL}	—	100	—	ns
Load→Clock Time	t_{LC}	—	200	—	ns
Output Delay Time 1	t_{PD1}	$C_L = 50\text{pF}$	—	300	ns
Output Delay Time 2	t_{PD2}	—	—	300	ns



FUNCTIONAL DESCRIPTION

Pin Functional Description

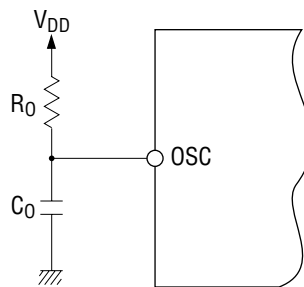
- **OSC**

This is an input pin for the oscillator to generate LCD display and keyscan signals. Connect an external capacitor and a resistor as shown below to form an RC oscillation circuit.

The relationship between frame frequency f_{FRM} , keyscan period T_{SCN} , and oscillation frequency f_{OSC} is:

$$T_{SCN} = 15/f_{OSC}, f_{FRM} = f_{OSC}/32$$

(See the reference data for information on relationship between C_O and R_O values, and frame frequency or keyscan periods.)



- **Data I/O**

This is a serial data input/output. The pin is in output state from the first shift clock rise after "Key Data Output" command writing, to the load signal rise, and in input state otherwise. (The pin is in input state after reset.)

The relationship between the data level and operation is as shown below:

Level	Display	Key Status
"H"	ON	ON (close)
"L"	OFF	OFF (open)

- **CLOCK**

This is an input pin for the shift clock. DATA I/O pin data is either input or output in synchronization with the rising edge of the clock.

- **LOAD**

This is a load signal input pin used to transfer serial input data to a latch for display, to write commands, or to reset the DATA I/O pin to an input state.

- **BLANK**

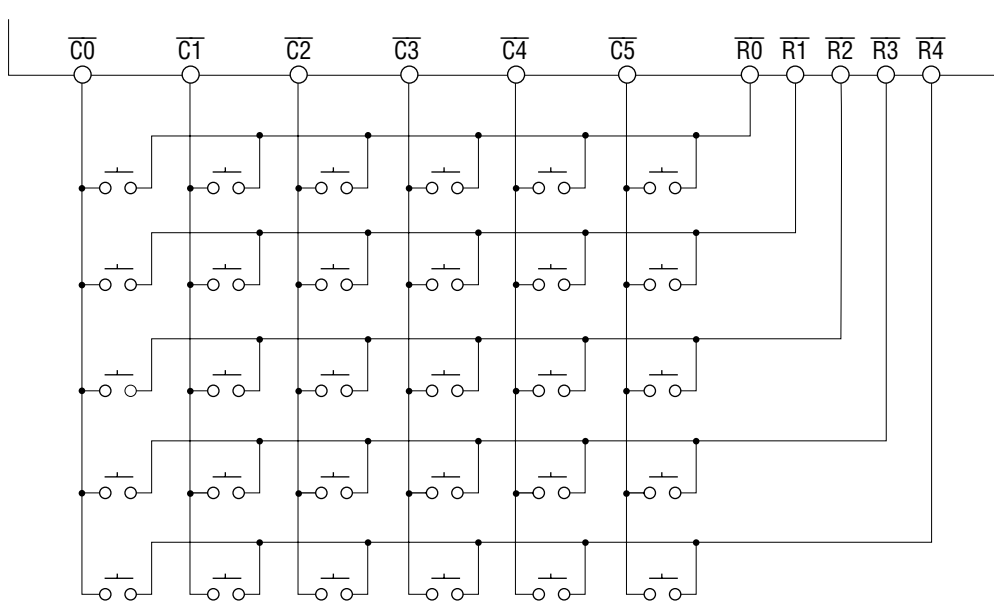
This is a display blanking signal input pin. At "H" level the LED and LCD displays go out regardless of the display data. The display returns to the original status at "L" level.

- $\overline{R0} - \overline{R4}$

These are keyswitch scan signal output pins. During the scan operating, "L" level is output in the order of $\overline{R0}$, $\overline{R1}$, ..., $\overline{R4}$. All signals go to "L" level when scanning stops.

- $\overline{C0} - \overline{C5}$

These are input pins that detect the key status. A pull-up resistor is built in. Key matrices are formed with $\overline{R0} - \overline{R4}$ pins.

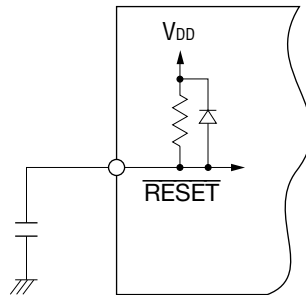


- INT

This is the keyscan end signal output pin. This pin becomes "H" level when one scan cycle ends, and returns to "L" level by a load signal after data is output or the "Key Scan Stop" command is written. (This pin goes to "L" level at reset.)

- **RESET**

This is the reset signal input pin that initializes the IC, and it is activated at "L" level. A pull-up resistor is built in. The power ON reset operation is performed by externally connecting a capacitor.



- **SEG1 - SEG40**

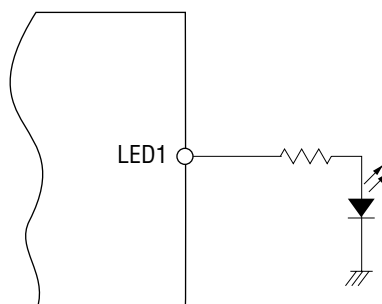
These are the output pins for the LCD display, and are connected to the segment pins of the LCD panel. See the section on data configuration for the relationship between the SEG output and input data.

- **COM-A, COM-B**

These are output pins for the LCD display and are connected to the common pins of the LCD panel.

- **LED1**

This is an output pin for the LED drive. A LED and a current limiting resistor are externally connected.



- **TEST**

This is an input pin for IC testing. This pin should be connected to V_{SS} .

- **V_{DD} , V_{SS}**

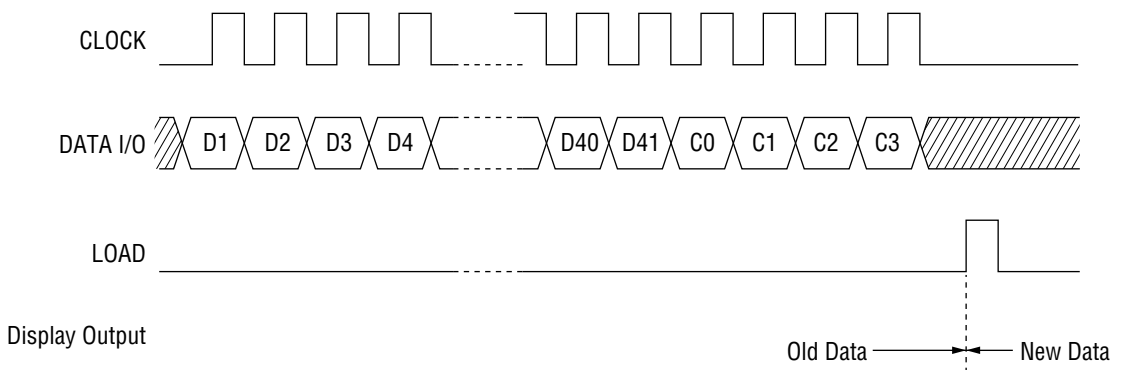
These are power supply voltage and ground pins, respectively.

Operational Description

• Display data input

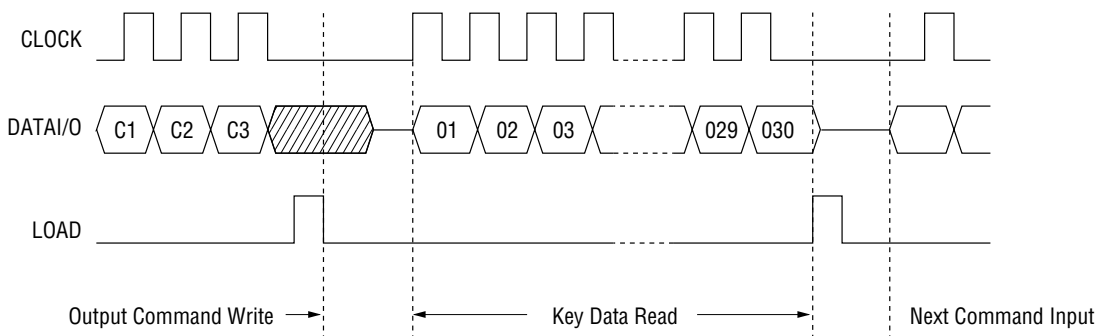
As shown in the section on data configuration, the data for display consists of a data field corresponding to segments ON/OFF and a command field indicating display data input.

The C0 bit of the command field is set to "0" (common A) or "1" (common B) according to the common corresponding to the display data. LED display data corresponds to common A. Data input to the DATA I/O pin is captured by a shift register at rising edge of a clock signal, then is transferred to a data latch for display when the LOAD signal is at "H" level, and is output through a segment driver.



• Key data output

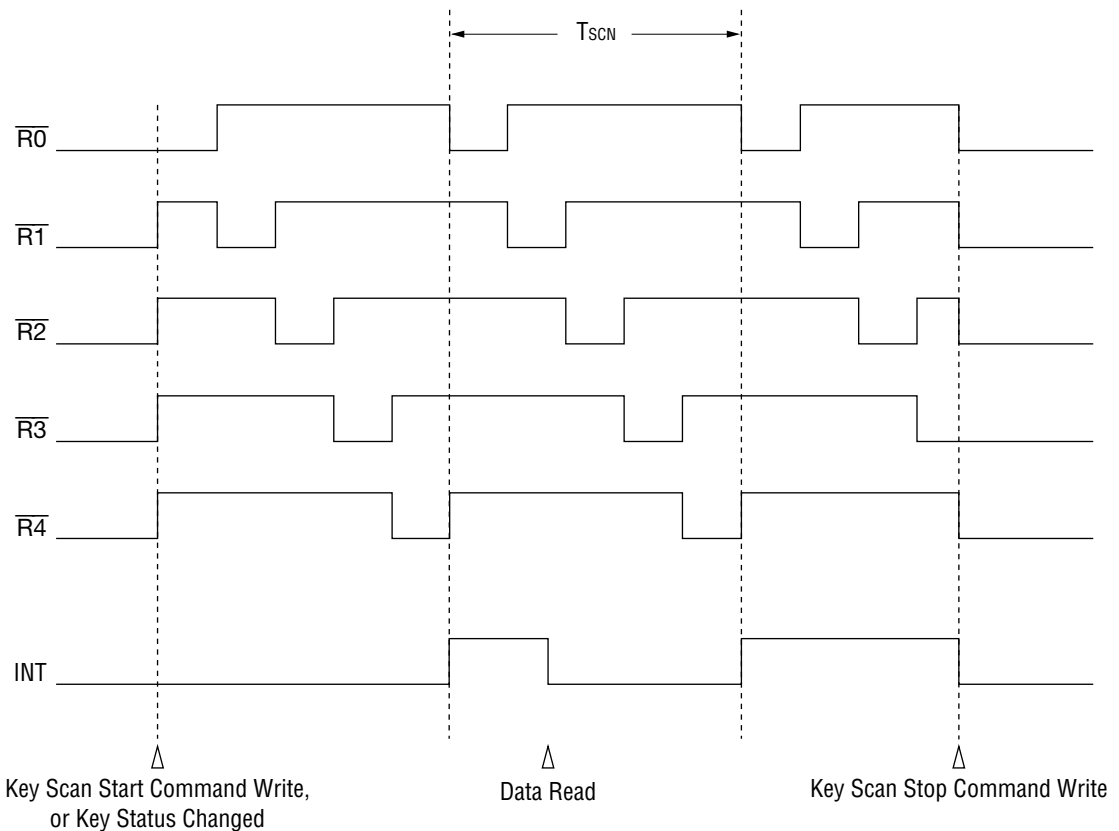
The status of a key switch is indicated by ON = 1, OFF = 0, and is read as 30-bit serial data. (For information on the sequence, see the section on data configuration.) To output data, first write the "Key Data Output" command, then apply a clock signal. Data is then output synchronizing with the rising edge of the clock signal. After that, when a LOAD pulse is added, the DATA I/O pin returns to the input state, and the next data or command can be input.



• Keyscan

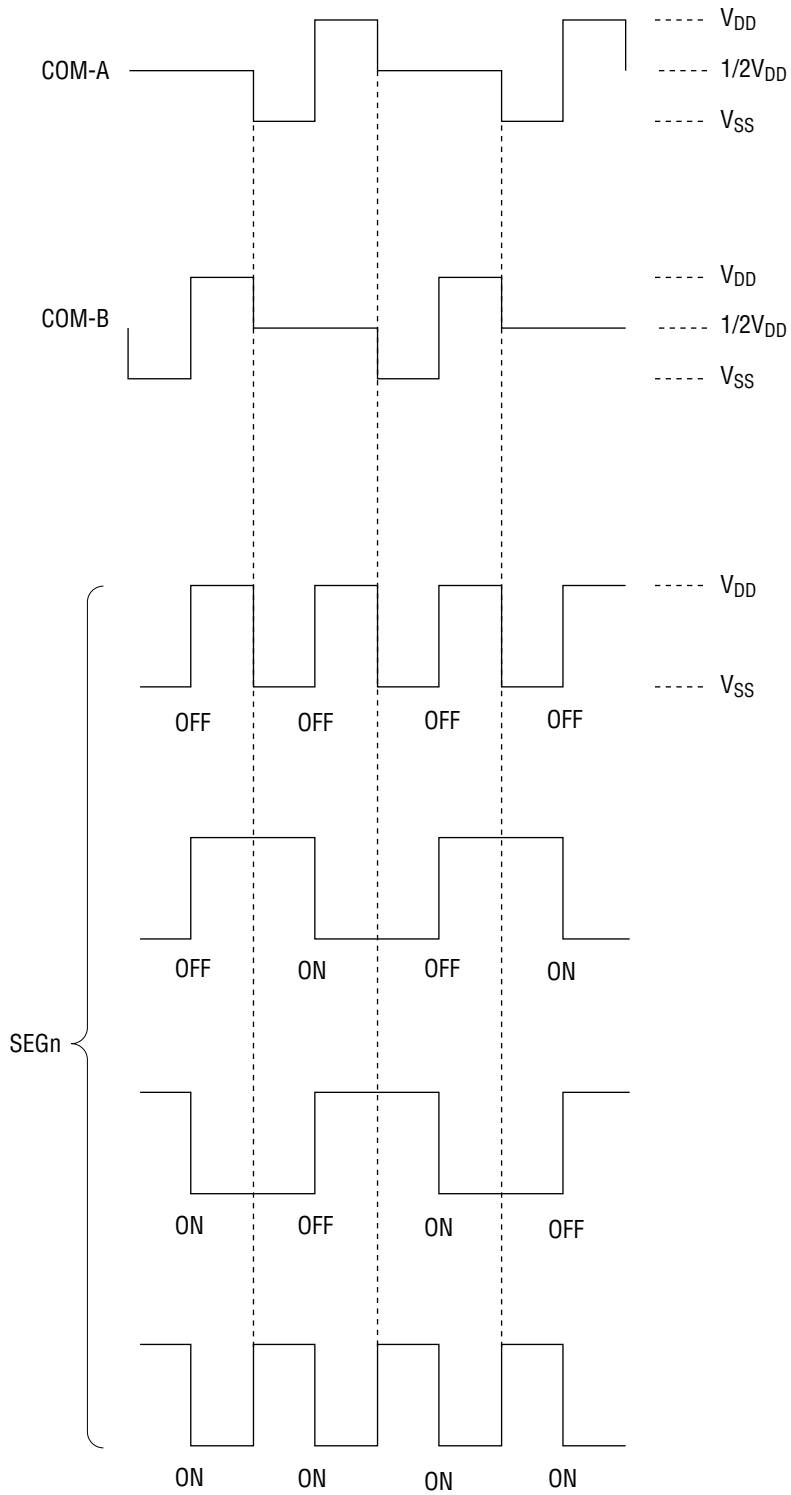
Keyscan starts when the key status has changed, or when the "Key Scan Start" command has been written. Scan continues until the "Key Scan Stop" command is written. (Scan stops when a reset signal is applied.)

When 1 keyscan cycle (T_{SCN}) ends, the INT signal becomes "H", so this signal can be used as an interrupt flag, which is dependent on switching conditions of keys. The INT signal is reset when either the LOAD pulse is input after the key data is output, when the "Key Scan Stop" command is set, or when a reset signal is applied.



- Notes:**
1. A recognition error (a switch that was actually not pressed is recognized as having been pressed) may occur if 3 or more key switches are pressed at the same time. If simultaneous pressing of 3 or more key switches needs recognizing, serially insert diodes into each switch. If pressing 3 or more key switches at the same time is not allowed, a possible software approach is to ignore the read data when there are 3 or more 1s in the key data.
 2. A change of key status is detected as a change of column inputs (C0 - C5). Therefore if multiple switches which are connected to the same column are pressed at the same time, a change of key status will not be detected.

LCD Drive Waveform



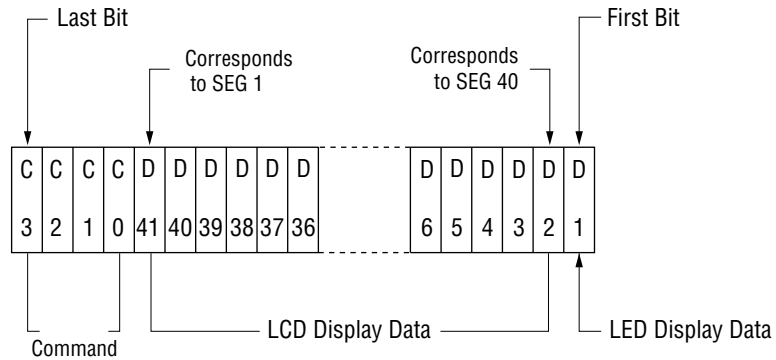
Commands List

Command	C3	C2	C1	C0	Operation
F1	0	0	1	0	Display Data Input (Corresponding to common A)
				1	Display Data Input (Corresponding to common B)
F2	0	1	0	x	Key Data Output
F3	0	1	1	0	Display Data Input (A) + Key Data Output
				1	Display Data Input (B) + Key Data Output
F4	1	1	0	x	Key Scan Stop + Key Data Output
F5	1	0	0	x	Key Scan Stop
F6	1	1	1	x	Key Scan Start + Key Data Output

x : Don't care

Data Configuration

[Input Data]



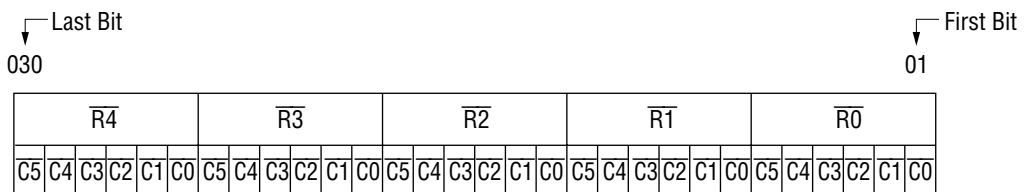
Note 1: LED data corresponds to common A side (C0 = 0).

Note 2: D1 bit is unnecessary when LED output is not used.

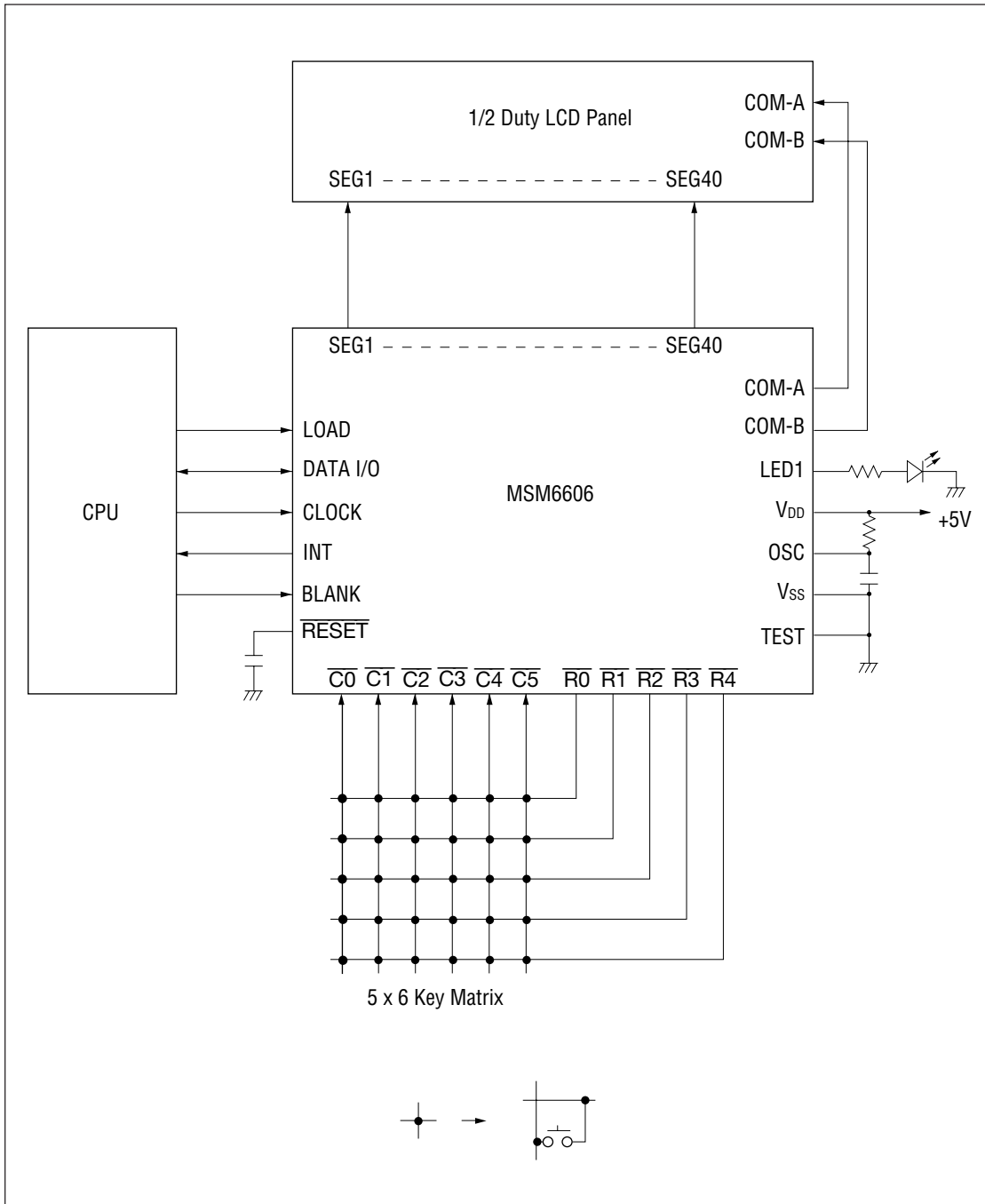
Note 3: Commands F2, F4-F6 become effective if at least 3 bits (C1-C3) are input (D1-D41, C0 bits are not necessary).

Note 4: If dummy bits are necessary, add them before first bit.

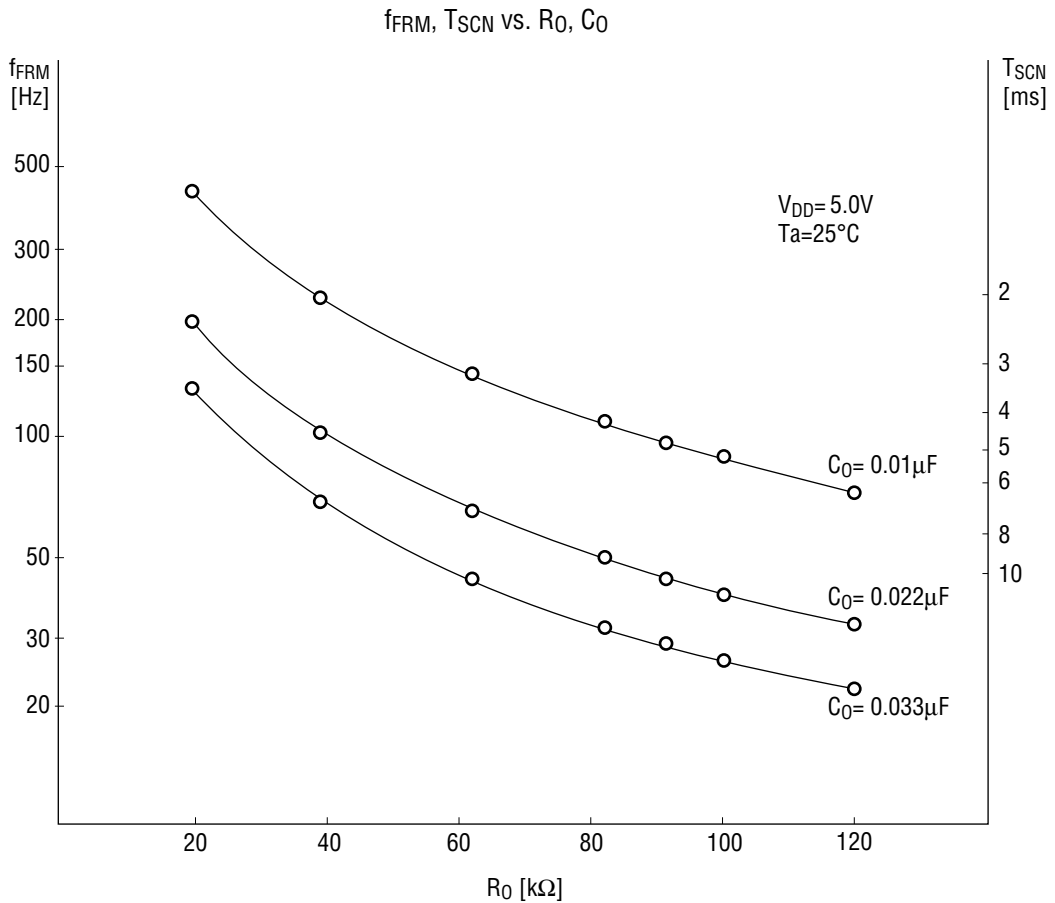
[Output Data]



APPLICATION CIRCUIT



REFERENCE DATA



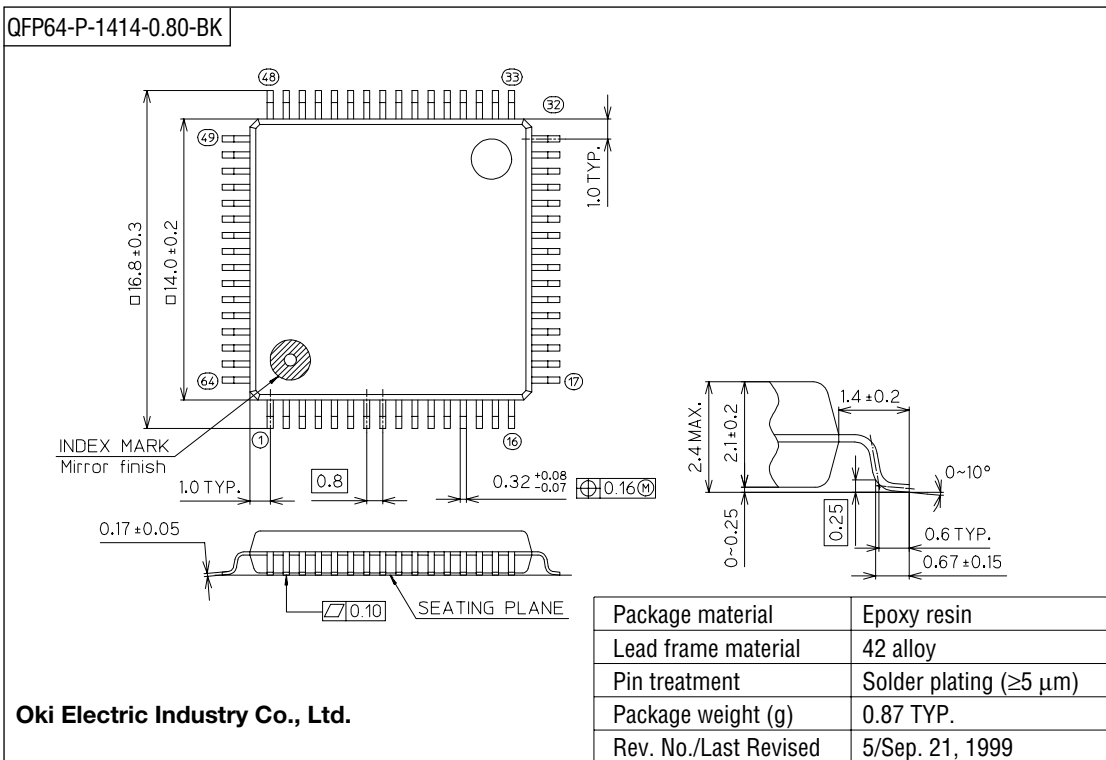
The frequency changes depending on supply voltages and temperatures.

For V_{DD} , the frequency becomes about 5% higher at $5 \pm 0.5V$ than at 5V.

For temperature, the frequency becomes about 12% higher at $T_a = -40^\circ C$ and becomes about 10% lower at $T_a = 85^\circ C$ than at $T_a = 25^\circ C$. (The temperature characteristic of an external resistor and capacitor is not taken into consideration here.)

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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