STV6886

LOW-COST I²C CONTROLLED DEFLECTION PROCESSOR FOR MULTISYNC MONITOR

FEATURES

General

- SYNC PROCESSOR (separate or composite)
- 12V SUPPLY VOLTAGE
- 8V REFERENCE VOLTAGE
- HOR. LOCK/UNLOCK OUTPUT
- HOR. & VERT. LOCK/UNLOCK INDICATION
- READ/WRITE I²C INTERFACE
- HORIZONTAL AND VERTICAL MOIRE
- B+ REGULATOR
  - Internal PWM generator for B+ current mode step-up converter
  - Switchable to step-down converter
  - I²C-adjustable B+ reference voltage
  - Output pulses synchronized on horizontal frequency
  - Internal maximum current limitation.

Horizontal

- Self-adaptative
- Dual PLL concept
- 80kHz maximum frequency
- X-ray protection input
- I²C controls: Horizontal duty-cycle, H-position, horizontal size amplitude

Vertical

- Vertical ramp generator
- 50 to 120 Hz agc loop
- Geometry tracking with VPOS & VAMP
- I²C controls:VAMP, VPOS, S-CORR, C-CORR
- Vertical breathing compensation

I²C Geometry Corrections

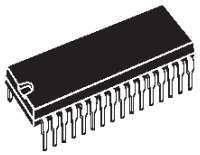
- Vertical parabola generator (Pin Cushion - E/W, Keystone, Corner Correction)
- Horizontal dynamic phase (Side Pin Balance & Parallelogram)
- Horizontal and vertical dynamic focus (Horizontal Focus Amplitude, Horizontal Focus Symmetry, Vertical Focus Amplitude)

DESCRIPTION

The STV6886 is a monolithic integrated circuit assembled in a 32-pin shrink dual-in-line plastic package. This IC controls all the functions related to horizontal and vertical deflection in multimode or multi-frequency computer display monitors.

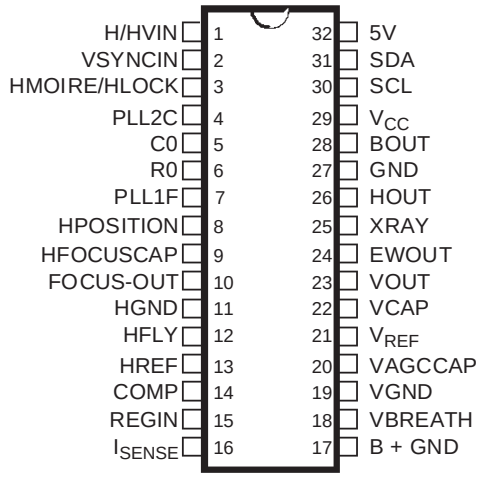
The internal sync processor, combined with the powerful geometry correction block, makes the STV6886 suitable for very high performance monitors, using few external components.

Combined with other ST components dedicated for CRT monitors (microcontroller, video preamplifier, video amplifier, OSD controller) the STV6886 allows fully I²C bus-controlled computer display monitors to be built with a reduced number of external components.



SHRINK32 (Plastic Package)
ORDER CODE: STV6886

PIN CONNECTIONS



Version 4.2

TABLE OF CONTENTS

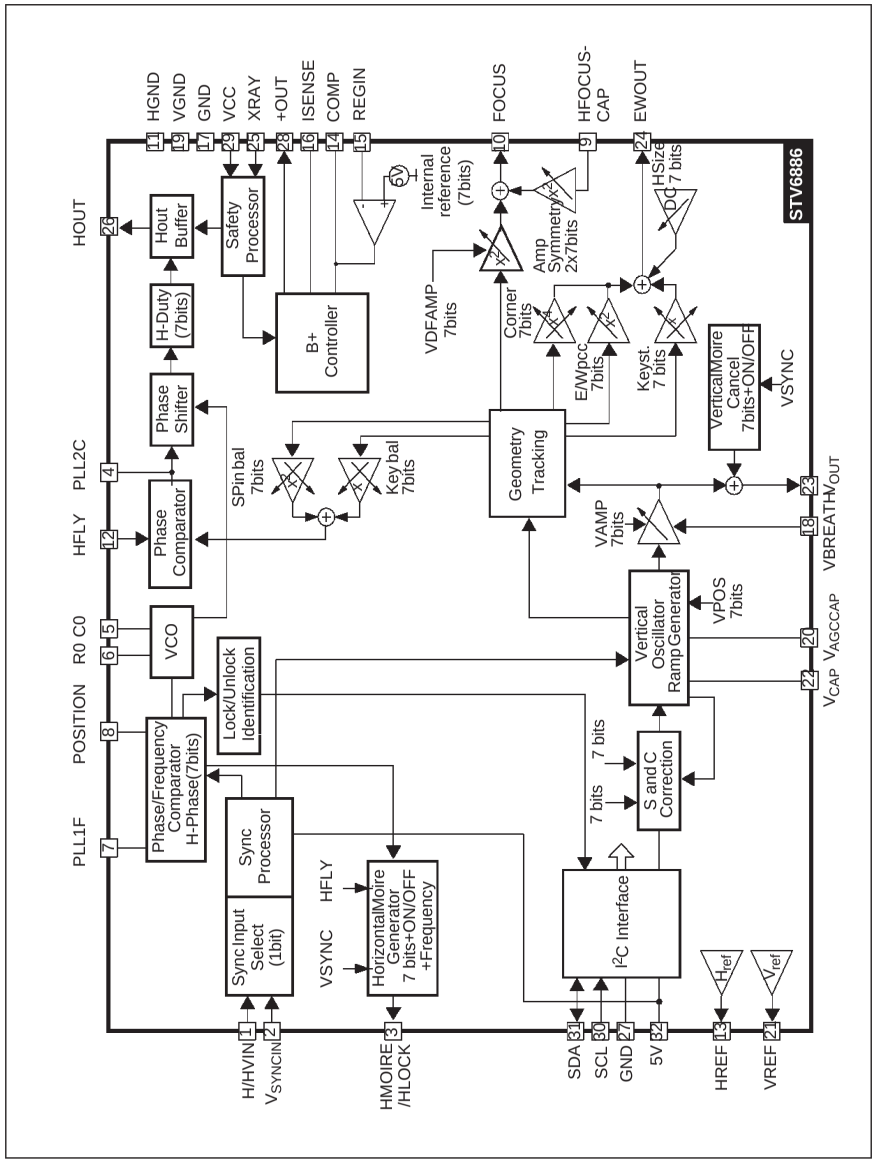
PIN CONNECTIONS

Pin	Name	Function
1	H/HVIN	TTL-compatible Horizontal sync Input (separate or composite)
2	VSYNCIN	TTL-compatible Vertical sync Input (for separated H&V)
3	HMOIRE/ HLOCK	Horizontal Moiré Output (to be connected to PLL2C through a resistor divider), HLock Output
4	PLL2C	Second PLL Loop Filter
5	C0	Horizontal Oscillator Capacitor
6	R0	Horizontal Oscillator Resistor
7	PLL1F	First PLL Loop Filter
8	HPOSITION	Horizontal Position Filter (capacitor to be connected to HGND)
9	HFOCUS-CAP	Horizontal Dynamic Focus Oscillator Capacitor
10	FOCUS OUT	Mixed Horizontal and Vertical Dynamic Focus Output
11	HGND	Horizontal Section Ground
12	HFLY	Horizontal Flyback Input (positive polarity)
13	HREF	Horizontal Section Reference Voltage (to be filtered)
14	COMP	B+ Error Amplifier Output for frequency compensation and gain setting
15	REGIN	Feedback Input of B+ control loop
16	I_{SENSE}	Sensing of external B+ switching transistor current, or switch for step-down converter
17	B+GND	Ground (related to B+ reference)
18	VBREATH	V Breathing Input Control (compensation of vertical amplitude against EHV variation)
19	VGND	Vertical Section Ground
20	VAGCCAP	Memory Capacitor for Automatic Gain Control in Vertical Ramp Generator
21	V_{REF}	Vertical Section Reference Voltage (to be filtered to pin 19)
22	VCAP	Vertical Sawtooth Generator Capacitor
23	VOUT	Vertical Ramp Output (with frequency-independent amplitude and S or C Corrections if any). It includes vertical position and vertical moiré voltages.
24	EWOUT	Pin Cushion (E/W) Correction Parabola Output
25	XRAY	X-RAY protection input (with internal latch)
26	HOUT	Horizontal Drive Output (NPN open collector)
27	GND	General Ground
28	BOUT	B+ PWM Regulator Output (NPN open collector)
29	V_{CC}	Supply Voltage(12V typ) (referenced to Pin 27)
30	SCL	I^2C Clock Input
31	SDA	I^2C Data Input
32	5V	5V Supply Voltage

QUICK REFERENCE DATA

Parameter	Value	Unit
Any polarity on H Sync & V Sync inputs	YES	
TTL or composite Syncs	YES	
Sync on Green	NO	
Horizontal Frequency	15 to 80	kHz
Horizontal Autosync Range (for given R0 and C0. Can be easily increased by application)	1 to 3.5 f0	
Control of free-running frequency	NO	
Frequency Generator for Burn-in	NO	
Control of H-Position through I^2C	YES	
Control for H-Duty Cycle through I^2C	30 to 65	%
PLL1 Inhibition Possibility	NO	
Output for Horizontal Lock/Unlock	YES	
Dual Polarity H-Drive Outputs	NO	
Vertical Frequency	35 to 150	Hz
Vertical Autosync Range (for 150nF on Pin 22 and 470nF on Pin 20)	50 to 120	Hz
Vertical S-Correction (adapted to normal or super flat tube), controlled through I^2C	YES	
Vertical C-Correction, controlled through I^2C	YES	
Control of Vertical Amplitude through I^2C	YES	
Control of Vertical Position through I^2C	YES	
Input for Vertical Amplitude compensation versus EHV	YES	
E/W Correction Output (also known as Pin Cushion Output)	YES	
Horizontal Size Adjustment through I^2C control of E/W Output DC level	YES	
Control of E/W (Pincushion) Adjustment through I^2C	YES	
Control of Keystone (Trapezoïd) Adjustment through I^2C	YES	
Control of Corner Adjustment through I^2C	YES	
Fully integrated Dynamic Horizontal Phase Control	YES	
Control of Side Pin Balance through I^2C	YES	
Control of Parallelogram through I^2C	YES	
H/V composite Dynamic Focus Output	YES	
Control of Horizontal Dynamic Focus Amplitude through I^2C	YES	
Control of Horizontal Dynamic Focus Symmetry through I^2C	YES	
Control of Vertical Dynamic Focus Amplitude through I^2C	YES	
Tracking of Geometric Corrections and of Vertical focus with Vertical Amplitude and Position	YES	
Control of Horizontal and Vertical Moiré cancellations through I^2C	YES	
Optimisation of HMoiré frequency through I^2C	YES	
B+ Regulation, adjustable through I^2C	YES	
Stand-by function, disabling H and V scanning and B+	YES	
X-Ray protection, disabling H scanning and B+	YES	
Blanking Outputs	NO	
Fast I^2C Read/Write	400	kHz
I^2C indication of the presence of Syncs (biased from 5V alone)	YES	
I^2C indication of the polarity and Type of Syncs	YES	
I^2C indication of Lock/Unlock, for both Horizontal and Vertical sections	YES	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 29)	13.5	V
V_{DD}	Supply Voltage (Pin 32)	5.7	V
V_{IN}	Max Voltage on Pin 4 Pin 9 Pin 5 Pins 6, 7, 8, 14, 15, 16, 20, 22 Pins 3, 10, 18, 23, 24, 25, 26, 28 Pins 1, 2 Pins 30, 31	4.0 5.5 6.4 8.0 V_{CC} V_{DD} 5	V V V V V V V
VESD	ESD susceptibility through 1.5kΩ Human Body Model, 100pF Discharge EIAJ Norm, 200pF Discharge through 0Ω	2 300	kV V
T_{stg}	Storage Temperature	-40, +150	°C
T_j	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	0, +70	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Max. Junction-Ambient Thermal Resistance	65	°C/W

SUPPLY AND REFERENCE VOLTAGES

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	Pin 29	10.8	12	13.2	V
V_{DD}	Supply Voltage	Pin 32	4.5	5	5.5	V
I_{CC}	Supply Current	Pin 29		50		mA
I_{DD}	Supply Current	Pin 32		5		mA
V_{REF-H}	Horizontal Reference Voltage	Pin 13, I = -2mA	7.6	8.2	8.8	V
V_{REF-V}	Vertical Reference Voltage	Pin 21, I = -2mA	7.6	8.2	8.8	V
I_{REF-H}	Max. Sourced Current on V_{REF-H}	Pin 13			5	mA
I_{REF-V}	Max. Sourced Current on V_{REF-V}	Pin 21			5	mA

I²C READ/WRITE

Electrical Characteristics (V_{DD} = 5V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I²C PROCESSOR (1)						
Fscl	Maximum Clock Frequency	Pin 30			400	kHz
Tlow	Low period of the SCL Clock	Pin 30	1.3			µs
Thigh	High period of the SCL Clock	Pin 30	0.6			µs
Vinth	SDA and SCL Input Threshold	Pins 30, 31		2.2		V
VACK	Acknowledged Output Voltage on SDA input with 3mA	Pin 31			0.4	V
I²C leak	Leakage current into SDA and SCL with no logic supply	V_{DD} = 0 Pins 30, 31 = 5 V			20	µA

Note: 1 See also I²C Bus Address Table.

SYNC PROCESSOR

Operating Conditions (V_{DD} = 5V, V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
HSVR	Voltage on H/HVIN Input	Pin 1	0		5	V
MinD	Minimum Horizontal Input Pulses Duration	Pin 1	0.7			µs
Mduty	Maximum Horizontal Input Signal Duty Cycle	Pin 1			25	%
VSVR	Voltage on VSYNCIN	Pin 2	0		5	V
VSW	Minimum Vertical Sync Pulse Width	Pin 2	5			µs
VSmD	Maximum Vertical Sync Input Duty Cycle	Pin 2			15	%
VextM	Maximum Vertical Sync Width on TTL H/Vcomposite	Pin 1			750	µs

Electrical Characteristics (V_{DD} = 5V, V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VINTH	Horizontal and Vertical Input Logic Level (Pins 1, 2)	High Level Low Level	2.2		 0.8	V V
RIN	Horizontal and Vertical Pull-Up Resistor	Pins 1, 2		250		kΩ
VoutT	Extracted Vsync Integration Time (% of T_H) on H/VComposite (2)	C0 = 820pF	26	35		%

Note: 2 T_H is the horizontal period.

HORIZONTAL SECTION

Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VCO						
I_{0max}	Max Current from Pin 6	Pin 6			1.5	mA
F(max.)	Maximum Oscillator Frequency				80	kHz
OUTPUT SECTION						
I12m	Maximum Input Peak Current	Pin 12			5	mA
HOI	Horizontal Drive Output Maximum Current	Pin 26, Sunk current			30	mA

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
1st PLL SECTION						
HpoIT	Delay Time for detecting polarity change(3)	Pin 1	0.75			ms
Vvco	VCO Control Voltage (Pin 7)	V_{REF-H} = 8.2V $f_H = f_0$ $f_{H=}f_H$ (Max.)		 1.4 4.9		 V V
Vcog	VCO Gain (Pin 7)	R_0 = 6.49kΩ, C_0 = 820pF	Tbd	15.9	Tbd	kHz/V
Hph	Horizontal Phase Adjustment (4)	% of Horizontal Period		±10		%
 Vbmi Vbtyp Vbmax	Horizontal Phase Setting Value (Pin 8)(4) Minimum Value Typical Value Maximum Value	Sub-Address 01 Byte x1111111 Byte x1000000 Byte x0000000		 2.9 3.5 4.2		 V V V
IPII1U IPII1L	PLL1 Filter Charge Current	PLL1 Unlocked PLL1 Locked		±140 ±1		µA mA
f_o	Free Running Frequency	R_0 = 6.49kΩ, C_0 = 820pF	Tbd	22.8	Tbd	kHz
dfo/dT	Free Running Frequency Thermal Drift (5)	Not including external componant drift		-150		ppm/C
CR	PLL1 Capture Range	fH(Min.) fH(Max.) (6)		f_o+0.5 3.5f_o		kHz kHz
HUnlock	DC level pin 3 when PLL1 is unlocked(7)	Sub-address 02 1xxx xxxx 0000 0000 0111 1111	6	 0.3 2.75	 3	 V V V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
2nd PLL SECTION AND HORIZONTAL OUTPUT SECTION						
FBth	Flyback Input Threshold Voltage (Pin 12)		0.65	0.75		V
Hjit	Horizontal Jitter (8)	At 31.4kHz		70		ppm
HDmin HDmax	Horizontal Drive Output Duty-Cycle (Pin 26) (9)	Sub-Address 00 Byte x1111111 Byte x0000000 (10)		 30 65		 % %
XRAYth	X-RAY Protection Input Threshold Voltage,	Pin 25, (see fig. 14)	7.6	8.2	8.8	V
Vphi2	Internal Clamping Levels on 2nd PLL Loop Filter (Pin 4)	Low Level High Level		1.6 4.2		V V
VSCinh	Inhibition threshold (The condition V_{CC} < VSCinh will stop H-Out, V-Out, B-Out and reset X-RAY)	Pin 29		7.5		V
HDvd	Horizontal Drive Output (low level)	Pin 26, I_{OUT} = 30mA			0.4	V

Note: 3 This delay is necessary to avoid a wrong detection of polarity change in the case of a composite sync.

4 See Figure 10 for explanation of reference phase.

5 These parameters are not tested on each unit. They are measured during our internal qualification.

6 A larger range may be obtained by application.

7 When at 0xxx xxxx, (HMoiré/HLock not selected), Pin 3 is a DAC with 0.3...2.75V range. When at 1xxx xxxx (HMoiré/HLock selected) and PLL1 is locked, Pin 3 provides the waveform for HMoiré. See also Moiré section.

8 Hjit = 10^6x(Standard deviation/Horizontal period).

9 Duty Cycle is the ratio between the output transistor OFF time and the period. The scanning transistor is controlled OFF when the output transistor is OFF.

10 Initial Condition for Safe Start Up.

VERTICAL SECTION

Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
R_{LOAD}	Minimum Load for less than 1% Vertical Amplitude Drift	Pin 20	65			MΩ

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VRB	Voltage at Ramp Bottom Point	Pin 22		2.1		V
VRT	Voltage at Ramp Top Point (with Sync)	Pin 22		5.1		V
VRTF	Voltage at Ramp Top Point (without Sync)	Pin 22		VRT-0.1		V
VSTD	Vertical Sawtooth Discharge Time	Pin 22, C_{22} = 150nF		70		µs
VFRF	Vertical Free Running Frequency (12)	Pin 22, C_{22} = 150nF		100		Hz
ASFR	AUTO-SYNC Frequency (13)	C_{22} = 150nF ±5%	50		120	Hz
RAFD	Ramp Amplitude Drift Versus Frequency at Maximum Vertical Amplitude (11)	C_{22} = 150nF 50Hz< f < 120Hz		200		ppm/Hz
Rlin	Ramp Linearity on Pin 22 (12)	2.5V < V_{27} < 4.5V		0.5		%
VPOS	Vertical Position Adjustment Voltage (Pin 23 - VOUT mean value)	Sub Address 06 Byte 00000000 Byte 01000000 Byte 01111111	 Tbd	 3.2 3.6 4.0	 Tbd 	 V V V
VOR	Vertical Output Voltage (peak-to-peak on Pin 23)	Sub Address 05 Byte 10000000 Byte 11000000 Byte 11111111	 Tbd	 2.15 3.0 3.9	 Tbd 	 V V V
VOI	Vertical Output Maximum Current (Pin 23)			±5		mA
dVS	Max Vertical S-Correction Amplitude (TV is the vertical period) (0xxxxxxx inhibits S-CORR 11111111 gives max S-CORR)	Sub Address 07 Byte 11111111 $\Delta V/V_{PP}$ at TV/4 $\Delta V/V_{PP}$ at 3TV/4		 -3.5 +3.5		 % %
Ccorr	Vertical C-Corr Amplitude (0xxxxxxx inhibits C-CORR)	Sub Address 08 $\Delta V/V_{PP}$ at TV/2 Byte 10000000 Byte 11000000 Byte 11111111		 -3 0 +3		 % % %
BRRANG	DC Breathing Control Range (14)	V_{18}	1		12	V
BRADj	Vertical Output Variation versus DC Breathing Control (Pin 23)	$V_{18} \geq V_{REF-V}$ 1V<V_{18}< V_{REF-V}		0 -2.5		%/V %/V

Note: 11 These parameters are not tested on each unit. They are measured during our internal qualification procedure.

Note: 12 Set Register 07 at Byte 0xxxxxxx (S correction inhibited) and Register 08 at Byte 0xxxxxxx (C correction inhibited), to obtain a vertical sawtooth with linear shape.

Note: 13 This is the frequency range for which the vertical oscillator will automatically synchronize, using a single capacitor value on Pin22 and Pin 20, and with a constant ramp amplitude.

Note: 14 When not used, the DC breathing control pin must be connected to 12V.

DYNAMIC FOCUS SECTION

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
HORIZONTAL DYNAMIC FOCUS FUNCTION (seeFigure 15 on page 28)						
HDFst	Horizontal Dynamic Focus Sawtooth Minimum Level Maximum Level	Pin 9, capacitor on HFO-CUSCAP and C0 = 820pF, T_H = 20µs		 2.2 4.9		 V V
HDFdis	Horizontal Dynamic Focus Sawtooth Discharge Width	Triggered by HDFstart		400		ns
HDFstart	Internal Phase Advance versus HFLY middle (Independent of frequency)			1		µs
HDFDC	Bottom DC Output Level	R_{LOAD} = 10kΩ, Pin 10		2.1		V
TDFHD	DC Output Voltage Thermal Drift (11)			200		ppm/C
HDFamp	Horizontal Dynamic Focus Amplitude Max Byte Typ Byte Max Byte	Sub-Address 03, Pin 10, fH = 50kHz, Symmetric Wave Form x1111111 x1000000 x0000000		 1 1.5 3.5		 V_{PP} V_{PP} V_{PP}
HDFKeyst	Horizontal Dynamic FocusSymmetry (For time reference, see Figure 15) Max Phase Advance Max Phase Delay	Subaddress 04 x1111111 (decimal 127) x0000000 (decimal 0)		 16 16		 % %
VERTICAL DYNAMIC FOCUS FUNCTION (see Figure 1)						
AMPVDF	Vertical Dynamic Focus Parabola (added to horizontal) Amplitude with VAMP and VPOS Typical	Sub-Address 0F Min Byte x0000000 Typ Byte x1000000 Max Byte x1111111		 0 0.5 1		 V_{PP} V_{PP} V_{PP}
VDFAMP	Parabola Amplitude Function of VAMP (tracking between VAMP and VDF) with VPOS Typ. (see Figure 1 on page 15, and (15))	Sub-Address 05 Byte x0000000 Byte x1000000 Byte x1111111		 0.6 1 1.5		 V_{PP} V_{PP} V_{PP}
VHDFKeyt	Parabola Asymmetry Function of VPOS Control (tracking between VPOS and VDF) with VAMP Max. B/A Ratio A/B Ratio	Sub-Address 06 Byte x0000000 Byte x1111111		 0.52 0.52		

Note: 15 S and C correction are inhibited to obtain a linear vertical sawtooth.

GEOMETRY CONTROL SECTION

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
SYMMETRIC CONTROL THROUGH E/W OUTPUT (see Figure 2 on page 15 and Figure 4 on page 15)						
VEWM	Maximum E/W Output Voltage	Pin 24			6.5	V
VEWm	Minimum E/W Output Voltage	Pin 24	1.8			V
EW_{DC}	For control of Horizontal size. DC Output Voltage with: -E/W Corner inhibited -Keystone inhibited	Pin 24, see Figure 2 Subaddress 11 Byte x0000000 Byte x1000000 Byte x1111111		 2 3.25 4.2		 V V V
$TDEW_{DC}$	DC Output Voltage Thermal Drift	See (16)		100		ppm/C
EWpara	Parabola Amplitude with: -VAMP max, -VPOS typ., -Keystone and Corner inhibited	Subaddress 0A Byte 11111111 Byte 11000000 Byte 10000000		 1.4 0.7 0		 V_{PP} V_{PP} V_{PP}
EWtrack	Parabola Amplitude Function of VAMP Control (tracking between VAMP & E/W): -VPOS typ. -E/W Amplitude, Corner & Keystone inhibited (17)	Subaddress 05 Byte 10000000 Byte 11000000 Byte 11111111		 0.2 0.4 0.7		 V_{PP} V_{PP} V_{PP}
KeyAdj	Keystone Adjustment Capability with: -VPOS typ. -E/W inhibited, -Corner inhibited -Vert. Amplitude max (see (17) and Figure 4)	 Subaddress 09 Byte 10000000 Byte 11111111		 0.4 0.4		 V_{PP} V_{PP}
EW Corner	Corner Adjustment Capability with: -VPOS typ, -E/W inhibited -Keystone inhibited -Vertical Amplitude max.	Subaddress 10 Byte 11111111 Byte 11000000 Byte 10000000		 +1.25 0 –1.25		 V_{PP} V_{PP} V_{PP}
KeyTrack	Intrinsic Keystone Function of VPOS Control (tracking between VPOS & E/W): - E/W Amplitude -Vertical Amplitude max -Corner inhibited B/A Ratio A/B Ratio	Subaddress 06 Byte 00000000 Byte 01111111		 0.52 0.52		

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
ASYMMETRIC CONTROL THROUGH INTERNAL DYNAMIC HORIZONTAL PHASE MODULATION (see Figure 3)						
SPBpara	Side Pin Balance Parabola Amplitude (Figure 3) with : -VAMP max., -VPOS typ. -Parallelogram inhibited (17 & 18)	Subaddress 0D Byte 11111111 Byte 10000000		 +2.8 -2.8		 %T_H %T_H
SPBtrack	Side Pin Balance Parabola Amplitude function of VAMP Control (tracking between VAMP and SPB) with: -SPB max., -VPOS typ. -Parallelogram inhibited (17 & 18)	Subaddress 05 Byte 10000000 Byte 11000000 Byte 11111111		 1 1.8 2.8		 %T_H %T_H %T_H
ParAdj	Parallelogram Adjustment Capability with: -VAMP max., -VPOS typ. -SPB inhibited (17 & 18)	Subaddress 0E Byte 11111111 Byte 11000000		 +2.8 -2.8		 %T_H %T_H
Partrack	Intrinsic Parallelogram Function of VPOS Control (tracking between VPOS and DHPC) with : -VAMP max., -SPB max. -Parallelogram inhibited (17 & 18) B/A Ratio A/B Ratio	Subaddress 06 Byte x0000000 Byte x1111111		 0.52 0.52		

Note: 16 These parameters are not tested on each unit. They are measured during our internal qualification procedure.

Note: 17 With Register 07 at Byte 0xxxxxxx (S correction inhibited) and Register 08 at Byte 0xxxxxxx (C correction inhibited), the sawtooth has a linear shape.

MOIRE CANCELLATION SECTION

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
HORIZONTAL AND VERTICAL MOIRE						
R_{MOIRE}	Minimum Output Resistor to GND	Pin 3	4.7			kΩ
DacOut	DC Voltage pin 3 DAC configuration	R_{MOIRE} = 4.7kΩ sub-address 02 Byte 00000000 Byte 01000000 Byte 01111111		 0.3 1.1 2.75	 3	 V V V
HMOIRE	Moiré pulse (See also Hunlock in 1st PLL section) H Frequency: Locked	R_{MOIRE} = 4.7kΩ Sub-address 02 Byte 10000000 Byte 11000000 Byte 11111111		 0 0.8 2.2		 V_{PP} V_{PP} V_{PP}
T_{HMOIRE}	Preferred Scanning/EHT structure	Sub-address II: 0xxx xxxx 1xxx xxxx		Separate Combined		
VMOIRE	Vertical Moiré (measured on VOUT: Pin 23)	Sub-address 0C Byte 11111111		 3		 mV

Note: 18 T_H is the horizontal period.

B+ SECTION

Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
FeedRes	Minimum Feedback Resistor	Resistor between Pins 15 and 14	5			kΩ

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
OLG	Error Amplifier Open Loop Gain	At low frequency (19)		85		dB
UGBW	Unity Gain Bandwidth	See (19)		6		MHz
IRI	Feedback Input Bias Current	Current sourced by Pin 15 (PNP base)		0.2		µA
EAOI	Error Amplifier Output Current	Current sourced by Pin 14 Current sunk by Pin 14 (20)	 2	1.4		mA mA
CSG	Current Sense Input Voltage Gain	Pin 16		3		
MCEth	Max Current Sense Input Threshold Voltage	Pin 16		1.3		V
ISI	Current Sense Input Bias Current	Current sunk by Pin 16 (PNP base)		1		µA
Tonmax	Maximum ON Time of the external power transistor	% of horizontal period, f_o = 27kHz) (21)		100		%
B+OSV	B+Output Saturation Voltage	V_{28} with I_{28} = 10mA		0.25		V
IV_{REF}	Internal Reference Voltage	On error amp (+) input Subaddress OB: Byte 1000000		5		V
V_{REFADJ}	Internal Reference Voltage Adjustment Range	Byte 01111111 Byte 00000000		+20 -20		% %
PWMSEL	Threshold for step-up/step-down selection (step-up configuration if V_{16} < PWMSEL)	Pin 16		6		V
t_{FB+}	Fall Time	Pin 28		100		ns

Note: 19 These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches coming from corners of our process and also temperature characterization.

Note: 20 To make soft start possible, 0.5mA are sunk when B+ is disabled.

Note: 21 The external power transistor is OFF during 400ns of the HFOCUSCAP discharge

Figure 1. Vertical Dynamic Focus Function

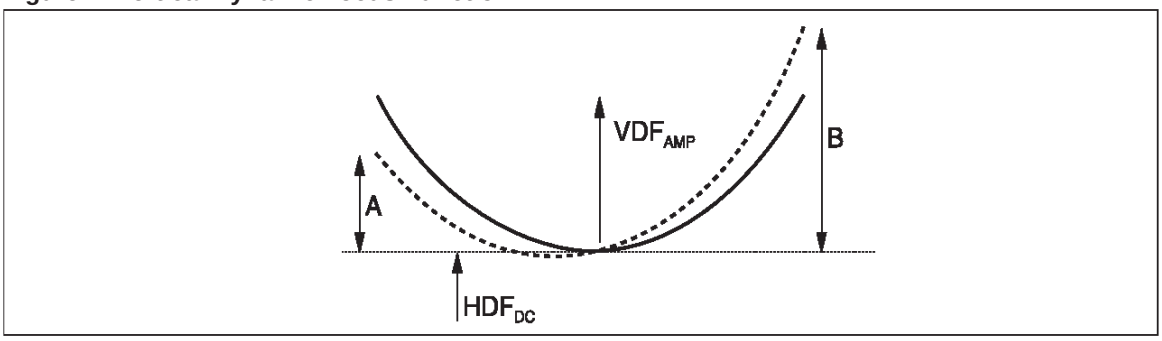


Figure 2. E/W Output

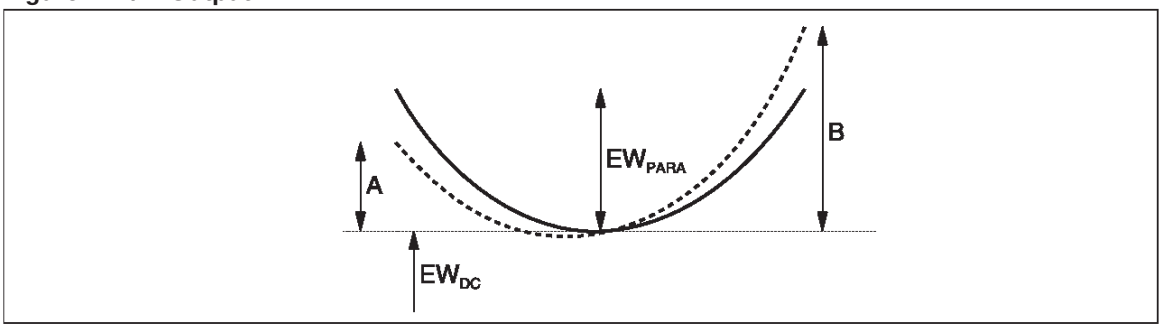


Figure 3. Dynamic Horizontal Phase Control

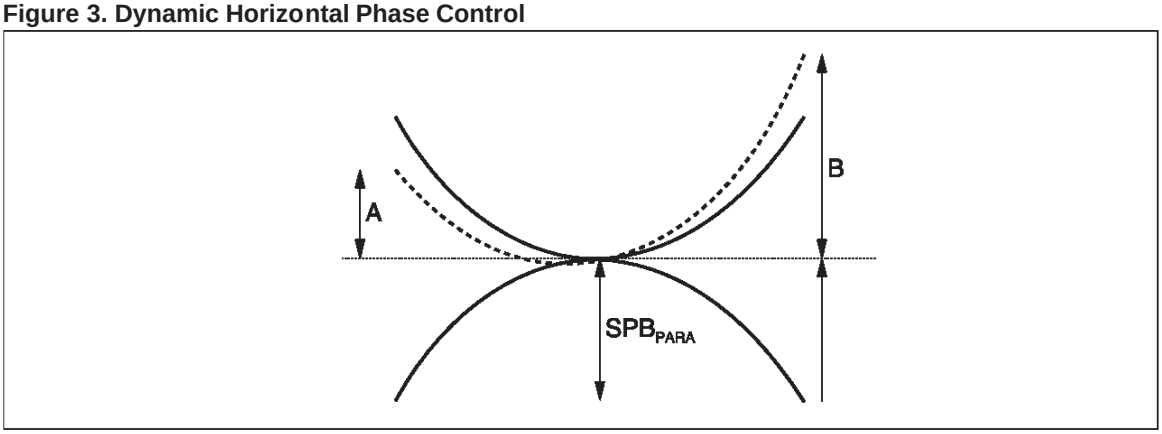
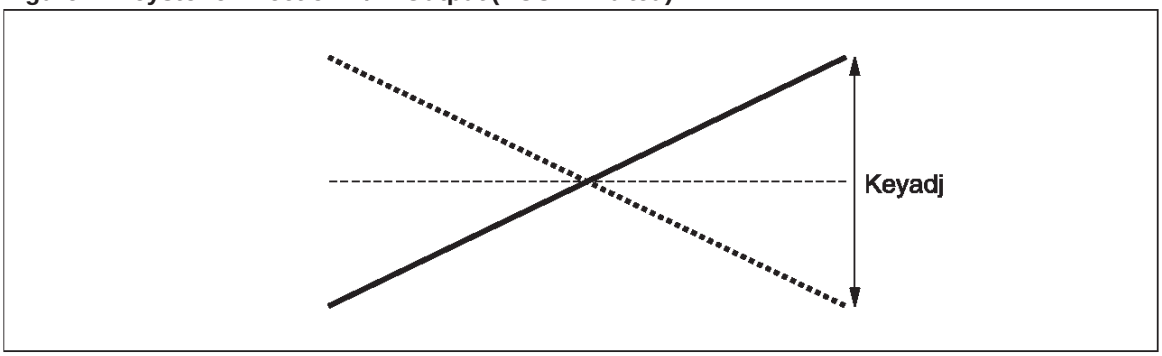
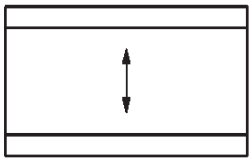
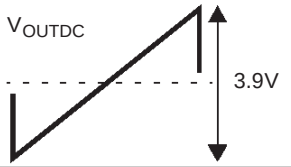
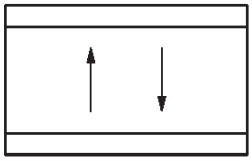
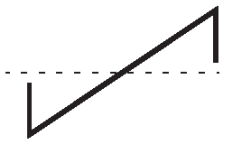
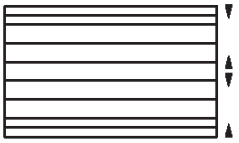
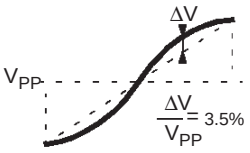
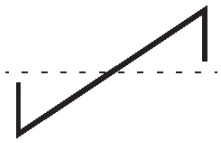
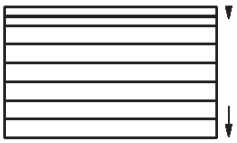
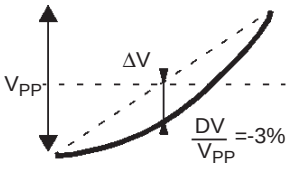
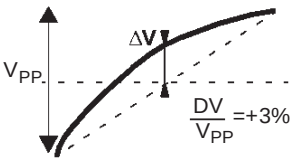
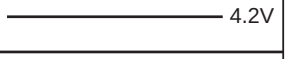
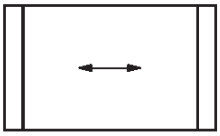
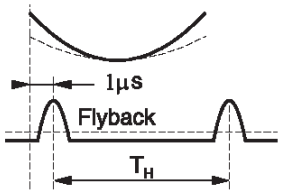
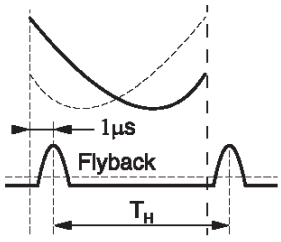


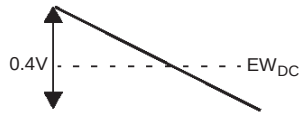
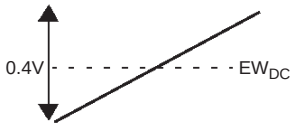
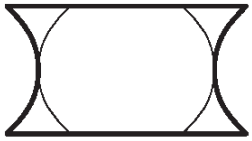
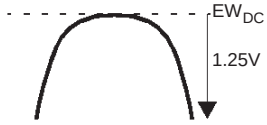
Figure 4. Keystone Effect on E/W Output (PCC Inhibited)

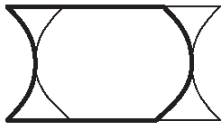
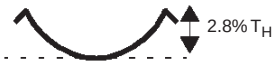
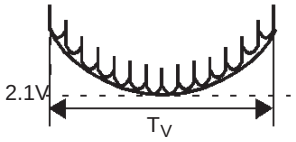
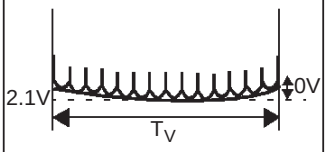


TYPICAL OUTPUT WAVEFORMS

Function	Sub Address	Pin	Byte	Specification	Effect on Screen
Vertical Size	05	23	10000000		
			11111111		
Vertical Position DC Control	06	23	00000000	V_{OUTDC} = 3.2V	
			01000000	V_{OUTDC} = 3.6V	
			01111111	V_{OUTDC} = 4.0V	
Vertical S Linearity	07	23	0xxxxxxx: Inhibited		
			11111111		

Function	Sub Address	Pin	Byte	Specification	Effect on Screen
Vertical C Linearity	08	23	0xxxxxxx : Inhibited		
			10000000		
			11111111		
Horizontal Size	11	24	x1111111		
			x0000000		
Horizontal Dynamic Focus with: Amplitude	03	10	X000 0000 — X111 1111 ---		
Horizontal Dynamic Focus with: Symmetry	04	10	X000 0000 — X111 1111 ---		

Function	Sub Address	Pin	Byte	Specification	Effect on Screen
Keystone (Trapezoid) Control	09	24	(E/W + Corner Inhibited)		
			10000000		
			11111111		
E/W (Pin Cushion) Control	0A	24	(Keystone + Corner Inhibited)		
			10000000		
			11111111		
Corner Control	10	24	(Keystone+ E/W Inhibited)		
			11111111		
			10000000		
Parallel-ogram Control	0E	Internal	(SPB Inhibited)		
			10000000		
			11111111		

Function	Sub Address	Pin	Byte	Specification	Effect on Screen
Side Pin Balance Control	0D		(Parallelogram Inhibited)		
			10000000		
			11111111		
Vertical Dynamic Focus with Horizontal	0F	10	X111 1111		
			X000 0000		

I²C BUS ADDRESS TABLE

Slave Address (8C): Write Mode

Sub Address Definition

	D8	D7	D6	D5	D4	D3	D2	D1	
0	0	0	0	0	0	0	0	0	Horizontal Drive Selection/Horizontal Duty Cycle
1	0	0	0	0	0	0	0	1	X-ray Reset/Horizontal Position
2	0	0	0	0	0	0	1	0	Horizontal Moiré/H Lock
3	0	0	0	0	0	0	1	1	Sync. Priority/Horizontal Focus Amplitude
4	0	0	0	0	0	1	0	0	Refresh/Horizontal Focus Symmetry
5	0	0	0	0	0	1	0	1	Vertical Ramp Amplitude
6	0	0	0	0	0	1	1	0	Vertical Position Adjustment
7	0	0	0	0	0	1	1	1	S Correction
8	0	0	0	0	1	0	0	0	C Correction
9	0	0	0	0	1	0	0	1	E/W Keystone
A	0	0	0	0	1	0	1	0	E/W Amplitude
B	0	0	0	0	1	0	1	1	B+ Reference Adjustment
C	0	0	0	0	1	0	0	0	Vertical Moiré
D	0	0	0	0	1	0	0	1	Side Pin Balance
E	0	0	0	0	1	0	1	0	Parallelogram
F	0	0	0	0	1	0	1	1	Vertical Dynamic Focus Amplitude
10	0	0	0	1	0	0	0	0	E/W Corner
11	0	0	0	1	0	0	0	1	H. Moiré Frequency/Horizontal Size Amplitude

Slave Address (8D): Read Mode: No sub address needed.

I²C BUS ADDRESS TABLE (continued)

	D8	D7	D6	D5	D4	D3	D2	D1
WRITE MODE								
00	HDrive 0, off [1], on	**Horizontal Duty Cycle**						
		[0]	[0]	[0]	[0]	[0]	[0]	[0]
01	Xray 1, reset [0]	**Horizontal Phase Adjustment**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
02	HMoiré/HLock 1, on [0], off	**Horizontal Moiré Amplitude**						
		[0]	[0]	[0]	[0]	[0]	[0]	[0]
03	Sync 0, Comp [1], Sep	**Horizontal Focus Amplitude**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
04	Detect Refresh [0], off	**Horizontal Focus Symmetry**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
05	Vramp 0, off [1], on	**Vertical Ramp Amplitude Adjustment**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
06	Test V 1, on [0], off	**Vertical Position Adjustment**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
07	S Select 1, on [0]	**S Correction**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
08	C Select 1, on [0]	**C Correction**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
09	E/W Key 0, off [1]	**E/W Keystone**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0A	E/W Sel 0, off [1]	**E/W Amplitude**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0B	Test H 1, on [0], off	**B + Reference Adjustment**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0C	V. Moiré 1, on [0]	**Vertical Moiré Amplitude**						
		[0]	[0]	[0]	[0]	[0]	[0]	[0]
0D	SPB Sel 0, off [1]	**Side Pin Balance**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0E	Parallelo 0, off [1]	**Parallelogram**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]

	D8	D7	D6	D5	D4	D3	D2	D1
0F	Eq. Pulse 1, ignore $T_H/2$ [0], accept all	**Vertical Dynamic Focus Amplitude**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
10	Corner Sel 1, on [0], off	**E/W Corner**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
11	H. Moiré suited to 1 Combined [0] Separate scanning/EHT	**Horizontal Size Amplitude**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
READ MODE								
	Hlock 0, on [1], no	Vlock 0, on [1], no	Xray 1, on [0], off	Polarity Detection		Sync Detection		
				H/V pol [1], negative	V pol [1], negative	Vext det [0], no det	H/V det [0], no det	V det [0], no det

[x] at Power-on Reset value
Data is transferred with vertical sawtooth retrace.
We recommend setting the unspecified bits to [0] in order to ensure compatibility with future devices.

OPERATING DESCRIPTION

1 GENERAL CONSIDERATIONS

1.1 Power Supply

The typical values of the power supply voltages V_{CC} and V_{DD} are 12 V and 5 V respectively. Optimum operation is obtained for V_{CC} between 10.8 and 13.2 V and V_{DD} between 4.5 and 5.5 V.

In order to avoid erratic operation of the circuit during the transient phase of VCC switching on, or off, the value of V_{CC} is monitored: if V_{CC} is less than 7.5 V typ., the outputs of the circuit are inhibited.

Similarly, before V_{DD} reaches 4 V, all the I^2C register are reset to their default value (see I^2C Bus Address Table).

In order to have very good power supply rejection, the circuit is internally supplied by several voltage references (typ. value: 8.2 V). Two of these voltage references are externally accessible, one for the vertical and one for the horizontal part. They can be used to bias external circuitry (if I_{LOAD} is less than 5 mA). It is necessary to filter the voltage references by external capacitors connected to the respective grounds, in order to minimize the noise and consequently the “jitter” on vertical and horizontal output signals.

1.2 I^2C Control

STV6886 belongs to the I^2C-controlled device family. Instead of being controlled by DC voltages on dedicated control pins, each adjustment can be done via the I^2C Interface.

The I^2C bus is a serial bus with a clock and a data input. The general function and the bus protocol are specified in the Philips-bus data sheets.

The inputs (Data and Clock) are comparators with a 2.2 V threshold at 5 V supply. Spikes of up to 50 ns are filtered by an integrator and the maximum clock speed is limited to 400 kHz.

The data line (SDA) can receive or transmit data. In read-mode the IC sends reply information (1 byte) to the micro-processor.

The bus protocol prescribes a full-byte transmission in all cases. The first byte after the start condition is used to transmit the IC-address (hexa 8C for write, 8D for read).

1.3 Write Mode

In write mode the second byte is the subaddress of the selected function to adjust (or controls to affect) and the third byte the corresponding data byte. It is possible to send more than one data byte to the IC. If after the third byte no stop or start condition is detected, the circuit increments automatically by one the momentary subaddress in the subaddress counter (auto-increment mode). So it is possible to transmit immediately the following data bytes without sending the IC address or subaddress. This can be useful to reinitialize all the controls very quickly (flash manner). This procedure can be finished by a stop condition.

The circuit has 18 adjustment capabilities: 3 for the horizontal part, 4 for the vertical, 3 for the E/W correction, 2 for the dynamic horizontal phase control, 2 for the vertical and horizontal Moiré options, 3 for the horizontal and the vertical dynamic focus and 1 for the B+ reference adjustment.

18 bits are also dedicated to several controls (ON/OFF, Horizontal Forced Frequency, Sync Priority, Detection Refresh and XRAY reset).

1.4 Read Mode

During the read mode the second byte transmits the reply information.

The reply byte contains the horizontal and vertical lock/unlock status, the XRAY activation status, and the horizontal and vertical polarity detection. It also contains the sync detection status which is used by the MCU to assign the sync priority. A stop condition always stops all the activities of the bus decoder and switches to high impedance both the data and clock line (SDA and SCL).

See I^2C Bus Address Table.

1.5 Sync Processor

The internal sync processor allows the STV6886 to accept:

– separated horizontal & vertical TTL-compatible sync signal

– composite horizontal & vertical TTL-compatible sync signal

1.6 Sync Identification Status

The MCU can read (address read mode: 8D) the status register via the I^2C bus, and then select the sync priority depending on this status.

Among other data this register indicates the presence of sync pulses on H/HVIN, VSYNCIN and (when 12 V is supplied) whether a Vext has been extracted from H/HVIN. Both horizontal and vertical sync are detected even if only 5 V is supplied.

In order to choose the right sync priority the MCU may proceed as follows (see I²C Bus Address Table):

– refresh the status register,

– wait at least for 20ms (Max. vertical period),

– read the status register.

Sync priority choice should be :

Vextdet	H/V det	V det	Sync priority Subaddress 03 (D8)	Comment Sync type
No	Yes	Yes	1	Separated H&V
Yes	Yes	No	0	Composite TTL H&V

Of course, when the choice is made, we can refresh the sync detections and verify that the extracted Vsync is present and that no sync type change has occurred. The sync processor also gives sync polarity information.

1.7 IC status

The IC can inform the MCU about the 1st horizontal PLL and vertical section status (locked or not) and about the XRAY protection (activated or not).Resetting the XRAY internal latch can be done either by decreasing the V_{CC} supply or directly resetting it via the I²C interface.

1.8 Sync Inputs

Both H/HVIN and VSYNCIN inputs are TTL compatible triggers with hysteresis to avoid erratic detection. Both inputs include a pull up resistor connected to V_{DD}.

1.9 Sync Processor Output

The sync processor indicates on bit D8 of the status register whether 1st PLL is locked to an incoming horizontal sync. Its level goes to low when locked. This information is also available on pin 3 if sub-address 02 D8 is equal to 1. When PLL1 is unlocked, pin 3 output voltage becomes higher than 6V. When it is locked, the HMoiré waveform is available on pin 3 (max voltage: 3V).

2 HORIZONTAL PART

2.1 Internal Input Conditions

A digital signal (horizontal sync pulse or TTL composite) is sent by the sync processor to the horizontal input. It may be positive or negative (see Figure 5).

Using internal integration, both signals are recognized if Z/T < 25%. Synchronization takes place on the leading edge of the internal sync signal.

The minimum value of Z is 0.7 µs.

Another integration is able to extract the vertical pulse from composite sync if the duty cycle is higher than 25% (typically d = 35%),
(see Figure 6).

Figure 5.

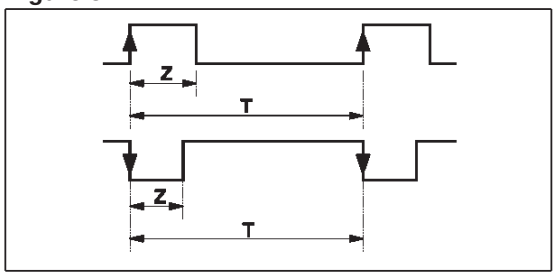
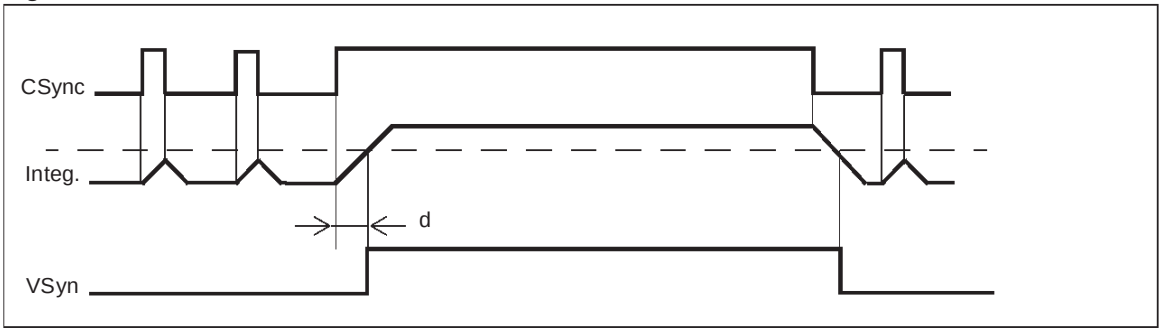


Figure 6.

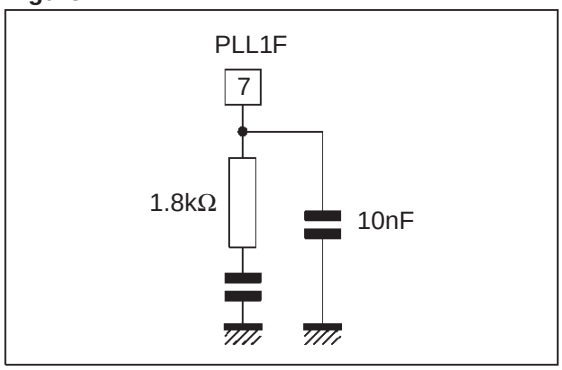


The last feature performed is the removal of these equalization pulses which fall in the middle of a line, to avoid parasitic pulses on the phase comparator (which would be disturbed by missing or extraneous pulses). This last feature is switched on/off by sub-address 0F D8. By default [0], equalization pulses will not be removed.

2.2 PLL1

The PLL1 consists of a phase comparator, an external filter and a voltage-controlled oscillator (VCO).The phase comparator is a “phase/frequency” type designed in CMOS technology. This kind of phase detector avoids locking on wrong frequencies. It is followed by a “charge pump”, composed of two current sources : sunk and sourced (typically I =1 mA when locked and I = 140 µA when unlocked). This difference between lock/unlock allows smooth catching of the horizontal frequency by PLL1. This effect is reinforced by an internal original slow down system when PLL1 is locked, avoiding the horizontal frequency changing too quickly. The dynamic behavior of PLL1 is fixed by an external filter which integrates the current of the charge pump. A “CRC” filter is generally used (see Figure 7 on page 25).

Figure 7.



The PLL1 is internally inhibited during extracted vertical sync (if any) to avoid taking in account missing pulses or wrong pulses on phase comparator. Inhibition is obtained by stopping high and low signals at the input of the charge pump block (see Figure 8 on page 25).

Figure 8.

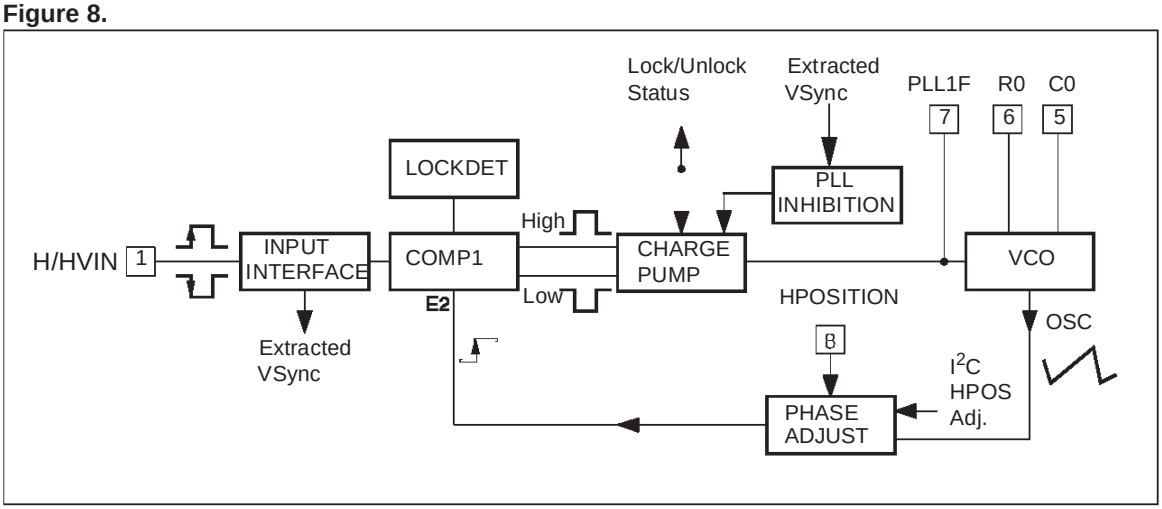
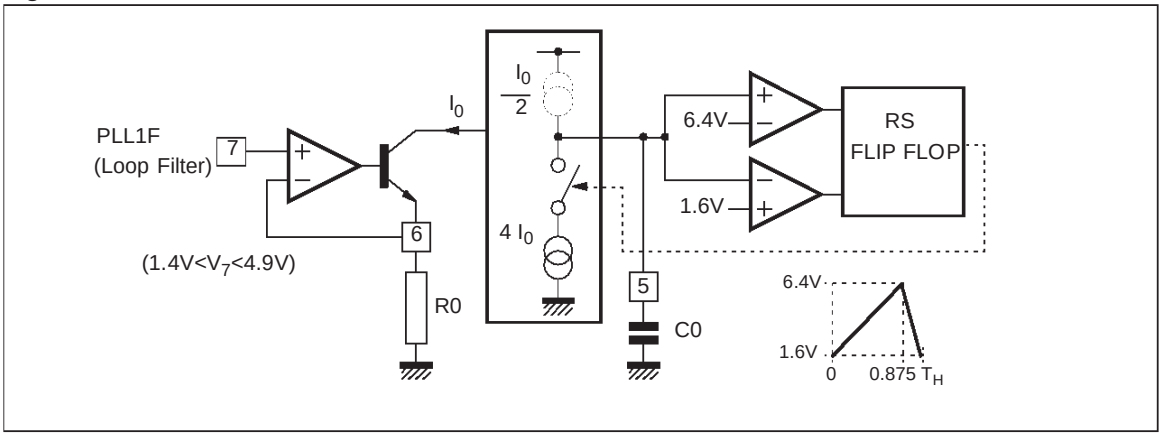


Figure 9.



The VCO uses an external RC network. It delivers a linear sawtooth obtained by the charge and the discharge of the capacitor, with a current proportional to the current in the resistor. The typical thresholds of the sawtooth are 1.6 V and 6.4 V.

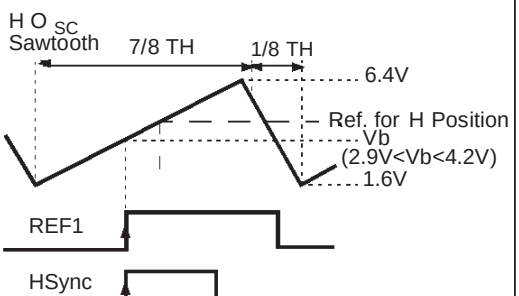
The control voltage of the VCO is between 1.4 V and 4.9 V (see Figure 9). The theoretical frequency range of this VCO is in the ratio of 1 to 3.5. The effective frequency range has to be smaller due to clamp intervention on the filter lowest value.

The sync frequency must always be higher than the free running frequency. For example, when using a sync range between 25 kHz and 80 kHz, the suggested free running frequency is 22 kHz.

PLL1 ensures the coincidence between the leading edge of the sync signal and a phase reference REF1 obtained by comparison between the sawtooth of the VCO and an internal DC voltage Vb. Vb is I^2C adjustable between 2.9 V and 4.2 V (corresponding to ±10 %) (see Figure 10).

The STV6886 also includes a Lock/Unlock identification block which senses in real time whether PLL1 is locked or not on the incoming horizontal sync signal. This information is available through I^2C, and also on pin 3 if HLock/Unlock option has been set through Subaddress 02,D8.

Figure 10. PLL1 Timing Diagram

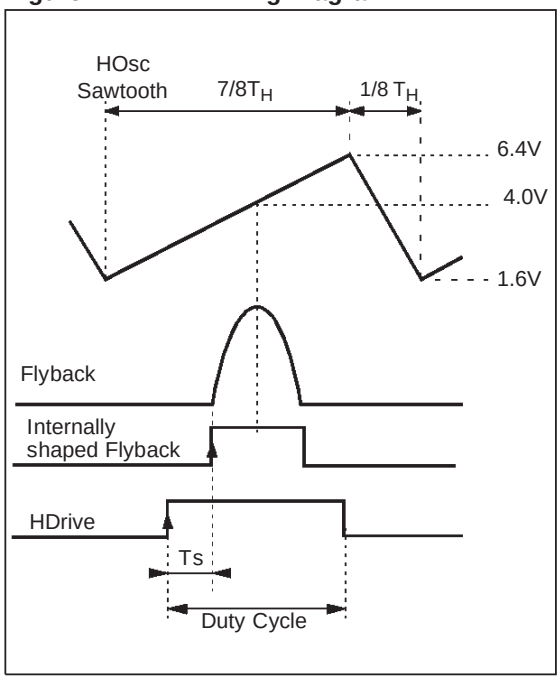


Phase REF1 is obtained by comparison between the sawtooth and a DC voltage adjustable between 2.9 V and 4.2 V.
The PLL1 ensures the exact coincidence between the signal phase REF and HSYNC. A ±10% T_H phase adjustment is possible around the 3.5V point.

2.3 PLL2

PLL2 ensures a constant position of the shaped flyback signal in comparison with the sawtooth of the VCO, taking into account the saturation time Ts (see Figure 11 on page 26)

Figure 11. PLL2 Timing Diagram

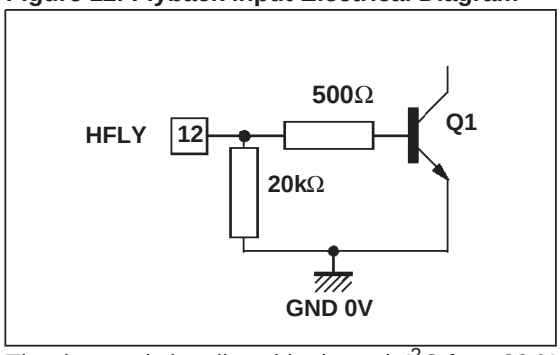


The phase comparator of PLL2 is followed by a charge pump (typical output current: 0.5 mA).

The flyback input consists of an NPN transistor.

The input current must be limited to less than 5 mA (see Figure 12).

Figure 12. Flyback Input Electrical Diagram



The duty cycle is adjustable through I^2C from 30 % to 65 %. For a safe start-up operation, the initial duty cycle (after power-on reset) is 65% in order to avoid having too long a conduction period of the horizontal scanning transistor.

The maximum storage time (Ts Max.) is ($0.44T_H$-$T_{FLY}/2$). Typically, T_{FLY}/T_H is around 20 %, at maximum frequency, which means that Ts max is around 34 % of T_H.

2.4 Output Section

The H-drive signal is sent to the output through a shaping stage which also controls the H-drive duty cycle (I^2C adjustable) (see Figure 11). In order to secure the scanning power part operation, the output is inhibited in the following cases:

– when V_{CC} or V_{DD} are too low

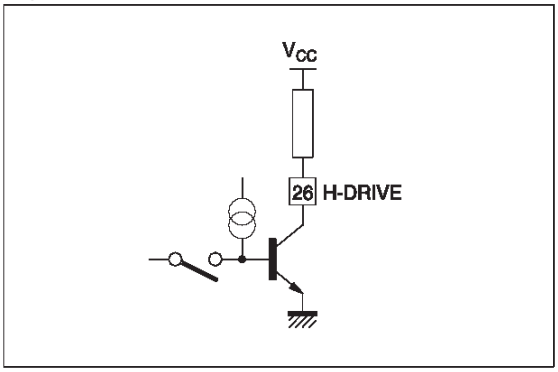
– when the XRAY protection is activated

– during the Horizontal flyback

– when the HDrive I^2C bit control is off.

The output stage consists of a NPN bipolar transistor. Only the collector is accessible (see Figure 13).

Figure 13.



This output stage is intended for “reverse” base control, where setting the output NPN in off-state will control the power scanning transistor in off-state.

The maximum output current is 30mA, and the corresponding voltage drop of the output V_{CEsat} is 0.4V Max.

Obviously the power scanning transistor cannot be directly driven by the integrated circuit. An interface has to be added between the circuit and the power transistor either of bipolar or MOS type.

2.5 X-RAY Protection

The X-Ray protection is activated by application of a high level on the X-Ray input (more than 8.2V on Pin 25). It inhibits the H-Drive and B+ outputs.

This activation is internally delayed by 2 lines to avoid erratic detection when short parasitics are present .

This protection is latched; it may be reset either by V_{CC} switch-off or by I^2C (see Figure 14 on page 28).

2.6 Horizontal and Vertical Dynamic Focus

For dynamic focus adjustment, the STV6886 delivers the sum of two signals on pin 10:

– a parabolic waveform at horizontal frequency,

– a parabolic waveform at vertical frequency.

The horizontal parabola comes from a sawtooth in phase advance with flyback pulse middle. The phase advance versus horizontal flyback middle is kept constant versus frequency (about 1µs). Symmetry and amplitude are I^2C adjustable (see Figure 15 on page 28).

The vertical parabola is tracked with VPOS and VAMP. Its amplitude can be adjusted. It is also affected by S and C corrections.

This positive signal once amplified is to be sent to the CRT focusing grids.

Because the DC/DC converter is triggered by the HFocus sawtooth, it is recommended to connect a capacitor to pin 9, even if HFocus is not needed. The capacitor value is critical only if Focus is used.

Figure 14. Safety Functions Block Diagram

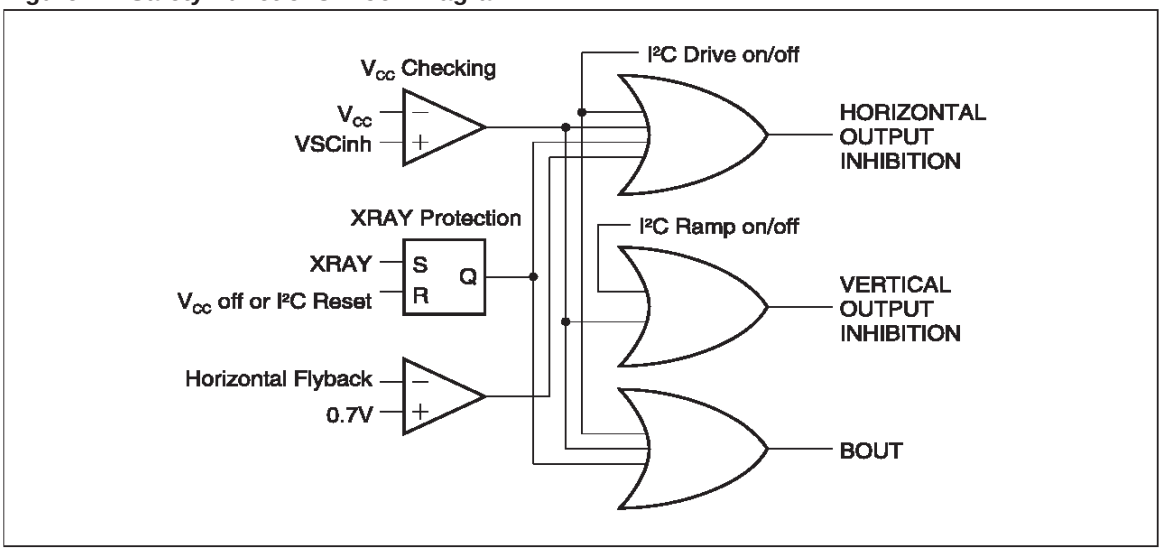
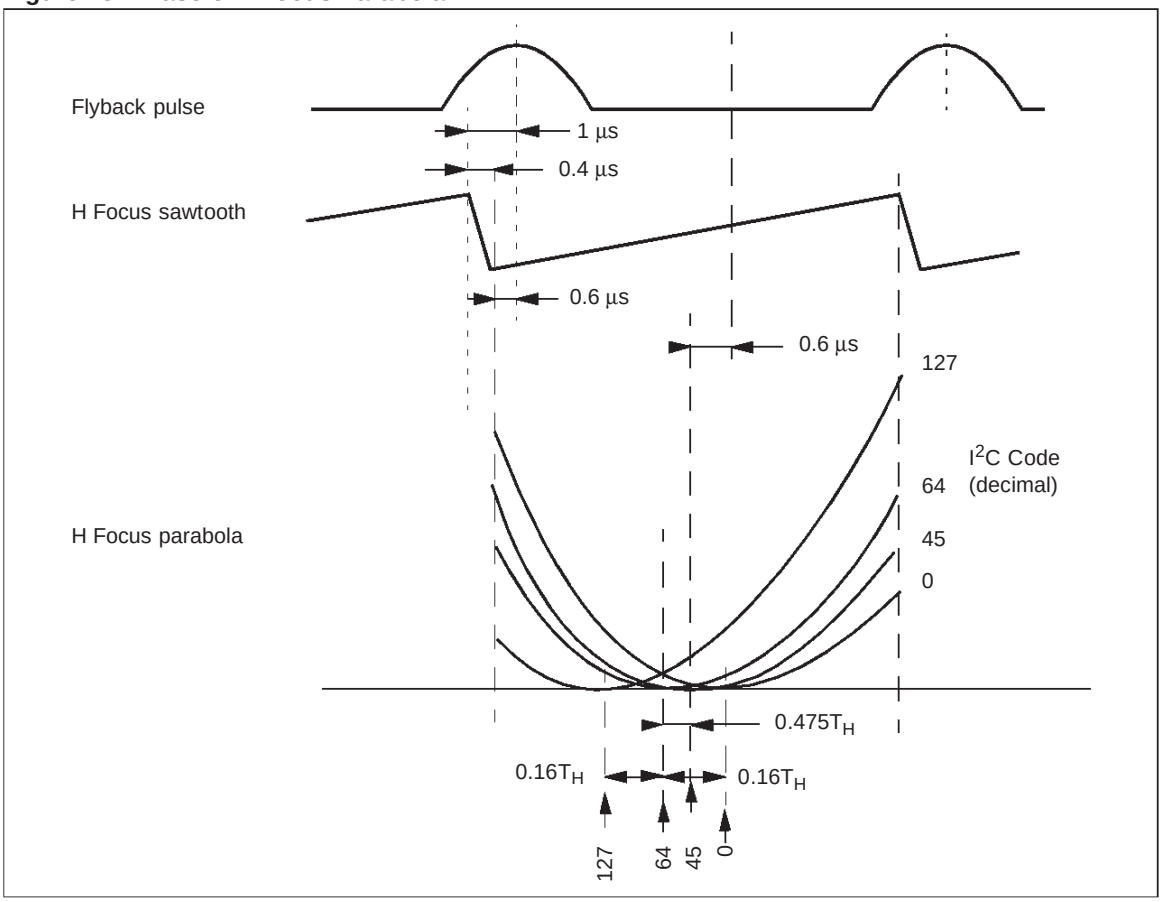


Figure 15. Phase of HFocus Parabola



2.7 Horizontal Moiré Output

The Horizontal Moiré output is intended to correct a beat between the horizontal video pixel period and the CRT pixel width.

The Moiré signal is a combination of the horizontal and vertical frequency signals.

To achieve a Moiré cancellation, the Moiré output has to be connected so as to modulate the horizontal position. We recommend introducing this "Horizontal Controlled Jitter" on the ground side of PLL2 capacitor where this "controlled jitter" will directly affect the horizontal position.

The amplitude of the signal is I^2C adjustable. The H-Moiré frequency can be chosen via the I^2C.

If H Scanning and EHT are separated, bit D8 in subaddress 11 should be set to 0. If H Scanning and EHT are combined, setting this bit to 1 will provide a better screen aspect.

The H-Moiré output is combined with the PLL1 horizontal unlock output.

If HMoiré/HLock is selected (bit 02D8 to 1):

– when PLL1 is unlocked, pin 3 output voltage goes above 6V.

– when PLL1 is locked, the HMoiré signal (up to 2.2V peak) is present on pin 3.

If HMoiré/HLock is not selected, pin 3 can be used as a 0....2.5V DAC.

3 VERTICAL PART

3.1 Function

When the synchronization pulse is not present, an internal current source sets the free-running frequency. For an external capacitor C_{OSC} = 150nF, the typical free running frequency is 100Hz.

The typical free running frequency can be calculated by:

$$fo(Hz) = 1.5 \cdot 10^{-5} \cdot \frac{1}{C_{OSC}}$$

A negative or positive TTL level pulse applied on Pin 2 (VSYNC) as well as a TTL composite sync on Pin 1 can synchronize the ramp in the range [fmin, fmax] (See Figure 16 on page 30). This frequency range depends on the external capacitor connected on Pin 22. A 150nF (± 5%) capacitor is recommended for 50Hz to 120Hz applications.

If a synchronization pulse is applied, the internal oscillator is synchronized immediately but with wrong amplitude. An internal correction then adjusts it in less than half a second. The top value of the ramp (Pin 22) is sampled on the AGC capacitor (Pin 20) at each clock pulse and a transconductance amplifier modifies the charge current of the capacitor so as to adjust the amplitude to the right value.

The Read Status register provides the vertical Lock-Unlock and the vertical sync polarity information.

We recommend to use an AGC capacitor with low leakage current. A value lower than 100nA is mandatory.

A good stability of the internal closed loop is reached with a 470nF ± 5% capacitor value on Pin 20 (VAGC).

3.2 I^2C Control Adjustments

S and C correction shapes can then be added to this ramp. These frequency-independent S and C corrections are generated internally. Their amplitudes are adjustable by their respective I^2C registers. They can also be inhibited by their select bits.

Finally, the amplitude of this S and C corrected ramp can be adjusted by the vertical ramp amplitude control register.

The adjusted ramp is available on Pin 23 (V_{OUT}) to drive an external power stage.

The gain of this stage can be adjusted (± 25%) depending on its register value.

The mean value of this ramp is driven by its own I^2C register (vertical position). Its value is VPOS = 7/16 · V_{REF-V} ± 400mV.

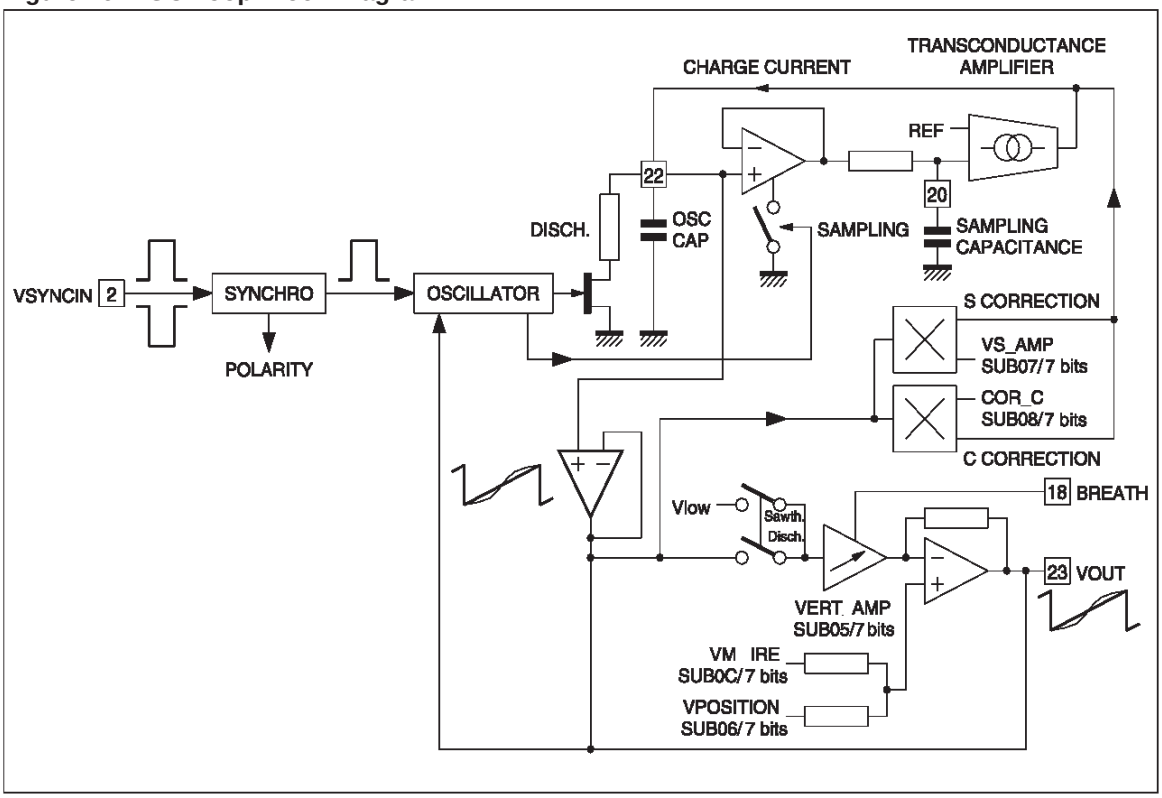
Usually V_{OUT} is sent through a resistive divider to the inverting input of the booster. Since VPOS derives from V_{REF-V}, the bias voltage sent to the non-inverting input of the booster should also derive from V_{REF-V} to optimize the accuracy (see Application Diagram).

3.3 Vertical Moiré

By using the vertical Moiré, VPOS can be modulated from frame to frame. This function is intended to cancel the fringes which appear when the line to line interval is very close to the CRT vertical pitch.

The amplitude of the modulation is controlled by register VMOIRE on sub-address 0C and can be switched-off via the control bit D8.

Figure 16. AGC Loop Block Diagram



3.4 Basic Equations

In first approximation, the amplitude of the ramp on Pin 23 (VOUT) is:

V_{OUT} - VPOS = (V_{OSC} - V_{DCMID}) · (1 + 0.3 (V_{AMP}))

where:

V_{DCMID} = 7/16 V_{REF} (middle value of the ramp on Pin 22, typically 3.6V)

V_{OSC} = V_{22} (ramp with fixed amplitude)

V_{AMP} = -1 for minimum vertical amplitude register value and +1 for maximum

VPOS is calculated by:

VPOS = V_{DCMID} + 0.4 V_P

where V_P = -1 for minimum vertical position register value and +1 for maximum.

The current available on Pin 22 is:

$$I_{OSC} = \frac{3}{8} \cdot V_{REF} \times C_{OSC} \times f$$

where C_{OSC} = capacitor connected on Pin 22 and f = synchronization frequency.

3.5 Geometric Corrections

The principle is represented in Figure 17 on page 31.

Starting from the vertical ramp, a parabola-shaped current is generated for E/W correction (also known as Pin Cushion correction), dynamic horizontal phase control correction, and vertical dynamic focus correction.

The parabola generator is made by an analog multiplier, the output current of which is equal to:

DI = k ·(V_{OUT} - V_{DCMID})^2

where V_{OUT} is the vertical output ramp (typically between 2 and 5V) and V_{DCMID} is 3.6V (for V_{REF-V} = 8.2V). The VOUT sawtooth is typically centered on 3.6V. By changing the vertical position, the sawtooth shifts by ±0.4V.

To provide good screen geometry for any end-user adjustment, the STV6886 has the “geometry tracking” feature which automatically adapts the parabola shape, depending on the vertical position and size.

Due to the large output stage voltage range (E/W Pin Cushion, Keystone, E/W Corner), the combination of the tracking function, maximum vertical amplitude, maximum or minimum vertical position and maximum gain on the DAC control may lead to output stage saturation. This must be avoided by limiting the output voltage with appropriate I^2C register values.

For the E/W part and the dynamic horizontal phase control part, a sawtooth-shaped differential current in the following form is generated:

$\Delta I' = k' \cdot (V_{OUT} - V_{DCMID})$

Then ΔI and $\Delta I'$ are added and converted into voltage for the E/W part.

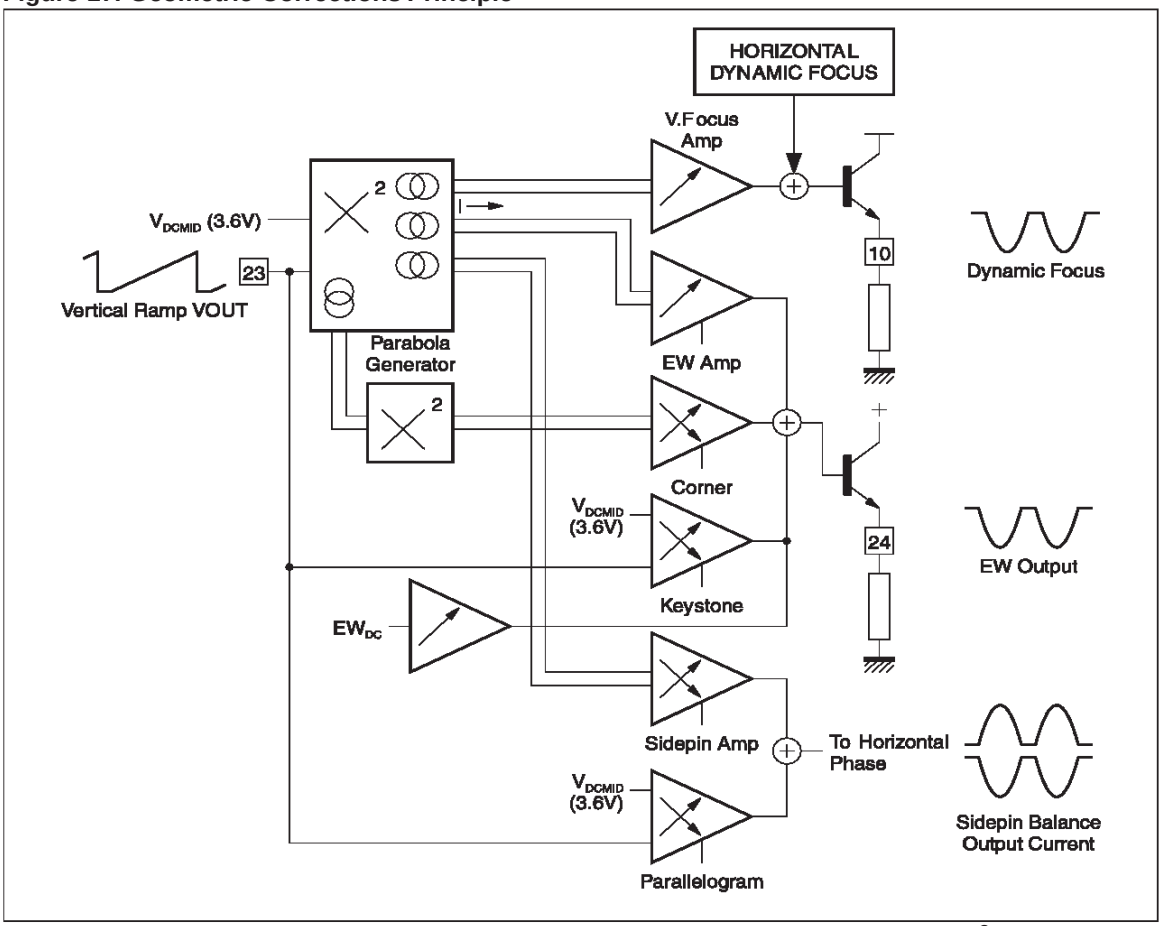
Each of the three E/W components or the two dynamic horizontal phase control components may be inhibited by their own I^2C select bit.

The E/W parabola is available on Pin 24 via an emitter follower output stage which has to be biased by an external resistor (10kΩ to ground). Being stable in temperature, the device can be DC coupled with external circuitry (mandatory to obtain H Size control).

The vertical dynamic focus is combined with the horizontal focus on Pin 10.

The dynamic horizontal phase control drives internally the H-position, moving the HFLY position on the horizontal sawtooth in the range of $\pm$ 2.8 $\%T_H$ both for side pin balance and parallelogram.

Figure 17. Geometric Corrections Principle



3.6 E/W

$EWOUT = EW_{DC} + K1 (V_{OUT} - V_{DCMID}) + K2 (V_{OUT} - V_{DCMID})^2 + K3 (V_{OUT} - V_{DCMID})^4$

K1 is adjustable by the keystone I^2C register.

K2 is adjustable by the E/W amplitude I^2C register.

K3 is adjustable by the E/W corner I^2C register.

3.7 Dynamic Horizontal Phase Control

I_{OUT}= K4 (V_{OUT} - V_{DCMID}) + K5 (V_{OUT} - V_{DCMID})^2

K4 is adjustable by the parallelogram I^2C register.

K5 is adjustable by the side pin balance I^2C register.

4 DC/DC CONVERTER PART

This unit controls the switch-mode DC/DC converter. It converts a DC constant voltage into the B+ voltage (roughly proportional to the horizontal frequency) necessary for the horizontal scanning.

This DC/DC converter can be configured either in step-up or step-down mode. In both cases it operates very similarly to the well known UC3842.

4.1 Step-up Configuration

Operating Description

– The power MOS is switched ON during the flyback (at the beginning of the positive slope of the horizontal focus sawtooth).

– The power MOS is switched OFF when its current reaches a predetermined value. For this purpose, a sense resistor is inserted in its source. The voltage on this resistor is sent to Pin16 (I_{SENSE}).

– The feedback (coming either from the EHV or from the flyback) is divided to a voltage close to 5.0V and compared to the internal 5.0V reference (I_{VREF}). The difference is amplified by an error amplifier, the output of which controls the power MOS switch-off current.

Main Features

– Switching synchronized on the horizontal frequency,

– B+ voltage always higher than the DC source,

– Current limited on a pulse-by-pulse basis.

The DC/DC converter is disabled:

– when V_{CC} or V_{DD} are too low,

– when X-Ray protection is latched,

– directly through I^2C bus.

When disabled, BOUT is driven to GND by a 0.5mA current source. This feature allows to implement externally a soft start circuit.

4.2 Step-down Configuration

In step-down configuration, the I_{SENSE} information is not used any more and therefore not sent to the Pin16. This configuration is selected by connecting this Pin16 to a DC voltage higher than 6V (for example V_{REF-V}).

Instead of I_{SENSE} waveform the H-Focus Sawtooth is used for comparison with the amplified error voltage. For that reason, the Step-down configuration can operate only if the H-Focus capacitor is connected.

Operating Description

– The power MOS is switched ON as for the step-up configuration.

– The feedback to the error amplifier is done as for the step-up configuration.

– The power MOS is switched OFF when the HFOCUSCAP voltage gets higher than the error amplifier output voltage.

Main Features

– Switching synchronized on the horizontal frequency,

– B+ voltage always lower than the DC source,

– No current limitation.

4.3 Step-up and Step-down Configuration Comparison

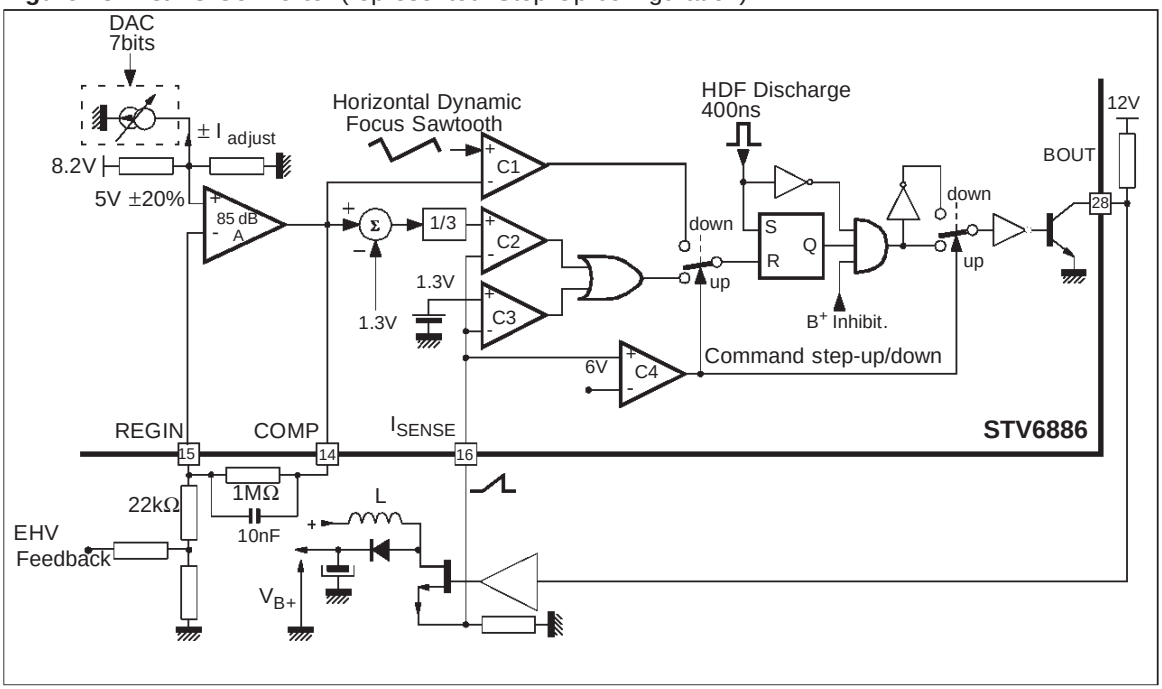
In step-down configuration the control signal is inverted compared with the step-up mode.This, for the following reason:

– In step-up mode, the switch is a N-channel MOS referenced to ground and made conductive by a high level on its gate.

– In step-down, a high-side switch is necessary. It can be either a P- or a N-channel MOS.

- For a P-channel MOS, the gate is controlled directly from Pin 28 through a capacitor (this allows to spare a Transformer). In this case, a negative-going pulse is needed to make the MOS conductive. Therefore it is necessary to invert the control signal.
- For a N-channel MOS, a transformer is needed to control the gate. The polarity of the transformer can be easily adapted to the negative-going control pulse.

Figure 18. DC/DC Converter (represented: Step-Up configuration)



INTERNAL SCHEMATICS

Figure 19.

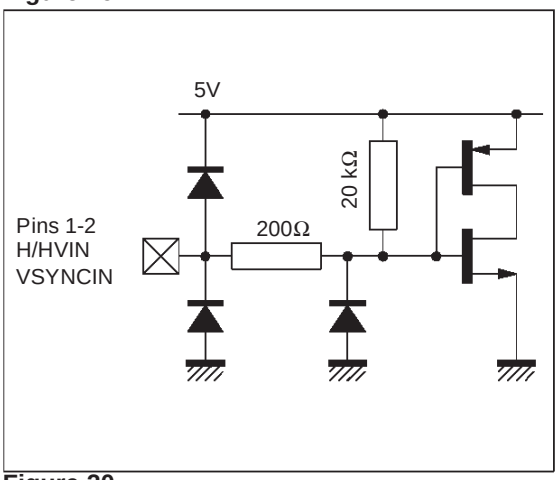


Figure 20.

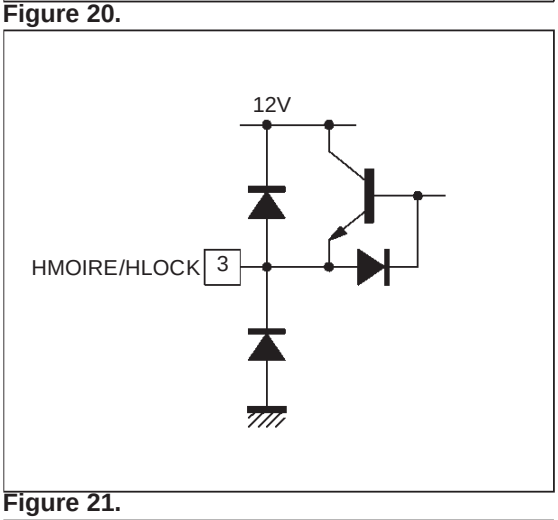


Figure 21.

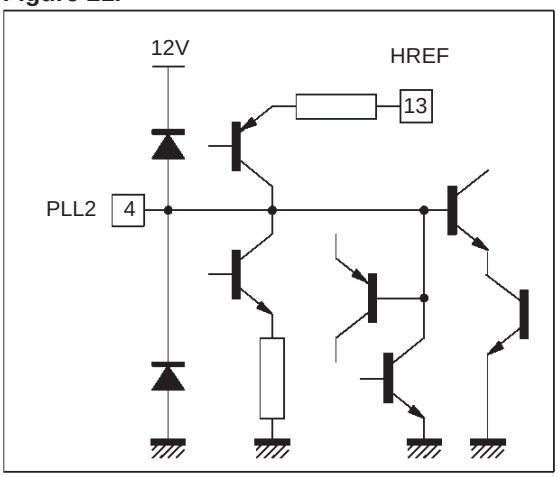


Figure 22.

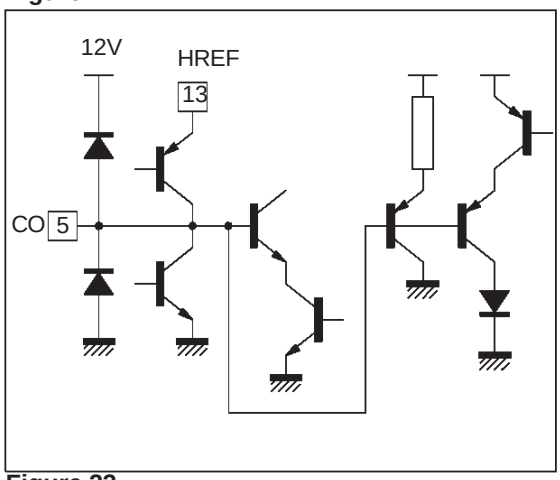


Figure 23.

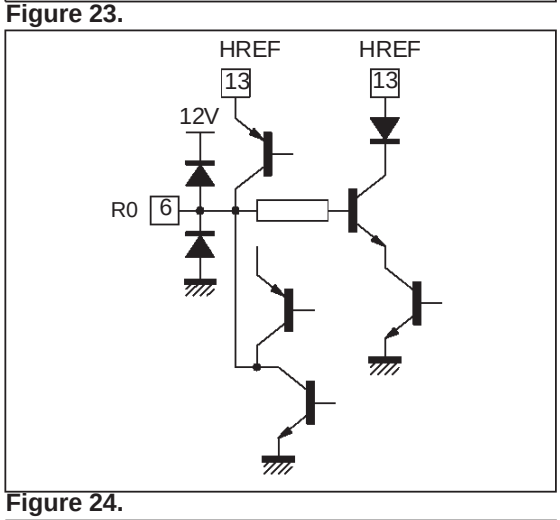


Figure 24.

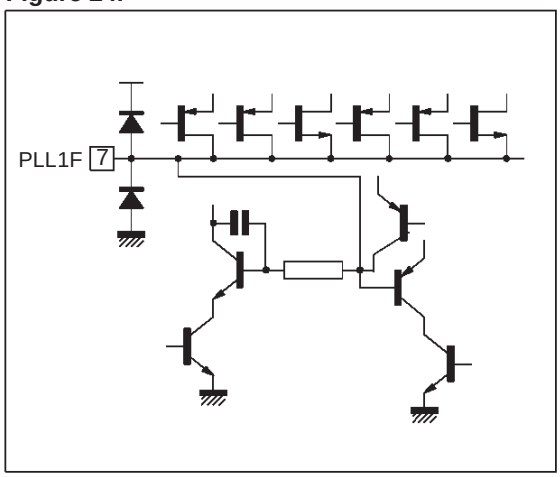


Figure 25.

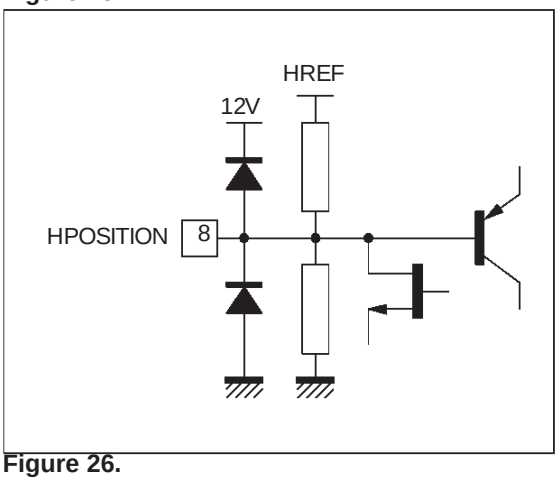


Figure 26.

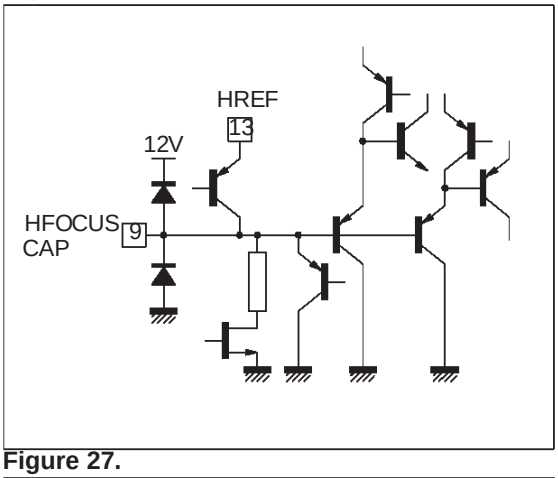


Figure 27.

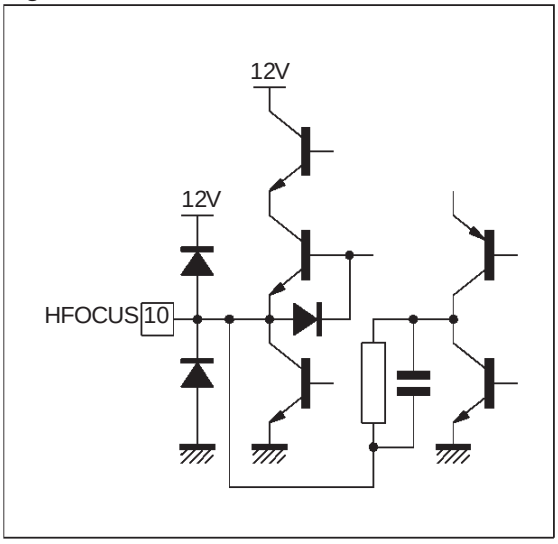


Figure 28.

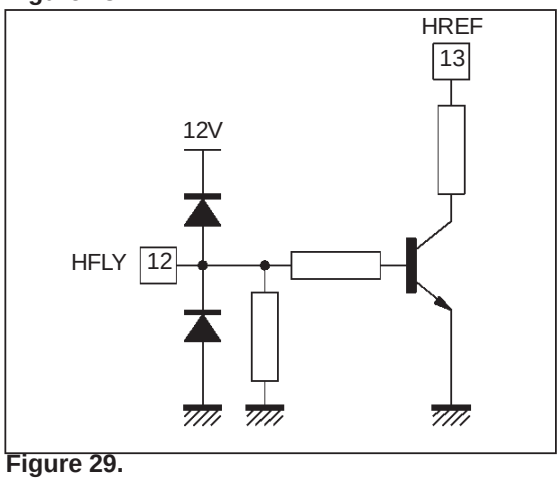


Figure 29.

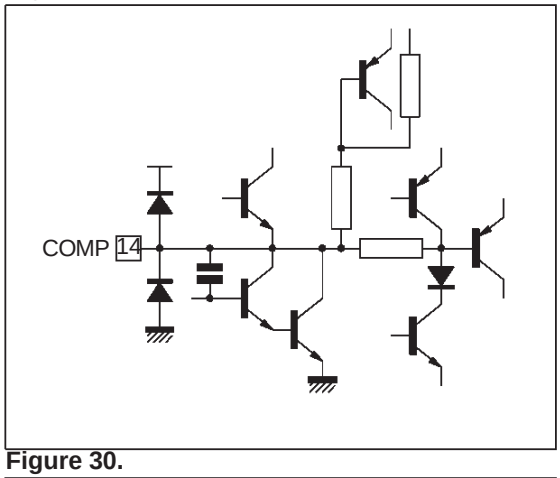


Figure 30.

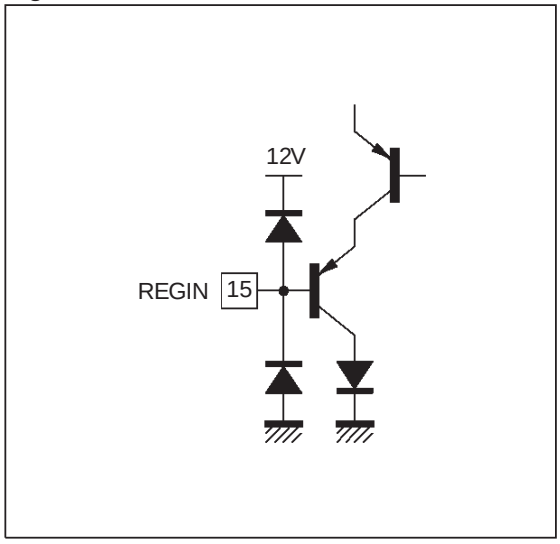


Figure 31.

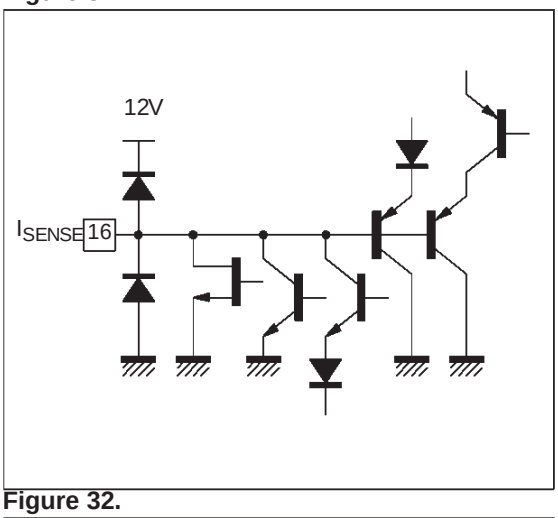


Figure 32.

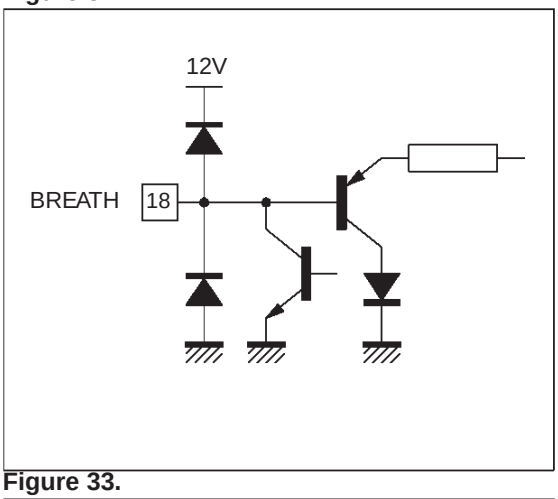


Figure 33.

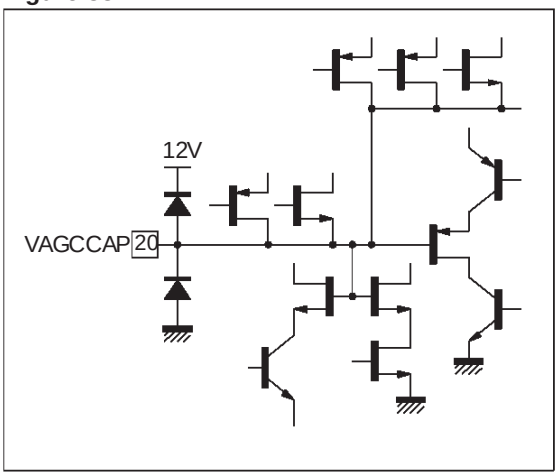


Figure 34.

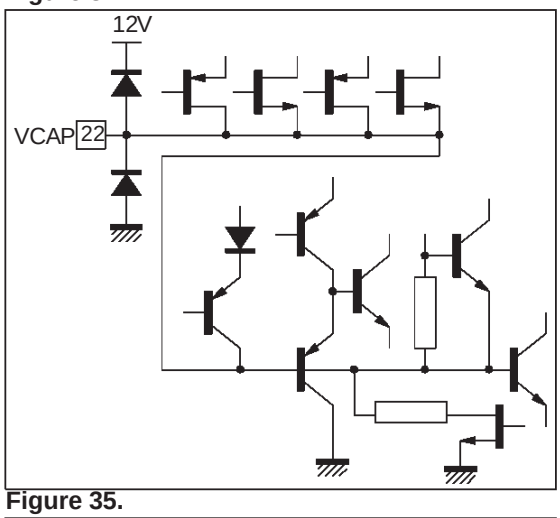


Figure 35.

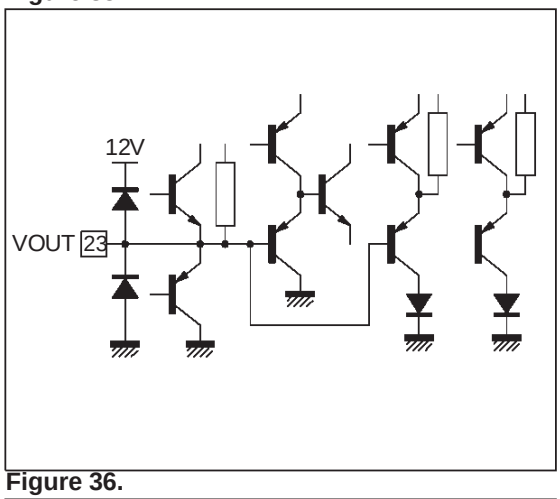


Figure 36.

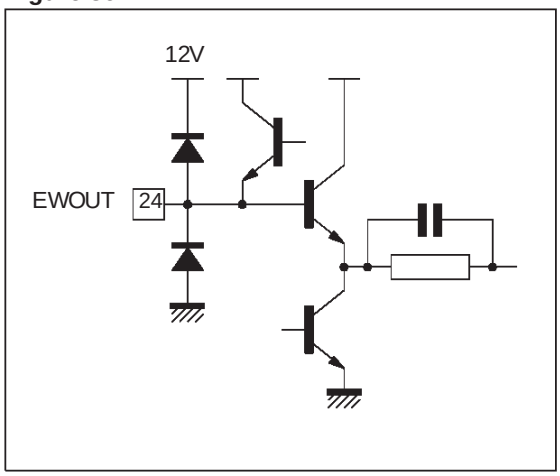


Figure 37.

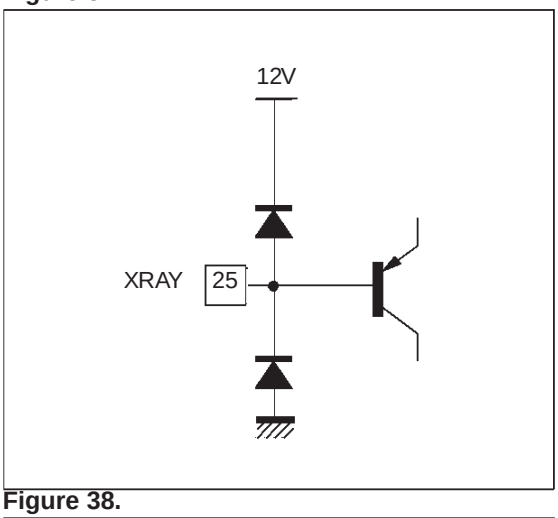


Figure 38.

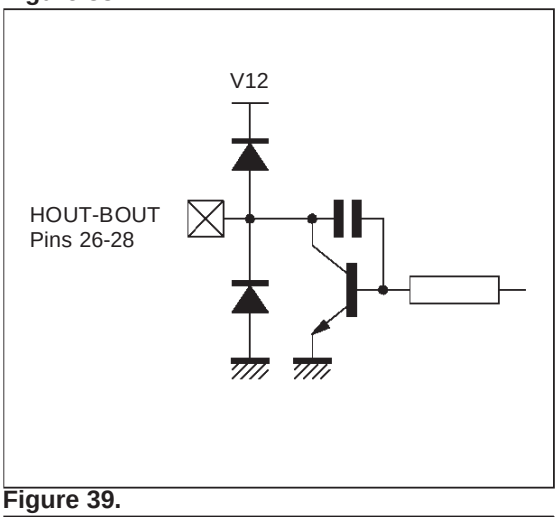


Figure 39.

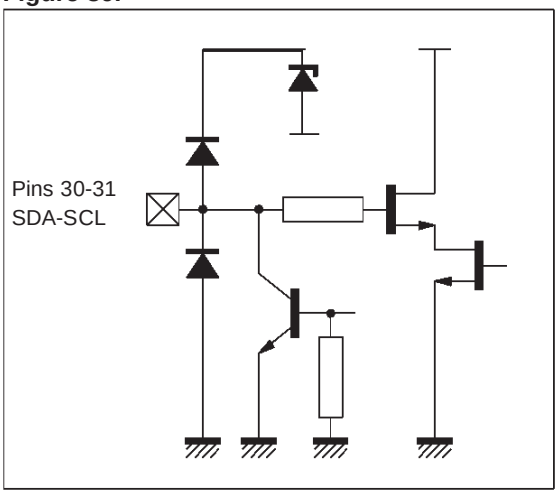


Figure 40. Demonstration Board

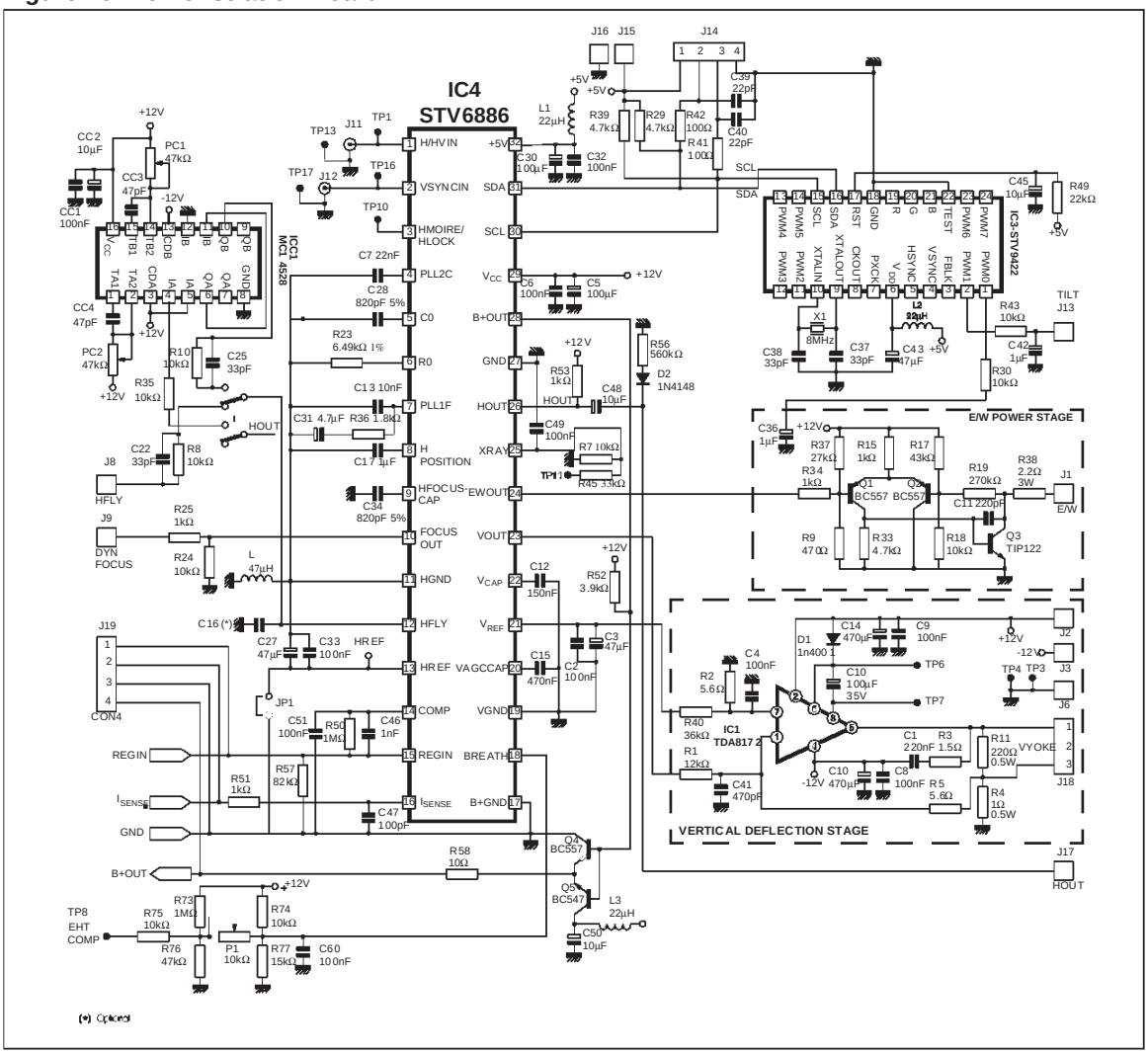


Figure 41.

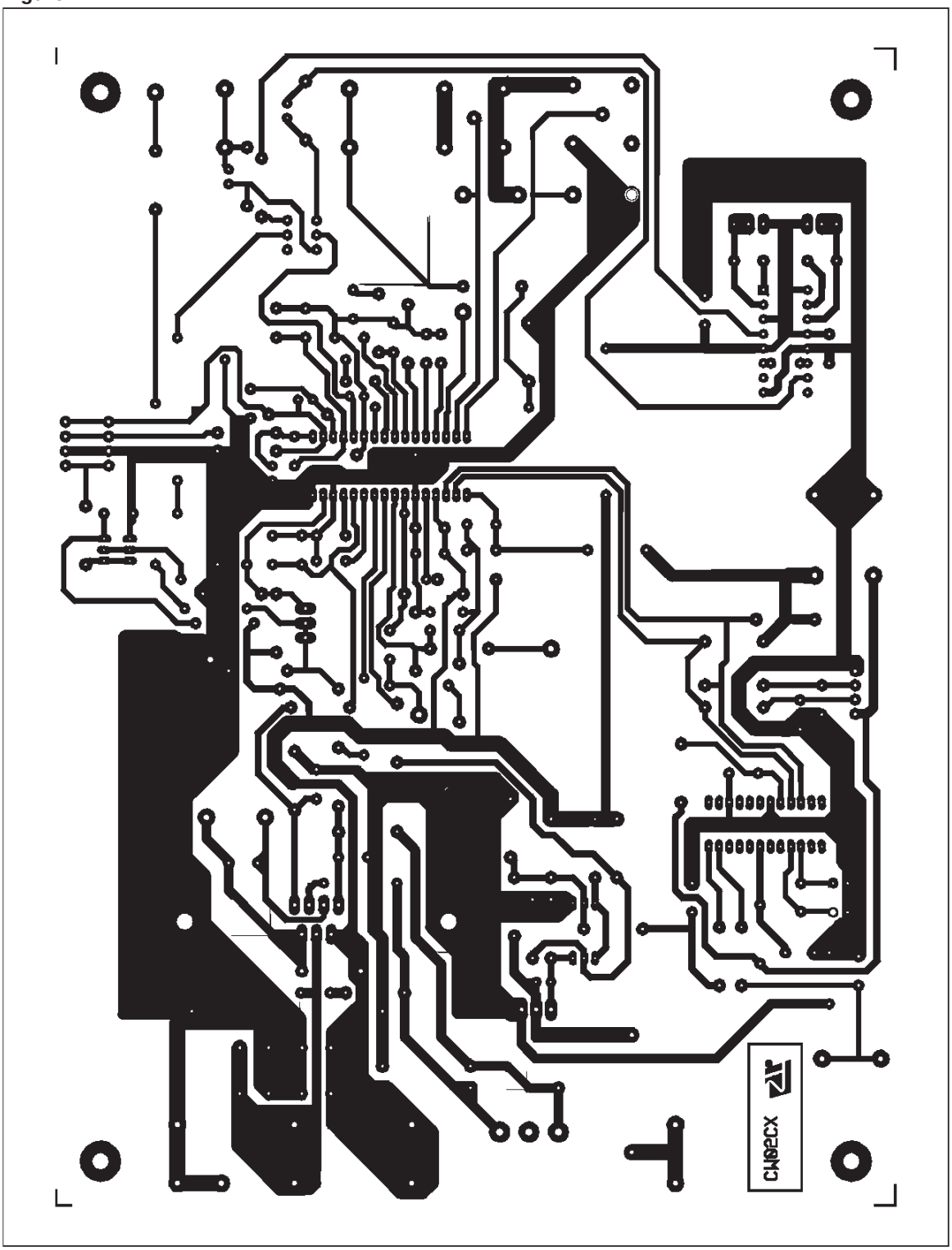
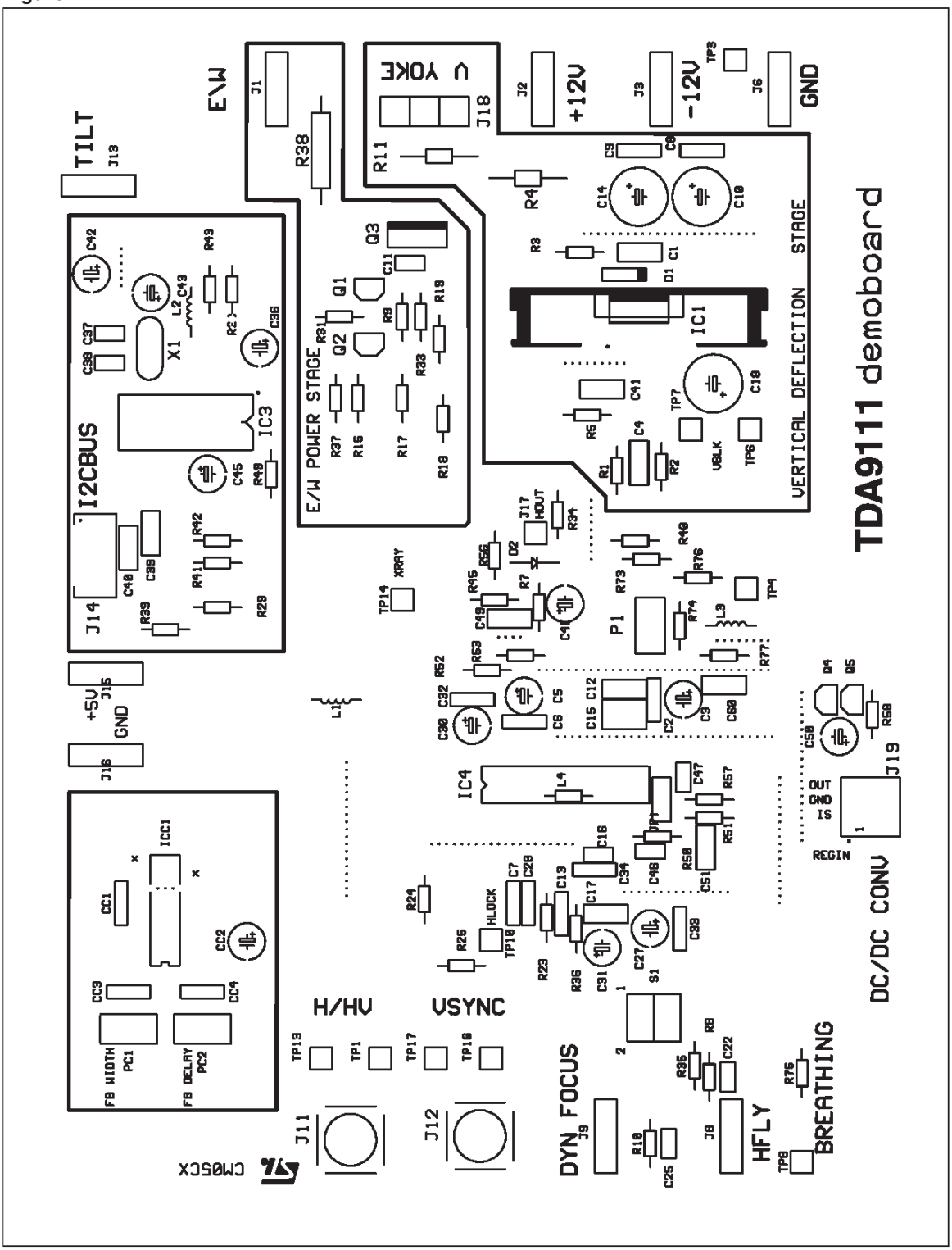


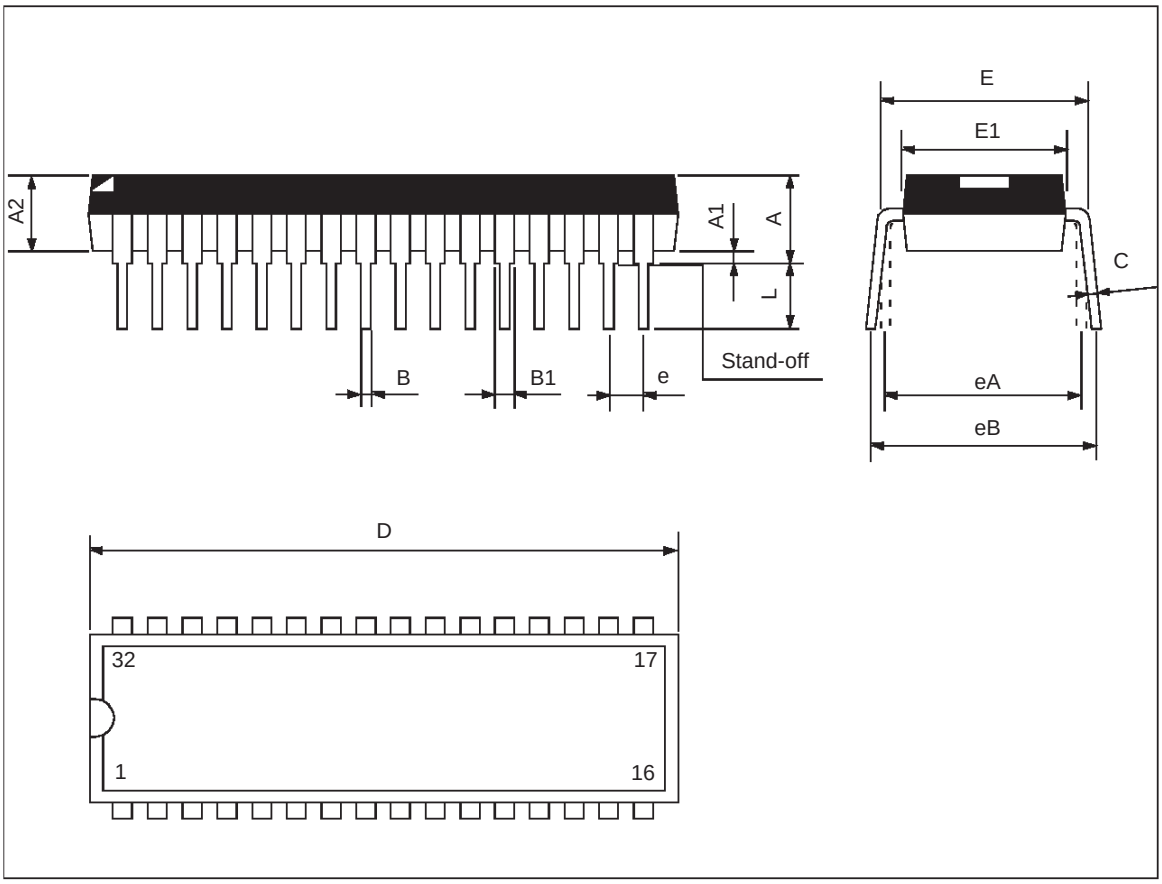
Figure 42.



PACKAGE MECHANICAL DATA

PACKAGE MECHANICAL DATA

32 PINS - PLASTIC SHRINK



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.556	3.759	5.080	0.140	0.148	0.200
A1	0.508			0.020		
A2	3.048	3.556	4.572	0.120	0.140	0.180
B	0.356	0.457	0.584	0.014	0.018	0.023
B1	0.762	1.016	1.397	0.030	0.040	0.055
C	.203	0.254	0.356	0.008	0.010	0.014
D	27.43	27.94	28.45	1.080	1.100	1.120
E	9.906	10.41	11.05	0.390	0.410	0.435
E1	7.620	8.890	9.398	0.300	0.350	0.370
e		1.778			0.070	
eA		10.16			0.400	
eB			12.70			0.500
L	2.540	3.048	3.810	0.100	0.120	0.150