STV9427
STV9428-STV9429

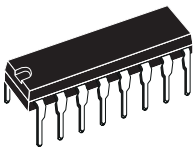
HIGH SPEED MULTISYNCH ON-SCREEN DISPLAY FOR MONITOR

- CMOS SINGLE CHIP OSD FOR MONITOR
- BUILT IN 1 KBYTE RAM HOLDING :
  - CHARACTER CODES
  - USER DEFINABLE CHARACTERS
- 207 ALPHANUMERIC CHARACTERS OR GRAPHIC SYMBOLS IN INTERNAL ROM
- 12 x 18 CHARACTER DOT MATRIX
- PROGRAMMABLE ACCENTUATED CHARACTER SET
- CHARACTER BLINKING
- RAM DEFINABLE COLOR LOOK UP TABLE
- UP TO 16 USER DEFINABLE CHARACTERS
- UP TO 80MHz PIXEL CLOCK
- INTERNAL HORIZONTAL PLL (15 TO 120kHz)
- PROGRAMMABLE VERTICAL HEIGHT OF CHARACTER WITH A SLICE INTERPOLATOR TO MEET MULTI-SYNCH REQUIREMENTS
- PROGRAMMABLE VERTICAL AND HORIZONTAL POSITIONING
- FLEXIBLE SCREEN DESCRIPTION
- 22 CONTROL CODES FOR POWERFULL SERIAL ATTRIBUTES
- 2-WIRES ASYNCHRONOUS SERIAL MCU INTERFACE (I^2C PROTOCOL)
- 8 x 8 BITS PWM DAC OUTPUTS
- SINGLE POSITIVE 5V SUPPLY

DESCRIPTION

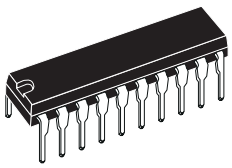
The STV9427/28/29 is an ON SCREEN DISPLAY for monitor. It is built as a slave peripheral connected to a host MCU via a serial I^2C bus. It includes a display memory, controls all the display attributes and generates pixels from the data read in its on chip memory. The line PLL and a special slice interpolator allow to have a display aspect which does not depend on the line and frame frequencies. I^2C interface allows MCU to make transparent internal access to prepare the next pages during the display of the current page. Toggle from one page to another by programming only one register.

8 x 8 bits PWM DAC are available to provide DC voltage control to other peripherals.
The STV9427/28/29 provides the user an easy to use and cost effective solution to display alphanumeric or graphic information on monitor screen.



DIP16
(Plastic Package)

ORDER CODE : STV9427



DIP20
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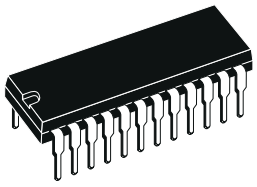
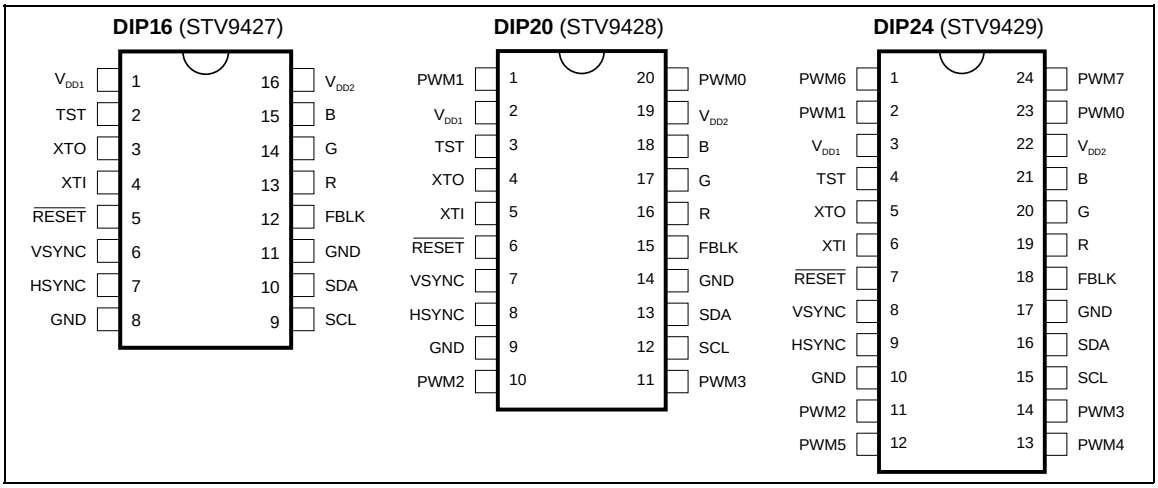
ORDER CODE : STV9428



DIP24
(Plastic Package)

ORDER CODE : STV9429

PIN CONNECTIONS



PIN DESCRIPTION

Symbol	Pin Number			I/O	Description
	DIP24	DIP20	DIP16		
PWM6	1	-	-	O	DAC0 Output
PWM1	2	1	-	O	DAC1 Output
V_{DD1}	3	2	1	S	+5V Logic Supply
TST	4	3	2	I	Reserved (not to be connected)
XTO	5	4	3	O	Crystal Output
XTI	6	5	4	I	Crystal or Clock Input
$\overline{\text{RESET}}$	7	6	5	I	Reset Input (Active Low)
VSYNC	8	7	6	I	Vertical Sync Input
HSYNC	9	8	7	I	Horizontal Sync Input
GND	10	9	8	S	Logic Ground
PWM2	11	10	-	O	DAC2 Output
PWM5	12	-	-	O	DAC3 Output
PWM4	13	-	-	O	DAC4 Output
PWM3	14	11	-	O	DAC5 Output
SCL	15	12	9	I	Serial Clock
SDA	16	13	10	I/O	Serial Input/output Data
GND	17	14	11	S	Ground
FBLK	18	15	12	O	Fast Blanking Output
R	19	16	13	O	Red Output
G	20	17	14	O	Green Output
B	21	18	15	O	Blue Output
V_{DD2}	22	19	16	S	+5V Outputs Supply
PWM0	23	20	-	O	DAC6 Output
PWM7	24	-	-	O	DAC7 Output

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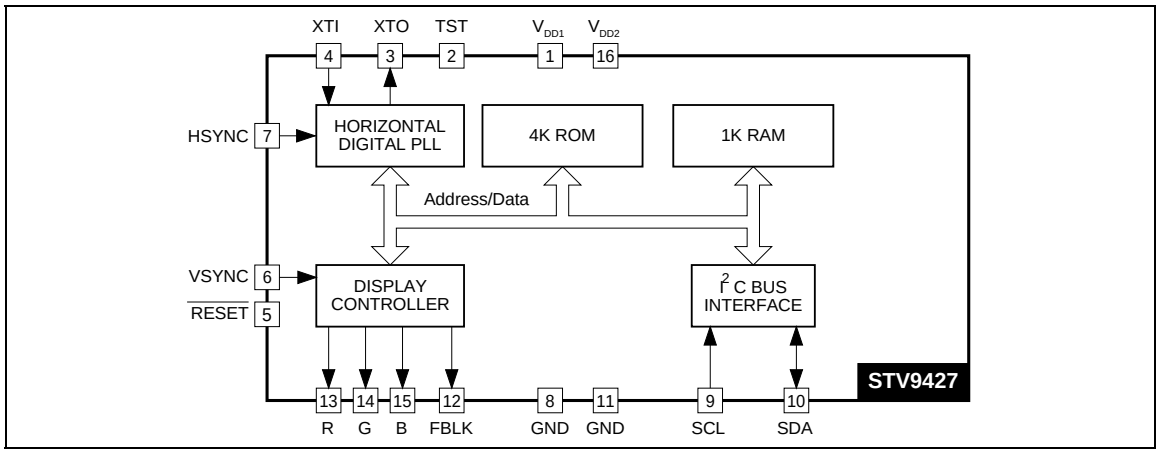
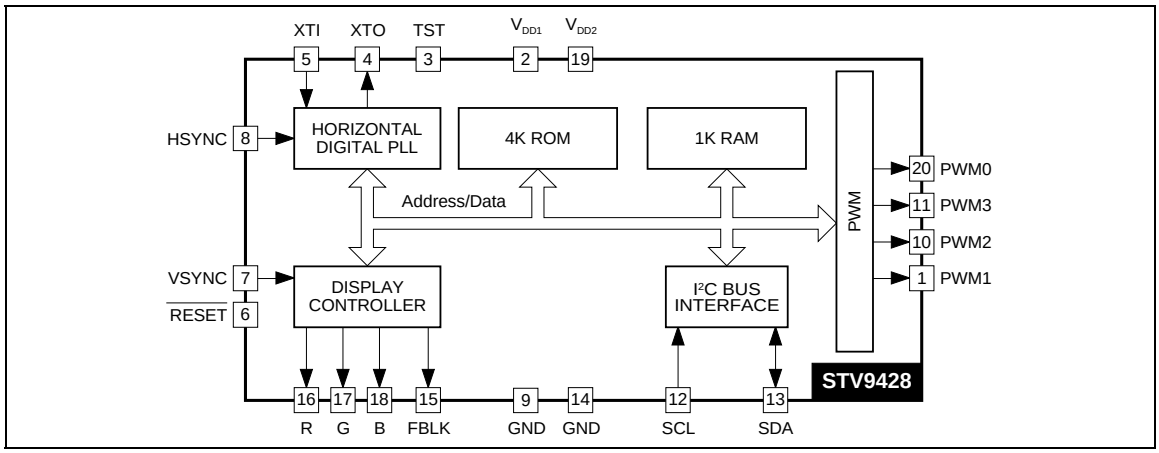
BLOCK DIAGRAMS

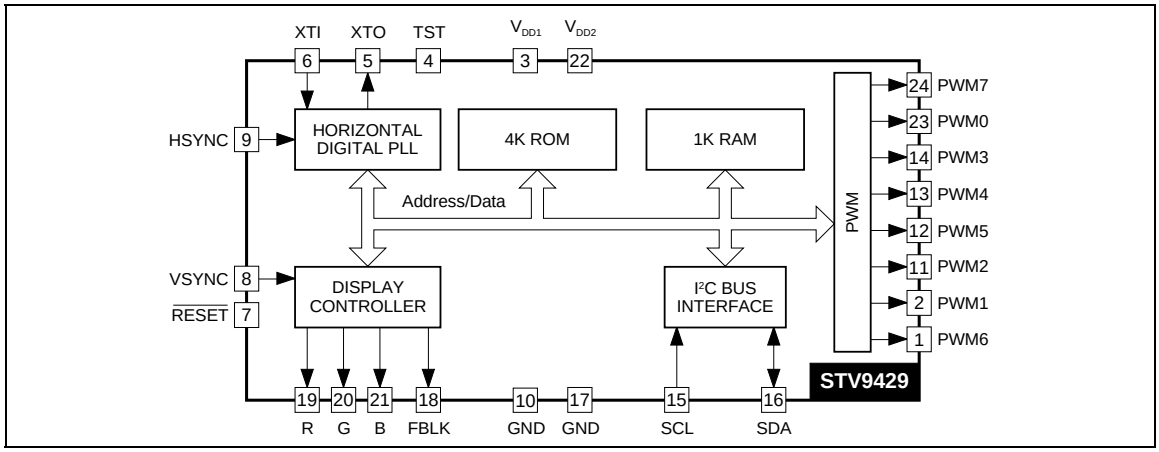
STV9427



STV9428



STV9429



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3, +7.0	V
V_{IN}	Input Voltage	-0.3, +7.0	V
T_{OPER}	Operating Temperature	0, +70	°C
T_{STG}	Storage Temperature	-40, +125	°C

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ELECTRICAL CHARACTERISTICS

(V_{DD1} = V_{DD2} = 5V, V_{SS} = 0V, T_A = 0 to 70°C, f_{XTAL} = 8 to 15MHz, TEST = 0 V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY					
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DD}	Supply Current	-	65	90	mA
INPUTS					
SCL, SDA, $\overline{\text{RESET}}$, VSYNC and HSYNC					
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.4			V
I_{IL}	Input Leakage Current	-10		+10	µA
OUTPUTS					
SDA open drain and PWMi (i = 0 to 7)					
V_{OL}	Output Low Voltage (I_{OL} = 1.6mA)	0		0.4	V
V_{OH}	Output High Voltage (I_{OH} = -0.1mA)	0.9V_{DD}		V_{DD}	V
R, G, B, FBLK					
V_{OL}	Output Low Voltage (I_{OL} = 1.6mA)	0		0.4	V
V_{OH}	Output High Voltage (I_{OH} = -0.1mA)	0.9V_{DD}		V_{DD}	V

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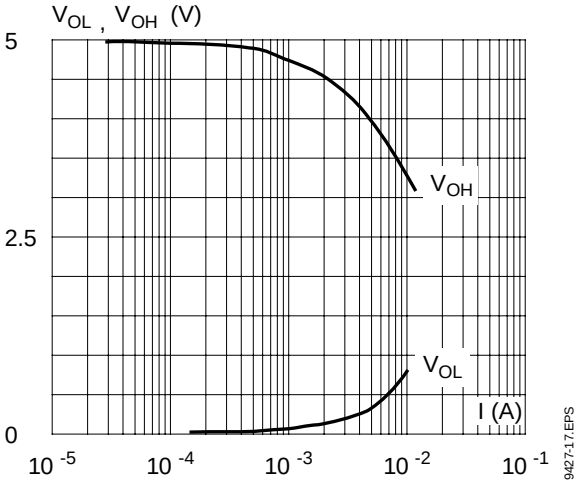
Figure 1 : R, G, B, FBLK Typical Outputs Static Characteristics



TIMINGS

Symbol	Parameter	Min.	Typ.	Max.	Unit
OSCILATOR INPUT : XTI (see Figure 2)					
t_{WH}	Clock High Level	20			ns
t_{WL}	Clock Low Level	20			ns
f_{XTAL}	Clock Frequency	6		15	MHz
f_{PXL}	Pixel Frequency	30		80	MHz
RESET					
t_{RES}	$\overline{\text{RESET}}$ Low Level Pulse	4			µs
R, G, B, FBLK (C_{LOAD} = 30pF)					
t_R	Rise Time (see Note 1)		5		ns
t_F	Fall Time (see Note 1)		5		ns
t_{SKEW}	Skew between R, G, B, FBLK		5		ns
I^2C INTERFACE : SDA AND SCL (see Figure 3)					
f_{SCL}	SCL Clock Frequency (Horizontal frequency = 32kHz)			288	kHz
t_{BUF}	Time the bus must be free between 2 access	500			ns
t_{HDS}	Hold Time for Start Condition	500			ns
t_{SUP}	Set up Time for Stop Condition	500			ns
t_{LOW}	Clock Low Level	400			ns
t_{HIGH}	Clock High Level	400			ns
t_{HDAT}	Hold Time Data	0			ns
t_{SUDAT}	Set up Time Data	500			ns
t_F	SDA Fall Time			20	ns
t_R	SCL and SDA Rise Time	Depend on the pull-up resistor and on the load capacitance			

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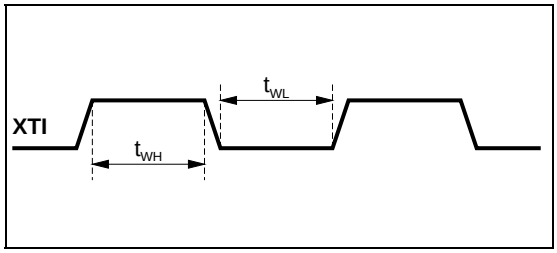
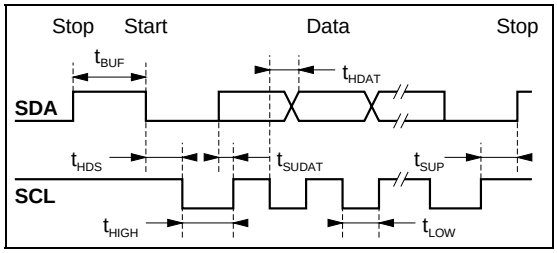
Note 1 : These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches comming from corners of our processes and also temperature characterization.

Figure 2



9427-03.EPS

Figure 3



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FUNCTIONAL DESCRIPTION

The STV9427/28/29 display processor operation is controlled by a host MCU via the I²C interface. It is fully programmable through internal read/write registers and performs all the display functions by generating pixels from data stored in its internal memory. After the page downloading from the MCU, the STV9427/28/29 refreshes screen by its built in processor, without any MCU control (access). In addition, the host MCU has a direct access to the on chip 1Kbytes RAM during the display of the current page to make any update of its contents.

With the STV9427/28/29, a page displayed on the screen is made of several strips which can be of 2 types : spacing or character and which are described by a table of descriptors and character codes in RAM. Several pages can be downloaded at the same time in the RAM and the choice of the current display page is made by programming the DISPLAY CONTROL register.

I - Serial Interface

The 2-wires serial interface is an I²C interface. To be connected to the I²C bus, a device must own its slave address ; the slave address of the STV9427/28/29 is BA (in hexadecimal).

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	1	1	1	0	1	

I.1 - Data Transfer in Write Mode

The host MCU can write data into the STV9427/28/29 registers or RAM.

To write data into the STV9427/28/29, after a start, the MCU must send (Figure 4) :
- First, the I²C address slave byte with a low level for the R/W bit,
- The two bytes of the internal address where the MCU wants to write data(s),
- The successive bytes of data(s).

All bytes are sent MSB bit first and the write data transfer is closed by a stop.
Each byte is synchronously transfered at each HSYNC period.

I.2 - Data Transfer in Read Mode

The host MCU can read data from the STV9427/28/29 registers, RAM or ROM.

To read data from the STV9427/28/29 (Figure 5), the MCU must send 2 different I²C sequences. The first one is made of I²C slave address byte with R/W bit at low level and the 2 internal address bytes. The second one is made of I²C slave address byte with R/W bit at high level and all the successive data bytes read at successive addresses starting from the initial address given by the first sequence. Each byte is synchronously transfered at each HSYNC period. The first data byte, in read mode, is available one Hsync period after the acknowledge of the address byte.

Figure 4 : MCU I²C Write Operation

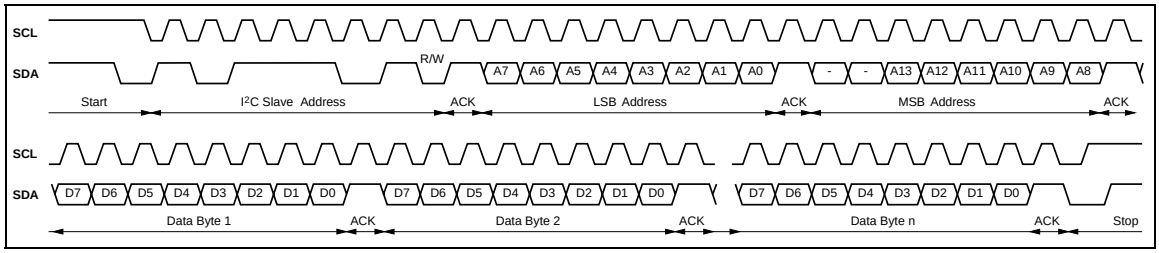
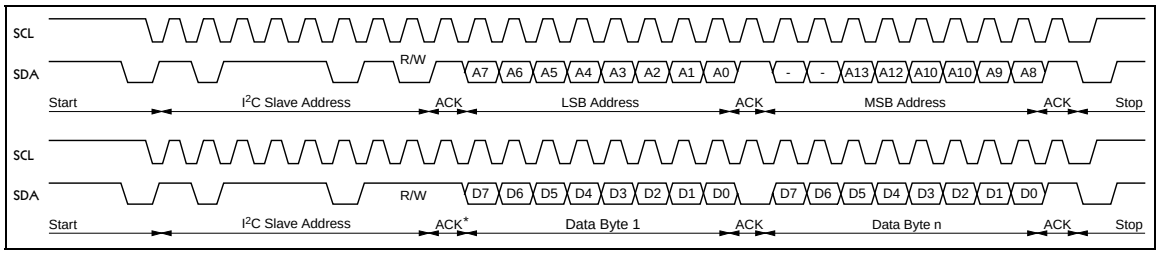


Figure 5 : MCU I²C Read Operation



Note : The first data bit out (D7) is valid after one scanline period.

FUNCTIONAL DESCRIPTION (continued)

I.3 - Addressing Space

I.3.1 - General Mapping

STV9427/28/29 registers, RAM and ROM are mapped in a 16Kbytes addressing space. The mapping is the following :

0000 03FF	1024 bytes RAM	Descriptors character codes and user definable characters
0400 07FF	Empty Space	
0800 3FBF	Character Generator ROM	
3FC0 3FD0	Empty Space	
3FCF 3FD0	Internal Registers	

I.3.2 - I^2C Registers Mapping

3FCF		
3FD0	PWM0	PWM registers
	PWM1	
	PWM2	
	PWM3	
	PWM4	
	PWM5	
	PWM6	
3FD7	PWM7	
3FD8	Reserved	
3FDF		
3FE0	Color 0	Color look-up table (CLUT)
	Color 1	
	Color 2	
	Color 3	
	Color 4	
	Color 5	
	Color 6	
3FE7	Color 7	
3FE8	Color 8	
	Color 9	
	Color 10	
	Color 11	
	Color 12	
	Color 13	
	Color 14	
3FEF	Color 15	
3FF0	Line Duration	Control registers
	Top Margin	
	Horizontal Delay	
	Character Height	
	Display Control	
	Locking Time Constant	
	Capture Time Constant	
	Initial Pixel period	
3FF8	Frequency Multiplier	
3FF9	Reserved	
3FFF		

I.4 - Register Set

I.4.1 - PWM Registers

The eight registers described below are only available with the STV9429 :

PULSE WIDTH MODULATOR 0 (STV9429)

3FD0	V07	V06	V05	V04	V03	V02	V01	V00

V0[7:0] : Digital value of the 1st PWM D to A converter.

PULSE WIDTH MODULATOR 1 (STV9429)

3FD1	V17	V16	V15	V14	V13	V12	V11	V10

V1[7:0] : Digital value of the 2nd PWM DAC.

PULSE WIDTH MODULATOR 2 (STV9429)

3FD2	V27	V26	V25	V24	V23	V22	V21	V20

V2[7:0] : Digital value of the 3rd PWM DAC.

PULSE WIDTH MODULATOR 3 (STV9429)

3FD3	V37	V36	V35	V34	V33	V32	V31	V30

V3[7:0] : Digital value of the 4th PWM DAC.

PULSE WIDTH MODULATOR 4 (STV9429)

3FD4	V47	V46	V45	V44	V43	V42	V41	V40

V4[7:0] : Digital value of the 5th PWM DAC.

PULSE WIDTH MODULATOR 5 (STV9429)

3FD5	V57	V56	V55	V54	V53	V52	V51	V50

V5[7:0] : Digital value of the 6th PWM DAC.

PULSE WIDTH MODULATOR 6 (STV9429)

3FD6	V67	V66	V65	V64	V63	V62	V61	V60

V6[7:0] : Digital value of the 7th PWM DAC.

PULSE WIDTH MODULATOR 7 (STV9429)

3FD7	V77	V76	V75	V74	V73	V72	V71	V70

V7[7:0] : Digital value of the 8th PWM DAC.

Note : Power on reset default value of PMW register is 00H

FUNCTIONAL DESCRIPTION (continued)

I.4.2 - Look-up Table Registers

Color look-up table [CLUT] is read/write RAM table. Mapping address is described in Chapter I.3.2.

The CLUT is splitted in 2 blocks of 8 bytes. Each byte contains foreground and background informations as described below :

SHA	BR	BG	BB	FL	FR	FG	FB

SHA : Shadowing
FL : Flashing foreground
BR, BG, BB : Background color
FR, FG, FB : Foreground color

If SHA = 1 and BR = BG = BB = 0, the background of the character is transparent.

Each block may store a different set of colors. One block of colors may be used for the normal items of the menu while the second block, with brighter colors, may be used for selected items of the menu.

The block selection is done by programming bit CLU3 of CLU[3:0] of the character descriptor (see Table 1). It remains selected all the row long.

Bit CLU2, CLU1 and CLU0 of CLU[3:0] of the character descriptor select the active color at the beginning of the row.

The active color can be changed along the row, using 8 control codes COL0 to COL7.

Each control code (COL0 to COL7) active a dedicated color byte in the CLUT as described in Table 2.

Table 1 : CLUT Block Selection

CLU3	CLU[2:0]	Code Name	Ram @(hex)	Reset Value (hex)
0	0	Col 0	@3FE0	07
	1	Col 1	@3FE1	16
	2	Col 2	@3FE2	25
	3	Col 3	@3FE3	34
	4	Col 4	@3FE4	43
	5	Col 5	@3FE5	52
	6	Col 6	@3FE6	61
	7	Col 7	@3FE7	70
1	0	Col 0	@3FE8	70
	1	Col 1	@3FE9	61
	2	Col 2	@3FEA	52
	3	Col 3	@3FEB	43
	4	Col 4	@3FEC	34
	5	Col 5	@3FED	25
	6	Col 6	@3FEE	16
	7	Col 7	@3FEF	07

Table 2 : CLUT Color Selection

Code Name	Code Nbr (h)	Color Look-up Table in RAM
COL1	10	@ 3FE0 : Color 0
COL2	11	@ 3FE1 : Color 1
COL6	16	@ 3FE6 : Color 6
COL7	17	@ 3FE7 : Color 7
COL0	10	@ 3FE8 : Color 8
COL1	11	@ 3FE9 : Color 9
COL6	16	@ 3FEE : Color 14
COL7	17	@ 3FEF : Color 15

I.4.3 - Control Registers

LINE DURATION (Reset Value : 20h)

3FF0	VSP	HSP	LD6	LD5	LD4	LD3	LD2	LD1

VSP : V-SYNC active edge selection
= 0, falling egde,
= 1, rising edge.

HSP : H-SYNC active edge selection
= 0, falling egde,
= 1, rising edge.

LD[6:1] : LINE DURATION
LD0 = 0
LD1 = 2 periods of character
One character period is 12 pixels long.

TOP MARGIN (Reset Value : 60h)

3FF1	M8	M7	M6	M5	M4	M3	M2	M1

M[8:1] : TOP MARGIN height from the VSYNC reference edge.
M0 = 0
M1 = 2 scan lines

Note : The top margin is displayed before the first strip of descriptor list. It can be black if FBK of DISPLAY CONTROL register is set or transparent if FBK is clear.

HORIZONTAL DELAY (Reset Value : 20h)

3FF2	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

DD[7:0] : HORIZONTAL DISPLAY DELAY from the HSYNC reference edge to the 1st pixel position of the character strips.
Unit = 6 pixel periods. Minimum value is 08h.
First pixel position = [DD[7:0] - 6] x 6 + 54.
with DD[7:0] = 1,3,5 then the delay is 60 pixel.

FUNCTIONAL DESCRIPTION (continued)

CHARACTERS HEIGHT (Reset Value : 24h)

3FF3	-	-	CH5	CH4	CH3	CH2	CH1	CH0

CH[5:0] : HEIGHT of the character strips in scan lines. For each scan line, the number of the slice which is displayed is given by :

SLICE-NUMBER =

$$\text{round}\left(\frac{\text{SCAN–LINE–NUMBER x 18}}{\text{CH[5:0]}}\right)$$

SCAN-LINE-NUMBER = Number of the current scan line of the strip.

DISPLAY CONTROL (Reset Value : 00h)

3FF4	OSD	FBK	FL1	FL0	P9	P8	P7	P6

OSD : ON/OFF (if 0, R, G, B and FBLK outputs are 0).

FBK : Fast blanking control :
= 1, forces FBLK pin at "1" outside and inside the OSD area. This leads to blank video RGB and to only display OSD RGB.
= 0, FBLK pin is driven according character code for normal display of OSD data.

FL[1:0] : Flashing mode :
- 00 : No flashing. The character attribute is ignored,
- 01 : Flashing at f_F (50% duty cycle),
- 10 : Flashing at 2 f_F,
- 11 : Flashing at 4 f_F.

Note : f_F is 128 time vertical frequency.

P[9:6] : Address of the 1st descriptor of the current displayed pages.
P[13:10] and P[5:0] = 0 ; up to 16 different pages can be stored in the RAM.

LOCKING CONDITION TIME CONSTANT (Reset Value : 01h)

3FF5	FR	AS2	AS1	AS0	LUK	BS2	BS1	BS0

FR : Free Running ; if = 1 PLL is disabled and the pixel frequency keeps its last value.

AS[2:0] : Phase constant during locking conditions.

BS[2:0] : Frequency constant during locking conditions.

LUK : Lock unlock status bit
0 = unlocked PLL
1 = Locked PLL

CAPTURE PROCESS TIME CONSTANT (Reset Value : 24h)

3FF6	LEN	AF2	AF1	AF0	-	BF2	BF1	BF0

LEN : Lock enable
0 = R,G,B, FBLK are always enabled,
1 = R,G,B, FBLK are enabled only when PLL is locked.

AF[2:0] : Phase constant during the capture process.

BF[2:0] : Frequency constant during the capture process.

INITIAL PIXEL PERIOD (Reset Value : 28h)

3FF7	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0

PP[7:0] : Value to initialize the pixel period of the PLL.

FREQUENCY MULTIPLIER (Reset Value : 0Ah)

3FF8	-	-	-	-	FM3	FM2	FM1	FM0

FM[3:0] : Frequency multiplier of the crystal frequency to reach the high frequency used by the PLL to derive the pixel frequency.

Note : For high pixel frequency (over 70MHz), write at address 3FFF, Data F0h.

II - Descriptors

SPACING

MSB	0	L/$\overline{C}$	-	-	-	-	-	-
LSB	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

L/$\overline{C}$: LINE or CHARACTER spacing :
= 0, spacing descriptor defined as character height (SL[7:0] = 1 to 255 character).
= 1, spacing descriptor defined as scan line height (SL[7:0] = 1 to 255 scan lines).

SL[7:0] : Number of selected height (character or scan lines according L/$\overline{C}$).

CHARACTER

MSB	1	DE	CLU3	CLU2	CLU1	CLU0	C9	C8
LSB	C7	C6	C5	C4	C3	C2	C1	UEN

DE : Display enable :
= 0, R = G = B = 0 and FBLK = FBK bit of display control register on the whole strip,
= 1, display of the characters.

CLU[3:0] : Active color selection at the begining of the strip.

C[9:1] : Address of the first character code of the strip.

UEN : UDC enable
0 : codes 240 to 254 (FOh to FEh) are read in ROM,
1 : codes 240 to 255 (FOh to FFh) are read in RAM (UDC).

FUNCTIONAL DESCRIPTION (continued)

III - Code Format

The codes of STV9427/28/29 are all single byte codes. There are basically 3 kinds of code :

- The control codes from 0 to 27 (00h to 1Bh) and from 224 to 239 (E0h to EFh).
- The ROM character codes from 32 to 223 (20h to DFh) and from 240 to 255 (F0h to FFh).
- The user definables characters codes from 240 to 254 (F0h to FFh).

Each row must begin with a displayable character code followed by a NOP or any control code.

For code definition see Table 4.

III.1 - Control Codes

Control codes must be followed by a displayable code (from 32 to 223), except for RTN & EOL. They must not be used twice consecutively without a displayable code between them.
The control code CALL is preceded by an address byte.
The control codes are not displayed except if mentioned.

***Code 0** (00h)* **:** NOP : no operation and no display is performed, can be used to spare a location in RAM for an active control code.

***Codes 1 to 7** (01h to 07h)* **:** SYMETRIES :
TSHS(01) Top Side Horizontal Symetry code displays the top half side of the following displayable code symetricaly to the bottom side.
BSHS(02) Bottom Side Horizontal Symetry code displays the bottom half side of the following displayable code symetricaly to the top side.
HFLIP(03) Horizontal Flip code flips horizontaly the following displayable code.
LSVS(04) Left Side Vertical Symetry code displays the left half side of the following displayable code symetricaly to the right side.
RSVS(05) Right Side Vertical symetry code displays the right half side of the following displayable code symetricaly to the left side.
VFLIP(06) Vertical Flip code flips verticaly the following displayable code.
HVFLIP(07) Horizontal & Vertical Flip code flips horizontaly and verticaly the following displayable code.

***Codes 8** (08h) (at odd @)* **:** RTN : return to the CALL + 1 code location (see Note).

***Code 09 to 14** (09h to 0Eh)* **:** Reserved

***Code 15** (0Fh)* **:** EOL, end of line terminates the display of the current row.

***Codes 16 to 23** (10h to 17h)* **:** COL0 to COL7 codes select 1 byte among 8 within the CLUT in RAM. The block selection is fixed by CLU3 bit of the active character descriptor (see Table 1 and Table 2).

***Codes 24 to 27** (18h to 19h)* **:** CALL, these control codes switch the display of the next character to the code address given by the next byte as following :

CALL CODE (odd @) MSB	0	0	0	1	1	0	0	A9
ADDRESS BYTE (even @) LSB	A8	A7	A6	A5	A4	A3	A2	A1

A[9:1] : Address of the next code to be used (A0 = 0 only even addresses).

Notes :
CALL and RTN code must be used twin. They cannot be nested.
CALL and RTN codes are displayed as a SPACE character.
CALL and RTN codes must be placed at odd addresses. They may be preceed by a NOP in order to place them at the right position.

***Codes 28 to 31** (1Ch to 1Fh)* **:** Reserved

***Code 224 to 239** (E0h to EFh)* **:** Accent shapes from 224 to 239 (E0h to EFh) are used combined with all other character codes 32 to 223 (10h to DFh) and placed before the target character.
The first set of accents, 224 to 231 (E0h to E7h) must be used with lower case letters. The 5 upper slices of the target character are replaced by the accent shape.
The second set of accents, 232 to 239 (E8h to EFh) must be used with the upper case letters (capital letters). The 3 upper slices of the target character are replaced by the accent shape. Accent code must always be followed by a displayable character or a space.

III.2 - ROM Character Codes

***Codes 32 to 223** (20h to DFh) and **Codes 240 to 254** (F0h to FEh)* : ROM character shapes are described as 12x18 pixel matrix as shown in Table 5.
It comprises 60 logos dedicated for monitor application (Horizontal position, keystone, ...), 25 characters for horizontal bar-graph and additional shapes.

FUNCTIONAL DESCRIPTION (continued)

Table 4

Code N°	MSB	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LSB	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NOP	COL0	Space	0	@	P	¢	p	Ç	Cont1	Hlin1	Box0	Bar5	Bar21	' dn	R
1	1	TSHS	COL1	!	1	A	Q	a	q	ç	Cont2	Hlin2	Box1	Bar6	Bar22	' up	G
2	2	BSHS	COL2	"	2	B	R	b	r	Æ	Bright	Kystn	Box2	Bar7	10o	^ dn	B
3	3	HFLIP	COL3	#	3	C	S	c	s	æ	Color	Kybal1	Box3	Bar8	1o0	x dn	1
4	4	LSVS	COL4	$	4	D	T	d	t	Ø	Spkr	Kybal2	Box4	Bar9	Indxrgt	~ dn	2
5	5	RSVS	COL5	%	5	E	U	e	u	ø	Mute	Pincus	Box5	Bar10	Indxup	° up	clock0
6	6	VFLIP	COL6	&	6	F	V	f	v	ß	Dgaus	Pinbal	Box6	Bar11	rtn	dot dn	clock1
7	7	HVFLIP	COL7	'	7	G	W	g	w	«	Balance	Tilt1	Box7	Bar12	hbar0	¨ dn	clock2
8	8	RTN	CALL	(	8	H	X	h	x	1/2	Vfcus	Tilt2	Box8	Bar13	hbar1	' up	A
9	9	-	CALL	±	9	I	Y	i	y	1/4	Hfcus	Cornr0	Box9	Bar14	vbar0	‘ up	E
10	A	-	-	*	:	J	Z	j	z	3/4	Vsz	Cornr1	Box10	Bar15	vbar1	^ up	T
11	B	-	-	+	;	K	[	k	{	≈	Vpos	Cornr2	Bar0	Bar16	treble	x up	S
12	C	-	-	,	<	L	®	l	|	≡	Vlin	Cornr3	Bar1	Bar17	bass	~ up	Z
13	D	-	-	-	=	M	©	m	<<	fh	Hsz	Cornr4	Bar2	Bar18	mic	° up	L
14	E	-	-	.	÷	N	¥	n	Arr lf	fv	Hpos1	kh	Bar3	Bar19	upidx0	dot up	D
15	F	EOL	-	/	?	O	_	o	Arr up	hz	Hpos2	hz	Bar4	Bar20	upidx1	¨ up	

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FUNCTIONAL DESCRIPTION (continued)

III.3 - User Definable Character Codes (UDC)

Codes 240 to 254 (F0h to FEh) refer to character shape loaded in RAM.

The STV9427/28/29 allows the user to dynamically define character(s) for his own needs (for a special LOGO for example). Like the ROM characters, a UDC is made of a 12 pixels x 18 slices dot matrix.

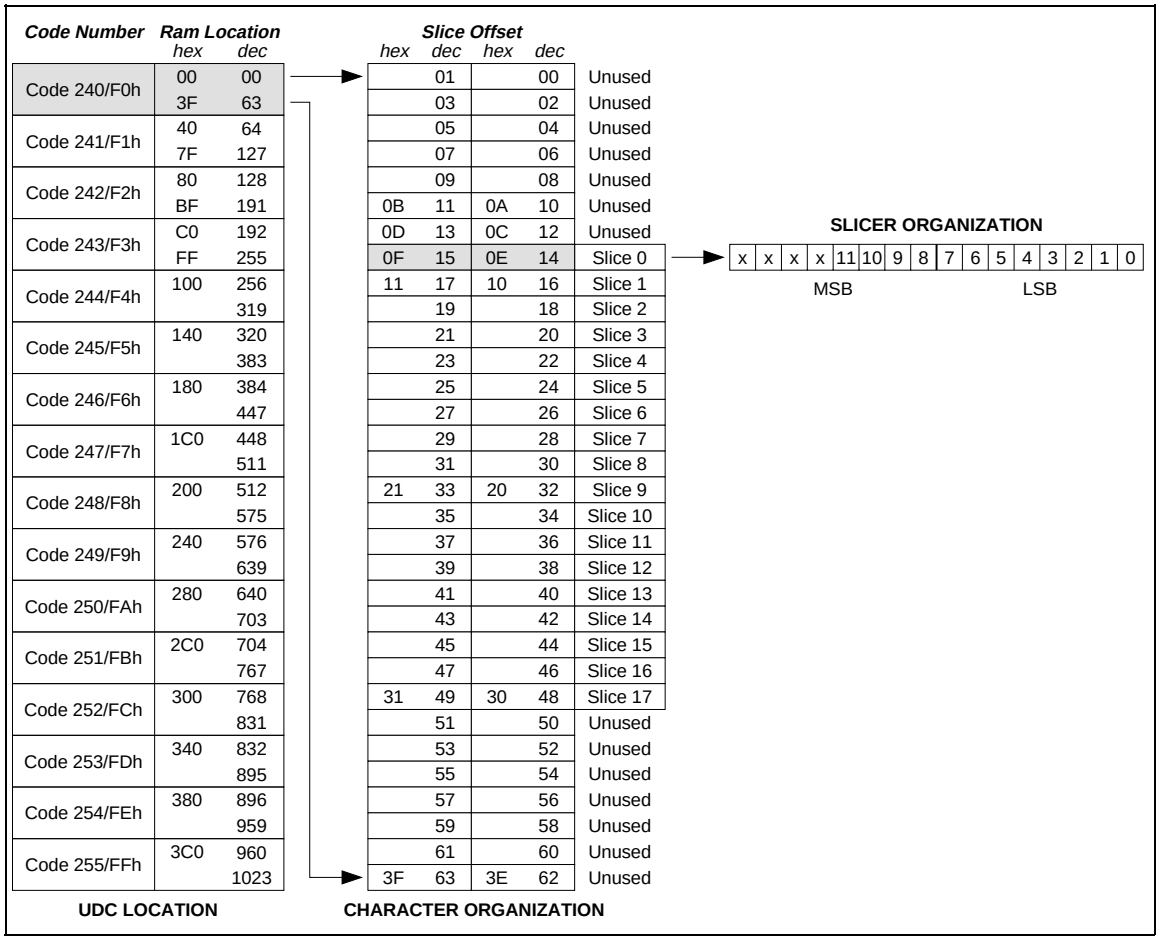
In a UDC, each pixel is defined with a bit, 1 refers to foreground, and 0 to background color. Each slice of a UDC uses 2 bytes :

add + 1	-	-	-	-	PX11	PX10	PX9	PX8
add (even)	PX7	PX6	PX5	PX4	PX3	PX2	PX1	PX0

PX11 is the left most pixel. Character slice address : SLICE ADDRESS = 64 (CHARACTER NUMBER - 240) + (SLICE NUMBER + 7) x 2.

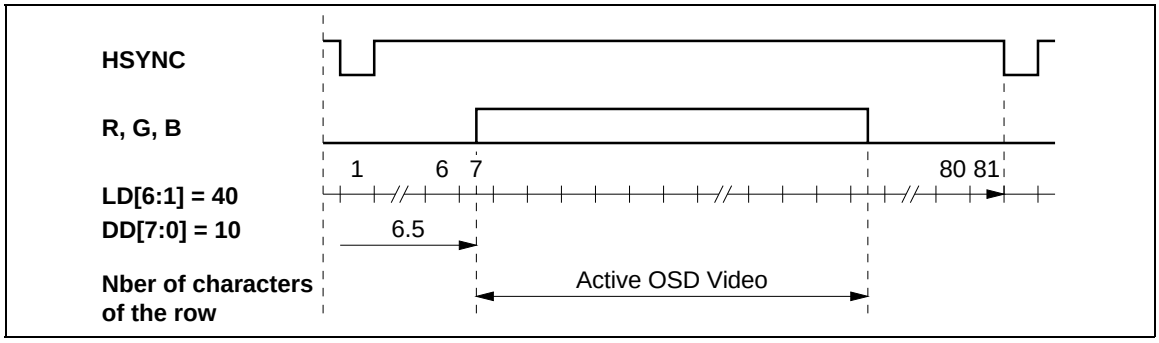
Where :
- CHARACTER NUMBER is the number given by the character code.
- SLICE NUMBER is the number given by the slice interpolator (n° of the current slice of the strip : 1 <<18).

Figure 6 : User Definable Character Codes



FUNCTIONAL DESCRIPTION (continued)

Figure 7 : Hozizontal Timing



IV - Clock and Timing

The whole timing is derived from the XTI and the horizontal SYNCHRO input frequencies. The XTI input frequency can be an external clock, crystal or a ceramic resonator signal thanks to XTI/XTO pins. The value of this frequency can be chosen between 6 and 15MHz is used by the PLL to generate a pixel clock locked on the horizontal synchro input signal.

IV.1 - Horizontal Timing (see Figure 7)

The number of pixel periods is given by the LINE DURATION register and is equal to :
[LD[6:1] x 2 + 1] x 12.
(LD[6:1] : value of the LINE DURATION register).
This value allows to define the horizontal size of the characters.

The horizontal left margin is given by the HORIZONTAL DELAY register and is equal to :
(DD[7:0] -6) x 6 + 54
(DD[7:0] : value of the DISPLAY DELAY register).
This value allows to define the horizontal position of the characters on the screen. Due to internal logic, minimum horizontal delay is fixed at 4.5 characters (54 pixel) when DD is even and lower or equal to 6, and it is fixed at 5 characters (60 pixel) when DD is odd and lower or equal to 7.

IV.2 - D to A Timing (STV9427)

The D/A converters of the STV9427 are pulse width modulator converter.

The frequency of the output signal is : $\frac{f_{XTAL}}{256 \times 6}$ and the duty cycle is : $\frac{Vi[7:0]}{256 \times 6}$ per cent.

After a low pass filter, the average value of the output is : $\frac{Vi\ [7:0]}{256 \times 6} \cdot V_{DD}$

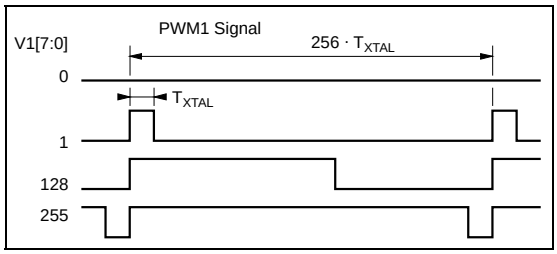
V - Display Control

A screen is composed of successive scanlines gathered in several strips. Each strip is defined by a descriptor stored in memory. A table of descriptors allows screen composition and different tables can be stored in memory at the page addresses (16 possible ≠ addresses). Two types of strips are available :

- Spacing strip : its descriptor (see II) gives the number of black (FBK = 1 in DISPLAY CONTROL register) or transparent (FBK = 0) lines.
- Character strip : its descriptor gives the memory address of the character codes corresponding to the 1st displayed character. The characters and attributes (see code format III) are defined by a succession of codes stored in the RAM at addresses starting from the 1st one given by the descriptor. A character strip can be displayed or not by using the DE bit of its descriptor.

After the VSYNC edge, the first strip descriptor is read at the top of the current table of descriptors at the address given by P[9:0] (see DISPLAY CONTROL register) ; if it is a spacing strip, SL[7:0] black or transparent scan lines are displayed ; if it is a character strip, during CH[5:0] scan lines (CH[5:0] given by the CHARACTER HEIGHT register), the character codes are read at the addresses starting from the 1st one given by the descriptor until a end of line character or the end of the scan line ; the next descriptor is then read and the same process is repeated until the next edge of VSYNC.

Figure 8 : PWM Timing



FUNCTIONAL DESCRIPTION (continued)

Figure 9 : Relation between Screen/Address Page/Character Code in RAM

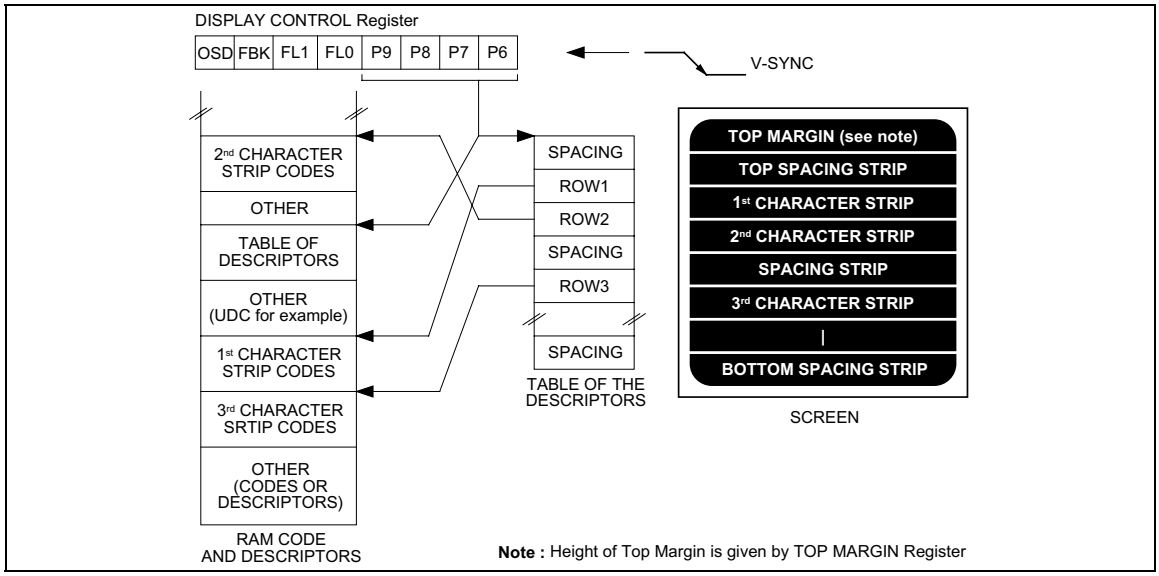
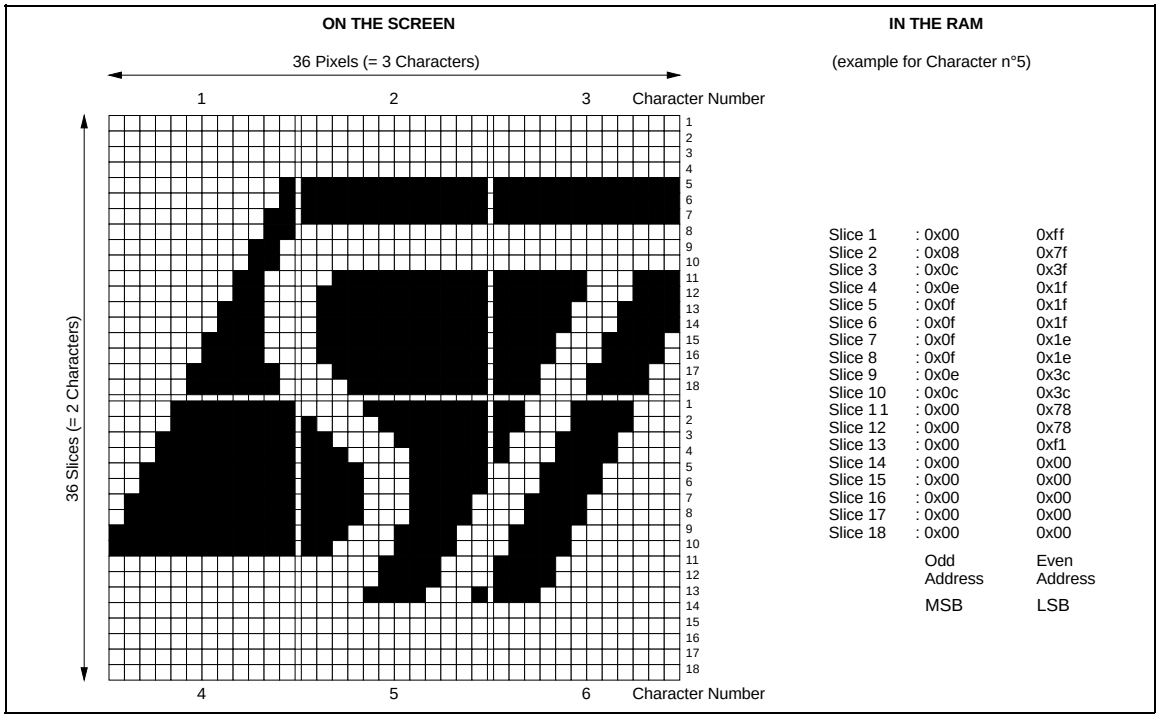
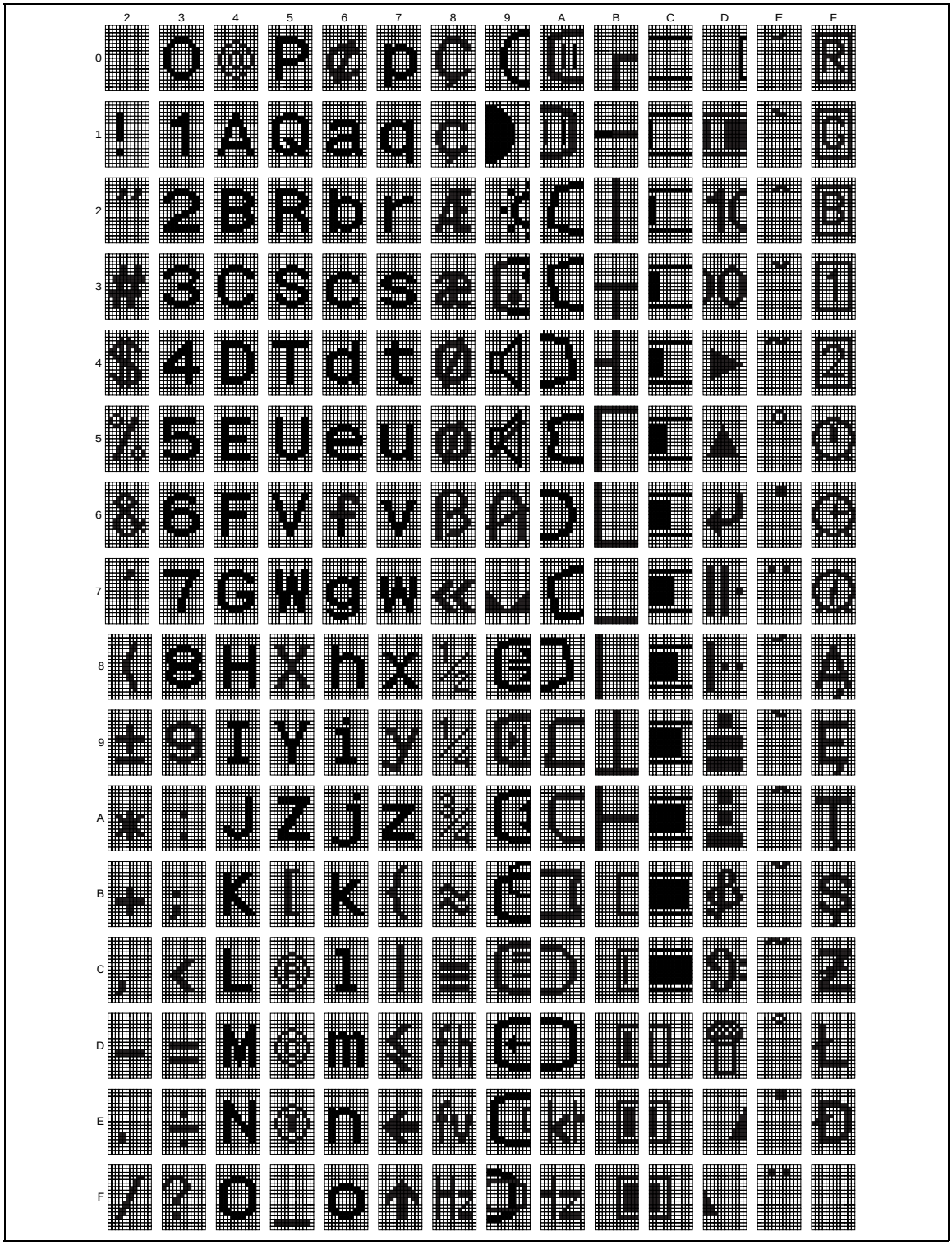


Figure 10 : User Definable Character



FUNCTIONAL DESCRIPTION (continued)

Table 5 : ROM Character Generator



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FUNCTIONAL DESCRIPTION (continued)

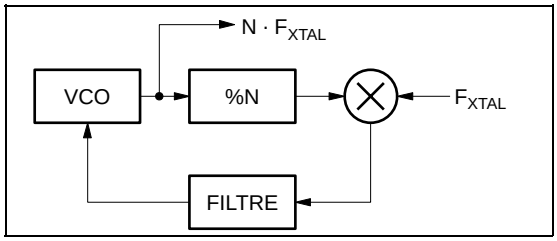
VI - PLL

The PLL function of the STV9427/28/29 provides the internal pixel clock locked on the horizontal synchro signal and used by the display processor to generate the R, G, B and fast blancking signals. It is made of 2 PLLs. The first one analogic (see Figure 11), provides a high frequency signal locked on the crystal frequency. The frequency multiplier is given by :

$N = 2 \cdot (FM[3:0] + 3)$

Where FM[3:0] is the value of the FREQUENCY MULTIPLIER register.

Figure 11 : Analogic PLL

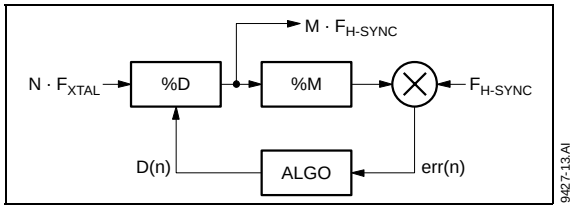


The second PLL, full digital (see Figure 12), provides a pixel frequency locked on the horizontal synchro signal. The ratio between the frequencies of these 2 signals is :

$M = 12 \times (LD[6:1] \times 2 + 1)$

Where LD[6:1] is the value of the LINE DURATION register.

Figure 12 : Digital PLL



VI.1 - Programming of the PLL Registers

Frequency Multiplier (@3FF8)

This register gives the ratio between the crystal frequency and the high frequency of the signal used by the 2nd PLL to provide, by division, the pixel clock. The value of this high frequency must be near to 200MHz (for example if the crystal is a 8MHz, the value of FM must be equal to 10) and greater than 2.5 x (pixel frequency). The frequency of VCO must stand within limits given below :

$$F_{pxlmin} \times 16 \geq F_{VCO} \geq F_{pxlmax} \times 2.5$$

Initial Pixel Period (@3FF7)

This register allows to increase the speed of the convergence of the PLL when the horizontal frequency changes (new graphic standart). The relationship between FM[3:0], PP[7:0], LD[6:1], f_{HSYNC} and f_{XTAL} is :

$$PP[7:0] = \text{round}\left(8 \cdot \frac{2 \cdot (FM[3:0] + 3) \cdot F_{XTAL}}{6 \cdot (LD[6:1] \cdot 2 + 1) \cdot F_{HSYNC}} - 24\right)$$

Locking Condition Time Constant (@ 3FF5)

This register gives the constants AS[2:0] and BS[2:0] used by the algo part of the PLL (see Figure 11) to calculate, from the phase error, err(n), the new value, D(n), of the division of the high frequency signal to provide the pixel clock. These two constants are used only in locking condition, which is true, if the phase error is less than a fixed value during at least, 4 scan lines. If the phase error becomes greater than the fixed value, the PLL is not in locking condition but in capture process. In this case, the algo part of the PLL used the other constants, AF[2:0] and BF[2:0], given by the next register.

Capture Process Time Constant (@ 3FF6)

The choice between these two time constants (locking condition or capture process) allows to decrease the capture process time by changing the time response of the PLL.

FUNCTIONAL DESCRIPTION (continued)

VI.2 - How to choose the value of the time constant ?

The time response of the PLL is given by its characteristic equation which is :

$$(x-1)^2 + (\alpha+\beta)\cdot(x-1) + \beta = 0.$$

Where :

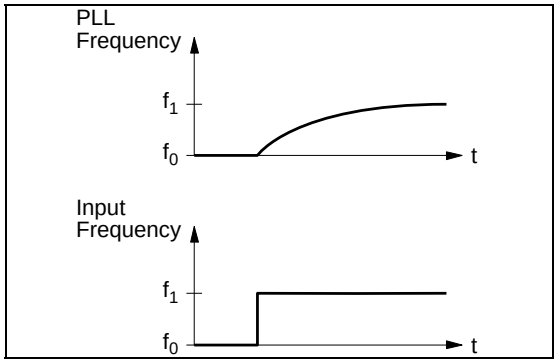
$\alpha = 3 \cdot LD[6:1] \cdot 2^{A-11}$ and $\beta = 3 \cdot LD[6:1] \cdot 2^{B-19}$.

(LD[6:1] = value of the LINE DURATION register, A = value of the 1st time constant, AF or AS and B = value of the 2d time constant, BF or BS).

As you can see, the solution depend only on the LINE DURATION and the TIME CONSTANTS given by the I^2C registers.

If $(\alpha+\beta)^2 - 4\beta \geq 0$ and $2\alpha - \beta < 4$, the PLL is stable and its response is like this presented on Figure 13.

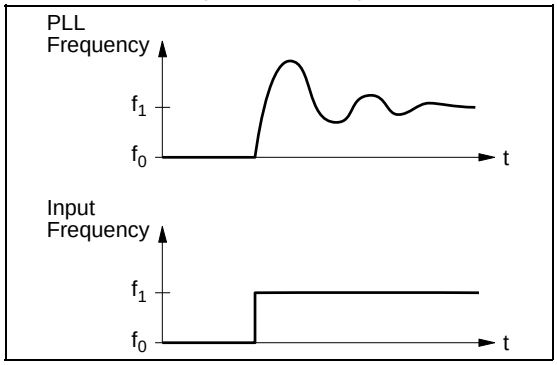
Figure 13 : Time Response of the PLL/Characteristic Equation Solutions (with real solutions)



If $(\alpha+\beta)^2 - 4\beta \leq 0$, the response of the PLL is like this presented on Figure 14.

In this case the PLL is stable if $\tau > 0.7$ damping coefficient).

Figure 14 : Time Response of the PLL/Characteristic Equation Solutions (with Complex Solutions)



The Table 6 gives some good values for A and B constants for different values of the LINE DURATION.

Summary

For a good working of the PLL :

- A and B time constants must be chosen among values for which the PLL is stable,
- B must be equal or greater than A and the difference between them must be less than 3,
- The greater (A, B) are, the faster the capture is.

An optimal choice for the most of applications might be :

- For locking condition : AS = 0 and BS = 1,
- For capture process : AF = 2 and BF = 4.

But for each application the time constants can be calculated by solving the characteristic equation and choosing the best response.

Table 6 : Valid Time Constants Examples

B \ A	0	1	2	3	4	5	6
0	YYYY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
1	YYYY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
2	NYYY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
3	NNNY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
4	NNNN	NYYY(1)	YYYY	YYYN	YNNN	NNNN	NNNN
5	NNNN	NNNY	YYYY	YYYN	YNNN	NNNN	NNNN
6	NNNN	NNNN	NYYY	YYYN	YNNN	NNNN	NNNN
7	NNNN	NNNN	NNNY	YYYN	YNNN	NNNN	NNNN

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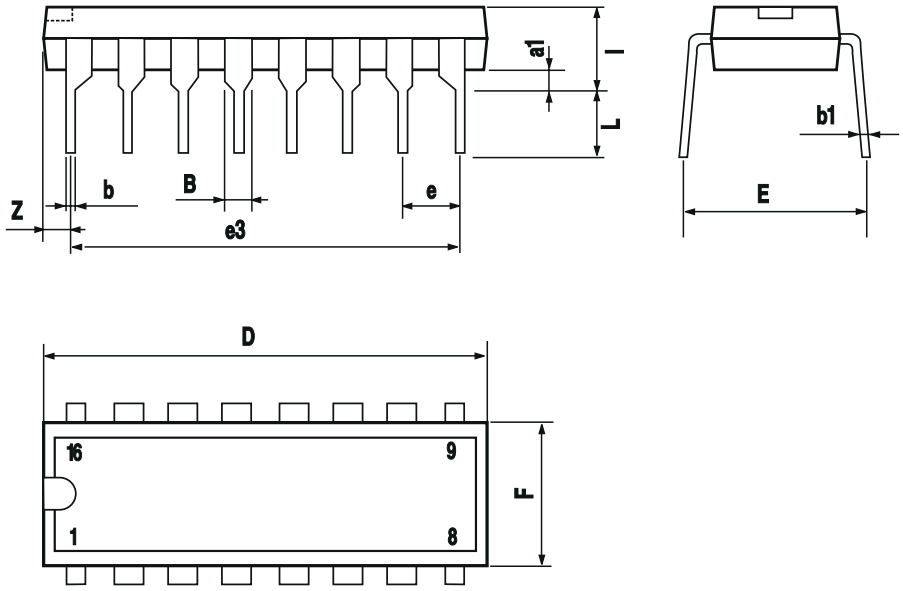
Note 1 : Case of A[2:0] = 1 (001) and B[2:0] = 4 (100) :

LD	16	32	48	64
Valid Time Constants	N	Y	Y	Y

Value of LINE DURATION Register (@ 3FF0) :
LD = 16 :LD[6:0] = 0010000, LD[6:1] = 001000
LD = 32 :LD[6:0] = 0100000
LD = 48 :LD[6:0] = 0110000
LD = 64 :LD[6:0] = 1000000, LD[6:1] = 100000.
Table meaning : N = No possible capture - No stability
Y = PLL can lock

PACKAGE MECHANICAL DATA (STV9427)
16 PINS - PLASTIC DIP

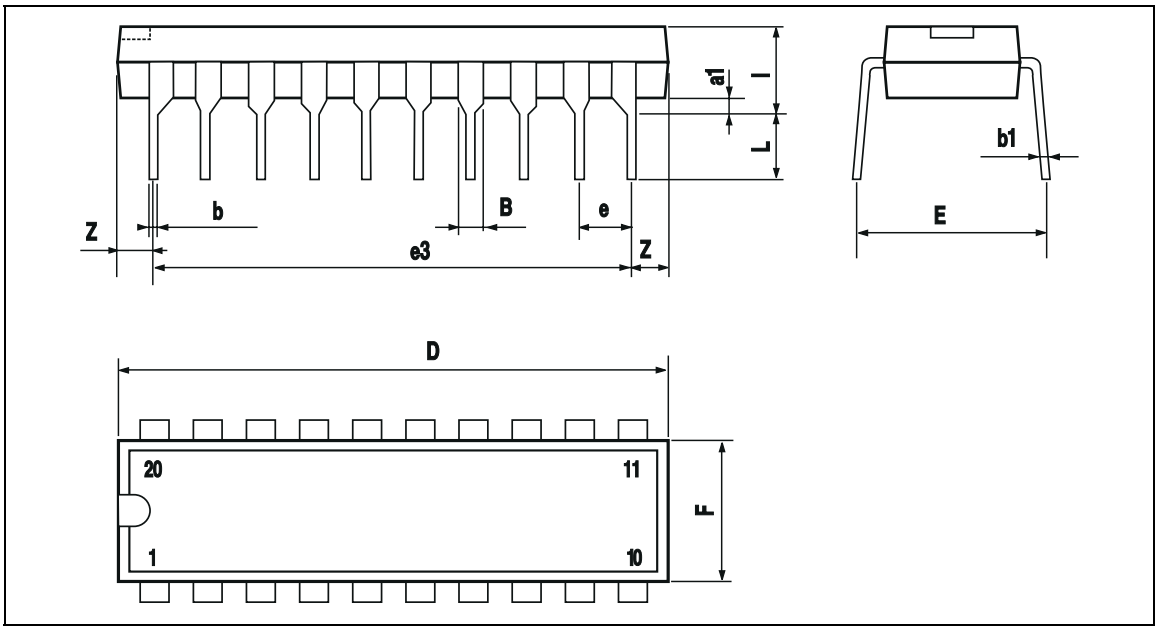


PM-DIP16.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

DIP16.TBL

PACKAGE MECHANICAL DATA (STV9428)
20 PINS - PLASTIC DIP

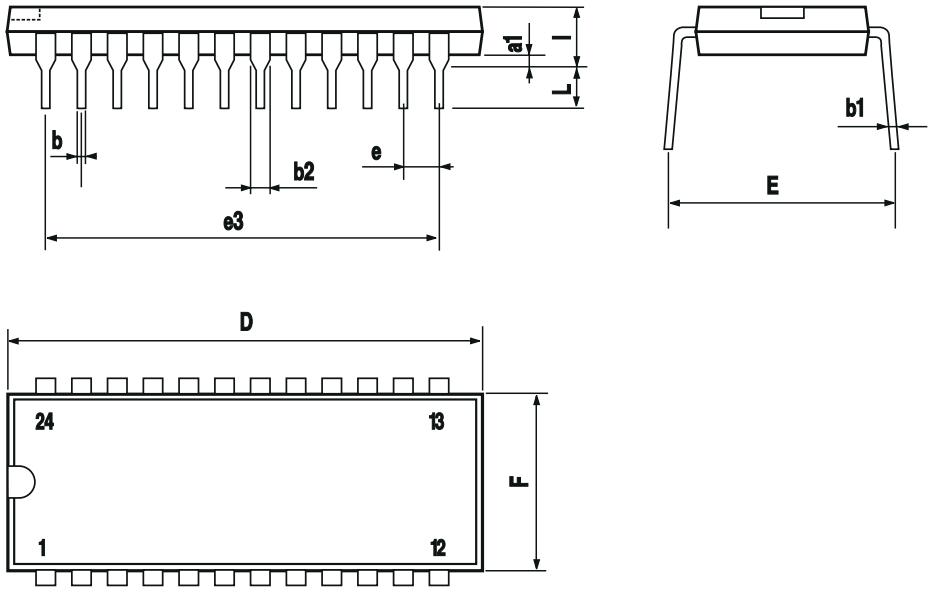


PM-DIP20.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

DIP20.TBL

PACKAGE MECHANICAL DATA (STV9429)
24 PINS - PLASTIC DIP



PM-DIP24.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

DIP24.TBL