TDA9115

LOW-COST I²C CONTROLLED DEFLECTION PROCESSOR FOR MULTISYNC MONITOR

FEATURES

General

- I²C-BUS-CONTROLLED DEFLECTION PROCESSOR DEDICATED FOR LOW-END CRT MONITORS
- SINGLE SUPPLY VOLTAGE 12V
- VERY LOW JITTER
- DC/DC CONVERTER CONTROLLER
- ADVANCED EW DRIVE
- AUTOMATIC MULTISTANDARD SYNCHRONIZATION
- DYNAMIC CORRECTION WAVEFORM OUTPUT
- X-RAY PROTECTION AND SOFT-START & STOP ON HORIZONTAL AND DC/DC DRIVE OUTPUTS

Horizontal section

- 150 kHz maximum frequency
- Corrections of geometric asymmetry: Pin cushion asymmetry, Parallelogram
- Tracking of asymmetry corrections with vertical size and position
- Horizontal moiré cancellation output

Vertical section

- 200 Hz maximum frequency
- Vertical ramp for DC-coupled output stage with adjustments of: C-correction, S-correction for super-flat CRT, Vertical size, Vertical position
- Vertical moiré cancellation through vertical ramp waveform
- Compensation of vertical breathing with EHT variation

EW section

- Symmetrical geometry corrections: Pin cushion, Keystone
- Horizontal size adjustment
- Tracking of EW waveform with Vertical size and position and adaptation to frequency
- Compensation of horizontal breathing through EW waveform

Dynamic correction section

- Vertical dynamic correction waveform output for dynamic corrections like focus, brightness uniformity, ...
- Fixed on screen by means of tracking system

DC/DC controller section

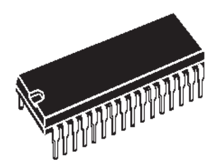
- Step-up and step-down conversion modes
- External sawtooth configuration
- Synchronization on hor. frequency with phase selection
- Selectable polarity of drive signal

DESCRIPTION

The TDA9115 is a monolithic integrated circuit assembled in a 32-pin shrink dual-in-line plastic package. This IC controls all the functions related to horizontal and vertical deflection in multimode or multi-frequency computer display monitors.

The device only requires very few external components.

Combined with other ST components dedicated for CRT monitors (microcontroller, video preamplifier, video amplifier, OSD controller) the TDA9115 allows fully I²C bus-controlled computer display monitors to be built with a reduced number of external components.



SHRINK 32 (Plastic Package)
ORDER CODE: TDA9115

Version 4.0

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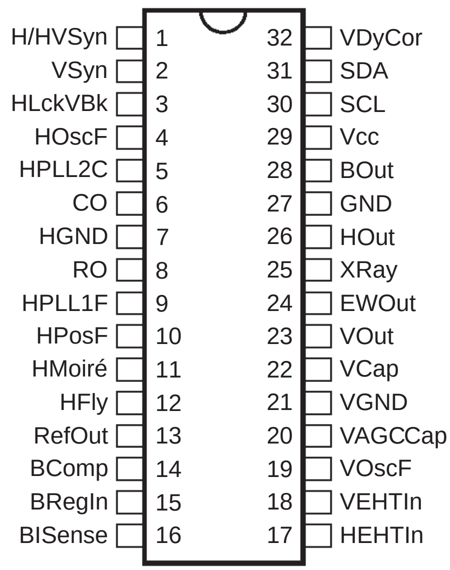
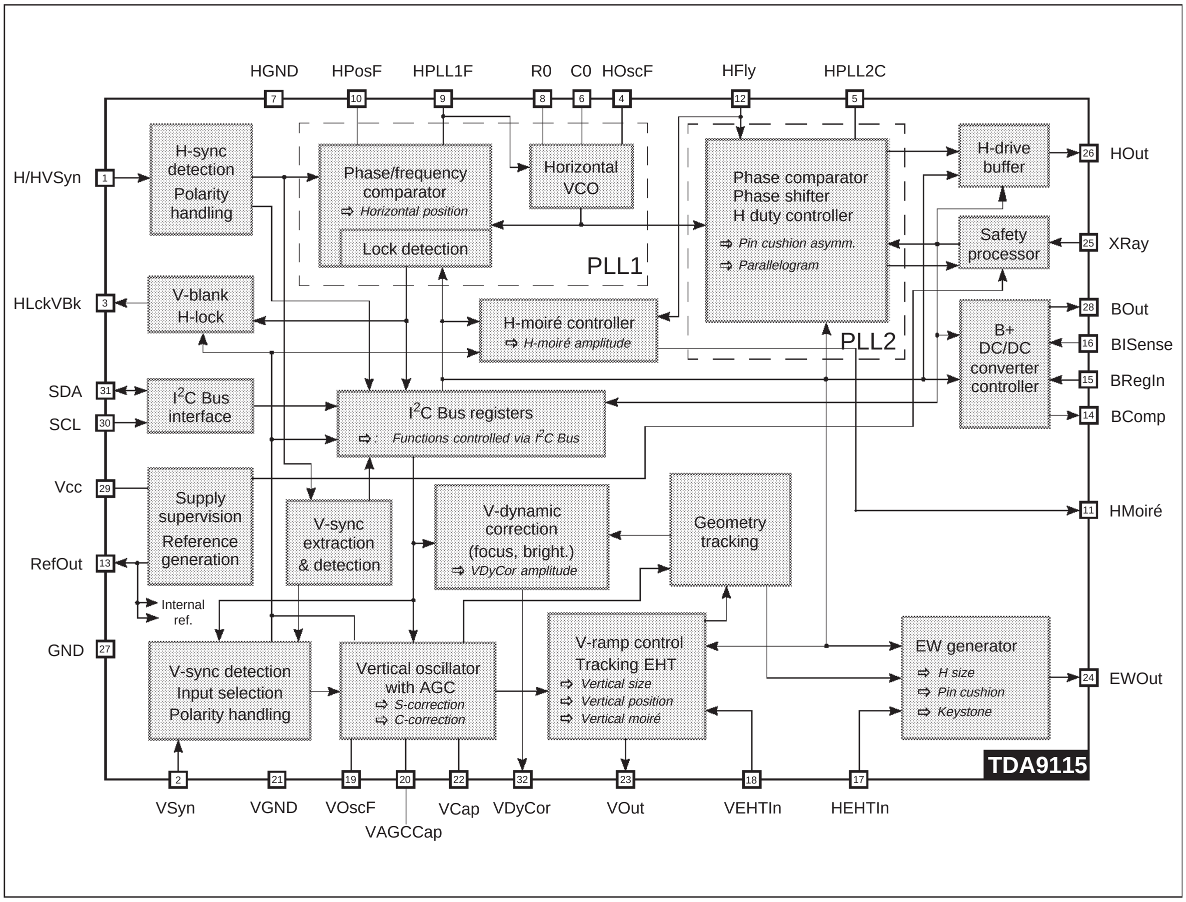
1 - PIN CONFIGURATION



2 - BLOCK DIAGRAM



3 - PIN FUNCTION REFERENCE

Pin	Name	Function
1	H/HVSyn	TTL compatible **H**orizontal **/ H**orizontal and **V**ertical **Syn**c. input
2	VSyn	TTL compatible **V**ertical **Syn**c. input
3	HLckVBk	**H**orizontal PLL1 **L**o**ck** detection and **V**ertical early **B**lan**k**ing composite output
4	HOscF	High **H**orizontal **Osc**illator sawtooth threshold level **F**ilter input
5	HPLL2C	**H**orizontal **PLL2** loop **C**apacitive filter input
6	CO	Horizontal **O**scillator **C**apacitor input
7	HGND	**H**orizontal section **G**rou**ND**
8	RO	Horizontal **O**scillator **R**esistor input
9	HPLL1F	**H**orizontal **PLL1** loop **F**ilter input
10	HPosF	**H**orizontal **Pos**ition **F**ilter and soft-start time constant capacitor input
11	HMoiré	**H**orizontal **Moiré** cancellation output
12	HFly	**H**orizontal **Fly**back input
13	RefOut	**Ref**erence voltage **Out**put
14	BComp	**B**+ DC/DC error amplifier (**Comp**arator) output
15	BRegIn	**Reg**ulation feedback **In**put of the **B**+ DC/DC converter controller
16	BISense	**B**+ DC/DC converter current (**I**) **Sense** input
17	HEHTIn	**In**put for compensation of **H**orizontal amplitude versus **EHT** variation
18	VEHTIn	**In**put for compensation of **V**ertical amplitude versus **EHT** variation
19	VOscF	**V**ertical **Osc**illator sawtooth low threshold **F**ilter (capacitor to be connected to VGND)
20	VAGCCap	Input for storage **Cap**acitor for **A**utomatic **G**ain **C**ontrol loop in **V**ertical oscillator
21	VGND	**V**ertical section **G**rou**ND**
22	VCap	**V**ertical sawtooth generator **Cap**acitor
23	VOut	**V**ertical deflection drive **Out**put for a DC-coupled output stage
24	EWOut	**E/W Out**put
25	XRay	**X**-**Ray** protection input
26	HOut	**H**orizontal drive **Out**put
27	GND	Main **G**rou**ND**
28	BOut	**B**+ DC/DC converter controller **Out**put
29	Vcc	Supply voltage
30	SCL	I^2C bus **S**erial **CL**ock Input
31	SDA	I^2C bus **S**erial **DA**ta input/output
32	VDyCor	**V**ertical **Dy**namic **Cor**rection output

4 - QUICK REFERENCE DATA

Characteristic	Value	Unit
General		
Package	SDIP 32	
Supply voltage	12	V
Supply current	55	mA
Application category	Low-end	
Means of control/Maximum clock frequency	I^2C Bus/400	kHz
EW drive	Yes	
DC/DC convertor controller	Yes	
Horizontal section		
Frequency range	15 to 150	kHz
Autosync frequency ratio (can be enlarged in application)	4.28	
Positive/Negative polarity of horizontal sync signal/Automatic adaptation	Yes/Yes/Yes	
Duty cycle of the drive signal	48	%
Position adjustment range with respect to H period	±11	%
Soft start/Soft stop feature	Yes/Yes	
Hardware/Software PLL lock indication	Yes/No	
Parallelogram	Yes	
Pin cushion asymmetry correction (also called Side pin balance)	Yes	
Top/Bottom/Common corner asymmetry correction	No/No/No	
Tracking of asymmetry corrections with vertical size & position	Yes	
Horizontal moiré cancellation (ext.) for Combined/Separated architecture	Yes/Yes	
Vertical section		
Frequency range	35 to 200	Hz
Autosync frequency range (150nF at VCap and 470nF at VAGCCap)	50 to 180	Hz
Positive/Negative polarity of vertical sync signal/Automatic adaptation	Yes/Yes/Yes	
S-correction/C-correction/Super-flat tube characteristic	Yes/Yes/Yes	
Vertical size/Vertical position adjustment	Yes/Yes	
Vertical moiré cancellation (internal)	Yes	
Vertical breathing compensation	Yes	
EW section		
Pin cushion correction	Yes	
Keystone correction	Yes	
Top/Bottom/Common corner correction	No/No/No	
Horizontal size adjustment	Yes	
Tracking of EW waveform with Frequency/Vertical size & position	Yes/Yes	
Breathing compensation on EW waveform	Yes	
Dynamic correction section (dyn. focus, dyn. brightness,...)		
Vertical dynamic correction output VDyCor	Yes	
Horizontal dynamic correction output	No	
Composite HV dynamic correction output	No	
Tracking of horizontal waveform with Horizontal size/EHT	No/No	
Tracking of vertical waveform with V. size & position	Yes	
DC/DC controller section		
Step-up/Step-down conversion mode	Yes/Yes	
Internal/External sawtooth configuration	No/Yes	
Bus-controlled output voltage	No	
Soft start/Soft stop feature	Yes/Yes	
Positive(N-MOS)/Negative(P-MOS) polarity of BOut signal	Yes/Yes	

5 - ABSOLUTE MAXIMUM RATINGS

All voltages are given with respect to ground.

Currents flowing from the device (sourced) are signed negative. Currents flowing to the device are signed positive.

Symbol	Parameter	Value		Unit
		Min	Max	
V_{CC}	Supply voltage (pin Vcc)	-0.4	13.5	V
$V_{(pin)}$	Pins HEHTIn, VEHTIn, XRay, HOut, BOut Pins H/HVSyn, VSyn, SCL, SDA Pins HLckVBk, CO, RO, HPLL1F, HPosF, HMoiré, BRegIn, BI-Sense, VAGCCap, VCap, VDyCor, HOscF, VOscF Pin HPLL2C Pin HFly	-0.4 -0.4 -0.4 -0.4 -0.4	V_{CC} 5.5 V_{RefO} $V_{RefO}/2$ V_{RefO}	V V V V V
V_{ESD}	ESD susceptibility (human body model: discharge of 100pF through 1.5kΩ)	-2000	2000	V
T_{stg}	Storage temperature	-40	150	°C
T_j	Junction temperature		150	°C

6 - ELECTRICAL PARAMETERS AND OPERATING CONDITIONS

Medium (middle) value of an I^2C Bus control or adjustment register composed of bits D0, D1,...,Dn is the one having Dn at "1" and all other bits at "0". Minimum value is the one with all bits at 0, maximum value is the one with all at "1".

Currents flowing from the device (sourced) are signed negative. Currents flowing to the device are signed positive.
T_H is period of horizontal deflection.

6.1 THERMAL DATA

Symbol	Parameter	Value			Unit
T_{amb}	Operating ambient temperature	0		70	°C
$R_{th(j-a)}$	Junction-ambience thermal resistance		65		°C/W

6.2 SUPPLY AND REFERENCE VOLTAGES

T_{amb} = 25°C

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{CC}	Supply voltage at Vcc pin		10.8	12	13.2	V
I_{CC}	Supply current to Vcc pin	V_{CC} = 12V		55		mA
V_{RefO}	Reference output voltage at RefOut pin	V_{CC} = 12V, I_{RefO}= -2mA	7.4	8	8.6	V
I_{RefO}	Current sourced by RefOut output		-5		0	mA

6.3 SYNCHRONIZATION INPUTS

Vcc = 12V, T_{amb} = 25°C

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$V_{LoH/HVSyn}$	LOW level voltage on H/HVSyn		0		0.8	V
$V_{HiH/HVSyn}$	HIGH level voltage on H/HVSyn		2.2		5	V
V_{LoVSyn}	LOW level voltage on VSyn		0		0.8	V
V_{HiVSyn}	HIGH level voltage on VSyn		2.2		5	V
R_{PdSyn}	Internal pull-down on H/HVSyn, VSyn		100	175	250	kΩ
$t_{PulseHSyn}$	H sync. pulse duration on H/HVSyn pin		0.5			µs
$t_{PulseHSyn}/T_H$	Proportion of H sync pulse to H period	Pin H/HVSyn			0.2	
$t_{PulseVSyn}$	V sync. pulse duration	Pins H/HVSyn, VSyn	0.5		750	µs
$t_{PulseVSyn}/T_V$	Proportion of V sync pulse to V period	Pins H/HVSyn, VSyn			0.15	
t_{extrV}/T_H	Proportion of sync pulse length to H period for extraction as V sync pulse	Pin H/HVSyn, cap. on pin CO = 820pF	0.21	0.3		
$t_{HPolDet}$	Polarity detection time (after change)	Pin H/HVSyn	0.75			ms

6.4 HORIZONTAL SECTION

Vcc = 12V, T_{amb} = 25°C

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
PLL1						
I_{RO}	Current load on RO pin				1.5	mA
C_{CO}	Capacitance on CO pin		390			pF
f_{HO}	Frequency of hor. oscillator				150	kHz
$f_{HO(0)}$	Free-running frequency of hor. oscill. (1)	R_{RO}=5.23kΩ, C_{CO}=820pF	27	28.5	29.9	kHz
f_{HOCapt}	Hor. PLL1 capture frequency (4)	$f_{HO(0)}$ = 28.5kHz	29		122	kHz
$\frac{\Delta f_{HO(0)}}{f_{HO(0)} \cdot \Delta T}$	Temperature drift of free-running freq. (3)			-150		ppm/°C
$\Delta f_{HO}/\Delta V_{HO}$	Average horizontal oscillator sensitivity	$f_{HO(0)}$ = 28.5kHz		19.6		kHz/V
V_{HO}	H. oscill. control voltage on pin HPLL1F	V_{RefO}=8V	1.4		6.0	V
$V_{HOThrfr}$	Threshold on H. oscill. control voltage on HPLL1F pin for tracking of EW with freq.	V_{RefO}=8V		5.0		V
V_{HPosF}	Control voltage on HPosF pin	*HPOS* (Sad01): 11111111b 10000000b 00000000b	 2.60 3.30 3.85	 2.8 3.4 4.0	 3.05 3.55 4.15	 V V V
$V_{HOThrLo}$	Bottom of hor. oscillator sawtooth(6)			1.6		V
$V_{HOThrHi}$	Top of hor. oscillator sawtooth(6)			6.4		V
PLL2						
$R_{In(HFly)}$	Input impedance on HFly input (2)	$V_{(HFly)} > V_{ThrHFly}$	300	500	700	Ω
I_{InHFly}	Current into HFly input	At top of H flyback pulse			5	mA
$V_{ThrHFly}$	Voltage threshold on HFly input		0.6	0.7		V
$V_{S(0)}$	H flyback lock middle point(6)	No PLL2 phase modulation		4.0		V
$V_{BotHPLL2C}$	Low clamping voltage on HPLL2C pin(5)			1.6		V
$V_{TopHPLL2C}$	High clamping voltage on HPLL2C pin(5)		3.75	4.0	4.25	V
$t_{ph}(min)/T_H$	Min. advance of H-drive OFF before middle of H flyback(7)	Null asym. correction		0		%
$t_{ph}(max)/T_H$	Max. advance of H-drive OFF before middle of H flyback(8)	Null asym. correction		44		%
H-drive output on pin HOut						
I_{HOut}	Current into HOut output	Output driven LOW			30	mA
t_{Hoff}/T_H	Duty cycle of H-drive signal	 Soft-start/Soft-stop value		48 85		% %
Picture geometry corrections through PLL1 & PLL2						
t_{Hph}/T_H	H-flyback (center) static phase vs. sync signal (via PLL1), see Figure 7	*HPOS* (Sad01): 11111111b 00000000b		 +11 -11		 % %

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
t_{PCAC}/T_H	Contribution of pin cushion asymmetry correction to phase of H-drive vs. static phase (via PLL2), measured in corners (9	*PCAC* (Sad11h) full span *VPOS* at medium *VSIZE* at minimum *VSIZE* at medium *VSIZE* at maximum		 ±1.0 ±1.8 ±2.8		 % % %
t_{ParalC}/T_H	Contribution of parallelogram correction to phase of H-drive vs. static phase (via PLL2), measured in corners (9)	*PARAL* (Sad12h) full span *VPOS* at medium *VSIZE* at minimum *VSIZE* at medium *VSIZE* at maximum *VPOS* at max. or min. *VSIZE* at minimum		 ±1.75 ±2.2 ±2.8 ±1.75		 % % % %

Note 1: Frequency at no sync signal condition. For correct operation, the frequency of the sync signal applied must always be higher than the free-running frequency. The application must consider the spread of values of real electrical components in R_{RO} and C_{CO} positions so as to always meet this condition. The formula to calculate the free-running frequency is $f_{HO(0)}=0.12125/(R_{RO}\ C_{CO})$

Note 2: Base of NPN transistor with emitter to ground is internally connected on pin HFly through a series resistance of about 500Ω and a resistance to ground of about 20kΩ.

Note 3: Evaluated and figured out during the device qualification phase. Informative. Not tested on every single unit.

Note 4: This capture range can be enlarged by external circuitry.

Note 5: The voltage on HPLL2C pin corresponds to immediate phase of leading edge of H-drive signal on HOut pin with respect to internal horizontal oscillator sawtooth. It must be between the two clamping levels given. Voltage equal to one of the clamping values indicates a marginal operation of PLL2 or non-locked state.

Note 6: Internal threshold. See Figure 7.

Note 7: The $t_{ph}(min)/T_H$ parameter is fixed by the application. For correct operation of asymmetry corrections through dynamic phase modulation, this minimum must be increased by maximum of the total dynamic phase required in the direction leading to bending of corners to the left. Marginal situation is indicated by reach of $V_{TopHPLL2C}$ high clamping level by waveform on pin HPLL2C. Also refer to Note 5 and Figure 7.

Note 8: The $t_{ph}(max)/T_H$ parameter is fixed by the application. For correct operation of asymmetry corrections through dynamic phase modulation, this maximum must be reduced by maximum of the total dynamic phase required in the direction leading to bending of corners to the right. Marginal situation is indicated by reach of $V_{BotHPLL2C}$ low clamping level by waveform on pin HPLL2C. Also refer to Note 5 and Figure 7 .

Note 9: All other dynamic phase corrections of picture asymmetry set to their neutral (medium) positions.

6.5 VERTICAL SECTION

V_{CC} = 12V, T_{amb} = 25°C

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
AGC-controlled vertical oscillator sawtooth; V_{RefO} = 8V						
$R_{L(VAGCCap)}$	Ext. load resistance on VAGCCap pin(10)	$\Delta V_{amp}/V_{amp}(R=\infty) \leq 1\%$	65			MΩ
V_{VOB}	Sawtooth bottom voltage on VCap pin(11)	No load on VOscF pin(11)	1.8	1.9	2.0	V
V_{VOT}	Sawtooth top voltage on VCap pin	AGC loop stabilized V sync present No V sync		 5 4.9		 V V
t_{VODis}	Sawtooth Discharge time	C_{VCap}=150nF		80		µs
$f_{VO(0)}$	Free-running frequency	C_{VCap}=150nF		100		Hz
f_{VOCapt}	AGC loop capture frequency	C_{VCap}=150nF	50		185	Hz
$\frac{\Delta V_{VOdev}}{V_{VOamp}}$(16)	Sawtooth non-linearity(12)	AGC loop stabilized, (12)		0.5		%
$\frac{\Delta V_{VOS-cor}}{V_{VOamp}}$	S-correction range	AGC loop stabilized, (13) t_{VR}=1/4 T_{VR}(15) t_{VR}=3/4 T_{VR}		 -5 +5		 % %
$\frac{\Delta V_{VOC-cor}}{V_{VOamp}}$	C-correction range	AGC loop stabilized, (14) t_{VR}=1/2 T_{VR}(15) *CCOR*(Sad0A): x0000000b x1000000b x1111111b		 -3 0 +3		 % % %
$\frac{\Delta V_{VOamp}}{V_{VOamp} \cdot \Delta f_{VO}}$	Frequency drift of sawtooth amplitude(17)(18)	AGC loop stabilized $f_{VOCapt(min)} \leq f_{VO} \leq f_{VOCapt(max)}$		200		ppm/Hz
Vertical output drive signal (on pin VOut); V_{RefO} = 8V						
$V_{mid(VOut)}$	Middle point on VOut sawtooth	*VPOS* (Sad08): x0000000b x1000000b x1111111b	 3.65	 3.2 3.5 3.8	 3.3	 V V V
V_{amp}	Amplitude of VOut sawtooth (peak-to-peak voltage)	*VSIZE* (Sad07): x0000000b x1000000b x1111111b	 3.5	 2.25 3.0 3.75	 2.5	 V V V
$V_{offVOut}$	Level on VOut pin at V-drive "off"	I^2Cbit VOutEn at 0		3.8		V
I_{VOut}	Current delivered by VOut output		-5		5	mA
V_{VEHT}	Control input voltage range on VEHTIn pin		1		V_{RefO}	V
$\frac{\Delta V_{amp}}{V_{amp} \cdot \Delta V_{VEHT}}$	Breathing compensation	$V_{VEHT} > V_{RefO}$ $V_{VEHT(min)} \leq V_{VEHT} \leq V_{RefO}$		0 2.5		%/V %/V

Note 10: Value of acceptable cumulated parasitic load resistance due to humidity, AGC storage capacitor leakage, etc., for less than 1% of V_{amp} change.

Note 11: The threshold for V_{VOB} is generated internally and routed to VOscF pin. Any DC current on this pin will influence the value of V_{VOB}.

Note 12: Maximum of deviation from an ideally linear sawtooth ramp at null *SCOR* (Sad09 at x0000000b) and null *CCOR* (Sad0A at x1000000b). The same rate applies to V-drive signal on VOut pin.

Note 13: Maximum *SCOR* (Sad09 at x1111111b), null *CCOR* (Sad0A at x1000000b).

Note 14: Null *SCOR* (Sad09 at x0000000b).

Note 15: "t_{VR}" is time from the beginning of vertical ramp of V-drive signal on VOut pin. "T_{VR}" is duration of this ramp, see chapter TYPICAL OUTPUT WAVEFORMS and Figure 19.

Note 16: $V_{VOamp} = V_{VOT} - V_{VOB}$

Note 17: The same rate applies to V-drive signal on VOut pin.

Note 18: Informative, not tested on each unit.

6.6 EW DRIVE SECTION

V_{CC} = 12V, T_{amb} = 25°C

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{EW}	Output voltage on EWOut pin		1.8		6.5	V
I_{EWOut}	Current sourced by EWOut output		-1.5		0	mA
V_{HEHT}	Control voltage range on HEHTIn pin		1		V_{RefO}	V
V_{EW-DC}	DC component of the EW-drive signal on EWOut pin	(19)(20)(21)(28) t_{VR}=1/2 T_{VR}(15) *HSIZE* (Sad10h): 00000000b 10000000b 11111111b		 2 3.25 4.5		 V V V
$\frac{\Delta V_{EW-DC}}{\Delta V_{HEHT}}$	Breathing compensation on V_{EW-DC}	(19)((20) t_{VR}=1/2 T_{VR}(15) $V_{HEHT}>V_{RefO}$ $V_{HEHT}(min) \le V_{HEHT} \le V_{RefO}$		 0 -0.125		 V/V V/V
$\frac{\Delta V_{EW-DC}}{V_{EW-DC} \cdot \Delta T}$	Temperature drift of DC component of the EW-drive signal on EWOut pin	(18)(19)(21)(28) t_{VR}=1/2T_{VR}(15)		100		ppm/°C
V_{EW-PCC}	Pin cushion correction component of the EW-drive signal on EWOut pin	(19)(21)(22)(23)(24)(28) *VSIZE* at maximum *PCC* (Sad0C): x0000000b x1000000b x1111111b Tracking with *VSIZE* : *PCC* at x1000000b *VSIZE* (Sad07): x0000000b x1000000b		 0 0.7 1.5 0.25 0.5		 V V V V V
$\frac{V_{EW-PCC}[t_{vr}=0]}{EW-PCC[t_{vr}=T_{VR}]}$	Tracking of PCC component of the EW-drive signal with vertical position adjustment	(19)(22)(25)(27)(28) *PCC* at x1111111b *VPOS* (Sad08): x0000000b x1111111b		 0.52 1.92		

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$V_{EW\text{-}Key}$	Keystone correction component of the EW-drive signal on EWOut pin	(20)(21)(22)(25)(26)(28) *KEYST* (Sad0D): x0000000b x1111111b		0.4 -0.4		V V
$\frac{\Delta V_{EW}}{V_{EW}[f_{max}] \cdot \Delta V_{HO}}$ -	Tracking of EW-drive signal with horizontal frequency(30)	$V_{HO}>V_{HOThrfr}$ $V_{HO}(min) \leq V_{HO} \leq V_{HOThrfr}$		0 20		%/V %/V
$\frac{\Delta V_{EW-AC}}{V_{EW-AC} \cdot \Delta V_{HEHT}}$	Breathing compensation on $V_{EW\text{-}AC}$(29)	(23)(24) $V_{HEHT}>V_{RefO}$ $V_{HEHT}(min) \leq V_{HEHT} \leq V_{RefO}$		0 1.75		%/V %/V

Note 19: *KEYST* at medium (neutral) value.

Note 20: *PCC* at minimum value.

Note 21: *VPOS* at medium (neutral) value.

Note 22: *HSIZE* at minimum value.

Note 23: Defined as difference of (voltage at t_{VR}=0) minus (voltage at t_{VR}=1/2 T_{VR}).

Note 24: Defined as difference of (voltage at $t_{VR}=T_{VR}$) minus (voltage at t_{VR}=1/2 T_{VR}).

Note 25: *VSIZE* at maximum value.

Note 26: Difference: (voltage at t_{VR}=0) minus (voltage at $t_{VR}=T_{VR}$).

Note 27: Ratio "A/B"of parabola component voltage at t_{VR}=0 versus parabola component voltage at $t_{VR}=T_{VR}$. See Figure 2.

Note 28: $V_{HEHT}>V_{RefO}$, $V_{VEHT}>V_{RefO}$

Note 29: $V_{EW\text{-}AC}$ is the sum of all components other than $V_{EW\text{-}DC}$ (contribution of PCC and keystone correction).

Note 30: More precisely tracking with voltage on HPLL1F pin which itself depends on frequency at a rate given by external components on PLL1 pins. $V_{EW}[fmax]$ is the value at condition $V_{HO}>V_{HOThrfr}$.

6.7 DYNAMIC CORRECTION OUTPUTS SECTION

V_{CC} = 12V, T_{amb} = 25°C

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
Vertical Dynamic Correction output VDyCor						
I_{VDyCor}	Current sunk from VDyCor output		-1.5		-0.1	mA
$V_{VD\text{-}DC}$	DC component of the drive signal on VDyCor output	$R_{L(VDyCor)}$=10kΩ		4		V
$\|V_{VD\text{-}V}\|$	Amplitude of V-parabola on VDy-Cor output (21)	*VSIZE* at medium *VDC-AMP* (Sad15h): xxxxxx00 xxxxxx01 xxxxxx10 xxxxxx11 *VDC-AMP* at maximum *VSIZE* (Sad07): x0000000b x1111111b		 0.25 0.50 0.75 1.00 0.6 1.6		 V V V V V V
$\frac{V_{VD-V}[t_{vr}=0]}{V_{VD-V}[t_{vr}=T_{VR}]}$	Tracking of V-parabola on VDyCor output with vertical position (31)	*VDC-AMP* at maximum *VPOS* (Sad08): x0000000b x1111111b		 0.52 1.92		

Note 31: Ratio "A/B"of vertical parabola component voltage at t_{VR}=0 versus vertical parabola component voltage at t_{VR}=T_{VR}.

6.8 DC/DC CONTROLLER SECTION

V_{CC} = 12V, T_{amb} = 25°C

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
R_{B+FB}	Ext. resistance applied between BComp output and BRegIn input		5			kΩ
A_{OLG}	Open loop gain of error amplifier on BRegIn input	Low frequency(18)		100		dB
f_{UGBW}	Unity gain bandwidth of error amplifier on BRegIn input	(18)		6		MHz
I_{RI}	Bias current delivered by regulation input BRegIn			-0.2		µA
I_{BComp}	Output current capability of BComp output.	HBOutEn = "Enable" HBOutEn = "Disable" (32)	-0.5	 0.5	2.0	mA mA
$A_{BISense}$	Voltage gain on BISense input			3		
$V_{ThrBIsCurr}$	Threshold voltage on BISense input corresponding to current limitation		1.98	2.1	2.22	V
$I_{BISense}$	Input current sourced by BISense input			-1		µA
I_{BOut}	Output current capability of BOut output		0		10	mA
V_{BOSat}	Saturation voltage of the internal output transistor on BOut	I_{BOut}=10mA		0.25	0.35	V
V_{BReg}	Regulation reference for BRegIn voltage(33)	V_{RefO}=8V	4.7	4.8	5.0	V
$t_{BTrigDel}$ / T_H	Delay of BOut "Off-to-On" edge after middle of flyback pulse, as part of T_H (34)	BOutPh = "0"		16		%

Note 32: A current sink is provided by the BComp output while BOut is disabled:

Note 33: Internal reference related to V_{RefO}. The same values to be found on pin BRegIn, while regulation loop is stabilized.

Note 34: Only applies to configuration specified in "Test conditions" column, i.e. synchronization of BOut "Off-to-On" edge with horizontal flyback signal. Refer to chapter "DC/DC controller" for more details.

6.9 MISCELLANEOUS

V_{CC} = 12V, T_{amb} = 25°C

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
Vertical blanking and horizontal lock indication composite output HLckVBk						
$I_{SinkLckBk}$	Sink current to HLckVBk pin	(35)		100		µA
V_{OLckBk}	Output voltage on HLckVBk output	V.blank / H.lock No / Yes Yes / Yes No / No Yes / No		 0.1 1.1 5 6		 V V V V
Horizontal moiré canceller						
$V_{AC\text{-}HMoiré}$	H-moiré pulse amplitude on HMoiré pin	Rext=10kΩ *HMOIRE* (Sad02): x0000000b x1111111b		 0.1 2.1		 V V
$V_{DC\text{-}HMoiré}$	DC level on HMoiré pin	Rext=10kΩ		0.1		V
Vertical moiré canceller						
$V_{V\text{-}moiré}$	Amplitude of modulation of V-drive signal on VOut pin by vertical moiré.	*VMOIRE* (Sad0Bh): x0000000b x1111111b		 0 3		 mV mV
Protection functions						
$V_{ThrXRay}$	Input threshold on XRay input(36)		7.65	7.9	8.2	V
$t_{XRayDelay}$	Delay time between XRay detection event and protection action			$2T_H$		
V_{CCEn}	V_{CC} value for start of operation at V_{CC} ramp-up(37)			8.5		V
V_{CCDis}	V_{CC} value for stop of operation at V_{CC} ramp-down(37)			6.5		V
Control voltages on HPosF **pin for Soft start/stop operation**(18)						
V_{HOn}	Threshold for start/stop of H-drive signal			1		V
V_{BOn}	Threshold for start/stop of B-drive signal			1.7		V
$V_{HBNorm\ f}$	Threshold for full operational duty cycle of H-drive and B-drive signals			2.4		
V_{HPos}	Voltage on HPosF pin as function of adjustment of *HPOS* register	Normal operation *HPOS* (Sad01) 00000000b 11111111b	 3.85 2.60	 4.0 2.8	 4.15 3.05	 V V

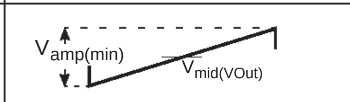
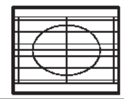
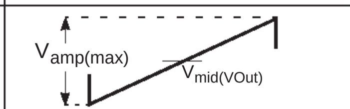
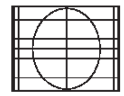
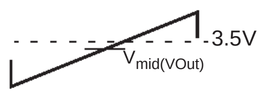
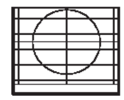
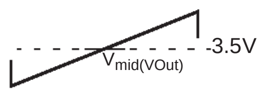
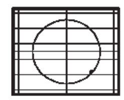
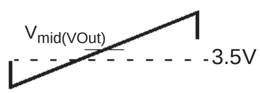
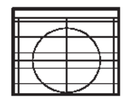
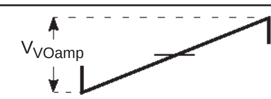
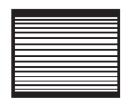
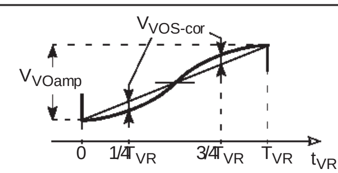
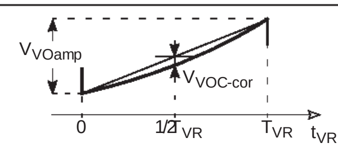
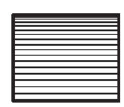
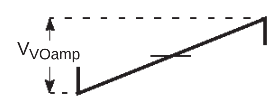
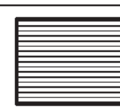
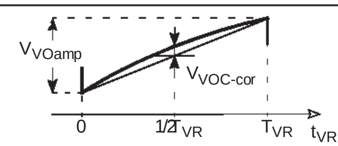
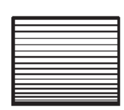
Note 35: Current sunk by the pin if the external voltage is higher than one the circuit tries to force.

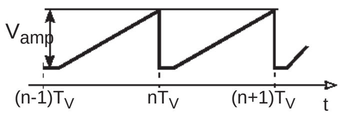
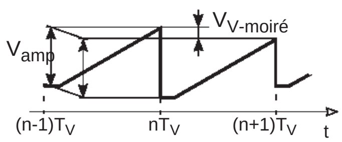
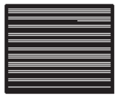
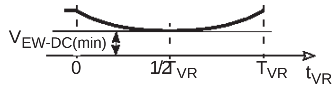
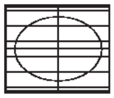
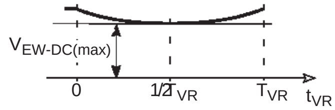
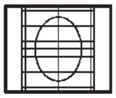
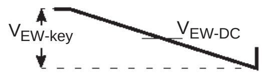
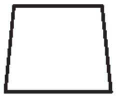
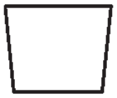
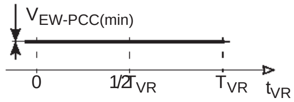
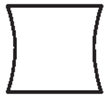
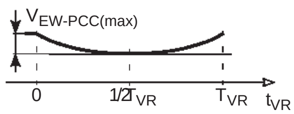
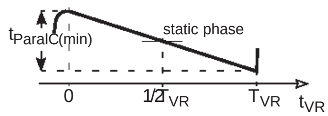
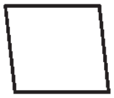
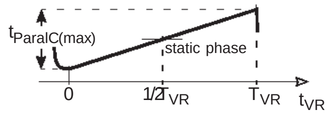
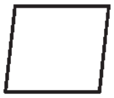
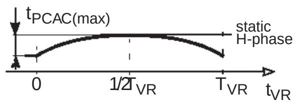
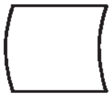
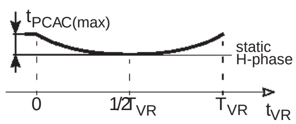
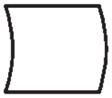
Note 36: The threshold is equal to actual V_{RefO}.

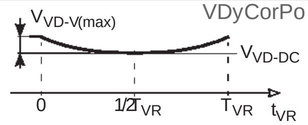
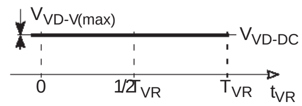
Note 37: In the regions of V_{CC} where the device's operation is disabled, the H-drive, V-drive and B+-drive signals on HOut, VOut and BOut pins, resp., are inhibited, the I^2C Bus does not accept any data.

7 - TYPICAL OUTPUT WAVEFORMS

Note ([38])

Function	Sad	Pin	Byte	Waveform	Effect on Screen
Vertical Size	07	VOut	x0000000		
			x1111111		
Vertical Position	08	VOut	x0000000		
			x1000000		
			x1111111		
S-correction	09	VOut	x0000000: Null		
			x1111111: Max.		
C-correction	0A	VOut	x0000000		
			x1000000 : Null		
			x1111111		

Function	Sad	Pin	Byte	Waveform	Effect on Screen
Vertical moiré amplitude	0B	VOut	x0000000: Null		
			x1111111: Max.		
Horizontal size	10h	EWOut	00000000		
			11111111		
Keystone correction	0D	EWOut	x0000000		
			x1111111		
Pin cushion correction	0C	EWOut	x0000000		
			x1111111		
Parallelogram correction	12h	Internal	x0000000		
			x1111111		
Pin cushion asymmetry correction	11h	Internal	x0000000		
			x1111111		

Function	Sad	Pin	Byte	Waveform	Effect on Screen
Vertical dynamic correction amplitude	15h	VDyCor	xxxxxx11		Application dependent
			xxxxxx00		

Note 38: For any H and V correction component of the waveforms on EWOut and VOut pins and for internal waveform for corrections of H asymmetry, displayed in the table, weight of the other relevant components is nullified (minimum for parabola, S-correction, medium for keystone, all corner corrections, C-correction, parallelogram, parabola asymmetry correction, written in corresponding registers).

8 - I²C BUS CONTROL REGISTER MAP

The device slave address is 8C in write mode and 8D in read mode.

Bold weight denotes default value at Power-On-Reset.
I²C Bus data in the adjustment register is buffered and internally applied with discharge of the vertical oscillator .
In order to ensure compatibility with future devices, all “Reserved” bits should be set to 0.

Sad	D7	D6	D5	D4	D3	D2	D1	D0
WRITE MODE (SLAVE ADDRESS = 8C)								
00	Reserved							
01	*HPOS (Horizontal position)*							Reserved
	1	**0**	**0**	**0**	**0**	**0**	**0**	
02	HMoiré	*HMOIRE (Horizontal moiré amplitude)*						
	1: Separated **0**: Combined	**0**	**0**	**0**	**0**	**0**	**0**	**0**
03	Reserved							
04	Reserved							
05	Reserved							
06	BOutPol **0**: Type N	Reserved						
07	BOutPh	*VSIZE (Vertical size)*						
	0: H-flyback 1: H-drive	**1**	**0**	**0**	**0**	**0**	**0**	**0**
08	EWTrHFr	*VPOS (Vertical position)*						
	0: No tracking	**1**	**0**	**0**	**0**	**0**	**0**	**0**
09	Reserved	*SCOR (S-correction)*						
		1	**0**	**0**	**0**	**0**	**0**	**0**
0A	Reserved	*CCOR (C-correction)*						
		1	**0**	**0**	**0**	**0**	**0**	**0**
0B	Reserved	*VMOIRE (Vertical moiré amplitude)*						
		0	**0**	**0**	**0**	**0**	**0**	**0**
0C	Reserved	*PCC (Pin cushion correction)*						
		1	**0**	**0**	**0**	**0**	**0**	**0**
0D	Reserved	*KEYST (Keystone correction)*						
		1	**0**	**0**	**0**	**0**	**0**	**0**
0E	Reserved							
0F	Reserved							
10	*HSIZE (Horizontal size)*							Reserved
	1	**0**	**0**	**0**	**0**	**0**	**0**	
11	Reserved	*PCAC (Pin cushion asymmetry correction)*						
		1	**0**	**0**	**0**	**0**	**0**	**0**
12	Reserved	*PARAL (Parallelogram correction)*						
		1	**0**	**0**	**0**	**0**	**0**	**0**
13	Reserved							
14	Reserved							
15	Reserved						*VDC-AMP*	
							0	**0**

Sad	D7	D6	D5	D4	D3	D2	D1	D0
16	XRayReset **0**: No effect 1: Reset	VSyncAuto **1**: On	VSyncSel 0:Comp **1**:Sep	**0**	**0**	PLL1Pump 1: Fast **0**: Slow	PLL1InhEn **1**: On	HLockEn **1**: On
17	TV **0**: Off(39)	TH **0**: Off(39)	TVM **0**: Off(39)	THM **0**: Off(39)	BOHEdge **0**: Falling	HBOutEn **0**: Disable	VOutEn **0**: Disable	BlankMode **1**: Perm.

Note 39: The TV, TH, TVM and THM bits are for testing purposes and must be kept at 0 by application.

Description of I^2C Bus switches

Write-to bits

Sad02/D7 - HMoiré

Horizontal **Moiré** characteristics
- 0: Adapted to an architecture with EHT generated in deflection section
- 1: Adapted to an architecture with separated deflection and EHT sections

Sad06/D7 - BOutPol

Polarity of B+ drive signal on BOut pin
- 0: adapted to N type of power MOS - high level to make it conductive
- 1: adapted to P type of power MOS - low level to make it conductive

Sad07/D7 - BOutPh

Phase of start of B+ drive signal on BOut pin
- 0: Just after horizontal flyback pulse
- 1: With one of edges of line drive signal on HOut pin, selected by BOHEdge bit

Sad08/D7 - EWTrHFr

Tracking of all corrections contained in waveform on pin EWOut with **H**orizontal **Fr**equency
- 0: Not active
- 1: Active

Sad16/D0 - HLockEn

Enable of output of **H**orizontal PLL1 **Lock**/unlock status signal on pin HLckVBk
- 0: Disabled, vertical blanking only on the pin HLckVBk
- 1: Enabled

Sad16/D1 - PLL1InhEn

Enable of **Inh**ibition of horizontal **PLL1** during extracted vertical synchronization pulse
- 0: Disabled, PLL1 is never inhibited
- 1: Enabled

Sad16/D2 - PLL1Pump

Horizontal **PLL1** charge **Pump** current
- 0: Slow PLL1, low current
- 1: Fast PLL1, high current

Sad16/D5 - VSyncSel

Vertical **Sync**hronization input **Sel**ection between the one extracted from composite HV signal on pin H/HVSyn and the one on pin VSyn. No effect if VSyncAuto bit is at 1.
- 0: V. sync extracted from composite signal on H/HVSyn pin selected
- 1: V. sync applied on VSyn pin selected

Sad16/D6 - VSyncAuto

Vertical **Sync**hronization input selection **Auto**matic mode. If enabled, the device automatically selects between the vertical sync extracted from composite HV signal on pin H/HVSyn and the one on pin VSyn, based on detection mechanism. If both are present, the one coming first is kept.
- 0: Disabled, selection done according to bit VSyncSel
- 1: Enabled, the bit VSyncSel has no effect

Sad16/D7 - XRayReset

Reset to 0 of **XRay** effected with ACK bit of I^2C Bus data transfer into register containing the XRayReset bit.
- 0: No effect
- 1: Reset with automatic return of the bit to 0

This bit is not latched, it will return to 0 by itself.

Sad17/D0 - BlankMode

Blanking operation **Mode**
- 0: Blanking pulse starting with detection of vertical synchronization pulse and ending with end of vertical oscillator discharge

(start of vertical sawtooth ramp on the VOut pin)

1: Permanent blanking - high blanking level in composite signal on pin HLckVBk is permanent

Sad17/D1 - VOutEn

Vertical **Out**put **En**able

0: Disabled, $V_{offVOut}$ on VOut pin (see 6.5 Vertical section)

1: Enabled, vertical ramp with vertical position offset on VOut pin

Sad17/D2 - HBOutEn

Horizontal and **B**+ **Out**put **En**able

0: Disabled, levels corresponding to "power transistor off" on HOut and BOut pins (high for HOut, high or low for BOut, depending on BOutPol bit).

1: Enabled, horizontal deflection drive signal on HOut pin providing that it is not inhibited by another internal event (activated XRay protection). B+ drive signal on BOut pin.

Programming the bit to 1 after prior value of 0, will initiate soft start mechanism of horizontal drive and of B+ DC/DC convertor

Sad17/D3 - BOHEdge

Selection of **Edge** of **H**orizontal drive signal to phase **B**+ drive **O**utput signal on BOut pin. Only applies if the bit BOutPh is set to 1, otherwise BOHEdge has no effect.

0: Falling edge

1: Rising edge

Sad17/D4,D5,D6,D7 - THM, TVM, TH, TV

Test bits. They must be kept at 0 level by application S/W.

9 - OPERATING DESCRIPTION

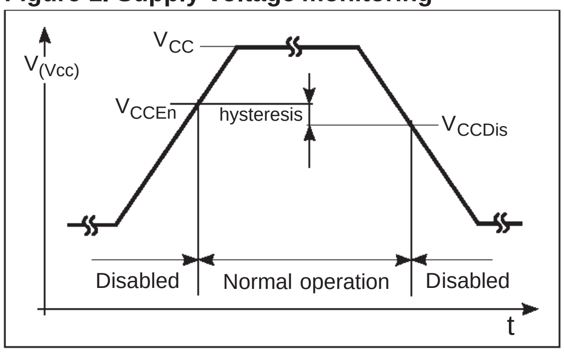
9.1 SUPPLY AND CONTROL

9.1.1 Power supply and voltage references

The device is designed for a typical value of power supply voltage of 12 V.

In order to avoid erratic operation of the circuit at power supply ramp-up or ramp-down, the value of V_{CC} is monitored. See Figure 1 and electrical specifications. At switch-on, the device enters a "normal operation" as the supply voltage exceeds V_{CCEn} and stays there until it decreases below V_{CCDis}. The two thresholds provide, by their difference, a hysteresis to bridge potential noise. Outside the "normal operation", the signals on HOut, BOut and VOut outputs are inhibited and the I^2C bus interface is inactive (high impedance on SDA, SCL pins, no ACK), all I^2C bus control registers being reset to their default values (see chapter I^2C BUS CONTROL REGISTER MAP on page 20).

Figure 1. Supply voltage monitoring



Internal thresholds in all parts of the circuit are derived from a common internal reference supply V_{RefO} that is lead out to RefOut pin for external filtering against ground as well as for external use with load currents limited to I_{RefO}. The filtering is necessary to minimize interference in output signals, causing adverse effects like e.g. jitter.

9.1.2 I^2C Bus Control

The I^2C bus is a 2 line bi-directional serial communication bus introduced by Philips. For its general description, refer to corresponding Philips I^2C bus specification.

This device is an I^2C bus slave, compatible with fast (400kHz) I^2C bus protocol, with write mode slave address of 8C. Integrators are employed at the SCL (Serial Clock) input and at the input buffer of the SDA (Serial Data) input/output to filter off the spikes of up to 50ns.

The device supports multiple data byte messages (with automatic incrementation of the I^2C bus subaddress) as well as repeated Start Condition for I^2C bus subaddress change inside the I^2C bus messages. All I^2C bus registers with specified I^2C bus subaddress are of WRITE ONLY type.

For the I^2C bus control register map, refer to chapter I^2C BUS CONTROL REGISTER MAP on page 20.

9.2 SYNC. PROCESSOR

9.2.1 Synchronization signals

The device has two inputs for TTL-level synchronization signals, both with hysteresis to avoid erratic detection and with a pull-down resistor. On H/HVSyn input, pure horizontal or composite horizontal/vertical signal is accepted. On VSyn input, only pure vertical sync. signal is accepted. Both positive and negative polarities may be applied on either input, see Figure 2. Polarity detector and programmable inverter are provided on each of the two inputs. The signal applied on H/HVSyn pin, after polarity treatment, is directly lead to horizontal part and to an extractor of vertical sync. pulses, working on principle of integration, see Figure 3. The vertical sync. signal applied to the vertical deflection processor is selected between the signal extracted from the composite signal on H/HVSyn input and the one applied on VSyn input. The selector is controlled by VSyncSel I^2C bus bit.

Besides the polarity detection, the device is capable of detecting the presence of sync. signals on each of the inputs and at the output of vertical sync. extractor. The device is equipped with an automatic mode (switched on or off by VSyncAuto I^2C bus bit) that uses the detection information.

Figure 2. Horizontal sync signal

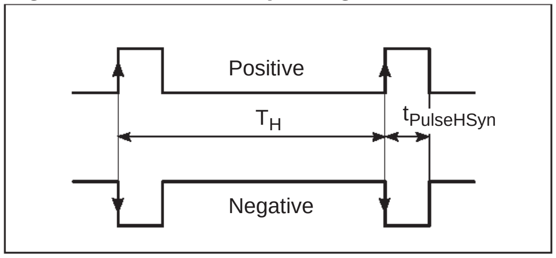
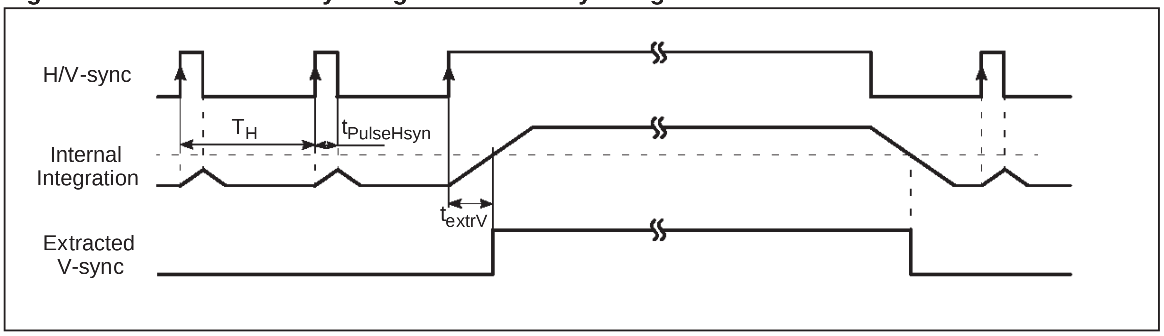


Figure 3. Extraction of V-sync signal from H/V-sync signal



9.2.2 Automatic sync. selection mode

I²C bus bit VSyncAuto is set to 1. In this mode, the device itself controls the I²C bus bits switching the polarity inverters and the vertical sync. signal selector (VSyncSel), using the information provided by detection circuitry. If both extracted and pure vertical sync. signals are present, the one already selected is maintained. No intervention of the MCU is necessary.

9.3 HORIZONTAL SECTION

9.3.1 General

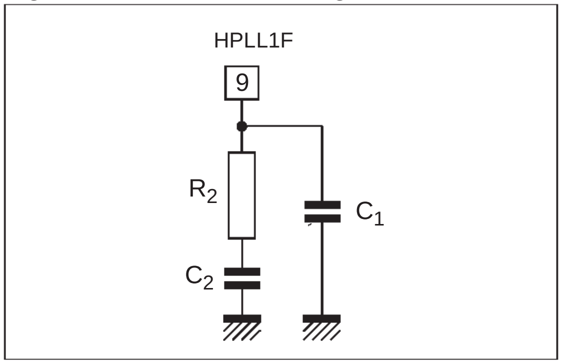
The horizontal section consists of two PLLs with various adjustments and corrections, working on horizontal deflection frequency, then phase shifting and output driving circuitry providing H-drive signal on HOut pin. Input signal to the horizontal section is output of the polarity inverter on H/HVSyn input. The device ensures automatically that this polarity be always positive.

9.3.2 PLL1

The PLL1 block diagram is in Figure 5. It consists of a voltage controlled oscillator (VCO), a shaper with adjustable threshold, a charge pump with inhibition circuit, a frequency and phase comparator and timing circuitry. The goal of the PLL1 is to make the VCO ramp signal match in frequency the sync. signal and to lock this ramp in phase to the sync. signal, with a possibility to adjust a permanent phase offset. On the screen, this offset results in the change of horizontal position of the picture. The loop, by tuning the VCO accordingly, gets and maintains in coincidence the rising edge of input sync. signal with signal REF1, which is derived from the VCO ramp by a comparator with threshold adjustable through *HPOS* I²C bus control. The coincidence is identified and flagged by lock detection circuit on pin HLckVBk .

The charge pump provides positive and negative currents charging the external loop filter on HPosF pin. The loop is independent of the trailing edge of sync. signal and only locks to its leading edge. By design, the PLL1 does not suffer from any dead band even while locked. The speed of the PLL1 depends on the current value provided by the charge pump. While not locked, the current is very low, to slow down the changes of VCO frequency and thus protect the external power components at sync. signal change. In locked state, the currents are much higher, two different values being selectable via PLL1Pump I²C bus bit to provide a mean to control the PLL1 speed by S/W. Lower values make the PLL1 slower, but more stable. Higher values make it faster and less stable. In general, the PLL1 speed should be higher for high deflection frequencies. The response speed and stability (jitter level) depends on the choice of external components making up the loop filter. A “CRC” filter is generally used (see Figure 4 on page 25).

Figure 4. H-PLL1 filter configuration



The PLL1 is internally inhibited during extracted vertical sync. pulse (if any) to avoid taking into account missing or wrong pulses on the phase comparator. Inhibition is obtained by forcing the charge pump output to high impedance state. The inhibition mechanism can be disabled through PLL1Pump I^2C bus bit.

The Figure 7, in its upper part, shows the position of the VCO ramp signal in relation to input sync. pulse for three different positions of adjustment of horizontal position control *HPOS*.

Figure 5. Horizontal PLL1 block diagram

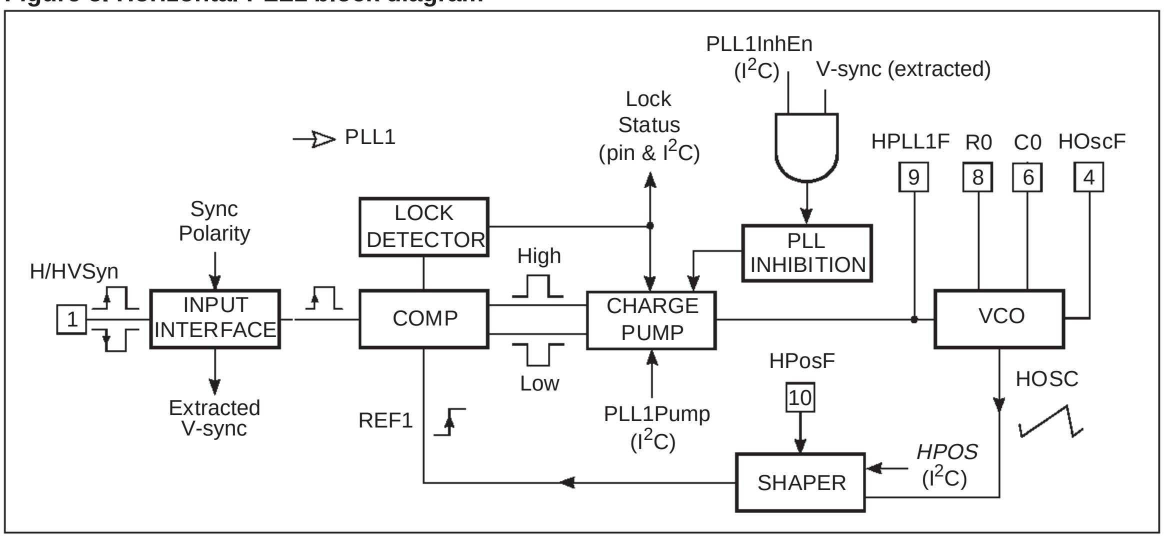
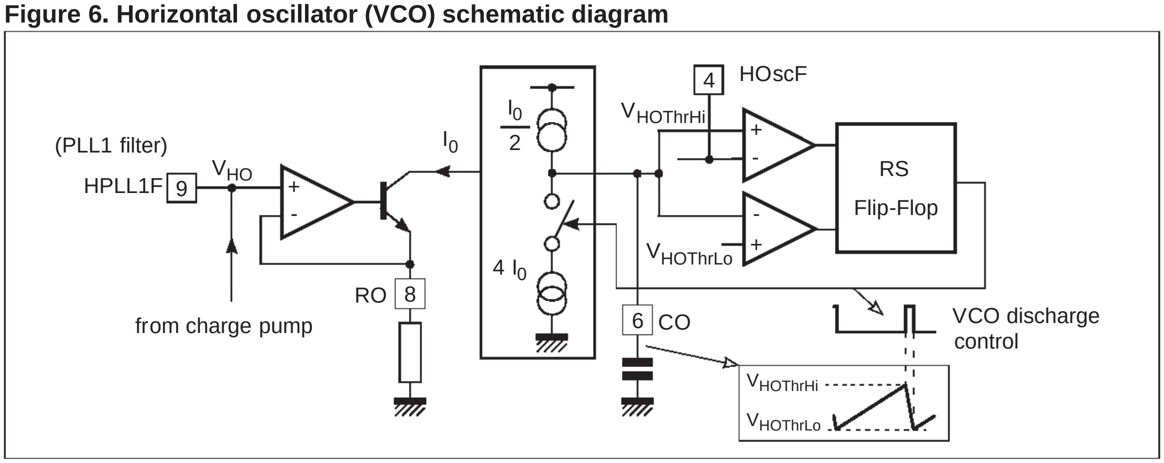


Figure 6. Horizontal oscillator (VCO) schematic diagram



9.3.3 Voltage controlled oscillator

The VCO makes part of both PLL1 and PLL2 loops, being an “output” to PLL1 and “input” to PLL2. It delivers a linear sawtooth. Figure 6 explains its principle of operation. The linears are obtained by charging and discharging an external capacitor on pin CO, with currents proportional to the current forced through an external resistor on pin RO, which itself depends on the input tuning voltage V_{HO} (filtered charge pump output). The rising and falling linears are limited by $V_{HOThrLo}$ and $V_{HOThrHi}$ thresholds filtered through HOscF pin.

At no signal condition, the V_{HO} tuning voltage is clamped to its minimum (see chapter ELECTRICAL PARAMETERS AND OPERATING CONDITIONS, part horizontal section), which corresponds to the free-running VCO frequency $f_{HO(0)}$. Refer to Note1 for the formula to calculate this frequency using external components values. The ratio between the frequency corresponding to maximum V_{HO} and the one corresponding to minimum V_{HO} (free-running frequency) is about 4.5. This range can easily be increased in the application. The PLL1 can only lock to input frequencies falling inside these two limits.

9.3.4 PLL2

The goal of the PLL2 is, by means of phasing the signal driving the power deflection transistor, to lock the middle of the horizontal flyback to a certain threshold of the VCO sawtooth. This internal threshold is affected by geometry phase corrections, like e.g., parallelogram. The PLL2 is much faster than PLL1 to be able to follow the dynamism of this phase modulation. The PLL2 control current (see Figure 7) is significantly increased during discharge of vertical oscillator (during vertical retrace period) to be able to make up for the difference of dynamic phase at the bottom and at the top of the picture. The PLL2 control current is integrated on the external filter on pin HPLL2C to obtain smoothed voltage, used, in comparison with VCO ramp, as a threshold for H-drive rising edge generation.

As both leading and trailing edges of the H-drive signal in the Figure 7 must fall inside the rising part of the VCO ramp, an optimum middle position of the threshold has been found to provide enough margin for horizontal output transistor storage time as well as for the trailing edge of H-drive signal with maximum duty cycle. Yet, the constraints thereof must be taken into account while considering the application frequency range and H-flyback duration. The Figure 7 also shows regions for rising and falling edges of the H-drive signal on HOut pin. As it is forced high during the H-flyback pulse and low during the VCO discharge period, no edge during these two events takes effect.

The flyback input configuration is in Figure 8.

9.3.5 Dynamic PLL2 phase control

The dynamic phase control of PLL2 is used to compensate for picture asymmetry versus vertical axis across the middle of the picture. It is done by modulating the phase of the horizontal deflection with respect to the incoming video (synchronization). Inside the device, the threshold $V_{S(0)}$ is compared with the VCO ramp, the PLL2 locking the middle of H-flyback to the moment of their match. The dynamic phase is obtained by modulation of the threshold by correction waveforms. Refer to Figure 12 and to chapter TYPICAL OUTPUT WAVEFORMS. The correction waveforms have no effect in vertical middle of the screen (for middle vertical position). As they are summed, their effect on the phase tends to reach maximum span at top and bottom of the picture. As all the components of the resulting correction waveform (linear for parallelogram correction and parabola of 2nd order for Pin cushion asymmetry correction) are generated from the output vertical deflection drive waveform, they both track with real vertical amplitude and position (including breathing compensation), thus being fixed on the screen. Refer to I^2C BUS CONTROL REGISTER MAP on page 20 for details on I^2C bus controls.

Figure 7. Horizontal timing diagram

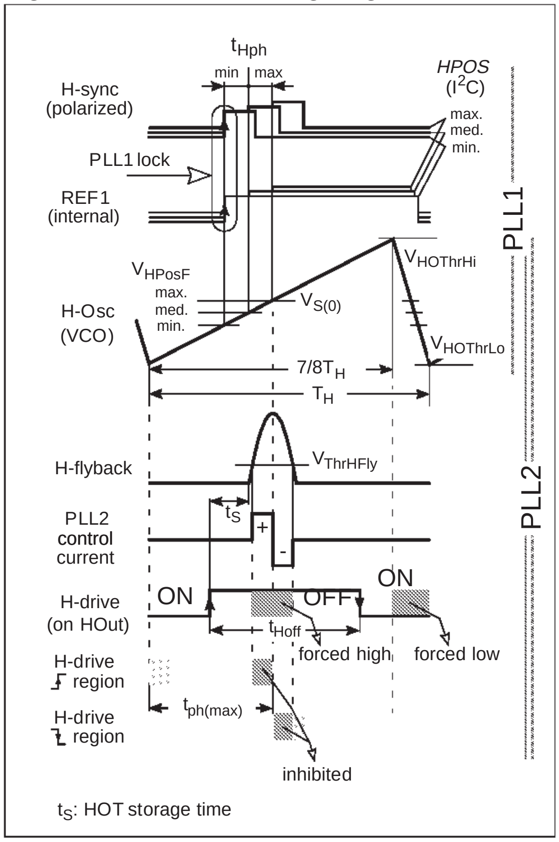
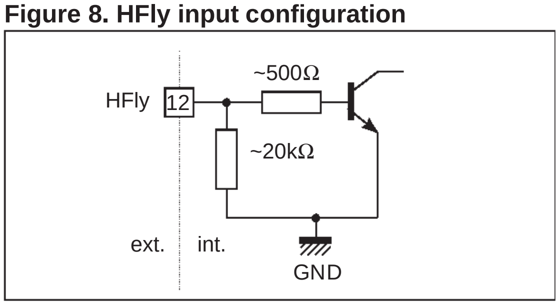


Figure 8. HFly input configuration



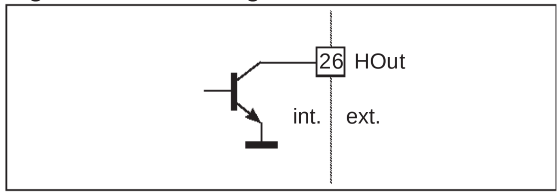
9.3.6 Output section

The H-drive signal is inhibited (high level) during flyback pulse, and also when V_{CC} is too low, when I^2C bus bit HBOutEn is set to 0 (default position).

The PLL2 is followed by a rapid phase shifting which accepts the signal from H-moiré canceller (see sub chapter Horizontal moiré cancellation on page 27)

The output stage consists of a NPN bipolar transistor, the collector of which is routed to HOut pin (see Figure 9).

Figure 9. HOut configuration



Non-conductive state of HOT (Horizontal Output Transistor) must correspond to non-conductive state of the device output transistor.

9.3.7 Soft-start and soft-stop on H-drive

The soft-start and soft-stop procedure is carried out at each switch-on or switch-off of the H-drive signal via HBOutEn I^2C bus bit to protect external power components. By its second function, the external capacitor on pin HPosF is used to time out this procedure, during which the duty cycle of H-drive signal starts at its maximum ("t_{Hoff}/T_H for soft start/stop" in electrical specifications) and slowly decreases. This is controlled by voltage on pin HPosF. See Figure 10 and sub chapter Safety functions on page 33.

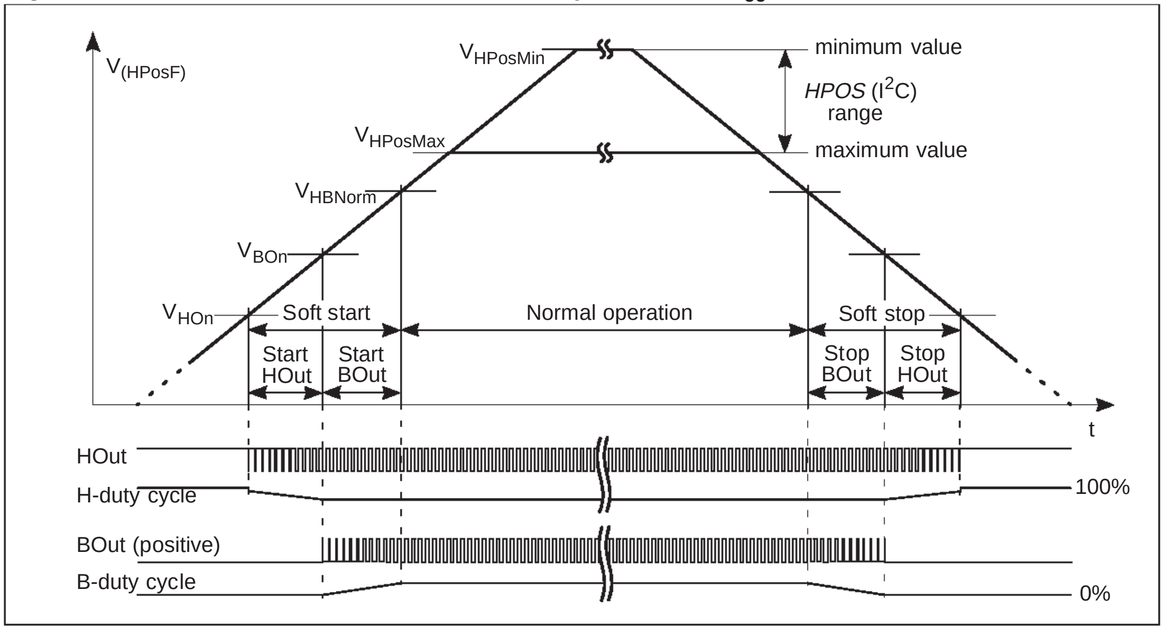
9.3.8 Horizontal moiré cancellation

The horizontal moiré canceller is intended to blur a potential beat between the horizontal video pixel period and the CRT pixel width, which causes visible moiré patterns in the picture.

On pin HMoiré, it generates a square line-synchronized waveform with amplitude adjustable through *HMOIRE* I^2C bus control.

The behaviour of horizontal moiré is to be optimised for different deflection design configurations using HMoiré I^2C bus bit. This bit is to be kept at 0 for common architecture (B+ and EHT common regulation) and at 1 for separated architecture (B+ and EHT each regulated separately).

Figure 10. Control of HOut and BOut at start/stop at nominal V_{cc}



9.4 VERTICAL SECTION

9.4.1 General

The goal of the vertical section is to drive vertical deflection output stage. It delivers a sawtooth waveform with an amplitude independent of deflection frequency, on which vertical geometry corrections of C- and S-type are superimposed (see chapter TYPICAL OUTPUT WAVEFORMS).

Block diagram is in Figure 11. The sawtooth is obtained by charging an external capacitor on pin VCap with controlled current and by discharging it via transistor Q1. This is controlled by the CONTROLLER. The charging starts when the voltage across the capacitor drops below V_{VOB} threshold. The discharging starts either when it exceeds V_{VOT} threshold or a short time after arrival of synchronization pulse. This time is necessary for the AGC loop to sample the voltage at the top of the sawtooth. The V_{VOB} reference is routed out onto VOscF pin in order to allow for further filtration.

The charging current influences amplitude and shape of the sawtooth. Just before the discharge, the voltage across the capacitor on pin VCap is sampled and stored on a storage capacitor connected on pin VAGCCap. During the following vertical period, this voltage is compared to internal reference REF (V_{VOT}), the result thereof controlling the gain of the transconductance amplifier providing the charging current. Speed of this AGC loop depends on the storage capacitance on pin VAGCCap. On the screen, this corresponds to stabilized vertical size of picture. After a change of frequency on the sync. input, the stabilization time depends on the frequency difference and on the capacitor value. The lower its value, the shorter the stabilization time, but on the other hand, the lower the loop stability. A practical compromise is a capacitance of 470nF. The leakage current of this capacitor results in difference in amplitude between low and high frequencies. The higher its parallel resistance $R_{L(VAGCCap)}$, the lower this difference.

When the synchronization pulse is not present, the charging current is fixed. As a consequence, the free-running frequency $f_{VO(0)}$ only depends on the value of the capacitor on pin VCap. It can be roughly calculated using the following formula

$$f_{VO(0)} = \frac{150\text{nF}}{C_{(VCap)}} \cdot 100\text{Hz}$$

The frequency range in which the AGC loop can regulate the amplitude also depends on this capacitor.

The C- and S-corrections of shape serve to compensate for the vertical deflection system non-linearity. They are controlled via *CCOR* and *SCOR* I^2C bus controls.

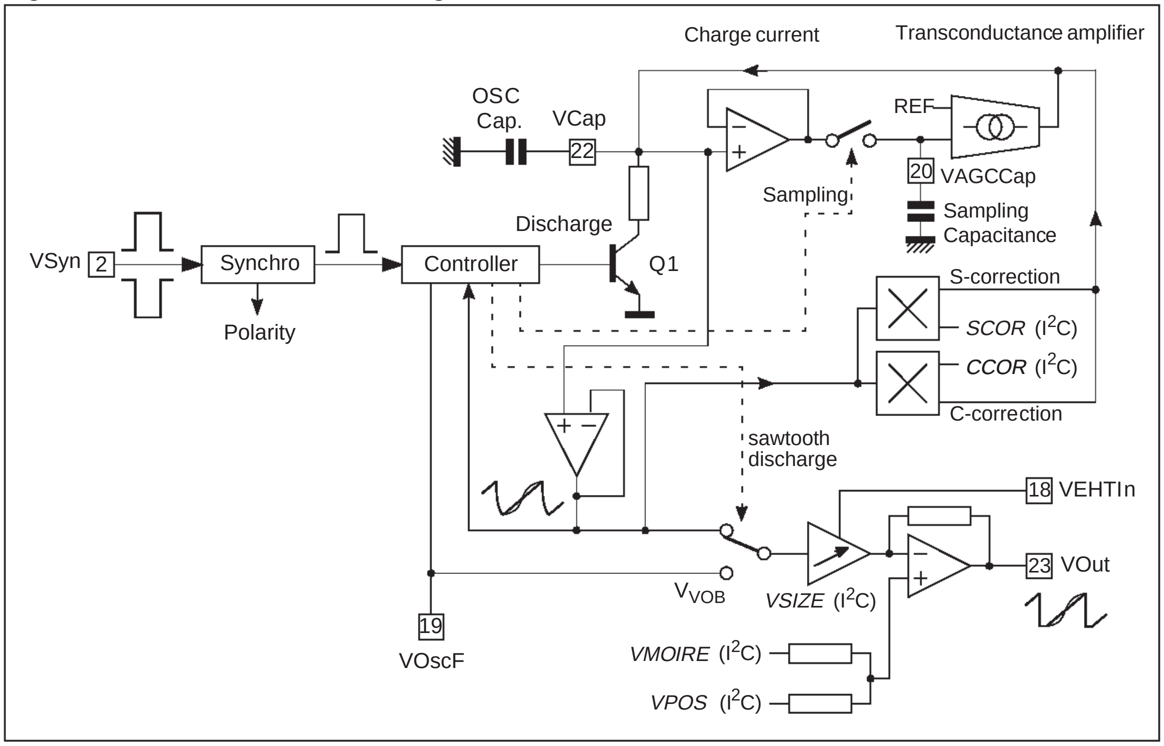
Shape-corrected sawtooth with regulated amplitude is lead to amplitude control stage. The discharge exponential is replaced by V_{VOB} level, which, under control of the CONTROLLER, creates a rapid falling edge and a flat part before beginning of new ramp. Mean value of the waveform output on pin VOut is adjusted by means of *VPOS* I^2C bus control, its amplitude through *VSIZE* I^2C bus control. Vertical moiré is superimposed.

The biasing voltage for external DC-coupled vertical power amplifier is to be derived from V_{RefO} voltage provided on pin RefOut, using a resistor divider, this to ensure the same temperature drift of mean (DC) levels on both differential inputs and to compensate for spread of V_{RefO} value (and so mean output value) between particular devices.

9.4.2 Vertical moiré

To blur the interaction of deflection lines with CRT mask grid pitch that can generate moiré pattern, the picture position is to be alternated at frame frequency. For this purpose, a square waveform at half-frame frequency is superimposed on the output waveform's DC value. Its amplitude is adjustable through *VMOIRE* I^2C bus control,.

Figure 11. Vertical section block diagram



9.5 EW DRIVE SECTION

The goal of the EW drive section is to provide, on pin EWOut, a waveform which, used by an external DC-coupled power stage, serves to compensate for those geometry errors of the picture that are symmetric versus vertical axis across the middle of the picture.

The waveform consists of an adjustable DC value, corresponding to horizontal size, a parabola of 2nd order for "pin cushion" correction and a linear for "keystone" correction. All of them are adjustable via I^2C bus, see I^2C BUS CONTROL REGISTER MAP on page 20.

Refer to Figure 12, Figure 13 and to chapter TYPICAL OUTPUT WAVEFORMS. The correction waveforms have no effect in the vertical middle of the screen (if the *VPOS* control is adjusted to its medium value). As they are summed, the resulting waveform tends to reach its maximum span at top and bottom of the picture. The voltage at the EWOut is top and bottom limited (see parameter V_{EW}). According to Figure 13, especially the bottom limitation seems to be critical for maximum horizontal size (minimum DC). Actually it is not critical since the parabola component must always be applied. As all the components of the resulting correction waveform are generated from the output vertical deflection drive waveform, they all track with real vertical amplitude and position (including breathing compensation), thus being fixed vertically on the screen. They are also affected by C- and S-corrections. The sum of components other than DC is affected by value in *HSIZE* I^2C bus control in reversed sense. Refer to electrical specifications for value. The DC value, adjusted via *HSIZE* control, is also affected by voltage on HEHTIn input, thus providing a horizontal breathing compensation (see electrical specifications for value). The resulting waveform is conditionally multiplied with voltage on HPLL1F, which depends on frequency. Refer to electrical specifications for value and more precision. This tracking with frequency provides a rough compensation of variation of picture geometry with frequency and allows to fix the adjustment ranges of I^2C bus controls throughout the operating range of horizontal frequencies. It can be switched off by EWTrHFr I^2C bus bit (off by default).

The EW waveform signal is buffered by an NPN emitter follower, the emitter of which is directly routed to EWOut output, with no internal resistor to ground. It is to be biased externally.

Figure 12. Geometric corrections' schematic diagram

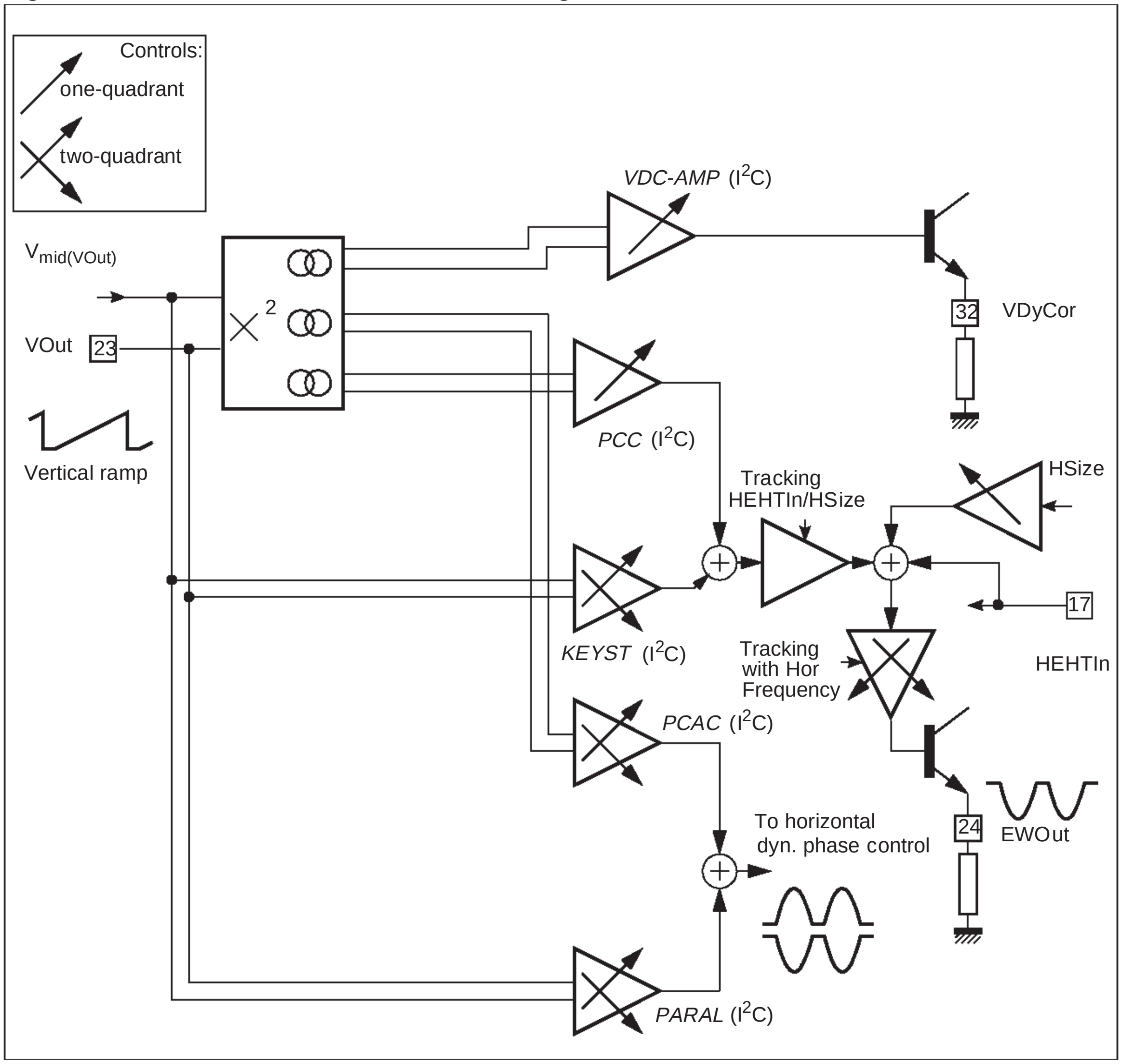
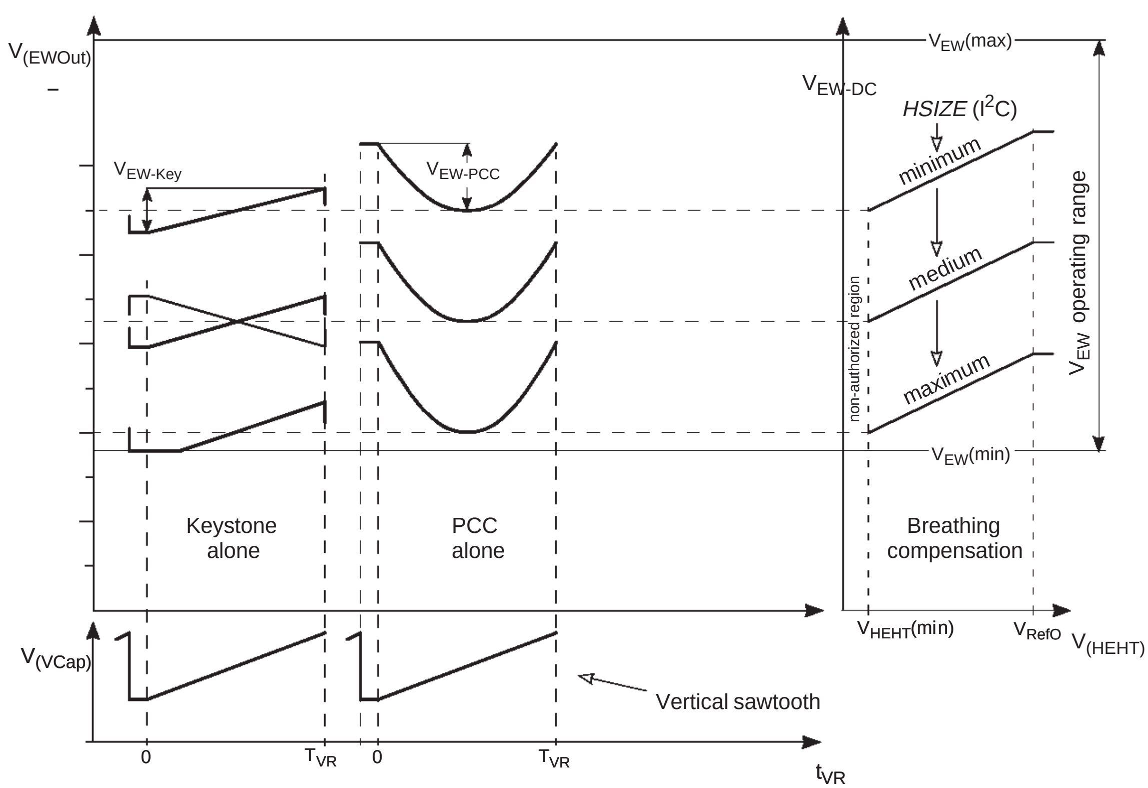


Figure 13. EWOut output waveforms



9.6 DYNAMIC CORRECTION OUTPUT SECTION

9.6.1 Vertical Dynamic Correction output VDyCor

A parabola at vertical deflection frequency is available on pin VDyCor. Its amplitude is adjustable via *VDC-AMP* I^2C bus control. It tracks with real vertical amplitude and position (including breathing compensation). It is also affected by C- and S-corrections.

The use of this correction waveform is up to the application (e.g. dynamic focus).

9.7 DC/DC CONTROLLER SECTION

The section is designed to control a switch-mode DC/DC converter. A switch-mode DC/DC convertor generates a DC voltage from a DC voltage of different value (higher or lower) with little power losses. The DC/DC controller is synchronized to horizontal deflection frequency to minimize potential interference into the picture.

Its operation is similar to that of standard UC3842.

The schematic diagram of the DC/DC controller is in Figure 14. The BOut output controls an external switching circuit (a MOS transistor) delivering pulses synchronized on horizontal deflection frequency, the phase of which depends on I^2C bus configuration, see the table at the end of this chapter. Their duration depends on feedback provided to the circuit, generally a copy of DC/DC converter output voltage and a copy of current passing through the DC/DC converter circuitry (e.g. current through external power component). The polarity of the output can be controlled by BOutPol I^2C bus bit. A NPN transistor open-collector is routed out to the BOut pin.

During the operation, a sawtooth is to be found on pin BISense, generated externally by the application. According to BOutPh I^2C bus bit, the R-S flip-flop is set either at H-drive signal edge (rising or falling, depending on BOHEdge I^2C bus bit), or a certain delay ($t_{BTrigDel}$ / T_H) after middle of H-flyback. The output is set On at the end of a short pulse generated by the monostable trigger.

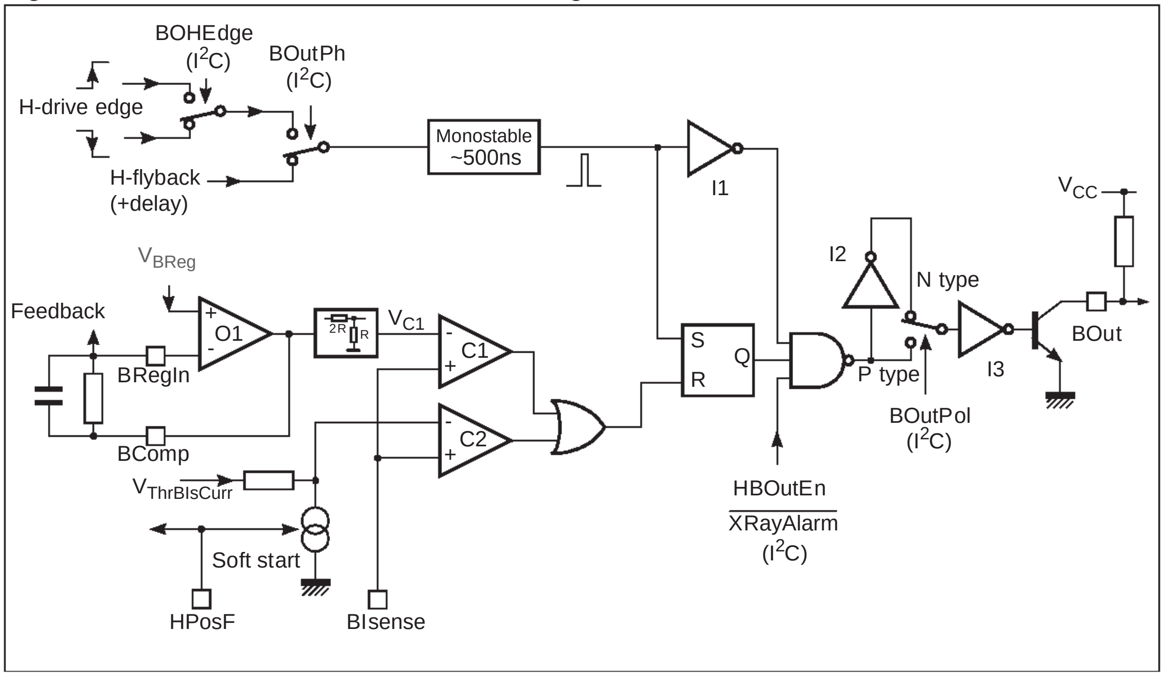
Timing of reset of the R-S flip-flop affects duty cycle of the output square signal and so the energy transferred from DC/DC converter input to its output. A reset edge is provided by comparator C2 if the voltage on pin BISense exceeds the internal threshold $V_{ThrBIsCurr}$. This represents current limitation if a voltage proportional to the current through the power component or deflection stage is available on pin BISense. This threshold is affected by the voltage on pin HPosF, which rises at soft start and descends at soft stop. This ensures self-contained soft control of duty cycle of the output signal on pin BOut. Refer to Figure 10. Another condition for the reset of the R-S flip-flop, OR-ed with the one described before, is that the voltage on pin BISense exceeds the voltage V_{C1}, which depends on the voltage applied on input BISense of the error amplifier O1. The two voltages are compared, and the reset signal generated by the comparator C1. The error amplifier amplifies (with a factor defined by external components) the difference between the input voltage proportional to DC/DC convertor output voltage and internal reference V_{BReg}.

Both step-up (DC/DC converter output voltage higher than its input voltage) and step-down (output voltage lower than input) are possible.

DC/DC controller Off-to-On edge timing

BOutPh (Sad07/ D7)	BOHEdge (Sad17/ D3)	Timing of Off-to-On transition on BOut output
0	don't care	Middle of H-flyback plus $t_{BTrigDel}$
1	0	Falling edge of H-drive signal
1	1	Rising edge of H-drive signal

Figure 14. DC/DC converter controller block diagram



9.8 MISCELLANEOUS

9.8.1 Safety functions

The safety functions comprise supply voltage monitoring with appropriate actions, soft start and soft stop features on H-drive and B-drive signals on HOut and BOut outputs and X-ray protection.

For supply voltage supervision, refer to paragraph Power supply and voltage references on page 23 and Figure 1. A schematic diagram putting together all safety functions and composite PLL1 lock and V-blanking indication is in Figure 15.

9.8.2 Soft start and soft stop functions

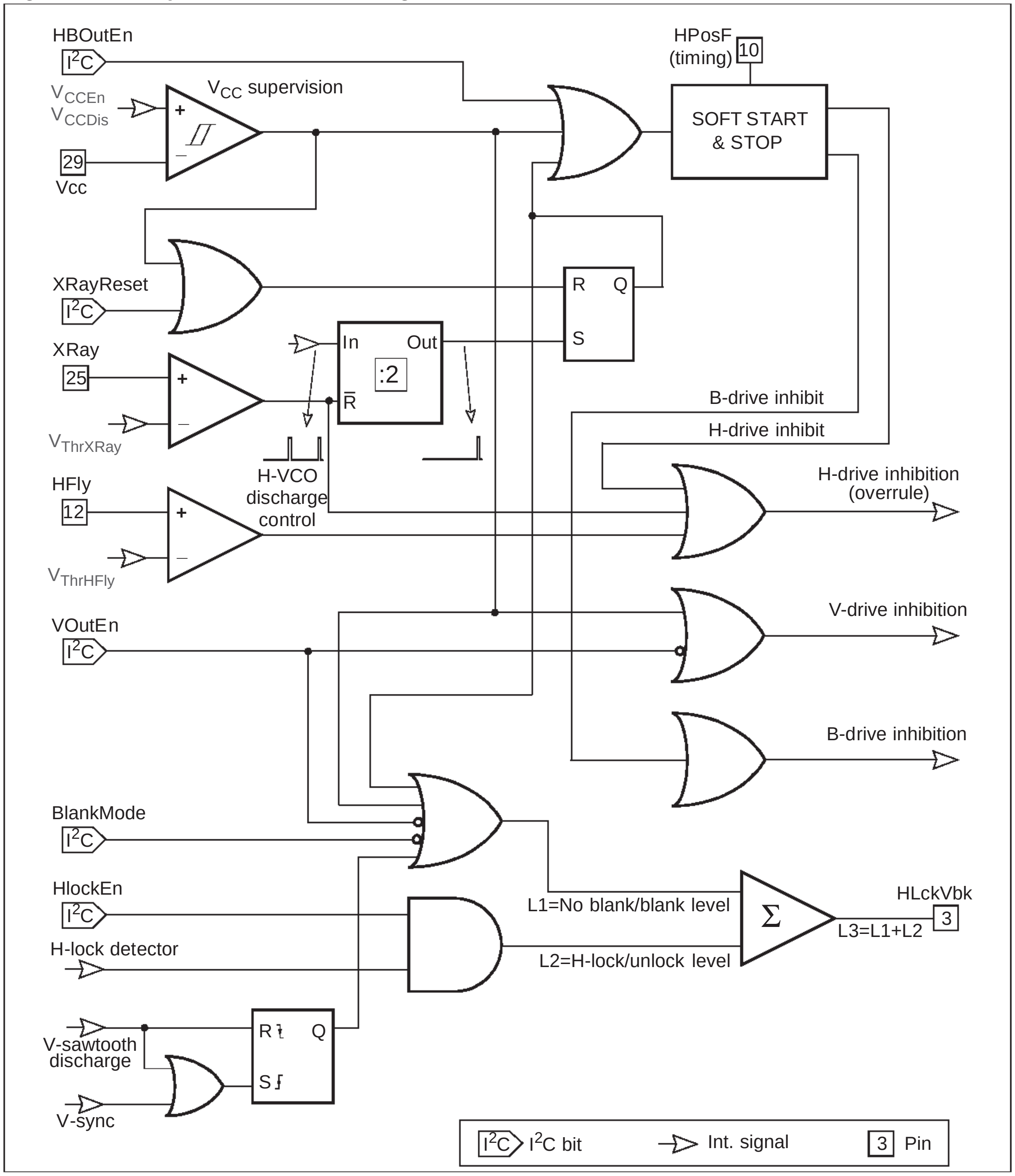
For soft start and soft stop features for H-drive and B-drive signal, refer to paragraph Soft-start and soft-stop on H-drive on page 27 and sub chapter-DC/DC CONTROLLER SECTION on page 31, respectively. See also the Figure 10. Regardless why the H-drive or B-drive signal are switched on or off (I^2C bus command, power up or down, X-ray protection), the signals always phase-in and phase-out in the way drawn in the figure, the first to phase-in and last to phase-out being the H-drive signal, which is to better protect the power stages at abrupt changes like switch-on and off. The timing of phase-in and phase-out only depends on the capacitance connected to HPosF pin which is virtually unlimited for this function. Yet it has a dual function (see paragraph PLL1 on page 24), so a compromise thereof is to be found.

9.8.3 X-ray protection

The X-ray protection is activated if the voltage level on XRay input exceeds $V_{ThrXRay}$ threshold. As a consequence, the H-drive and B-drive signals on HOut and BOut outputs are inhibited (switched off) after a 2-horizontal deflection line delay provided to avoid erratic excessive X-ray condition detection at short parasitic spikes.

This protection is latched; it may be reset either by V_{CC} drop or by I^2C bus bit XRayReset (see chapter I^2C BUS CONTROL REGISTER MAP on page 20).

Figure 15. Safety functions - block diagram

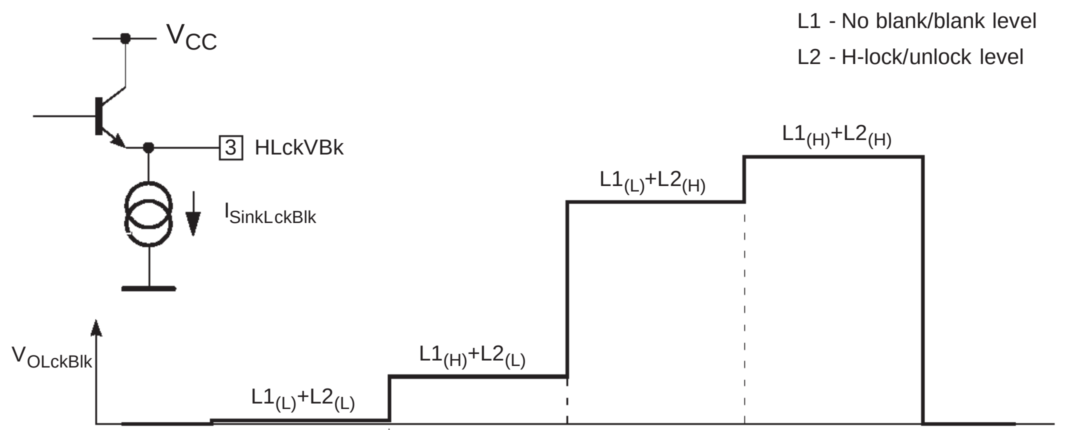


9.8.4 Composite output HLckVBk

The composite output HLckVBk provides, at the same time, information about lock state of PLL1 and early vertical blanking pulse. As both signals have two logical levels, a four level signal is used to define the combination of the two. Schematic diagram putting together all safety functions and composite PLL1 lock and V-blanking indication is in Figure 15, the combinations, their respective levels and the HLckVBk configuration in Figure 16.

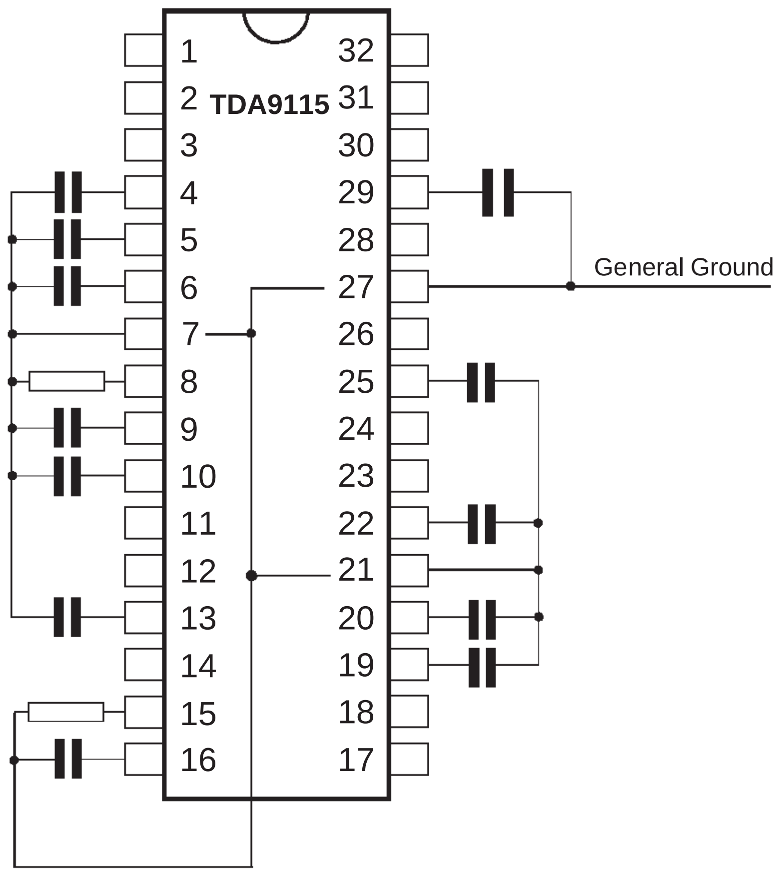
The early vertical blanking pulse is obtained by a logic combination of vertical synchronization pulse and pulse corresponding to vertical oscillator discharge. The combination corresponds to the drawing in Figure 16. The blanking pulse is started with the leading edge of any of the two signals, whichever comes first. The blanking pulse is ended with the trailing edge of vertical oscillator discharge pulse. The device has no information about the vertical retrace time. Therefore, it does not cover, by the blanking pulse, the whole vertical retrace period. By means of BlankMode I^2C bus bit, when at 1 (default), the blanking level (one of two according to PLL1 status) is made available on the HLckVBk permanently. The permanent blanking, irrespective of the BlankMode I^2C bus bit, is also provided if the supply voltage is low (under V_{CCEn} or V_{CCDis} thresholds), if the X-ray protection is active or if the V-drive signal is disabled by VOutEn I^2C bus bit.

Figure 16. Levels on HLckVBk composite output



V-early blanking	No	Yes	No	Yes
HPLL1 locked	Yes	Yes	No	No

Figure 17. Ground layout recommendations



10 - INTERNAL SCHEMATICS

Figure 18.

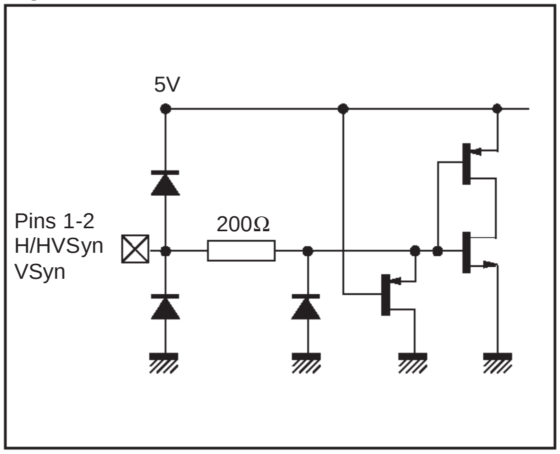


Figure 19.

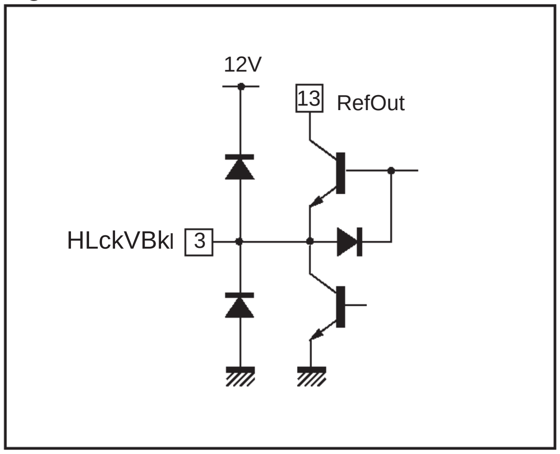


Figure 20.

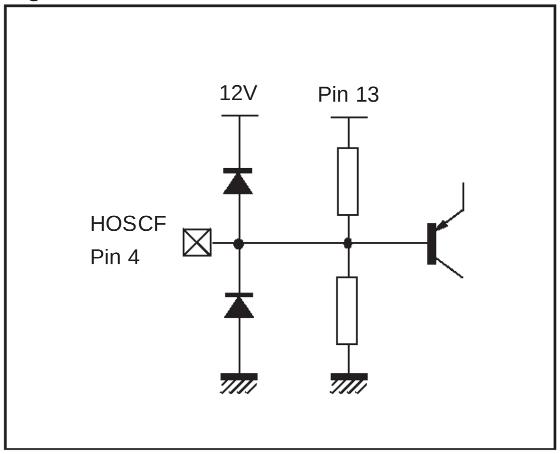
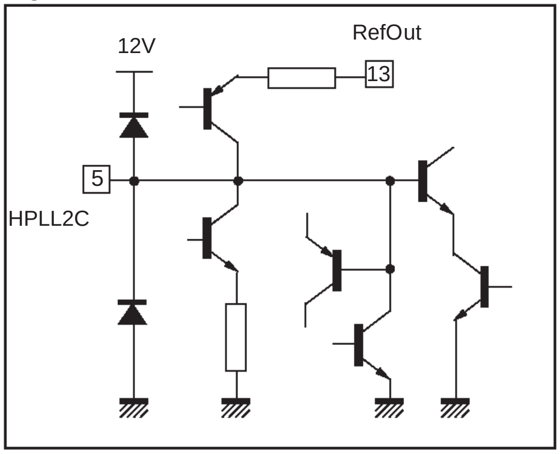


Figure 21.



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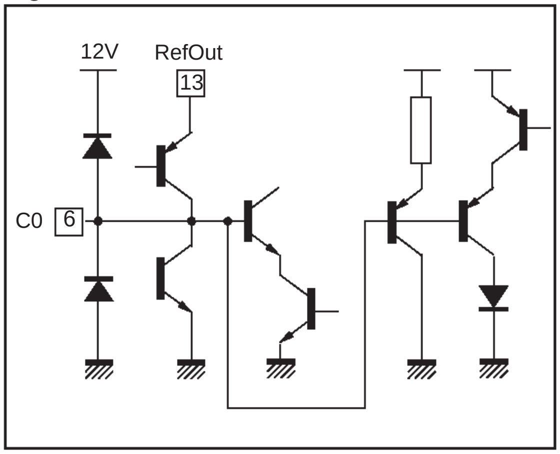

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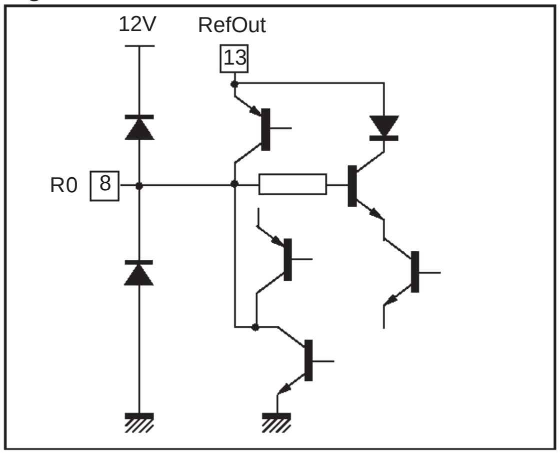

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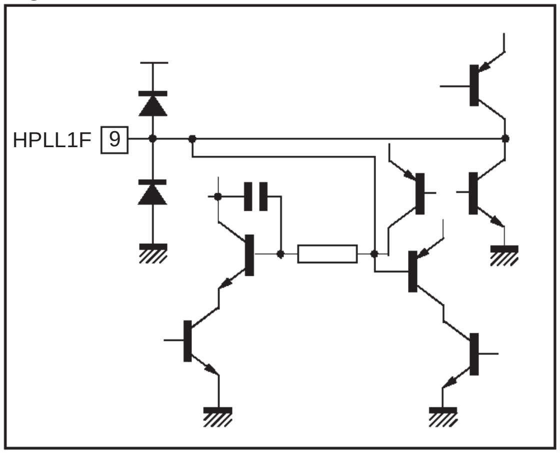
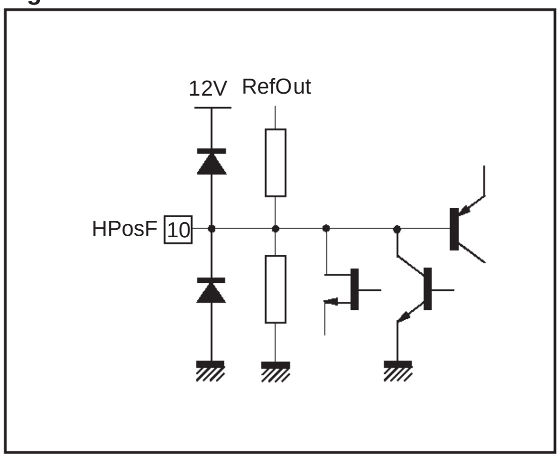


Figure 25.



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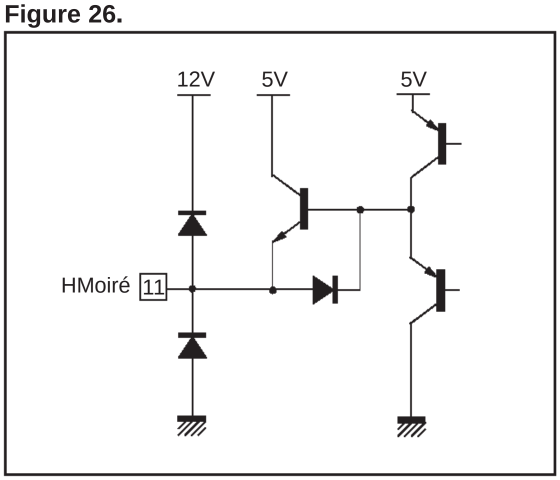

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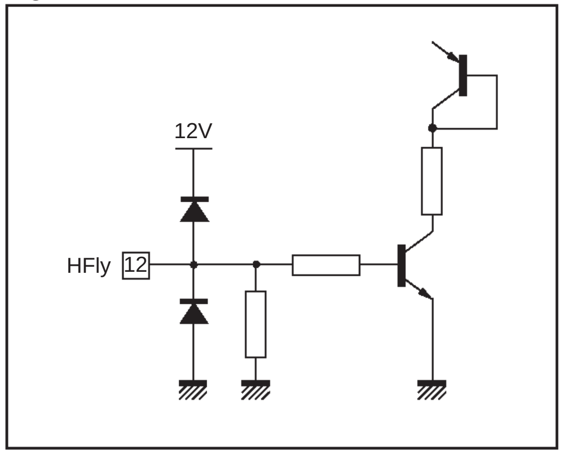


Figure 28.

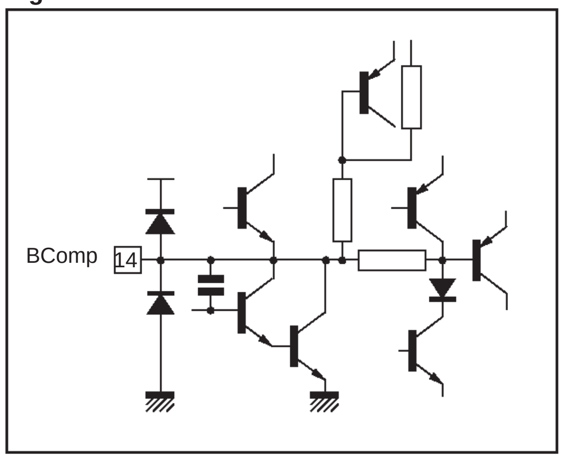


Figure 29.

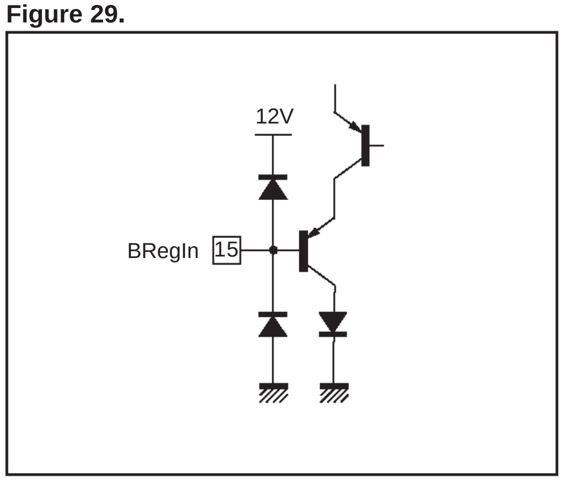


Figure 30.

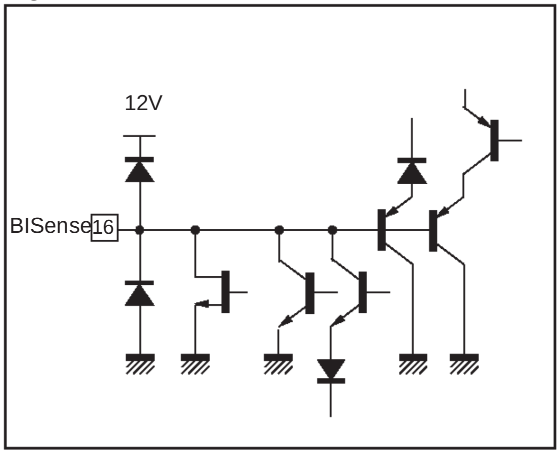


Figure 31.

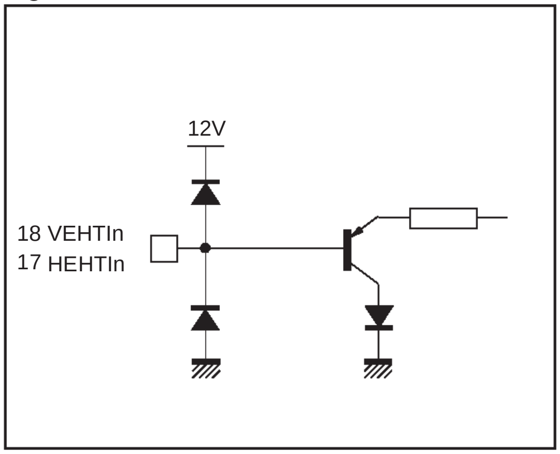


Figure 32.

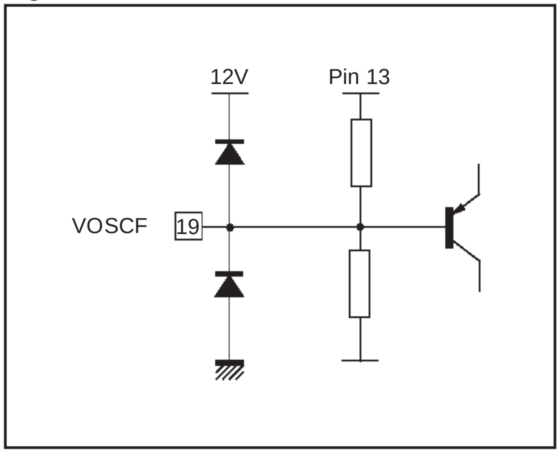
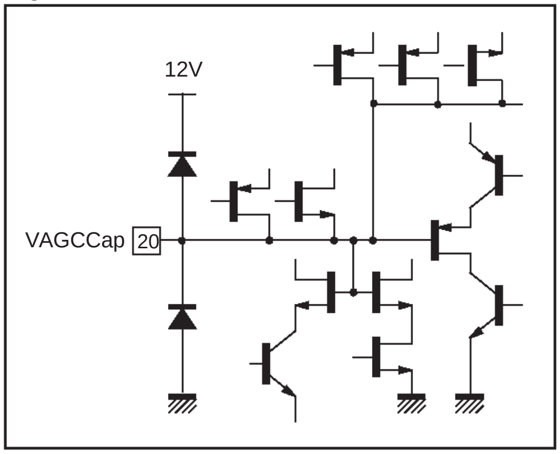


Figure 33.



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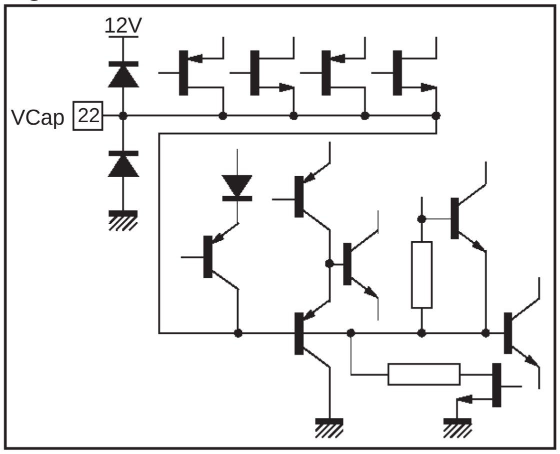

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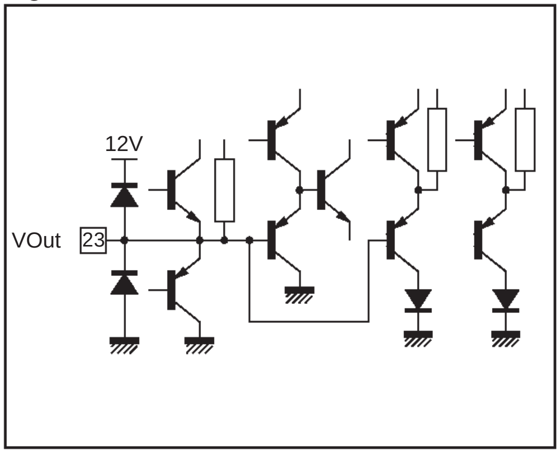

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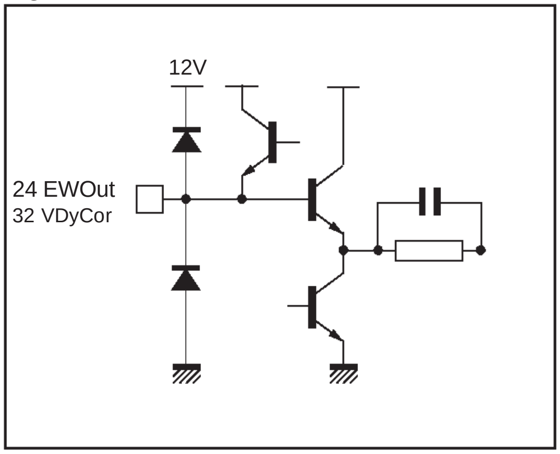

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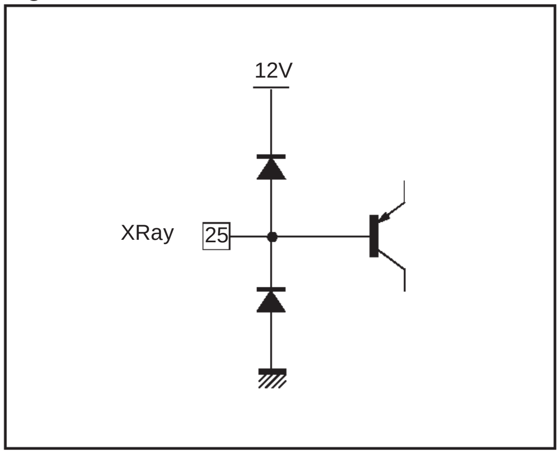

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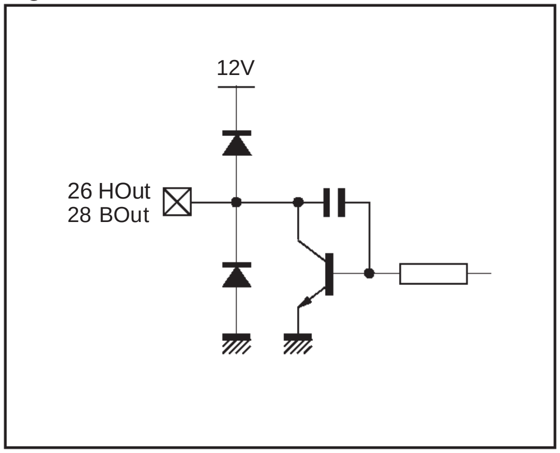
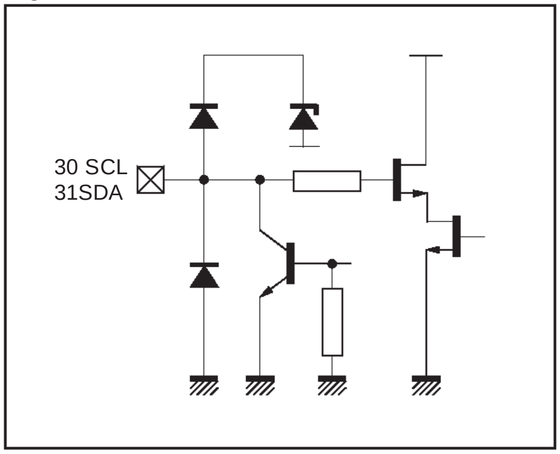
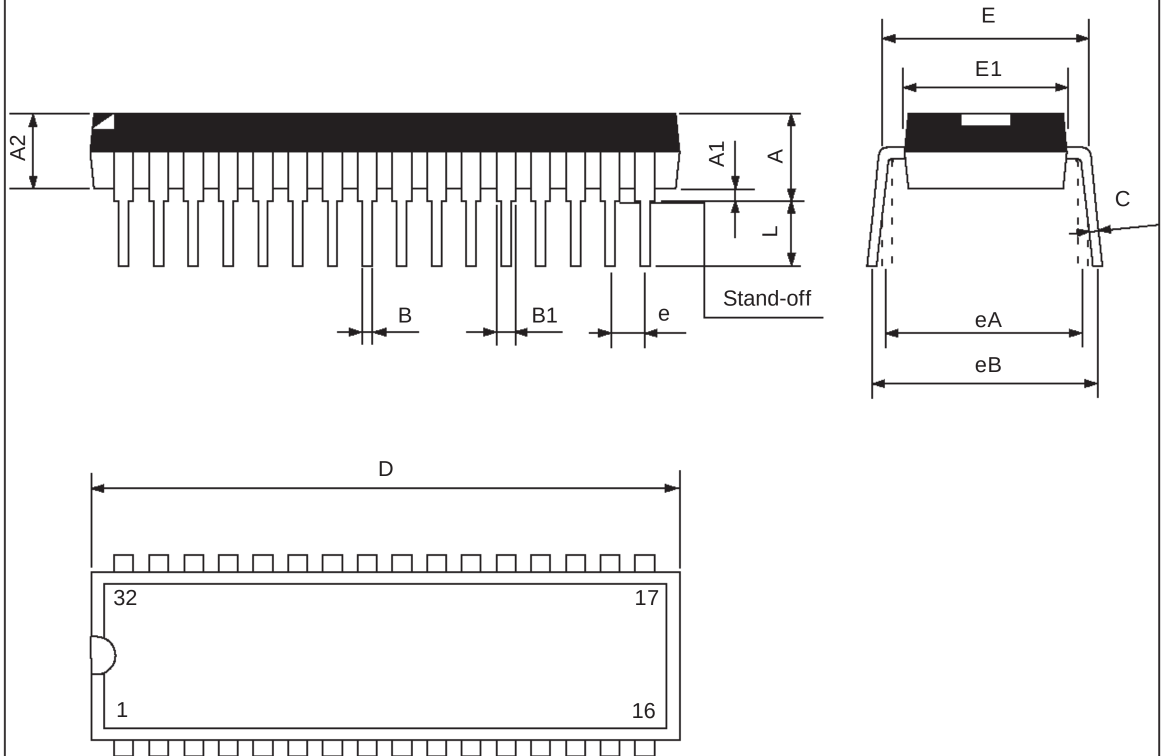


Figure 39.



11 - PACKAGE MECHANICAL DATA

32 PINS - PLASTIC SHRINK



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.556	3.759	5.080	0.140	0.148	0.200
A1	0.508			0.020		
A2	3.048	3.556	4.572	0.120	0.140	0.180
B	0.356	0.457	0.584	0.014	0.018	0.023
B1	0.762	1.016	1.397	0.030	0.040	0.055
C	.203	0.254	0.356	0.008	0.010	0.014
D	27.43	27.94	28.45	1.080	1.100	1.120
E	9.906	10.41	11.05	0.390	0.410	0.435
E1	7.620	8.890	9.398	0.300	0.350	0.370
e		1.778			0.070	
eA		10.16			0.400	
eB			12.70			0.500
L	2.540	3.048	3.810	0.100	0.120	0.150

12 - GLOSSARY

AC	**Al**ternate **C**urrent
ACK	**ACK**nowledge bit of I²C-bus transfer
AGC	**A**utomatic **G**ain **C**ontrol
COMP	**COMP**arator
CRT	**C**athode **R**ay **T**ube
DC	**D**irect **C**urrent
EHT	**E**xtra **H**igh **V**oltage
EW	**E**ast-**W**est
H/W	**H**ard**W**are
HOT	**H**orizontal **O**utput **T**ransistor
I^2C	**I**nter-**I**ntegrated **C**ircuit
IIC	**I**nter-**I**ntegrated **C**ircuit
MCU	**M**icro-**C**ontroller **U**nit
NAND	**N**egated **AND** (logic operation)
NPN	**N**egative-**P**ositive-**N**egative
OSC	**OSC**illator
PLL	**P**hase-**L**ocked **L**oop
PNP	**P**ositive-**N**egative-**P**ositive
REF	**REF**erence
RS, R-S	**R**eset-**S**et
S/W	**S**oft**W**are
TTL	**T**ransistor **T**ransistor **L**ogic
VCO	**V**oltage-**C**ontrolled **O**scillator

Revision follow-up

PRODUCT PREVIEW

June 2000 version 2.0

Document created (issued from TDA9112)

Work on figures and text; version finalized and displayed on Intranet.

July 2000 version 2.1

Sentence modified in first page : The internal sync processor.;." replaced by :"the device only requires..;"

Bloc diagram : addition of Hsize under E/W correction

Quick Reference Data: Addition of parrallelogram

Register Map: subaddress 08: 0:No tracking

Few corrections in text.

PRELIMINARY DATA

September 2000 version 3:0

Uniformity in the writing of cross references for notes.

In internal schematics, correction of figure for pin 11.

In bloc diagram: the line between PLL2 and HMoiré controller has been deleted

In Horizontal Moiré Cancellation: 1 sentence changed

VDC AMP replaced by VDC-AMP

In electrical parameters:

$\Delta V_{HMoiré}$ becomes $\Delta V_{AC\text{-}HMoiré}$

Addition of $V_{DC\text{-}HMoiré}$,.

January 11, 2001 version 3.1

page 6: value for autosync frequency ratio replaced : 4.28 instead of 4.5 previously.

April 19, 2001 version 3.2

page 16 Section 6.9 .Vtrh-XRay: new values 7.65 min, 7.9 typ., 8.2 max.

DATASHEET

July 18, 2001 version 4.0

Section 9.4.1 right column"The higher its value,..." ---> "The lower its value"

Section 9.5 ."...at the vertical middle..." ---> "...in the vertical middle..."

Section 6.6 : addition of [fmax] to parameter "ΔVEW/VEW[fmax].ΔVHO" .and changed its value to 20

Note 28: added: "VEW[fmax] is the value at condition VHO>VHOThrfr".

Section 6.4 : addition of min and max values for V_{HPosF} and $V_{TopHPLL2C}$

Section 6.5 addition of min and max values for V_{VOB} + correction of typ. value

Section 6.8 addition of min and max values for $V_{ThrBlsCurr}$ and V_{BReg}, max value added for V_{BOSat}

Section 6.9 addition of min and max values for V_{HPos}

Section 9.4 “stabilizing time” changed to “stabilization time” (twice)

Section 6.9 : max values for vertical moiré cancellers moved to typ. values

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