OKI Semiconductor

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MSM6636B

SAE-J1850 Multiplex Communication Protocol Conformity Transmission Controller for Automotive LAN

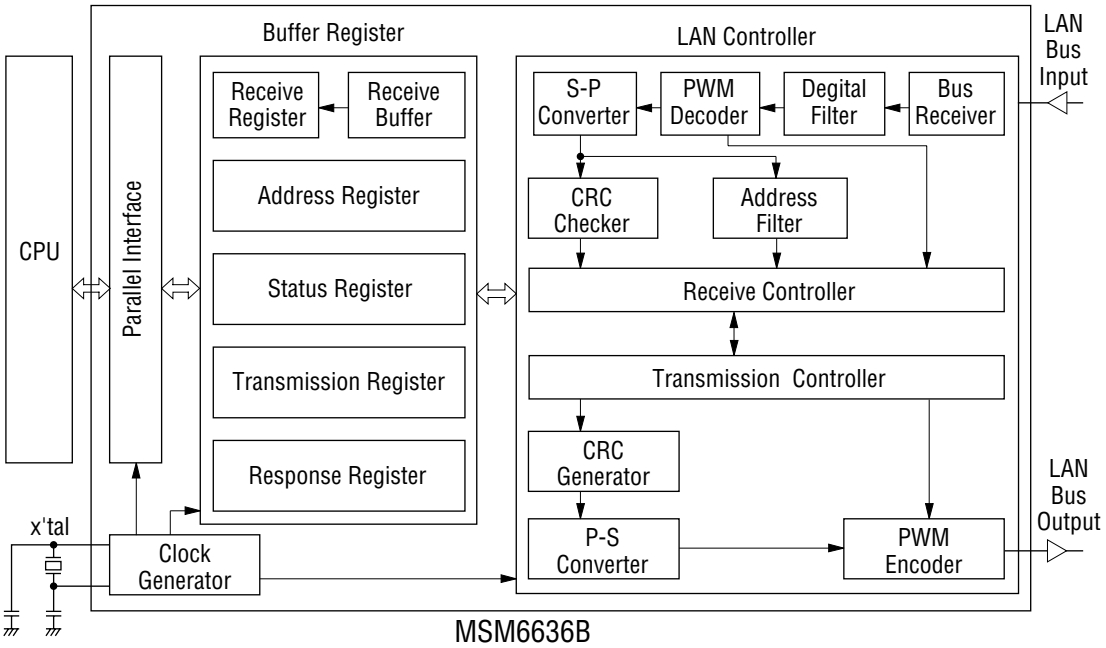
GENERAL DESCRIPTION

The MSM6636B is a transmission controller for automotive LAN based on data communication protocol SAE-J1850. This device can realize a data bus topology bus LAN system with a PWM bit encoding method (41.6 kbps). In addition to a protocol control circuit, MSM6636B has an enclosed quartz oscillation circuit, host CPU interface (parallel interface), a transmit/receive buffer, and a bus receiver circuit that decreases the burden on the host CPU.

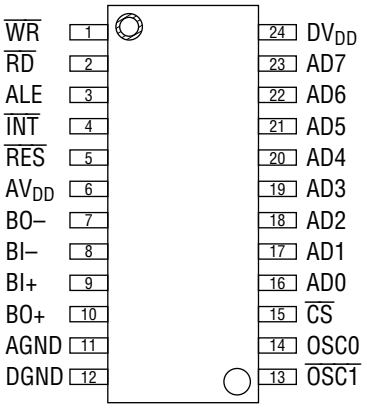
FEATURES

- Based on SAE-J1850 CLASS B DATA COMMUNICATION NETWORK INTERFACE (issued August 12, 1991)
- Non-destructive collision and priority control using CSMA/CD
- Internal transmit buffer (1 frame) and receive buffer (2 frames)
- Modulating/demodulating: PWM (Pulse Width Modulation)
- Transmission speed: 41.6 kbps
- Multi-address setting with physical addressing: 1 type / functional addressing: 15 types
- Address filter function by multi-addressing (broadcasting possible)
- Automatic retransmission function by arbitration loss and non ACK
- Three types of in-frame response support:
  ① Single-byte response from a single node
  ② Multi-byte response from a single node (with CRC code)
  ③ Single-byte response from multiple nodes (ID response as ACK)
- Error detection by cyclic redundancy check (CRC)
- Various communication error detections
- Dual-wire bus abnormality detection by internal bus receiver and fault tolerance function
- Host CPU interface is accessed in parallel
- Sleep function
  Low current consumption mode by oscillation stop (IDS Max < 50µA)
  SLEEP / WAKE UP control from host CPU, WAKE UP via LAN bus
- Package: 24-pin plastic SOP (SOP24-P-430-1.27-K) (Product name : MSM6636BGS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



24-Pin Plastic SOP

PIN DESCRIPTION

Pin	Symbol	Type	Description
1	$\overline{WR}$	I	Data write enable input pin
2	$\overline{RD}$	I	Data read enable input pin
3	ALE	I	Address latch input pin
4	$\overline{INT}$	O	Interrupt output pin
5	$\overline{RES}$	I	Reset input pin
6	AV_{DD}	—	Analog power supply voltage
7	BO–	O	LAN—BUS output –
8	BI–	I	LAN—BUS input –
9	BI+	I	LAN—BUS input +
10	BO+	O	LAN—BUS output +
11	AGND	—	Analog ground pin
12	DGND	—	Digital ground pin
13	$\overline{OSC1}$	O	Crystal (or ceramic resonator) oscillation output
14	OSC0	I	Crystal (or ceramic resonator) oscillaiton input
15	$\overline{CS}$	I	Chip select input pin
16-23	AD0-7	I/O	Address input/data input-output pin
24	DV_{DD}	—	Digital power supply voltage

ABSOLUTE MAXIMUM RATINGS

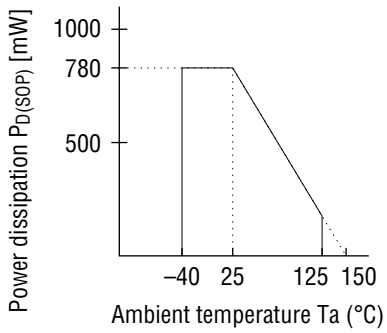
DGND=AGND=0V

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	DV_{DD}, AV_{DD}	—	–0.3 to +7.0	V
Input Voltage	V_I	$AV_{DD}=DV_{DD}$	–0.3 to DV_{DD}+0.3	V
Output Voltage	V_O	$AV_{DD}=DV_{DD}$	–0.3 to DV_{DD}+0.3	V
Power Dissipation	$P_{D(SOP)}$*1	Ta=25°C	780	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

*1 24-pin SOP package power dissipation

Power Dissipation Curve

< 24-pin SOP package>



RECOMMENDED OPERATING CONDITIONS

DGND=AGND=0V

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	DV_{DD}, AV_{DD}	AV_{DD}=DV_{DD}	4.5 to 5.5	V
Operating Frequency	f_{OSC}	DV_{DD}=AV_{DD}=5V±10%	2 to 16	MHz
Ambient Temperature	Ta	—	–40 to +85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

DV_{DD}=AV_{DD}=5V±10%, DGND=AGND=0V, Ta=–40 to +85°C

Parameter	Symbol	Condition	Applied pin (see below for A-E)	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH1}	—	A	$DV_{DD} \times 0.8$	—	DV_{DD}+0.3	V
"L" Input Voltage	V_{IL1}	—	A	DGND–0.3	—	$DV_{DD} \times 0.2$	V
"H" Input Voltage	V_{IH2}	—	E	$DV_{DD} \times 0.7$	—	DV_{DD}+1.0	V
"L" Input Voltage	V_{IL2}	—	E	DGND–1.0	—	DGND × 0.3	V
"H" Input Voltage	V_{IH3}	—	B	2.4	—	DV_{DD}+0.3	V
"L" Input Voltage	V_{IL3}	—	B	–0.3	—	0.8	V
Receiver Hysteresis Width	V_H	—	E	100	—	400	mV
"H" Input Current	I_{IH1}	V_I=V_{DD}	B	—	—	+1	µA
"L" Input Current	I_{IL1}	V_I=0V	B	—	—	–1	µA
"H" Input Current	I_{IH2}	V_I=V_{DD}	$\overline{RES}$	—	—	+1	µA
"L" Input Current	I_{IL2}	V_I=0V	$\overline{RES}$	—	—	–100	µA
"H" Input Current	I_{IH3}	V_I=V_{DD}	BI (+)	—	—	+100	µA
"L" Input Current	I_{IL3}	V_I=0V	BI (–)	—	—	–100	µA
"H" Output Voltage	V_{OH1}	I_O=–400µA	C, AD0–7	DV_{DD}–0.4	—	—	V
"L" Output Voltage	V_{OL1}	I_O=+3.2mA	C, AD0–7	—	—	DGND+0.4	V
"H" Output Voltage	V_{OH2}	I_O=–4.0mA	D	DV_{DD}–0.4	—	—	V
"L" Output Voltage	V_{OL2}	I_O=+4.0mA	D	—	—	DGND+0.4	V
GND Offset Voltage	V_{OFF}	—	—	—	—	±1	V
Current Consumption 1	I_{DS}	During sleep	—	—	*1	50	µA
Current Consumption 2	I_{DD}	f=16MHz, no load	—	—	—	10	mA

A: $\overline{RES}$, $\overline{CS}$
B: ALE, $\overline{WR}$, $\overline{RD}$, AD0-7
C: $\overline{INT}$
D: BO–, BO+
E: BI–, BI+

*1 Typ.=0.2µA when V_{DD}=5V, f=16 MHz, Ta=25°C

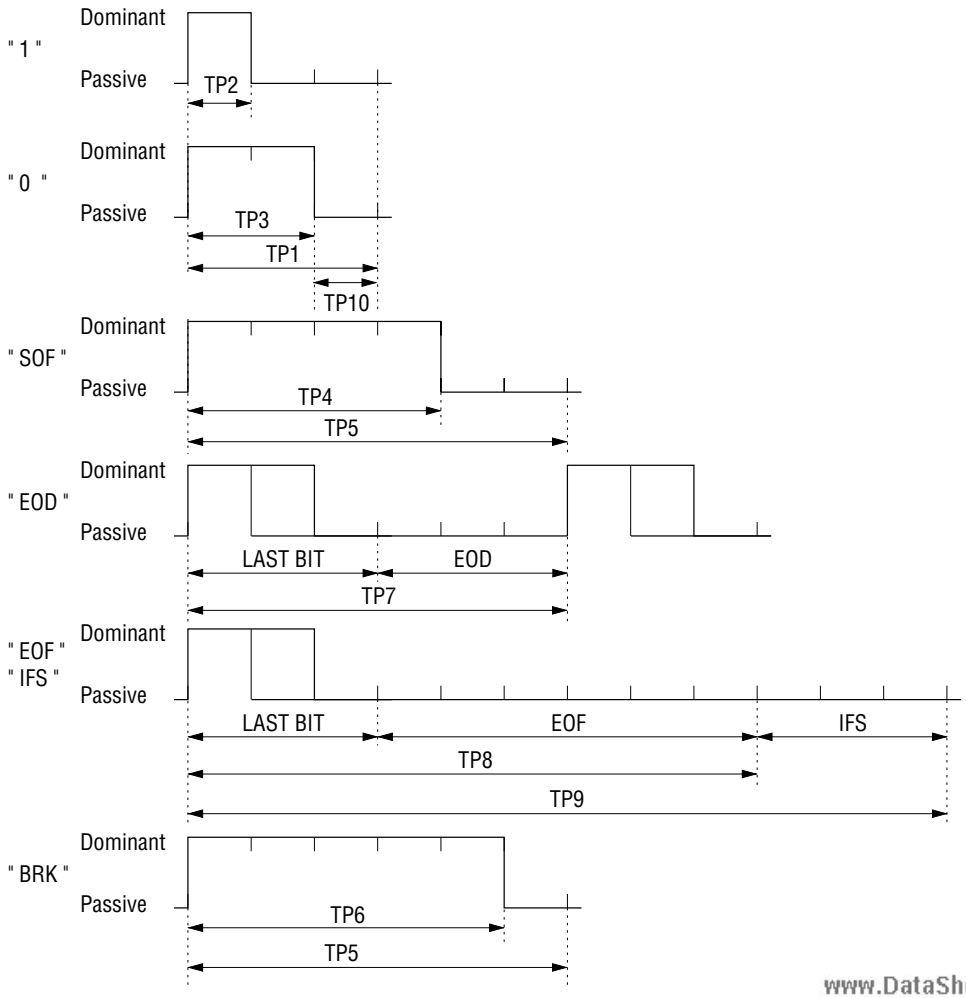
AC Chacteristics

- PWM bit timing

DV_{DD}=AV_{DD}=5V±10%, Ta=–40 to +85°C, In setting 41.6 kbps

Parameter	Symbol	Transmit			Receive		Unit
		min	typ	max	min	max	
Bit Length	TP1	23.64	24.00	24.36	21.00	28.00	µs
"1" Dominant Width	TP2	6.90	7.00	7.11	5.00	12.00	µs
"0" Dominant Width	TP3	14.87	15.00	15.23	13.00	20.00	µs
"SOF" Dominant Width	TP4	30.54	31.00	31.47	29.00	36.00	µs
"SOF, BRK" Length	TP5	47.28	48.00	48.72	45.00	52.00	µs
"BRK" Dominant Width	TP6	38.42	39.00	39.59	37.00	44.00	µs
"EOD" + Bit Length	TP7	47.28	48.00	48.72	43.00	51.00	µs
"EOF" + Bit Length	TP8	70.92	72.00	—	69.00	76.00	µs
"EOF + IFS" " + Bit Length	TP9	94.56	96.00	—	86.00	—	µs
"0" Passive Width	TP10	8.86	9.00	9.14	4.00	15.00	µs

Note: The sending timing in the above table does not include the delay of the bus drivers.

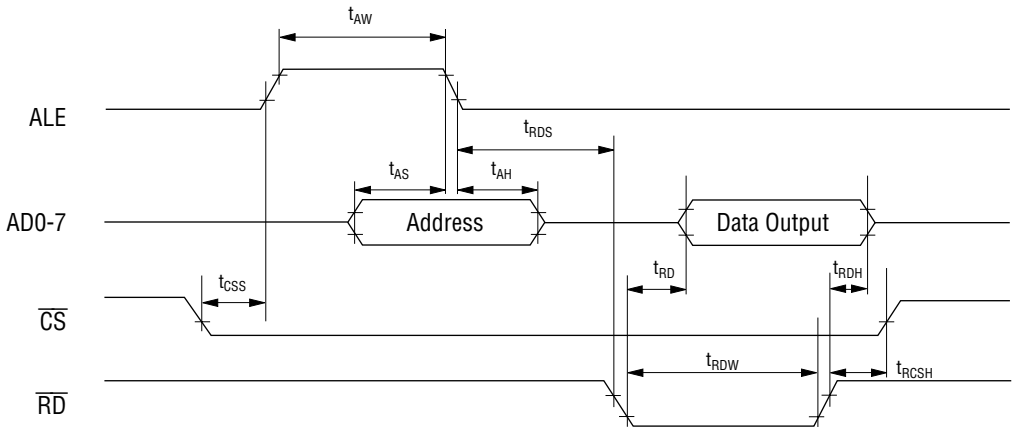


• CPU parallel interface timing

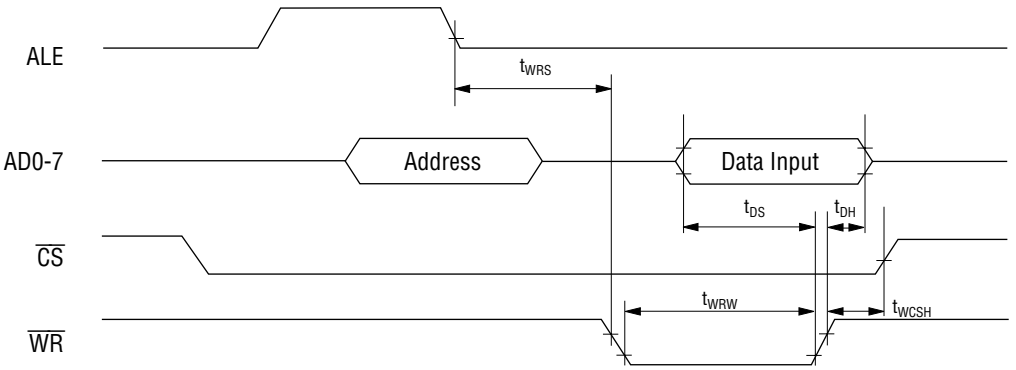
$DV_{DD}=AV_{DD}=5V\pm10\%$, Ta=–40 to +85°C

Parameter	Symbol	Measuring condition	Min.	Max.	Unit
ALE Pulse Width	t_{AW}	C_L=50pF	65	—	ns
Address Setup Time	t_{AS}		65	—	
Address Hold Time	t_{AH}		5	—	
$\overline{CS}$ Setup Time	t_{CSS}		50	—	
$\overline{RD}$ Setup Time	t_{RDS}		20	—	
Continuous Read Cycle Time	t_{RDCY}		160	—	
$\overline{RD}$ Output Enable Delay Time	t_{RD}		—	70	
$\overline{RD}$ Output Floating Delay Time	t_{RDH}		—	50	
$\overline{RD}$ Pulse Width	t_{RDW}		75	—	
$\overline{RD}$ Hold Time at Read	t_{RCSH}		0	—	
$\overline{WR}$ Setup Time	t_{WRS}		100	—	
Continuous Write Cycle Time	t_{WRCY}		160	—	
$\overline{WR}$ Pulse Width	t_{WRW}		75	—	
Data Setup Time	t_{DS}		100	—	
Data Hold Time	t_{DH}		40	—	
$\overline{CS}$ Hold Time at Write	t_{WCSH}		50	—	

Parallel Interface Timing

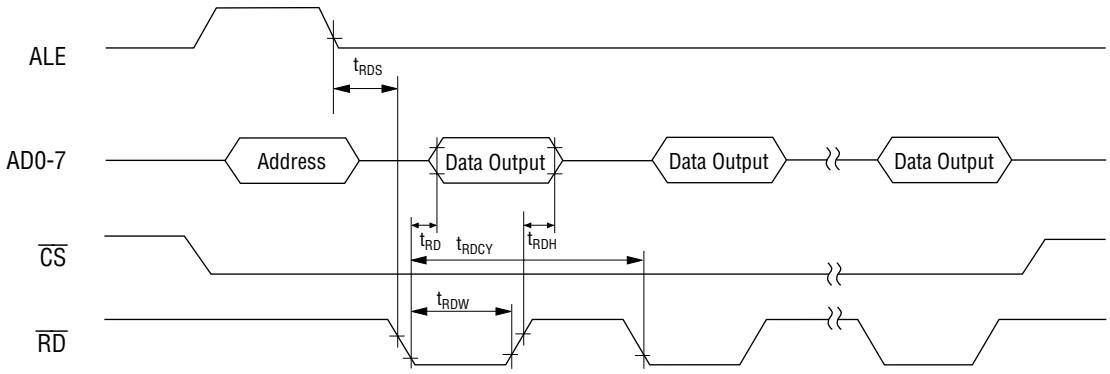


Read Timing

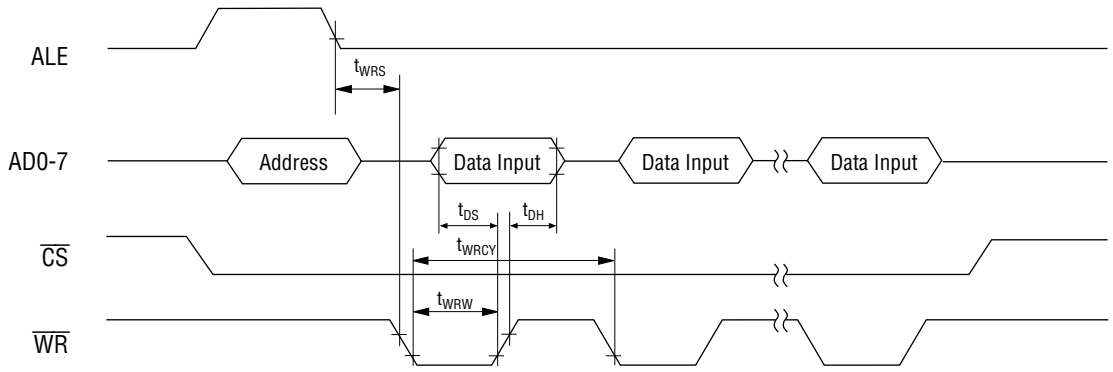


Write Timing

Timing When Automatic Address Increment is Used



Read Timing



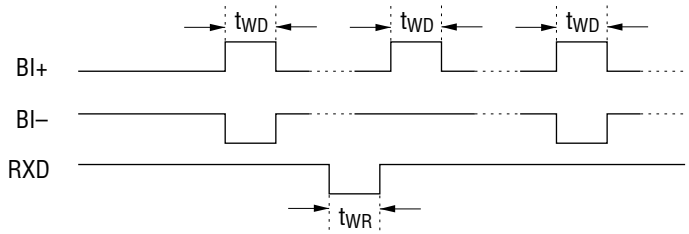
Write Timing

• Wakeup input signal

$DV_{DD}=AV_{DD}=5V\pm10\%$, Ta=–40 to +85°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
LAN bus Passive → Dominant Change Pulse Width	t_{WD}	7	—	—	µs
RXD Terminal Input Pulse Width	t_{WR}	400	—	—	ns
Bus Receiver Stable Time *1	t_{RS}	1	—	—	µs

*1 The stable time of the bus receiver is from just after wakeup to the restart of message transmission and reception. However, the clock oscillation source should use an external clock. (A clock is input even in the sleep status.)

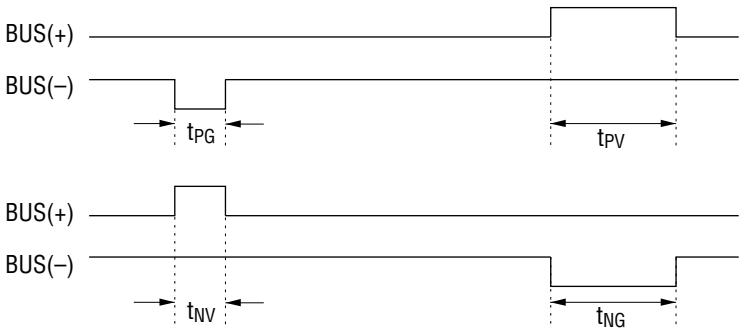


Note: The time chart shows the wakeup input signals from each sleep status.

• Fault tolerant function operation conditions

DV_{DD}=AV_{DD}=5V±10%, Ta=–40 to +85°C, In setting 41.6 kbps

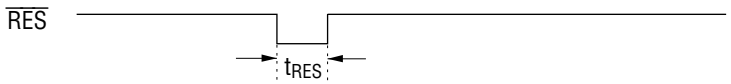
Parameter	Symbol	Min.	Typ.	Max.	Unit
LAN bus (+) GND Short Circuit Detection Pulse Width	t_{PG}	5	—	—	µs
LAN bus (+) V_{DD} Short Circuit Detection Pulse Width	t_{PV}	48	—	—	µs
LAN bus (–) GND Short Circuit Detection Pulse Width	t_{NG}	48	—	—	µs
LAN bus (–) V_{DD} Short Circuit Detection Pulse Width	t_{NV}	5	—	—	µs



• Reset input pulse width

DV_{DD}=AV_{DD}=5V±10%, Ta=–40 to +85°C

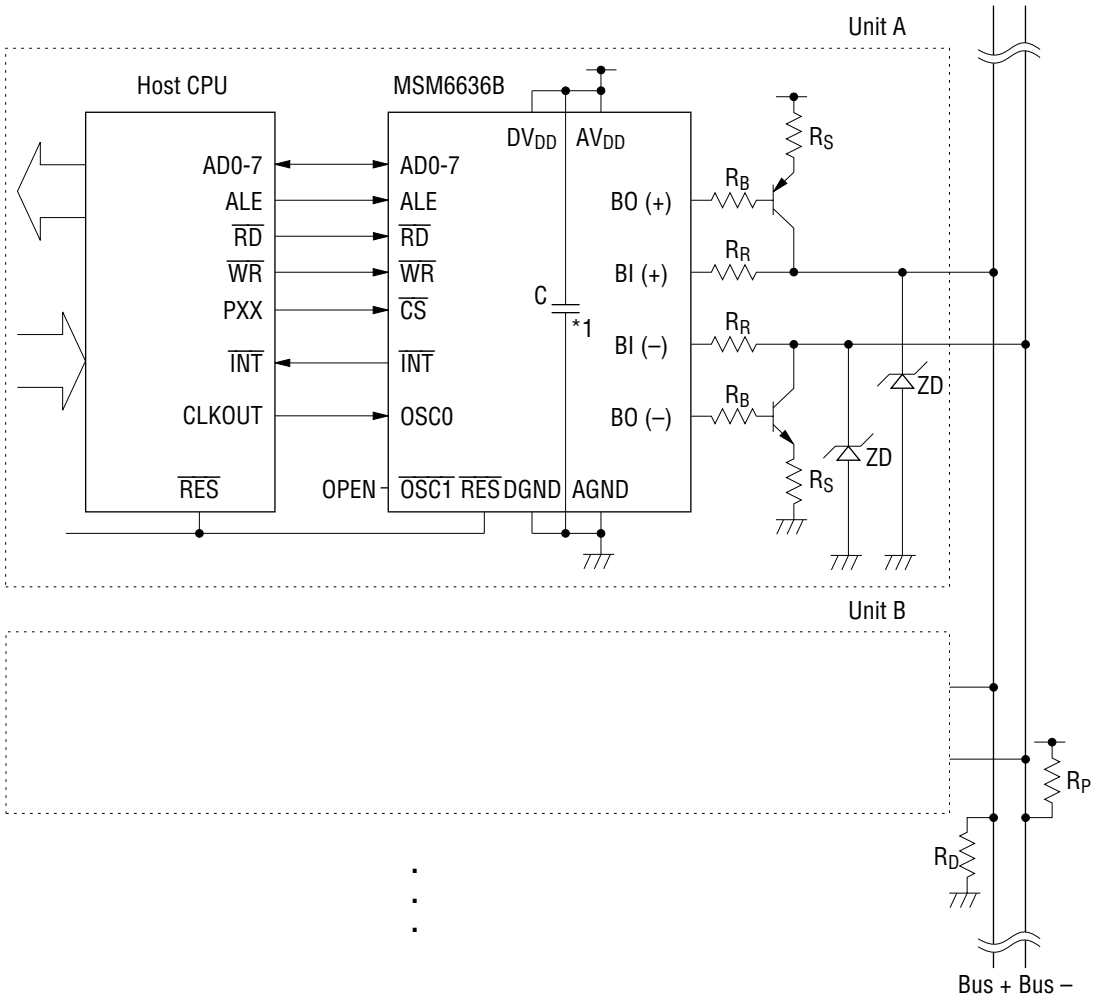
Parameter	Symbol	Min.	Typ.	Max.	Unit
Reset Input Pulse Width	t_{RES}	0.1	—	—	µs



Note: The oscillation stable time after power ON is determined by the crystal used and the parasitic capacitance generated by connection.
Make t_{RES} greater than or equal to the oscillation stable time.
In the table above, the reset input pulse width indicates the minimum pulse width when oscillation is stable after power is turned on.

APPLICATION CIRCUIT

Host CPU and J1850 Line Bus Connection Example



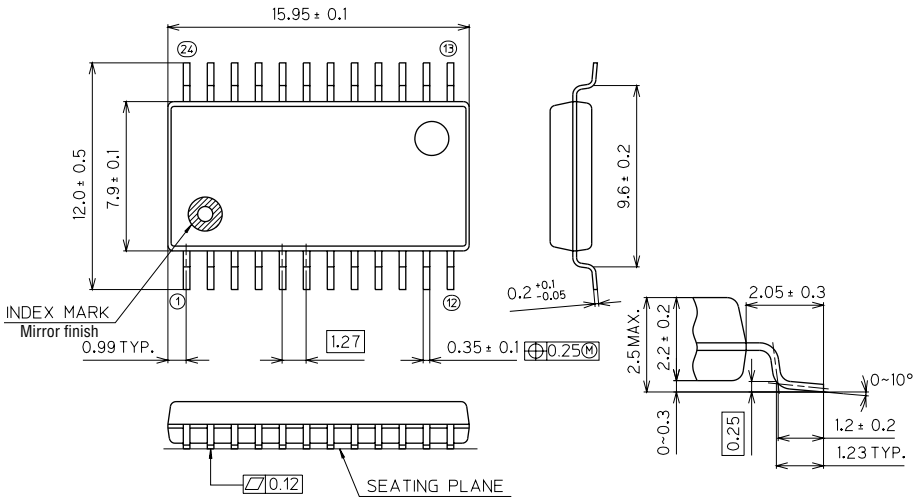
An optimum system can be constructed by selecting an optimum host CPU and combining it with the MSM6636B.

*1 Insert a capacitor between the power supply and GND to prevent supply noise.
It is recommended to connect a small-capacitance bypass capacitor and a large-capacitance filter capacitor serially. The typical capacitors are as follows:
0.01 to 0.22 µF : Ceramic capacitor
10 to 100 µF : Tantalum capacitor

PACKAGE DIMENSIONS

(Unit : mm)

SOP24-P-430-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).