OKI Semiconductor

This version: Feb. 1999
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MSC1157

Speaker Drive Amplifier

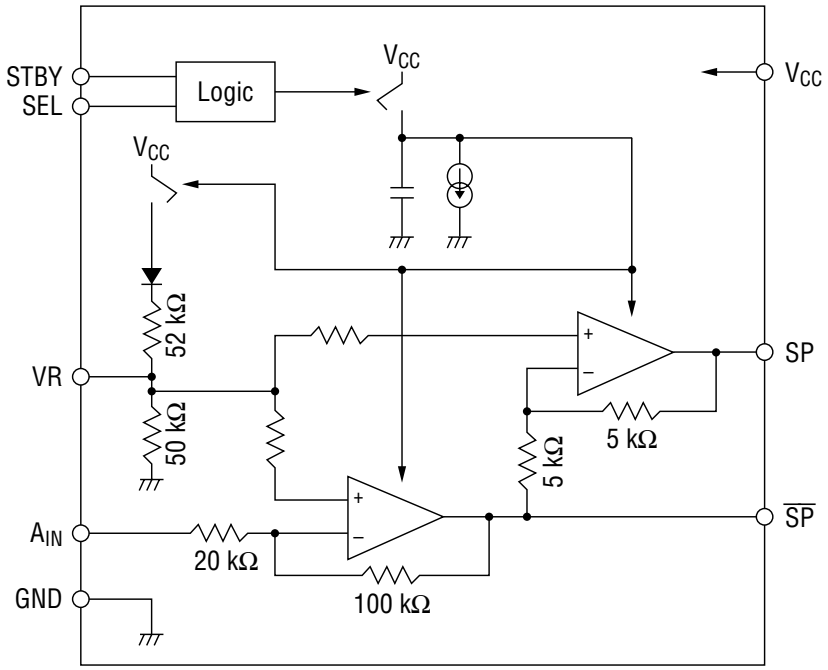
GENERAL DESCRIPTION

The MSC1157, designed specifically to operate at a low voltage with low current consumption, is a power amplifier developed for driving a speaker for a voice IC.
The voltage gains can be adjusted over a range of up to ten. The differential output can directly drive a speaker without any output coupling capacitors. The MSC 1157, because of its ability to stand by, is ideally suitable for portable equipment applications powered by a battery.

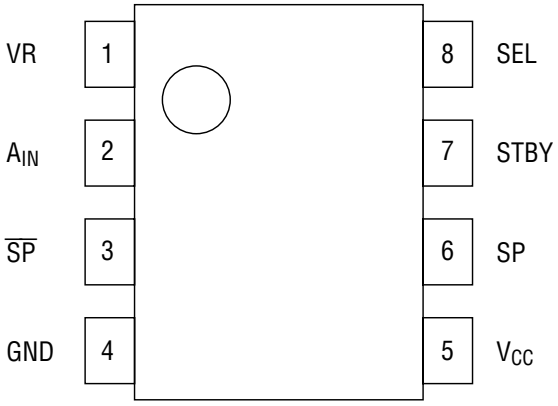
FEATURES

- Low voltage operation : 2.0 to 6.0 V (Single power supply)
- Low current dissipation
  Operating current : 1.6mA without load (typ.)
- Standby function : Current dissipation less than 1 µA in standby
- High output current : 350mA peak
- Differential outputs : A speaker can be directly connected between differential outputs.
- Adjustable gain : Gain can be adjusted by use of an external resistor.
- Package options:
  8-pin plastic DIP (DIP8-P-300-2.54) (Product name : MSC1157RS)
  8-pin plastic SOP (SOP8-P-250-1.27-K) (Product name : MSC1157MS-K)
  Chip

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



8-Pin Plastic DIP
or
8-Pin Plastic SOP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
5	V_{CC}	—	Power supply pin.
4	GND	—	Ground pin.
2	A_{IN}	I	Signal input pin for analog signal inputs, etc.
7, 8	STBY, SEL	I	Digital input pins. Setting these pins configures the standby status. See the table below for how to set the pins. SEL / STBY / Status 0 / 0 / Operation 0 / 1 / Standby 0 / Clock / Operation 1 / 0 / Standby 1 / 1 / Operation 1 / Clock / Operation Clock / 0 / Operation Clock / 1 / Operation Clock / Clock / Unstable Operation Applying a clock between 32kHz and 4MHz to either the STBY or the SEL pin leads the IC to operation status regardless of the status set at the other pin. Applying clocks to both of the pins at the same time may cause malfunction. Refer to the section, RECOMMENDED OPERATING CONDITIONS since clock frequencies are changed by setting the SEL pin.
1	VR	O	Bias output pin for internal circuits. This pin is at GND potential during standby. Connecting a capacitor between VR and the GND pin reduces the pop-up noise at power on and improves the ripple elimination ratio.
3	$\overline{SP}$	O	Speaker output pin. This pin outputs a negative phase with respect to the input signal.
6	SP	O	Speaker output pin. This pin outputs a positive phase with respect to the input signal.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Remark
Power Supply Voltage	V_{CC}	Ta=25°C	–0.3 to +6.5	V	V_{CC}
Input Voltage	V_{IN}	Ta=25°C	–0.3 to V_{CC}+0.3	V	STBY A_{IN}, SEL
Maximum Output Current	I_{OMAX}	Ta=25°C	(*1) ±400	mA	SP, $\overline{SP}$
Power Dissipation	P_D	Ta=25°C	470	mW	DIP type
			400	mW	SOP type
Junction Temperature	T_{jMAX}	—	125	°C	Chip
Storage Temperature	T_{STG}	—	–55 to +150	°C	

*1 Avoid shorting the output pins (SP and $\overline{SP}$) to V_{CC} or GND because the IC may be damaged.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	—	2.0	6.0	V
Load Impedance (*2)	RL	—	8.0	—	Ω
Peak Load Current	I_{O-P}	—	—	350	mA
"H" Input Voltage	V_{IH}	For STBY and SEL pins	0.7 V_{CC}	—	V
"L" Input Voltage	V_{IL}		—	0.3 V_{CC}	V
STBY Operating Frequency (*3)	f_{STBY}	SEL = "L" At clock input $V_{CC} \geq 2.4$ V	32 k	4.096 M	Hz
		SEL = "H" At clock input $V_{CC} \geq 2.4$ V	32 k	1 M	
Operating Temperature	Top	—	–20	+70	°C

*2 A speaker of 8 Ω (standard) or more should be used.
*3 The input of clocks may cause a little noise in output waveforms.
It is recommended to input the DC voltage to inprove voice quality.

ELECTRICAL CHARACTERISTICS

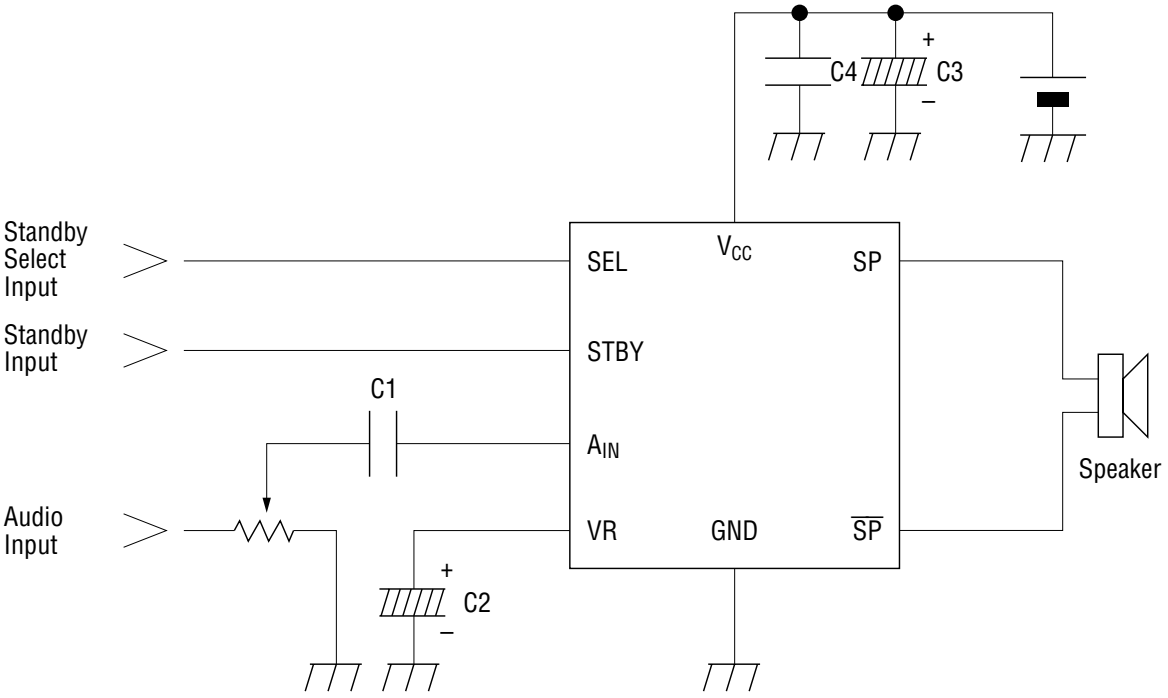
Unless otherwise specified, Ta=25°C, V_{CC}=2 to 6 V

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
A_{IN} Input Resistance	R_{IN}	—		14	20	26	kΩ
Voltage Gain	A_{V1}	$A_{IN}\rightarrow\overline{SP}$		13.44	14	14.49	dB
	A_{V2}	$\overline{SP}\rightarrow SP$		–1.94	0	+1.58	
	A_{V3}	$A_{IN}\rightarrow$(Between $\overline{SP}$-SP)		19.46	20	20.51	
Output Power	P_{OUT1}	V_{CC}=3 V, f=1 kHz RL=8 Ω, THD≥10%		100	178	—	mW
	P_{OUT2}	V_{CC}=6 V, f=1 kHz RL=32 Ω, THD≥10%		300	440	—	mW
Total Harmonic Distortion	THD1	V_{CC}=3 V, RL=8 Ω f=1 kHz, P_{OUT}=45 mW		—	1.2	—	%
	THD2	V_{CC}=6 V, RL=32 Ω f=1 kHz, P_{OUT}=125 mW		—	0.37	—	%
Ripple Elimination Ratio	RR	f=1 kHz, C2=4.7 µF		30	43	—	dB
Output DC Voltage (*4)	V_O	In no signal state	V_{CC}=2 V	0.53	0.65	0.77	V
			V_{CC}=6 V	2.49	2.61	2.73	
Output Offset Voltage	ΔV_O	Between SP-$\overline{SP}$		—	—	±30	mV
Output "H" Voltage	V_{OH}	A_{IN}=V_{CC} or GND I_{OUT}=–100 mA		V_{CC}–1.15	V_{CC}–1.04	—	V
Output "L" Voltage	V_{OL}	A_{IN}=V_{CC} or GND I_{OUT}=100 mA		—	0.17	0.3	V
STBY, SEL	I_{IH}	V_I=V_{CC}		—	—	±0.1	µA
Input Current	I_{IL}	V_I=GND		—	—	±0.1	µA
VR Equivalent Resistance	R_{VR}	—		18	25	32	kΩ
Circuit Current During Operation	I_{CC}	V_{CC}=6 V, RL=∞		1.1	1.6	2.4	mA
Circuit Current During Standby	I_{CCS}	—		—	—	1.0	µA

*4 The typical value of the output voltage in no signal state is determined from the following equation.

$$V_O = (V_{CC} - 0.67)\ \frac{50\ k\Omega}{50\ k\Omega + 52\ k\Omega}$$

APPLICATION CIRCUIT



- If parasitic capacitance of 60pF or more exists between GND and the speaker output pin $\overline{SP}$ or $\overline{SP}$, oscillation may occur. Implement the circuit mount design so as to be less than 60pF.

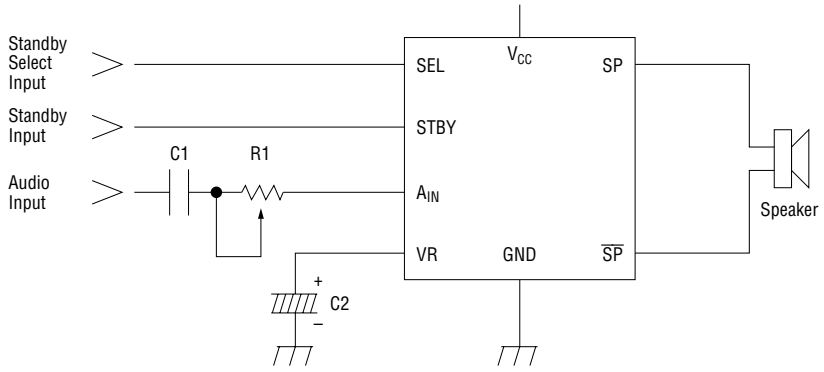
- C1 is the AC coupling capacitor. Cutoff frequency fc on the low frequency side is determined by the following equation. Choose a value of C1 according to the bandwidth.

$$fc = \frac{1}{2 \times \pi \times C1 \times 20k} \text{ (Hz)}$$

- Choose a value of C2 that is 80 to 100 times as large as that of C1.
- When the standby function is not used, connect the pins STBY and SEL to V_{CC} or GND.
- It is recommended that the capacitor C4 (approximately 0.1µF) having better high frequency characteristics and the capacitor C3 (approximately 10µF) be placed between the pins V_{CC} and GND.

GAIN ADJUSTMENT

1. Gain Adjustment Using Input Resistance (This approach allows gain adjustment with fewer external components)



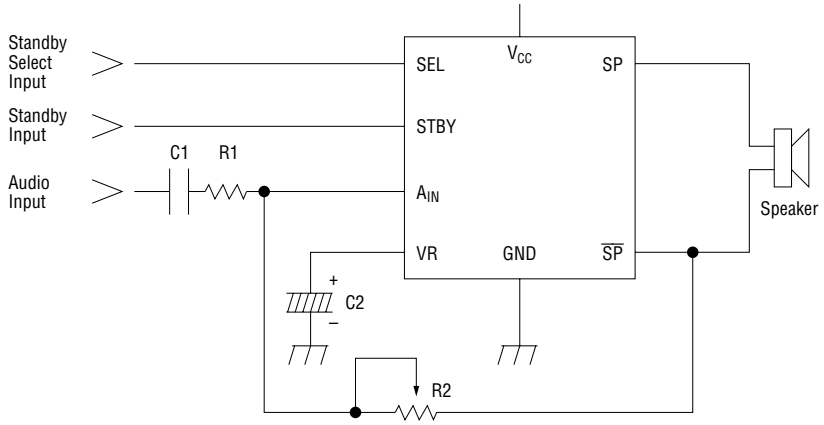
• Cutoff frequency fc on the low frequency side is determined from the equation:

$$fc \fallingdotseq \frac{1}{2 \times \pi \times C1 \times (R1 + 20k)} \quad (Hz)$$

• Voltage gain A_{V1} is determined from the equation:

$$A_{V1} \fallingdotseq \frac{100k}{R1 + 20k} \quad (V/V)$$

2. Gain Adjustment Using Feedback Resistance (This approach has the advantage over the above approach (less noise approach), but the number of components is increased)



• Cutoff frequency fc on the low frequency side is determined from the equation:

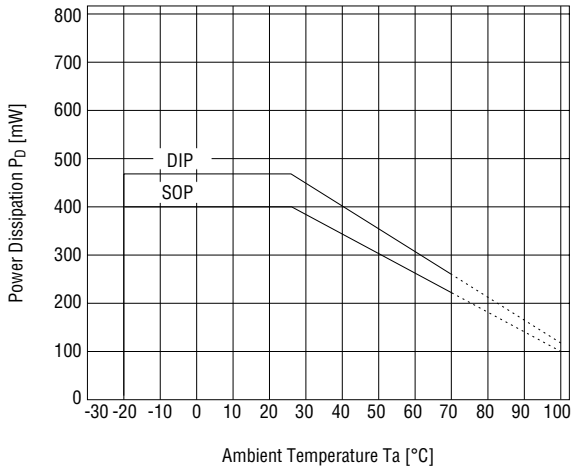
$$fc \fallingdotseq \frac{1}{2 \times \pi \times C1 \times Zin} \quad (Hz) \qquad Zin \fallingdotseq R1 + \frac{R2 \times 20k}{R2 + 120k} \quad (\Omega)$$

• Voltage gain A_{V1} is determined from the equation:

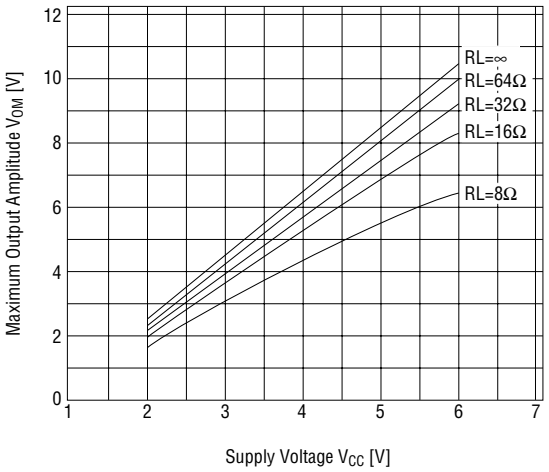
$$A_{V1} \fallingdotseq \frac{5}{1 + \frac{R1}{20k} + \frac{6 \times R1}{R2}} \quad (V/V)$$

OPERATING CHARACTERISTICS

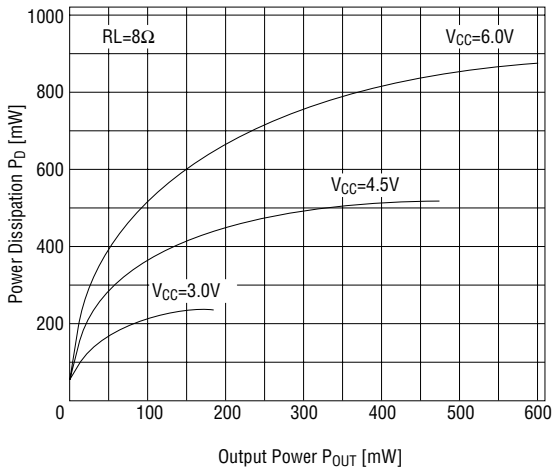
Power Dissipation vs. Ambient Temperature



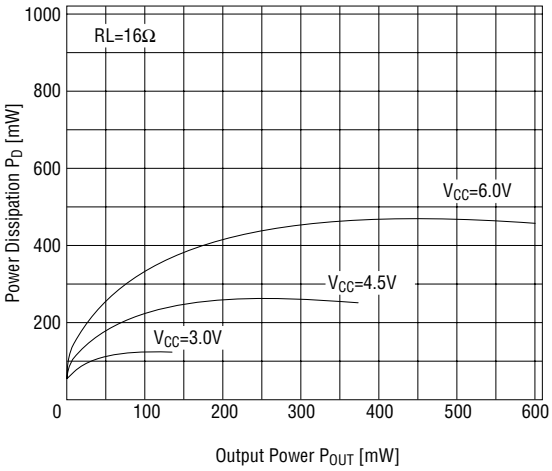
Maxiumum Output Amplitude vs. Voltage Supply



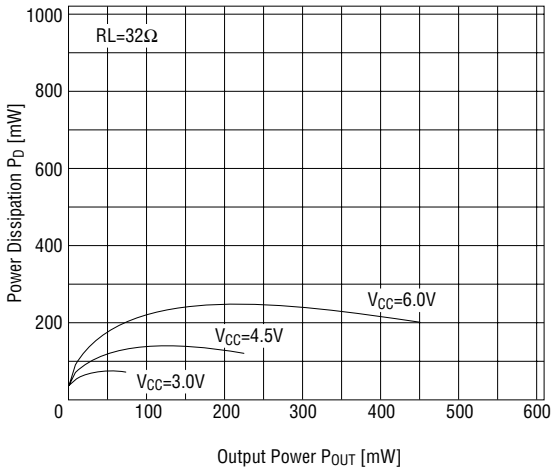
Power Dissipation vs. Output Power



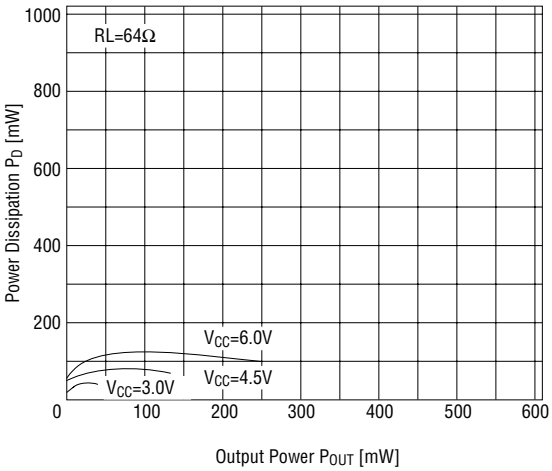
Power Dissipation vs. Output Power



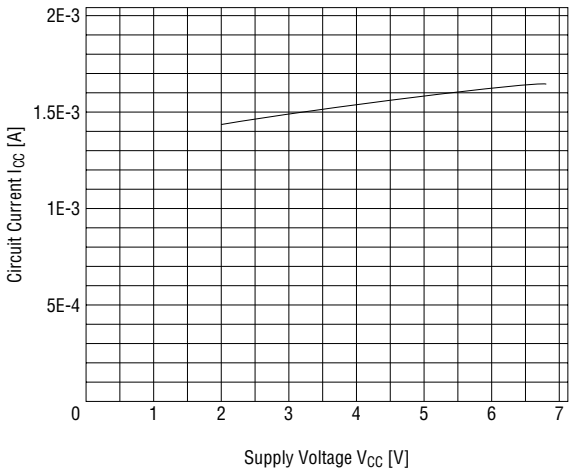
Power Dissipation vs. Output Power



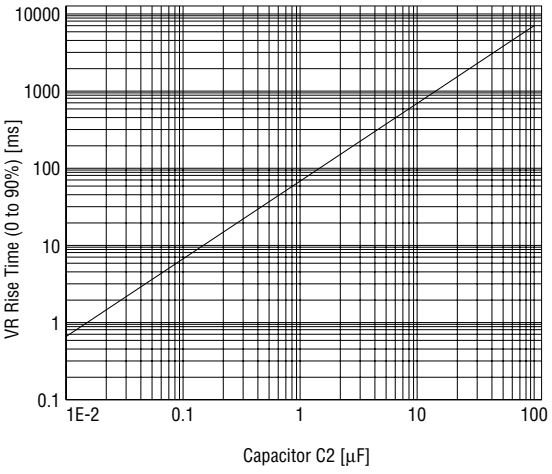
Power Dissipation vs. Output Power



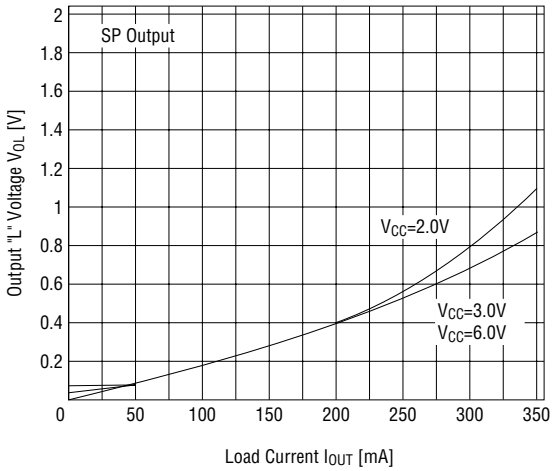
Circuit Current vs. Voltage Supply



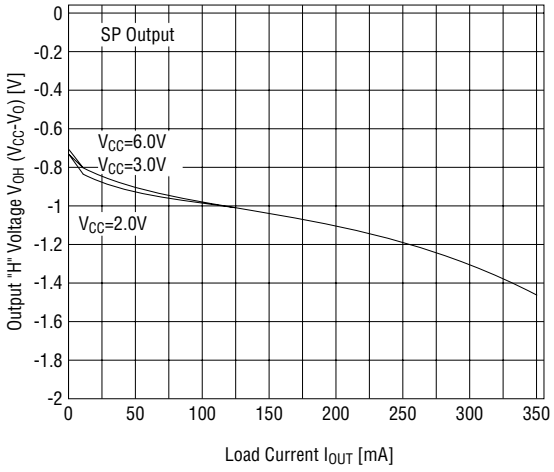
VR Rise Time vs. Capacitor Value (C2)



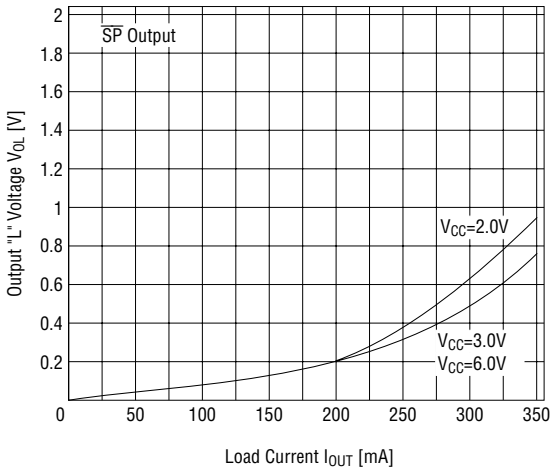
Output Voltage vs. Load Current



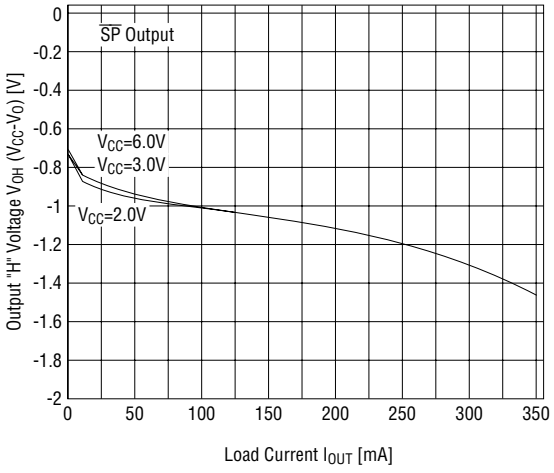
Output Voltage vs. Load Current



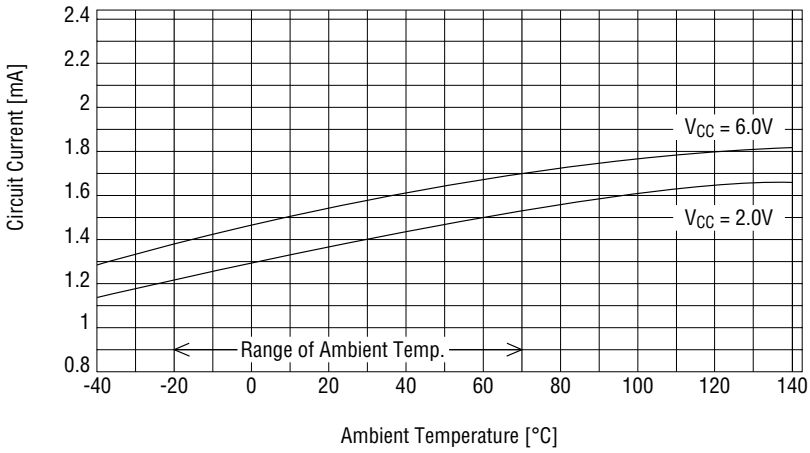
Output Voltage vs. Load Current



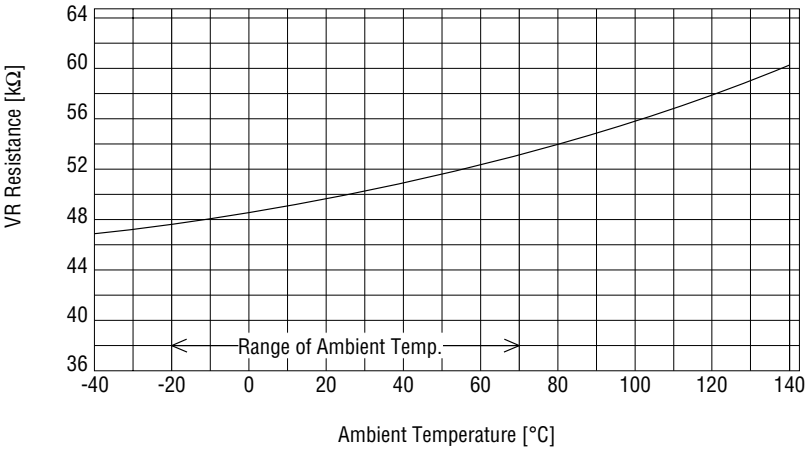
Output Voltage vs. Load Current



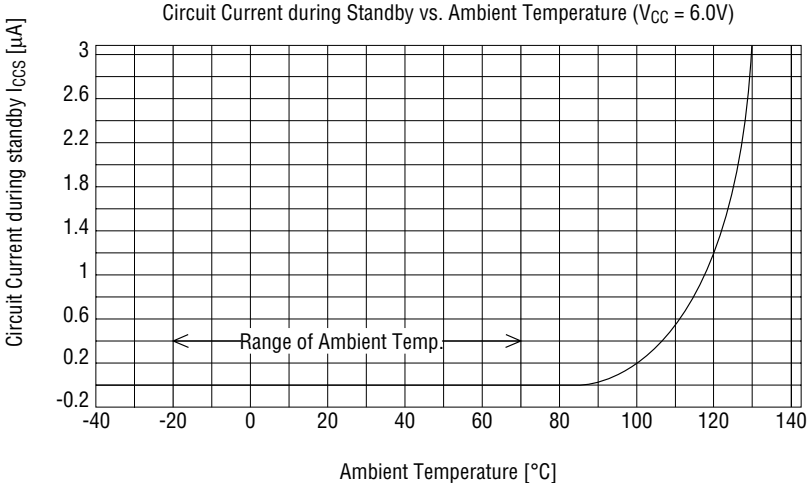
Circuit Curent vs. Ambient Temperature

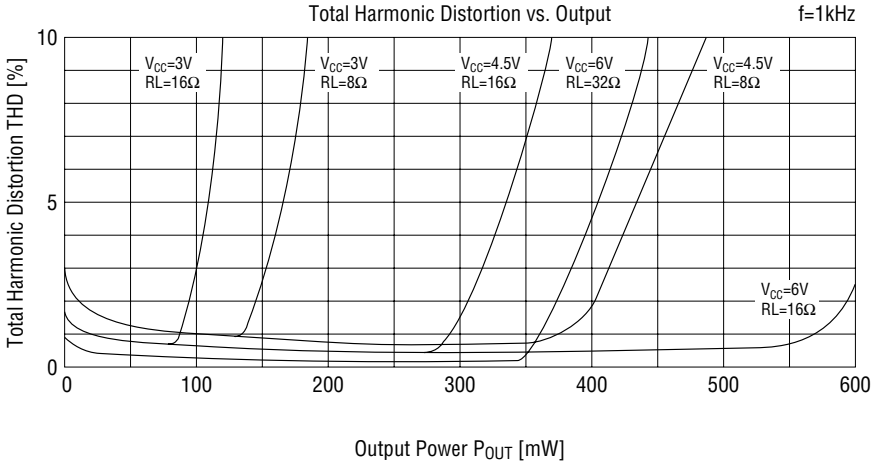


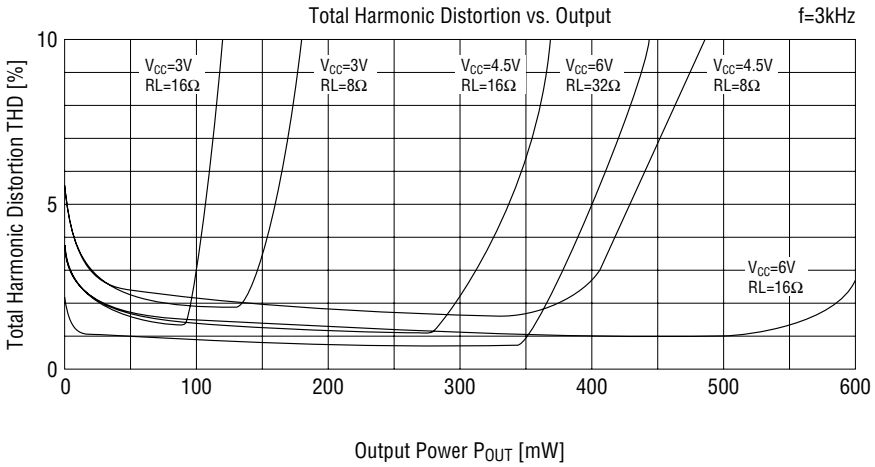
VR Resistance vs. Ambient Temperature

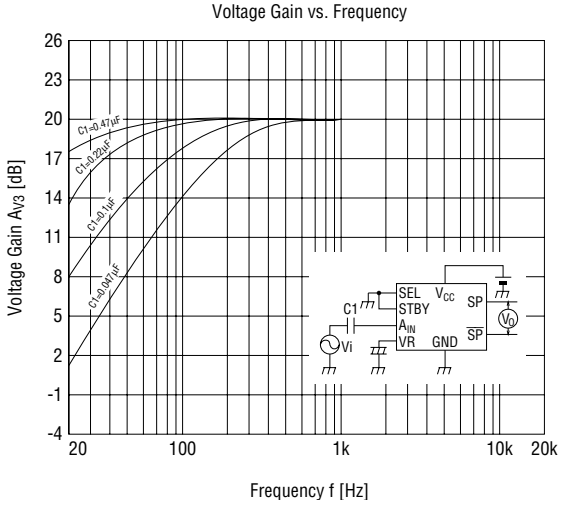


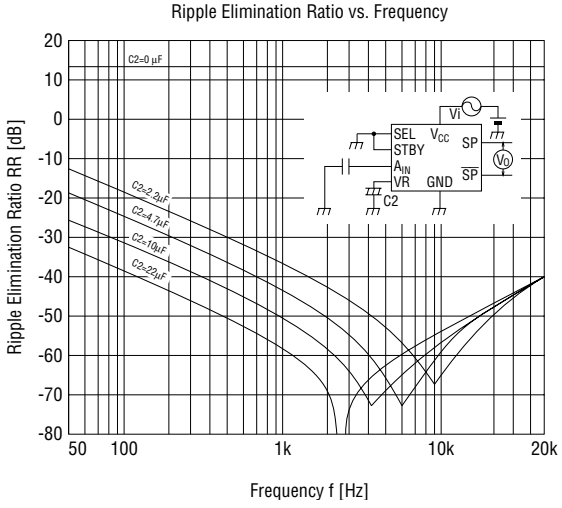
Circuit Current during Standby vs. Ambient Temperature (V_{CC} = 6.0V)







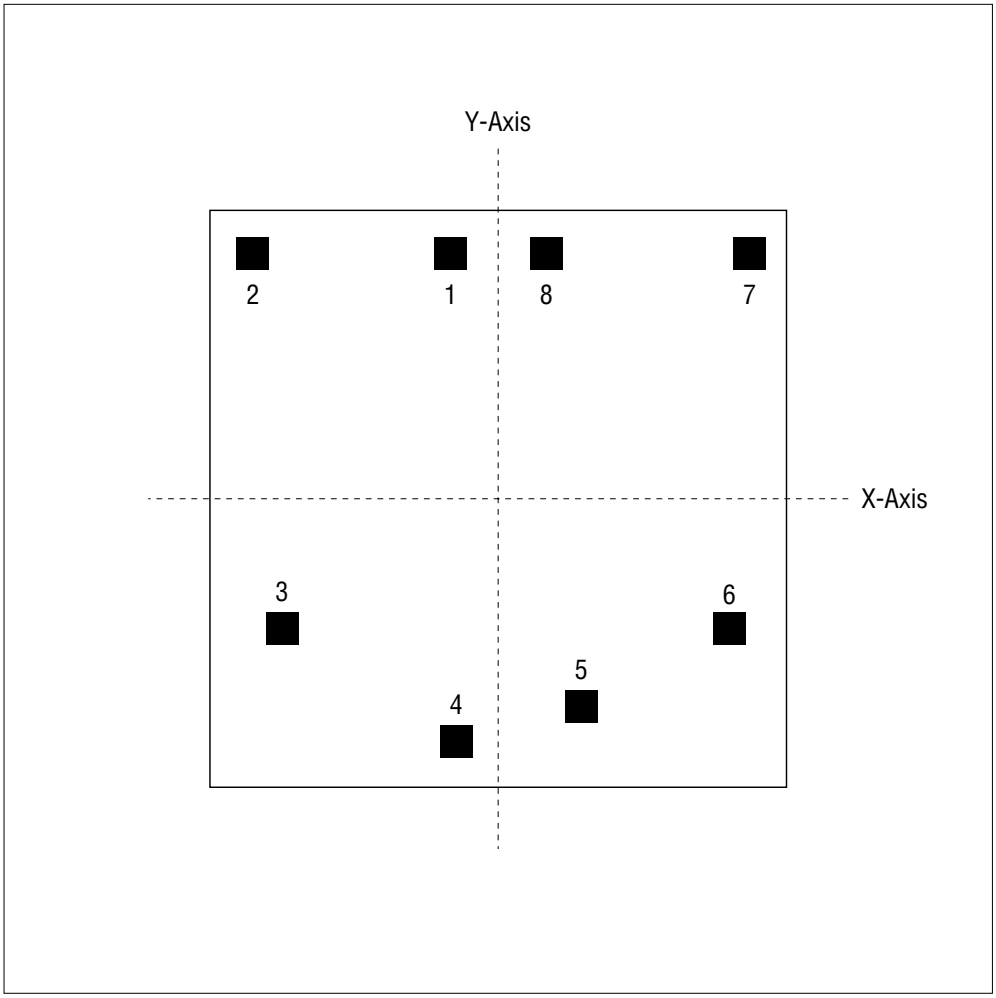




PAD CONFIGURATION

Pad Layout

Chip size : X=2.3mm, Y=2.4mm
Chip thickness : 350±30µm
Pad size (PV aperture) : 110×110µm
Substrate potential : GND
Pad location diagram



Pad Coordinates

(Chip center is located at X=0 and Y=0.)

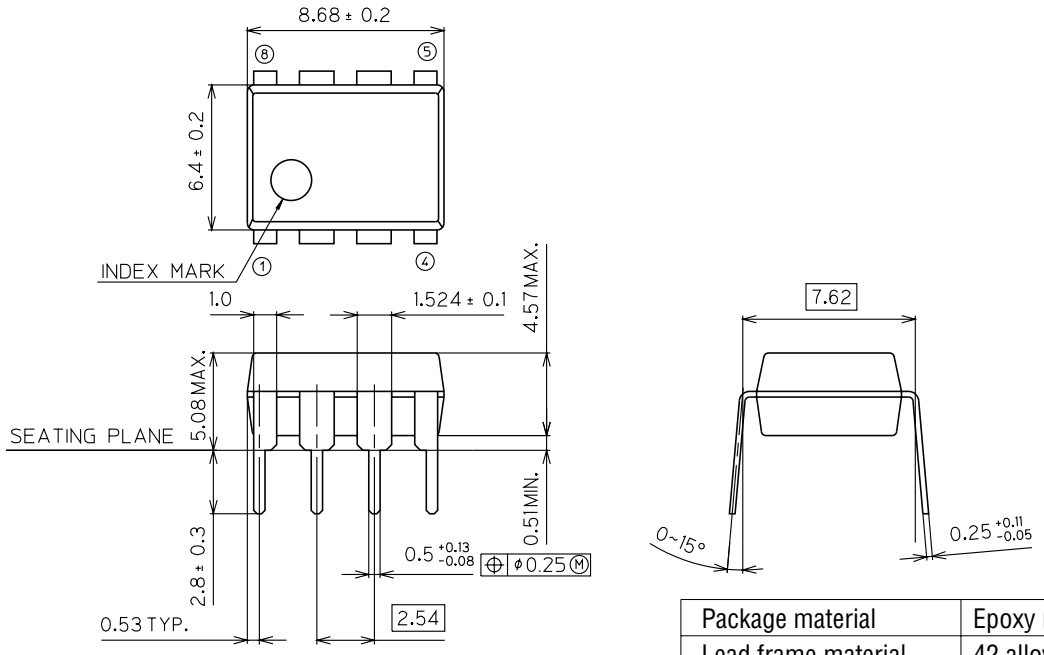
(Unit: µm)

Pad No.	Pad Name	X-AXIS	Y-AXIS
1	VR	–133	1035
2	A_{IN}	–985	1035
3	$\overline{SP}$	–950	–263
4	GND	–180	–1027
5	V_{CC}	240	–914
6	SP	950	–263
7	STBY	985	1035
8	SEL	159	1035

PACKAGE DIMENSIONS

(Unit : mm)

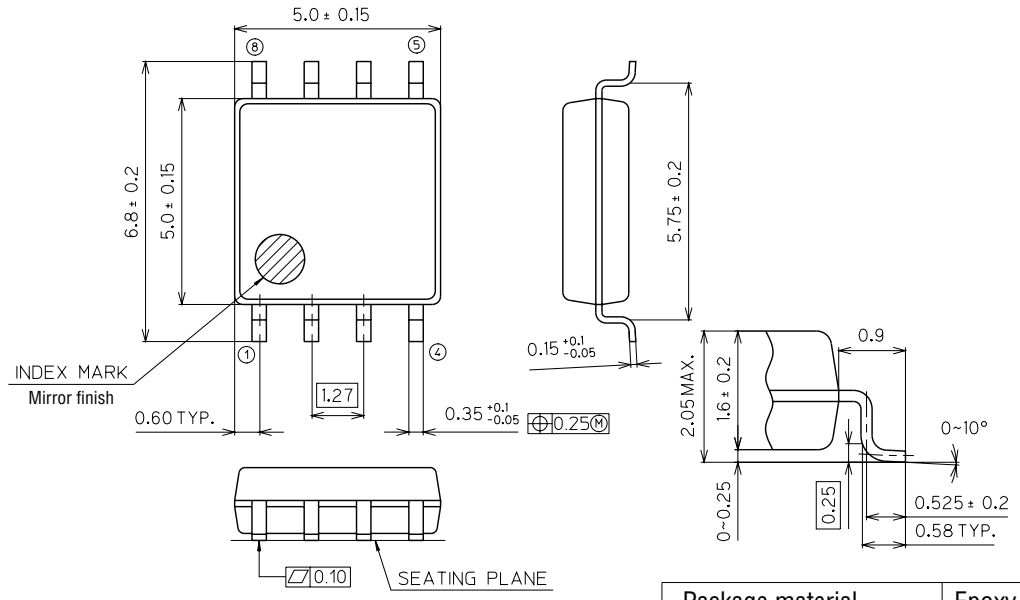
DIP8-P-300-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.46 TYP.

(Unit : mm)

SOP8-P-250-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.10 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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