

## MSM6722

### Pitch Control IC for The Speech Signal

#### GENERAL DESCRIPTION

The MSM6722 converts in real-time the pitch of the speech signal in a range of one octave upward or downward.

Two pitch control methods can be selected. One is to change the pitch in 17 steps by two switch inputs, and the other is to select one of 16 steps by four binary input lines.

Since a microphone preamplifier and a low-pass filter are built in, the pitch conversion set can easily be configured by connecting a microphone, amplifier, and speaker in the peripheral circuit. The MSM6722 is functionally compared to the MSM6322, as described below.

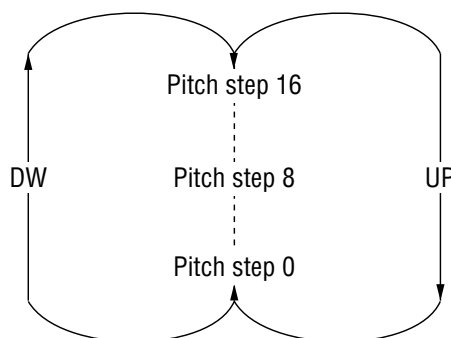
#### 1. Speech pitch step reset (UP/DW mode)

MSM6322 ..... PRST pin only

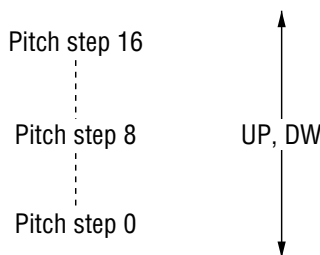
MSM6722 ..... PRST pin and UP•C (DW•C) pin available.

#### 2. Change in pitch

MSM6322 ..... Speech pitch is changeable in 17 steps.



MSM6722 ..... The pitch step does not change if a signal is input to the UP•C (DW•C) pin when the pitch step is 16 or 0.



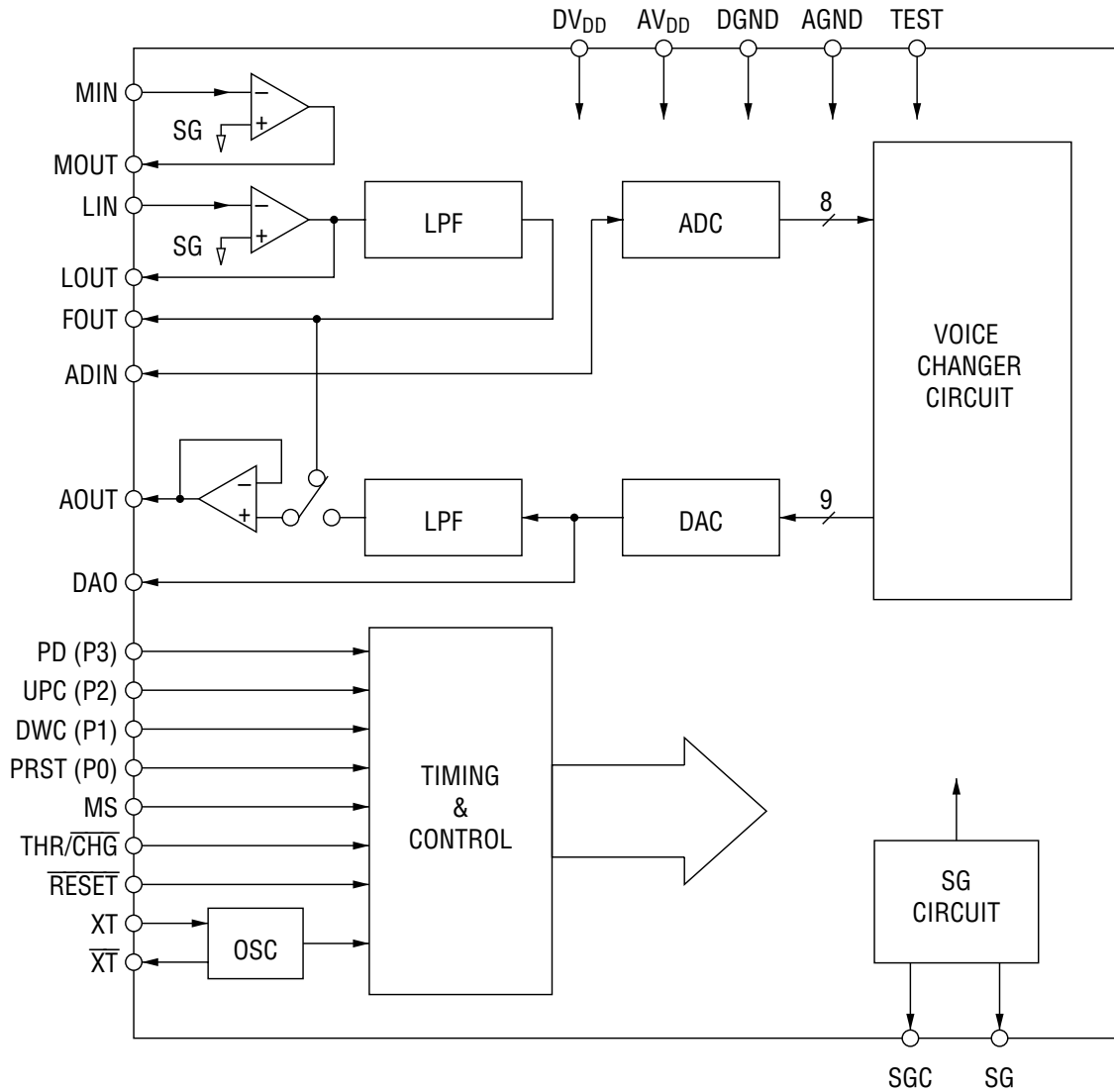
#### 3. Additional THR/ $\overline{\text{CHA}}$ pin

This pin outputs a voice signal without passing the pitch conversion circuit including ADC•DAC.

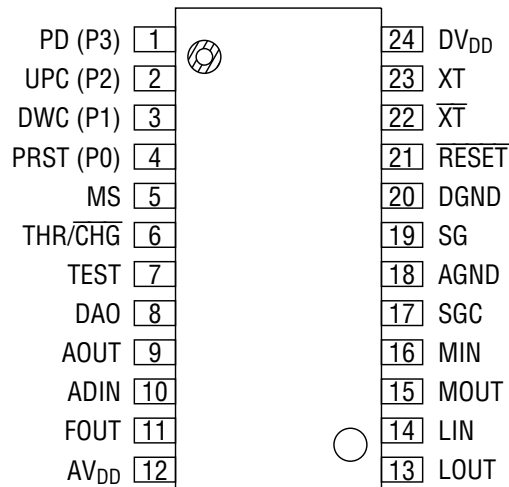
## FEATURES

- Built-in microphone preamplifier
- Built-in low-pass filters
- Built-in 8-bit AD converter
- Built-in 9-bit DA converter
- Speech pitch alterable in 17 steps (including the no pitch change step)
- Master clock frequency at 4 MHz
- 5 V single power supply
- Package : 24-pin plastic SOP (SOP24-P-430-1.27-K) (Product name : MSM6722GS-K)  
Chip

**BLOCK DIAGRAM**



**PIN CONFIGURATION (TOP VIEW)**



**24-Pin Plastic SOP**

## PIN DESCRIPTIONS

## Common to UP/DOWN Mode and BINARY Mode

Pin	Symbol	Type	Description
24	DV <sub>DD</sub>	—	Digital power supply pin. Insert a bypass capacitor of 0.1 μF or more between this pin and DGND.
20	DGND	—	Digital ground pin.
12	AV <sub>DD</sub>	—	Analog power supply pin. Insert a bypass capacitor of 0.1μF or more between this pin and AGND.
18	AGND	—	Analog ground pin.
16	MIN	I	Inverting input pins for the built-in OP amplifier. The non-inverting input pin is connected internally to SG.
14	LIN		
15	MOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN respectively.
13	LOUT		
10	ADIN	I	Input pin for the built-in 8-bit AD converter.
11	FOUT	O	Output pin from the built-in LPF. Connect to ADIN Pin.
9	AOUT	O	Output pin from built-in LPF. This pin is used to output speech signals and to connect the amplifier for driving speaker.
8	DAO	O	Output pin from built-in 9-bit DA converter.
21	$\overline{\text{RESET}}$	I	The IC enters the initial state when this pin is at the "L" level. At this time, the oscillation stops and the DA converter output (DAO) and audio output (AOUT) fall to the GND level. Then the IC returns to the initial state. The IC has a built-in power-on-reset circuit. For normal power-on reset operation, supply the power within 1 msec. If power cannot be supplied within 1 msec, apply a $\overline{\text{RESET}}$ pulse after the power is switched on.
6	THR/ $\overline{\text{CHG}}$	I	Select pin for the pitch control or non-pitch control. With a "H" level input, the IC outputs a normal speech signal from the AOUT pin through the built-in OP amplifier. With a "L" level input, the IC outputs a pitch controlled speech signal from the AOUT pin.
7	TEST	I	Test pin to be fixed to "L" level.
23	XT	I	Crystal oscillator connecting pin. When using the external clock, use this pin as the input.
22	$\overline{\text{XT}}$	O	Crystal oscillator connecting pin. When using the external clock, this pin must be left OPEN.
19	SG	O	These pins output the reference voltage (signal ground (SG)) of the analog circuit. The output is approximately 1/2 the AV <sub>DD</sub> level.
17	SGC		

**UP/DOWN Mode Only**

Pin	Symbol	Type	Description
5	MS	I	Mode select pin. This pin must always be tied low.
2	UPC	I	Pins for raising or lowering the pitch by one step at a time. The pitch changes by one step upward (or downward) each time a "H" level pulse is input to the UPC (or DWC) pin. The circuit enters the "no pitch change" state when an "H" level pulse is input to these pins simultaneously.
3	DWC		
1	PD	I	Power-down pin. All clocks, including the internal oscillator circuit, are stopped when the PD pin is set to the "H" level.
4	PRST	I	Pitch reset pin. The circuit enters the "no pitch change" state when this pin is set to the "H" level.

**Binary Mode Only**

Pin	Symbol	Type	Description
5	MS	I	Mode select pin. This pin must always be tied high.
1	P3	I	The pitch step is directly set by 4 pins (bits) of P3 (MSB) to P0 (LSB). One of the 16 steps from step 0 (P3=P2=P1=P0="L") to step 15 (P3=P2=P1=P0="H") can be set.
2	P2		
3	P1		
4	P0		

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Power-supply voltage	$V_{DD}$	$T_a = 25^\circ\text{C}$	-0.3 to +7.0	V
Input voltage	$V_{IN}$	$T_a = 25^\circ\text{C}$	-0.3 to $V_{DD} + 0.3$	V
Storage temperature	$T_{STG}$	—	-55 to +150	$^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Range	Unit
Power-supply voltage	$V_{DD}$	DGND = AGND = 0 V	4.5 to 5.5	V
Operating temperature	$T_{op}$	—	-10 to +70	$^\circ\text{C}$
Master clock frequency	$f_{OSC}$	—	4 to 4.5	MHz

**ELECTRICAL CHARACTERISTICS****DC Characteristics**(Ta = -10 to +70°C, DV<sub>DD</sub> = AV<sub>DD</sub> = 4.5 V to 5.5 V, DGND = AGND = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
"H" input voltage	$V_{IH}$	—	$0.8 \times V_{DD}$	—	—	V
"L" input voltage	$V_{IL}$	—	—	—	$0.2 \times V_{DD}$	V
"H" input current *1	$I_{IH1}$	$V_{IH} = V_{DD}$	—	—	10	$\mu\text{A}$
"H" input current *2	$I_{IH2}$	$V_{IH} = V_{DD}$	—	—	20	$\mu\text{A}$
"H" input current *4	$I_{IH3}$	$V_{IH} = V_{DD}$	20	—	650	$\mu\text{A}$
"L" input current *3	$I_{IL1}$	$V_{IL} = \text{GND}$	-10	—	—	$\mu\text{A}$
"L" input current *2	$I_{IL2}$	$V_{IL} = \text{GND}$	-20	—	—	$\mu\text{A}$
Operating current consumption (1)	$I_{DD}$	$f_{OSC} = 4 \text{ MHz}$ , no load	—	6	12	mA
Operating current consumption (2)	$I_{PD}$	At power down, no load $T_a = -40 \text{ to } +70^\circ\text{C}$	—	—	10	$\mu\text{A}$
		At power down, no load $T_a = -40 \text{ to } +85^\circ\text{C}$	—	—	50	$\mu\text{A}$

\*1 Applies to all input pins excluding the XT pin.

\*2 Applies to the XT pin.

\*3 Applies to all the input pins without pull-down resistors, excluding the XT pin (i.e., pins 1, 5-7, 10, 14, 16, 21; however pin 1 is applied only during UP/DOWN mode).

\*4 Applies to the input pins with pull-down resistors, excluding the XT pin (i.e., pins 1, 2, 3, 4; however, pin 1 is applied only during BINARY mode).

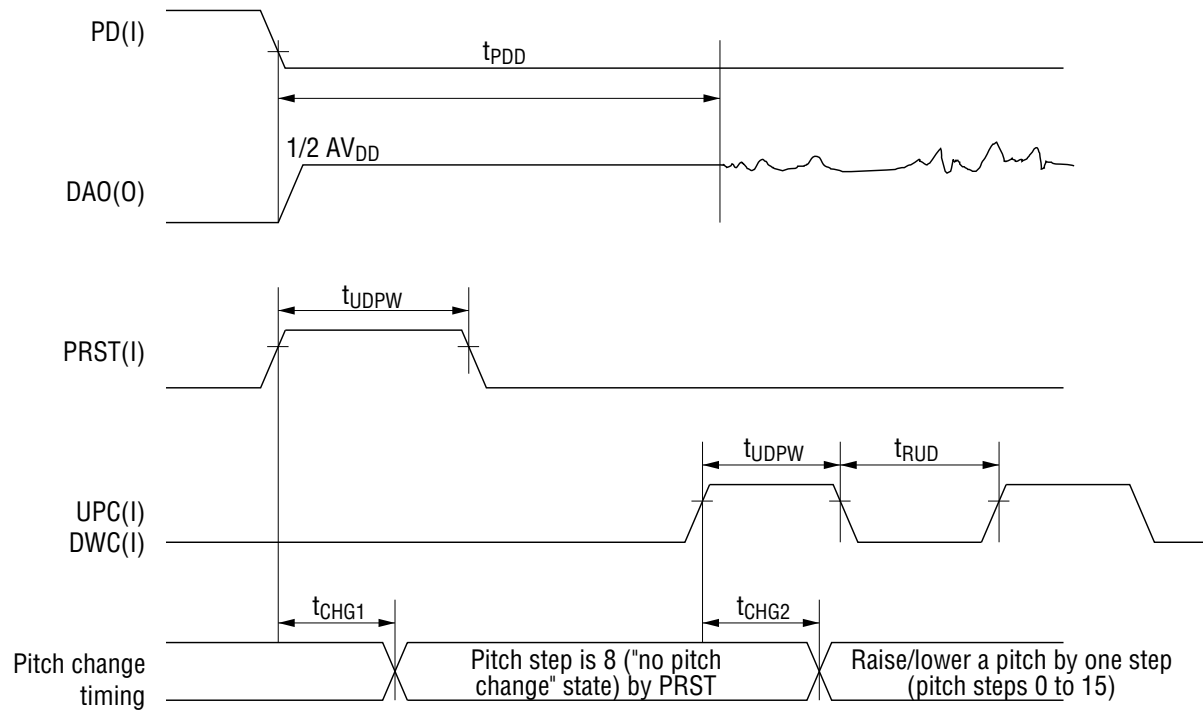
**Analog Characteristics**(Ta = -10 to +70°C, DV<sub>DD</sub> = AV<sub>DD</sub> = 4.5 V to 5.5 V, DGND = AGND = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DA output relative error	V <sub>DAE</sub>	No load	—	—	40	mV
AD output relative error	V <sub>ADE</sub>	No load	—	—	40	mV
SCF allowable input voltage range	V <sub>FIN</sub>	—	1	—	V <sub>DD</sub> -1	V
SCF input impedance	R <sub>FIN</sub>	—	1	—	—	MΩ
OP amplifier open loop gain	G <sub>OP</sub>	f <sub>IN</sub> = 0 to 4 kHz	40	—	—	dB
OP amplifier input impedance	R <sub>INA</sub>	—	1	—	—	MΩ
OP amplifier load resistance	R <sub>OUTA</sub>	—	200	—	—	kΩ
AOUT load resistance	R <sub>AOUT</sub>	—	50	—	—	kΩ

**AC Characteristics**(Ta = -10 to +70°C, f<sub>OSC</sub> = 4 MHz, DV<sub>DD</sub> = AV<sub>DD</sub> = 4.5 V to 5.5 V, DGND = AGND = 0 V)

Parameter	Symbol	Condition	Min	Max	Unit
DAO output delay from falling edge of PD	t <sub>PDD</sub>	f <sub>OSC</sub> = 4 MHz	—	16	ms
Pulse width of PRST, UPC, and DWC pulses	t <sub>UDPW</sub>	f <sub>OSC</sub> = 4 MHz	62	—	ms
Time between UPC and DWC pulses	t <sub>RUUD</sub>	f <sub>OSC</sub> = 4 MHz	31	—	ms
Pitch change delay from rising edge of PRST	t <sub>CHG1</sub>	f <sub>OSC</sub> = 4 MHz	62	—	ms
Pitch change delay from rising edge of UPC and DWC	t <sub>CHG2</sub>	f <sub>OSC</sub> = 4 MHz	31	—	ms

TIMING DIAGRAM



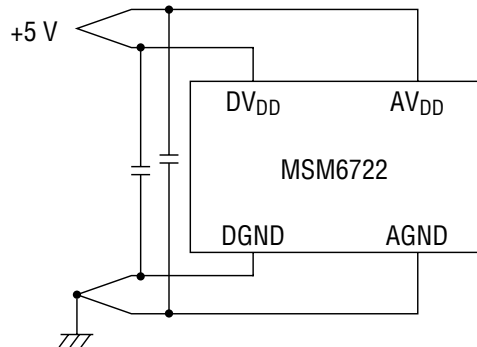


## FUNCTIONAL DESCRIPTION

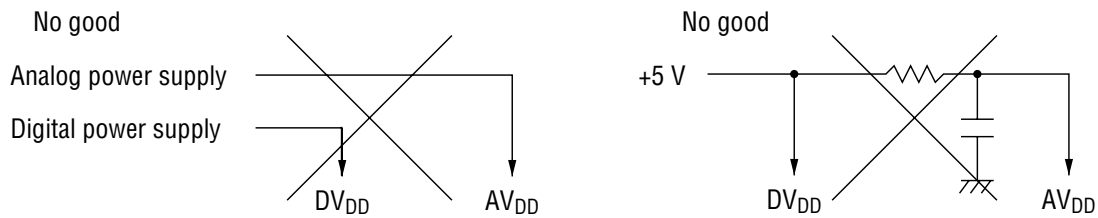
### Power Supply Wiring

As shown in the diagram below, supply the power to this IC from the same power source, but separate the wiring for the analog and the logic sections.

To improve the electrical characteristics, insert a bypass capacitor of 0.1  $\mu\text{F}$  or more between  $\text{DV}_{\text{DD}}$  and  $\text{DGND}$  and between  $\text{AV}_{\text{DD}}$  and  $\text{AGND}$ .



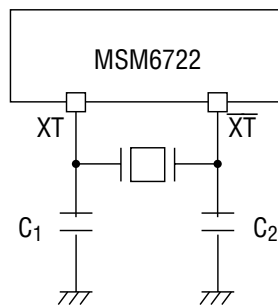
Do not supply the power to the analog section and the logic section from separate power sources; otherwise latch-up may occur.



### Connecting an Oscillator

Connect ceramic or crystal oscillators to the XT and  $\overline{\text{XT}}$  pins as shown below.

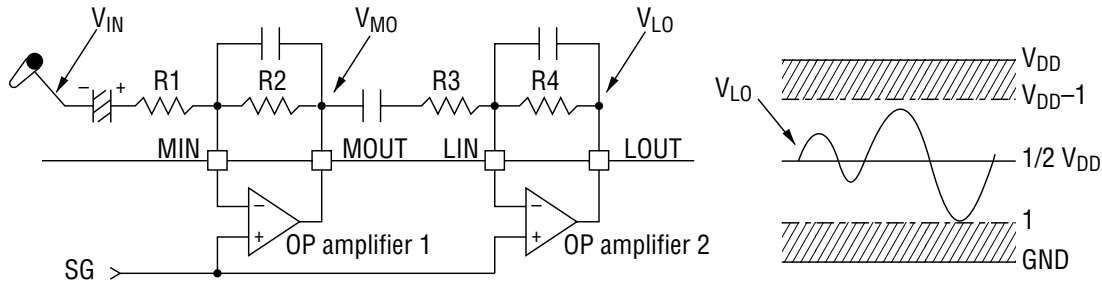
The optimal load capacitance values when connecting ceramic oscillators of MURATA MFG. and KYOCERA CORPORATION are shown below for reference.



Ceramic oscillator		Optimal load capacitance		
	Model name	Frequency (MHz)	C <sub>1</sub> (pF)	C <sub>2</sub> (pF)
MURATA MFG.	CSA4.00MG	4.0	30	30
	CST4.00MGW (with capacitor)			
KYOCERA CORPORATION	KBR-4.0MSA	4.0	33	33
	KBR-4.0MKS			
	PBRC4.00B			

### Analog Input Amplifier Circuit

The MSM6722 has two built-in operational amplifiers for amplifying the microphone output. Each output amplifier is provided with an inverting input pin and output pin. The analog circuit reference voltage SG (signal ground) is connected internally to the non-inverting input of each output amplifier. For amplification, form an inverting amplifier circuit and adjust the amplification ratio by using external resistors, as shown below.



$$V_{LO} = \frac{R_4}{R_3} V_{M0} = \frac{R_2 \cdot R_4}{R_1 \cdot R_3} V_{IN} (V)$$

The output  $V_{LO}$  of output amplifier 2 is connected to the input  $F_{IN}$  of the built-in LPF. The  $F_{IN}$  allowable input voltage ( $V_{FIN}$ ) ranges from 1 V to  $(V_{DD}-1)$  V. Therefore, the amplification ratio must be adjusted so that the  $V_{LO}$  amplitude can be within the  $F_{IN}$  allowable input voltage range. For example, if  $V_{DD} = 5$  V,  $V_{LO}$  becomes  $3 V_{p-p}$  max. If  $V_{LO}$  exceeds the  $F_{IN}$  allowable input voltage range, the output of the LPF will be a clipped waveform. The load resistance  $R_{OUTA}$  of the OP amplifier is 200 k $\Omega$  or more. Therefore, the feedback resistors R2 and R4 of the inverting amplifier circuit must be 200 k $\Omega$  or more.

## Analog Input Amplifier Circuit

The output  $V_{LO}$  of OP amplifier 2 is connected to the input FIN of the built-in LPF.

The allowable FIN input voltage  $V_{FIN}$  ranges from 1 V to  $(V_{DD} - 1)$  V.

Therefore, the amplification factor must be adjusted so that the  $V_{FIN}$  amplitude can be within the allowable FIN input voltage range. For example, if  $V_{DD} = 5$  V,  $V_{LO}$  becomes 3 V<sub>P-P</sub> max.

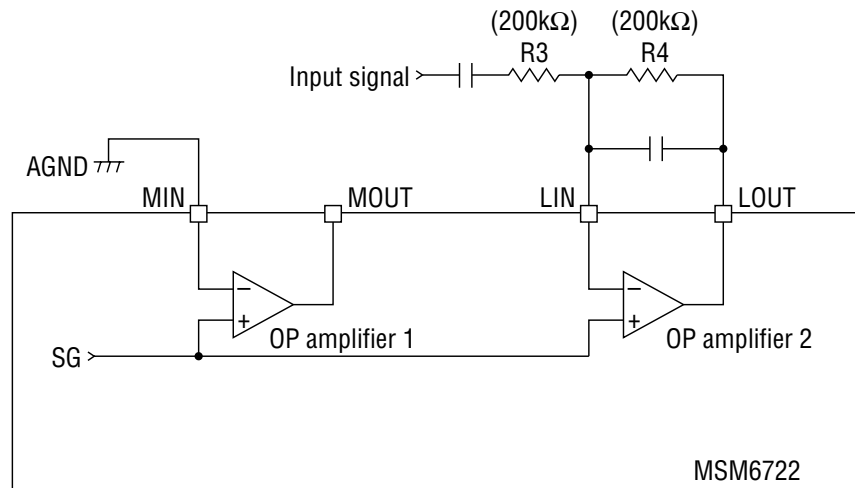
If  $V_{LO}$  exceeds the allowable FIN input voltage range, the output of the LPF will be a clipped waveform. The load resistance  $R_{OUTA}$  of the OP amplifier is 200 k $\Omega$  or more.

Therefore, the feedback resistors R2 and R4 must be 200 k $\Omega$  or more.

When OP amplifier 1 is not used and OP amplifier 2 is used, the MIN pin must be connected to AGND or AVDD, and the MOUT pin must be open.

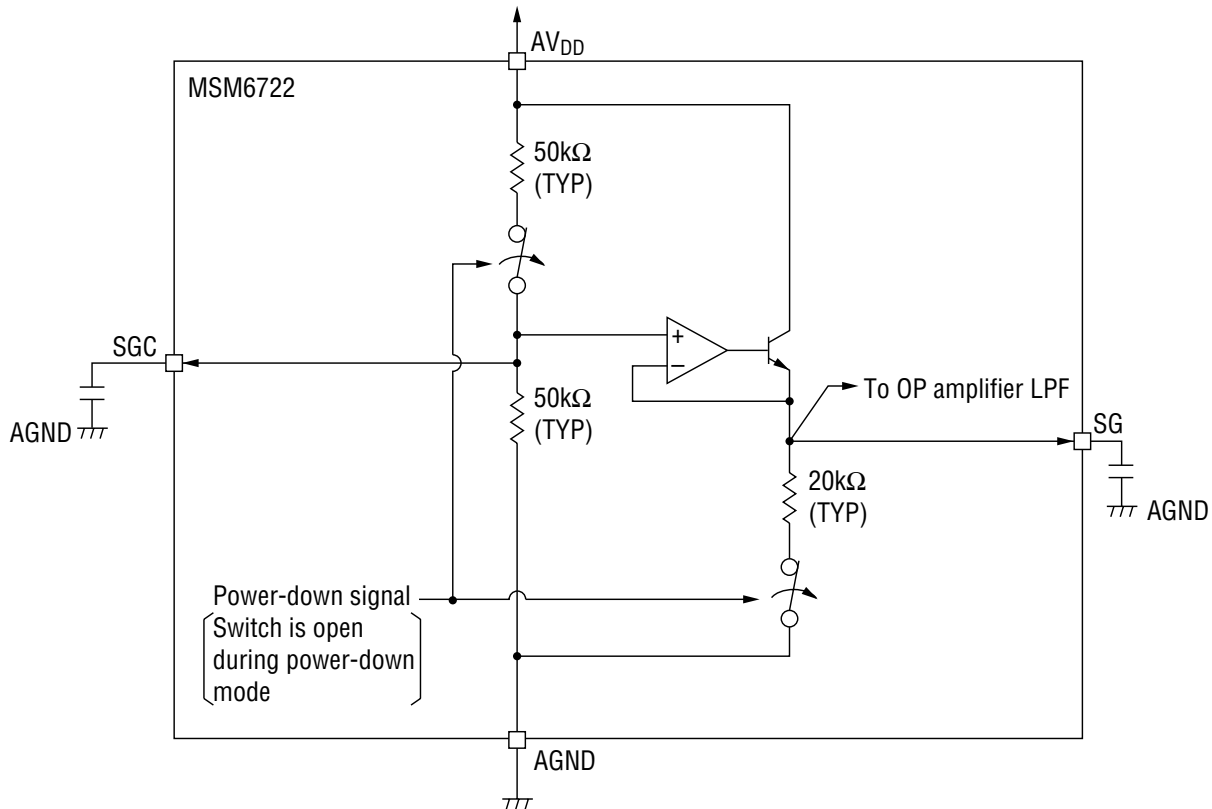
Even if amplification is unnecessary, OP amplifier 2 must be always used.

Below is an example of an analog input amplifier circuit when the amplification factor is 1.



## Configuring SGC and SG pins

The internal equivalent circuit around the SGC and SG pins is shown below.



The SG signal is reference voltage (signal ground) for internal OP amplifiers and LPF. Install a capacitor between the SGC pin and AGND and between the SG pin and AGND respectively in order to make the SG signal noiseless. It is recommended to install an approx. 1μ capacitor, which should be determined after evaluating the tone quality.

It takes several ten msec until the DC levels such as the SG level of the analog circuit is stabilized after the power-down mode is cancelled. The larger capacitance of a capacitor connected to SGC or SG requires the longer time for stabilizing.

After the power-down mode is cancelled, enter voices after the DC levels for the analog circuit has been stabilized.

When the device is in power-down mode, the output voltage of the SG pin becomes unstable. Therefore, SG must not be supplied to external circuits.

Otherwise, power supply current may be leaked via the internal SG circuit.

Same is true for the SGC pin.

**Pitch-Control Circuit**

[BINARY mode] (P3, P2, P1, P0)

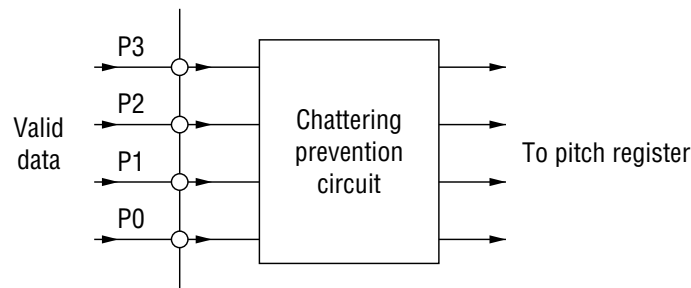
As shown in the diagram below, this IC has an internal prevention circuit for approximately 62 ms of chattering . Therefore, hold these pins at "H" level for 62 ms or more. P3, P2, P1, and P0 pins are used to directly set the pitch steps.

Sixteen pitch steps are provided, but step 16 cannot be set.

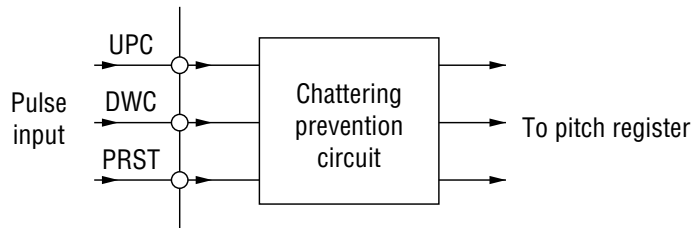
[UP/DOWN mode] (UPC, DWC, PRST)

As shown in the diagram below, this IC has an internal prevention circuit for approximately 62 ms of chattering . Therefore, hold these pins at "H" level for 62 ms or more.

[BINARY mode]



[UP/DOWN mode]

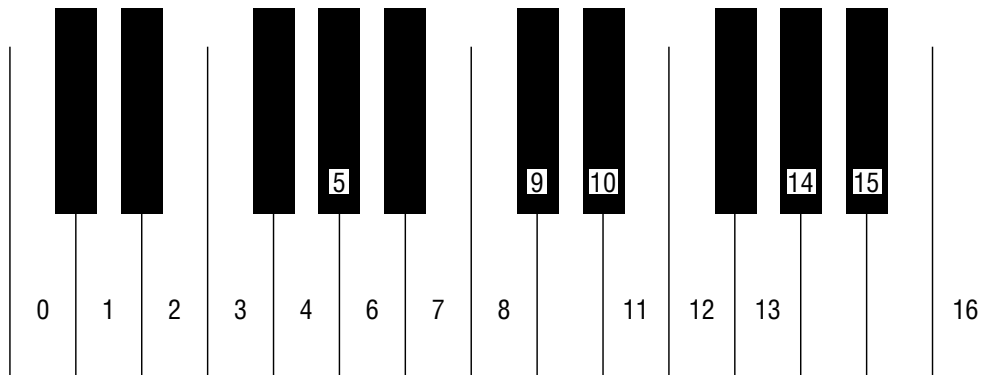


**Pitch-Control Circuit**

Inputting a "H" level pulse to the UPC pin raises the pitch by one step, and inputting a "H" level pulse to the DWC pin lowers the pitch by one step. Inputting a "H" level pulse to the PRST pin or to the UPC and DWC pins at the same time sets the no-pitch change state (pitch step 8).

A pitch shifts in a range of one octave upward or downward, centered at pitch step 8. The pitch shift is illustrated in the following keyboard diagram and the following table via corresponding frequencies.

**Pitch Conversion Diagram**

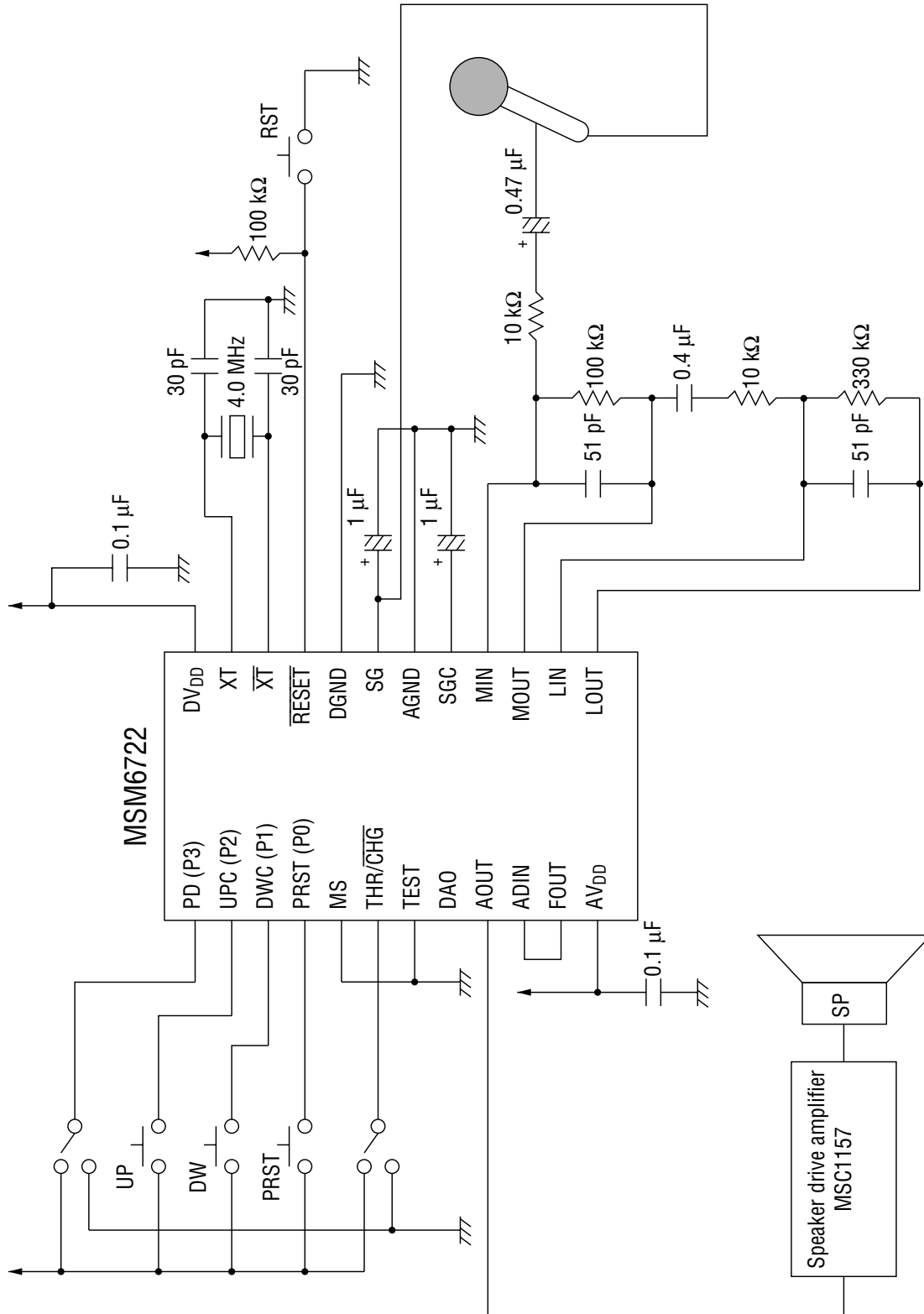


**Pitch Conversion Table**

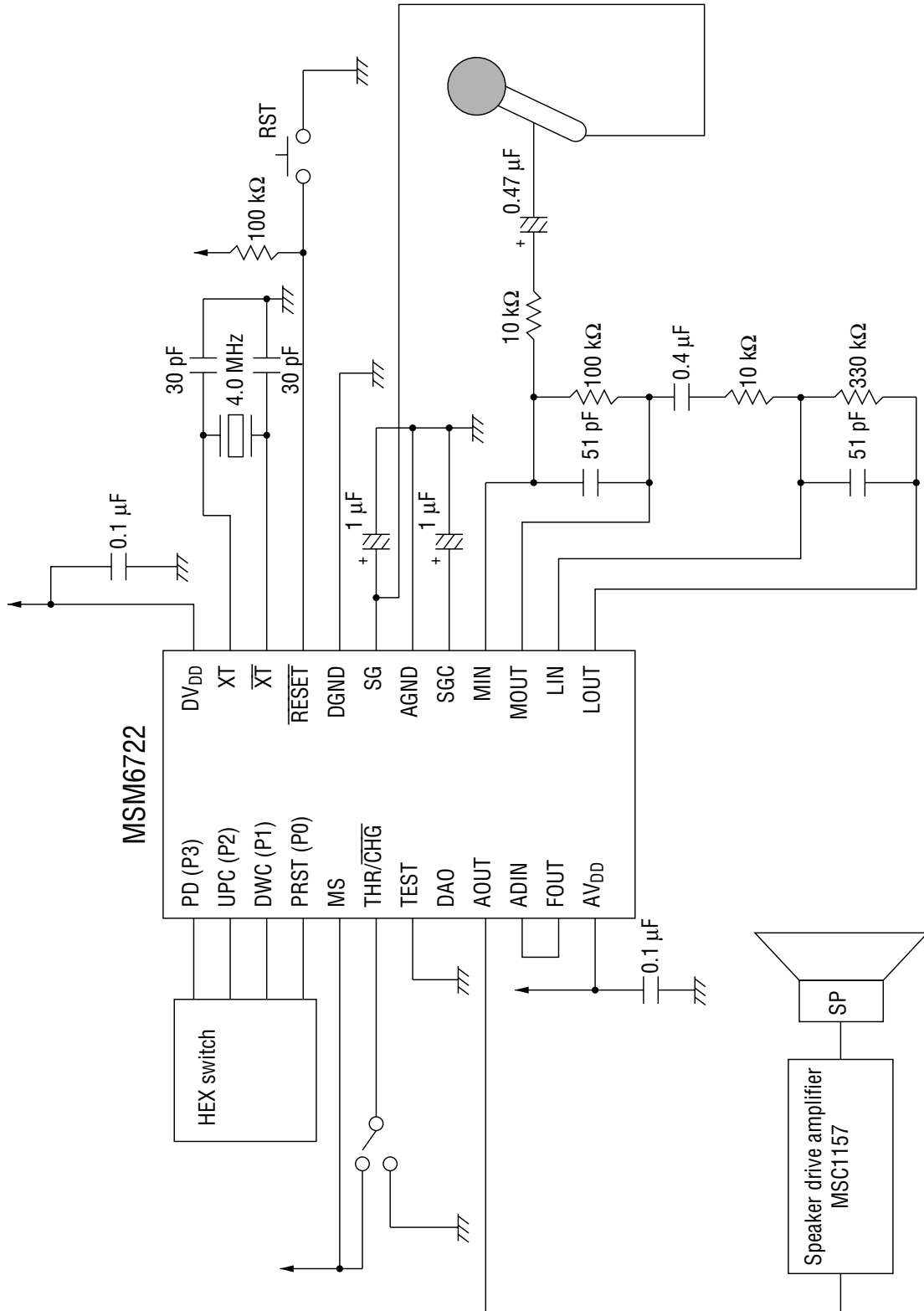
Pitch step	DA sampling cycle (μs)/ frequency (kHz)
16	60/16.6
15	71/14.0
14	76/13.1
13	80/12.5
12	90/11.1
11	90/10.5
10	101/9.90
9	113/8.84
8	120/8.33
7	127/7.87
6	143/6.99
5	151/6.62
4	160/6.25
3	180/5.55
2	190/5.26
1	202/4.95
0	227/4.40

APPLICATION CIRCUITS

UP/DOWN Mode



BINARY Mode

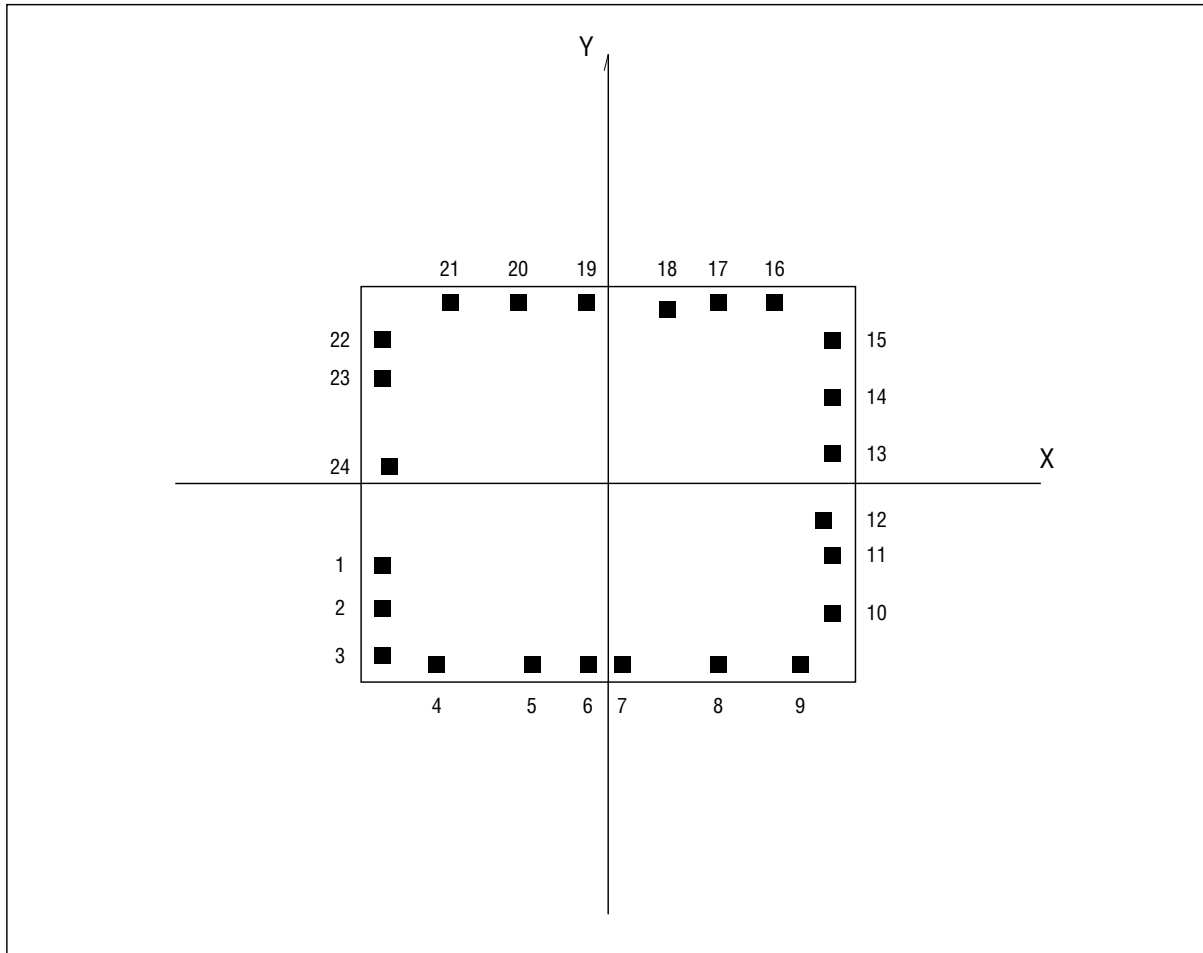




### PAD CONFIGURATION

#### Pad Layout

Chip Size : 3.99 × 3.08 (mm)



#### Pad Coordinates

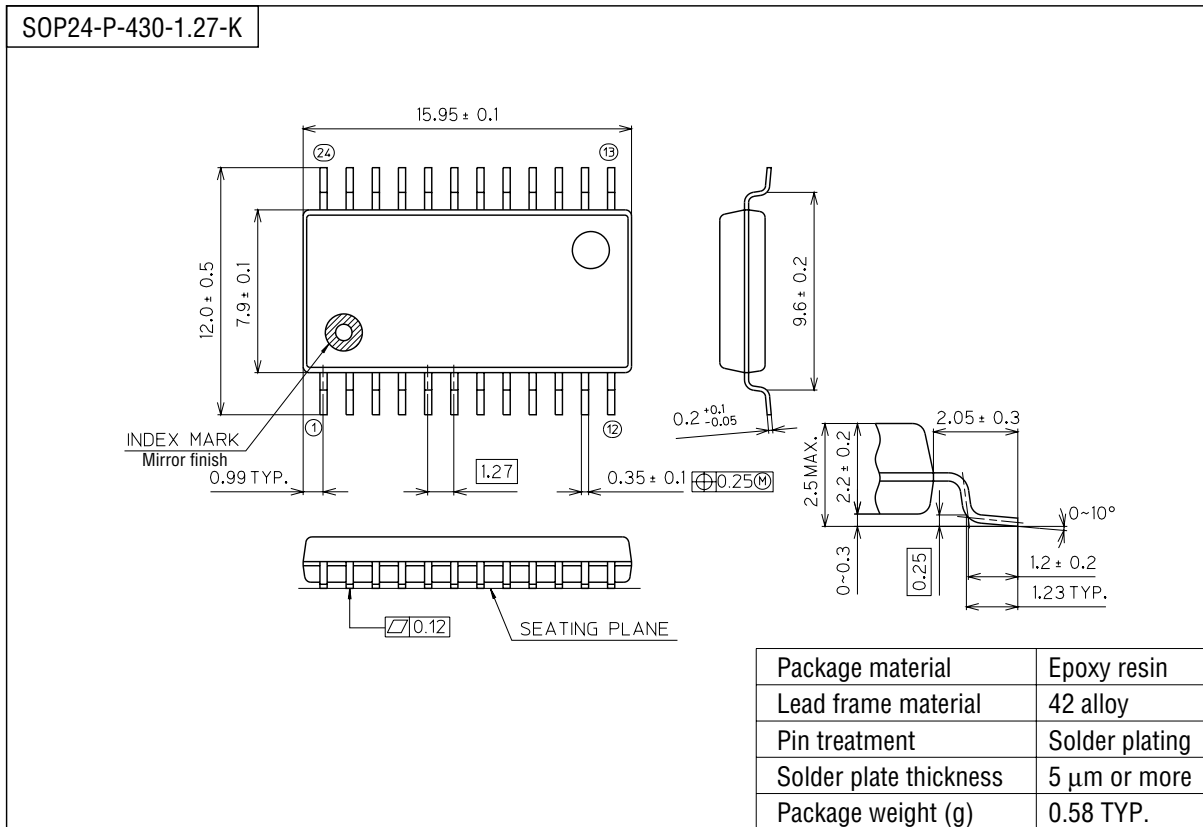
(Chip center is located at X=0 and Y=0.)

Pad No	PAD name	X (um)	Y (um)
1	PD	-1784	-602
2	UPC	-1784	-955
3	DWC	-1784	-1310
4	PRST	-1314	-1391
5	MS	-736	-1397
6	THR/CHG	-275	-1397
7	TEST	53	-1397
8	DAO	912	-1396
9	AOUT	1447	-1396
10	ADIN	1783	-974
11	FOUT	1783	-561
12	AV <sub>DD</sub>	1733	-238

Pad No	PAD Name	X (um)	Y (um)
13	LOUT	1782	356
14	LIN	1782	780
15	MOUT	1782	1193
16	MIN	1351	1359
17	SGC	938	1359
18	AGND	598	1295
19	SG	-127	1359
20	DGND	-650	1359
21	RESET	-1198	1359
22	XT	-1787	1053
23	XT	-1786	703
24	DV <sub>DD</sub>	-1736	84

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

## NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.
4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.
5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.
6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans. Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.
7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.
8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.
9. MS-DOS is a registered trademark of Microsoft Corporation.

Copyright 1999 Oki Electric Industry Co., Ltd.