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Oki, Network Solutions for a Global Society

QSY-43404

ML9362DVx

Specification

(258-Channel Organic EL Anode Driver)

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OKI Semiconductor

ML9362

258 (86 × RGB) Channel Organic EL Anode Driver

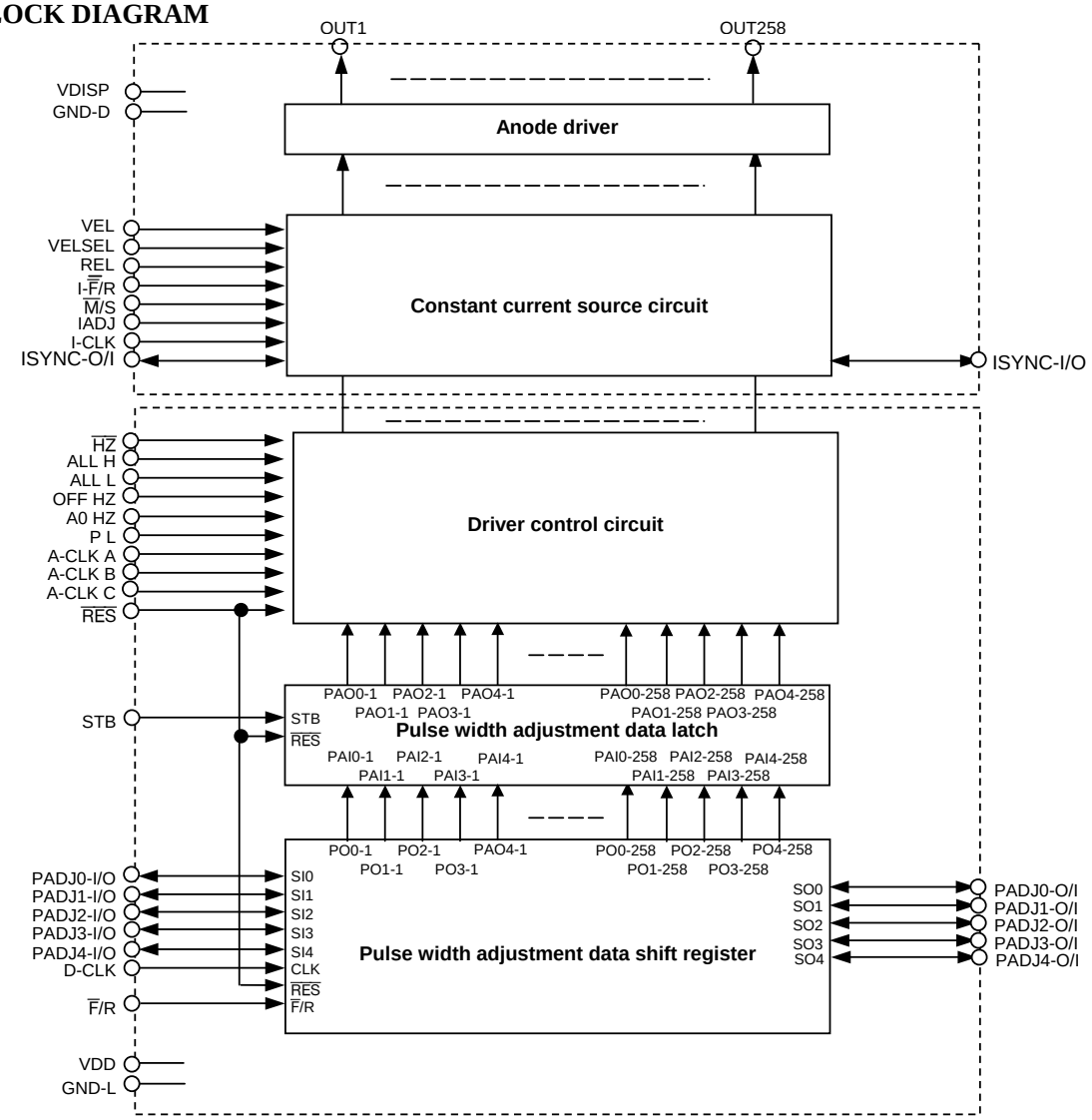
GENERAL DESCRIPTION

The ML9362 is an organic EL anode driver LSI with 258 (86 × RGB) driver outputs. The anode driver is constant current output type and allows adjustment of pulse width for each output. Since this LSI has the output condition setting function, which allows setting of all outputs High, all outputs Low, and all outputs High Impedance, the user can set driving methods suited to the characteristics of individual organic EL panel. When combined with the organic EL cathode driver series (ML937x), the ML9362 can drive a full-dot panel.

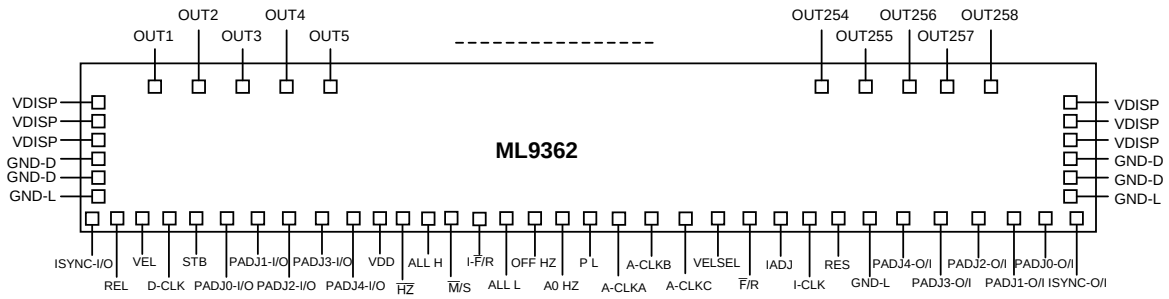
FEATURES

- Logic power supply voltage : 2.7 to 5.5 V
- EL drive voltage : 8.0 to 20 V
- Anode outputs : 258 outputs (86 × RGB)
- Anode high output current : –400 μA (constant current output)
- Anode low output current : 35 mA (max.)
- Output pulse width adjustment : Adjustable in 32 different degrees (adjusted by external clock input for each RGB)
- Output current adjustment range : 20 to 337.5% (1 step = 2.5 %, 128 steps, all outputs)
- All outputs High, all outputs Low, and all outputs High Impedance can be set as output conditions
- Package : Gold bump chip (ML9362DVWA)
  TCP (ML9362DVVxZ0yy (Vx denotes TCP version; yy is determined by the chip orientation in relation to the reel).)

BLOCK DIAGRAM



PIN CONFIGURATION (TRACE SIDE VIEW)



PIN DESCRIPTION

Symbol	I/O	Connected to	Description
V_{DISP} V_{DD} GND-D GND-L	—	Power supply	V_{DISP} is a power supply pin of anode driver circuit and constant current source circuit. V_{DD} is a power supply pin of logic circuit. GND-D is the ground pin of anode driver circuit and constant current source circuit. GND-L is the ground pin of logic circuit. GND-D and GND-L should be connected outside the LSI.
V_{EL}	I	Power supply	Input pin of OUT1 to OUT258 output current setting voltage. Input voltage to this pin is enabled when V_{EL}SEL is high, and disabled when it is low. Input a voltage within the guaranteed operating range.
V_{EL}SEL	I	Microcontroller	Pin (pull-down input) for selecting the output current adjusting voltage of anode driver circuit. • When this pin is low, LSI's internal voltage (5 V) is selected. • When this pin is high, the input voltage at the V_{EL} pin is selected.
REL	—	Resistor	Pin connecting to OUT1 to OUT258 output current setting resistor.
$\overline{F}$/R	I	Microcontroller	Input pin (pull-down input) of data transfer direction select signal for pulse width adjusting data shift register. • When this pin is low, data is transferred starting at POn-1 toward POn-258. • When this pin is high, data is transferred starting at POn-258 toward POn-1. (n = 1 to 5)
IADJ	I	Microcontroller	Input pin of Anode output current adjusting data. Data is read into at the rising edge of I-CLK.
I-CLK	I	Microcontroller	Input pin (Schmitt trigger input) of Anode output current adjusting data transfer clock.
PADJn-I/O (n = 0 to 4)	I/O	Microcontroller, or ML9362 on succeeding stage	Input-output pins of Anode output pulse width adjusting data. When the $\overline{F}$/R pin is low, these pins are input pins and data is read into at the rising edge of D-CLK. When the $\overline{F}$/R pin is high, these pins are output pins and the output status changes at the falling edge of D-CLK.
PADJn-O/I (n = 0 to 4)	O/I		input-output pins of Anode output pulse width adjusting data. When the $\overline{F}$/R pin is high, these pins are input pins and data is read into at the rising edge of D-CLK. When the $\overline{F}$/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK.
D-CLK	I	Microcontroller	Input pin (Schmitt trigger input) of Anode output pulse width adjusting data transfer clock
STB	I	Microcontroller	Input pin (Schmitt trigger input) of Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal
$\overline{RES}$	I	Microcontroller	Input pin (pull-down input) of Initialization signal. When this pin is set low, the LSI enters the following initial setting states: • All anode drive signal outputs: "high impedance"
$\overline{HZ}$	I	Microcontroller	Input pin (pull-up input) of anode drive signal output control signal. When this pin is low, all anode drive signal outputs are high impedance.
ALL H	I	Microcontroller	Input pin (Schmitt trigger and pull-down input) of anode drive signal output control signal. When this pin is high, all anode drive signal outputs are constant current output.
ALL L	I	Microcontroller	Input pin (Schmitt trigger and pull-down input) of anode drive signal output control signal. When this pin is high, anode drive signal outputs are all low.
OFF HZ	I	Microcontroller	Input pin of anode drive signal output control signal. Used to set the anode drive signal output condition at the time that dot is OFF with the combination of A0 HZ and P L.
A0 HZ	I	Microcontroller	Input pin (pull-up input) of anode drive signal output control signal. Used to set the anode drive signal output condition at the time that dot is OFF with the combination of OFF HZ and P L.
P L	I	Microcontroller	Input pin (pull-down input) of anode drive signal output control signal. Used to set the anode drive signal output condition at the time that dot is OFF with the combination of A0 HZ and P L.
A-CLK A A-CLK B A-CLK C	I	Microcontroller	Input pin (Schmitt trigger input) of anode output pulse width adjusting clock. The pulse width adjusting clocks of the anode drive signal outputs of the OUT (3m+1) pin, the OUT (3m+2) pin, and the OUT (3m+3) pin are input to A-CLK A, A-CLOK B, and A-CLOK C, respectively. (m represents 0 to 85).

Symbol	I/O	Connected to	Description
ISYNC-I/O	I/O	Open	Input-output pin for testing anode output reference current. Leave this pin open.
ISYNC-O/I	O/I	Open	Input-output pin for testing anode output reference current. Leave this pin open.
I-$\overline{F}$/R	I	Open	Input pin (pull-down input) for testing anode output reference current. Leave this pin open or connect it to GND-L.
$\overline{M}$/S	I	Open	Input pin (pull-down input) for testing anode output constant current source circuit. Leave this pin open or connect it to GND-L.
OUT 1 to 258	O	Organic EL anode	Output pin of Anode drive signal for organic EL.

FUNCTION TABLE

1. Operation during Transfer of Anode Output Pulse Width Adjusting Data (when $\overline{F}$/R is low)

Input				Shift Register					Latch					Output
$\overline{RES}$	D-CLK	PADJ m-I/O	STB	PO n-1	PO n-2		PO n-257	PO n-258	PAO m-1	PAO m-2		PAO m-257	PAO m-258	PADJ m-O/I
L	X	X	X	L	L		L	L	L	L		L	L	L
H	↑	L	L	L	PO n-1		PO n-256	PO n-257	Invariable					Invariable
		H	L	H	PO n-1		PO n-256	PO n-257	Invariable					Invariable
	↓	L	L	Invariable					Invariable					POn-258
		H	L	Invariable					Invariable					POn-258
	L	X	L	Invariable					Invariable					Invariable
			H	Invariable					PO n-1	PO n-2		PO n-257	PO n-258	Invariable

m = 0 to 4 n = 0 to 4

2. Operation during Transfer of Anode Output Pulse Width Adjusting Data (When $\overline{F}$/R is high)

Input				Shift Register					Latch					Output
$\overline{RES}$	D-CLK	PADJ m-O/I	STB	PO n-258	PO n-257		PO n-2	PO n-1	PAO m-258	PAO m-257		PAO m-2	PAO m-1	PADJ m-I/O
L	X	X	X	L	L		L	L	L	L		L	L	L
H	↑	L	L	L	PO n-258		PO n-3	PO n-2	Invariable					Invariable
		H	L	H	PO n-258		PO n-3	PO n-2	Invariable					Invariable
	↓	L	L	Invariable					Invariable					POn-1
		H	L	Invariable					Invariable					POn-1
	L	X	L	Invariable					Invariable					Invariable
			H	Invariable					PO n-258	PO n-257		PO n-2	PO n-1	Invariable

m = 0 to 4 n = 0 to 4

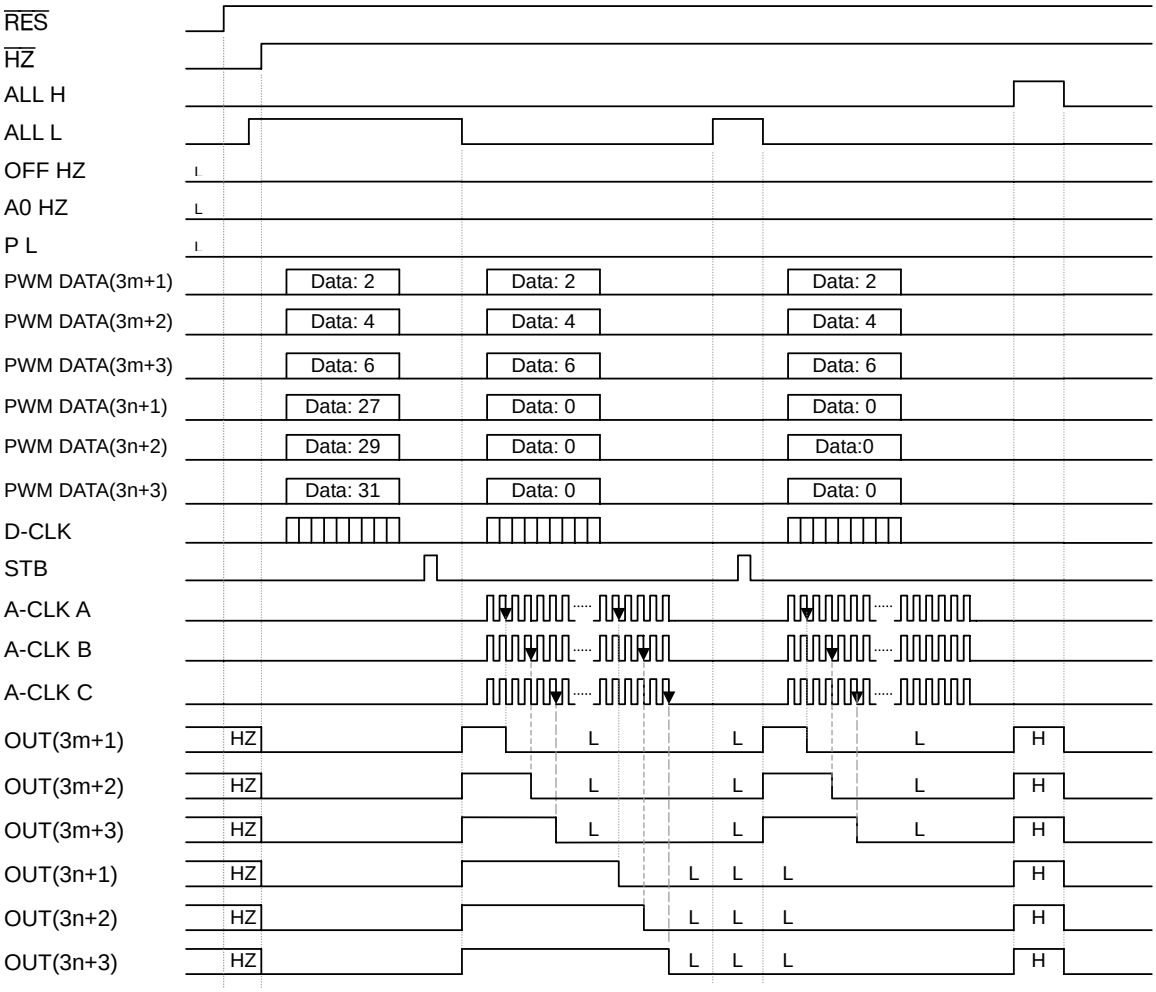
3. Operation of Output Section (When $\overline{RES}$ is high)

$\overline{HZ}$	ALL H	ALL L	OFF HZ	A0 HZ	P L	COMP OUTn	PWM Data n	OUTn
L	X	X	X	X	X	X	X	High impedance
H	H	X	X	X	X	X	X	Constant current output
	L	H	X	X	X	X	X	Low
		L	L	X	L	H	X	Constant current output
						L	X	Low
					H	H	One of PWM data n is "H"	Low
						L	All "L"	High impedance
			H	L	L	H	X	Constant current output
						L	One of PWM data n is "H"	High impedance
							All "L"	Low
					H	H	One of PWM data n is "H"	Low
						L	All "L"	High impedance
				H	L	H	X	Constant current output
						L	One of PWM data n is "H"	High impedance
							All "L"	High impedance
					H	H	One of PWM data n is "H"	Low
						L	All "L"	High impedance

Note: • Set the STB pin to a high level only when both the $\overline{HZ}$ pin and the ALL L pin are high or both are low.
• COMP OUT n remains high until the pulse count of each A-CLK A, A-CLK B, and A-CLK C coincides with the value of PWM data n.

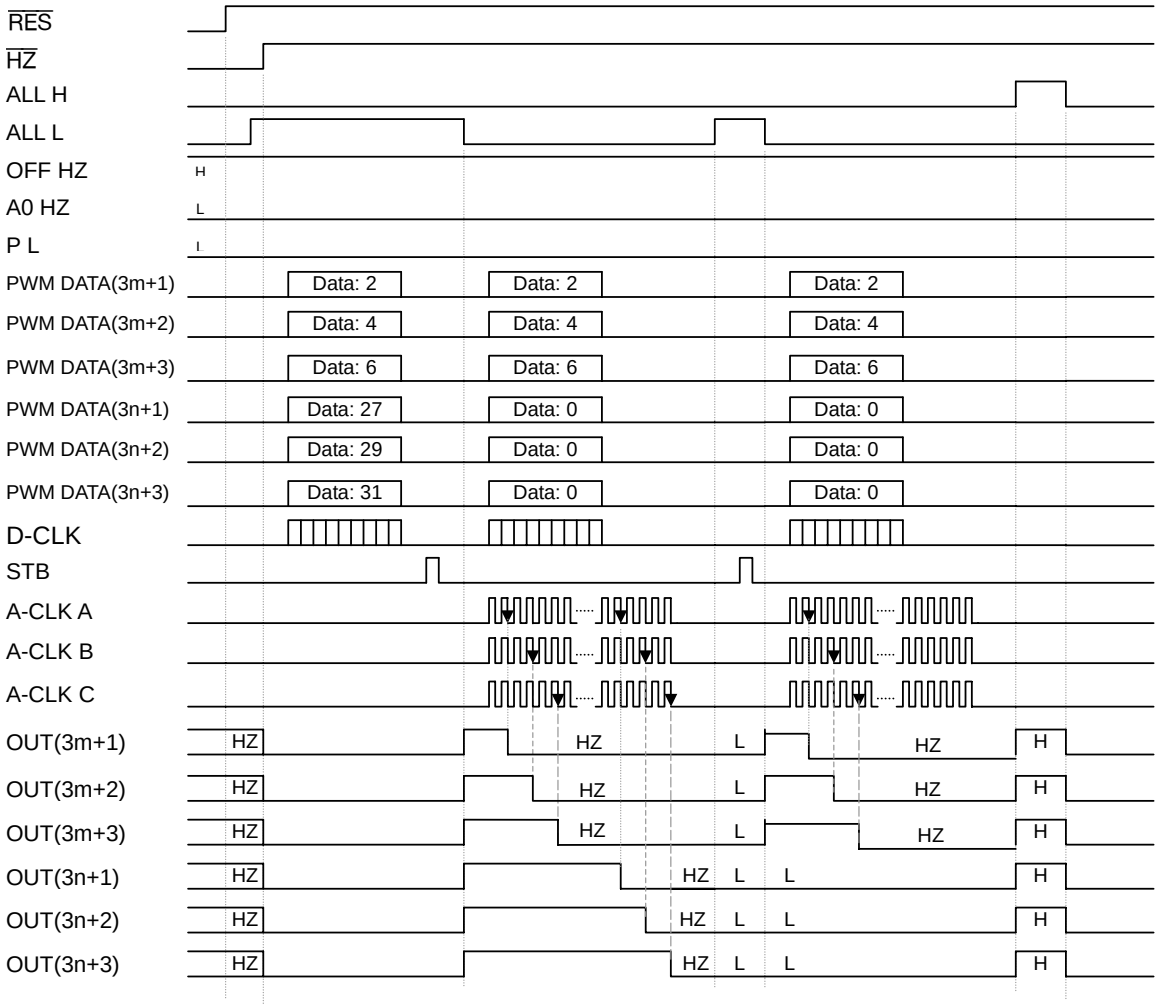
OUTPUT WAVEFORMS

1. When OFF HZ, A0 HZ, and P L are all low



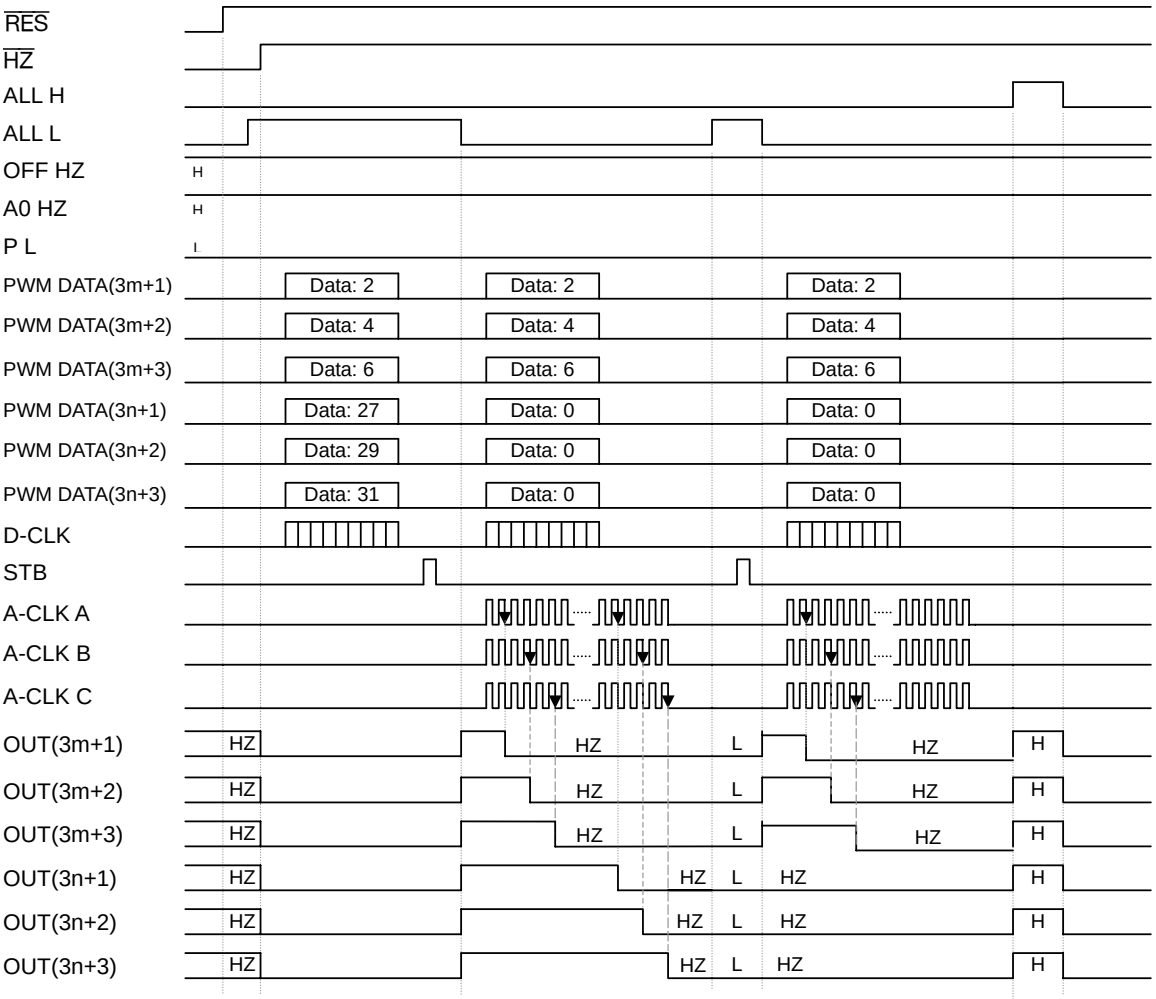
* m, n: 0 to 85

2. When OFF HZ is high and A0 HZ and P L are low



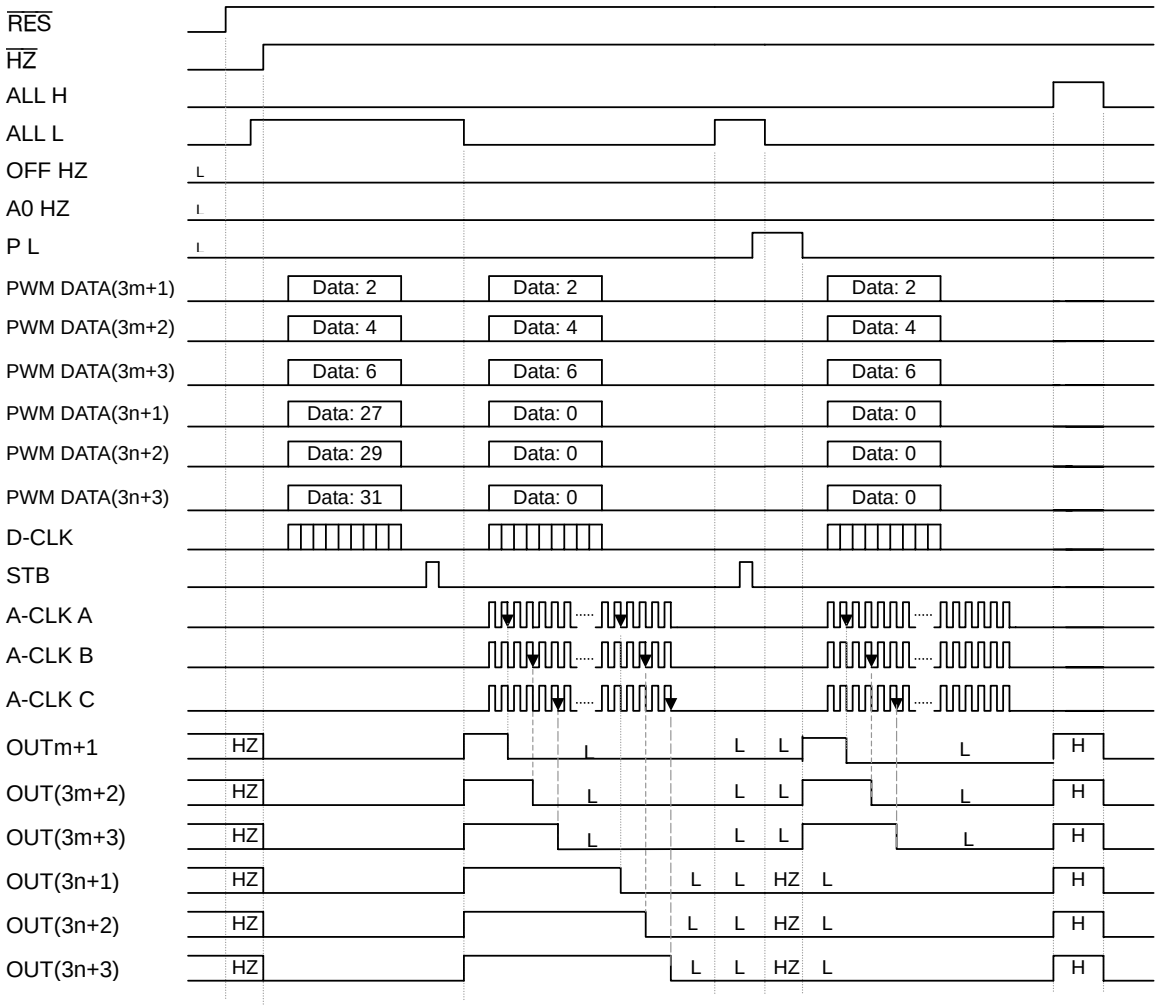
* m, n: 0 to 85

3. When OFF HZ and A0 HZ are high and P L is low



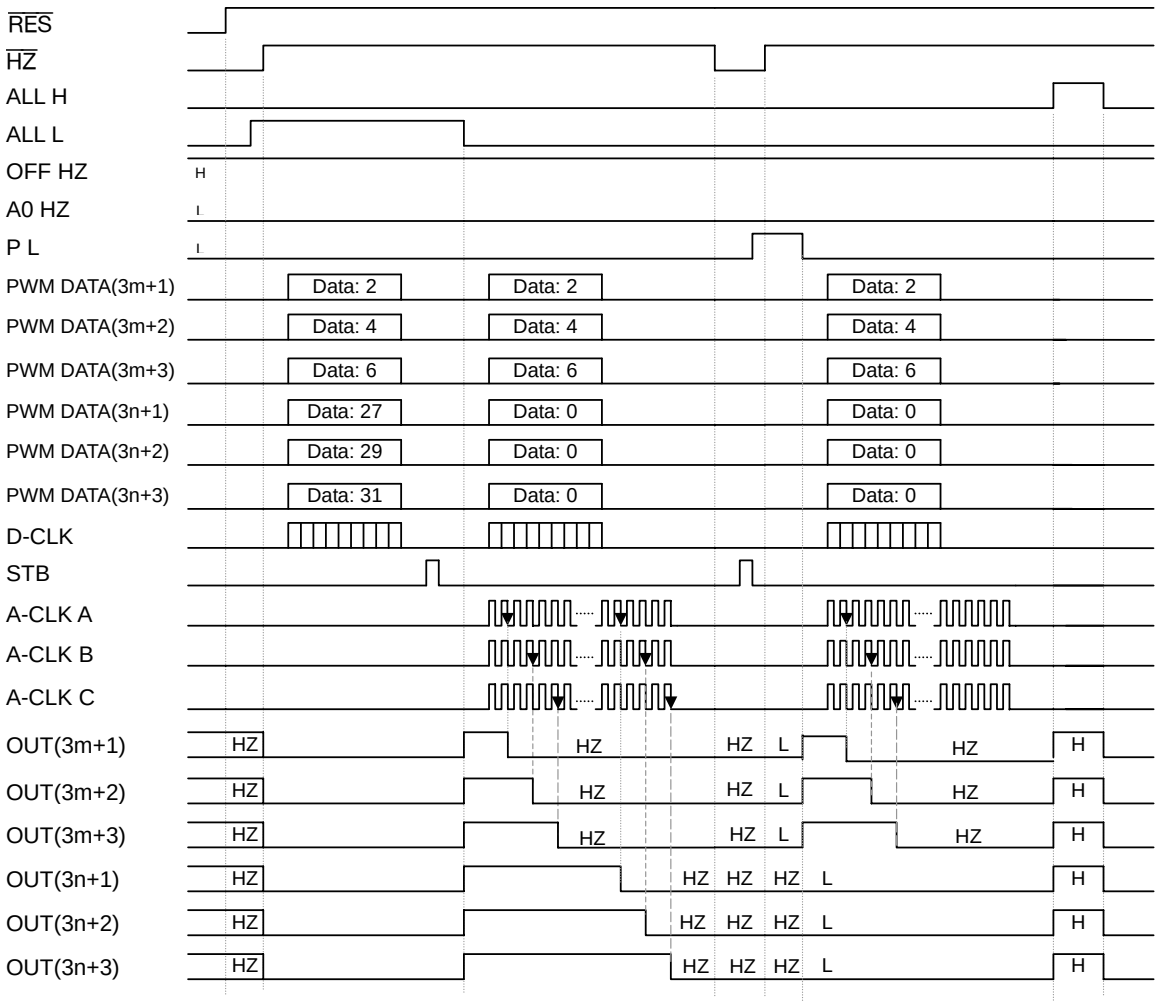
* m, n: 0 to 85

4. When OFF HZ and A0 HZ are low and P L is controlled by pulse



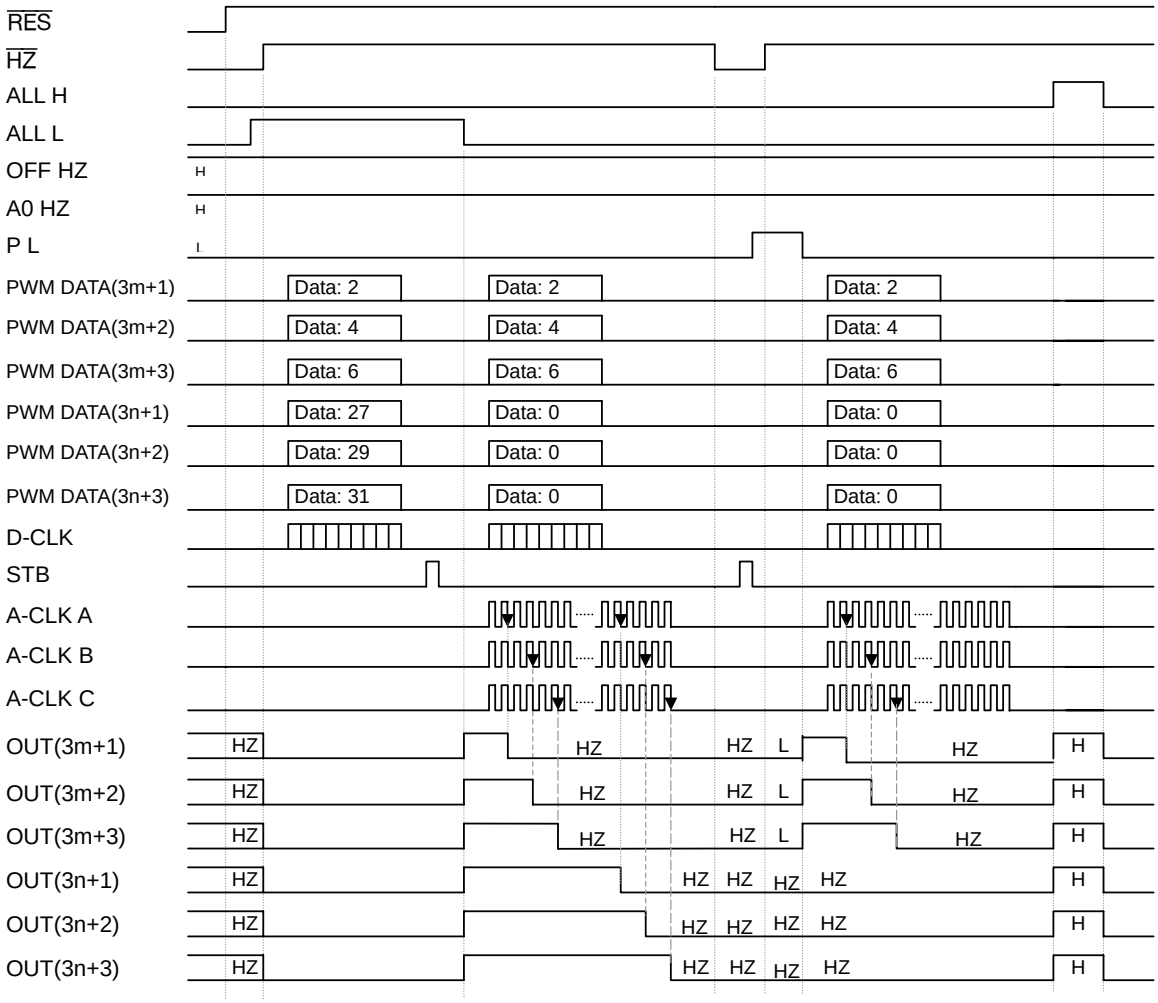
* m, n: 0 to 85

5. When OFF HZ is high, A0 HZ is low, and P L is controlled by pulse



* m, n: 0 to 85

6. When OFF HZ and A0 HZ are high and P L is controlled by pulse



* m, n: 0 to 85

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Logic power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +6.5	V
EL drive power supply voltage (anode)	V_{DISP}	Ta = 25°C	–0.3 to +25	V
Logic input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Logic output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
EL output current adjustment voltage	V_{EL}	Ta = 25°C	–0.3 to V_{DISP} + 0.3	V
EL driver output voltage	V_{OUT-EL}	Applied to OUT1 to OUT258	–0.3 to V_{DISP} + 0.3	V
EL driver output voltage (pulse)	$V_{OUT-ELP}$	Applied to OUT1 to OUT258	$-V_{DISP}$ to $V_{DISP} \times 2$	V
EL driver output current	I_{ELH} (source)	Applied to OUT1 to OUT258	–500	µA
	I_{ELL} (sink)		50	mA
Storage temperature	Tstg	—	–40 to +125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Logic power supply voltage	V_{DD}	—	2.7 to 5.5	V
EL drive power supply voltage (anode)	V_{DISP}	—	8 to 20	V
Logic input voltage	V_{IN}	—	0.0 to V_{DD}	V
EL output current adjustment voltage	V_{EL}	—	5 to V_{DISP}/2	V
EL driver output current	I_{ELH} (source)	Applied to OUT1 to OUT258	–400 to 0	µA
	I_{ELL} (sink)	Applied to OUT1 to OUT258	0 to 35	mA
Junction operating temperature	Tjop	—	–40 to +125	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{DD} = 2.7 to 5.5 V, V_{DISP} = 8 to 20 V, Tjop = –40 to +125°C

Parameter	Symbol	Applicable Pins	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	All input pins	—	$0.8V_{DD}$	—	V_{DD}	V
"L" input voltage	V_{IL}	All input pins	—	0	—	$0.2V_{DD}$	V
Schmitt voltage width	V_{SH}	D-CLK, A-CLK, STB, I-CLK, ALL H, ALL L	V_{DD} = 5.0 V	0.4	—	0.9	V
"H" input current	I_{IH1}	Inputs other than $\overline{RES}$, $\overline{HZ}$, A0HZ, $\overline{M}$/S, PL ALL H, ALL L, V_{EL}SEL, $\overline{F}$/R, and I-$\overline{F}$/R	V_{DD} = 5.5 V V_I = 5.5 V	—	—	10	µA
	I_{IH2}	$\overline{RES}$, PL, $\overline{M}$/S, ALL H, ALL L, V_{EL}SEL, $\overline{F}$/R, I-$\overline{F}$/R	V_{DD} = 5.5 V V_I = 5.5 V	30	—	300	µA
	I_{IH3}	$\overline{HZ}$, A0HZ	V_{DD} = 5.5 V V_I = 5.5 V	—	—	10	µA
"L" input current	I_{IL1}	Inputs other than $\overline{RES}$, $\overline{HZ}$, A0HZ, $\overline{M}$/S, PL, ALL H, ALL L, V_{EL}SEL, $\overline{F}$/R, and I-$\overline{F}$/R	V_{DD} = 5.5 V V_I = 0.0 V	—	—	10	µA
	I_{IL2}	$\overline{RES}$, PL, $\overline{M}$/S, ALL H, ALL L, V_{EL}SEL, $\overline{F}$/R, I-$\overline{F}$/R	V_{DD} = 5.5 V V_I = 0.0 V	—	—	10	µA
	I_{IL3}	$\overline{HZ}$, A0HZ	V_{DD} = 5.5 V V_I = 0.0 V	–300	—	–30	µA
"H" output voltage	V_{OH}	PADJn-I/O, PADJn-O/I	V_{DD} = 2.7 V I_O = –200 µA	$0.9V_{DD}$	—	—	V
"L" output voltage	V_{OL}	PADJn-I/O, PADJn-O/I	V_{DD} = 2.7 V I_O = 200 µA	—	—	$0.1V_{DD}$	V
Anode driver ON current 1	I_{ELON1}	OUT1 to OUT258	V_{DISP} = 20 V V_{EL} = V_O = 5 V V_{EL}SEL = high R_{EL} =33.3 kΩ Current adjustment range = 337.5%	–93 (–7%)	–100	–107 (+7%)	µA
Anode driver ON current 2	I_{ELON2}	OUT1 to OUT258	V_{DISP} = 20 V V_O = 5 V V_{EL}SEL = low R_{EL} = 33.3 kΩ Current adjustment range = 337.5%	–90 (–10%)	–100	–110 (+10%)	µA
Anode driver low output current 1	I_{ELL1}	OUT1 to OUT258	V_{DISP} = 8 V V_O = 8 V	5	—	—	mA
Anode driver low output current 2	I_{ELL2}	OUT1 to OUT258	V_{DISP} = 20 V V_O = 20 V	35	—	—	mA
Anode driver low output current 3	I_{ELL3}	OUT1 to OUT258	V_{DISP} = 8 V V_O = 1 V	0.5	—	—	mA
Anode driver low output current 4	I_{ELL4}	OUT1 to OUT258	V_{DISP} = 20 V V_O = 1 V	5	—	—	mA
Anode driver HZ output current	I_{ELHZ}	OUT1 to OUT258	OUT1 to OUT258 = "HZ"	–1	—	1	µA

DC Characteristics

V_{DD} = 2.7 to 5.5 V, V_{DISP} = 8 to 20 V, Tjop = –40 to +125°C

Parameter	Symbol	Applicable Pins	Condition	Min.	Typ.	Max.	Unit
V_{DISP} dependence coefficient for anode driver ON current *1	ΔI_{ELON1}	OUT1 to OUT258	V_{EL} = V_O = 5 V R_{EL} = 33.3 kΩ Current adjustment range = 337.5%	–2.5	0	2.5	%/V
V_O dependence coefficient for anode driver ON current *2	ΔI_{ELON2}	OUT1 to OUT258	V_{DISP} = 20 V V_{EL} = 5 V V_O = 5 to 18 V R_{EL} = 33.3 kΩ Current adjustment range = 337.5%	–2.5	0	2.5	%/V
Temperature coefficient for anode driver ON current	ΔI_{ELON3}	OUT1 to OUT258	V_{DISP} = 20 V V_{EL} = V_O = 5 V R_{EL} = 33.3 kΩ Current adjustment range = 337.5%	–0.1	0	0.1	%/°C
Relative error between dots (excluding adjoining dots) for anode driver ON current	ΔI_{ELON4}	OUT1 to OUT258	V_{DISP} = 20 V V_{EL} = V_O = 5 V R_{EL} = 33.3 kΩ Current adjustment range = 337.5% OUT1 to OUT258 = “ON” Inside one chip.	–5	0	5	%
Relative error between adjoining dots for anode driver ON current *3	ΔI_{ELON5}	OUT1 to OUT258	V_{DISP} = 20 V V_{EL} = V_O = 5 V R_{EL} = 33.3 kΩ Current adjustment range = 337.5% OUT1 to OUT258 = “ON” Inside one chip.	–2.0	0	2.0	%

*1 V_{DISP} dependence coefficient depends on the following conditions:
$\{(I_{ELON(@VDISP=nV)}) - (I_{ELON(@VDISP=8V)})\}*100 / \{(I_{ELON(@VDISP=8V)})*(n-8)\}$ n = 9 to 20 V , step 1 V

*2 V_O dependence coefficient depends on the following conditions:
$\{(I_{ELON(@VO=nV)}) - (I_{ELON(@VO=5V)})\}*100 / \{(I_{ELON(@VO=5V)})*(n-5)\}$ n = 6 to 18 V , step 1 V

*3 A relative error between adjoining dots depends on the following condition:
$(I_{ELON(@OUT[N+1])} - I_{ELON(@OUT[N])})*100 / \{(I_{ELON(@OUT[N+1])} + I_{ELON(@OUT[N])}) / 2\}$ N = 1 to 257

Supply Current

V_{DD} = 2.7 to 5.5 V, V_{DISP} = 8 to 20 V, Tjop = –40 to +125°C

Parameter	Symbol	Applicable Pins	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{DISP1}	V_{DISP}	V_{DISP} = 20 V V_{EL} = 5 V A-CLK = 10 MHz R_{EL} = 33.3 kΩ Current adjustment range = 337.5% Output = open PWM data = other than “0”	—	—	20	mA
	I_{DISP2}	V_{DISP}	V_{DD} = 0 V V_{DISP} = 20 V V_{EL} = 5 V R_{EL} = 33.3 kΩ Output = open	—	—	400	µA
	I_{DD1}	V_{DD}	V_{DD} = 5.5 V D-CLK = 10 MHz DATA = “1010.....10”	—	—	45	mA
		V_{DD}	V_{DD} = 5.5 V D-CLK, A-CLK = 10 MHz DATA = “1010.....10”	—	—	70	mA
		V_{DD}	V_{DD} = 5.5 V A-CLK = 10 MHz DATA = “1010.....10”	—	—	25	mA
	I_{DD2}	V_{DD}	V_{DD} = 5.5 V, D-CLK = halted $\overline{RES}$ = 0 V $\overline{HZ}$, A0HZ = 5.5 V All the other inputs are also 0 V.	—	—	350	µA

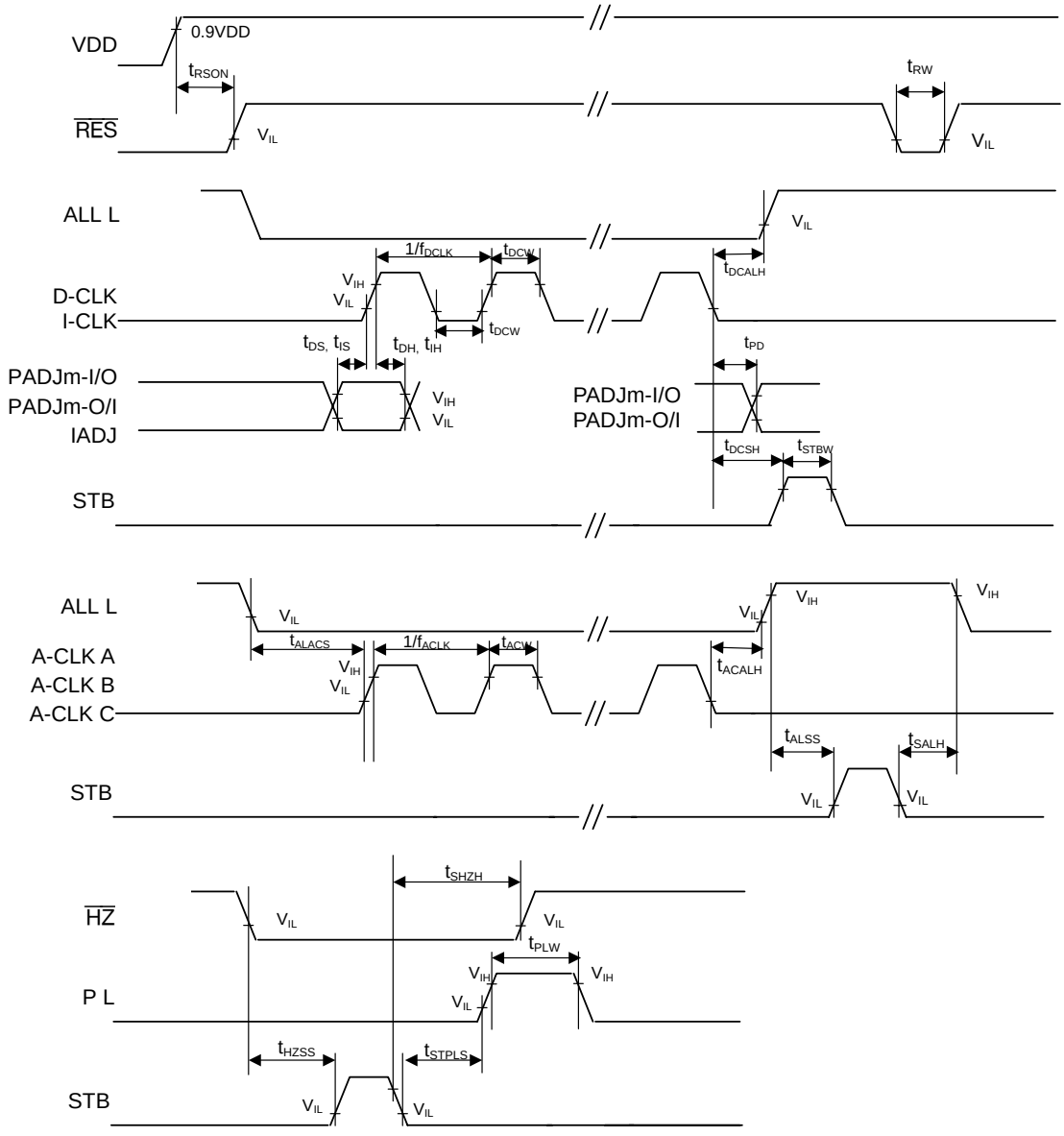
AC Characteristics

V_{DD} = 2.7 to 5.5 V, V_{DISP} = 8 to 20 V, Tjop = –40 to +125°C

Parameter	Symbol	Applicable pins	Condition	Min.	Typ.	Max.	Unit
D-CLK frequency	f_{DCLK}	D-CLK	—	0		10	MHz
D-CLK pulse width	t_{DCW}	D-CLK	—	25	—	—	ns
I-CLK frequency	f_{ICLK}	I-CLK	—	0		10	MHz
I-CLK pulse width	t_{ICW}	I-CLK	—	25	—	—	ns
A-CLK frequency	f_{ACLK}	A-CLK	—	0		10	MHz
A-CLK pulse width	t_{ACW}	A-CLK	—	25	—	—	ns
DATA→I-CLK setup time	t_{IS}	I-CLK IADJ	—	25	—	—	ns
I-CLK→DATA hold time	t_{IH}	I-CLK IADJ	—	25	—	—	ns
DATA→D-CLK setup time	t_{DS}	D-CLK PADJm-I/O PADJm-O/I	—	25	—	—	ns
D-CLK→DATA hold time	t_{DH}	D-CLK PADJm-I/O PADJm-O/I	—	25	—	—	ns
STB pulse width	t_{STBW}	STB	—	25	—	—	ns
ALL L→STB setup time	t_{ALSS}	ALL L, STB	—	50	—	—	ns
STB→ALL L hold time	t_{SALH}	ALL L, STB	—	50	—	—	ns
$\overline{HZ}$→STB setup time	t_{HZSS}	$\overline{HZ}$, STB	—	50	—	—	ns
STB→$\overline{HZ}$ hold time	t_{SHZH}	$\overline{HZ}$, STB	—	50	—	—	ns
D-CLK→ALL L hold time	t_{DCALH}	ALL L, D-CLK	—	50	—	—	ns
ALL L→A-CLK setup time	t_{ALACS}	ALL L, A-CLK	—	50	—	—	ns
A-CLK→ALL L hold time	t_{ACALH}	ALL L, A-CLK	—	50	—	—	ns
P L pulse width	t_{PLW}	P L	—	50	—	—	ns
P L→ALL L setup time	t_{PLALS}	ALL L, P L	—	50	—	—	ns
STB→P L setup time	t_{STPLS}	P L, STB	—	50	—	—	ns
D-CLK→STB hold time	t_{DCSH}	D-CLK STB	—	50	—	—	ns
$\overline{RES}$ time when powered up time	t_{RSON}	$\overline{RES}$, V_{DD}	—	250	—	—	ns
$\overline{RES}$ pulse width	t_{RW}	$\overline{RES}$	—	100	—	—	ns
D-CLK→DATA output time	t_{PD}	D-CLK PADJm-I/O PADJm-O/I	—	—	—	25	ns
A-CLK → output delay time	t_{Df}	$\overline{HZ}$, ALL H, ALL L P L, A-CLK OUT1 to OUT258	—	—	—	1.0	µs

TIMING DIAGRAM

Data Input



DESCRIPTION OF OPERATION

Initial Settings

The following initial settings can be made by setting the $\overline{RES}$ pin to low.

- Anode drive signal output pins (OUT1 to 258) become high impedance.

Anode Output Current Adjustment

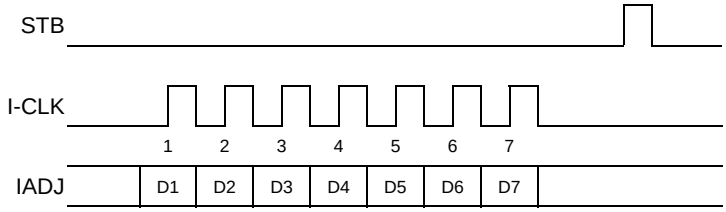
1. Output current settings
   Output currents of anode drive signal output pins (OUT1 to OUT258) are adjusted by varying the value of the resistor connected between the REL pin and GND. Output currents (typ.) at the time that the V_{EL}SEL pin is "high" and "low" are given by the following expressions:

   [When the V_{EL}SEL pin is "high"]
   Output current (typ.) = V_{EL} pin voltage ÷ (value of resistor connected to REL pin) × 2/3

   [When the V_{EL}SEL pin is "low"]
   Output current (typ.) = 5 V ÷ (value of resistor connected to REL pin) × 2/3

2. Output current adjustment for entire output
   Output currents of anode drive signal output pins (OUT1 to OUT258) can be adjusted, as a batch adjustment for all the output pins. Adjustment of output current is made by 7-bit data of IADJ. The data is shifted in the shift register at the rising edge of the I-CLK signal and latched at the rising edge of the STB signal.

   Relation between IADJ and output current is shown below. The output current of 337.5% is equal to the output current (typ.) set by the resistor connected to the REL pin.



	MSB						LSB	
Bit	D7	D6	D5	D4	D3	D2	D1	Output current adjustment range
Input data (IADJ)	0	0	0	0	0	0	0	20.0%
	0	0	0	0	0	0	1	22.5%
	0	0	0	0	0	1	0	25.0%
	0	0	0	0	0	1	1	27.5%
	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•
	1	1	1	1	1	0	0	330.0%
	1	1	1	1	1	0	1	332.5%
	1	1	1	1	1	1	0	335.0%
	1	1	1	1	1	1	1	337.5%

3. Output pulse width adjustment
   Output pulse width of anode drive signal output pins (OUT1 to OUT258) can be adjusted for each output pin. Adjustment of each output pulse width is made by 5-bit data PADJ0-n, PADJ1-n, PADJ2-n, PADJ3-n, and PADJ4-n (n represents I/O or O/I). This 5-bit data is shifted in the shift register at the rising edge of the D-CLK signal and latched at the rising edge of the STB signal. An anode drive signal output pin is configured as constant current output until the number of A-CLK A, A-CLK B, and A-CLK C pulses becomes equal to the output data of 5 bits of PADJ0-n, PADJ1-n, PADJ2-n, PADJ3-n, and PADJ4-n. The output becomes low or high impedance at the rising edge of the A-CLK A, A-CLK B, and A-CLK C pulse that has matched the output data of PADJ0-n, PADJ1-n, PADJ2-n, PADJ3-n, and PADJ4-n. The pulse width adjusting clocks of the anode drive signal outputs of the OUT (3m+1) pin, OUT (3m+2) pin, and OUT (3m+3) pin are input to A-CLK A, A-CLK B, and A-CLK C, respectively (m represents 0 to 85).

   Relation between PADJ0-n, PADJ1-n, PADJ2-n, PADJ3-n, and PADJ4-n and output pulse width is shown below.

PADJ4-n	PADJ3-n	PADJ2-n	PADJ1-n	PADJ0-n	Output pulse width
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

Setting of Output Condition When Dot is OFF

The output condition when dot is OFF is set with the combination of $\overline{HZ}$, ALL L, OFF HZ, A0 HZ, and P L signals. See “3. Operation of Output Section” in “FUNCTION TABLE” and the section of “OUTPUT WAVEFORMS”.

Power Applying Sequence

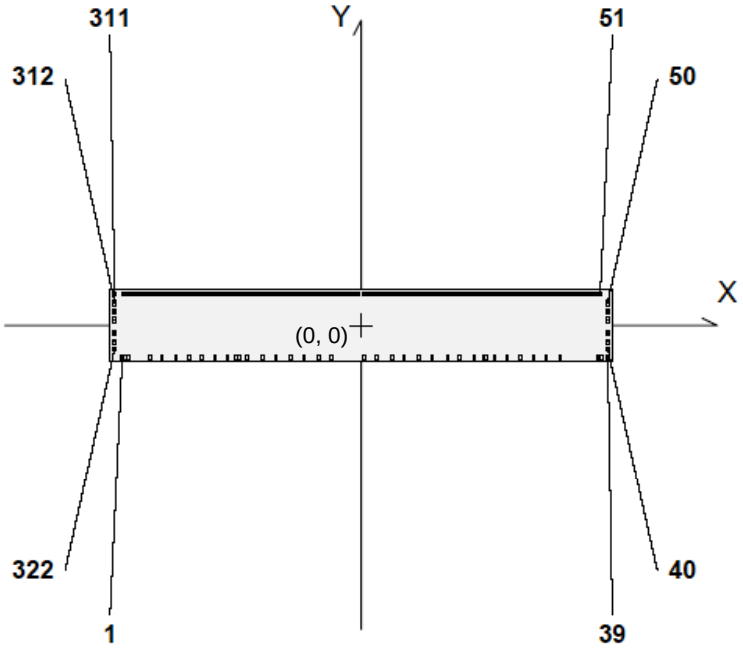
There is no restriction in power applying sequence of V_{DD} and V_{DISP}. When V_{DISP} is applied and V_{DD} is not applied, the following operating states occur.

- Constant current source circuit does not operate.
- Anode drive signal output pins (OUT1 to 258) become high impedance.

Make the $\overline{RES}$ pin high at least 250 ns after V_{DD} is applied.
(Refer to $\overline{RES}$ execution time in AC Characteristics.)
Make the other input pins high after applying power to the logic power supply (V_{DD}).
In addition, make all the input pins low before turning off the logic power supply (V_{DD}).

ML9362DVx PAD INFORMATION

- Chip View

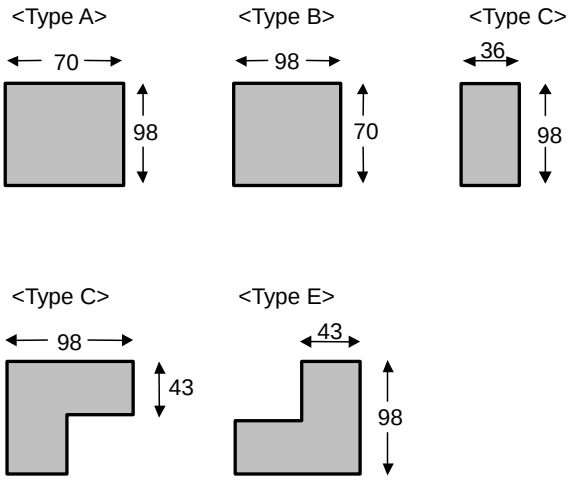


Numbers indicate pin numbers.

- Chip Size

· Chip size 14.75 (0 to –0.04) x 2.18 (0 to –0.04) x 0.625 (±0.015) [mm]

- Bump Pad Size (μm)



• PAD Coordinates

Pin No.	Pin Name	Coordinates		Pad Type	Pin No.	Pin Name	Coordinates		Pad Type
		X [μm]	Y [μm]				X [μm]	Y [μm]	
1	ISYNC-I/O	-7015	-956	A	161	OUT149	1080	956	C
2	REL	-6925	-956	A	162	OUT148	1026	956	C
3	VEL	-6835	-956	A	163	OUT147	972	956	C
4	D-CLK	-6204	-956	A	164	OUT146	918	956	C
5	STB	-5848	-956	A	165	OUT145	864	956	C
6	PADJ0-I/O	-5439	-956	A	166	OUT144	810	956	C
7	PADJ1-I/O	-5053	-956	A	167	OUT143	756	956	C
8	PADJ2-I/O	-4679	-956	A	168	OUT142	702	956	C
9	PADJ3-I/O	-4293	-956	A	169	OUT141	648	956	C
10	PADJ4-I/O	-3919	-956	A	170	OUT140	594	956	C
11	VDD	-3665	-956	A	171	OUT139	540	956	C
12	VDD	-3585	-956	A	172	OUT138	486	956	C
13	HZ	-3346	-956	A	173	OUT137	432	956	C
14	ALLH	-2892	-956	A	174	OUT136	378	956	C
15	M/S	-2506	-956	A	175	OUT135	324	956	C
16	I-F/R	-2062	-956	A	176	OUT134	270	956	C
17	ALLL	-1676	-956	A	177	OUT133	216	956	C
18	OFFHZ	-1232	-956	A	178	OUT132	162	956	C
19	A0HZ	-876	-956	A	179	OUT131	108	956	C
20	PL	86	-956	A	180	OUT130	54	956	C
21	A-CLKA	457	-956	A	181	OUT129	-54	956	C
22	A-CLKB	901	-956	A	182	OUT128	-108	956	C
23	A-CLKC	1257	-956	A	183	OUT127	-162	956	C
24	VELSEL	1701	-956	A	184	OUT126	-216	956	C
25	F/R	2087	-956	A	185	OUT125	-270	956	C
26	IADJ	2531	-956	A	186	OUT124	-324	956	C
27	I-CLK	2887	-956	A	187	OUT123	-378	956	C
28	RES	3331	-956	A	188	OUT122	-432	956	C
29	GND-L	3585	-956	A	189	OUT121	-486	956	C
30	GND-L	3665	-956	A	190	OUT120	-540	956	C
31	PADJ4-O/I	3919	-956	A	191	OUT119	-594	956	C
32	PADJ3-O/I	4293	-956	A	192	OUT118	-648	956	C
33	PADJ2-O/I	4679	-956	A	193	OUT117	-702	956	C
34	PADJ1-O/I	5053	-956	A	194	OUT116	-756	956	C
35	PADJ0-O/I	5439	-956	A	195	OUT115	-810	956	C
36	DUMMY	5848	-956	A	196	OUT114	-864	956	C
37	ISYNC-O/I	6945	-956	A	197	OUT113	-918	956	C
38	DUMMY	7060	-956	A	198	OUT112	-972	956	C
39	TCPMARK	7241	-956	E	199	OUT111	-1026	956	C
40	GND-L	7241	-707	B	200	OUT110	-1080	956	C
41	GND-D	7241	-527	B	201	OUT109	-1134	956	C

Pin No.	Pin Name	Coordinates		Pad Type	Pin No.	Pin Name	Coordinates		Pad Type
		X [μm]	Y [μm]				X [μm]	Y [μm]	
42	GND-D	7241	-447	B	202	OUT108	-1188	956	C
43	GND-D	7241	-267	B	203	OUT107	-1242	956	C
44	GND-D	7241	-187	B	204	OUT106	-1296	956	C
45	VDISP	7241	132	B	205	OUT105	-1350	956	C
46	VDISP	7241	212	B	206	OUT104	-1404	956	C
47	VDISP	7241	382	B	207	OUT103	-1458	956	C
48	VDISP	7241	462	B	208	OUT102	-1512	956	C
49	VDISP	7241	632	B	209	OUT101	-1566	956	C
50	VDISP	7241	712	B	210	OUT100	-1620	956	C
51	DUMMY	7020	956	C	211	OUT99	-1674	956	C
52	OUT258	6966	956	C	212	OUT98	-1728	956	C
53	OUT257	6912	956	C	213	OUT97	-1782	956	C
54	OUT256	6858	956	C	214	OUT96	-1836	956	C
55	OUT255	6804	956	C	215	OUT95	-1890	956	C
56	OUT254	6750	956	C	216	OUT94	-1944	956	C
57	OUT253	6696	956	C	217	OUT93	-1998	956	C
58	OUT252	6642	956	C	218	OUT92	-2052	956	C
59	OUT251	6588	956	C	219	OUT91	-2106	956	C
60	OUT250	6534	956	C	220	OUT90	-2160	956	C
61	OUT249	6480	956	C	221	OUT89	-2214	956	C
62	OUT248	6426	956	C	222	OUT88	-2268	956	C
63	OUT247	6372	956	C	223	OUT87	-2322	956	C
64	OUT246	6318	956	C	224	OUT86	-2376	956	C
65	OUT245	6264	956	C	225	OUT85	-2430	956	C
66	OUT244	6210	956	C	226	OUT84	-2484	956	C
67	OUT243	6156	956	C	227	OUT83	-2538	956	C
68	OUT242	6102	956	C	228	OUT82	-2592	956	C
69	OUT241	6048	956	C	229	OUT81	-2646	956	C
70	OUT240	5994	956	C	230	OUT80	-2700	956	C
71	OUT239	5940	956	C	231	OUT79	-2754	956	C
72	OUT238	5886	956	C	232	OUT78	-2808	956	C
73	OUT237	5832	956	C	233	OUT77	-2862	956	C
74	OUT236	5778	956	C	234	OUT76	-2916	956	C
75	OUT235	5724	956	C	235	OUT75	-2970	956	C
76	OUT234	5670	956	C	236	OUT74	-3024	956	C
77	OUT233	5616	956	C	237	OUT73	-3078	956	C
78	OUT232	5562	956	C	238	OUT72	-3132	956	C
79	OUT231	5508	956	C	239	OUT71	-3186	956	C
80	OUT230	5454	956	C	240	OUT70	-3240	956	C
81	OUT229	5400	956	C	241	OUT69	-3294	956	C
82	OUT228	5346	956	C	242	OUT68	-3348	956	C
83	OUT227	5292	956	C	243	OUT67	-3402	956	C
84	OUT226	5238	956	C	244	OUT66	-3456	956	C
85	OUT225	5184	956	C	245	OUT65	-3510	956	C

Pin No.	Pin Name	Coordinates		Pad Type	Pin No.	Pin Name	Coordinates		Pad Type
		X [μm]	Y [μm]				X [μm]	Y [μm]	
86	OUT224	5130	956	C	246	OUT64	-3564	956	C
87	OUT223	5076	956	C	247	OUT63	-3618	956	C
88	OUT222	5022	956	C	248	OUT62	-3672	956	C
89	OUT221	4968	956	C	249	OUT61	-3726	956	C
90	OUT220	4914	956	C	250	OUT60	-3780	956	C
91	OUT219	4860	956	C	251	OUT59	-3834	956	C
92	OUT218	4806	956	C	252	OUT58	-3888	956	C
93	OUT217	4752	956	C	253	OUT57	-3942	956	C
94	OUT216	4698	956	C	254	OUT56	-3996	956	C
95	OUT215	4644	956	C	255	OUT55	-4050	956	C
96	OUT214	4590	956	C	256	OUT54	-4104	956	C
97	OUT213	4536	956	C	257	OUT53	-4158	956	C
98	OUT212	4482	956	C	258	OUT52	-4212	956	C
99	OUT211	4428	956	C	259	OUT51	-4266	956	C
100	OUT210	4374	956	C	260	OUT50	-4320	956	C
101	OUT209	4320	956	C	261	OUT49	-4374	956	C
102	OUT208	4266	956	C	262	OUT48	-4428	956	C
103	OUT207	4212	956	C	263	OUT47	-4482	956	C
104	OUT206	4158	956	C	264	OUT46	-4536	956	C
105	OUT205	4104	956	C	265	OUT45	-4590	956	C
106	OUT204	4050	956	C	266	OUT44	-4644	956	C
107	OUT203	3996	956	C	267	OUT43	-4698	956	C
108	OUT202	3942	956	C	268	OUT42	-4752	956	C
109	OUT201	3888	956	C	269	OUT41	-4806	956	C
110	OUT200	3834	956	C	270	OUT40	-4860	956	C
111	OUT199	3780	956	C	271	OUT39	-4914	956	C
112	OUT198	3726	956	C	272	OUT38	-4968	956	C
113	OUT197	3672	956	C	273	OUT37	-5022	956	C
114	OUT196	3618	956	C	274	OUT36	-5076	956	C
115	OUT195	3564	956	C	275	OUT35	-5130	956	C
116	OUT194	3510	956	C	276	OUT34	-5184	956	C
117	OUT193	3456	956	C	277	OUT33	-5238	956	C
118	OUT192	3402	956	C	278	OUT32	-5292	956	C
119	OUT191	3348	956	C	279	OUT31	-5346	956	C
120	OUT190	3294	956	C	280	OUT30	-5400	956	C
121	OUT189	3240	956	C	281	OUT29	-5454	956	C
122	OUT188	3186	956	C	282	OUT28	-5508	956	C
123	OUT187	3132	956	C	283	OUT27	-5562	956	C
124	OUT186	3078	956	C	284	OUT26	-5616	956	C
125	OUT185	3024	956	C	285	OUT25	-5670	956	C
126	OUT184	2970	956	C	286	OUT24	-5724	956	C
127	OUT183	2916	956	C	287	OUT23	-5778	956	C
128	OUT182	2862	956	C	288	OUT22	-5832	956	C

Pin No.	Pin Name	Coordinates		Pad Type	Pin No.	Pin Name	Coordinates		Pad Type
		X [μm]	Y [μm]				X [μm]	Y [μm]	
129	OUT181	2808	956	C	289	OUT21	-5886	956	C
130	OUT180	2754	956	C	290	OUT20	-5940	956	C
131	OUT179	2700	956	C	291	OUT19	-5994	956	C
132	OUT178	2646	956	C	292	OUT18	-6048	956	C
133	OUT177	2592	956	C	293	OUT17	-6102	956	C
134	OUT176	2538	956	C	294	OUT16	-6156	956	C
135	OUT175	2484	956	C	295	OUT15	-6210	956	C
136	OUT174	2430	956	C	296	OUT14	-6264	956	C
137	OUT173	2376	956	C	297	OUT13	-6318	956	C
138	OUT172	2322	956	C	298	OUT12	-6372	956	C
139	OUT171	2268	956	C	299	OUT11	-6426	956	C
140	OUT170	2214	956	C	300	OUT10	-6480	956	C
141	OUT169	2160	956	C	301	OUT9	-6534	956	C
142	OUT168	2106	956	C	302	OUT8	-6588	956	C
143	OUT167	2052	956	C	303	OUT7	-6642	956	C
144	OUT166	1998	956	C	304	OUT6	-6696	956	C
145	OUT165	1944	956	C	305	OUT5	-6750	956	C
146	OUT164	1890	956	C	306	OUT4	-6804	956	C
147	OUT163	1836	956	C	307	OUT3	-6858	956	C
148	OUT162	1782	956	C	308	OUT2	-6912	956	C
149	OUT161	1728	956	C	309	OUT1	-6966	956	C
150	OUT160	1674	956	C	310	DUMMY	-7020	956	C
151	OUT159	1620	956	C	311	TCPMARK	-7241	956	D
152	OUT158	1566	956	C	312	VDISP	-7241	712	B
153	OUT157	1512	956	C	313	VDISP	-7241	632	B
154	OUT156	1458	956	C	314	VDISP	-7241	462	B
155	OUT155	1404	956	C	315	VDISP	-7241	382	B
156	OUT154	1350	956	C	316	VDISP	-7241	212	B
157	OUT153	1296	956	C	317	VDISP	-7241	132	B
158	OUT152	1242	956	C	318	GND-D	-7241	-187	B
159	OUT151	1188	956	C	319	GND-D	-7241	-267	B
160	OUT150	1134	956	C	320	GND-D	-7241	-447	B
					321	GND-D	-7241	-527	B
					322	GND-L	-7241	-707	B

- Bump Pad Specification

Item	Bump specification
Bump height	15 μm ±5 μm
Variation in height	4 μm or less
Bump hardness	30 to 80 HV

Definitions

- Bump height: Distance between the passivated surface and the center of the bump pin
- Variation in height: Difference between the maximum value and the miminum value of the bump height inside the chip
- Bump hardness: Micro Vickers hardness of the bump pin (load: 25 g)

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
QSY-43404	Oct. 18, 2005	–	–	Final edition 1

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