Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH

Datasheet

June 2003

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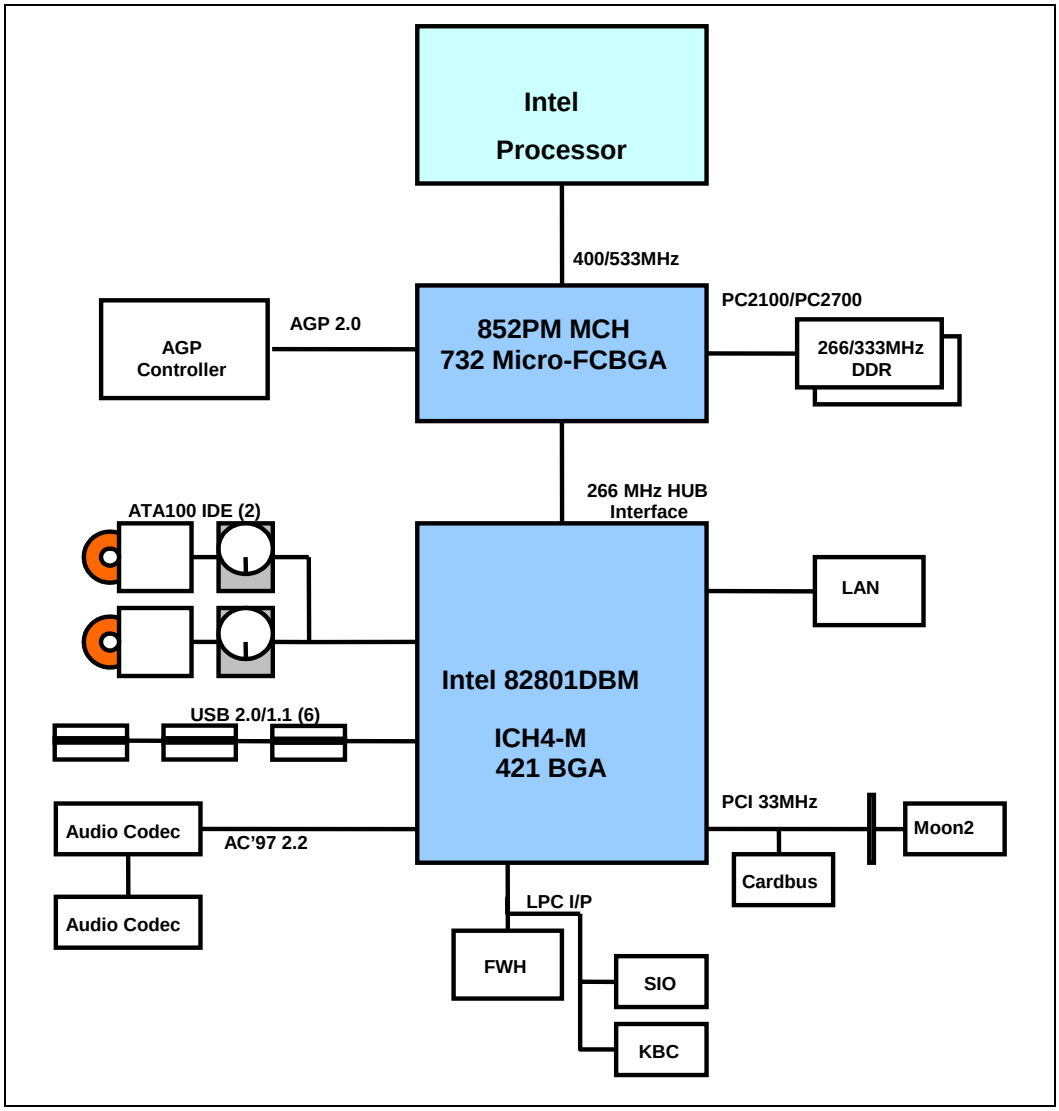
Revision History

Document No.	Rev. No.	Description	Rev. Date
253027	-001	Initial release	June 2002

Intel® 852PM Chipset MCH Features

- Processor/Host Bus Support
  - Mobile Intel® Pentium® 4 processor
  - Intel® Celeron® processor
  - Source synchronous double pumped Address (2X)
  - Source synchronous quad pumped Data (4X)
  - Supports a subset of the Enhanced Mode Scalable Bus Protocol
  - Intel Pentium 4 processor system bus interrupt delivery
  - Supports processor system bus at 400 & 533 MHz
  - Supports host Dynamic Bus Inversion (DBI)
  - Supports 32-bit host bus addressing
  - 8-deep, In-Order-Queue
  - AGTL+ bus driver technology with integrated AGTL termination resistors
  - Supports Enhanced Intel® SpeedStep® technology
- Memory System
  - Directly supports one DDR SDRAM channel, 64-bits wide
  - Supports 200/266/333-MHz DDR SDRAM devices with max of 2 Double-Sided SO-DIMMs with unbuffered PC1600/PC2100 DDR SDRAM.
  - Supports 128-Mbit, 256-Mbit, and 512-Mbit technologies
  - System memory support up to 1-GB with x16 devices and up to 2-GB with high density 512-Mbit devices
  - All supported devices have 4 banks
  - Supports up to 16 simultaneous open pages
  - ECC only supported with internal graphics
- System Interrupts
  - Supports Intel 8259 and processor system bus interrupt delivery mechanism
  - Supports interrupts signaled as upstream Memory Writes from PCI and hub interface
  - MSI sent to the CPU through the processor system bus
  - IOxAPIC in ICH4-M provides redirection for upstream interrupts to the system bus
- Accelerated Graphics Port (AGP) interface
  - Supports a single AGP device
  - Supports AGP 2.0 including 1x, 2x, and 4x AGP data transfers and 2x/4x
- Fast Write protocol
  - Supports only 1.5-V AGP electricals
  - 32 deep AGP request queue
  - PCI semantic (FRAME# initiated) accesses to DDR SDRAM are snooped
  - AGP semantic (PIPE# and SBA) accesses to DDR SDRAM are not snooped
  - Hierarchical PCI configuration mechanism
  - Delayed transaction support
  - 32-bit upstream address support for inbound AGP and PCI cycles
  - 32-bit downstream address support for outbound PCI and Fast Write cycles
  - AGP Busy/Stop Protocol
- Hub interface to ICH4-M
  - 266 MB/s point-to-point hub interface to ICH4-M
  - 66-MHz base clock
- Power Management
  - SMRAM space remapping to A0000h (128 kB)
  - Supports extended SMRAM space above 256-MB, additional 1-MB TSEG from Top of Memory, cacheable (cacheability controlled by CPU)
  - APM Rev 1.2 compliant power management
  - Supports Suspend to System Memory (S3), Suspend to Disk (S4) and Hard Off/Total Reboot (S5)
  - ACPI 1.0b, 2.0 Support
- Package
  - 732-pin Micro-FCBGA (37.5 x 37.5 mm)

Figure 1. Intel 852PM GMCH Chipset System Block Diagram



Intel® 852GME Chipset GMCH Features

Note: The Intel® 852GME chipset GMCH shares the same chipset features as the Intel 852PM chipset MCH along with the following additional integrated graphics features.

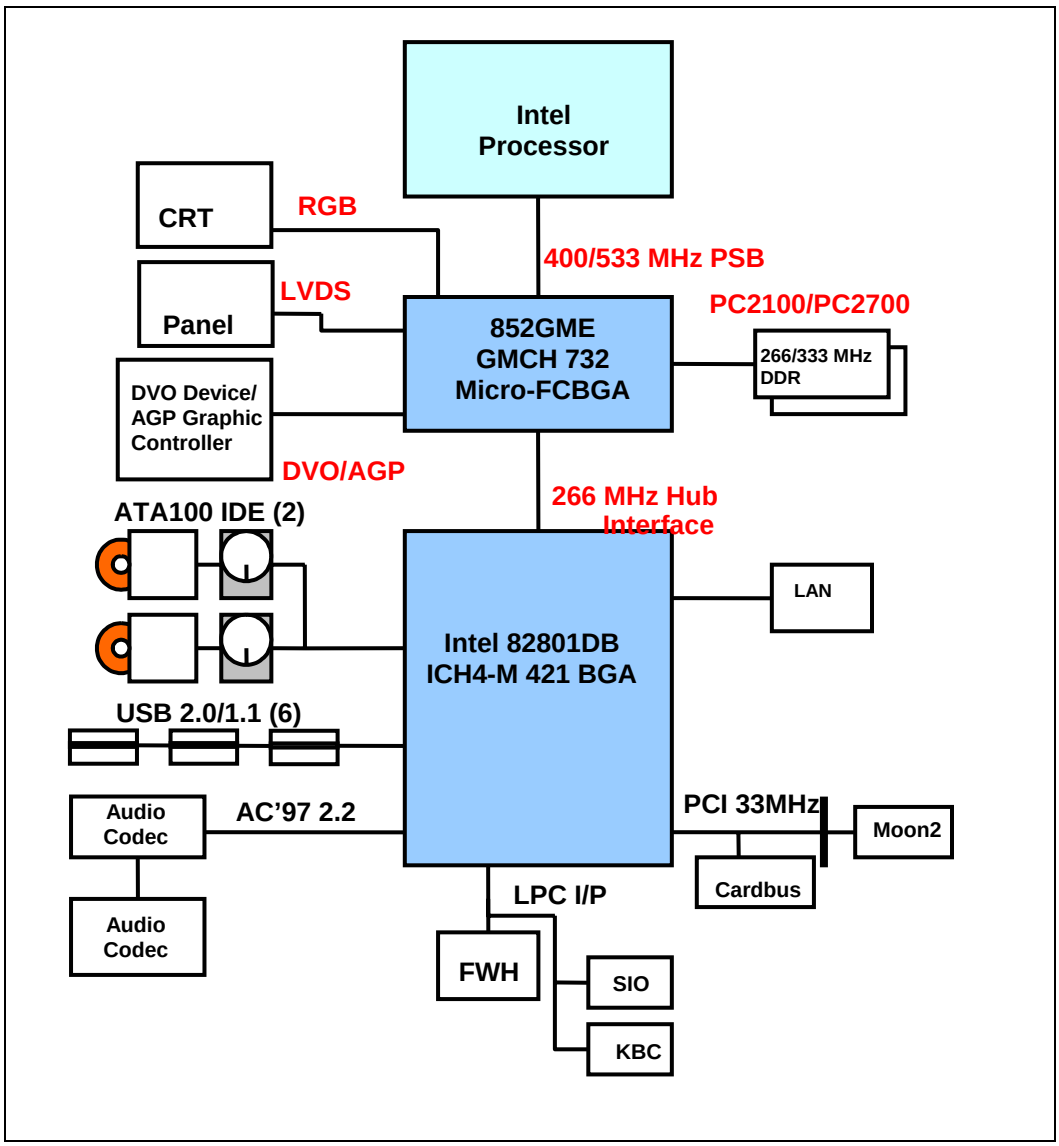
- Memory System
  - — ECC not supported with AGP
- Integrated Graphics Features
  - — Up to 64 MB of dynamic video memory allocation
  - — Display Image Rotation
  - — Core Frequency
    - Max 266-MHz graphics core frequency support at 1.5V
    - Display Core frequency of 133, 200, 250 266 MHz
    - Render Core frequency of 100,133, 200, 250, 266 MHz
- Video Stream Decoder
  - — HW Motion Compensation for MPEG2
  - — All format decoder (18 ATSC formats) supported
  - — Dynamic Bob and Weave support for Video Streams
  - — Support for standard definition DVD quality encoding at low CPU utilization
- Video Overlay
  - — Single high quality scalable Overlay and second Sprite to support second Overlay
  - — Multiple Overlay functionality provided via Arithmetic Stretch BLT (Block Transfer)
  - — 5-tap horizontal, 3-tap vertical filtered scaling
  - — Multiple Overlay formats
  - — Direct YUV from Overlay to TV-out
  - — Independent Gamma Correction
  - — Independent Brightness / Contrast / Saturation
  - — Independent Tint / Hue support
  - — Destination Colorkeying
  - — Source Chromakeying
- Display
  - — Analog Display Support
    - 350-MHz integrated 24-bit RAMDAC
  - — Dual independent pipe support
    - Concurrent: Different images and native display timings on each display device
  - — DVO support
    - Two Digital Video Out (DVO) port
- 2D Graphics Features
  - — Optimized 128-bit BLT engine
  - — Ten programmable and predefined
  - — monochrome patterns
  - — Alpha Stretch Blt (via 3D pipeline)
  - — Anti-aliased lines
  - — Hardware-based BLT Clipping and Scissoring
  - — 32-bit Alpha Blended cursor
  - — 64 x 64 3-color Transparent cursor
  - — Color Space Conversion
  - — 3 Operand Raster BLTs
  - — ROP support
- 3D Graphics Features
  - — 3D Setup and Render engine
  - — Viewpoint Transform and Perspective Divide
  - — Triangle Lists, Strips and Fans support
  - — Indexed Vertex and Flexible Vertex formats
  - — Pixel accurate Fast Scissoring and Clipping operation
  - — Backface Culling support
  - — DirectX* and OGL support
  - — Anti-Aliased and Sprite Points support
  - — High quality performance Texture Engine
  - — 266-MegaTexel/s peak performance
  - — Per Pixel Perspective Corrected Texture Mapping
  - — Single Pass Texture Compositing (Multi-Textures) at rate
  - — Enhanced Texture Blending functions
  - — Twelve Level of Detail MIP map sizes from 1x1 to 2Kx2K
  - — Alpha and Luminance Maps
  - — Texture Chromakeying
  - — Bilinear, Trilinear, and Anisotropic MIP-Mapped Filtering
  - — Cubic Environment Reflection Mapping
  - — Embossed Bump-Mapping
  - — DXTn Texture Decompression
  - — FX1 Texture Compression
  - — Flat and Gouraud Shading
  - — Color Alpha Blending for Transparency
  - — Vertex and Programmable Pixel Fog

supported
- Max 165-MHz dot clock
- Variety of DVO devices supported
- Compliant with DVI Specification 1.0

— Dedicated LFP LVDS interface
- Single or dual channel LVDS panel support up UXGA panel resolution with frequency range from 25-MHz to 112-MHz (single channel/dual channel)
- Supports data format of 18-bpp
- Compliant with ANSI/TIA/EIA –644-1995 specification
- SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
- LCD panel power sequencing compliant with SPWG timing specification
- Integrated PWM interface for LCD backlight inverter control
- Bi-linear Panel fitting

— Color Specular Lighting
— Z Bias support
— 16 and 24-bit Z Buffering
— 16 and 24-bit W Buffering
— 8-bit Stencil Buffering
— Double and Triple Render Buffer support
— Maximum 3D resolution of 1600x1200 at 85-Hz (contact your Intel Field Representative for detailed display information, i.e. pixel depths, etc.)
— Fast Clear support

Figure 2. Intel 852GME GMCH Chipset System Block Diagram



1 Overview

This datasheet provides Intel's specifications for the Intel® 852PM and Intel® 852GME chipset based systems.

The Intel 852PM chipset MCH is designed for use with the mobile Intel® Pentium® 4 processor or the Intel® Celeron® processor. The Intel MCH manages the flow of information between its five interfaces: the system bus interface, the system memory interface, the AGP interface, and the hub interface.

The Intel 852GME chipset GMCH is designed for use with the mobile Intel Pentium 4 processor or the Intel Celeron processor. The GMCH manages the flow of information between its seven interfaces: the system bus interface, the system memory interface, the analog VGA port, the DVOB and C interfaces, the hub interface, and the LVDS panel interface.

All recommendations will apply to all platforms unless specified. Any references to GMCH apply to both platforms unless otherwise specified.

1.1 Terminology

Term	Description
AGTL+	Advanced Gunning Transceiver Logic + (AGTL+) bus
DDC	Display Data Channel (standard created by VESA)
DPMS	Display Power Management Signaling (standard created by VESA)
I2C	Inter-IC (a two wire serial bus created by Philips)
CRT	Cathode Ray Tube
LCD	Liquid Crystal Display
BLI	Backlight Inverter
Core	The internal base logic in the Intel® 852GME/852PM GMCH
CPU	Central Processing Unit
DBI	Dynamic Bus inversion
DBL	Display Brightness Link
DVO	Digital Video Out
DVI*	Digital Visual Interface is the interface specified by the DDWG (Digital Display Working Group) DVI Spec. Rev. 1.0 utilizing only the Silicon Image developed TMDS protocol

Term	Description
DVMT	Dynamic Video Memory Technology
EDID	Extended Display Identification Data
Full Reset	A Full GMCH Reset is defined in this document when RSTIN# is asserted
GMCH	Graphics and Memory Controller Hub
Hub Interface (HI)	The proprietary interconnect between the GMCH and the ICH4-M component. In this document, the hub interface cycles originating from or destined for the ICH4-M are generally referred to as “hub interface cycles.” Hub cycles originating from or destined for the primary PCI interface on are sometimes referred to as “hub interface/PCI cycles”
Host	This term is used synonymously with processor
IGD	Integrated Graphics Device
Intel® 852GME GMCH	Refers to the GMCH component. Throughout this datasheet, the Intel /852GME GMCH will be referred to as the GMCH.
Intel® 852PM MCH	Refers to the MCH component. Throughout this datasheet, the Intel 852PM MCH will be referred to as the MCH.
Intel® 852 chipset Family	Refers to both 852GME and 852PM chipset.
Intel® 82801DBM ICH4-M	The component contains the primary PCI interface, LPC interface, USB 2.0, ATA-100, AC’97, and other I/O functions. It communicates with the GMCH over a proprietary interconnect called the hub interface. Throughout this datasheet, the Intel® 82801DBM ICH4-M component will be referred to as the ICH4-M
IPI	Inter Processor Interrupt
LFP	Local Flat Panel
LVDS	Low Voltage Differential Signals used for interfacing to LCD Flat Panels
MSI	Message Signaled Interrupts. MSI allow a device to request interrupt service via a standard memory write transaction instead of through a hardware signal
PSB	Processor System Bus. Connection between GMCH and the CPU. Also known as the Host interface
PWM	Pulse Width Modulation
SSC	Spread Spectrum Clocking
System Bus	Processor-to-GMCH interface. The Enhanced mode of the Scalable bus is the P6 Bus plus enhancements, consisting of source synchronous transfers for address and data, and system bus interrupt delivery. The mobile Intel Pentium 4 processor implements a subset of Enhanced mode.
UMA	Unified Memory Architecture with graphics memory for the IGD inside System Memory

Term	Description
VDL	Video Data Link
Primary PCI	Physical PCI bus that is driven directly by the component. It supports 3.3-V, 33-MHz PCI or PCI0 2.2 compliant components. Communication between PCI0 and the GMCH occurs over the hub interface. Note that although the Primary PCI bus is referred to as PCI0, it is not PCI Bus #0 from a configuration standpoint.
AGP	Accelerated Graphics Port. Refers to the AGP/PCI interface that is in the GMCH. It supports a 1.5-V, 66/266 MHz component. PIPE# and SBA cycles are generally referred to as AGP transactions. FRAME# cycles are generally referred to as AGP/PCI transactions.
AGP/PCI1	The physical bus that is driven directly by the AGP/PCI1 Bridge (Device #1) in the GMCH. This is the primary AGP bus.
GART	Graphics Aperture Re-map Table. This table contains the page re-map information used during AGP aperture address translations.
GTLB	Graphics Translation Look-aside Buffer. A cache used to store frequently used GART entries.

1.2 Reference Documents

Document	Document No./Location
Mobile Intel® Pentium® 4 Processor with 533 MHz System Bus Datasheet	Contact your Intel Field Representative
Intel® Celeron® Processor on 0.13 Micron Processor Datasheet	Contact your Intel Field Representative
PCI Local Bus Specification 2.2	http://www.pcisig.com
Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet (252337-001)	http://developer.intel.com/design/mobile/datashts/252337.htm
Advanced Configuration and Power Management(ACPI) Specification 1.0b & 2.0	http://www.teleport.com/~acpi/
Advanced Power Management (APM) Specification 1.2	http://www.microsoft.com/hwdev/busbios/amp_12.htm
IA-32 Intel® Architecture Software Developer Manual Volume 3: System Programming Guide	http://developer.intel.com/design/Pentium4/manuals/24547203.pdf
Intel® Graphics Software PC 13.0 Product Requirements	Contact your Intel Field Representative
Common Panel Interface Specification Version 1.6	Contact your Intel Field Representative

1.3 System Architecture Overview

1.3.1 Intel 852GME GMCH System Architecture

The Intel 852GME GMCH component provides the processor interface, DDR SDRAM interface, display interface, and hub interface in an Intel 852GME chipset platform. The GMCH is optimized for use with the Intel Celeron processor and the mobile Intel Pentium 4 processor. It supports a single channel of DDR SDRAM memory. The GMCH contains advanced power management logic. The Intel 852GME chipset platform supports the fourth generation mobile I/O Controller Hub (ICH4-M) to provide the features required by a mobile platform.

The Intel 852GME GMCH are in a 732-pin Micro-FCBGA package and contain the following functionality:

- Supports a single mobile Intel Pentium 4 processor configurations at 533 MHz
- System SDRAM supports 266/333MHz (SSTL_2) DDR SDRAM
- Up to 2 GB (with 256-Mbit technology and two SO-DIMMs) of PC2100/2700 DDR SDRAM with ECC
- Digital display support through two DVO ports (165-MHz, 12-bit DVO)
- Integrated 350-MHz, 24-bit RAMDAC with maximum pixel resolution support up to 1600x1200 at 85 Hz and up to 2048x1536 at 75 Hz
- One Dedicated Dual Channel LFP LVDS interface with frequency range of 25 MHz to 112 MHz (single channel/dual channel) for support up to UXGA (1600 x 1200 @ 60 Hz) panel resolutions with maximum pixel depth of 18-bpp
- AGP interface with 1x/2x/4x SBA/Data Transfer and 2x/4x Fast Write capability

1.3.2 Intel 852PM MCH System Architecture

The Intel 852PM MCH component share the same features as the Intel 852GME GMCH component, except it does not support internal graphics nor any corresponding display features (i.e., LFP LVDS interface, DAC interface, and DVO interface). It only supports external AGP graphics.

1.4 Processor Host Interface

Intel 852GME GMCH and 852PM MCH are optimized for the mobile Intel Pentium 4 processor. The key features are:

- Source synchronous double pumped address (2X)
- Source synchronous quad pumped data (4X)
- System Bus interrupt and side-band signal delivery
- A System Bus frequency of 400/533-MHz (Dual processor is not supported)

- AGTL+ termination resistors on all of the AGTL+ signals
- 32-bit host bus addressing allowing the CPU to access the entire 4 GB of the memory address space

The GMCH/MCH has a 12-deep In-Order Queue to support up to twelve outstanding pipelined address requests on the host bus. The GMCH/MCH supports one outstanding defer cycle at a time; however, it supports only one to any particular I/O interface. Host initiated I/O cycles are positively decoded to the GMCH/MCH configuration space and subtractively decoded to the hub interface. Host initiated memory cycles are positively decoded to DDR SDRAM. Memory accesses initiated from the hub interface to DDR SDRAM will be snooped on the System Bus.

Host initiated I/O cycles are decoded to AGP/PCI1, hub interface, or GMCH/MCH configuration space. Host initiated memory cycles are decoded to AGP/PCI1, hub interface, system memory. All memory accesses from the PSB that hit the graphics aperture are translated using an AGP address translation table. The GMCH/MCH access to graphics memory and AGP/PCI1 device accesses to non-cacheable system memory are not snooped on the PSB. Memory accesses initiated from AGP/PCI1 using PCI semantics and from hub interface to system memory will be snooped on the host bus.

1.4.1 Host Bus Error Checking

The Intel 852GME GMCH and Intel 852PM MCH do not generate nor check parity for Data, Address/Request, and Response signals on the processor bus.

1.5 Intel 852PM and 852GME DDR SDRAM Interface

The System Memory controller directly supports the following:

- One channel of PC1600/2100 SO-DIMM DDR SDRAM memory
- DDR SDRAM devices with densities of 128-Mbit, 256-Mbit, and 512-Mbit technology
- Maximum system memory support of two, double-sided SO-DIMMs (four rows populated) with up to 2 GB memory
- Variable page sizes of 2 kB, 4 kB, 8 kB, and 16 kB. Page size is individually selected for every row and a maximum of 16 pages may be opened simultaneously 2 GB of memory support is realized by utilizing a high density memory configuration.

Table 1. SDRAM Memory Capacity

Technology	Width	System Memory Capacity	System Memory Capacity with High Density
128 Mb	16	256 MB	-
256 Mb	16	512 MB	-
512 Mb	16	1 GB	-
128 Mb	8	256 MB	512 MB
256 Mb	8	512 MB	1 GB
512 Mb	8	1 GB	2 GB

The Intel 852PM MCH and Intel 852GME system memory interface supports a thermal throttling scheme to selectively throttle reads and/or writes. Throttling can be triggered either by on-die thermal sensor, or by preset write bandwidth limits. Read throttle can also be triggered by an external input pin. The memory controller logic supports aggressive dynamic row power down features (SCKE) to help reduce power and supports Address and Control lines tri-stating when DDR SDRAM is in active power down or self refresh.

The system memory architecture is optimized to maintain open pages (up to 16-kB page size) across multiple rows. As a result, up to 16 pages across four rows. To complement this, the GMCH will tend to keep pages open within rows, or will only close a single bank on a page miss. Intel 852PM MCH and Intel 852GME support only two bank memory technologies.

The Intel 852GME GMCH and Intel 852PM MCH allow the memory interface to provide optional ECC error checking for DDR SDRAM data integrity. During DDR SDRAM writes, ECC is generated on a QWORD (64-bit) basis. Because the GMCH/MCH stores only entire cache lines in its internal buffers, partial QWORD writes initially cause a read of the underlying data, and the write-back into memory is no different from that of a complete cache line. During DDR SDRAM reads and the read of the data that underlies partial writes, the GMCH/MCH supports detection of single-bit and multiple-bit errors, and will correct single bit errors when correction is enabled.

1.6 GMCH Internal Graphics Interface

The GMCH provides a highly integrated graphics accelerator delivering high performance 3D, 2D, and video capabilities. With its interfaces to UMA using a DVMT configuration, analog display, LVDS, and digital display (e.g. flat panel), the GMCH provides a complete graphics solution.

The GMCH also provides 2D hardware acceleration for block transfers of data (BLTs). The BLT engine provides the ability to copy a source block of data to a destination and perform raster operations (e.g., ROP1, ROP2, and ROP3) on the data using a pattern, and/or another destination. Performing these common tasks in hardware reduces processor load, and thus improves performance.

High bandwidth access to data is provided through the system memory ports. The GMCH uses Tiling architecture to increase system memory efficiency and thus maximize effective rendering bandwidth.

The GMCH has four display ports, one analog and three digital. These provide support for a progressive scan analog monitor, a dedicated dual channel LVDS panel and two DVO devices. The data that is sent out to the display port is selected from one of the two possible sources, pipe A or pipe B.

1.6.1 GMCH Analog Display Port

Intel 852GME GMCH has an integrated 350-MHz, 24-bit RAMDAC that can directly drive a progressive scan analog monitor pixel resolution up to 1600x1200 at 85-Hz refresh and up to 2048x1536 at 75-Hz refresh. The DAC port can be driven on Pipe A or Pipe B.

1.6.2 GMCH Integrated LVDS Port

The Intel 852GME GMCH has an integrated dual channel LFP Transmitter interface to support LVDS LCD panel resolutions up to UXGA with center and down spread SSC support of 0.5%, 1%, and 2.5% utilizing an external SSC clock.

The display pipe provides panel up-scaling to fit a source image into a specific panel size as well as panning and centering support. The LVDS port is only supported on Pipe B. The LVDS port can only be driven on Pipe B, either independently or simultaneously with the DAC port.

1.6.3 GMCH Integrated DVO Port

The DVO B/C interfaces are compliant with the DVI Specification 1.0. When combined with a DVI compliant external device (e.g. TMDS Flat Panel Transmitter, TV-out encoder, etc.), the GMCH provides a high-speed interface to a digital or analog display (e.g. flat panel, TV monitor, etc.).

Intel 852GME GMCH provides a DVO B and DVO C port that are each capable of driving a 165-MHz pixel clock. When DVO B and DVO C are combined, the effective dot clock can be increased to 330 MHz to support a dual channel (12-bit per channel) TV-Out Encoder. The DVO B/C ports can be driven on Pipe A or Pipe B. If driven on port B, then the LVDS port must be disabled.

1.7 External AGP Graphics Interface

1.7.1 Intel 852PM MCH and Intel 852GME GMCH AGP Interface

A single AGP component is supported by the AGP interface. The AGP buffers operate only in 1.5-V mode. They are not 3.3-V safe.

The AGP interface supports 1x/2x/4x AGP signaling and 2x/4x Fast Writes. AGP semantic cycles to DDR SDRAM are not snooped on the host bus. PCI semantic cycles to DDR SDRAM are snooped on the host bus. The GMCH/MCH support PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization. Both upstream and downstream addressing is limited to 32-bits for AGP and AGP/PCI transactions. The GMCH/MCH contains a 32-deep AGP request queue. High priority accesses are supported. All accesses from the AGP/PCI interface that fall

within the Graphics Aperture address range pass through an address translation mechanism with a fully associative 20 entry TLB. Accesses between AGP and hub interface are limited to memory writes originating from the hub interface destined for AGP. The AGP interface is clocked from a dedicated 66-MHz clock (GLCKIN). The AGP-to-host/core interface is asynchronous.

The AGP interface should be powered-off or tri-stated without voltage on the interface during ACPI S3 or APM Suspend to RAM state.

Refer to the AGP Busy and Stop Signals Specification for more information.

1.8 Hub Interface

A proprietary interconnect connects the GMCH/MCH to the ICH4-M chipset. All communication between the GMCH/MCH and the ICH4-M occur over the hub interface. The hub interface runs at 66 MHz or 266 MB/s.

1.9 Address Decode Policies

Host initiated I/O cycles are positively decoded to the GMCH/MCH configuration space and subtractively decoded to hub interface. Host initiated system memory cycles are positively decoded to DDR SDRAM and are again subtractively decoded to hub interface if under 4 GB. System memory accesses from hub interface to DDR SDRAM will be snooped on the PSB.

1.10 Platform Clocking

The GMCH/MCH has the following clock input/output pins:

- 400-MHz, Spread Spectrum, Low Voltage Differential BCLK, BCLK# for processor system bus
- 533-MHz Spread Spectrum, Low Voltage Differential BCLK, BCLK# for processor system bus (Intel 852GME GMCH and Intel 852PM MCH only)
- 66-MHz Spread Spectrum, 3.3-V GCLKIN for AGP and hub interface buffers
- Four pairs of differential output clocks (SCK[4,3,1:0], SCK[4,3,1:0]#), 200/266 MHz, 2.5 V for system memory interface
- 48-MHz, non-Spread Spectrum, 3.3-V DREFCLK for the Display Frequency Synthesis
- 48-MHz or 66-MHz, Spread Spectrum, 3.3-V DREFSSCLK for the Display Frequency Synthesis
- Up to 85-MHz, 1.5-V DVOBCCLKINT for TV-Out mode
- DPMS clock for S1-M

Clock Synthesizer chip(s) are responsible for generating the system host clocks, display and hub interface clocks, PCI clocks, and system memory clocks. The host target speed is 400 MHz or 533 MHz. The GMCH does not require any relationship between the BCLK host clock and the 66-MHz clock generated for the AGP and hub interface; they are asynchronous to each other. The

AGP and hub interface run at a constant 66-MHz base frequency. The hub interface runs at 4x, while AGP transfers may be at 1x, 2x, or 4x.

The following table indicates the frequency ratios between the various interfaces that the GMCH/MCH supports:

Table 2. Intel 852GME GMCH Interface Clocks

Interface	Clock Speed	CPU System Bus Frequency Ratio	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (Bytes)	Peak Bandwidth (MB/s)
CPU Bus	133 MHz	Reference	4	533	8	4264
DDR SDRAM	133 MHz	1:1 Synchronous	2	266	8	2128
	166 MHz	1:1 Synchronous	2	333	8	2664
AGP	66 MHz	Asynchronous	AGP Spec	AGP Spec	AGP Spec	AGP Spec

1.11 System Interrupts

The GMCH/MCH supports both the legacy Intel 8259 Programmable Interrupt delivery mechanism and the respective processor Interrupt delivery mechanism. The serial APIC Interrupt mechanism is not supported.

The Intel 8259 Interrupt delivery mechanism support consists of flushing in bound hub interface write buffers when an Interrupt Acknowledge cycle is forwarded from the system bus to the hub interface.

PCI MSI interrupts are generated as Memory Writes. The GMCH/MCH decodes upstream Memory Writes to the range 0FEE0_0000h - 0FEEF_FFFFh from the AGP and hub interface as message-based interrupts. The GMCH/MCH forwards the Memory Writes along with the associated write data to the system bus as an Interrupt Message transaction. Since this address does not decode as part of main system memory, the write cycle and the write data does not get forwarded to system memory via the write buffer. The GMCH/MCH provides the response and HTRDY# for all Interrupt Message cycles including the ones originating from the GMCH/MCH. The GMCH/MCH also supports interrupt re-direction for upstream interrupt memory writes.

For message based interrupts, system write buffer coherency is maintained by relying on strict ordering of Memory Writes. The GMCH/MCH ensure that all Memory Writes received from a given interface prior to an interrupt message Memory Write are delivered to the system bus for snooping in the same order that they occur on the given interface.

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2 Signal Description

This section describes the GMCH/MCH signals. These signals are arranged in functional groups according to their associated interface. The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal:

AGTL+	Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The GMCH integrates AGTL+ termination resistors, and AGTL+ signals are “inverted bus” style where a low voltage represents a logical 1.
DVO	DVO buffers (1.5-V tolerant)
AGP	AGP interface signals. These signals are compatible with AGP 2.0 1.5-V Signaling Environment DC and AC Specifications. The buffers are 1.5-V tolerant
Hub	Compatible to hub interface 1.5
SSTL_2	Stub series termination logic compatible signals (2.5-V tolerant)
LVTTL	Low voltage TTL compatible signals (3.3-V tolerant)
CMOS	CMOS buffers (3.3-V tolerant)
LVDS	Low voltage differential signal interface
Analog	Analog signal interface
Ref	Voltage reference signal

System Address and Data Bus signals are logically inverted signals. In other words, the actual values are inverted of what appears on the system bus. This must be taken into account and the addresses and data bus signals must be inverted inside the GMCH/MCH. All processor control signals follow normal convention: A 0 indicates an active level (low voltage), and a 1 indicates an active level (high voltage).

2.1 Host Interface Signals

Table 3. Host Interface Signal Descriptions

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase. The GMCH/MCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O AGTL+	**Bus Priority Request:** The GMCH/MCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	I/O AGTL+	**Bus Request 0#:** The GMCH/MCH pull the processor bus BREQ0# signal low during **CPURST#**. The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 BCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 BCLKs. BREQ0# should be tristated after the hold time requirement has been satisfied. During regular operation, the GMCH/MCH will use BREQ0# as an early indication for PSB Address and Ctl input buffer and sense amp activation.
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the GMCH/MCH. The GMCH/MCH asserts CPURST# while RESET# (PCIRST# from ICH4-M) is asserted and for approximately 1 ms after RESET# is deasserted. The CPURST# allows the processor to begin execution in a known state. Note that the ICH4-M must provide CPU strap set-up and hold-times around CPURST#. This requires strict synchronization between GMCH/MCH, CPURST# deassertion and ICH4-M driving the straps.
DBSY#	I/O AGTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer:** GMCH/MCH will generate a deferred response as defined by the rules of the GMCH/MCH's Dynamic Defer policy. The GMCH/MCH will also use the DEFER# signal to indicate a CPU retry response.
DINV[3:0]#	I/O AGTL+	**Dynamic Bus Inversion:** Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DINV#** **Data Bits** DINV[3]# HD[63:48]# DINV[2]# HD[47:32]# DINV[1]# HD[31:16]# DINV[0]# HD[16:0]#
DPSLP#	I CMOS	**Deep Sleep #:** This signal comes from the ICH4-M device, providing an indication of C3 and C4 state control to the CPU. Deassertion of this signal is used as an early indication for C3 and C4 wake up (to active HPLL).

Signal Name	Type	Description
		Note that this is a low-voltage CMOS buffer operating on the PSB VTT power plane.
DRDY#	I/O AGTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH/MCH drive HA[31:3]# during snoop cycles on behalf of hub interface. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSTB[1:0]#	I/O AGTL+	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe** **Address Bits** HADSTB[0]# HA[16:3]#, HREQ[4:0]# HADSTB[1]# HA[31:17]#
HD[63:0]#	I/O AGTL+	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus.
HDSTBP[3:0]# **HDSTBN[3:0]#**	I/O AGTL+	**Differential Host Data Strobes:** The differential source synchronous strobes are used to **transfer HD[63:0]# and DINV[3:0]# at** the 4x transfer rate. **Strobe** **Data Bits** HDSTBP[3]#, HDSTBN[3]# HD[63:48]#, DINV[3]# HDSTBP[2]#, HDSTBN[2]# HD[47:32]#, DINV[2]# HDSTBP[1]#, HDSTBN[1]# HD[31:16]#, DINV[1]# HDSTBP[0]#, HDSTBN[0]# HD[15:0]#, DINV[0]#
HIT#	I/O AGTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I/O AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no hub interface snoopable access to system memory is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O AGTL+	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the GMCH/MCH Host Bridge are defined in the Host Interface section of this document.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.

Signal Name	Type	Description
RS[2:0]#	O AGTL+	**Response Status:** Indicates the type of response according to the following the table: **RS[2:0]#** — **Response type** 000 — Idle state 001 — Retry response 010 — Deferred response 011 — Reserved (not driven by GMCH/MCH) 100 — Hard Failure (not driven by GMCH/MCH) 101 — No data response 110 — Implicit Write back 111 — Normal data response

2.2 DDR SDRAM Interface

Table 4. DDR SDRAM Interface Descriptions

Signal Name	Type	Description
SCS[3:0]#	O SSTL_2	**Chip Select:** These pins select the particular DDR SDRAM components during the active state. **NOTE:** There is one SCS# per DDR-SDRAM Physical SO-DIMM device row. These signals can be toggled on every rising system memory clock edge (SCMDCLK).
SMA[12:0]	O SSTL_2	**Multiplexed Memory Address:** These signals are used to provide the multiplexed row and column address to the DDR SDRAM.
SBA[1:0]	O SSTL_2	**Bank Select (Memory Bank Address):** These signals define which banks are selected within each DDR SDRAM row. The SMA and SBA signals combine to address every possible location within a DDR SDRAM device.
SRAS#	O SSTL_2	**DDR Row Address Strobe: SRAS#** may be heavily loaded and requires tw0 DDR SDRAM clock cycles for setup time to the DDR SDRAMs. Used with SCAS# and SWE# (along with SCS#) to define the system memory commands.
SCAS#	O SSTL_2	**DDR Column Address Strobe:** SCAS# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs. Used with SRAS# and SWE# (along with SCS#) to define the system memory commands.
SWE#	O SSTL_2	**Write Enable:** Used with SCAS# and SRAS# (along with SCS#) to define the DDR SDRAM commands. SWE# is asserted during writes to DDR SDRAM. SWE# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs.
SDQ[71:0]	I/O SSTL_2	**Data Lines:** These signals are used to interface to the DDR SDRAM data bus. **NOTE:** Intel 852GME/852PM: ECC error detection is not supported by the SDQ[71:64] signals if AGP interface is enabled

SDQS[8:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS is centered on data. During reads, SDQS is edge aligned with data. The following list matches the data strobe with the data bytes. There is an associated data strobe (DQS) for each data signal (DQ) and check bit (CB) group. SDQS[7] -> SDQ[63:56] SDQS[6] -> SDQ[55:48] SDQS[5] -> SDQ[47:40] SDQS[4] -> SDQ[39:32] SDQS[3] -> SDQ[31:24] SDQS[2] -> SDQ[23:16] SDQS[1] -> SDQ[15:8] SDQS[0] -> SDQ[7:0] **NOTE:** Intel 852GME/852PM: ECC error detection is not supported by the SDQ[71:64] signals if AGP interface is enabled
SCKE[3:0]	O SSTL_2	**Clock Enable:** These pins are used to signal a self-refresh or power down command to the DDR SDRAM array when entering system suspend. SCKE is also used to dynamically power down inactive DDR SDRAM rows. There is one SCKE per DDR SDRAM row. These signals can be toggled on every rising SCK edge.
SMAB[5,4,2,1]	O SSTL_2	**Memory Address Copies:** These signals are identical to SMA[5,4,2,1] and are used to reduce loading for selective CPC(clock-per-command). These copies are not inverted.
SDM[8:0]	O SSTL_2	**Data Mask:** When activated during writes, the corresponding data groups in the DDR SDRAM are masked. There is one SDM for every eight data lines. SDM can be sampled on both edges of the data strobes. **NOTE:** Intel 852GME/852PM: ECC error detection is not supported by the SDQ[71:64] signals if AGP interface is enabled
RCVENOUT#	O SSTL_2	**Reserved**: No connect.
RCVENIN#	O SSTL_2	**Reserved**: No connect.

2.3 AGP Interface Signals

Unless otherwise specified, the voltage level for all signals in this interface is 1.5 volts.

2.3.1 AGP Addressing Signals

Table 5. AGP Addressing Signal Descriptions

Signal Name	Type	Description
GPIPE#	I AGP	**Pipelined Read:** This signal is asserted by the AGP master to indicate a full width address is to be enqueued on by the target using the **AD** bus. One address is placed in the AGP request queue on each rising clock edge while **PIPE#** is asserted. When **PIPE#** is deasserted no new requests are queued across the AD bus. **During SBA Operation:** This signal is **not used** if SBA (Side Band Addressing) is selected. **During FRAME# Operation:** This signal is **not used** during AGP FRAME# operation. **PIPE#** is a sustained tri-state signal from masters (graphics controller), and is an input to the GMCH/MCH.
GSBA[7:0]	I AGP	**Side-band Address:** These signals are used by the AGP master (graphics controller) to pass address and command to the GMCH/MCH. The **SBA** bus and AD bus operate independently. That is, transactions can proceed on the **SBA** bus and the AD bus simultaneously. **During PIPE# Operation:** These signals are **not used** during PIPE# operation. **During FRAME# Operation:** These signals are **not used** during AGP FRAME# operation. **NOTE:** When sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).

The AGP interface contains two mechanisms to queue requests by the AGP master. Note that the master can only use one mechanism. The master may not switch methods without a full reset of the system. When PIPE# is used to queue addresses the master is not allowed to queue addresses using the SBA bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master will continue to use the mechanism selected until the master is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism, but rather a static decision when the device is first being configured after reset.

2.3.2 AGP Flow Control Signals

Table 6. AGP Flow Control Signals

Signal Name	Type	Description
GRBF#	I AGP	**Read Buffer Full:** Read buffer full indicates if the master is ready to accept previously requested low priority read data. When **RBF#** is asserted the GMCH/MCH is not allowed to initiate the return low priority read data. That is, the GMCH/MCH can finish returning the data for the request currently being serviced. **RBF#** is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.
GWBF#	I AGP	**Write-Buffer Full:** indicates if the master is ready to accept Fast Write data from the GMCH/MCH. When **WBF#** is asserted the GMCH/MCH is not allowed to drive Fast Write data to the AGP master. **WBF#** is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.

2.3.3 AGP Status Signals

Table 7. AGP Status Signal Descriptions

Signal Name	Type	Description	
GST[2:0]	O AGP	**Status:** Provides information from the arbiter to an AGP Master on what it may do. **ST[2:0]** only have meaning to the master when its **GNT#** is asserted. When **GNT#** is deasserted these signals have no meaning and must be ignored.	
		ST[2:0]	**Meaning**
		000	Previously requested low priority read data is being returned to the master
		001	Previously requested high priority read data is being returned to the master
		010	The master is to provide low priority write data for a previously queued write command
		011	The master is to provide high priority write data for a previously queued write command.
		100	Reserved
		101	Reserved
		110	Reserved
		111	The master has been given permission to start a bus transaction. The master may queue AGP requests by asserting **PIPE#** or start a PCI transaction by asserting FRAME#.

2.3.4 AGP Strobes

Table 8. AGP Strobe Descriptions

Signal Name	Type	Description
GADSTB[0]	I/O AGP	**Address/Data Bus Strobe-0:** provides timing for 2x and 4x data on **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
GADSTB#[0]	I/O AGP	**Address/Data Bus Strobe-0 Complement:** With AD STB0, forms a differential strobe pair that provides timing information for the **AD[15:0]** and **C/BE[1:0]#** signals in 4x mode. The agent that is providing the data will drive this signal.
GADSTB[1]	I/O AGP	**Address/Data Bus Strobe-1:** Provides timing for 2x and 4x data on **AD[31:16]** and **C/BE[3:2]#** signals. The agent that is providing the data will drive this signal.
GADSTB#[1]	I/O AGP	**Address/Data Bus Strobe-1 Complement:** With AD STB1, forms a differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]# signals in 4X mode. The agent that is providing the data will drive this signal.
GSBSTB	I AGP	**Sideband Strobe:** Provides timing for 2x and 4x data on the **SBA[7:0]** bus. It is driven by the AGP master after the system has been configured for 2x or 4x sideband address mode.
GSBSTB#	I AGP	**Sideband Strobe Complement:** The differential complement to the **SB_STB** signal. It is used to provide timing 4x mode.

2.3.5 AGP/PCI Signals-Semantics

For transactions on the AGP interface carried using AGP FRAME# protocol these signals operate similarly to their semantics in the PCI 2.1 specification, as defined below.

Table 9. AGP/PCI Signals-Semantics Descriptions

Signal Name	Type	Description
GFRAME#	I/O AGP	**G_FRAME:** Frame. **During PIPE# and SBA Operation:** Not used by AGP SBA and PIPE# operations. **During Fast Write Operation:** Used to frame transactions as an output during Fast Writes. **During FRAME# Operation:** G_FRAME# is an output when the GMCH/MCH acts as an initiator on the AGP Interface. G_FRAME# is asserted by the GMCH/MCH to indicate the beginning and duration of an access. G_FRAME# is an input when the GMCH/MCH acts as a FRAME#-based AGP target. As a FRAME#-based AGP target, the GMCH/MCH latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which GMCH/MCH samples FRAME# active.
GIRDY#	I/O AGP	**G_IRDY#:** Initiator Ready. **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_IRDY# is an output when GMCH/MCH acts as a FRAME#-based AGP initiator and an input when the GMCH acts as a FRAME#-based AGP target. The assertion of G_IRDY# indicates the current FRAME#-based AGP bus initiator's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_IRDY# indicates that the AGP-compliant master is ready to provide all write data for the current transaction. Once G_IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The master is never allowed to insert a wait state during the initial data transfer (32 bytes) of a write transaction. However, it may insert wait states after each 32-byte block is transferred.
GTRDY#	I/O AGP	**G_TRDY#:** Target Ready. **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_TRDY# is an input when the GMCH/MCH acts as an AGP initiator and is an output when the GMCH/MCH acts as a FRAME#-based AGP target. The assertion of G_TRDY# indicates the target's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_TRDY# indicates the AGP-compliant target is ready to receive write data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on write transactions.

Signal Name	Type	Description
GSTOP#	I/O AGP	**G_STOP#:** Stop. **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_STOP# is an input when the GMCH/MCH acts as a FRAME#-based AGP initiator and is an output when the GMCH/MCH acts as a FRAME#-based AGP target. G_STOP# is used for disconnect, retry, and abort sequences on the AGP interface.
GDEVSEL#	I/O AGP	**G_ DEVSEL#: Device Select.** **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_DEVSEL#, when asserted, indicates that a FRAME#-based AGP target device has decoded its address as the target of the current access. The GMCH/MCH asserts G_DEVSEL# based on the DDR SDRAM address range being accessed by a PCI initiator. As an input, G_DEVSEL# indicates whether the AGP master has recognized a PCI cycle to it.
GREQ#	I AGP	**G_REQ#:** Request. **During SBA Operation:** This signal is not used during SBA operation. **During PIPE# and FRAME# Operation:** G_REQ#, when asserted, indicates that the AGP master is requesting use of the AGP interface to run a FRAME#- or PIPE#-based operation.
GGNT#	O AGP	**G_GNT#: Grant.** **During SBA, PIPE# and FRAME# Operation:** G_GNT#, along with the information on the ST[2:0] signals (status bus), indicates how the AGP interface will be used next. Refer to the *AGP Interface Specification, Revision 2.0* for further explanation of the ST[2:0] values and their meanings.
GAD[31:0]	I/O AGP	**G_AD[31:0]: Address/Data Bus.** **During PIPE# and FRAME# Operation:** The G_AD[31:0] signals are used to transfer both address and data information on the AGP interface. **During SBA Operation:** The G_AD[31:0] signals are used to transfer data on the AGP interface.
GCBE#[3:0]	I/O AGP	**Command/Byte Enable.** **During FRAME# Operation:** During the address phase of a transaction, the G_CBE[3:0]# signals define the bus command. During the data phase, the G_CBE[3:0]# signals are used as byte enables. The byte enables determine which byte lanes carry meaningful data. The commands issued on the G_CBE# signals during FRAME#-based AGP transactions are the same G_CBE# command described in the PCI 2.2 specification. **During PIPE# Operation:** When an address is enqueued using PIPE#, the C/BE# signals carry command information. Refer to the *AGP 2.0 Interface Specification, Revision 2.0* for the definition of these commands. The command encoding used during PIPE#-based AGP is *different* than the command encoding used during FRAME#-based AGP cycles (or standard PCI cycles on a PCI bus). **During SBA Operation:** These signals are not used during SBA operation.

Signal Name	Type	Description
GPAR	I/O AGP	**Parity.** **During FRAME# Operation:** G_PAR is driven by the GMCH/MCH when it acts as a FRAME#-based AGP initiator during address and data phases for a write cycle, and during the address phase for a read cycle. G_PAR is driven by the GMCH/MCH when it acts as a FRAME#-based AGP target during each data phase of a FRAME#-based AGP memory read cycle. Even parity is generated across G_AD[31:0] and G_CBE[3:0]#. **During SBA and PIPE# Operation:** This signal is not used during SBA and PIPE# operation.

PCIRST# from the ICH4-M is assumed to be connected to RSTIN# and is used to reset AGP interface logic within the GMCH/MCH. The AGP agent will also typically use PCIRST# provided by the ICH4-M as an input to reset its internal logic.

2.4 Hub Interface Signals

Table 10. Hub Interface Signals

Signal Name	Type	Description
HL[10:0]	I/O	**Packet Data:** Data signals used for HI read and write operations
HLSTB	I/O	**Packet Strobe:** One of two differential strobe signals used to transmit or receive packet data over HI.
HLSTB#	I/O	**Packet Strobe Complement**: One of two differential strobe signals used to transmit or receive packet data over HI.

2.5 Clocks

Table 11. Clock Signals

Signal Name	Type	Description
Host Processor Clocking		
BCLK **BCLK#**	I CMOS	**Differential Host Clock In:** These pins receive a buffered host clock from the external clock synthesizer. This clock is used by all of the GMCH/MCH logic that is in the Host clock domain (host, hub and system memory). The clock is also the reference clock for the graphics core PLL. This is a low voltage differential input.
System Memory Clocking		
SCK[5:0]	O SSTL_2	**Differential DDR SDRAM Clock:** SCK and SCK# pairs are differential clock outputs. The crossing of the positive edge of SCK and the negative edge of SCK# is used to sample the address and control signals on the DDR SDRAM. There are 3 pairs to each SO-DIMM. **NOTE:** Intel 852GME ECC error detection is supported by the SCK[2] and SCK[5] signals.
SCK[5:0]#	O SSTL_2	**Complementary Differential DDR SDRAM Clock:** These are the complimentary differential DDR SDRAM clock signals. **NOTE:** Intel 852GME/852PM: ECC error detection is supported by the SCK[2]# and SCK[5]# signals.
DVO/Hub Input Clocking		
GCLKIN	I CMOS	**Input Clock:** 66-MHz, 3.3-V input clock from external buffer DVO/hub interface.
DVO Clocking		
DVOBCLK **DVOBCLK#**	O DVO	**Differential DVO Clock Output:** These pins provide a differential pair reference clock that can run up to 165 MHz. DVOBCLK corresponds to the primary clock out. DVOBCLK# corresponds to the primary complementary clock out.
DVOCCLK **DVOCCLK#**	O DVO	**Differential DVO Clock Output**: These pins provide a differential pair reference clock that can run up to 165 MHz. DVOCCLK corresponds to the primary clock out. DVOCCLK# corresponds to the primary complementary clock out.

DVOBCCLKINT	I DVO	**DVOBC Pixel Clock Input/Interrupt:** This input can be programmed to be either a TV reference clock input from a TV encoder or an Interrupt input pin for LFP display Hot Plug support. DVOBC Pixel Clock Input: This signal may be configured as the reference clock input from a TV-OUT device. The maximum input frequency for this signal is 85 MHz. DVOBC Interrupt: This signal may be configured as an interrupt input for Hot plug support. DVOBCCLKINT needs to be pulled down if the signal is NOT used.
DPMS	I DVO	**Display Power Management Signaling:** This signal is used only in mobile systems to act as the DREFCLK in certain power management states (i.e. Display Power Down Mode); DPMS Clock is used to refresh video during S1-M. Clock Chip is powered down in S1-M. DPMS should come from a clock source that runs during S1-M and needs to be 1.5 V. So, an example would be to use a 1.5-V version of SUSCLK from ICH4-M.
DAC Clocking		
DREFCLK	I LVTTL	**Display Clock Input:** This pin is used to provide a 48-MHz input clock to the Display PLL that is used for 2D/Video and DAC.
LVDS LCD Flat Panel Clocking		
DREFSSCLK	I LVTTL	**Display SSC Clock Input:** This pin provides a 48-MHz or 66-MHz input clock (SSC or non-SSC) to the Display PLL B.

2.6 GMCH Internal Graphics Display Signals

The Intel 852GME internal graphics device has support for four display ports: a dedicated LVDS panel interface, two DVO ports, and an analog VGA port.

2.6.1 Dedicated LVDS Panel Interface

Table 12. Dedicated LVDS Panel Interface Signal Descriptions

Name	Type	Voltage	Description
ICLKAP	O LVDS	1.25 V± 225 mV	**Channel A differential clock pair output (true):** 245-800 MHz
ICLKAM	O LVDS	1.25 V±225 mV	**Channel A differential clock pair output (compliment):** 245-800 MHz.
IYAP[3:0]	O LVDS	1.25 V±225 mV	**Channel A differential data pair 3:0 output (true):** 245-800 MHz.
IYAM[3:0]	O LVDS	1.25 V±225 mV	**Channel A differential data pair 3:0 output (compliment):** 245-800 MHz.
ICLKBP	O LVDS	1.25 V±225 mV	**Channel B differential clock pair output (true):** 245-800 MHz.
ICLKBM	O LVDS	1.25 V±225 mV	**Channel B differential clock pair output (compliment):** 245-800 MHz.
IYBP[3:0]	O LVDS	1.25 V±225 mV	**Channel B differential data pair 3:0 output (true):** 245-800 MHz.
IYBM[3:0]	O LVDS	1.25 V± 225 mV	**Channel B differential data pair 3:0 output (compliment):** 245-800 MHz.

2.6.2 Digital Video Port B (DVOB)

Table 13. Digital Video Port B Signal Descriptions

Signal Name	Type	Description
DVOBD[11:0]	O DVO	**DVOB Data:** This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOBCLK and DVOBCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the lower 12-bits of pixel data. DVOBD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOBHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOB interface. DVOBHSYNC should be left as left as NC (“Not Connected”) if not used.
DVOBVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOB interface. DVOBVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOBBLANK#	O DVO	**Flicker Blank or Border Period Indication: DVOBBLANK# is** a programmable output pin driven by the GMCH/MCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOBBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOBFLDSTL	I DVO	**TV Field and Flat Panel Stall Signal**. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOB TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOB Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOBFLDSTL needs to be pulled down if not used.

2.6.3 Digital Video Port C (DVOC)

Table 14. Digital Video Port C Signal Descriptions

Signal Name	Type	Description
DVOCD[11:0]	O DVO	**DVOC Data**: This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOCCLK and DVOCCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the upper 12-bits of pixel data. DVOCD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOCHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOC interface. DVOCHSYNC should be left as left as NC (“Not Connected”) if not used.
DVOCVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOC interface. DVOCVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOCBLANK#	O DVO	**Flicker Blank or Border Period Indication**: **DVOCBLANK#** is a programmable output pin driven by the GMCH/MCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOCBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOCFLDSTL	I DVO	**TV Field and Flat Panel Stall Signal**. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. **DVOC TV Field Signal**: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. **DVOC Flat Panel Stall Signal**: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOCFLDSTL needs to be pulled down if not used.

Table 15. DVOB and DVOC Port Common Signal Descriptions

Signal Name	Type	Description
DVOBCINTR#	I DVO	**DVOBC Interrupt**: This pin is used to signal an interrupt, typically used to indicate a hot plug or unplug of a digital display.
ADDID[7:0]	I DVO	**ADDID[7:0]**: These pins are used to communicate to the video BIOS when an external device is interfaced to the DVO port. **NOTE**: Bit[7] needs to be strapped low when an on-board DVO device is present. The other pins should be left as NC.
Signal Name	**Type**	**Description**
DVODETECT	I DVO	**DVODETECT**: This strapping signal indicates to the GMCH/MCH whether a DVO device is present or not. When a DVO device is connected, then DVODETECT = 0.

2.6.4 GMCH DVO & I2C to AGP Pin Mapping

The GMCH will mux a DVODETECT signal with the GPAR signal on the AGP bus. This signal will act as a strap and indicate whether the interface is in AGP or DVO mode. The GMCH/MCH has an internal pull-down on DVODETECT signal that will by default pull it low. For an AGP graphics device, pin should be pulled up high and the AGP/DVO Mux select bit in the SHIC (Device 0, function 0, offset 74h bit 1) register will be set to AGP mode (AGP/DVO Mux Strap = 1). Boards that use only Integrated Graphics should leave DVODETECT NC (No Connect). If board has digital display devices connected to the AGP/DVO interface, SBA [7:0] will act as straps for an ADDID.

Table 16. Intel 852GME GMCH AGP/DVO Pin Muxing

DVO MODE	AGP MODE	DVO MODE	AGP MODE	DVO MODE	AGP MODE
DVOBD[0]	GAD[3]	DVOCD[0]	GAD[19]	MI2CCLK	GIRDY#
DVOBD[1]	GAD[2]	DVOCD[1]	GAD[20]	MI2CDATA	GDEVSEL#
DVOBD[2]	GAD[5]	DVOCD[2]	GAD[21]	MDVICLK	GTRDY#
DVOBD[3]	GAD[4]	DVOCD[3]	GAD[22]	MDVIDATA	GFRAME#
DVOBD[4]	GAD[7]	DVOCD[4]	GAD[23]	MDDCCDATA	GAD[15]
DVOBD[5]	GAD[6]	DVOCD[5]	GCBE#[3]	MDDCCLK	GSTOP#
DVOBD[6]	GAD[8]	DVOCD[6]	GAD[25]	DVOBCINT#	GAD[30]
DVOBD[7]	GCBE#[0]	DVOCD[7]	GAD[24]	DVOBCCLKINT	GAD[13]
DVOBD[8]	GAD[10]	DVOCD[8]	GAD[27]	ADDID[7]	GSBA[7]
DVOBD[9]	GAD[9]	DVOCD[9]	GAD[26]	ADDID[6]	GSBA[6]
DVOBD[10]	GAD[12]	DVOCD[10]	GAD[29]	ADDID[5]	GSBA[5]
DVOBD[11]	GAD[11]	DVOCD[11]	GAD[28]	ADDID[4]	GSBA[4]
DVOBCLK	GADSTB[0]	DVOCCLK	GADSTB[1]	ADDID[3]	GSBA[3]
DVOBCLK#	GADSTB#[0]	DVOCCLK#	GADSTB#[1]	ADDID[2]	GSBA[2]
DVOBHSYNC	GAD[0]	DVOCHSYNC	GAD[17]	ADDID[1]	GSBA[1]
DVOBVSYNC	GAD[1]	DVOCVSYNC	GAD[16]	ADDID[0]	GSBA[0]
DVOBBLANK#	GCBE#[1]	DVOCBLANK#	GAD[18]	DVODETECT	GPAR
DVOBFLDSTL	GAD[14]	DVOCFLDSTL	GAD[31]	DPMS	GPIPE#

2.6.5 Analog Display

Table 17. Analog Display Signal Descriptions

Signal Name	Type	Description
VSYNC	O CMOS	**CRT Vertical Synchronization**: This signal is used as the vertical sync signal.
HSYNC	O CMOS	**CRT Horizontal Synchronization**: This signal is used as the horizontal sync signal.
RED	O Analog	**Red (Analog Video Output)**: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-Ω equivalent load on each pin (e.g., 75-Ω resistor on the board, in parallel with the 75-Ω CRT load).
RED#	O Analog	**Red# (Analog Output):** Tied to ground.
GREEN	O Analog	**Green (Analog Video Output)**: This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5-Ω equivalent load on each pin (e.g., 75-Ω resistor on the board, in parallel with the 75-Ω CRT load).
GREEN#	O Analog	**Green# (Analog Output):** Tied to ground.
BLUE	O Analog	**Blue (Analog Video Output)**: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-Ω equivalent load on each pin (e.g., 75-ohm resistor on the board, in parallel with the 75-Ω CRT load).
BLUE#	O Analog	**Blue# (Analog Output):** Tied to ground.

2.6.6 Graphics General Purpose Input/Output Signals

Table 18. Graphics GPIO Signal Descriptions

GPIO I/F Total	Type	Comments
AGPBUSY#	O CMOS	**AGPBUSY:** Output of the GMCH IGD to the ICH4-M, which indicates that certain graphics activity is taking place. It will indicate to the ACPI software not to enter the C3 state. It will also cause a C3/C4 exit if C3/C4 was being entered, or was already entered when AGPBUSY# went active. Not active when the IGD is in any ACPI state other than D0.
EXTTS_0	I CMOS	**External Thermal Sensor Input:** This signal is an active low input to the GMCH/MCH and is used to monitor the thermal condition around the system memory and is used for triggering a read throttle. The GMCH/MCH can be optionally programmed to send a SERR, SCI, or SMI message to the ICH4-M upon the triggering of this signal.
Panel Power Sequencing Control Signals		
PANELVDDEN	O CMOS	**LVDS LCD Flat Panel Power Control:** This signal is used to enable the power to the panel interface.
PANELBKLTEN	O CMOS	**LVDS LCD Flat Panel Backlight Enable:** This signal is used to enable the backlight inverter (BLI).
PANELBKLTCTL	O CMOS	**LVDS LCD Flat Panel Backlight Brightness Control:** This signal is used as the Pulse Width Modulated (PWM) control signal to inverter for control the of backlight brightness.
GPIO pins for DDC/GMBUS support		
LCLKCTLA	O CMOS	**SSC Chip Clock Control:** Can be used to control an external clock chip with SSC control. If external SSC chip not used, may optionally use for DDC/GMBUS support.
LCLKCTLB	O CMOS	**SSC Chip Data Control:** Can be used to control an external clock chip for SSC control. If external SSC chip not used, may optionally use for DDC/GMBUS support.
DDCACLK	I/O CMOS	**CRT DDC Clock:** This signal is used as the DDC clock signal between the CRT monitor and the GMCH.
DDCADATA	I/O CMOS	**CRT DDC Data:** This signal is used as the DDC data signal between the CRT monitor and the GMCH.
DDCPCLK	I/O CMOS	**Panel DDC Clock:** This signal is used as the DDC clock signal between the LFP and the GMCH.
DDCPDATA	I/O CMOS	**Panel DDC Data:** This signal is used as the DDC data signal between the LFP and the GMCH.
GPIO pins for DDC/GMBUS support		
MI2CCLK	I/O DVO	**DVO I2C Clock:** This signal is used as the I2C_CLK for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.

GPIO I/F Total	Type	Comments
MI2CDATA	I/O DVO	**DVO I2C Data:** This signal is used as the I2C_DATA for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MDVICLK	I/O DVO	**DVI DDC Clock:** This signal is used as the DDC clock for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDVIDATA	I/O DVO	**DVI DDC Data:** The signal is used as the DDC data for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDDCDATA	I/O DVO	**DVI DDC Clock:** The signal is used as the DDC data for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.
MDDCCLK	I/O DVO	**DVI DDC Data:** The signal is used as the DDC clock for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.

2.7 Power Sequencing Signal Description

GPIO I/F Total	Type	Comments
RSTIN#	I CMOS	**Reset:** Primary Reset, Connected to PCIRST# of ICH4-M.
PWROK	I CMOS	**Power OK**: Indicates that power to GMCH/MCH is stable.

2.8 Voltage References, PLL Power

Table 19. Voltage References, PLL Power

GPIO I/F Total	Type	Comments
Host Processor		
HXRCOMP	Analog	**Host RCOMP:** Used to calibrate the Host AGTL+ I/O buffers.
HYRCOMP	Analog	**Host RCOMP:** Used to calibrate the Host AGTL+ I/O buffers.
HXSWING	Analog	**Host Voltage Swing (RCOMP reference voltage):** These signals provide a reference voltage used by the PSB RCOMP circuit.
HYSWING	Analog	**Host Voltage Swing (RCOMP reference voltage)**: These signals provide a reference voltage used by the PSB RCOMP circuit.
HDVREF[2:0]	Ref Analog	**Host Data (input buffer) VREF**: Reference voltage input for the data signals of the Host AGTL+ interface. Input buffer differential amplifier to determine a high versus low input voltage.
HAVREF	Ref Analog	**Host Address (input buffer) VREF**: Reference voltage input for the address signals of the Host AGTL+ interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
HCCVREF	Ref Analog	**Host Common Clock (Command input buffer) VREF**: Reference voltage input for the common clock signals of the Host AGTL+ Interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
VTTLF	Power	**PSB Power Supply:** VTTLF is the low frequency connection from the board. This signal is the primary connection of power for GMCH.
VTTHF	Power	**PSB Power Supply:** VTTHF is the high frequency supply. It is for direct connection from an internal package plane to a capacitor placed immediately adjacent to the GMCH. **NOTE:** Not to be connected to power rail.
System Memory		
SMRCOMP	Analog	**System Memory RCOMP**: This signal is used to calibrate the memory I/O buffers.
SMVREF_0	Ref Analog	**Memory Reference Voltage (Input buffer VREF)**:Reference voltage input for Memory Interface. Input buffer differential amplifier to determine a high versus low input voltage.
SMVSWINGH	Ref Analog	**RCOMP reference voltage:** This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
SMVSWINGL	Ref Analog	**RCOMP reference voltage**: This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
VCCSM	Power	Power supply for Memory I/O.
VCCQSM	Power	Power supply for system memory clock buffers.

VCCASM	Power	Power supply for system memory logic running at the core voltage (isolated supply, not connected to the core).
Hub Interface		
HLRCOMP	Analog	**Hub Interface RCOMP**: This signal is connected to a reference resistor in order to calibrate the buffers.
PSWING	Analog	**RCOMP reference voltage**: This is connected to the RCOMP buffer differential amplifier and is used to calibrate the buffers.
HLVREF	Ref Analog	**Input buffer VREF**: Input buffer differential amplifier to determine a high versus low input voltage.
VCCHL	Power	Power supply for Hub interface buffers
DVO (Intel 852GME GMCH Only)		
DVORCOMP	Analog Analog	**Compensation for DVO**: This signal is used to calibrate the DVO I/O buffers.
GVREF	Ref Analog	**Input buffer VREF**: Input buffer differential amplifier to determine a high versus low input voltage.
VCCDVO	Power	Power supply for DVO
GPIO		
VCCGPIO	Power	Power supply for GPIO buffers
DAC (Intel 852GME GMCH Only)		
REFSET	Ref Analog	**Resistor Set:** Set point resistor for the internal color palette DAC.
VCCADAC	Power	Power supply for the DAC
VSSADAC	Power	Ground supply for the DAC
LVDS (Intel 852GME GMCH Only)		
LIBG	Analog	LVDS reference current: signal connected to reference resistor.
VCCDLVDS	Power	Digital power supply.
VCCTXLVDS	Power	Data/Clk Tx power supply.
VCCALVDS	Power	Analog power supply.
VSSALVDS	Power	Ground supply for LVDS.
Clocks		
VCCAHPLL	Power	Power supply for the Host PLL.
VCCAGPLL	Power	Power supply for the Hub/DVO PLL.
VCCADPLLA	Power	Power supply for the display PLL A.
VCCADPLLB	Power	Power supply for the display PLL B.
Core		
VCC	Power	Power supply for the core.
VSS	Power	Ground supply for the chip.

2.9 Reset States and Pull-up/Pull-downs

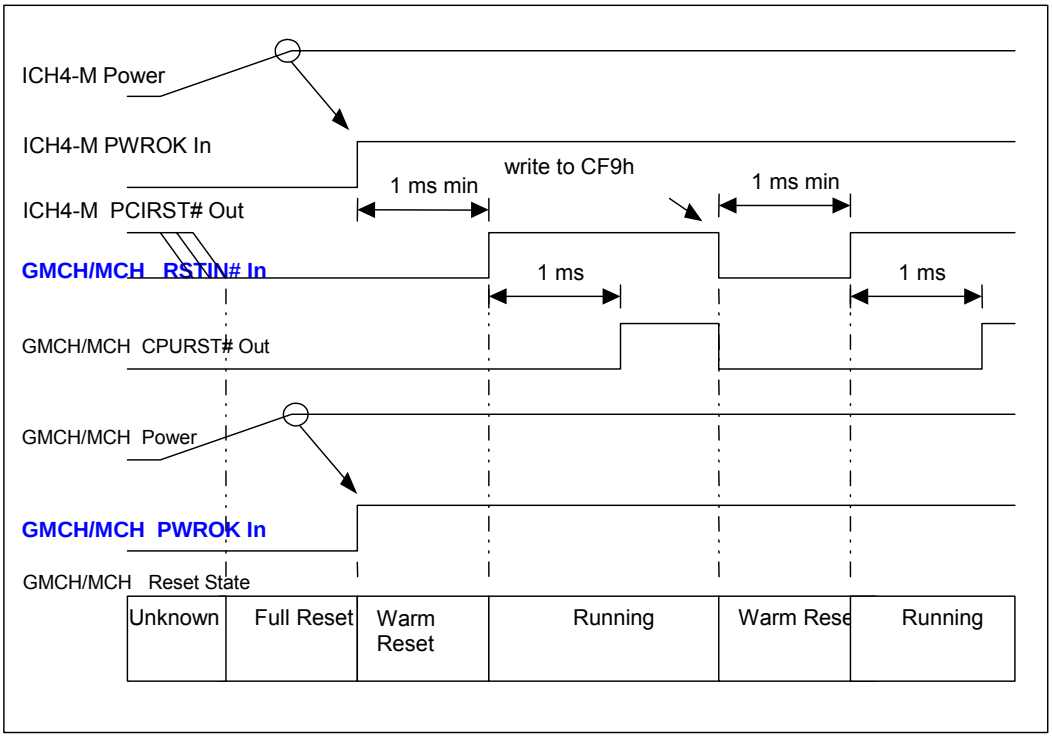
This section describes the expected states of the Intel 852GME GMCH and 852PM MCH I/O buffers. These tables refer only to the contributions on the interface from the GMCH/MCH and do NOT reflect any external influence (such as external pullup/pulldown resistors or external drivers).

Legend:

Z:	Tristate Outputs
Hi:	Pulled High
1:	High
Low:	Pulled Low
0:	Low
Term H/L:	Normal internal termination devices are turned on high/low
Pwrdn:	Power down
Drive H/L:	Strong Drive high/low
Input:	Input Buffer
PU, PD:	Weak internal pull-up, Weak internal pull down
External PU, PD:	Must be externally pulled-up or pulled down
Intern:IG:	Internal GFX
Internal GFX:	Must keep system memory running for display
External GFX:	Can be in self-refresh
Self-refresh:	CKE is not asserted, all other pins can be hi-z
X:	Do not Care

2.9.1 Full and Warm Reset State

Figure 3 . Full and Warm Reset Waveforms



All register bits assume their default values during full reset. PCIRST# resets all internal flops and state machines (except for a few configuration register bits). A full reset occurs when PCIRST# (RSTIN#) and CPURST# are asserted and PWROK is deasserted. This means that all the registers are changed to their default values in the entire system. A warm reset (CPU only reset) occurs when PCIRST# (RSTIN#) is asserted and PWROK is asserted. CPU only reset drives only CPURST# and can be initiated by write of a bit in dedicated register and HALT special cycle. As a result, CPU only registers must be reset. Table 20 describes the reset states.

The PWROK input pin is used to latch the GMCH/MCH strap values upon exiting S3. This imposes a system requirement in that the ICH4-M expects power to be removed (PWROK to go low) when SLP_S3# goes low.

Table 20. Full and Warm Reset Waveforms

Reset State	RSTIN#	PWROK
Full Reset	L	L
Warm Reset	L	H
Doesn't Occur	H	L
Normal Operation	H	H

Table 21. Host Signal Reset and Power Managed States

Host I/F Total	Before CPURST# Deassertion	Just out of CPURST#	C3	S1	S3	S4/S5
ADS#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
BNR#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
BPRI#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
BREQ0#	Low	Term H after 2 clocks	Term H	Term H	Pwrdn	Pwrdn
CPURST#	Low	Term H	Term H	Term H	Pwrdn	Pwrdn
DBSY#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
DEFER#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
DINV[3:0]#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
DPWR#	Low	Low	Term H	Term H	Pwrdn	Pwrdn
DPSLP#	Input	Input	Input	Input	Pwrdn	Pwrdn
DRDY#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
HA[31:3]#	TBD	Term H after 3 clocks	Term H	Term H	Pwrdn	Pwrdn
HADSTB[1:0]#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
HDB_63:0	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
HDSTBNB_3:0	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
HDSTBPB_3:0	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
HIT#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
HITM#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
HLOCK#	Input	Input	Input	Input	Pwrdn	Pwrdn
HREQ[4:0]#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
HTRDY#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn
RS[2:0]#	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn

Table 22. System Memory Signal Reset and Power Managed States

Host I/F Total	Before CPURST# Deassertion	Just out of CPURST#	C3	S1	S3	S4/S5
SDQ[63:0]	Hi-Z	Hi-Z	Intern: IG	Hi-Z	Hi-Z	Pwrdn
SDM[8:0]	Hi-Z	Hi-Z	Intern: IG	Hi-Z	Hi-Z	Pwrdn
SDQS[7:0]	Hi-Z	Hi-Z	Intern: IG	Hi-Z	Hi-Z	Pwrdn
SCK[5:0]	Hi-Z	Hi-Z	If ECC not enabled, ECC clocks are Hi-Z. Intern: Hi-Z if self refresh, else toggling	Hi-Z	Hi-Z	Pwrdn
SCK[5:0]#	Hi-Z	Hi-Z	If ECC not enabled, ECC clocks are Hi-Z. Intern: Hi-Z if self refresh, else toggling	Hi-Z	Hi-Z	Pwrdn
SMA[12:0]	Hi-Z	Hi-Z	Intern: IG	Hi-Z	Hi-Z	Pwrdn
SMAB_5,4,2,1	Hi-Z	Hi-Z	Intern: IG	Hi-Z	Hi-Z	Pwrdn
SBA_1:0	Hi-Z	Hi-Z	Intern: IG	Hi-Z	Hi-Z	Pwrdn
SRAS#	Hi-Z	Hi-Z	Intern: IG	Hi-Z	Hi-Z	Pwrdn
SCAS#	Hi-Z	Hi-Z	Intern: IG	Hi-Z	Hi-Z	Pwrdn
SWE#	Hi-Z	HiZ	Intern: IG	Hi-Z	Hi-Z	Pwrdn
SCS[3:0]#	Hi	Hi	Intern: IG	Hi-Z	Hi-Z	Pwrdn
SCKE[3:0]	Low	Low	Intern: IG	Low	Low	Pwrdn
RCVENIN#	Input	Input	Input	Input	Input	Pwrdn
RCVENOUT#	X	Hi	Intern: IG	Hi	Hi-Z	Pwrdn

Table 23. Hub Interface Signal Reset and Power Managed States

Host I/F Total	Before CPURST# Deassertion	Just out of CPURST#	C3	S1	S3	S4/S5
HL[7:0]	Term L	Term L	Term L	Term L	Pwrdn	Pwrdn
HL[10]	Term L	Term L	Term L	Term L	Pwrdn	Pwrdn
HLSTB	Term L	Term L	Term L	Term L	Pwrdn	Pwrdn
HLSTB#	TermL	Term L	Term L	Term L	Pwrdn	Pwrdn
HL[9]	Input	Input	Input	Input	Pwrdn	Pwrdn
HL[8]	Low	Low	Low	Low	Pwrdn	Pwrdn

Table 24. GMCH DVO Signal Reset and Power Managed States

Host I/F Total	Before CPURST# Deassertion	Just out of CPURST#	C3	S1	S3	S4/S5
DVOCCLK# DVOBCLK#	Hi-Z	Hi-Z	Normal Operation	PD	Pwrdn	Pwrdn
DVOBHSYNC	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBVSYNC	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[1]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[0]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[3]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[2]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[5]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[4]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[6]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[9]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[8]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[11]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBD[10]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBCCLKINT	Input	Input	Normal Operation	Input	Pwrdn	Pwrdn

Host I/F Total	Before CPURST# Deassertion	Just out of CPURST#	C3	S1	S3	S4/S5
DVOBFLDSTL	Input	Input	Normal Operation	Input	Pwrdn	Pwrdn
MDDCDATA	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Pwrdn	Pwrdn
DVOCVSYNC	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCHSYNC	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCBLANK#	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[0]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[1]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[2]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[3]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[4]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[7]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[6]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[8]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[11]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[10]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBCINTR#	Input	Input	Normal Operation	External PU	Pwrdn	Pwrdn

Host I/F Total	Before CPURST# Deassertion	Just out of CPURST#	C3	S1	S3	S4/S5
DVOCFLDSTL	Input	Input	Normal Operation	Input	Pwrdn	Pwrdn
DVOBD[7]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOBBLANK#	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
DVOCD[5]	Hi-Z	Hi-Z	Normal Operation	Hi-Z if port not enabled	Pwrdn	Pwrdn
MI2CDATA	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Pwrdn	Pwrdn
MDVIDATA	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Pwrdn	Pwrdn
MI2CCLK	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Pwrdn	Pwrdn
MDDCCLK	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Pwrdn	Pwrdn
MDVICLK	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Hi-Z External PU	Pwrdn	Pwrdn
DPMS	Input	Input	Input	Clocking	Pwrdn	Pwrdn

Table 25. GMCH GPIO Signal Reset and Power Managed States

Host I/F Total	Before CPURST# Deassertion	Just out of CPURST#	C3	S1	S3	S4/S5
RSTIN#	Hi	Hi	Hi	Hi	Pwrdn	Pwrdn
PWROK	Hi	Hi	Hi	Hi	Pwrdn	Pwrdn
HSYNC	Low	Low	If analog display enabled, Normal Operation	See ADPA Register	Pwrdn	Pwrdn
VSYNC	Low	Low	If analog display enabled, Normal Operation	See ADPA Register	Pwrdn	Pwrdn
AGPBUSY#	External PU	External PU	See C3 Operation	External PU	Pwrdn	Pwrdn
EXTTS_0	External PU	External PU	External PU	External PU	Pwrdn	Pwrdn
LCLKCTLA	PU	PU	Normal Operation	Normal Operation	Pwrdn	Pwrdn
LCLKCTLB	PU	PU	Normal Operation	Normal Operation	Pwrdn	Pwrdn
PANELVDDEN	Hi-Z	Hi-Z	Normal Operation	Low	Pwrdn	Pwrdn
PANELBKLTEN	Hi-Z	Hi-Z	Normal Operation	Low	Pwrdn	Pwrdn
PANELBKLTCTL	Hi-Z	Hi-Z	Normal Operation	Hi-Z	Pwrdn	Pwrdn
DDCACLK	Hi	Hi	Hi	Hi	Pwrdn	Pwrdn
DDCADATA	Hi	Hi	Hi	Hi	Pwrdn	Pwrdn
DDCPCLK	Hi	Hi	Hi	Hi	Pwrdn	Pwrdn
DDCPDATA	Hi	Hi	Hi	Hi	Pwrdn	Pwrdn

Table 26. GMCH LVDS Signal Reset and Power Managed States

Host I/F Total	Before CPURST# Deassertion	Just out of CPURST#	C3	S1	S3	S4/S5
IYAP[3:0]	Drive-VSS	Drive-VSS	Normal Operation	Drive-VSS/ Hi-Z	Drive-VSS/ Hi-Z	Pwrdn
IYAM[3:0]	Drive-VSS	Drive-VSS	Normal Operation	Drive-VSS/ Hi-Z	Drive-VSS/ Hi-Z	Pwrdn
ICLKAP	Drive-VSS	DriveVSS	Normal Operation	Drive-VSS/ Hi-Z	Drive-VSS/ Hi-Z	Pwrdn
ICLKAM	Drive-VSS	Drive-VSS	Normal Operation	Drive-VSS/ Hi-Z	Drive-VSS/ Hi-Z	Pwrdn
IYBP[3:0]	Drive-VSS	Drive-VSS	Normal Operation	Drive-VSS/ Hi-Z	Drive-VSS/ Hi-Z	Pwrdn
IYBM[3:0]	Drive-VSS	Drive-VSS	Normal Operation	Drive-VSS/ Hi-Z	Drive-VSS/ Hi-Z	Pwrdn
ICLKBP	Drive-VSS	Drive-VSS	Normal Operation	Drive-VSS/ Hi-Z	Drive-VSS/ Hi-Z	Pwrdn
ICLKBM	Drive-VSS	Drive-VSS	Normal Operation	Drive-VSS/ Hi-Z	Drive-VSS/ Hi-Z	Pwrdn

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3 Register Description

3.1 Conceptual Overview of the Platform Configuration Structure

The Intel 852GME GMCH, Intel 852PM MCH and ICH4-M are physically connected by hub interface. From a configuration standpoint, the hub interface is logically PCI bus #0. As a result, all devices internal to the GMCH/MCH and ICH4-M appear to be on PCI bus #0. The system's primary PCI expansion bus is physically attached to the ICH4-M and from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. Note that the primary PCI bus is referred to as PCI_A in this document and is not PCI bus #0 from a configuration standpoint. The AGP appears to system software to be real PCI bus behind PCI-to-PCI bridges resident as devices on PCI bus #0.

The GMCH/MCH contains two PCI devices within a single physical component. The configuration registers for the three devices are mapped as devices residing on PCI bus #0.

Device #0: Host-Hub Interface Bridge/DDR SDRAM Controller. Logically this appears as a PCI device residing on PCI bus #0. Physically, Device #0 contains the standard PCI registers, DDR SDRAM registers, the Graphics Aperture Controller registers, Hub Interface Control registers and other GMCH/MCH specific registers. Device #0 is divided into the following functions:

Function #0: Host Bridge Legacy registers including Graphics Aperture Control registers, Hub Interface Configuration registers and Interrupt Control registers

Function #1: DDR SDRAM Interface Registers

Function #3: Intel Configuration Process Registers

Device #1: Host-AGP Bridge. Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI bus #0. Physically Device #1 contains the standard PCI-to-PCI bridge registers and the standard AGP/PCI configuration registers (including the AGP I/O and memory address mapping).

Device #2: Integrated Graphics Controller. Logically this appears as a PCI device residing on PCI bus #0. Physically Device #2 contains the Configuration registers for 2D, 3D, and display functions. Table 27 shows the Device # assignment for the various internal GMCH/MCH devices.

Table 27. Device Number Assignment

GMCH/MCH Function	Bus #0, Device#
Host-Hub Interface, DDR SDRAM I/F, Legacy control	Device #0 (Intel 852GME GMCH and Intel 852PM MCH)
Host-to-AGP Bridge(Virtual PCI-to-PCI)	Device #1 (Intel 852GME GMCH and Intel 852PM MCH)
Integrated Graphics Controller (IGD)	Device #2 (Intel 852GME GMCH)

3.2 Nomenclature for Access Attributes

Table 28 provides the nomenclature for the access attributes.

Table 28. Assignment Nomenclature for Access Attributes

RO	**Read Only**. If a register is Read Only, Writes to this register have no effect.
R/W	**Read/Write**. A register with this attribute can be Read and Written.
R/W/L	**Read/Write/Lock**. A register with this attribute can be Read, Written, and Locked.
R/WC	**Read/Write Clear**. A register bit with this attribute can be Read and Written. However, a Write of a 1 clears (sets to 0) the corresponding bit and a Write of a 0 has no effect.
R/WO	**Read/Write Once**. A register bit with this attribute can be Written to only once after power up. After the first Write, this bit becomes Read Only.
L	**Lock**. A register bit with this attribute becomes Read Only after a Lock bit is set.
Reserved Bits	Some of the GMCH/MCH registers described in this section contain reserved bits, which are labeled "Reserved." Software must deal correctly with fields that are Reserved. On Reads, software must use appropriate masks to extract the defined bits and not rely on Reserved bits being of any particular value. On Writes, software must ensure that the values of Reserved bit positions are preserved. That is, the values of Reserved bit positions must first be Read, Merged with the new values for other bit positions and then Written back. Note the software does not need to perform Read, Merge, and Write operations for the Configuration Address register.
Reserved Registers	In addition to Reserved bits within a register, the GMCH/MCH contains address locations in the configuration space of the Host-Hub Interface Bridge entity that are marked either "Reserved" or "Intel Reserved." The GMCH/MCH responds to accesses to "Reserved" address locations by completing the Host cycle. When a "Reserved" register location is Read, in certain cases, a zero value can be returned ("Reserved" registers can be 8-bit, 16-bit, or 32-bit in size) or a non-zero value can be returned. In certain cases, Writes to "Reserved" registers may have no effect on the GMCH/MCH or may cause system failure. Registers that are marked as "Intel Reserved" must not be modified by system software.
Default Value upon a Reset	Upon Reset, the GMCH/MCH sets its entire internal configuration registers to predetermined default states. Some register values at Reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DDR SDRAM configurations, operating parameters and optional system features that are applicable, and to program the GMCH/MCH registers accordingly.
S	SW Semaphore.

A physical PCI Bus #0 does not exist. The hub interface and the internal devices in the GMCH/MCH and ICH4-M logically constitute PCI Bus #0 to configuration software.

3.3 Standard PCI Bus Configuration Mechanism

The PCI bus defines a slot based “configuration space” that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The PCI Specification defines two bus cycles to access the PCI Configuration Space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the CPU.

Configuration Space is supported by a mapping mechanism implemented within the GMCH/MCH. The PCI 2.2 specification defines two mechanisms to access Configuration Space: Mechanism #1 and Mechanism #2. The GMCH/MCH support only Mechanism #1.

The Configuration Access Mechanism makes use of the CONFIG_ADDRESS register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA register (at I/O address 0CFCh though 0CFFh). To reference a Configuration register a Dword I/O Write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device, and a specific Configuration register of the device function being accessed.

CONFIG_ADDRESS[31] must be a 1 to enable a Configuration cycle. CONFIG_DATA then becomes a window into the four Bytes of Configuration Space specified by the contents of CONFIG_ADDRESS. Any Read or Write to CONFIG_DATA will result in the GMCH translating the CONFIG_ADDRESS into the appropriate Configuration cycle.

The GMCH is responsible for translating and routing the CPU’s I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal GMCH/MCH Configuration registers, hub interface, or AGP_PCI_B.

3.4 Routing Configuration Accesses

The GMCH/MCH support two bus interfaces: the hub and the AGP/PCI interface. PCI Configuration cycles are selectively routed to this interface. The GMCH/MCH is responsible for routing PCI Configuration cycles to the proper interface. PCI configuration cycles to the ICH4-M internal devices, and Primary PCI (including downstream devices) are routed to the ICH4-M via the hub interface.

AGP/PCI_B configuration cycles are routed to AGP. The AGP/PCI_B interface is treated as a separate PCI bus from the configuration point of view. Routing of configuration AGP/PCI_B is controlled via the standard PCI-to-PCI bridge mechanism using information contained within the Primary bus number, the Secondary bus number, and the Subordinate bus number registers of the corresponding PCI-to-PCI bridge device.

3.4.1 PCI Bus #0 Configuration Mechanism

The GMCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0, then the Configuration cycle is targeting a PCI bus #0 device.

The Host-Hub Interface Bridge entity within the GMCH/MCH is hardwired as Device #0 on PCI Bus #0. The Host-AGP/PCI_B Bridge entity within the GMCH/MCH is hardwired as Device #1 on PCI Bus #0.

Configuration cycles to any of the GMCH/MCH's internal devices are confined to the GMCH/MCH and not sent over hub interface. Accesses to disabled GMCH/MCH internal devices will be forwarded over the hub interface as Type 0 Configuration cycles.

3.4.2 Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero, and is less than the value in the Host-AGP/PCI_B device's Secondary bus number register or greater than the value in the Host-AGP/PCI_B device's Subordinate bus number register, the GMCH/MCH will generate a Type 1 Hub interface configuration cycle. A[1:0] of the hub interface request packet for the Type 1 configuration cycle will be "01". This Hub interface configuration cycle will be sent over hub interface.

If the cycle is forwarded to the ICH4-M via hub interface, the ICH4-M compares the non-zero Bus Number with the Secondary bus number and Subordinate bus number registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI, one of the ICH4-M's hub interfaces, or a downstream PCI bus.

3.4.3 AGP/PCI_B Bus Configuration Mechanism

From the chipset configuration perspective, AGP/PCI_B is seen as PCI bus interfaces residing on a Secondary Bus side of the "virtual" PCI-to-PCI bridges referred to as the GMCH/MCH Host-PCI_B/AGP bridge. On the Primary bus side, the "virtual" PCI-to-PCI bridge is attached to PCI Bus #0. Therefore the Primary bus number register is hardwired to "0". The "virtual" PCI-to-PCI bridge entity converts Type #1 PCI Bus Configuration cycles on PCI Bus #0 into Type 0 or Type 1 configuration cycles on the AGP/PCI_B interface. Type 1 configuration cycles on PCI Bus #0 that have a Bus number that matches the Secondary bus number of the GMCH/MCH's "virtual" Host-to-PCI_B/AGP bridge will be translated into Type 0 configuration cycles on the PCI_B/AGP interface. The GMCH/MCH will decode the Device Number field [15:11] and assert the appropriate GAD signal as an IDSEL in accordance with the PCI-to-PCI Bridge Type 0 configuration mechanism.

If the Bus Number is non-zero, greater than the value programmed into the Secondary bus number register, and less than or equal to the value programmed into the Subordinate bus number register, then the configuration cycle is targeting a PCI bus downstream of the targeted interface. The GMCH/MCH will generate a Type 1 PCI configuration cycle on PCI_B/AGP.

To prepare for mapping of the configuration cycles on AGP/PCI_B, the initialization software will go through the following sequence:

1. Scan all devices residing on the PCI Bus #0 using Type 0 configuration accesses.
2. For every device residing at bus #0 which implements PCI-to-PCI bridge functionality, it will configure the secondary bus of the bridge with the appropriate number and scan further down the hierarchy. This process will include the configuration of the "virtual" PCI-to-PCI bridges within the GMCH/MCH used to map the AGP device's address spaces in a software specific manner.

Note: Although initial AGP platform implementations will not support hierarchical buses residing below AGP, this specification still must define this capability in order to support PCI-66 compatibility. Note also that future implementations of the AGP devices may support hierarchical PCI or AGP-like buses coming out of the root AGP device.

3.5 Register Definitions

The GMCH/MCH contains four sets of software accessible registers accessed via the Host CPU I/O Address Space, and they are as follows:

Control registers: I/O Mapped into the CPU I/O Space, which control access to PCI and AGP Configuration Space via Configuration Mechanism #1 in the PCI 2.2 specification.

Internal Configuration registers: residing within the GMCH/MCH, they are partitioned into three logical device register sets ("logical" since they reside within the single physical device).

- The first register set is dedicated to Host-HI Bridge functionality (i.e. DDR SDRAM configuration, other chip-set operating parameters and optional features).
- The second register block is dedicated to Host-AGP/PCI_B Bridge functions (controls AGP/PCI_B interface configurations and operating parameters).
- The third register block is for the integrated graphics functions.

Internal Memory Mapped Configuration registers: reside in the GMCH/MCH Device #0.

Internal Memory Mapped Configuration registers and Legacy VGA registers: reside in the GMCH Device #2 that controls the Integrated Graphics Controller.

The GMCH/MCH internal registers (I/O Mapped and Configuration registers) are accessible by the Host CPU. The registers can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities, with the exception of CONFIG_ADDRESS, which can only be accessed as a Dword. All multi-byte numeric fields use "Little Endian Byte Ordering" (i.e., lower addresses contain the least significant parts of the field).

Reserved Bits

Some of the GMCH/MCH registers described in this section contain Reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are Reserved. On Reads, software must use appropriate Masks to extract the defined bits and not rely on Reserved bits being any particular value. On Writes, software must ensure that the values of Reserved bit positions are preserved. That is, the values of Reserved bit positions must first be Read, Merged with the new values for other bit positions and then Written back.

Note: The software does not need to perform Read, Merge, and Write operations for the Configuration Address register.

Default Value Upon Reset

Upon a Full Reset, the GMCH/MCH set all of its Internal Configuration registers to a predetermined default state. Some register values at Reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the

DDR SDRAM configurations, operating parameters, and optional system features that are applicable and to program the GMCH/MCH registers accordingly.

3.6 I/O Mapped Registers

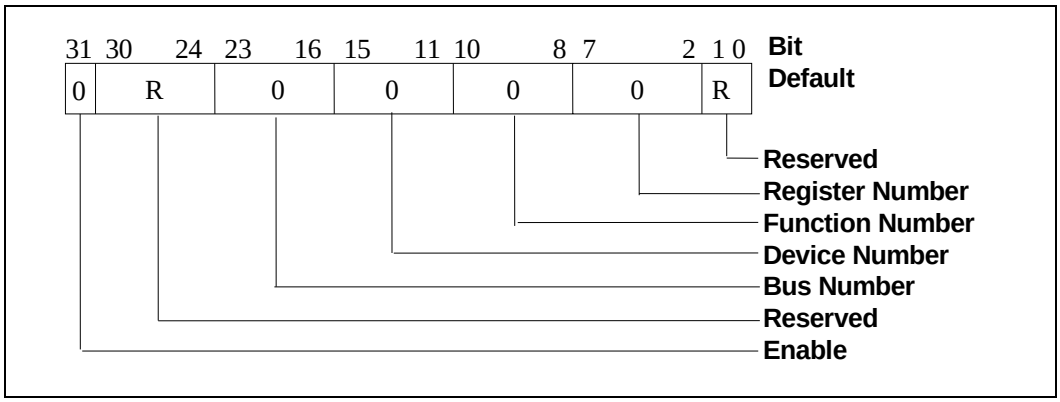
The GMCH/MCH contains two registers that reside in the CPU I/O Address Space: the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the Configuration Space and determines what portion of Configuration Space is visible through the Configuration Data window.

3.6.1 CONFIG_ADDRESS – Configuration Address Register

I/O Address:	0CF8h Accessed as a Dword
Default Value:	00000000h
Access:	Read/Write
Size:	32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a Dword. A Byte or Word reference will “pass through” the Configuration Address register and the hub interface, onto the PCI bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Figure 4. Configuration Address Register



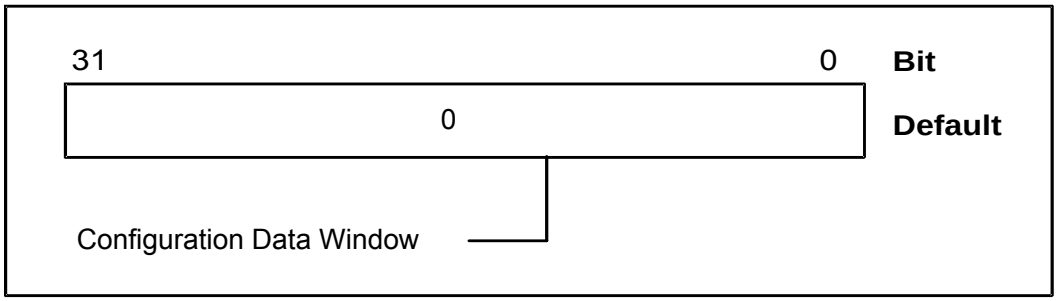
Bit	Description
31	**Configuration Enable (CFGE):** When this bit is set to 1, accesses to PCI Configuration Space are enabled. If this bit is Reset to 0, accesses to PCI Configuration Space are disabled.
30:24	**Reserved**
23:16	**Bus Number:** When the Bus Number is programmed to 00h, the target of the Configuration Cycle is a hub interface agent (GMCH, ICH4-M, etc.). The Configuration Cycle is forwarded to hub interface if the Bus Number is programmed to 00h and the GMCH/MCH is not the target (the device number is >= 2).
15:11	**Device Number:** This field selects one agent on the PCI Bus selected by the Bus Number. When the Bus Number field is 00 the GMCH/MCH decode the Device Number field. The GMCH/MCH is always Device #0 for the Host-hub interface bridge entity. Therefore, when the Bus Number =0 and the Device Number=0-1 the internal GMCH/MCH devices are selected. For Bus Numbers resulting in Hub Interface Configuration cycles, the GMCH/MCH propagates the device number field as A[15:11].
10:8	**Function Number:** This field is mapped to A[10:8] during Hub Interface Configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The GMCH/MCH ignore Configuration cycles to its internal Devices if the function number is not equal to 0.
7:2	**Register Number:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address register. This field is mapped to A[7:2] during Hub Interface Configuration cycles.
1:0	**Reserved**

3.6.2 CONFIG_DATA – Configuration Data Register

I/O Address:	0CFCh
Default Value:	00000000h
Access:	Read/Write
Size:	32 bits

CONFIG_DATA is a 32-bit Read/Write window into Configuration Space. The portion of Configuration Space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Figure 5. Configuration Data Register



Bit	Description
31:0	**Configuration Data Window (CDW).** If bit 31 of CONFIG_ADDRESS is 1, then any I/O access to the CONFIG_DATA register will be mapped to Configuration Space using the contents of CONFIG_ADDRESS.

3.7 Host-Hub Interface Bridge Device Registers (Device #0, Function #0)

Table 29 summarizes the configuration space for Device #0, Function#0.

Table 29. GMCH/MCH Configuration Space - Device #0, Function#0

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	00	01	8086h	RO
Device Identification	DID	02	03	3580h	RO
PCI Command	PCICMD	04	05	0006h	RO,R/W
PCI Status	PCISTS	06	07	0090h	RO,R/WC
Revision Identification	RID	08	08	01h 02h	RO
Sub-Class Code	SUBC	0A	0A	00h	RO
Base Class Code	BCC	0B	0B	06h	RO
Header Type	HDR	0E	0E	80h	RO
Aperture Base Configuration	APBASE	10	13	08h	R/W, RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	40h	RO
Capability Identification	CAPID	40	44	Chipset Dependent	RO
Registers – RCOMP Base Address	RRBAR	48	4B	0000h	R/W, RO
GMCH Misc. Control	GMC	50	51	0000h	R/W
GMCH Graphics Control	GGC	52	53	0030h	R/W
Device and Function Control	DAFC	54	55	0000h	R/W
Fixed Dram Hole Control	FDHC	58	58	00h	R/W
Programmable Attribute Map	PAM (6:0)	59	5F	00h Each	R/W

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
System Management RAM Control	SMRAM	60	60	02h	R/W/L
Extended System Management RAM Control	ESMRAMC	61	61	38h	R/W/L
Error Status	ERRSTS	62	63	0000h	R/WC
Error Command	ERRCMD	64	65	0000h	R/W
SMI Command	SMICMD	66	66	00h	R/W
SCI Command	SCICMD	67	67	00h	R/W
Secondary Host Interface Control Register	SHIC	74	77	00006010h	RO, R/W
AGP Capability Identifier	ACAPID	A0	A3	00200002h	RO
AGP Status Register	AGPSTAT	A4	A7	1F000217h	RO
AGP Command	AGPCMD	A8	AB	0000 0000h	RO, R/W
AGP Control	AGPCTRL	B0	B1	0000h	RO, R/W
AGP Functional	AFT	B2	B3	E9F0h	R/W, R/WC
Aperture Translation Table Base	ATTBASE	B8	BB	00000000h	RO, R/W
AGP Interface Multi Transaction Timer	AMTT	BC	BC	00h	R/W
Low Priority Transaction Timer	LPTT	BD	BD	00h	R/W

3.7.1 VID – Vendor Identification Register (Device #0)

Address Offset: 00-01h
Default Value: 8086h
Access: Read Only
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register, combined with the Device Identification Register, uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification (VID):** This register field contains the PCI standard identification for Intel = 8086h

3.7.2 DID – Device Identification Register (Device #0)

Address Offset: 02-03h
Default Value: 3580h
Access: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number (DID):** This is a 16-bit value assigned to the GMCH/MCH Host-hub interface bridge, Device #0. = 3580h

3.7.3 PCICMD – PCI Command Register (Device #0)

Address Offset: 04-05h
Default Value: 0006h
Access: Read Only, Read/Write
Size: 16 bits

Since GMCH/MCH Device #0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Description
15:10	**Reserved**
9	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back Write. Since Device #0 is strictly a target, this bit is not implemented and is hardwired to 0. Writes to this bit position have no affect.
8	**SERR Enable (SERRE):** This bit is a global enable bit for Device #0 SERR messaging. The GMCH/MCH does not have an SERR# signal, but communicates the SERR# condition by sending an SERR message to the ICH4-M. 1 = Enable. GMCH/MCH is enabled to generate SERR messages over hub interface for specific Device #0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. 0 = SERR message is not generated by the GMCH/MCH for Device #0. **NOTE**: This bit only controls SERR messaging for the Device #0. Device #1 has its own SERRE bit to control error reporting for error conditions occurring on Device #1. The two control bits are used in a logical OR manner to enable the SERR hub interface message mechanism.
7	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the GMCH/MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	**Parity Error Enable (PERRE):** PERR# is not implemented by GMCH/MCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5	**VGA Palette Snoop Enable (VGASNOOP):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	**Memory Write and Invalidate Enable (MWIE):** The GMCH/MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	**Special Cycle Enable (SCE):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	**Bus Master Enable (BME):** The GMCH/MCH is always enabled as a master on hub interface. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	**Memory Access Enable (MAE):** The GMCH/MCH always allows access to main system memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	**I/O Access Enable (IOAE):** This bit is not implemented in the GMCH/MCH and is hardwired to a 0. Writes to this bit position have no effect.

3.7.4 PCI Status Register (Device #0)

Address Offset: 06-07h
Default Value: 0090h
Access: Read Only, Read/WriteClear
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #0's PCI Interface. Bit 14 is Read/Write Clear. All other bits are Read Only. Since GMCH/MCH Device #0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Description
15	**Detected Parity Error (DPE):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	**Signaled System Error (SSE):** R/WC. This bit is set to 1 when GMCH Device #0 generates an SERR message over hub interface for any enabled Device #0 error condition. Device #0 error conditions are enabled in the PCICMD and ERRCMD registers. Device #0 error flags are read/reset from the PCISTS or ERRSTS registers. Software sets SSE to 0 by writing a 1 to this bit.
13	**Received Master Abort Status (RMAS):** R/WC. This bit is set when the GMCH/MCH generates a hub interface request that receives a Master Abort completion packet or Master Abort Special Cycle. Software clears this bit by writing a 1 to it.
12	**Received Target Abort Status (RTAS):** R/WC. This bit is set when the GMCH/MCH generates a hub interface request that receives a Target Abort completion packet or Target Abort Special Cycle. Software clears this bit by writing a 1 to it. If bit 6 in the ERRCMD is set to a one and an Serr# special cycle is generated on the hub interface bus.
11	**Signaled Target Abort Status (STAS):** The GMCH/MCH will not generate a Target Abort hub interface completion packet or Special Cycle. This bit is not implemented in the GMCH/MCH and is hardwired to a 0. Writes to this bit position have no effect.
10:9	**DEVSEL Timing (DEVT):** These bits are hardwired to "00". Writes to these bit positions have no affect. Device #0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that the GMCH/MCH does not limit optimum DEVSEL timing for PCI_A.
8	**Master Data Parity Error Detected (DPD):** PERR signaling and messaging are not implemented by the GMCH/MCH therefore this bit is hardwired to 0. Writes to this bit position have no effect.
7	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device #0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the GMCH/MCH does not limit the optimum setting for PCI_A.
6:5	**Reserved**
4	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h.
3:0	**Reserved**

3.7.5 RID – Revision Identification (Device #0)

Address Offset: 08h
Default Value: 02h
Access: Read Only
Size: 8 bits

This register contains the revision number of the GMCH/MCH Device #0. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH/MCH Device #0. Intel 852GME = 02 Intel 852PM = 02

3.7.6 SUBC – Sub Class Code Register (Device #0)

Address Offset: 0Ah
Default Value: 00h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the GMCH/MCH Device #0. This code is 00h indicating a Host Bridge device.

Bit	Description
7:0	**Sub-Class Code (SUBC):** This is an 8-bit value that indicates the category of Bridge into which the GMCH/MCH falls. The code is 00h indicating a Host Bridge.

3.7.7 BCC – Base Class Code Register (Device #0)

Address Offset: 0Bh
Default Value: 06h
Access: Read Only
Size: 8 bits

This register contains the Base Class code of the GMCH/MCH Device #0. This code is 06h indicating a Bridge device.

Bit	Description
7:0	**Base Class Code (BASEC):** This is an 8-bit value that indicates the Base Class Code for the GMCH/MCH. This code has the value 06h, indicating a Bridge device.

3.7.8 HDR – Header Type Register (Device #0)

Address Offset: 0Eh
Default Value: 80h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Description
7:0	**PCI Header (HDR):** This field always returns 80 to indicate that Device #0 is a multifunction device. If Functions other than 0 are disabled, this field returns a 00 to indicate that the GMCH/MCH is a single function device with standard header layout. Writes to this location have no effect.

3.7.9 APBASE – Aperture Base Configuration (Device #0)

Address Offset: 10h
Default Value: 00000008h
Access: Read Only, Read/Write
Size: 32 bits

The APBASE is a standard PCI Base Address register that is used to set the base of the Graphics Aperture. The standard PCI Configuration mechanism defines the base address configuration register such that only a fixed amount of space can be requested (dependent on which bits are hardwired to "0" or behave as hardwired to "0"). To allow for flexibility (of the aperture), an additional register called APSIZE controls bits of the APBASE that behave as hardwired to "0" to keep the aperture size aligned. This register is programmed by the GMCH/MCH specific BIOS code before any of the generic configuration software runs.

Note: Bit 1 of the register 51h is used to prevent accesses to the aperture range before this register is initialized and the appropriate translation table structure has been established in the main memory.

Bit	Description
31:28	**Upper Programmable Base Address (UPBITS):** Upper Programmable Base Address bits—R/W. These bits are used to locate the range size selected via lower bits 27:25. Default = 0000
27:22	**Lower "Hardwired"/Programmable Base Address bits (LOBITS):** These bits behave as "hardwired" or as a programmable depending on the contents of the APSIZE register as defined below: 27 26 Aperture Size **r/w r/w 64 MB** **r/w 0 128 MB** **0 0 256 MB** **Bits 25:22 = 0, enforcing a minimum aperture size to 64 MB.** If AGP Capability in CAPREG is intact ("0") then: Bits 27:26 are controlled by the bits 5:4 of the APSIZE register in the following manner: If bit APSIZE[5]=0 then APBASE[27]=0 and if APSIZE[5]=1 then APBASE[27]=r/w (read/write).
21:4	**Lower Bits (LOWBITS):** These bits are 0.
3	**Prefetchable (PF):** This bit is 1 to identify the Graphics Aperture range as a prefetchable as per the PCI specification for base address registers. This implies that there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and the GMCH/MCH may merge processor writes into this range without causing errors.
2:1	**Addressing Type (TYPE):** These bits determine addressing type and they are hardwired to 00 to indicate that address range defined by the upper bits of this register can be located anywhere in the 32-bit address space as per the PCI specification for base address registers.
0	**Memory Space Indicator (MSPACE):** This bit is 0 and is used to identify the aperture range as a memory range as per the specification for PCI base address registers.

3.7.10 SVID – Subsystem Vendor Identification Register (Device #0)

Address Offset: 2C-2Dh
Default Value: 0000h
Access: Read/Write Once
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Description
15:0	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes Read Only.

3.7.11 SID – Subsystem Identification Register (Device #0)

Address Offset: 2E-2Fh
Default Value: 0000h
Access: Read/Write Once
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Description
15:0	**Subsystem ID (SUBID):** This field should be programmed during BIOS initialization. After it has been written once, it becomes Read Only.

3.7.12 CAPPTR – Capabilities Pointer Register (Device #0)

Address Offset: 34h
Default Value: 40h
Access: Read Only
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Description
7:0	**Pointer to the offset of the first capability ID register block:** In this case the first capability is the Product-Specific Capability, which is located at offset 40h.

3.7.13 CAPID—Capability Identification Register (Device #0)

Address Offset: 40 – 44h
Default: Chipset Dependent
Access: Read Only
Size 40 bits

The Capability Identification Register uniquely identifies chipset capabilities as defined in the table below. The bits in this register are intended to define a capability ceiling for each feature, not a capability select. The BIOS must read this register to identify the part and comprehend the capabilities specified within when configuring the effected portions of the GMCH/MCH.

The default setting, in most cases, allows the maximum capability. This register is Read Only. Writes to this register have no effect.

Bit	Description
39:37	**Capability ID [2:0]:** 000-001= Reserved 010 = Intel 852GME GMCH 011 = Intel 852PM MCH 100 = Reserved 101 = Intel 852GM GMCH 110 – 111 = Reserved
36:31	**Reserved**
30	Limit System Memory ECC Capability **0 = ECC capability supported.** **1 = ECC capabiltiy not supported.**
29:28	**Reserved**
27:24	**CAPREG Version:** This field has the value 0001b to identify the first revision of the CAPREG definition.
23:16	**Cap_length:** This field has the value 05h indicating the structure length.
15:0	**Reserved**

3.7.14 RRBAR – Register Range Base Address Register (Device #0)

Address Offset: 48–4Bh
Default Value: 00000000h
Access: Read/Write, Read Only
Size: 32 bits

This register requests a 64-kB allocation for the Device registers. The base address is defined by bits 31 to 16 and can be used to access device configuration registers. Only Dword aligned writes are allowed to this space. See Table below for address map within the 64-kB space. This addressing mechanism may be used to write to registers that modify the device address map. However, before using or allowing the use of the modified address map the bios must synchronize using an IO or Read cycle. Bit 8 of the GCC register is used to prevent accesses to this range before the configuration software initializes this register.

Bit	Description
31:16	**Memory Base Address—**R/W. Set by the OS, these bits correspond to address signals [31:16].
15:0	**Reserved**

Address Range		Description
0000h to FFFFh Space	Sub Ranges	
	0000h to 00FFh	**Read/Write (As in Configuration Space):** Maps to 00–FFh of Device #0, Function #0 register space.
	0100h to 01FFh	**Read/Write (As in Configuration Space):** Maps to 00–FFh of Device #0, Function #1 register space.
	0200h to 02FFh	**Reserved**
	0300h to 03FFh	**Read/Write (As in Configuration Space**): Maps to 00–FFh of Device #0, Function #3 register space.
	0400h to 07FFh	**Reserved**
	0800h to 08FFh	**Read/Write (As in Configuration Space):** Maps to 00–FFh of Device #1, Function #0 register space.
	0900h to 0FFFh	**Reserved**
	1000h to 10FFh	**Read/Write (As in Configuration Space)**: Maps to 00–FFh of Device #2, Function #0 register space.
	1100h to 11FFh	**Read/Write (As in Configuration Space):** Maps to 00–FFh of Device #2, Function #1 register space.
	1200h to 7FFFh	**Reserved**
	8000h to 8FFFh	**System memory Rcomp memory Range.**
	9000h to FFFFh	**Reserved**

3.7.15 GMC – GMCH Miscellaneous Control Register (Device #0)

Address Offset: 50–51h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
15:10	**Reserved**
9	**Aperture Access Global Enable—R/W**. This bit is used to prevent access to the aperture from any port (CPU, PCI0 or AGP/PCI1) before the aperture range is established and appropriate translation table in the main DDR SDRAM has been initialized. Default is 0. It must be set after system is fully configured for aperture accesses. **NOTE:** If the AGP_DVO strap is set to DVO then this bit is is RO.
8	**RRBAR Access Enable—R/W:** 1 = Enables the RRBAR space. 0 = Disable
7:1	**Reserved**
0	**MDA Present (MDAP)—R/W:** This bit should not be set when the VGA Enable bit is not set. If the VGA enable bit is set, then accesses to IO address range x3BCh–x3BFh are forwarded to hub interface. If the VGA enable bit is not set then accesses to IO address range x3BCh–x3BFh are treated just like any other IO accesses. MDA resources are defined as the following: Memory: 0B0000h – 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to hub interface even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGA MDA Behavior 0 0 All References to MDA and VGA go to hub interface (Default) 0 1 Reserved 1 0 All References to VGA go to PCI. MDA-only references (I/O address 3BF and aliases) will go to hub interface. 1 1 VGA References go to PCI; MDA References go to hub interface

3.7.16 GGC – GMCH Graphics Control Register (Device 0)

Address Offset: 52–53h
Default Value: 0030h
Access: Read/Write
Size: 16 bits

Bit	Description
15:7	**Reserved**
6:4	**Graphics Mode Select (GMS):** This field is used to select the amount of main system memory that is pre-allocated to support the Internal Graphics Device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that system memory is pre-allocated only when Internal Graphics is enabled. 000 = No system memory pre-allocated. Device #2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device #2 Function #0 Class Code register is 80. 001 = DVMT (UMA) mode, 1 MB of system memory pre-allocated for frame buffer. 010 = DVMT (UMA) mode, 4 MB of system memory pre-allocated for frame buffer. 011 = DVMT (UMA) mode, 8 MB of system memory pre-allocated for frame buffer. 100 = DVMT (UMA) mode, 16 MB of system memory pre-allocated for frame buffer. 101 = DVMT (UMA) mode, 32 MB of system memory pre-allocated for frame buffer. All other combinations reserved.
3:2	**Reserved**
1	**IGD VGA Disable (IVD):** 1 = Disable. Device #2 (IGD) does not claim VGA Memory and I/O Mem cycles, and the Sub-Class Code field within Device #2 Function #0 Class Code register is 80. 0 = Enable. Device #2 (IGD) claims VGA Memory and I/O cycles, the Sub-Class Code within Device #2 Class Code register is 00.
0	**Reserved**

3.7.17 DAFC – Device and Function Control Register (Device 0)

Address Offset: 54–55h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This 16-bit register controls the visibility of devices and functions within the GMCH/MCH to configuration software.

Bit	Description
15:8	**Reserved**
7	**Device #2 Disable:** 1 = Disabled. 0 = Enabled.
6:3	**Reserved**
2	**Device #0 Function #3 Disable:** 1 = Disable Function #3 registers within Device #0 and all associated DDR SDRAM and I/O ranges. 0 = Enable Function #3 within Device #0.
1	**Reserved**
0	**Device #0 Function #1 Disable:** 1 = Disable Function #1 within Device #0. 0 = Enable Function #1 within Device #0.

3.7.18 FDHC – Fixed DRAM Hole Control Register (Device #0)

Address Offset: 58h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This 8-bit register controls a single fixed DDR SDRAM hole: 15–16 MB.

Bit	Description
7	**Hole Enable (HEN):** This field enables a memory hole in DDR SDRAM space. Host cycles matching an enabled hole are passed onto ICH4-M through hub interface. The GMCH/MCH will ignore hub interface cycles matching an enabled hole. **NOTE**: A selected hole is not re-mapped. 0 = None 1 = 15 MB–16 MB (1MBs)
6:0	**Reserved**

3.7.19 PAM(6:0) – Programmable Attribute Map Register (Device #0)

Address Offset: 59–5Fh
Default Value: 00h Each
Attribute: Read/Write
Size: 4 bits/register, 14 registers

The GMCH allows programmable DDR SDRAM attributes on 13 legacy system memory segments of various sizes in the 640 kB –1 MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify system memory attributes for each system memory segment. These bits apply to both Host and hub interface initiator accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE = 1, the CPU Read accesses to the corresponding system memory segment are claimed by the GMCH/MCH and directed to main system memory. Conversely, when RE = 0, the Host Read accesses are directed to PCI0.

WE - Write Enable. When WE = 1, the Host Write accesses to the corresponding system memory segment are claimed by the GMCH/MCH and directed to main system memory. Conversely, when WE = 0, the Host Write accesses are directed to PCI0.

The RE and WE attributes permit a system memory segment to be Read Only, Write Only, Read/Write, or Disabled. For example, if a system memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM register controls two regions, typically 16 kB in size. Each of these regions has a 4-bit field. The 4 bits that control each region have the same encoding and are defined in the following table.

Table 30. Attribute Bit Assignment

Bits [7, 3] Reserved	Bits [6, 2] Reserved	Bits [5, 1] WE	Bits [4, 0] RE	Description
X	X	0	0	**Disabled**. DDR SDRAM is disabled and all accesses are directed to hub interface. The GMCH/MCH does not respond as a hub interface target for any Read or Write access to this area.
X	X	0	1	**Read Only**. Reads are forwarded to DDR SDRAM and Writes are forwarded to hub interface for termination. This Write protects the corresponding DDR SDRAM segment. The GMCH/MCH will respond as a hub interface target for Read accesses but not for any Write accesses.
X	X	1	0	**Write Only**. Writes are forwarded to DDR SDRAM and Reads are forwarded to the hub interface for termination. The GMCH/MCH will respond as a hub interface target for Write accesses but not for any Read accesses.
X	X	1	1	**Read/Write**. This is the normal operating mode of main system memory. Both Read and Write cycles from the host are claimed by the GMCH/MCH and forwarded to DDR SDRAM. The GMCH/MCH will respond as a hub interface target for both Read and Write accesses.

As an example, consider a BIOS that is implemented on the Expansion bus. During the initialization process, the BIOS can be shadowed in main system memory to increase the system performance. When BIOS is shadowed in main system memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to Write Only. The BIOS is shadowed by first doing a Read of that address. This Read is forwarded to the Expansion bus. The Host then does a Write of the same address, which is directed to main system memory. After the BIOS is shadowed, the attributes for that system memory area are set to Read Only so that all Writes are forwarded to the Expansion bus. Figure 6 and Table 36 show the PAM registers and the associated attribute bits.

Figure 6. PAM Registers

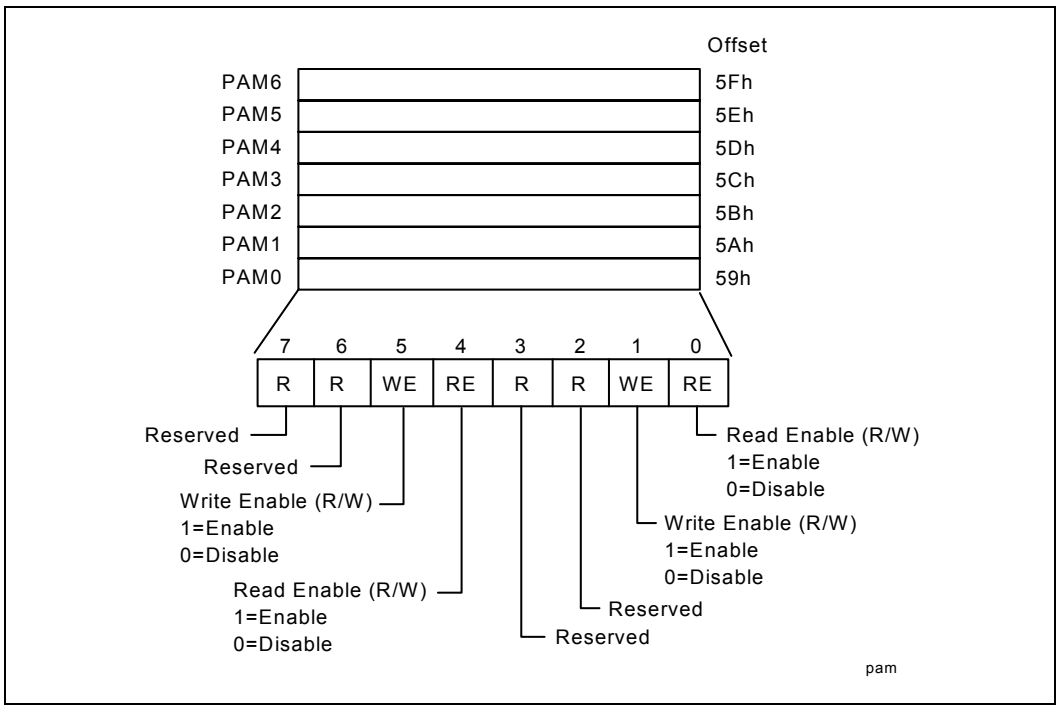


Table 31. PAM Registers and Associated System Memory Segments

PAM Reg	Attribute Bits				System Memory Segment	Comments	Offset
PAM0[3:0]	**Reserved**						59h
PAM0[7:4]	R	R	WE	RE	0F0000h–0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	R	WE	RE	0C0000h–0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	R	WE	RE	0C4000h–0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	R	WE	RE	0C8000h–0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	R	WE	RE	0CC000h–0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	R	WE	RE	0D0000h–0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	R	WE	RE	0D4000h–0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	R	WE	RE	0D8000h–0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	R	WE	RE	0DC000h–0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	R	WE	RE	0E0000h–0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	R	WE	RE	0E4000h–0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	R	WE	RE	0E8000h–0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	R	WE	RE	0EC000h–0EFFFFh	BIOS Extension	5Fh

For details on overall system address mapping scheme see the Address Decoding section of this document.

DOS Application Area (00000h–9FFFh)

The DOS area is 640 kB in size and it is further divided into two parts. The 512-kB area at 0 to 7FFFFh is always mapped to the main system memory controlled by the GMCH/MCH, while the 128-kB address range from 080000 to 09FFFFh can be mapped to PCI0 or to main DDR SDRAM. By default this range is mapped to main system memory and can be declared as a main system memory hole (accesses forwarded to PCI0) via GMCH/MCH's FDHC Configuration register.

Video Buffer Area (A0000h–BFFFFh)

Attribute Bits do not control this 128-kB area. The Host-initiated cycles in this region are always forwarded to either PCI0 or PCI2 unless this range is accessed in SMM mode. ***Routing of accesses is controlled by the Legacy VGA Control Mechanism of the "Virtual" PCI-PCI Bridge Device embedded within the GMCH.***

This area can be programmed as SMM area via the SMRAM register. When used as an SMM space, this range can not be accessed from the hub interface.

Expansion Area (C0000h–DFFFFh)

This 128-kB area is divided into eight 16-kB segments that can be assigned with different attributes via PAM Control register as defined in Table 31 and Figure 6.

Extended System BIOS Area (E0000h–EFFFFh)

This 64-kB area is divided into four 16-kB segments that can be assigned with different attributes via PAM Control register as defined in Table 31 and Figure 6.

System BIOS Area (F0000h–FFFFFh)

This area is a single 64-kB segment that can be assigned with different attributes via PAM Control register as defined in Table 31 and Figure 6.

3.7.20 SMRAM – System Management RAM Control Register (Device #0)

Address Offset: 60h
Default Value: 02h
Access: Read/Write/Lock, Read Only
Size: 8 bits

The SMRAM register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock Bits function only when G_SMRAME Bit is set to a 1. Also, the Open Bit must be Reset before the LOCK Bit is set.

Bit	Description
7	**Reserved**
6	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DDR SDRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. When D_LCK is set to a 1, D_OPEN is Reset to 0 and becomes Read Only.
5	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM Space, DDR SDRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DDR SDRAM. This will allow SMM software to reference “through” SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. D_CLS applies to all SMM spaces (Cseg, Hseg, and Tseg).
4	**SMM Space Locked (D_LCK):** When D_LCK is set to 1, then D_OPEN is Reset to 0 and D_LCK, D_OPEN, G_SMRAME, C_BASE_SEG, GMS, DRB, DRA, H_SMRAM_EN, TSEG_SZ and TSEG_EN become Read Only. D_LCK can be set to 1 via a normal Configuration Space Write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	**Global SMRAM Enable (G_SMRAME):** If set to a 1, then Compatible SMRAM functions is enabled, providing 128 kB of DDR SDRAM accessible at the A0000h address while in SMM (ADS# with SMM decode). To enable Extended SMRAM function this bit must be set to 1, refer to the section on SMM for more details. Once D_LCK is set, this bit becomes Read Only.
2:0	**Compatible SMM Space Base Segment (C_BASE_SEG)—RO:** This field indicates the location of SMM space. “SMM DRAM” is not remapped. It is simply “made visible” if the conditions are right to access SMM space, otherwise the access is forwarded to hub interface. C_BASE_SEG is hardwired to 010 to indicate that the GMCH supports the SMM space at A0000h–BFFFFh.

3.7.21 ESMRAMC – Extended System Management RAM Control (Device #0)

Address Offset: 61h
Default Value: 38h
Access: Read/Write/Lock
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM Space. The Extended SMRAM (E_SMRAM) Memory provides a Write-Back cacheable SMRAM Memory Space that is above 1 MB.

Bit	Description
7	**H_SMRAM_EN (H_SMRAME):** Controls the SMM Memory Space location (i.e., above 1 MB or below 1 MB). When G_SMRAME is 1 and H_SMRAME this bit is set to 1, the high SMRAM Memory Space is enabled. SMRAM accesses from 0FEDA0000h to 0FEDBFFFFh are remapped to DDR SDRAM address 000A0000h to 000BFFFFh. Once D_LCK is set, this bit becomes Read Only.
6	**E_SMRAM_ERR (E_SMERR):** This bit is set when CPU accesses the defined DDR SDRAM ranges in Extended SMRAM (High system memory and T-segment) while not in SMM Space. It is software's responsibility to clear this bit. The software must Write a 1 to this bit to clear it.
5	**SMRAM_Cache (SM_CACHE):** GMCH/MCH forces this bit to 1.
4	**SMRAM_L1_EN (SM_L1):** GMCH/MCH forces this bit to 1.
3	**SMRAM_L2_EN (SM_L2):** GMCH/MCH forces this bit to 1.
2:1	**Reserved**
0	**TSEG_EN (T_EN):** Enabling of SMRAM Memory (TSEG, 1 Mbytes of additional SMRAM Memory) for Extended SMRAM Space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Once D_LCK is set, this bit becomes Read Only.

3.7.22 ERRSTS – Error Status Register (Device #0)

Address Offset: 62–63h
Default Value: 0000h
Access: Read/Write Clear
Size: 16 bits

This register is used to report various error conditions. An SERR or SMI cycle may be generated on a zero to one transition of any of these flags when enabled in the PCICMD/ERRCMD, SMICMD, or SCICMD registers respectively.

Bit	Description
15:14	**Reserved**
13	**PSB Strobe Glitch Detected (PSBAGL):** When this bit is set to 1 the GMCH/MCH has detected a glitch on one of the PSB strobes. Writing a 1 to it clears this bit.
12	**GMCH/MCH Software Generated Event for SMI:** 1 = This indicates the source of the SMI was a Device #2 Software Event. 0 = Software must Write a 1 to clear this bit.
11	**GMCH/MCH Thermal Sensor Event for SMI/SCI/SERR:** 1 = Indicates that a GMCH/MCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. Note that the status bit is set only if a message is sent based on Thermal event enables in Error Command, SMI Command and SCI Command registers. Note that a Trip Point can generate one of SMI, SCI or SERR interrupts (two or more per event is illegal). Multiple Trip Points can generate the same interrupt. If software chooses this mode, then subsequent Trips may be lost. 0 = Software must Write a 1 to clear this status bit. If this bit is set, then an interrupt message will not be sent on a new Thermal Sensor event.
10	**Reserved**
9	**LOCK to non-DDR SDRAM Memory Flag (LCKF)—R/WC:** 1 = Indicates that a CPU initiated LOCK cycle targeting non-DDR SDRAM Memory Space occurred. 0 = Software must Write a 1 to clear this status bit
8	**Received Refresh Timeout—R/WC:** 1 = This bit is set when 1024 memory core refresh are Queued up. 0 = Software must Write a 1 to clear this status bit.
7	**DRAM Throttle Flag (DTF)—R/WC:** 1 = Indicates that the DDR SDRAM Throttling condition occurred. 0 = Software must Write a 1 to clear this status bit.
6:0	**Reserved**

3.7.23 ERRCMD – Error Command Register (Device #0)

Address Offset: 64–65h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register enables various errors to generate. The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register. It is software's responsibility to make sure that when an SERR error message is enabled for an error condition, SMI and SCI error messages are disabled for that same error condition.

Bit	Description
15:14	**Reserved**
13	**SERR on PSB Strobe Glitch:** When this bit is asserted, the GMCH/MCH will generate a SERR message when a glitch is detected on one of the PSB strobes.
12	**Reserved**
11	**SERR on GMCH/MCH Thermal Sensor Event:** 1 = The GMCH/MCH generates a SERR cycle on a Thermal Sensor Trip that requires an SERR. The SERR must not be enabled at the same time as the SMI/SCI for a Thermal Sensor Trip event. 0 = Software must Write a 1 to clear this status bit.
10	**Reserved**
9	**SERR on LOCK to non-DDR SDRAM Memory:** 1 = The GMCH/MCH generates an SERR cycle when a CPU initiated LOCK transaction targeting non-DDR SDRAM Memory Space occurs. 0 = Reporting of this condition is disabled.
8	**SERR on DDR SDRAM Refresh timeout:** 1 = The GMCH/MCH generates an SERR cycle when a DDR SDRAM Refresh timeout occurs. 0 = Reporting of this condition is disabled.
7	**SERR on DDR SDRAM Throttle Condition:** 1 = The GMCH/MCH generates an SERR cycle when a DDR SDRAM Read or Write Throttle condition occurs. 0 = Reporting of this condition is disabled.
6	**SERR on Receiving Target Abort on Hub Interface:** 1 = The GMCH/MCH generates an SERR cycle when a GMCH/MCH cycle is terminated with a Target Abort. 0 = Reporting of this condition is disabled.
5	**SERR on Receiving Unimplemented Special Cycle Completion Packet:** 1 = The GMCH/MCH generates an SERR cycle when a GMCH/MCH initiated request is terminated with a Unimplemented Special cycle completion packet. 0 = Reporting of this condition is disabled.

Bit	Description
4:2	**Reserved**
1	**SERR on Multiple-bit ECC Error:** 1 = For systems that support ECC, this field must be set to 1. 0 = Reserved
0	**SERR on Single-bit ECC Error:** 1 = For systems that support ECC, this field must be set to 1. 0 = Reserved

3.7.24 SMICMD – SMI Error Command Register (Device #0)

Address Offset: 66h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register enables various errors to generate an SMI cycle. When an Error Flag is set in the ERRSTS register, it can generate a SERR or SMI cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers respectively. An error can generate one and only one Error cycle. It is software's responsibility to make sure that when an SMI Error Message is enabled for an error condition, SERR, and SCI Error Messages are disabled for that same error condition.

Bit	Description
7:4	**Reserved**
3	**SMI on GMCH/MCH Thermal Sensor Trip:** 1 = An SMI Hub Interface Special cycle is generated by GMCH/MCH when the Thermal Sensor Trip requires an SMI. A Thermal Sensor Trip Point cannot generate more than one special cycle.
2	**Reserved**
1	**SMI on Multiple-bit ECC Error:** 1 = For systems that support ECC, this field must be set to 1. 0 = Reserved
0	**SMI on Single-bit ECC Error:** 1 = For systems that support ECC, this field must be set to 1. 0 = Reserved

3.7.25 SCICMD – SCI Error Command Register (Device #0)

Address Offset: 67h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register enables various errors to generate a SCI cycle. When an Error Flag is set in the ERRSTS register, it can generate a SERR or SMI cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers respectively. An error can generate one and only one Error Special cycle. It is software's responsibility to make sure that when an SCI error message is enabled for an error condition, SERR and SMI Error Messages are disabled for that same error condition.

Bit	Description
7:4	**Reserved**
3	**SCI on GMCH/MCH Thermal Sensor Trip:** 1 = An SCI Hub Interface Special cycle is generated by GMCH/MCH when the Thermal Sensor Trip requires an SCI. A Thermal Sensor Trip Point cannot generate more than one special cycle.
2	**Reserved**
1	**SCI on Multiple-bit ECC Error:** 1 = For systems that support ECC, this field must be set to 1. 0 = For systems that do not support ECC, this field must be 0.
0	**SCI on Single-bit ECC Error:** 1 = For systems that support ECC, this field must be set to 1. 0 = For systems that do not support ECC, this field must be 0.

3.7.26 SHIC - Secondary Host Interface Control Register (Device #0)

Address Offset: 74-77h
Default Value: 00006010h
Access: Read Only, Read/Write
Size: 32 bits

Bit	Description
31:2	**Reserved**
1	**AGP/DVO Mux Strap (Read only):** Specifies the use of AGP bus muxed with DVO. This bit is defined at Reset by a strap on the G_PAR/DVO_DETECT signal. By default the AGP bus pulls this signal high. If AGP capability is disabled, then the AGP pins are dedicated to internal graphics DVO functionality. If AGP capability is available, then based on this strap, the AGP interface is used for AGP functionality or DVO functionality based on this strap. 1 = AGP. 0 = DVO
0	**Reserved**

3.7.27 ACAPID – AGP Capability Identifier Register (Device #0)

Address Offset: A0-A3h
Default Value: 00200002h
Access: Read Only
Size: 32 bits

This register provides standard identifier for AGP capability.

Bit	Description
31:24	**Reserved**
23:20	**Major AGP Revision Number.** These bits provide a major revision number of AGP specification to which this version of GMCH/MCH conforms. These bits are set to the value 0010b to indicate AGP Rev. 2.x.
19:16	**Minor AGP Revision Number**. These bits provide a minor revision number of AGP specification to which this version of GMCH/MCH conforms. This is set to 0000b (i.e., implying Rev x.0) Together with major revision number this field identifies GMCH/MCH as an AGP REV 2.0 compliant device.
15:8	**Next Capability Pointer**. AGP capability is the last capability described via the capability pointer mechanism and therefore these bits are set to 00h to indicate the end of the capability linked list.
7:0	**AGP Capability ID.** This field identifies the linked list item as containing AGP registers. This field has the value 02h as assigned by the PCI SIG.

3.7.28 AGPSTAT – AGP Status Register (Device #0)

Address Offset: A4–A7h
Default Value: 1F000217h
Access: Read Only
Size: 32 bits

This register reports AGP device capability/status.

Bit	Description
31:24	**Request (RQ).** Indicates a maximum of 32 outstanding AGP command requests can be handled by the GMCH/MCH. Default =1Fh to allow a maximum of 32 outstanding AGP command requests.
23:10	**Reserved**
9	**Side Band Addressing (SBA).** Indicates that the GMCH/MCH supports side band addressing.
8:6	**Reserved**
5	**Address Support Above 4 GB (4 GB).** Indicates that the GMCH/MCH does not support addresses greater than 4 gigabytes.
4	**Fast Writes.** 1 = The GMCH/MCH supports Fast Writes from the CPU to the AGP master. (Default)
3	**Reserved**
2:0	**RATE**. After reset the GMCH/MCH reports its data transfer rate capability. Bit 0 identifies if AGP device supports 1x data transfer mode, bit 1 identifies if AGP device supports 2x data transfer mode, bit 2 identifies if AGP device supports 4x data transfer mode. 1x , 2x , and 4x data transfer modes are supported by the GMCH/MCH and therefore this bit field has a Default Value = 111. **NOTE**: The selected data transfer mode applies to both AD bus and SBA bus.

3.7.29 AGPCMD – AGP Command Register (Device #0)

Address Offset: A8–ABh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides control of the AGP operational parameters.

Bit	Description
31:10	**Reserved**
9	**Side Band Addressing Enable (SBA_EN).** When this bit is set to 1, the side band addressing mechanism is enabled.
8	**AGP Enable.** 0 = Disable. When this bit is reset to 0, the GMCH/MCH will ignore all AGP operations, including the sync cycle. Any AGP operations received while this bit is set to 1 will be serviced even if this bit is reset to 0. If this bit transitions from a 1 to a 0 on a clock edge in the middle of an SBA command being delivered in 1X mode, the command will be issued. 1 = Enable. The GMCH/MCH will respond to AGP operations delivered via PIPE#, or to operations delivered via SBA if the *AGP Side Band Enable* bit is also set to 1.
7:6	**Reserved**
5	**Address Support Above 4 GB Enable (4 GB_EN).** The GMCH/MCH as an AGP target does not support addressing greater than 4 gigabytes.
4	**Fast Write Enable.** 1 = Enable. GMCH/MCH AGP master supports Fast Writes. 0 = Disable (Default). Fast Writes are disabled.
3	**Reserved**
2:0	**Data Rate.** The settings of these bits determine the AGP data transfer rate. One (*and only one*) bit in this field must be set to indicate the desired data transfer rate. Bit 0: 1X, Bit 1: 2X, Bit 2: 4x. The same bit must be set on both master and target. Configuration software will update this field by setting only one bit that corresponds to the capability of AGP master (after that capability has been verified by accessing the same functional register within the AGP masters configuration space.) **NOTE**: The selected data transfer mode applies to both AD bus and SBA bus.

3.7.30 AGPCTRL – AGP Control Register (Device #0)

Address Offset: B0–B1h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register provides for additional control of the AGP interface.

Note: Bit 7 is visible to the operating system and must be retained in this position.

Bit	Description
15:8	**Reserved**
7	**GTLB Enable (and GTLB Flush Control).** **NOTE:** This bit can be changed dynamically (i.e., while an access to GTLB occurs). This bit must not be changed through memory mapped configuration register access space.
6:0	**Reserved**

3.7.31 AFT – AGP Functional Register (Device #0)

Address Offset: B2–B3h
Default Value: E9F0h
Access: Read/Write, Read/WriteClear
Size: 16 bits

This register provides for additional control of the AGP interface.

Bit	Description
15:11	**Reserved**
10	**PCI Write Streaming Disable (PCIBWSD):** When this bit is set to ‘1’, PCI_B writes to DDR SDRAM are disconnected at a 32 byte cache line boundary (write streaming is disabled). When this bit is set to ‘0’ (default), write streaming is enabled.
9:0	**Reserved**

3.7.32 APSIZE – Aperture Size (Device #0)

Address Offset: B4h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register determines the effective size of the Graphics Aperture used for a particular GMCH/MCH configuration. This register can be updated by the GMCH/MCH-specific BIOS configuration sequence before the PCI standard bus enumeration sequence. If the register is not updated then a default value will select an aperture of maximum size (i.e., 256 MB). The size of the table that will correspond to a 256 MB aperture is not practical for most applications and therefore these bits must be programmed to a smaller practical value that will force adequate address range to be requested via APBASE register from the PCI configuration software.

Bit	Description
7:6	**Reserved**
5:0	**Graphics Aperture Size (APSIZE).** Each bit in APSIZE[5:4] operates on similarly ordered bits in APBASE[27:26] of the Aperture Base configuration register. When a particular bit of this field is “0” it forces the similarly ordered bit in APBASE[27:26] to behave as “0”. When a particular bit of this field is set to “1” it allows corresponding bit of the APBASE[27:26] to be read/write accessible. Only the following combinations are allowed when the Aperture is enabled: Bits[5:4] Aperture Size 11 64 MB 10 128 MB 00 256 MB Default for APSIZE[5:4]=00b forces default APBASE[27:26] =00b (i.e. all bits respond as “hardwired” to 0). This provides maximum aperture size of 256 MB. As another example, programming APSIZE[5:4]=11b enables APBASE[27:26] as read/write programmable providing a minimum size of 64 MB. 3:0: Reserved set to zero for software compatibility.

3.7.33 ATTBASE – Aperture Translation Table Base Register (Device #0)

Address Offset: B8–BBh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides the starting address of the Graphics Aperture Translation Table Base located in the main DDR SDRAM. This value is used by the GMCH/MCH's Graphics Aperture address translation logic (including the GTLB logic) to obtain the appropriate address translation entry required during the translation of the aperture address into a corresponding physical DDR SDRAM address. The ATTBASE register may be dynamically changed.

Note: The address provided via ATTBASE is 4 kB aligned.

Bit	Description
31:12	This field contains a pointer to the base of the translation table used to map memory space addresses in the aperture range to addresses in main memory.
11:0	**Reserved**

3.7.34 AMTT – AGP Interface Multi-Transaction Timer Register (Device #0)

Address Offset: BCh
Default Value: 00h
Access: Read/Write
Size: 8 bits

AMTT is an 8-bit register that controls the amount of time that the GMCH/MCH's arbiter allows AGP/PCI master to perform multiple back-to-back transactions. The GMCH/MCH's AMTT mechanism is used to optimize the performance of the AGP master (using PCI semantics) that performs multiple back-to-back transactions to fragmented memory ranges (and as a consequence it can not use long burst transfers). The AMTT mechanism applies to the CPU-AGP/PCI transactions as well and it guarantees to the CPU a fair share of the AGP/PCI interface bandwidth.

The number of clocks programmed in the AMTT represents the guaranteed time slice (measured in 66- MHz clocks) allotted to the current agent (either AGP/PCI master or Host bridge) after which the AGP arbiter will grant the bus to another agent. The default value of AMTT is 00h and disables this function. The AMTT value can be programmed with 8 clock granularity. For example, if the AMTT is programmed to 18h, then the selected value corresponds to the time period of 24 AGP (66-MHz) clocks.

Bit	Description
7:3	**Multi-Transaction Timer Count Value**. The number programmed in these bits represents the guaranteed time slice (measured in eight 66-MHz clock granularity) allotted to the current agent (either AGP/PCI master or Host bridge) after which the AGP arbiter will grant the bus to another agent.
2:0	**Reserved**

3.7.35 LPTT – Low Priority Transaction Timer Register (Device #0)

Address Offset: BDh
Default Value: 00h
Access: Read/Write
Size: 8 bits

LPTT is an 8-bit register similar in a function to AMTT. This register is used to control the minimum tenure on the AGP for low priority data transaction (both reads and writes) issued using PIPE# or SB mechanisms.

The number of clocks programmed in the LPTT represents the guaranteed time slice (measured in 66-MHz clocks) allotted to the current low priority AGP transaction data transfer state. This does not necessarily apply to a single transaction but it can span over multiple low-priority transactions of the same type. After this time expires the AGP arbiter may grant the bus to another agent if there is a pending request. The LPTT does not apply in the case of high-priority request where ownership is transferred directly to high-priority requesting queue. The default value of LPTT is 00h and disables this function. The LPTT value can be programmed with 8 clock granularity. For example, if the LPTT is programmed to 10h, then the selected value corresponds to the time period of 16 AGP (66-MHz) clocks.

Bit	Description
7:3	**Low Priority Transaction Timer Count Value**. The number of clocks programmed in these bits represents the guaranteed time slice (measured in eight 66 MHz clock granularity) allotted to the current low priority AGP transaction data transfer state.
2:0	**Reserved.**

3.8 Main Memory Control, Memory I/O Control Registers (Device #0, Function #1)

The following table shows the GMCH/MCH Configuration Space for Device #0, Function #1.

Table 32. Host-Hub interface Bridge/System Memory Controller Configuration Space (Device #0, Function#1)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	00	01	8086h	RO
Device Identification	DID	02	03	3584h	RO
PCI Command	PCICMD	04	05	0006h	RO,R/W
PCI Status	PCISTS	06	07	0080h	RO,R/WC
Revision Identification	RID	08	08	02h)	RO
Sub-Class Code	SUBC	0A	0A	80h	RO
Base Class Code	BCC	0B	0B	08h	RO
Header Type	HDR	0E	0E	80h	RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	00h	RO
DRAM Row 0-3 Boundary	DRB	40	43	00000000h	RW
DRAM Row 0-3 Attribute	DRA	50	51	7777h	RW
DRAM Timing	DRT	60	63	18004425h	RW
DRAM Controller Power Management Control	PWRMG	68	6B	00000000h	R/W
Dram Controller Mode	DRC	70	73	00000081h	R/W
DRAM Throttle Control	DTC	A0	A3	00000000h	R/W/L

3.8.1 VID – Vendor Identification Register (Device #0,Function #1)

Address Offset: 00-01h
Default Value: 8086h
Access: Read Only
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification (VID):** This register field contains the PCI standard identification for Intel.

3.8.2 DID – Device Identification Register (Device #0,Function #1)

Address Offset: 02-03h
Default Value: 3584h
Access: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number (DID):** This is a 16-bit value assigned to the GMCH/MCH Host– hub interface Bridge Function #1 (3584h).

3.8.3 PCICMD – PCI Command Register (Device #0,Function #1)

Address Offset: 04-05h
Default Value: 0006h
Access: Read Only, Read/Write
Size: 16 bits

Since GMCH/MCH Device #0 does not physically reside on PCI_A, many of the bits are not implemented.

Bit	Description
15:10	**Reserved**
9	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back Write. Since Device #0 is strictly a target, this bit is not implemented and is hardwired to 0. Writes to this bit position have no affect.
8	**SERR Enable (SERRE):** SERR# is not implemented by Function #1 of Device #0 of the GMCH/MCH and this bit is hardwired to 0. Writes to this bit position have no effect.
7	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the GMCH/MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	**Parity Error Enable (PERRE):** PERR# is not implemented by GMCH/MCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5	**VGA Palette Snoop Enable (VGASNOOP):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	**Memory Write and Invalidate Enable (MWIE):** The GMCH/MCH will never issue Memory Write and Invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	**Special Cycle Enable (SCE):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	**Bus Master Enable (BME):** The GMCH/MCH is always enabled as a master on hub interface. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	**Memory Access Enable (MAE):** The GMCH/MCH always allows access to main system memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	**I/O Access Enable (IOAE):** This bit is not implemented in the GMCH/MCH and is hardwired to a 0. Writes to this bit position have no effect.

3.8.4 PCISTS – PCI Status Register (Device #0,Function #1)

Address Offset: 06-07h
Default Value: 0080h
Access: Read Only, Read/WriteClear
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #0's PCI Interface. Bit 14 is Read/Write Clear. All other bits are Read Only. Since GMCH/MCH Device #0 does not physically reside on PCI_A, many of the bits are not implemented.

Bit	Description
15	**Detected Parity Error (DPE):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	**Signaled System Error (SSE):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
13	**Received Master Abort Status (RMAS):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
12	**Received Target Abort Status (RTAS):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
11	**Signaled Target Abort Status (STAS):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
10:9	**DEVSEL Timing (DEVT):** These bits are hardwired to "00". Writes to these bit positions have no affect. Device #0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that the GMCH/MCH does not limit optimum DEVSEL timing for PCI_A.
8	**Master Data Parity Error Detected (DPD):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
7	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device #0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the GMCH/MCH does not limit the optimum setting for PCI_A.
6:5	**Reserved**
4	**Capability List (CLIST):** This bit is hardwired to 0 to indicate to the configuration software that this device/function does not implement new capabilities. Default Value = 0
3:0	**Reserved**

3.8.5 RID – Revision Identification Register (Device #0,Function #1)

Address Offset: 08h
Default Value: 02h
Access: Read Only
Size: 8 bits

This register contains the revision number of the GMCH/MCH Device #0. These bits are Read Only and Writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH/MCH Device #0. Intel 852GME = 02 Intel 852PM = 02

3.8.6 SUBC – Sub-Class Code Register (Device #0,Function #1)

Address Offset: 0Ah
Default Value: 80h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class code for the GMCH/MCH Device #0. This code is 80h indicating Other Peripheral device.

Bit	Description
7:0	**Sub-Class Code (SUBC):** This is an 8-bit value that indicates the category of Peripheral device into which the GMCH/MCH Function #1 falls. The code is 80h indicating Other Peripheral device.

3.8.7 BCC – Base Class Code Register (Device #0,Function #1)

Address Offset: 0Bh
Default Value: 08h
Access: Read Only
Size: 8 bits

This register contains the Base Class code of the GMCH/MCH Device #0 Function #1. This code is 08h indicating Other Peripheral device.

Bit	Description
7:0	**Base Class Code (BASEC):** This is an 8-bit value that indicates the Base Class Code for the GMCH/MCH. This code has the value 08h, indicating Other Peripheral device.

3.8.8 HDR – Header Type Register (Device #0,Function #1)

Address Offset: 0Eh
Default Value: 80h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Description
7:0	**PCI Header (HDR):** This field always returns 80 to indicate that Device #0 is a multifunction device. Reads and Writes to this location have no effect.

3.8.9 SVID – Subsystem Vendor Identification Register (Device #0,Function #1)

Address Offset: 2C-2Dh
Default Value: 0000h
Access: Read/Write Once
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Description
15:0	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes Read Only.

3.8.10 SID – Subsystem Identification Register (Device #0,Function #1)

Address Offset: 2E-2Fh
Default Value: 0000h
Access: Read/Write Once
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Description
15:0	**Subsystem ID (SUBID):** This field should be programmed during BIOS initialization. After it has been Written once, it becomes Read Only.

3.8.11 CAPPTR – Capabilities Pointer Register (Device #0,Function #1)

Address Offset: 34h
Default Value: 00h
Access: Read Only
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Description
7:0	**Pointer to the offset of the first capability ID register block:** In this case there are no capabilities, therefore these bits are hardwired to 00h to indicate the end of the capability linked list.

3.8.12 DRB – DRAM Row (0:3) Boundary Register (Device #0,Function #1)

Address Offset: 40-43h
Default Value: 00h each
Access: Read/Write
Size: 8 bits each

The **DDR SDRAM Row Boundary Register** defines the upper boundary address of each DDR SDRAM row with a granularity of 32-MB. Each row has its own single-byte **DRB** register. For example, a value of 1 in **DRB0** indicates that 32-MB of DDR SDRAM has been populated in the first row. Since the GMCH/MCH supports a total of four rows of system memory, DRB0-3 are used. The registers from 44h-4Fh are reserved for DRBs 4-15.

Row0: 40h
Row1: 41h
Row2: 42h
Row3: 43h
44h to 4Fh is reserved.

DRB0 = Total System Memory in Row0 (in 32 -MB increments)
DRB1 = Total System Memory in Row0 + Row1 (in 32 -MB increments)
DRB2 = Total System Memory in Row0 + Row1 + Row2 (in 32 -MB increments)
DRB3 = Total System Memory in Row0 + Row1 + Row2 + Row3 (in 32- MB increments)

Each Row is represented by a Byte. Each Byte has the following format.

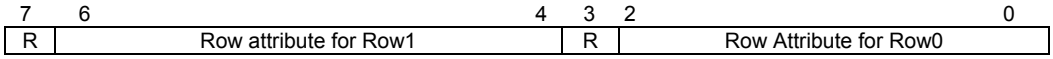
Bit	Description
7:0	**DDR SDRAM Row Boundary Address:** This 8-bit value defines the upper and lower addresses for each DDR SDRAM row. This 8-bit value is compared against a set of address lines to determine the upper address limit of a particular row. Also the minimum system memory supported is 64-MB in 64-Mb granularity; hence bit 0 of this register must be programmed to a zero.

3.8.13 DRA – DRAM Row Attribute Register (Device #0,Function #1)

Address Offset: 50-51h
Default Value: 77h Each
Access: Read/Write
Size: 8 bits

The DDR SDRAM Row Attribute register defines the page sizes to be used when accessing different pairs of rows. Each nibble of information in the DRA registers describes the page size of a pair of rows:

Row0, 1: 50h
Row2, 3: 51h
52h-5Fh: Reserved.



Bit	Description
7	**Reserved**
6:4	**Row Attribute for odd-numbered Row:** This field defines the page size of the corresponding row. 000: Reserved 001: 4 kB 010: 8 kB 011: 16 kB 111: Not Populated Others: Reserved
3	**Reserved**
2:0	**Row Attribute for even-numbered Row:** This field defines the page size of the corresponding row. 000: Reserved 001: 4 kB 010: 8 kB 011: 16 kB 111: Not Populated Others: Reserved

3.8.14 DRT – DRAM Timing Register (Device #0,Function #1)

Address Offset: 60-63h
Default Value: 18004425h
Access: Read/Write
Size: 32 bits

This register controls the timing of the DDR SDRAM controller.

Bit	Description
31	**DDR Internal Write to Read Command delay (tWTR):** The tWTR is a std. DDR SDRAM timing parameter with a value of 1 CK for CL=2 and 2.5. The tWTR is used to time RD command after a WR command (to same Row): 0: tWTR is set to 1 Clock (CK), used for DDR SDRAM CL=2 or 2.5 1: Reserved
30	**DDR SDRAM Write Recovery time (tWR):** Write recovery time is a std. DDR SDRAM timing parameter with the value of 15 ns. It should be set to 2 CK when DDR200 is used. The tWR is used to time PRE command launch after a WR command, when DDR SDRAM components are populated. 0: tWR is set to 2 Clocks (CK) 1: tWR is set to 3 Clocks (CK)
29:28	**Back To Back Write-Read commands spacing (DDR different Rows/Bank):** This field determines the WR-RD command spacing, in terms of common clocks for DDR SDRAM based on the following formula: DQSS + 0.5xBL + TA (WR-RD) – CL DQSS: is time from Write command to data and is always 1 CK BL: is Burst Length and can be set to 4 (using integrated graphics) or 8 (using AGP port) TA (WR-RD): is required DQ turn-around, can be set to 1 or 2 CK CL: is CAS Latency, can be set to 2 or 2.5 **Examples of usage:** For BL=4, with single DQ turn-around and CL=2, this field must be set to 2 CK (1+2+1-2) **Encoding** **CK between WR and RD commands** **BL=4** **BL=8** 00: 4 6 01: 3 5 10: 2 4 11: Reserved **NOTE**: This turn around control is used for DDR SDRAM parts only, for all cycle lengths. This field specifies timing for Write-Read commands to different rows. The bigger turn-around value is used in large configurations, where the difference in total channel delay between the fastest and slowest S0-DIMM is larger. It must be used for all configurations, so that read preamble (at maximum corner) will not overlap the previous write data.

Bit	Description
27:26	**Back To Back Read-Write commands spacing (DDR, same or different Rows/Bank):** This field determines the RD-WR command spacing, in terms of common clocks based on the following formula: CL + 0.5xBL + TA (RD-WR) – DQSS DQSS: is time from Write command to data and is always 1 CK BL: is Burst Length which is set to 4 or 8. TA (RD-WR): is required DQ turn-around, can be set to 1, 2 or 3 CK CL: is CAS latency, can be set to 2 or 2.5 **Examples of usage:** For BL=4, with single DQ turn-around and CL=2, this field must be set to 4 CK (2+2+1-1) For BL=8, with single DQ turn-around and CL=2.5, this field must be set to 8 CK (2.5+4+2-1) **Encoding** **CK between RD and WR commands** **BL = 4** **BL=8** 00: 7 9 01: 6 8 10: 5 7 11: 4 6 **NOTE:** Since reads in DDR SDRAM cannot be terminated by Writes, the Space between commands is not a function of Cycle Length but of Burst Length.
25	**Back To Back Read-Read commands spacing (DDR, different Rows):** This field determines the RD-RD Command Spacing, in terms of common clocks based on the following formula: 0.5xBL + TA(RD-RD) BL: is Burst Length and can be set to 4 or 8. TA (RD-RD): is required DQ turn-around, can be set to 1 or 2 CK **Examples of usage:** For BL=4, with single DQ turn-around, this field must be set to 3 CK (2+1) For BL=8, with single DQ turn-around, this field must be set to 6 CK (4+2) **Encoding** **CK between RD and RD commands** **BL = 4** **BL = 8** 0: 4 6 for 2 TA (Read-Read) 1: 3 5 for 1 TA (Read-Read) **NOTE:** Since a Read to a different row does not terminate a Read, the Space between commands is not a function of Cycle Length but of Burst Length.
24:15	**Reserved**

Bit	Description
14:12	**Refresh Cycle Time (tRFC):** Refresh Cycle Time is measured for a given row from REF command (to perform a refresh) until following ACT to same row (to perform a Read or Write). It is tracked separately from tRC for DDR SDRAM. Current DDR SDRAM spec requires tRFC of 75 ns (DDR266) and 80 ns (DDR200). Therefore, this field will be set to 8 clocks for DDR200, 10 clocks for DDR266. **Encoding tRFC** 000: 14 clocks 001: 13 clocks 010: 12 clocks 011: 11 clocks 100: 10 clocks 101: 9 clocks 110: 8 clocks 111: 7 clocks
11	**Activate to Precharge delay (tRAS), MAX:** This bit controls the maximum number of clocks that a DDR SDRAM bank can remain open. After this time period, the system memory Controller will guarantee to pre-charge the bank. Note that this time period may or may not be set to overlap with time period that requires a refresh to happen. The DDR SDRAM Controller includes a separate tRAS-MAX counter for every supported bank. With a maximum of four rows and four banks per row, there are 16 counters. 0: 120 micro-seconds 1: Reserved.
10:9	**Activate to Precharge delay (tRAS), MIN:** This bit controls the number of DDR SDRAM clocks for tRAS MIN 00: 8 Clocks 01: 7 Clocks 10: 6 Clocks 11: 5 Clocks
8:7	**Reserved**
6:5	**CAS# Latency (tCL):** Encoding DDR SDRAM CL 00: 2.5 01: 2 10: Reserved 11: Reserved
4	**Reserved**

Bit	Description
3:2	**DDR SDRAM RAS# to CAS# Delay (tRCD):** This bit controls the number of clocks inserted between a Row Activate command and a Read or Write command to that row. **Encoding** **tRCD** 00: 4 DDR SDRAM Clocks (DDR 333 SDRAM) 01: 3 DDR SDRAM Clocks 10: 2 DDR SDRAM Clocks 11: Reserved
1:0	**DDR SDRAM RAS# Precharge (tRP):** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same row. Encoding tRP 00: 4 DDR SDRAM Clocks (DDR 333 SDRAM) 01: 3 DDR SDRAM Clocks 10: 2 DDR SDRAM Clocks 11: Reserved

3.8.15 PWRMG – DRAM Controller Power Management Control Register (Device #0,Function #1)

Address Offset: 68h-6Bh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

Bit	Description
31:24	**Reserved**
23:20	**Row State Control:** This field determines the number of clocks the system memory controller will remain in the idle state before it begins pre-charging all pages or powering down rows. **- PDEn: Power Down Enable** **- PCEn: Page Close Enable** **- TC: Timer Control** **PDEn(23): PCEn(22): TC(21:20) Function** 0 0 XX All Disabled 0 1 XX Reserved 1 0 XX Reserved 1 1 00 Immediate Precharge and Powerdown 1 1 01 Reserved 1 1 10 Precharge and Power Down after 16 DDR SDRAM Clocks 1 1 11 Precharge and Power Down after 64 DDR SDRAM Clocks
19:17	**Reserved**
16	**SO-DIMM Clock Gating Disable - R/W** 0 = Only populated DIMMs received the clock. 1 = The DRAM interface controller will allow all SO-DIMM clocks to toggle.
15	**Self Refresh GMCH Memory Interface Data Bus Power Management Optimization Enable:** 0 = Enable 1 = Disable
14	**CS# Signal Drive Control:** 0 = Enable CS# Drive Control, based on rules described in DRC bit 12. 1 = Disable CS# Drive Control, based on rules described in DRC bit 12.
13	**Self Refresh GMCH Memory Interface Data Bus Power Management:** 0 = In Self Refresh Mode GMCH Power Management is Enabled. 1 = In Self Refresh Mode the GMCH Power Management is Disabled.

Bit	Description
12	**Dynamic Memory Interface Power Management:** 0 = Dynamic Memory Interface Power Management Enabled. 1 = Dynamic Memory Interface Power Management Disabled.
11	**Rcven DLL shutdown disable:** 0 = Normal operation. RCVEN DLL is turned off when the corresponding SO-DIMM is unpopulated. 1 = Reserved
10	**ECC SO-DIMM Clock tri-state Disable:** 0 = When DDR SDRAM ECC is not enabled, the ECC clocks (i.e., SCK2/SCK2#, SCK5/SCK5#,) are tri- stated. 1 = When DDR SDRAM ECC is enabled, the ECC clocks (i.e., SCK2/SCK2#, SCK5/SCK5#,) are treated just like the other clocks.
9:1	**Reserved**
0	**Power State S1/S3 Refresh Control:** 0 = Normal Operation, Pending refreshes are not completed before entering Self Refresh for S1/S3. 1 = All Pending Refreshes plus one extra is performed before entering Self Refresh for S1/S3.

3.8.16 DRC – DRAM Controller Mode Register (Device #0,Function #1)

Address Offset: 70-73h
Default Value: 00000081h
Access: RO, Read/Write
Size: 32 bits

Bit	Description
31:30	**Revision Number (REV):** Reflects the revision number of the format used for DDR SDRAM register definition (Read Only).
29	**Initialization Complete (IC):** This bit is used for communication of software state between the Memory Controller and the BIOS. BIOS sets this bit to 1 after initialization of the DDR SDRAM Memory Array is complete. Setting this bit to a 1 enables DDR SDRAM Refreshes. On power up and S3 exit, the BIOS initializes the DDR SDRAM array and sets this bit to a 1. This bit works in combination with the RMS bits in controlling Refresh state: **IC** **Refresh State** 0 OFF 1 ON
28:24	**Reserved**
23:22	**Number of Channels (CHAN):** Reflects that GMCH supports only one system memory channel. 00 One channel is populated appropriately Others: Reserved
21:20	**DDIM DDR SDRAM Data Integrity Mode:** 00: **No-ECC.** No read-merge-write on partial writes. ECC data sense-amps are disabled and the data output is tristated (Default). 01: **ECC** XX: Reserved
19:16	**Reserved**
15	**RAS Lock-Out Enable:** Set to a 1 if all populated rows support RAS Lock-Out. Defaults to 0. If this bit is set to a 1 the DDR SDRAM Controller assumes that the DDR SDRAM guarantees tRAS min before an auto precharge (AP) completes (Note: An AP is sent with a Read or a Write command). Also, the DDR SDRAM Controller does not issue an activate command to the auto pre-charged bank for tRP. If this bit is set to a 0 the DDR SDRAM Controller does not schedule an AP if tRAS min is not met.
14:13	**Reserved**
12	**Address Tri-state enable (ADRTRIEN):** When set to a 1, the SDRAM Controller will tri-state the MA, CMD, and CS# (only when all CKEs are deasserted). Note that when CKE to a row is deasserted, fast chip select assertion is not permitted by the hardware. CKEs deassert based on Idle Timer and/or max row count control. 0:- Address Tri-state Disabled 1:- Address Tri-state Enabled
11:10	**Reserved**

Bit	Description
9:7	**Refresh Mode Select (RMS)**: This field determines whether Refresh is enabled and, if so, at what rate Refreshes will be executed. **000:** Refresh disabled **001:** Refresh enabled. Refresh interval 15.6 µsec **010:** Refresh enabled. Refresh interval 7.8 µsec **011:** Reserved. **111:** Refresh enabled. Refresh interval 64 clocks (fast refresh mode) **Other:** Reserved Any change in the programming of this field Resets the Refresh counter to zero. This function is for testing purposes, it allows test program to align refresh events with the test and thus improve failure repeatability.

Bit	Description
6:4	Mode Select (SMS). These bits select the special operational mode of the DDR SDRAM Interface. The special modes are intended for initialization at power up. 000: Post Reset State – When the GMCH exits Reset (power-up or otherwise), the mode select field is cleared to 000. Software is not expected to Write this value, however if this value is Written, there are no side effects (no Self Refresh or any other special DDR SDRAM cycle). During any Reset sequence, while power is applied and Reset is active, the GMCH deasserts all CKE signals. After internal Reset is deasserted, CKE signals remain deasserted until this field is written to a value different than 000. On this event, all CKE signals are asserted. During Suspend (S3, S4), GMCH internal signal triggers DDR SDRAM Controller to flush pending commands and enter all rows into Self-Refresh mode. As part of Resume sequence, GMCH will be Reset, which will clear this bit field to 000 and maintain CKE signals deasserted. After internal Reset is deasserted, CKE signals remain deasserted until this field is Written to a value different than 000. On this event, all CKE signals are asserted. During Entry to other low power states (C3, S1-M), GMCH internal signal triggers DDR SDRAM Controller to flush pending commands and enter all rows in S1 and relevant rows in C3 (Based on RPDNC3) into Self-Refresh mode. During exit to Normal mode, the GMCH signal triggers DDR SDRAM Controller to Exit Self-Refresh and Resume Normal operation without S/W involvement. 001: NOP Command Enable – All CPU cycles to DDR SDRAM result in a NOP command on the DDR SDRAM interface. 010: All Banks Pre-charge Enable – All CPU cycles to DDR SDRAM result in an All Banks Precharge command on the DDR SDRAM interface. 011: Mode Register Set Enable – All CPU cycles to DDR SDRAM result in a Mode Register set command on the DDR SDRAM Interface. Host address lines are mapped to DDR SDRAM address lines in order to specify the command sent. Host address HA[13:3] are mapped to Memory address SMA[11,9:0]. SMA3 must be driven to 1 for interleave wrap type. For Double Data Rate MA[6:4] needs to be driven based on the value programmed in the CAS# Latency field. CAS Latency MA[6:4] 1.5 Clocks 001 2.0 Clocks 010 2.5 Clocks 110 SMA[7] should always be driven to a 0. SMA[8] Should be driven to a 1 for DLL Reset and 1 for Normal Operation. SMA[12:9] must be driven to 00000. BIOS must calculate and drive the correct host address for each row of Memory such that the correct command is driven on the SMA[12:0] lines. Note that SMAB[5,4,2,1]# are inverted from SMA[5,4,2,1]; BIOS must account for this. 100: Extended Mode Register Set Enable – All CPU cycles to DDR SDRAM result in an “Extended Mode register set” command on the DDR SDRAM Interface. Host address lines are mapped to DDR SDRAM address lines in order to specify the command sent. Host address lines are mapped to DDR SDRAM address lines in order to specify the command sent. Host address HA[13:3] are mapped to Memory address SMA[11,9:0]. SMA[0] = 0 for DLL enable and 1 for DLL disable. All the other SMA lines are driven to 0’s. Note that SMAB[5,4,2,1]# are inverted from SMA[5,4,2,1]; BIOS must account for this. 101: Reserved 110: CBR Refresh Enable – In this mode all CPU cycles to DDR SDRAM result in a CBR cycle on the DDR SDRAM interface 111: Normal operation

Bit	Description
3	**Reserved**
2	**DDR SDRAM Burst Length:** This bit is used to select the DDR SDRAM controller's Burst Length operation mode. It must be set consistently to the DDR SDRAM component setting. Can be set to 8 in DDR SDRAM mode only. Encoding: 0: Burst Length of 4 1: Burst Length of 8
1	**Reserved**

3.8.17 DTC – DRAM Throttling Control Register (Device #0,Function #1)

Offset Address: A0–A3h
Default Value: 00000000h
Access: Read/Write/Lock
Size: 32 bits

Throttling is independent for system memory banks, GMCH Writes, and Thermal Sensor Trips. Read and Write Bandwidth is measured independently for each bank. If the number of Octal - Words (16 bytes) Read/Written during the window defined below (Global DDR SDRAM Sampling Window: GDSW) exceeds the DDR SDRAM Bandwidth Threshold, then the DDR SDRAM Throttling mechanism will be invoked to limit DDR SDRAM Reads/Writes to a lower bandwidth checked over smaller time windows. The throttling will be active for the remainder of the current GDSW and for the next GDSW after which it will return to Non-Throttling mode. The throttling mechanism accounts for the actual bandwidth consumed during the sampling window, by reducing the allowed bandwidth within the smaller throttling window based on the bandwidth consumed during the sampling period. Although bandwidth from/to independent rows and GMCH Write bandwidth is measured independently, once Tripped all transactions except high priority graphics Reads are subject to throttling.

Bit	Description
31:28	**DDR SDRAM Throttle Mode (TMODE):** Four bits control which mechanisms for Throttling are enabled in an “OR” fashion. Counter-based Throttling is lower priority than Thermal Trips Throttling when both are enabled and Tripped. Counter-based trips point Throttling values and Thermal-based Trip Point Throttling values are specified in this register. 0000 = Throttling turned off. This is the default setting. All Counters are off. 0001 = Only GMCH Thermal Sensor based Throttling is enabled. If GMCH Thermal Sensor is Tripped, Write Throttling begins based on the setting in WTTC. 0010 = Only Rank Thermal Sensor based Throttling is enabled. When the external SO-DIMM Thermal sensor is Tripped, DDR SDRAM Throttling begins based on the setting in RTTC. 0011 = Both Rank and GMCH Thermal Sensor based throttling is enabled. When the external SO-DIMM Thermal Sensor is Tripped DDR SDRAM Throttling begins based on the setting in RTTC. If the GMCH Thermal Sensor is Tripped, Write Throttling begins based on the setting in WTTC. 0100 = Only the GMCH Write Counter mechanism is enabled. When the threshold set in the GDT field is reached, DDR SDRAM Throttling begins based on the setting in WCTC. 0101 = GMCH Thermal Sensor and GMCH Write DDR SDRAM Counter mechanisms are both enabled. If the GMCH Write DDR SDRAM Counter mechanism threshold is reached, DDR SDRAM Throttling begins based on the setting in WCTC. If the GMCH Thermal Sensor is tripped, DDR SDRAM Throttling begins based on the setting in WTTC. If both threshold mechanisms are tripped, the DDR SDRAM Throttling begins based on the settings in WTTC. 0110 = Rank Thermal Sensor and GMCH Write DDR SDRAM Counter mechanisms are both enabled. If the GMCH Write DDR SDRAM Counter mechanism threshold is reached, DDR SDRAM Throttling begins based on setting in WCTC. If the external SO-DIMM Thermal Sensor is tripped, Rank DDR SDRAM throttling begins based on the setting in RTTC.

Bit	Description
	0111 = Similar to 0101 for Writes and when the Rank Thermal Sensor is tripped, DDR SDRAM Throttling begins based on the setting in RTTC. 1000 = Only Rank Counter mechanism is enabled. When the threshold set in the GDT field is reached, DDR SDRAM Throttling begins based on the setting in RCTC. 1001 = Rank Counter mechanism is enabled and GMCH Thermal Sensor based throttling are both enabled. If GMCH Thermal Sensor is tripped, Write Throttling begins based on the setting in WTTC. When the threshold set in the GDT field is reached, DDR SDRAM Throttling begins based on the setting in RCTC. 1010 = Rank Thermal Sensor and Rank DDR SDRAM Counter mechanisms are both enabled. If the rank DDR SDRAM Counter mechanism threshold is reached, DDR SDRAM Throttling begins based on the setting in RCTC. If the external SO-DIMM Thermal Sensor is tripped, DRAM Throttling begins based on the setting in RTTC. 1011 = Similar to 1010 and if the GMCH Thermal Sensor is tripped, Write Throttling begins based on the setting in WTTC. 1111 = Rank and GMCH Thermal Sensor based Throttling and Rank and GMCH Write Counter based Throttling are enabled. If both the Write Counter and GMCH Thermal Sensor based mechanisms are tripped, DDR SDRAM Throttling begins based on the setting allowed in WTTC. If both the Rank Counter and Rank Thermal Sensor based mechanisms are tripped, DDR SDRAM Throttling begins based on the setting allowed in RTTC.
27:24	**Read Counter Based Power Throttle Control (RCTC):** These bits select the Counter based Power Throttle Bandwidth Limits for Read operations to system memory. R/W, RO if Throttle Lock. 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved

Bit	Description
23:20	**Write Counter Based Power Throttle Control (WCTC):** These bits select the counter based Power Throttle Bandwidth Limits for Write operations to system memory. R/W, RO if Throttle Lock 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved
19:16	**Read Thermal Based Power Throttle Control (RTTC):** These bits select the Thermal Sensor based Power Throttle Bandwidth Limits for Read operations to system memory. R/W, RO if Throttle Lock. 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved

Bit	Description
15:12	**Write Thermal Based Power Throttle Control (WTTC):** These bits select the Thermal based Power Throttle Bandwidth Limits for Write operations to system memory. R/W, RO if Throttle Lock 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved
11	**Counter Based Throttle Lock (CTLOCK):** This bit secures RCTC and WCTC. This bit defaults to 0. Once a 1 is written to this bit, RCTC and WCTC (including CTLOCK) become Read-Only.
10	**Thermal Throttle Lock (TTLOCK):** This bit secures the DDR SDRAM Throttling Control register. This bit defaults to 0. Once a 1 is written to this bit, all of the Configuration register bits in DTC (including TTLOCK) except CTLOCK, RCTC and WCTC become Read-Only.
9	**Thermal Power Throttle Control fields Enable:** 0 = RTTC and WTTC are not used. RCTC and WTCT are used for both Counter and Thermal based Throttling. 1 = RTTC and WTTC are used for Thermal based Throttling.
8	**High Priority Stream Throttling Enable:** Normally High Priority Streams are not Throttled when either the counter based mechanism or Thermal Sensor mechanism demands Throttling. 0 = Normal operation. 1 = Block High priority streams during Throttling.
7:0	**Global DDR SDRAM Sampling Window (GDSW):** This 8-bit value is multiplied by 4 to define the length of time in milliseconds (0–1020) over which the number of Octal Words (16 bytes) Read/Written is counted and Throttling is imposed. Note that programming this field to 00h disables system memory throttling. Recommended values are between 0.25 and 0.75 seconds.

3.9 Configuration Process Registers (Device #0, Function #3)

Table 33 summarizes all Device#0, Function #3 registers.

Table 33. Configuration Process Configuration Space (Device#0, Function #3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	00	01	8086h	RO
Device Identification	DID	02	03	3585h	RO
PCI Command	PCICMD	04	05	0006h	RO,R/W
PCI Status	PCISTS	06	07	0080h	RO,R/WC
Revision Identification	RID	08	08	01h 02h	RO
Sub-Class Code	SUBC	0A	0A	80h	RO
Base Class Code	BCC	0B	0B	08h	RO
Header Type	HDR	0E	0E	80h	RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	00h	RO
Strap Status	STRAP	A8	AB		RO
HPLL Clock Control	HPLLCC	C0	C1	00h	RO

3.9.1 VID – Vendor Identification Register (Device #0)

Address Offset: 00-01h
Default Value: 8086h
Access: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification (VID):** This register field contains the PCI standard identification for 8086h.

3.9.2 DID – Device Identification Register (Device #0)

Address Offset: 02-03h
Default Value: 3585h
Access: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number (DID):** This is a 16-bit value assigned to the GMCH/MCH Host-Hub Interface Bridge Function #3 (3585h).

3.9.3 PCICMD – PCI Command Register (Device #0)

Address Offset: 04-05h
Default Value: 0006h
Access: Read Only, Read/Write
Size: 16 bits

Since GMCH/MCH Device #0 does not physically reside on PCI_A, many of the bits are not implemented.

Bit	Description
15:10	**Reserved**
9	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back Write. Since Device #0 is strictly a target, this bit is not implemented and is hardwired to 0. Writes to this bit position have no effect.
8	**SERR Enable (SERRE):** SERR# is not implemented by Function #1 of Device #0 of the GMCH/MCH and this bit is hardwired to 0. Writes to this bit position have no effect.
7	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the GMCH/MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	**Parity Error Enable (PERRE):** PERR# is not implemented by GMCH/MCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5	**VGA Palette Snoop Enable (VGASNOOP):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	**Memory Write and Invalidate Enable (MWIE):** The GMCH/MCH will never issue Memory Write and Invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	**Special Cycle Enable (SCE):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	**Bus Master Enable (BME):** The GMCH/MCH is always enabled as a master on hub interface. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	**Memory Access Enable (MAE):** The GMCH/MCH always allows access to Main Memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	**I/O Access Enable (IOAE):** This bit is not implemented in the GMCH/MCH and is hardwired to a 0. Writes to this bit position have no effect.

3.9.4 PCISTS – PCI Status Register (Device #0)

Address Offset: 06-07h
Default Value: 0080h
Access: Read Only, Read/WriteClear
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #0's PCI Interface. Bit 14 is Read/Write clear. All other bits are Read Only. Since GMCH/MCH Device #0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Description
15	**Detected Parity Error (DPE):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	**Signaled System Error (SSE):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
13	**Received Master Abort Status (RMAS):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
12	**Received Target Abort Status (RTAS):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
11	**Signaled Target Abort Status (STAS):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
10:9	**DEVSEL Timing (DEVT):** These bits are hardwired to "00". Writes to these bit positions have no affect. Device #0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that the GMCH/MCH does not limit optimum DEVSEL timing for PCI_A.
8	**Master Data Parity Error Detected (DPD):** The GMCH/MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
7	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device #0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the GMCH does not limit the optimum setting for PCI_A.
6:5	**Reserved**
4	**Capability List (CLIST):** This bit is hardwired to 0 to indicate to the configuration software that this device/function does not implement new capabilities.
3:0	**Reserved**

3.9.5 RID – Revision Identification Register (Device #0)

Address Offset: 08h
Default Value: 02h
Access: Read Only
Size: 8 bits

This register contains the revision number of the GMCH/MCH. These bits are Read Only; Writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH/MCH. Intel 852GME = 02 Intel 852PM = 02

3.9.6 SUBC – Sub-Class Code Register (Device #0)

Address Offset: 0Ah
Default Value: 80h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the GMCH/MCH Device #0. This code is 80h indicating a peripheral device.

Bit	Description
7:0	**Sub-Class Code (SUBC):** This is an 8-bit value that indicates the category of Bridge into which GMCH/MCH falls. The code is 80h indicating other peripheral device.

3.9.7 BCC – Base Class Code Register (Device #0)

Address Offset: 0Bh
Default Value: 08h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the GMCH/MCH Device #0 Function #3. This code is 08h indicating a peripheral device.

Bit	Description
7:0	**Base Class Code (BASEC):** This is an 8-bit value that indicates the Base Class code for the GMCH/MCH. This code has the value 08h, indicating other peripheral device.

3.9.8 HDR – Header Type Register (Device #0)

Address Offset: 0Eh
Default Value: 80h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Description
7:0	**PCI Header (HDR):** This field always returns 80 to indicate that Device #0 is a multifunction device. If Functions other than #0 are disabled this field returns a 00 to indicate that the GMCH/MCH is a single function device with standard header layout. The default is 80 Reads and Writes to this location have no effect.

3.9.9 SVID – Subsystem Vendor Identification Register (Device #0)

Address Offset: 2C-2Dh
Default Value: 0000h
Access: Read/Write Once
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Description
15:0	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been Written once, it becomes Read Only.

3.9.10 ID – Subsystem Identification Register (Device #0)

Address Offset: 2E-2Fh
Default Value: 0000h
Access: Read/Write Once
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Description
15:0	**Subsystem ID (SUBID):** This field should be programmed during BIOS initialization. After it has been Written once, it becomes Read Only.

3.9.11 CAPPTR – Capabilities Pointer Register (Device #0)

Address Offset: 34h
Default Value: 00h
Access: Read Only
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Description
7:0	**Pointer to the offset of the first capability ID register block:** In this case there are no capabilities therefore these bits are hardwired to 00h to indicate the end of the capability-linked list.

3.9.12 STRAP – Strap Status (Device #0)

Address Offset: A8-ABh
Default Value:
Access: Read Only
Size: 32 bits

Bit	Description
31:27	**Reserved**
26	Clock Config: Bit_2
25	Clock Config: Bit_1
24	Clock Config: Bit_0
23:0	**Reserved**

3.9.13 HPLLCC – HPLL Clock Control Register (Device #0)

Address Offset: C0–C1h
Default Value: 00h
Access: Read Only
Size: 16 bits

Bit	Description
15:11	**Reserved**
10	**HPLL VCO Change Sequence Initiate Bit**: Software must Write a 0 to clear this bit and then Write a 1 to initiate sequence again.
9	**Hphase Reset Bit:** 1 = Assert 0 = Deassert (default)
8:2	**Reserved**
1:0	**HPLL Clock Control:** See the following tables below

Table 34. Intel 852GME GMCH and Intel 852PM MCH Configurations

Straps Read Through HPLLCC[2:0]: D0:F3:Register Offset C0-C1h, bits[2:0]	PSB Frequency	System Memory Frequency	GFX Core Clock – Low (Render Core Frequency only) Intel 852GME GMCH Only	GFX Core Clock – High (Render Core Frequency & Display Core Frequency) Intel 852GME GMCH Only
000	400 MHz	266 MHz	133 MHz	200 MHz
001	400 MHz	200 MHz	100 MHz	200 MHz
010	400 MHz	200 MHz	100 MHz	133 MHz
011	400 MHz	266 MHz	133 MHz	266 MHz
100	533 MHz	266 MHz	133 MHz	200 MHz
101	533 MHz	266 MHz	133 MHz	266 MHz
110	533 MHz	333 MHz	166 MHz	266 MHz
111	400 MHz	333 MHz	166 MHz	250 MHz

3.10 PCI to AGP Configuration Registers (Device #1, Function #0)

Table 35. Device 1 is the Virtual PCI to AGP bridge (Device #1, Function #0))

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	00	01	8086h	RO
Device Identification	DID	02	03	3581h	RO
PCI Command Register	PCICMD1	04	05	0000h	RO, R/W
PCI Status Register	PCISTS1	06	07	00A0h	RO, R/WC
Revision Identification	RID	08	08	01h 02h	RO
Sub-Class Code	SUBC1	0A	0A	04h	RO
Base Class Code	BCC1	0B	0B	06h	RO
Header Type	HDR1	0E	0E	01h	RO
Primary Bus Number	PBUSN1	18	18	00h	RO
Secondary Bus Number	SBUSN1	19	19	00h	R/W
Subordinate Bus Number	SUBUSN1	1A	1A	00h	R/W
Secondary Bus Master Latency Timer	SMLT1	1B	1B	00h	RO,R/W
I/O Base Address Register	IOBASE1	1C	1C	F0h	RO,R/W
I/O Limit Address Register	IOLIMIT1	1D	1D	00h	RO,R/W
Secondary Status Register	SSTS1	1E	1F	02A0h	RO,R/WC
Memory Base Address Register	MBASE1	20	21	FFF0h	RO,R/W
Memory Limit Address Register	MLIMIT1	22	23	0000h	RO,R/W
Prefetchable Memory Base Limit Address Reg.	PMBASE1	24	25	FFF0h	RO,R/W
Prefetchable Memory Limit Address Reg.	PMLIMIT1	26	27	0000h	RO,R/W

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Bridge Control Register	BCTRL1	3E	3E	00h	RO,R/W
Error Command Register	ERRCMD1	40	40	00h	RO,R/W

3.10.1 VID1 - Vendor Identification (Device #1)

Address Offset: 00h
Default Value: 8086h
Access: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number:** This is a 16-bit value assigned to Intel.

3.10.2 DID1 - Device Identification (Device #1)

Address Offset: 02h
Default Value: 3581h
Access: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number:** This is a 16-bit value assigned to the GMCH/MCH (3581h).

3.10.3 PCICMD1 - PCI Command Register (Device #1)

Address Offset: 04h
Default Value: 0000h
Access: Read Only, Read/Write
Size: 16 bits

Bit	Description
15:9	**Reserved**
8	**SERR Message Enable (SERRE):** This bit is a global enable bit for Device #1 SERR messaging. The GMCH/MCH communicates the SERR# condition by sending an SERR message to the ICH4-M. If this bit is set to a 1, the GMCH/MCH is enabled to generate SERR messages over hub interface for specific Device 1 error conditions that are individually enabled in the BCTRL1 register. The error status is reported in the PCISTS1 register. If SERRE1 is reset to 0, then the SERR message is not generated by the GMCH/MCH for Device #1.
7	**Address/Data Stepping (ADSTEP):** Address/data stepping is not implemented in the GMCH/MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6:5	**Reserved**
4	**Memory Write and Invalidate Enable (MWIE):** This bit is implemented as Read Only and returns a value of 0 when read.
3	**Special Cycle Enable (SCE):** This bit is implemented as Read Only and returns a value of 0 when read.
2	**Bus Master Enable (BME):** When the Bus Master Enabled is set to “0” (default), AGP Master initiated Frame# cycles will be ignored by the GMCH/MCH. The result is a master abort. Ignoring incoming cycles on the secondary side of the PCI to PCI bridge effectively disabled the bus master on the primary side. When 1, AGP master initiated Frame# cycles will be accepted by the GMCH/MCH if they hit a valid address decode range. This bit has no affect on AGP Master originated SBA or PIPE# cycles.
1	**Memory Access Enable (MAE):** This bit must be set to 1 to enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers. When set to 0 all of Device #1’s memory space is disabled.
0	**IO Access Enable (IOAE):** This bit must be set to1 to enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers. When set to 0 all of Device #1’s I/O space is disabled.

3.10.4 PCISTS1 - PCI Status Register (Device #1)

Address Offset: 06h
Default Value: 00A0h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS1 is a 16-bit status register that reports the occurrence of error conditions associated with the primary side of the "virtual" PCI to PCI bridge embedded within the GMCH/MCH.

Bit	Description
15	**Reserved**
14	**Signaled System Error (SSE):** This bit is set to 1 when GMCH/MCH Device#1 generates an SERR message over hub interface for any enabled Device #1 error condition. Device #1 error conditions are enabled in the ERRCMD, PCICMD1 and BCTRL registers. Device #1 error flags are read/reset from the ERRSTS and SSTS1 register. Software clears this bit by writing a 1 to it.
13:8	**Reserved**
7	**Fast Back-to-Back (FB2B):** Indicates that the AGP/PCI_B interface always supports fast back to back writes (set to 1).
6	**Reserved**
5	**66/60 MHz capability (CAP66):** Since the AGP/PCI bus is 66 MHz capable (set to 1).
4:0	**Reserved**

3.10.5 RID - Revision Identification (Device #1)

Address Offset: 08h
Default Value: 02h
Access: Read Only
Size: 8 bits

This register contains the revision number of the GMCH device #1. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number:** This is an 8-bit value that indicates the revision identification number for the GMCH/MCH. Intel 852GME = 02 Intel 852PM = 02

3.10.6 SUBC1 - Sub-Class Code (Device #1)

Address Offset: 0Ah
Default Value: 04h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the GMCH/MCH Device #1. This code is 04h indicating a PCI to PCI Bridge device.

Bit	Description
7:0	**Sub-Class Code (SUBC):** This is an 8-bit value that indicates the category of Bridge into which the Device #1 of the GMCH/MCH falls. The code is 04h indicating a PCI to PCI bridge.

3.10.7 BCC1 - Base Class Code (Device #1)

Address Offset: 0Bh
Default Value: 06h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the GMCH/MCH Device #1. This code is 06h indicating a Bridge device.

Bit	Description
7:0	**Base Class Code (BASEC):** This is an 8-bit value that indicates the Base Class Code for the GMCH device #1. This code has the value 06h, indicating a Bridge device.

3.10.8 HDR1 - Header Type (Device #1)

Address Offset: 0Eh
Default Value: 01h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Description
7:0	**Header Type Register (HDR):** This read only field always returns 01 to indicate that GMCH/MCH Device #1 is a single function device with bridge header layout. Writes to this location have no effect.

3.10.9 PBUSN1 - Primary Bus Number (Device #1)

Address Offset: 18h
Default Value: 00h
Access: Read Only
Size: 8 bits

This register identifies that “virtual” PCI to PCI bridge is connected to bus #0.

Bit	Description
7:0	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since Device #1 is an internal device and its primary bus is always 0.

3.10.10 SBUSN1 - Secondary Bus Number (Device #1)

Address Offset: 19h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the “virtual” PCI to PCI bridge i.e. to PCI_B/AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI_B/AGP.

Bit	Description
7:0	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI_B.

3.10.11 SUBUSN1 - Subordinate Bus Number (Device #1)

Address Offset: 1Ah
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI_B/AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI_B/AGP.

Bit	Description
7:0	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the Device #1 bridge. When only a single PCI device resides on the AGP/PCI_B segment, this register will contain the same value as the SBUSN1 register.

3.10.12 SMLT1 - Secondary Bus Master Latency Timer (Device #1)

Address Offset: 1Bh
Default Value: 00h
Access: Read Only, Read/Write
Size: 8 bits

This register controls the bus tenure of the GMCH/MCH on AGP/PCI the same way Device#0 MLT controls the access to the PCI_A bus.

Bit	Description
7:3	**Secondary MLT Counter Value (MLT):** Programmable, default = 0 (SMLT disabled)
2:0	**Reserved**

3.10.13 IOBASE1 - I/O Base Address Register (Device #1)

Address Offset: 1Ch
Default Value: F0h
Access: Read Only, Read/Write
Size: 8 bits

This register controls the CPU to PCI_B/AGP I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4-kB boundary.

Bit	Description
7:4	**I/O Address Base (IOBASE):** Corresponds to A[15:12] of the I/O addresses passed by bridge 1 to AGP/PCI_B.
3:0	**Reserved**

3.10.14 IOLIMIT1 - I/O Limit Address Register (Device #1)

Address Offset: 1Dh
Default Value: 00h
Access: Read Only, Read/Write
Size: 8 bits

This register controls the CPU to PCI_B/AGP I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4KB aligned address block.

Bit	Description
7:4	**I/O Address Limit (IOLIMIT):** Corresponds to A[15:12] of the I/O address limit of Device #1. Devices between this upper limit and IOBASE1 will be passed to AGP/PCI_B.
3:0	**Reserved**

3.10.15 SSTS1 - Secondary Status Register (Device #1)

Address Offset: 1Eh
Default Value: 02A0h
Access: Read Only, Read/Write Clear
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with a secondary side (i.e. PCI_B/AGP side) of the "virtual" PCI to PCI bridge embedded within GMCH/MCH.

Bit	Description
15	**Detected Parity Error (DPE):** This bit is set to a 1 to indicate GMCH/MCH's detection of a parity error in the address or data phase of PCI_B/AGP bus transactions. Software sets DPE1 to 0 by writing a 1 to this bit.
14	**Reserved**
13	**Received Master Abort Status (RMAS):** When the GMCH/MCH terminates a Host to PCI_B/AGP with an unexpected master abort, this bit is set to 1. Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS):** When a GMCH/MCH -initiated transaction on PCI_B/AGP is terminated with a target abort, RTAS1 is set to 1. Software resets RTAS1 to 0 by writing a 1 to it.
11	**Reserved**
10:9	**DEVSEL# Timing (DEVT):** This 2-bit field indicates the timing of the DEVSEL# signal when the GMCH/MCH responds as a target on PCI_B/AGP, and is hard-wired to the value 01b (medium) to indicate the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle.
8	**Reserved**
7	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1, since GMCH/MCH as a target supports fast back-to-back transactions on PCI_B/AGP.
6	**Reserved**
5	**66/60 MHz capability (CAP66):** The AGP/PCI_B bus is capable of 66Mhz operation (Set to 1)
4:0	**Reserved**

3.10.16 MBASE1 - Memory Base Address Register (Device #1)

Address Offset: 20h
Default Value: FFF0h
Access: Read Only, Read/Write
Size: 16 bits

This register controls the CPU to PCI_B non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1MB boundary.

Bit	Description
15:4	**Memory Address Base (MBASE):** Corresponds to A[31:20] of the lower limit of the memory range that will be passed by the Device #1 bridge to AGP/PCI_B.
3:0	**Reserved**

3.10.17 MLIMIT1 - Memory Limit Address Register (Device #1)

Address Offset: 22h
Default Value: 0000h
Access: Read Only, Read/Write
Size: 16 bits

This register controls the CPU to PCI_B non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block. NOTE: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI_B/AGP address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved CPU-AGP memory access performance.

Bit	Description
15:4	**Memory Address Limit (MLIMIT):** Corresponds to A[31:20] of the memory address that corresponds to the upper limit of the range of memory accesses that will be passed by the device 1 bridge to AGP/PCI_B.
3:0	**Reserved**

3.10.18 PMBASE1 - Prefetchable Memory Base Address Reg (Device #1)

Address Offset: 24h
Default Value: FFF0h
Access: Read Only, Read/Write
Size: 16 bits

This register controls the CPU to PCI_B prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE=< address =<PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Description
15:4	**Prefetchable Memory Address Base (PMBASE):** Corresponds to A[31:20] of the lower limit of the address range passed by bridge device 1 across AGP/PCI_B.
3:0	**Reserved**

3.10.19 PMLIMIT1 - Prefetchable Memory Limit Address Reg (Device #1)

Address Offset: 26h
Default Value: 0000h
Access: Read Only, Read/Write
Size: 16 bits

This register controls the CPU to PCI_B prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE=< address =<PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e. prefetchable) from the CPU perspective.

Bit	Description
15:4	**Prefetchable Memory Address Limit (PMLIMIT):** Corresponds to A[31:20] of the upper limit of the address range passed by bridge Device #1 across AGP/PCI_B.
3:0	**Reserved**

3.10.20 BCTRL - Bridge Control Register (Device #1)

Address Offset: 3Eh
Default Value: 00h
Access: Read Only, Read/Write
Size: 8 bits

This register provides extensions to the PCICMD1 register that are specific to PCI to PCI bridges. The BCTRL provides additional control for the secondary interface (i.e. PCI_B/AGP) as well as some bits that affect the overall behavior of the "virtual" PCI to PCI bridge embedded within GMCH/MCH, e.g. VGA compatible address ranges mapping.

Bit	Description
7:6	**Reserved**
5	**Master Abort Mode (MAMODE):** This means when acting as a master on AGP/PCI_B the GMCH/MCH will drop writes on the floor and return all 1s during reads when a Master Abort occurs (Set to 1).
4	**Reserved**
3	**VGA Enable (VGAEN):** This bit controls the routing of CPU initiated transactions targeting VGA compatible I/O and memory address ranges. When this bit is **set**, the GMCH will forward the following CPU accesses to the AGP: 1) memory accesses in the range 0A0000h to 0BFFFFh 2) I/O addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases - A[15:10] are not decoded) When this bit is **set**, forwarding of these accesses issued by the CPU is independent of the I/O address and memory address ranges defined by the previously defined base and limit registers. Forwarding of these accesses is also independent of the settings of the bit 2 (ISA Enable) of this register if this bit is "**1**". If the VGA enable bit is **set**, then accesses to IO address range x3BCh-x3BFh are forwarded to hub interface. If the VGA enable bit is **not set**, then accesses to IO address range x3BCh-x3BFh are treated just like any other IO accesses, i.e. the cycles are forwarded to AGP if the address is within IOBASE and IOLIMIT and ISA enable bit is not set, otherwise they are forwarded to hub interface. If this bit is **"0" (default)**, then VGA compatible memory and I/O range accesses are not forwarded to AGP. but rather they are mapped to primary PCI unless they are mapped to AGP via I/O and memory range registers defined above (IOBASE, IOLIMIT, MBASE, MLIMIT, PMBASE, PMLIMIT) The following table shows the behavior for all combinations of MDA and VGA: **VGA** / **MDA** / **Behavior** 0 / 0 / All References to MDA and VGA Go To hub interface (Default) 0 / 1 / Reserved 1 / 0 / All References To VGA Go to AGP. MDA-only references (I/O Address 3BF and aliases) will go to hub interface. 1 / 1 / VGA References go to AGP; MDA references go to hub interface

Bit	Description
2	**ISA Enable (ISAEN):** Modifies the response by the GMCH/MCH to an I/O access issued by the CPU that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. When this bit is set to 1, GMCH/MCH will not forward to PCI_B/AGP any I/O transactions addressing the last 768 bytes in each 1KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI_B/AGP these cycles will be forwarded to hub interface where they can be subtractively or positively claimed by the ISA bridge. If this bit is 0 (default) then all addresses defined by the IOBASE and IOLIMIT for CPU I/O transactions will be mapped to PCI_B/AGP.
1	**Reserved**
0	**Parity Error Response Enable (PEREN):** Controls GMCH/MCH's response to data phase parity errors on PCI_B/AGP. G_PERR# is not implemented by the GMCH/MCH. However, when this bit is set to 1, address and data parity errors detected on PCI_B are reported via the HI SERR messaging mechanism, if further enabled by SERRE1. If this bit is reset to 0, then address and data parity errors on PCI_B/AGP are not reported via the GMCH/MCH hub interface SERR messaging mechanism. Other types of error conditions can still be signaled via SERR messaging independent of this bit's state.

The bit field definitions for VGAEN and MDAP are detailed in the following table.

VGAEN: MDAP	Description
0 0	All References to MDA and VGA space are routed to hub interface.
0 1	Illegal combination
1 0	All VGA references are routed to this bus. Exclusive MDA references are routed to hub interface.
1 1	All VGA references are routed to this bus. All MDA references are routed to hub interface.

3.10.21 ERRCMD1 - Error Command Register (Device #1)

Address Offset: 40h
Default Value: 00h
Access: Read Only, Read/Write
Size: 8 bits

Bit	Description
7:1	**Reserved**
0	**SERR on Receiving Target Abort (SERTA):** When this bit is 1 the GMCH/MCH generates an SERR message over hub interface upon receiving a target abort on PCI_B. When this bit is set to 0, the GMCH/MCH does not assert an SERR message upon receipt of a target abort on PCI_B. SERR messaging for Device #1 is globally enabled in the PCICMD1 register.

3.11 Intel 852GME GMCH Integrated Graphics Device Registers (Device #2, Function #0)

This section contains the PCI configuration registers listed in order of ascending offset address. Device #2 incorporates Function #0.

Note: C0F0 = Copy of Function #0 and U1F1 = Unique in Function #1.

Table 36. Integrated Graphics Device Configuration Space (Device #2, Function#0)

Register Name	Register Symbol	Address Offset	Register End	Default Value	Access	Regs in Function#1
Vendor Identification	VID	00h	01h	8086h	RO	C0F0
Device Identification	DID	02h	03h	3582h	RO	C0F0
PCI Command	PCICMD	04h	05h	0000h	RO,R/W	U1F1
PCI Status	PCISTS	06h	07h	0090h	RO	U1F1
Revision Identification	RID	08h	08h	01h 02h	RO	C0F0
Class Code	CC	09h	0Bh	030000h	RO	U1F1
Cache Line Size	CLS	0Ch	0Ch	00h	RO	C0F0
Master Latency Timer	MLT	0Dh	0Dh	00h	RO	C0F0
Header Type	HDR	0Eh	0Eh	00h	RO	C0F0
Graphics Memory Range Address	GMADR	10h	13h	00000008h	RO,R/W	U1F1
Memory Mapped Range Address	MMADR	14h	17h	00000000h	RO,R/W	U1F1
IO Range	IOBAR	18h	1Bh	00000001h	RO,R/W	—
Subsystem Vendor ID	SVID	2Ch	2Dh	0000h	R/WO	C0F0
Subsystem ID	SID	2Eh	2Fh	0000h	R/ WO	C0F0
Video Bios ROM Base Address	ROMADR	30h	33h	00000000h	RO	C0F0
Interrupt Line	INTRLINE	3Ch	3Ch	00h	RO in F #1,R/W	—
Interrupt Pin	INTRPIN	3Dh	3Dh	01h	RO, Reserved In F#1	—
Minimum Grant	MINGNT	3Eh	3Eh	00h	RO	C0F0
Maximum Latency	MAXLAT	3Fh	3Fh	00h	RO	C0F0

Register Name	Register Symbol	Address Offset	Register End	Default Value	Access	Regs in Function#1
Power Management Capabilities	PMCAP	D2h	D3h	0221h	RO	C0F0
Power Management Control	PMCS	D4h	D5h	0000h	RO,R/W	U1F1
SWSMI Register	SWSMI	E0h	E1h	0000h	R/W	
Thermal INTR Command Register	TINTRCMD	Efh	EFh	00h	R/W	
GMCH Clock Control Register	GCCC	F0h	F1h	0000h	R/W	

3.11.1 VID – Vendor Identification Register (Device #2)

Address Offset: 00–01h
Default Value: 8086h
Access Attributes: Read Only
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number:** This is a 16-bit value assigned to Intel.

3.11.2 DID – Device Identification Register (Device #2)

Address Offset: 02–03h
Default Value: 3582h
Access Attributes: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number:** This is a 16-bit value assigned to the GMCH IGD (3582h).

3.11.3 PCICMD – PCI Command Register (Device #2)

Address Offset: 04–05h
Default: 0000h
Access: Read Only, Read/Write
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD register in the IGD disables the IGD PCI compliant master accesses to Main System memory.

Bit	Description
15:10	**Reserved**
9	**Fast Back-to-Back (FB2B)—RO**.
8	**SERR# Enable (SERRE) —RO**
7	**Address/Data Stepping—RO**
6	**Parity Error Enable (PERRE) —RO**
5	**Video Palette Snooping (VPS) —RO**
4	**Memory Write and Invalidate Enable (MWIE) —RO**
3	**Special Cycle Enable (SCE) —RO**
2	**Bus Master Enable (BME) —R/W:** This bit determines if the IGD is to function as a PCI compliant master. 0= Disable IGD bus mastering (default). 1 = Enable IGD bus mastering.
1	**Memory Access Enable (MAE) —R/W:** This bit controls the IGD's response to system memory space accesses. 0= Disable (default). 1 = Enable.
0	**I/O Access Enable (IOAE) —R/W:** This bit controls the IGD's response to I/O Space accesses. 0 = Disable (default). 1 = Enable.

3.11.4 PCISTS – PCI Status Register (Device #2)

Address Offset: 06–07h
Default Value: 0090h
Access: Read Only
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Description
15	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always set to 0.
14	**Signaled System Error (SSE) – RO**
13	**Received Master Abort Status (RMAS) – RO**
12	**Received Target Abort Status (RTAS) – RO**
11	**Signaled Target Abort Status (STAS) – RO**
10:9	**DEVSEL# Timing (DEVT) – RO**
8	**Data Parity Detected (DPD) – RO**
7	**Fast Back-to-Back (FB2B) – RO**
6	**User Defined Format (UDF) – RO**
5	**66-MHz PCI Capable (66C) – RO**
4	**CAP LIST:** This bit is set to 1 to indicate that the register at 34h provides an offset into the Function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3:0	**Reserved**

3.11.5 RID – Revision Identification Register (Device #2)

Address Offset: 08h
Default Value: 02h
Access: Read Only
Size: 8 bits

This register contains the revision number of the IGD. These bits are Read Only and Writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number:** This is an 8-bit value that indicates the revision identification number for the GMCH. Intel 852GME = 02 Intel 852PM = 02

3.11.6 CC – Class Code Register (Device #2)

Address Offset: 09–0Bh
Default Value: 030000h
Access: Read Only
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class code and Base Class code definition for the IGD. This register also contains the Base Class code and the function sub-class in relation to the Base Class code.

Bit	Description
23:16	**Base Class Code (BASEC):** 03=Display controller
15:8	**Sub-Class Code (SCC):** Function 0: 00h=VGA compatible or 80h=Non VGA Function 1: 80h=Non VGA
7:0	**Programming Interface (PI):** 00h=Hardwired as a Display controller.

3.11.7 CLS – Cache Line Size Register (Device #2)

Address Offset: 0Ch
Default Value: 00h
Access: Read only
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Description
7:0	**Cache Line Size (CLS) – RO**

3.11.8 MLT – Master Latency Timer Register (Device #2)

Address Offset: 0Dh
Default Value: 00h
Access: Read Only
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Description
7:0	**Master Latency Timer Count Value – RO**

3.11.9 HDR – Header Type Register (Device #2)

Address Offset: 0Eh
Default Value: 00h
Access: Read Only
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Description
7	**Multi Function Status (MFunc):** Indicates if the device is a multi-function device.
6:0	**Header Code (H):** This is a 7-bit value that indicates the Header code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

3.11.10 GMADR – Graphics Memory Range Address Register (Device #2)

Address Offset: 10–13h
Default Value: 00000008h
Access: Read/Write, Read Only
Size: 32 bits

IGD graphics system memory base address is specified in this register.

Bit	Description
31:27	**Memory Base Address—R/W:** Set by the OS, these bits correspond to address signals [31:26].
26	**128-MB Address Mask – RO:** 0 indicates 128-MB address
25:4	**Address Mask—RO:** Indicates (at least) a 32-MB address range.
3	**Prefetchable Memory—RO:** Enable prefetching.
2:1	**Memory Type—RO:** Indicate 32-bit address.
0	**Memory/IO Space—RO:** Indicate system memory space.

3.11.11 MMADR – Memory Mapped Range Address Register (Device #2)

Address Offset: 14–17h
Default Value: 00000000h
Access: Read/Write, Read Only
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512-kB and the base address is defined by bits [31:19].

Bit	Description
31:19	**Memory Base Address—R/W:** Set by the OS, these bits correspond to address signals [31:19].
18:4	**Address Mask—RO:** Indicate 512-kB address range.
3	**Prefetchable Memory—RO:** Prevents prefetching.
2:1	**Memory Type—RO:** Indicates 32-bit address.
0	**Memory / IO Space—RO:** Indicates system memory space.

3.11.12 IOBAR – I/O Base Address Register (Device #2)

Address offset: 18-1Bh
Default: 00000001h
Access: Read/Write
Size: 16-bits

This register provides the Base offset of the I/O registers within Device #2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16-bit I/O Address Space. Bits 2:1 are fixed and return zero, bit 0 is hardwired to a one indicating that 8-bytes of I/O space are decoded.

Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if internal graphics is disabled. Note that access to this IO BAR is independent of VGA functionality within Device #2.

If accesses to this I/O bar are allowed, then the GMCH claims all 8-bit, 16-bit, or 32-bit I/O cycles from the CPU that falls within the 8B claimed.

Bit	Description
31:16	**Reserved**
15:3	**IO Base Address—R/W:** Set by the OS, these bits correspond to address signals [15:3].
2:1	**Memory Type—RO:** Indicates 32-bit address.
0	**Memory / IO Space—RO**

3.11.13 SVID – Subsystem Vendor Identification Register (Device #2)

Address Offset: 2C–2Dh
Default Value: 0000h
Access: Read/Write Once
Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID:** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a reset.

3.11.14 SID – Subsystem Identification Register (Device #2)

Address Offset: 2E–2Fh
Default Value: 0000h
Access: Read/Write Once
Size: 16 bits

Bit	Description
15:0	**Subsystem Identification:** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a reset.

3.11.15 ROMADR – Video BIOS ROM Base Address Registers (Device #2)

Address Offset: 30–33h
Default Value: 00000000h
Access: Read Only
Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0's.

Bit	Description
31:18	**ROM Base Address—RO**
17:11	**Address Mask—RO:** Indicates 256-kB address range.
10:1	**Reserved**
0	**ROM BIOS Enable—RO:** Indicates ROM not accessible.

3.11.16 INTRLINE—Interrupt Line Register (Device #2)

Address Offset: 3Ch
Default Value: 00h
Access: Read/Write
Size: 8 bits

Bit	Description
7:0	**Interrupt Connection:** Used to communicate interrupt line routing information. POST software Writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the System Interrupt controller that the device's interrupt pin is connected to.

3.11.17 INTRPIN—Interrupt Pin Register (Device #2)

Address Offset: 3Dh
Default Value: 01h
Access: Read Only
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin:** As a single function device, the IGD specifies INTA# as its interrupt pin. 01h=INTA#. For Function #1, this register is set to 00h.

3.11.18 MINGNT – Minimum Grant Register (Device #2)

Address Offset: 3Eh
Default Value: 00h
Access: Read Only
Size: 8 bits

Bit	Description
7:0	**Minimum Grant Value:** The IGD does not burst as a PCI compliant master.

3.11.19 MAXLAT – Maximum Latency Register (Device #2)

Address Offset: 3Fh
Default Value: 00h
Access: Read Only
Size: 8 bits

Bit	Description
7:0	**Maximum Latency Value:** Bits[7:0]=00h. The IGD has no specific requirements for how often it needs to access the PCI bus.

3.11.20 PMCAP – Power Management Capabilities Register (Device #2)

Address Offset: D2h–D3h
Default Value: 0221h
Access: Read Only
Size: 16 bits

Bit	Description
15:11	**PME Support:** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10:6	**Reserved**
5	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	**Auxiliary Power Source:** Hardwired to 0.
3	**PME Clock:** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	**Version:** Hardwired to 001b to indicate there are 4 bytes of power management registers implemented.

3.11.21 PMCS – Power Management Control/Status Register (Device #2)

Address Offset: D4h–D5h
Default Value: 0000h
Access: Read/Write, Read Only
Size: 16 bits

Bit	Description
15	**PME_Status —RO:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:9	**Reserved**
8	**PME_En—RO:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	**Reserved**
1:0	**PowerState—R/W:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to Write an unsupported state to this field, Write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally Reset to initial values. **Bits[1:0] Power State** 00 D0 Default 01 D1 10 D2 Not Supported 11 D3

3.11.22 GCCC — GMCH Clock Control Register

Address Offset: F0–F1h
Default Value: 00 00h
Access: Read/Write
Size: 16 bits

Bit	Description
15:10	**Reserved**
9	**Core Display Clock Gate Control (CD-Gate):** 0 = Core Display Clock Trunk not Gated, Clock running to the Core. 1 = Core Display Clock Trunk Gated, Clock not running to the Core.
8	**Core Render Clock Gate Control (CR-Gate):** 0 = Core Render Clock Trunk not Gated, clock running to the core. 1 = Core Render Clock Trunk Gated, clock not running to the core.
7	**Reserved**
6	**Core Display Clock Control (CDCC):** 0 = Core Display Clock = Core High Clock (CH). 1 = Core Display Clock = Core Low Clock (CL). **NOTE:** This bit can be set to a 1 only when CRCC is set to 01. Setting this to a 1'with any other combination of CRCC can cause irrecoverable failures. Gate both core Render and Display Clocks using CR Gate and CD Gate Registers, then change the value of CDCC Register and update CR Gate and CD Gate to re-enable the Clocks.
5:4	**Core Render Clock Control (CRCC):** 00 = Core Render Clock = Core High Clock (CH). 01 = Core Render Clock = Core Low Clock (CL). 10 = Reserved 11 = Reserved **NOTE:** CRCC defaults to 00 (CH) and only certain transitions are allowed. 00 → 01 01 → 00 Gate Core Render Clock using CR Gate Register, then change the value of CRCC Register and update CR Gate to re-enable the Clock.
3:0	**Reserved**

4 System Address Map

A system based on the GMCH/MCH supports 4 GB of addressable system memory space and 64-kB+3 B of addressable I/O space. The I/O and system memory spaces are divided by system configuration software into regions. The system memory ranges are useful either as system memory or as specialized system memory, while the I/O regions are used solely to control the operation of devices in the system.

When the GMCH/MCH receives a Write request whose address targets an invalid space, the data is ignored. For Reads, the GMCH/MCH responds by returning all zeros on the requesting interface.

There is a programmable memory address space under the 1-MB region which is divided into regions which can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only. Attribute programming is described in the Register Description section. This section focuses on how the memory space is partitioned and how the separate memory regions are used. I/O address space has simpler mapping and is explained at the end of this section.

The GMCH/MCH claims any CPU access over 4 GB and terminates the transaction without forwarding it to hub interface or AGP (Intel 852GME GMCH and Intel 852PM MCH only). Simply dropping the data terminates writes and for reads the GMCH/MCH return all zeros on the host bus.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the hub interface/PCI. The exception to this rule is VGA ranges, which may be mapped to AGP or to the internal graphics device (IGD). In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the hub interface/PCI, while cycle descriptions referencing AGP or IGD are related to the AGP bus or the internal graphics device respectively.

The GMCH/MCH Memory Map includes a number of programmable ranges. All of these ranges must be unique and non-overlapping. There are no Hardware Interlocks to prevent problems in the case of overlapping ranges. Accesses to overlapped ranges may produce indeterminate results.

4.1 System Memory Address Ranges

The Intel 852GME GMCH and Intel 852PM MCH provide a maximum system memory of 2 GB. The GMCH/MCH does not re-map APIC memory space and does not limit DDR SDRAM space in hardware.

It is the BIOS or system designer's responsibility to limit system memory population so that adequate PCI, AGP, High BIOS and APIC memory space can be allocated.

The figures below depict the system memory address map in a simplified form and provide details on mapping specific system memory regions as defined and supported by the GMCH/MCH.

Figure 7. Simplified View of Intel 852GME GMCH and Intel 852PM MCH System Address Map

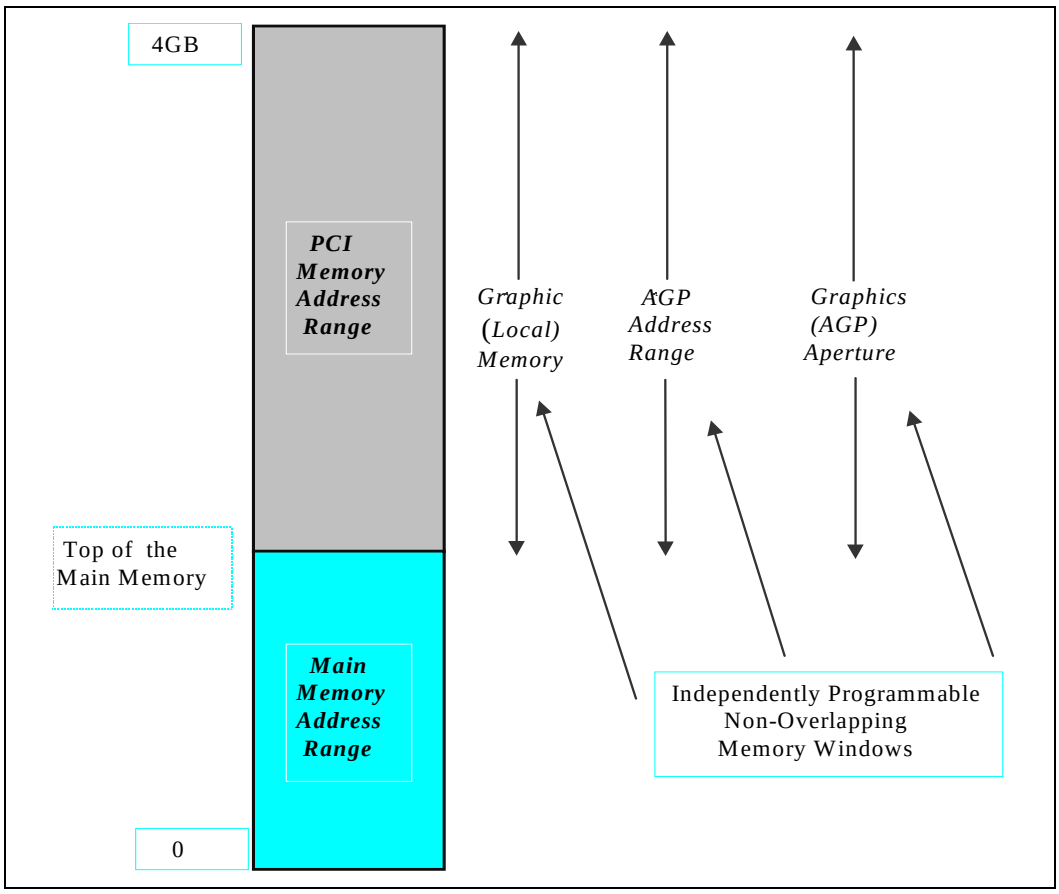
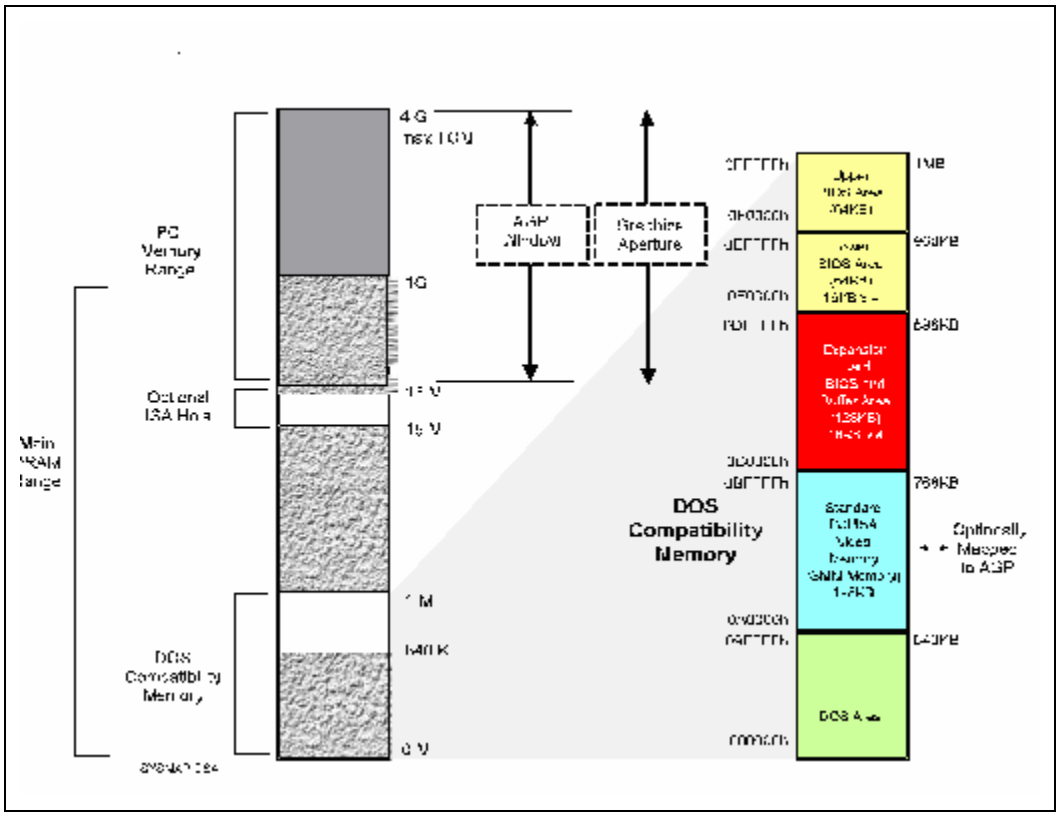


Figure 8. Detailed View of the Intel 852GME GMCH and Intel 852PM MCH System Address Map



4.2 DOS* Compatibility Area

This compatibility region is divided into the following address regions:

- Source synchronous 0 - 640 kB DOS Area
- 640 – 768 kB Video Buffer Area
- 768 - 896 kB in 16-kB sections (total of eight sections) - Expansion Area
- 896 –960 kB in 16-kB sections (total of four sections) - Extended System BIOS Area
- 960 kB - 1 MB System BIOS area

There are 16 system memory segments in the compatibility area. Thirteen of the system memory ranges can be enabled or disabled independently for both Read and Write cycles.

Table 37. System Memory Segments and Their Attributes

System Memory Segments	Attributes	Comments
000000H - 09FFFFH	Fixed - always mapped to main DDR SDRAM	0 to 640 kB – DOS Region
0A0000H - 0BFFFFH	Mapped to hub interface, AGP or IGD - configurable as SMM space	Video Buffer (physical DDR SDRAM configurable as SMM space)
0C0000H - 0C3FFFH	WE(Write Enable) RE (Read Enable)	Add-on BIOS
0C4000H - 0C7FFFH	WE RE	Add-on BIOS
0C8000H - 0CBFFFH	WE RE	Add-on BIOS
0CC000H - 0CFFFFH	WE RE	Add-on BIOS
0D0000H - 0D3FFFH	WE RE	Add-on BIOS
0D4000H - 0D7FFFH	WE RE	Add-on BIOS
0D8000H - 0DBFFFH	WE RE	Add-on BIOS
0DC000H - 0DFFFFH	WE RE	Add-on BIOS
0E0000H - 0E3FFFH	WE RE	BIOS Extension
0E4000H - 0E7FFFH	WE RE	BIOS Extension
0E8000H - 0EBFFFH	WE RE	BIOS Extension
0EC000H - 0EFFFFH	WE RE	BIOS Extension
0F0000H - 0FFFFFH	WE RE	BIOS Area

DOS Area (000000h-09FFFFh)

The DOS* area is 640 kB in size and is always mapped to the main system memory controlled by the GMCH/MCH.

Legacy VGA Ranges (0A0000h-0BFFFFh)

The legacy 128-kB VGA memory range 0A0000h-0BFFFFh (VGA Frame Buffer) can be mapped to IGD (Device #2), to AGP/PCI1 (Device#1) and to the hub interface depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the GMCH/MCH always decodes internally mapped devices first. Internal to the GMCH/MCH, decode precedence is always given to IGD. The GMCH/MCH always positively decodes internally mapped devices, namely the IGD and the AGP/PCI1. Subsequent decoding of regions mapped to the AGP/PCI1 or the hub interface depends on the Legacy VGA configurations bits (VGA Enable and MDAP). This region is also the default for SMM space.

Compatible SMRAM Address Range (0A0000h-0BFFFFh)

When compatible SMM space is enabled, SMM-mode CPU accesses to this range are routed to physical DDR SDRAM at this address. Non-SMM-mode CPU accesses to this range are considered to be to the video buffer area as described above. AGP and hub interface originated cycles to enabled SMM space are not allowed and are considered to be to the video buffer area if

IGD is not enabled. AGP cycles are allowed to master abort and hub interface writes are forwarded to AGP; hub interface reads are handled as invalid cycles. If IGD is enabled, all hub interface accesses are handled as invalid and AGP accesses are handled as invalid cycles.

Monochrome Display Adapter (MDA) Range (0B0000h - 0B7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, AGP/PCI1 and the hub interface (depending on configuration bits). Since the monochrome adapter may be mapped to any one of these devices, the GMCH/MCH must decode cycles in the MDA range and forward them either to IGD, AGP/PCI1 or to hub interface. This capability is controlled by VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the system memory range B0000h to B7FFFh, the GMCH/MCH decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3Bah, and 3BFh and forwards them to the either the IGD, AGP/PCI1 or the hub interface.

Expansion Area (0C0000h-0DFFFFh)

This 128-kByte ISA Expansion region is divided into eight, 16-kB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through GMCH/MCH and are subtractively decoded to ISA space. System memory that is disabled is not re-mapped.

Extended System BIOS Area (0E0000h-0EFFFFh)

This 64-kB area is divided into four, 16-kB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DDR SDRAM or to hub interface. Typically, this area is used for RAM or ROM. System memory segments that are disabled are not re-mapped elsewhere.

System BIOS Area (0F0000h-0FFFFFh)

This area is a single 64-kB segment. This segment can be assigned Read and Write attributes. It is by default (after Reset) Read/Write disabled and cycles are forwarded to hub interface. By manipulating the Read/Write attributes, the GMCH/MCH can “shadow” BIOS into the main DDR SDRAM. When disabled, this segment is not re-mapped.

4.3 Extended System Memory Area

This system memory area covers 100000h (1-MB) to FFFFFFFFh (4 GB-1B) address range and it is divided into the following regions:

- Main system memory from 1-MB to the top of system memory
- AGP or PCI Memory space from the top of system memory to 4-GB with two specific ranges
- APIC Configuration Space from FEC0_0000h (4 GB-20 MB) to FECF_FFFFh (4 GB-19 MB - 1) and FEE0_0000h (4 GB-18 MB) to FEEF_FFFFh (4 GB-17 MB-1B)
- High BIOS area from 4-GB to 4-GB – 2-MB

4.4 Main System Memory Address Range (0010_0000h to Top of Main Memory)

The address range from 1-MB to the top of main system memory is mapped to main DDR SDRAM address range controlled by the GMCH/MCH. The GMCH/MCH will forward all accesses to addresses within this range to the DDR SDRAM unless a hole in this range is created using the fixed hole as controlled by the FDHC register. Accesses within this hole are forwarded to hub interface.

The GMCH/MCH provides a maximum DDR SDRAM address decode space of 4 -GB. The GMCH/MCH does not re-map APIC memory space. The GMCH/MCH does not limit DDR SDRAM address space in hardware.

4.4.1 15 MB - 16 MB Window

A hole can be created at 15 MB-16 MB as controlled by the fixed hole enable (FDHC register) in Device 0 space. Accesses within this hole are forwarded to the hub interface. The range of physical DDR SDRAM disabled by opening the hole is not re-mapped to the top of the memory – that physical DDR SDRAM space is not accessible. This 15 MB-16 MB hole is an optionally enabled ISA hole. Video accelerators originally used this hole. Validation and customer SV teams also use it for some of their test cards and that is why it is being supported. There is no inherent BIOS request for the 15 MB-16 MB hole.

4.4.2 Pre-allocated System Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOM) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of the BIOS to properly initialize these regions**. The number of UMA options has been extended. Allocation is at a fixed address in terms of rigid positioning of UMA system memory →TOM-TSEG-UMA (size), but it is mapped at any available address by a PCI allocation algorithm. GMADR and MMADR are requested through BARs.

The following table details the location and attributes of the regions. Enabling/Disabling these ranges are described in the Control Register Device #0: GCC.

Table 38. Pre-allocated System Memory

System Memory Segments	Attributes	Comments
00000000H - 03E7FFFFH	R/W	Available system memory 62.5 -MB
03E80000H - 03F7FFFFH	R/W	Pre-allocated Graphics VGA memory 1 MB (or 4/8/16/32- MB) when IGD is enabled
03F80000H - 03FFFFFFH	SMM Mode Only - CPU Reads	TSEG Address Range
03F80000H - 03FFFFFFH	SMM Mode Only - CPU Reads	TSEG Pre-allocated system memory

4.4.2.1 Extended SMRAM Address Range (HSEG and TSEG)

The HSEG and TSEG SMM transaction address spaces reside in this extended system memory area.

4.4.2.2 HSEG

SMM mode processor accesses to enabled HSEG are remapped to 000A0000h-000BFFFFh. Non-SMM mode processor accesses to enabled HSEG are considered invalid are terminated immediately on the PSB. The exceptions to this rule are Non-SMM mode Write Back cycles that are re-mapped to SMM space to maintain cache coherency. AGP and hub interface originated cycles to enabled SMM space are not allowed. Physical DDR SDRAM behind the HSEG transaction address is not re-mapped and is not accessible.

4.4.2.3 TSEG

TSEG is 1-MB in size and is at the top of physical system memory. SMM mode processor accesses to enabled TSEG access the physical DDR SDRAM at the same address. AGP and hub interface originated cycles to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, CPU accesses to the TSEG range without SMM attribute or without WB attribute are forwarded to the hub interface.

Non-SMM mode CPU accesses to enabled TSEG are considered invalid and are terminated immediately on the PSB. The exceptions to this rule are Non-SMM-mode Write Back cycles that are directed to the physical SMM space to maintain cache coherency. Hub interface originated cycles that enable SMM space are not allowed.

The size of the SMRAM space is determined by the USMM value in the SMRAM register. When the extended SMRAM space is enabled, non-SMM CPU accesses and all other accesses in this range are forwarded to the hub interface. When SMM is enabled the amount of system memory available to the system is equal to the amount of physical DDR SDRAM minus the value in the TSEG register which is fixed at 1 MB for the Intel 852GME GMCH and Intel 852PM MCH.

4.4.2.4 Dynamic Video Memory Technology (DVMT)

The IGD supports DVMT in a non-graphics system memory configuration. DVMT is a mechanism that manages system memory and the internal graphics device for optimal graphics performance. DVMT-enabled software drivers, working with the memory arbiter and the operating system, utilize the system memory to support 2D graphics and 3D applications. DVMT dynamically responds to application requirements by allocating the proper amount of display and texturing memory.

4.4.2.5 PCI Memory Address Range (Top of Main System Memory to 4 GB)

The address range from the top of main DDR SDRAM to 4-GB (top of physical system memory space supported by the GMCH/MCH) is normally mapped via the hub interface to PCI.

With an internal graphics configuration (Intel 852GME GMCH), there are two exceptions to this rule.

1. The first exception is addresses decoded to the Graphics Memory range. One per function in device #2.
2. The second exception is addresses decoded to the system memory mapped range of the Internal Graphics device. One per function in device #2. Both exception cases are forwarded to the Internal Graphics device.

As an AGP configuration, there are two exceptions to this rule:

1. Addresses decoded to the AGP Memory Window defined by the MBASE, MLIMIT, PMBASE, and PMLIMIT registers are mapped to AGP.
2. Addresses decoded to the Graphics Aperture Range defined by the APBASE and APSIZE registers are mapped to the main DDR SDRAM.

There are two sub-ranges within the PCI Memory address range defined as APIC configuration space and High BIOS Address range. As an Internal Graphics device, the Graphics Memory range and the Memory mapped range of the Internal Graphics device **MUST NOT** overlap with these two ranges. Similarly, as an AGP device, the AGP memory window and Graphics Aperture Window **MUST NOT** overlap with these two ranges. These ranges are described in detail in the following paragraphs.

4.4.2.6 APIC Configuration Space (FEC0_0000h -FECF_FFFFh, FEE0_0000h-FEEF_FFFFh)

This range is reserved for APIC configuration space that includes the default I/O APIC configuration space. The default Local APIC configuration space is FEE0_0000h to FEEF_0FFFh.

Processor accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the CPU. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each processor should be relocated to the FEC0_0000h (4 GB-20 MB) to FECF_FFFFh range so that one MTRR can be programmed to 64-kB for the Local and I/O APICs. The I/O APIC(s) usually resides in the ICH4-M portion of the chip-set or as a stand-alone component(s).

I/O APIC units will be located beginning at the default address FEC0_0000h. The first I/O APIC will be located at FEC0_0000h. Each I/O APIC unit is located at FEC0_x000h where *x* is I/O APIC unit number 0 through F (hex). This address range will be normally mapped to hub interface.

The address range between the APIC configuration space and the High BIOS (FED0_0000h to FFDF_FFFFh) is always mapped to the hub interface.

4.4.2.7 High BIOS Area (FFE0_0000h -FFFF_FFFFh)

The top 2-MB of the Extended Memory region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to hub interface so that the upper subset of this region aliases to 16-MB to 256-kB range. The actual address space required for the BIOS is less than 2-MB but the minimum processor MTRR range for this region is 2-MB so that full 2-MB must be considered.

4.4.2.8 AGP Memory Address Ranges

The GMCH/MCH can be programmed to direct memory accesses to the AGP bus interface when addresses are within either of two ranges specified via registers in GMCH/MCH's Device #1 configuration space. The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers. The second range is controlled via the Prefetchable Memory Base (PMBASE) and Prefetchable Memory Limit (PMLIMIT) registers.

Conceptually, address decoding for each range follows the same basic concept. The top 12 bits of the respective Memory Base and Memory Limit registers correspond to address bits A[31:20] of a memory address . For the purpose of address decoding, the GMCH/MCH assumes that address bits A[19:0] of the memory base are zero and that address bits A[19:0] of the memory limit address are FFFFFh. This forces each memory address range to be aligned to 1MB boundary and to have a size granularity of 1MB.

The GMCH/MCH positively decodes memory accesses to AGP memory address space as defined by the following equations:

Prefetchable_Memory_Base_Address ≤ Address ≤ Prefetchable_Memory_Limit_Address

Memory_Base_Address ≤ Address ≤ Memory_Limit_Address

The window size is programmed by the plug-and-play configuration software. The window size depends on the size of memory claimed by the AGP device. Normally these ranges will reside above the Top-of-Main-Memory and below High BIOS and APIC address ranges. They normally reside above the top of memory (TOM) so they do not steal any physical DDR SDRAM memory space.

It is essential to support a separate Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note that the GMCH/MCH Device #1 memory range registers described above are used to allocate memory address space for any devices sitting on AGP that require such a window. These devices would include the AGP device, PCI-66MHz/3.3V agents, and multifunctional AGP devices where one or more functions are implemented as PCI devices.

The PCICMD1 register can override the routing of memory accesses to AGP. In other words, the memory access enable bit must be set in the device 1 PCICMD1 register to enable the memory base/limit and prefetchable base/limit windows.

4.4.3 System Management Mode (SMM) Memory Range

The GMCH/MCH supports the use of main system memory as System Management RAM (SMM RAM) enabling the use of System Management mode. The GMCH/MCH supports three SMM options: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a system memory area that is available for the SMI handler's and code and data storage. This system memory resource is normally hidden from the system OS so that the processor has immediate access to this system memory space upon entry to SMM. The GMCH/MCH provides three SMRAM options:

- Below 1 MB option that supports compatible SMI handlers.
- Above 1 MB option that allows new SMI handlers to execute with Write-back cacheable SMRAM.
- Above 1-MB solutions require changes to compatible SMRAM handler's code to properly execute above 1 MB.

The optional larger write-back cacheable TSEG area from 128 kB to 1 MB in size above 1 MB is reserved from the highest area in DDR SDRAM memory. The above 1 MB solutions require changes to compatible SMRAM handler's code to properly execute above 1 MB.

Note: Hub interface and AGP masters are not allowed to access the SMM space. This must be ensured even for the GTLB translation.

4.4.3.1 SMM Space Restrictions

If any of the following conditions are violated the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space **must not** be set-up as cacheable.
- High or TSEG SMM transaction address space **must not** overlap address space assigned to DDR SDRAM, the AGP aperture range, or to any PCI devices (including hub interface and graphics devices). This is a BIOS responsibility.
- Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available. This is a BIOS responsibility.
- Any address translated through the AGP Aperture GTLB must not target DDR SDRAM from 000A0000h to 000FFFFFh.

4.4.3.2 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DDR SDRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the CPU to access SMM space. DDR SDRAM SMM space is defined as the range of physical DDR SDRAM locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High, and TSEG. The Compatible and TSEG SMM space is not re-mapped and therefore the addressed and DDR SDRAM SMM space is the same address range. Since the High SMM space is re-mapped the addressed and DDR SDRAM SMM space is a different

address range. Note that the High DDR SDRAM space is the same as the Compatible Transaction Address space. Table 46 describes three unique address ranges:

1. Compatible Transaction Address (Adr C)
2. High Transaction Address (Adr H)
3. TSEG Transaction Address (Adr T)

These abbreviations are used later.

Table 39. SMM Space Transaction Handling

SMM Space Enabled	Transaction Address Space (Adr)	DRAM Space (DRAM)
Compatible (C)	A0000h to BFFFFh	A0000h to BFFFFh
High (H)	0FEDA0000h to 0FEDBFFFFh	A0000h to BFFFFh
TSEG (T)	(TOM-TSEG_SZ) to TOM	(TOM-TSEG_SZ) to TOM

4.4.3.3 SMM Access through GART/GTT TLB

CPU accesses through GART/GTT TLB address translation to enabled SMM DDR SDRAM space are not allowed. Writes will be routed to memory address 0h with byte enables deasserted and reads will be routed to memory address 0h. If a GART/GTT TLB translated address hits enabled SMM DDR SDRAM space, the Invalid Graphics Aperture Translation Table Entry Flag (ITTEF) in the ERRSTS register is set.

AGP and hub interface originated accesses are **never** allowed to access SMM space directly or through the GART/GTT TLB address translation. If a GART/GTT TLB translated address hits enabled SMM SDRAM space, the Invalid Graphics Aperture Translation Table Entry Flag (ITTEF) in the ERRSTS register is set.

AGP (PIPE/SBA) write accesses through GART/GTT TLB address translation to enabled SMM DDR SDRAM space will be re-mapped to address 0h with de-asserted byte enables. AGP (PIPE/SBA) read accesses through GART/GTT TLB address translation to enabled SMM DDR SDRAM space will be re-mapped to address 0h.

AGP (FRAME) write accesses through GART/GTT TLB address translation to enabled SMM DDR SDRAM space will be re-mapped to address 0h with de-asserted byte enables. AGP (PIPE/SBA) read accesses through GART/GTT TLB address translation to enabled SMM DDR SDRAM space will be re-mapped to address 0h.

All hub interface originated cycles are snooped and subsequently decoded on the PSB. Hub interface write accesses through GART/GTT TLB address translation to enabled SMM DDR SDRAM space will be snooped and then remapped to address 0h with de-asserted byte enables. Hub interface read accesses through GART/GTT TLB address translation to enabled SMM DDR SDRAM space will be snooped and remapped to address 0h. Any WB resulting from the snoop will be written to enabled SMM DDR SDRAM.

For CPU, AGP (SBA, PIPE and FRAME), and hub interface originated accesses, if a GART/GTT TLB translated address hits enabled High SMM transaction space, the access will go to DDR SDRAM (if 256-MB SDRAM or more) without being re-mapped.

4.4.4 System Memory Shadowing

Any block of system memory that can be designated as Read-Only or Write-Only can be "shadowed" into GMCH/MCH DDR SDRAM. Typically this is done to allow ROM code to execute more rapidly out of main DDR SDRAM. ROM is used as a Read-Only during the copy process while DDR SDRAM at the same time is designated Write-Only. After copying, the DDR SDRAM is designated Read-Only so that ROM is shadowed. CPU bus transactions are routed accordingly.

4.4.5 I/O Address Space

The GMCH/MCH does not support the existence of any other I/O devices beside itself on the CPU bus. The GMCH/MCH generates hub interface or PCI bus cycles for all CPU I/O accesses that it does not claim. Within the host bridge the GMCH/MCH contains two internal registers in the CPU I/O space, Configuration Address register (CONFIG_ADDRESS) and the Configuration Data register (CONFIG_DATA). These locations are used to implement Configuration Space Access Mechanism and as described in the Configuration register section.

The processor allows 64-kB +3-B to be addressed within the I/O space. The GMCH/MCH propagates the CPU I/O address without any translation on to the destination bus and therefore provides addressability for 64-k+3-B locations. Note that the upper three locations can be accessed only during I/O address wrap-around when CPU bus A16# address signal is asserted. A16# is asserted on the CPU bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. A16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) is consumed by the internal graphics device if it is enabled.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the hub interface bus unless they fall within the AGP I/O address range as defined by the mechanisms explained below. The GMCH will not post I/O Write cycles to IDE. The PCICMD1 register can disable the routing of I/O cycles to the AGP. The GMCH/MCH never responds to I/O cycles intiated on AGP.

4.4.5.1 AGP/PCI I/O Address Mapping

The GMCH/MCH can be programmed to direct non-memory (I/O) accesses to the AGP bus interface when CPU initiated I/O cycle addresses are within the AGP I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in GMCH/MCH Device #1 configuration space.

Address decoding for this range is based on the following concept. The top 4 bits of the respective I/O Base and I/O Limit registers correspond to address bits A[15:12] of an I/O address. For the purpose of address decoding, the GMCH/MCH assumes that lower 12 address bits A[11:0] of the I/O base are zero and that address bits A[11:0] of the I/O limit address are FFFh. This forces the I/O address range alignment to 4-kB boundary and produces a size granularity of 4 kB.

The GMCH/MCH positively decodes I/O accesses to AGP I/O address space as defined by the following equation:

I/O_Base_Address ≤ CPU I/O Cycle Address ≤I/O_Limit_Address

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the AGP device.

The GMCH/MCH also forwards accesses to the Legacy VGA I/O ranges according to the settings in the Device #1 configuration registers BCTRL (VGA Enable) and PCICMD1 (IOAE1), unless a second adapter (monochrome) is present on the hub interface/PCI (or ISA). The presence of a second graphics adapter is determined by the MDAP configuration bit. When MDAP is set, the GMCH/MCH will decode legacy monochrome IO ranges and forward them to the hub interface. The IO ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3Bah and 3BFh.

The GMCH/MCH Device #1 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on AGP. These devices would include the AGP device, PCI66 MHz/3.3 V agents, and multifunctional AGP devices where one or more functions are implemented as PCI devices.

The PCICMD1 register can disable the routing of I/O cycles to the AGP.

4.4.6 GMCH Decode Rules and Cross-Bridge Address Mapping

The address map described above applies globally to accesses arriving on any of the three interfaces i.e. Host bus, IGD, and hub interface or AGP.

4.4.6.1 Hub Interface Decode Rules

The GMCH/MCH accepts accesses from hub interface to the following address ranges:

- All memory read and write accesses to main DDR SDRAM including PAM region (except SMM space)
- All memory read/write accesses to the Graphics Aperture (DDR SDRAM) defined by APBASE and APSIZE.
- All hub interface memory write accesses to AGP memory range defined by MBASE, MLIMIT, PMBASE, and PMLIMIT.
- Memory writes to VGA range on AGP if enabled.

All memory reads from the hub interface A that are targeted > 4-GB memory range will be terminated with Master Abort completion, and all memory writes (>4-GB) from the hub interface will be ignored.

Hub interface memory accesses that fall elsewhere within the memory range are considered invalid and will be re-mapped to memory address 0h, snooped on the host bus, and dispatched to DDR SDRAM. Reads will return all 1’s with Master Abort completion. Writes will have BEs deasserted and will terminate with Master Abort if completion is required. I/O cycles will not be accepted. They are terminated with Master Abort completion packets.

4.4.6.1.1 Hub Interface Accesses to GMCH/MCH that Cross Device Boundaries

Hub interface accesses are limited to 256-bytes but have no restrictions on crossing address boundaries. A single hub interface request may therefore span device boundaries (AGP, DDR SDRAM) or cross from valid addresses to invalid addresses (or vise versa). The GMCH/MCH does not support transactions that cross device boundaries. For reads and for writes requiring completion, the GMCH/MCH will provide separate completion status for each naturally aligned 32 -or 64 -byte block. If the starting address of a transaction hits a valid address, the portion of a request that hits that target device (AGP or DDR SDRAM) will complete normally. The remaining portion of the access that crosses a device boundary (targets a different device than that of the starting address) or hits an invalid address will be remapped to memory address 0h, snooped on the host bus, and dispatched to DDR SDRAM. Reads will return all 1's with Master Abort completion. Writes will have BEs deasserted and will terminate with Master Abort if completion is required.

If the starting address of a transaction hits a invalid address the entire transaction will be re-mapped to memory address 0h, snooped on the host bus, and dispatched to DDR SDRAM. Reads will return all 1's with Master Abort completion. Writes will have BEs deasserted and will terminate with Master Abort if completion is required.

4.4.6.1.2 AGP Interface Decode Rules

Cycles Initiated Using PCI Protocol

The GMCH/MCH does not support any AGP/PCI access targeting hub interface. The GMCH will claim AGP/PCI initiated memory read and write transactions decoded to the main DDR SDRAM range or the Graphics Aperture range. All other memory read and write requests will be master-aborted by the AGP/PCI initiator as a consequence of GMCH/MCH not responding to a transaction.

Under certain conditions, the GMCH/MCH restricts access to the DOS Compatibility ranges governed by the PAM registers by distinguishing access type and destination bus. The GMCH/MCH accepts AGP/PCI write transactions to the compatibility ranges if the PAM designates DDR SDRAM as write-able. If accesses to a range are not write-enabled by the PAM, the GMCH/MCH does not respond and the cycle will result in a master-abort. The GMCH/MCH accepts AGP/PCI read transactions to the compatibility ranges if the PAM designates DDR SDRAM as readable. If accesses to a range are not read enabled by the PAM, the GMCH/MCH do not respond and the cycle will result in a master-abort.

If agent on AGP/PCI issues an I/O or PCI Special Cycle transaction, the GMCH will not respond and cycle will result in a master-abort. The GMCH will accept PCI configuration cycles to the internal GMCH devices as part of the PCI configuration/co-pilot mode mechanism.

Cycles Initiated Using AGP Protocol

All cycles must reference main memory i.e. main DDR SDRAM address range (*excluding* PAM) or Graphics Aperture range (also physically mapped within DDR SDRAM but using different address range). AGP accesses to the PAM region from 640 kB to 1 MB are not allowed. AGP accesses to SMM space are not allowed. AGP initiated cycles that target DDR SDRAM are not snooped on the host bus, even if they fall outside of the AGP aperture range.

If a cycle is outside of a valid main memory range then it will terminate as follows:

Reads: Remap to memory address 0h, return data from address 0h, and set the IAAF error flag.

Writes: Re-mapped to memory address 0h with BE's de-asserted (effectively dropped "on the floor") and set the IAAF error flag.

AGP Accesses to GMCH/MCH that Cross Device Boundaries

For FRAME# accesses, when an AGP or PCI master gets disconnected it will resume at the new address which allows the cycle to be routed to or claimed by the new target. Therefore accesses should be disconnected by the target on potential device boundaries. The GMCH/MCH will disconnect AGP/PCI transactions on 4-kB boundaries.

AGPPIPE# and SBA accesses are limited to 256 bytes and must hit DDR SDRAM. AGP accesses are dispatched to DDR SDRAM on naturally aligned 32 - byte block boundaries. The portion of the request that hits a valid address will complete normally. The portion of a read access that hits an invalid address will be re-mapped to address 0h, return data from address 0h, and set the IAAF error flag. The portion of a write access that hits an invalid address will be re-mapped to memory address 0h with BE's de-asserted (effectively dropped "on the floor") and set the IAAF error flag.

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5 Functional Description

5.1 Host Interface Overview

The processor system bus uses source synchronous transfers for the address and data signals. The address signals are double pumped and two addresses can be generated every bus clock. At 100 MHz bus frequency, the two address signals run at 200 MT/s for a maximum address queue rate of 50 M addresses/sec. The data is quad pumped and an entire 64 bits cache line can be transferred in two bus clocks. At 133-MHz bus frequency, the data signals run at 533-MT/s for a maximum bandwidth of 4.3-GB/s.

5.2 Dynamic Bus Inversion

The GMCH/MCH supports Dynamic Bus Inversion (DBI) when driving and receiving data from the Host bus. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the power consumption of the GMCH/MCH. DINV[3:0] indicates if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

Table 40. Relation of DBI Bits to Data Bits

DINV[3:0]	Data Bits
DINV[0]#	HD[15:0]#
DINV[1]#	HD[31:16]#
DINV[2]#	HD[47:32]#
DINV[3]#	HD[63:48]#

Whenever the processor or the GMCH/MCH drive data, each 16-bit segment is analyzed. If more than eight of the 16 data signals would normally be driven low on the bus the corresponding DINV# signal will be asserted and the data will be inverted prior to being driven on the bus. Whenever the CPU or the GMCH/MCH receive data, they monitor DINV[3:0]# to determine if the corresponding data segment should be inverted.

5.2.1 System Bus Interrupt Delivery

Each processor supports system bus interrupt delivery. They do not support the APIC serial bus interrupt delivery mechanism. Interrupt related messages are encoded on the System Bus as “Interrupt Message Transactions.” System bus interrupts may originate from the processor on the system bus, or from a downstream device on hub interface.

The ICH4-M contains IOxAPICs and its interrupts are generated as upstream hub interface Memory Writes. Furthermore, PCI 2.2 defines MSI’s (Message Signaled Interrupts) that are also in the form of Memory Writes. A PCI 2.2 device may generate an interrupt as an MSI cycle on its

PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC, which in turn generates an interrupt as an upstream hub interface Memory Write. Alternatively the MSI may be directed directly to the system bus. The target of an MSI is dependent on the address of the interrupt Memory Write. The GMCH forwards inbound hub interface Memory Writes to address 0FEEx_xxxxh, to the System Bus as “Interrupt Message Transactions”.

5.2.2 Upstream Interrupt Messages

The GMCH/MCH accepts message based interrupts from its hub interface and forwards them to the System Bus as Interrupt Message Transactions. The interrupt messages presented to the GMCH/MCH are in the form of Memory Writes to address 0FEEx_xxxxh. At the hub interface, the Memory Write interrupt message is treated like any other Memory Write; it is either posted into the inbound data buffer (if space is available) or retried (if data buffer space is not immediately available). Once posted, the Memory Write from the hub interface, to address 0FEEx_xxxxh, is decoded as a cycle that needs to be propagated by the GMCH/MCH to the System Bus as an Interrupt Message transaction.

5.3 System Memory Interface

5.3.1 DDR SDRAM Interface Overview

The Intel 852GME GMCH and Intel 852PM MCH support DDR SDRAM at 200/266/333 MHz, respectively. The GMCH/MCH includes support for:

- Up to 2-GB of PC2100/2700 DDR SDRAM
- PC2100/2700 unbuffered 200-pin DDR SO-DIMMs
- Maximum of 2 SO-DIMMs, single-sided and/or double-sided/or stacked

The 2-bank select lines SBA[1:0] and the 13 Address lines SMA[12:0] allow the GMCH/MCH to support 64-bit wide SO-DIMMs using 128-Mb, 256-Mb, and 512-Mb DDR SDRAM technology. While address lines SMA[9:0] determine the starting address for a burst, burst lengths can be 4 or 8. Four chip selects SCS[3:0]# lines allow a maximum of two rows of single-sided DDR SDRAM SO-DIMMs and four rows of double-sided DDR SDRAM SO-DIMMs.

The GMCH/MCH main memory controller targets CAS latencies of 2 and 2.5 for DDR SDRAM. The GMCH/MCH provides refresh functionality with a programmable rate (normal DDR SDRAM rate is 1 refresh/15.6 µs). For write operations of less than a full cache line, the GMCH/MCH will perform a cache-line read and into the write buffer and perform byte-wise write-merging in the write buffer.

5.3.2 Memory Organization and Configuration

5.3.2.1 Configuration Mechanism for SO-DIMMs

Detection of the type of DDR SDRAM installed on the SO-DIMM is supported via Serial Presence Detect mechanism as defined in the JEDEC 200-pin SO- DIMM specification.

Before any cycles to the system memory interface can be supported, the GMCH/MCH DDR SDRAM registers must be initialized. The GMCH/MCH must be configured for operation with the installed system memory types. Detection of system memory type and size is done via the System Management Bus (SMB) interface on the ICH4-M. This two-wire bus is used to extract the DDR SDRAM type and size information from the Serial Presence Detect port on the DDR SDRAM SO-DIMMs.

DDR SDRAM SO-DIMMs contain a 5-pin Serial Presence Detect interface, including SCL (serial clock), SDA (serial data) and SA[2:0]. Devices on the SMBus have a 7-bit address. For the DDR SDRAM SO-DIMMs, the upper four bits are fixed at 1010. The lower three bits are strapped on the SA[2:0] pins. SCL and SDA are connected directly to the system management bus on the ICH4-M. Thus data is read from the Serial Presence Detect port on the SO-DIMMs via a series of I/O cycles to the south bridge. The BIOS needs to determine the size and type of system memory used for each of the rows of system memory in order to properly configure the GMCH/MCH system memory interface.

For SMBus Configuration and Access of the Serial Presence Detect Ports, refer to the *Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet* (252337-001) for more detail.

5.3.2.2 System Memory Register Programming

This section provides summary of how the required information for programming the DDR SDRAM registers is obtained from the Serial Presence Detect ports on the SO-DIMMs. The Serial Presence Detect ports are used to determine Refresh Rate, MA and MD Buffer Strength, Row Type (on a row by row basis), DDR SDRAM timings, row sizes and row page sizes. The following table lists a subset of the data available through the on board Serial Presence Detect ROM on each SO-DIMM.

Table 41. Data Bytes on SO-DIMM Used for Programming DDR SDRAM Registers

Byte	Description
2	System Memory Type (DDR SDRAM)
3	Number of Row Addresses, not counting Bank Addresses
4	Number of Column Addresses
5	Number of SO-DIMM banks
11	ECC, No ECC
12	Refresh Rate/Type
17	Number Banks on each Device

The above table is only a subset of the defined SPD bytes on the SO-DIMMs. These bytes collectively provide enough data for programming the GMCH/MCH DDR SDRAM registers.

5.3.3 DDR SDRAM Performance Description

The overall system memory performance is controlled by the DDR SDRAM timing register, pipelining depth used in GMCH/MCH, system memory speed grade and the type of DDR SDRAM used in the system. Besides this, the exact performance in a system is also dependent on the total system memory supported, external buffering and system memory array layout. The most important contribution to overall performance by the system memory controller is to

minimize the latency required to initiate and complete requests to system memory, and to support the highest possible bandwidth (full streaming, quick turn-arounds). One measure of performance is the total flight time to complete a cache line request. A true discussion of performance really involves the entire chipset, not just the system memory controller.

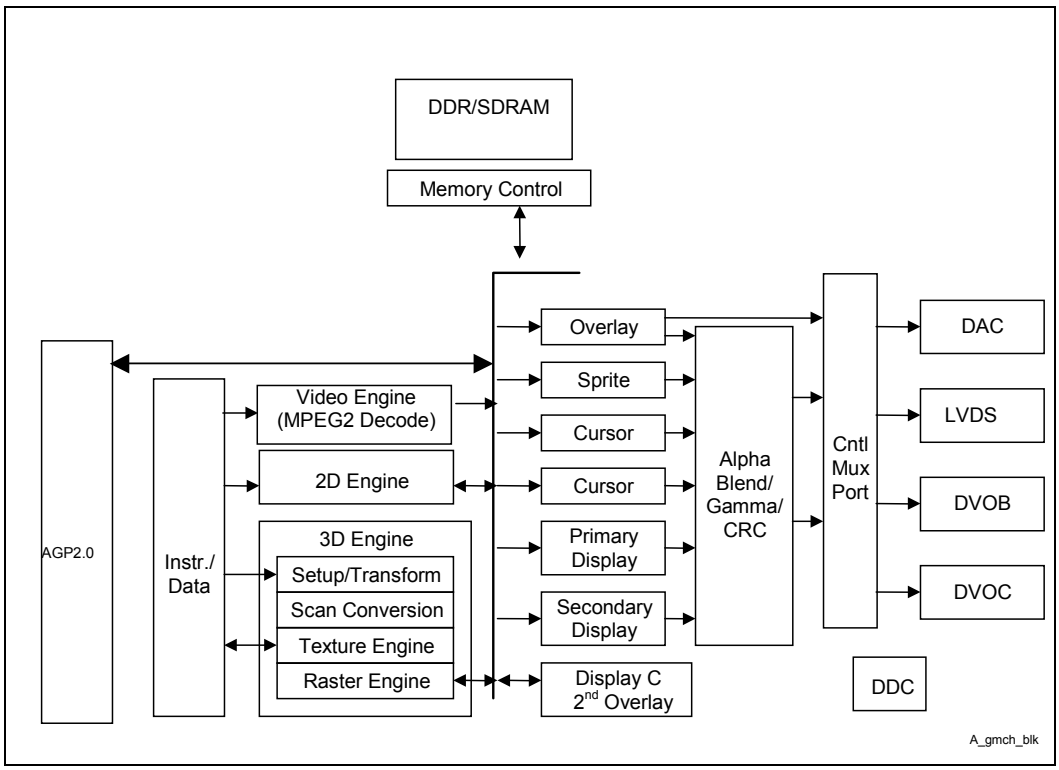
5.3.4 Intel 852GME GMCH and Intel 852PM MCH Data Integrity (ECC)

The GMCH/MCH supports single-bit Error Correcting Code (or Error Checking and Correcting) (ECC) and multiple-bit Error Checking (EC) on the main memory interface. The GMCH/MCH generates an 8-bit code word for each 64-bit Qword of memory. GMCH/MCH performs two Qword writes at a time so two 8-bit codes are sent with each write. Since the code word covers a full Qword, writes of less than a Qword require a read-merge-write operation. Consider a Dword write to memory. In this case, when in ECC mode, GMCH/MCH will read the Qword where the addressed Dword will be written, merge in the new Dword, generate a code covering the new Qword and finally write the entire Qword and code back to memory. Any correctable (single-bit) errors detected during the initial Qword read are corrected before merging the new Dword. The GMCH/MCH also supports another data integrity mode, EC mode. In this mode, the GMCH/MCH generates and stores a code for each Qword of memory. It then checks the code for reads from memory but does not correct any errors that are found.

5.4 Integrated Graphics Overview

The GMCH provides a highly integrated graphics accelerator and PCI set while allowing a flexible integrated system graphics solution.

Figure 9. Intel 852GME GMCH Graphics Block Diagram



High bandwidth access to data is provided through the system memory port. The GMCH accesses UMA memory located in system memory at 1.06 GB/s. The GMCH uses a tiling architecture to minimize page miss latencies and thus maximize effective rendering bandwidth.

5.4.1 Intel GMCH 3D/2D Instruction Processing

The GMCH contains an extensive set of instructions that control various functions including 3D rendering, BLT operations, display, MPEG decode acceleration, and overlay. The 3D instructions set 3D pipeline states and control the processing functions. The 2D instructions provide an efficient method for invoking BLT operations.

5.4.2 3D Engine

The 3D engine of the GMCH has been designed with a deeply pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive. The GMCH supports the following:

- Perspective-correct texture mapping
- Multitextures
- Embossed and Dot-Product Bump mapping
- Cubic Environment Maps
- Bilinear, Trilinear, and Anisotropic MIP mapped filtering

- Gouraud shading
- Alpha-blending
- Per-Vertex and Per- Pixel fog
- Z/W buffering

These features are independently controlled via a set of 3D instructions. The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the Setup Engine, Scan Converter, Texture Pipeline, and Raster Pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rendering instructions containing 3D primitive vertex data.

5.4.2.1 Setup Engine

The GMCH 3D setup engine takes the input data associated with each vertex of a 3D primitive and computes the various parameters required for scan conversion. In formatting this data, the GMCH maintains sub-pixel accuracy. The per-vertex data is converted into gradients that can be used to interpolate the data at any pixel within a polygon (colors, alpha, Z or W depth, fog, and texture coordinates). The pixels covered by a polygon are identified and per-pixel texture addresses are calculated.

5.4.2.2 Viewport Transform and Perspective Divide

A 3D-geometry pipeline typically involves transformation of vertices from model space to clipping space followed by clip test and clipping. Lighting can be performed during the transformation or at any other point in the pipeline. After clipping, the next stage involves perspective divide followed by transformation to the viewport or screen space. The GMCH can support Viewport Transform and Perspective Divide portion of the 3D geometry pipeline in hardware.

5.4.2.3 3D Primitives and Data Formats Support

The 3D primitives rendered by the GMCH are points, lines, discrete triangles, line strips, triangle strips, triangle fans, and polygons. In addition to this, the GMCH supports DirectX* Flexible Vertex Format* (FVF), which enables the application to specify a variable length parameter list, obviating the need for sending unused information to the hardware. Strips, Fans, and Indexed Vertices as well as FVF improve the delivered vertex rate to the setup engine significantly.

5.4.2.4 Pixel Accurate Fast Scissoring and Clipping Operation

The GMCH supports clipping to a scissoring rectangle within the drawing window. The GMCH clipping and scissoring in hardware reduce the need for software to process polygons, and thus improves performance. During the setup stage, the GMCH clips polygons to the drawing window. The scissor rectangle accelerates the clipping process by allowing the driver to clip to a bigger region than the hardware renders to. The scissor rectangle is pixel accurate, and independent of line and point width. The GMCH supports a single scissor box rectangle.

5.4.2.5 Backface Culling

As part of the setup, the GMCH can discard polygons from further processing, if they are either facing away from or towards the user's viewpoint. This operation, referred to as "Back Face Culling" is accomplished based on the "clockwise" or "counter-clockwise" orientation of the vertices on a primitive. This can be enabled or disabled by the driver.

5.4.2.6 Scan Converter

The Scan Converter takes the vertex and edge information is used to identify all pixels that are affected by features being rendered. It works on a per-polygon basis, and one polygon may be entering the pipeline while calculations finish on another.

5.4.2.7 Texture Engine

The GMCH allows an image pattern, or video to be placed on the surface of a 3D polygon. The texture engine performs texture color or chromakey matching texture filtering (an-isotropic, tri-linear, and bilinear), and YUV to RGB conversion.

As texture sizes increase beyond the bounds of graphics memory, executing textures from graphics memory becomes impractical. Every rendering pass would require copying each and every texture in a scene from system memory to graphics memory, then using the texture, and finally overwriting the local memory copy of the texture by copying the next texture into graphics memory. The GMCH, using the Intel Direct Memory Execution model, simplifies this process by rendering each scene using the texture located in system memory. The GMCH includes a cache controller to avoid frequent memory fetches of recently used texture data.

5.4.2.8 Perspective Correct Texture Support

A textured polygon is generated by mapping a 2D texture pattern onto each pixel of the polygon. A texture map is like wallpaper pasted onto the polygon. Since polygons are rendered in perspective, it is important that texture be mapped in perspective as well. Without perspective correction, texture is distorted when an object recedes into the distance. Perspective correction involves a compute-intensive "per-pixel-divide" operation on each pixel. Perspective correction is necessary for realistic 3D graphics.

5.4.2.9 Texture Decompression

As the textures' average size gets larger with higher color depth and multiple textures become the norm, it becomes increasingly important to provide support for compressed textures.

DirectX* supports Texture Compression/Decompression to reduce the bandwidth required to deliver textures. The GMCH supports several compressed texture formats (DirectX: DXT1, DXT2, DXT3, DXT4, DXT5) and OpenGL* FXT1 formats.

5.4.2.10 Texture Chromakey

Chromakey is a method for removing a specific color or range of colors from a texture map before it is applied to an object. For "nearest" texture filter modes, removing a color simply

makes those portions of the object transparent (the previous contents of the back buffer show through). For “linear“ texture filtering modes, the texture filter is modified if only the non-nearest neighbor texels match the key (range).

Chromakeying can be performed for both paletted and non-paletted textures, and removes texels that fall within a specified color range. The Chromakey mode refers to testing the RGB or YUV components to see if they fall between high and low state variable values. If the color of a texel contribution is in this range and chromakey is enabled, then this contribution is removed from the resulting pixel color.

5.4.2.11 Anti-Aliasing

Aliasing is one of the artifacts that degrade image quality. In its simplest manifestation, aliasing causes the jagged staircase effects on sloped lines and polygon edges. Another artifact is the moiré patterns, which occur as a result of the fact that there is very small number of pixels available on screen to contain the data of a high-resolution texture map.

Full Scene Anti-Aliasing uses super-sampling, which means that the image is rendered internally at a higher resolution than it is displayed on screen. The GMCH can render internally at 1600x1200 and then this image is down-sampled (via a Bilinear filter) to the screen resolution of 640x480 and 800x600. Full Scene Anti-aliasing removes jaggies at the edges as well as moiré patterns. The GMCH renders the super-sampled image up to 2K x 2K pixel dimensions. The GMCH then reads it as a texture and bilinearly filters it to the final resolution.

5.4.2.12 Texture Map Filtering

Many texture-mapping modes are supported. Perspective correct mapping is always performed. As the map is fitted across the polygon, the map can be tiled, mirrored in either the U or V directions, or mapped up to the end of the texture and no longer placed on the object (this is known as clamp mode). The way a texture is combined with other object attributes is also definable.

The GMCH supports up to 12 Levels-of-Detail (LODs) ranging in size from 2048x2048 to 1x1 texels. (A texel is defined as a texture map element.) Included in the texture processor is a texture cache, which provides efficient MIP-mapping.

The GMCH supports seven types of texture filtering:

- Nearest (also known as Point Filtering): Texel with coordinates nearest to the desired pixel is used. (This is used if only one LOD is present.)
- Linear (also known as Bilinear Filtering): A weighted average of a 2x2 area of texels surrounding the desired pixel is used. (This is used if only one LOD is present.)
- Nearest MIP Nearest (also known as Point Filtering): This is used if many LODs are present. The nearest LOD is chosen and the texel with coordinates nearest to the desired pixel is used.
- Linear MIP Nearest (Bilinear MIP Mapping): This is used if many LODs are present. The nearest LOD is chosen and a weighted average of a 2x2 area of texels surrounding the desired pixel is used (four texels). This is also referred to as Bilinear MIP Mapping.
- Nearest MIP Linear (Point MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and within each LOD the texel with coordinates nearest to the

desired pixel are selected. The Final texture value is generated by linear interpolation between the two texels selected from each of the MIP Maps.

- Linear MIP Linear (Trilinear MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and a weighted average of a 2x2 area of texels surrounding the desired pixel in each MIP Map is generated (four texels per MIP Map). The Final texture value is generated by linear interpolation between the two texels generated for each of the MIP Maps. Trilinear MIP Mapping is used to minimize the visibility of LOD transitions across the polygon.
- Anisotropic MIP Nearest (Anisotropic Filtering): This filter can be used when textured object pixels map back to significantly non-square regions of the texture (e.g., when the texture is scaled in one screen direction than the other screen direction).
- Both DirectX and OGL (Rev.1.1) allow support for all these filtering modes.

5.4.2.13 Multiple Texture Composition

The GMCH also performs multiple texture composition. This allows the combination of two or greater MIP maps to produce a new one with new LODs and texture attributes in a single or iterated pass. The setup engine supports up to four texture map coordinates in a single pass. The GMCH allows up to two Bilinear MIP Maps or a single Trilinear MIP Map to be composited in a single pass. Greater than two Bilinear MIP Maps or more than one Trilinear MIP Map would require multiple passes. The actual blending or composition of the MIP Maps is done in the raster engine. The texture engine provides the required texels including blending information.

Flexible vertex format support allows multi-texturing because it makes it possible to pass more than one texture in the vertex structure.

5.4.2.14 Cubic Environment Mapping

Environment maps allow applications to render scenes with complex lighting and reflections while significantly decreasing processor load. There are several methods to generate environment maps such as spherical, circular and cubic. The GMCH supports cubic reflection mapping over spherical and circular since it is the best choice to provide real-time environment mapping for complex lighting and reflections.

Cubic Mapping supports a texture map for each of the 6 cube faces. These can be generated by pointing a camera with a 90-degree field-of-view in the appropriate direction. Per-vertex vectors (normal, reflection or refraction) are interpolated across the polygon and the intersection of these vectors with the cube texture faces are calculated. Texel values are then read from the intersection point on the appropriate face and filtered accordingly.

5.4.2.15 Bump Mapping

The GMCH only supports embossed and dot product bump mapping, not environment bump mapping.

5.4.3 Raster Engine

The Raster Engine is where the color data such as fogging, specular RGB, texture map blending, etc. is processed. The final color of the pixel is calculated and the RGB value combined with the

corresponding components resulting from the Texture Engine. These textured pixels are modified by the specular and fog parameters. These specular highlighted, fogged, textured pixels are color blended with the existing values in the frame buffer. In parallel, stencil, alpha, and depth buffer tests are conducted which will determine whether the Frame and Depth Buffers will be updated with the new pixel values.

5.4.3.1 Texture Map Blending

Multiple Textures can be blended together in an iterative process and applied to a primitive. The GMCH allows up to four distinct or shared texture coordinates and texture maps to be specified onto the same polygon. Also, the GMCH supports a texture coordinate set to access multiple texture maps. State variables in multiple textures are bound to texture coordinates, texture map or texture blending.

5.4.3.2 Combining Intrinsic and Specular Color Components

The GMCH allows an independently specified and interpolated “specular RGB” attribute to be added to the post-texture blended pixel color. This feature provides a full RGB specular highlight to be applied to a textured surface, permitting a high quality reflective colored lighting effect not available in devices, which apply texture after the lighting components have been combined. If specular-add state variable is disabled, only the resultant colors from the map blending are used. If this state variable is enabled, the specular RGB color is added to the RGB values from the output of the map blending.

5.4.3.3 Color Shading Modes

The Raster Engine supports the flat and Gouraud shading modes. These shading modes are programmed by the appropriate state variables issued through the command stream.

- Flat shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue), Specular (R, G, B), Fog, and Alpha to the pixel, where each vertex color has the same value. The setup engine substitutes one of the vertex’s attribute values for the other two vertices attribute values thereby creating the correct flat shading terms. This condition is set up by the appropriate state variables issued prior to rendering the primitive.
- Gouraud shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue). Specular (RGB), Fog, and Alpha to the pixel, where each vertex color has a different value. All the attributes can be selected independently to one of the shading modes by setting the appropriate value state variables.

5.4.3.4 Color Dithering

Color Dithering in the GMCH helps to hide color quantization errors for 16-bit color buffers. Color Dithering takes advantage of the human eye’s propensity to “average” the colors in a small area. Input color, alpha, and fog components are converted from 8-bit components to 5-bit or 6-bit component by dithering. Dithering is performed on blended textured pixels. In 32-bit mode, dithering is not performed.

5.4.3.5 Vertex and Per Pixel Fogging

Fogging is used to create atmospheric effects such as low visibility conditions in flight simulator-type games. It adds another level of realism to computer-generated scenes. Fog can be used for depth cueing or hiding distant objects. With fog, distant objects can be rendered with fewer details (less polygons), thereby improving the rendering speed or frame rate. Fog is simulated by attenuating the color of an object with the fog color as a function of distance, and the greater the distance, the higher the density (lower visibility for distant objects). There are two ways to implement the fogging technique: per-vertex (linear) fogging and per-pixel (non-linear) fogging. The per-vertex method interpolates the fog value at the vertices of a polygon to determine the fog factor at each pixel within the polygon. This method provides realistic fogging as long as the polygons are small. With large polygons (such as a ground plane depicting an airport runway), the per-vertex technique results in unnatural fogging.

The GMCH supports both types of fog operations, vertex and per pixel or table fog. If fog is disabled, the incoming color intensities are passed unchanged to the destination blend unit. If fog is enabled, the incoming pixel color is blended with the fog color based on a fog coefficient on a per pixel basis using the following equation before sending to the destination blend unit.

5.4.3.6 Alpha Blending

Alpha Blending in the GMCH adds the material property of transparency or opacity to an object. Alpha blending combines a source pixel color and alpha component with a destination pixel color and alpha component. For example, a glass surface on top (source) of a red surface (destination) would allow much of the red base color to show through.

Blending allows the source and destination color values to be multiplied by programmable factors and then combined via a programmable blend function. The combined and independent selection of factors and blend functions for color and alpha is supported.

5.4.3.7 Color Buffer Formats: (Destination Alpha)

The Raster Engine supports 8-bit, 16-bit, and 32-bit Color Buffer Formats. The 8-bit format is used to support planar YUV420 format, which is used only in Motion Compensation and Arithmetic Stretch format. The bit format of Color and Z is allowed to mix.

The GMCH can support an 8-bit destination alpha in 32-bit mode. Destination alpha is supported in 16-bit mode in 1555 or 4444 format. The GMCH does not support general 3D rendering to 8-bit surfaces. 8-bit destinations are supported for operations on planar YUV surfaces (e.g., stretch Blts) where each 8-bit color component is written in a separate pass. The GMCH also supports a mode where both U and V planar surfaces can be operated on simultaneously.

The frame buffer of the GMCH contains at least two hardware buffers, the Front Buffer (display buffer) and the Back Buffer (rendering buffer). While the back buffer may actually coincide with (or be part of) the visible display surface, a separate (screen or window-sized) back buffer is typically used to permit double-buffered drawing. That is, the image being drawn is not visible until the scene is complete and the back buffer made visible or copied to the front buffer via a 2D BLT operation. Rendering to one buffer and displaying from the other buffer removes image tearing artifacts. Additionally, more than two back buffers (e.g., triple-buffering) can be supported.

5.4.3.8 Depth Buffer

The Raster Engine is able to read and write from this buffer and use the data in per fragment operations that determine resultant color and depth value of the pixel for the fragment are to be updated or not.

Typical applications for entertainment or visual simulations with exterior scenes require far/near ratios of 1000 to 10000. At 1000, 98% of the range is spent on the first 2% of the depth. This can cause hidden surface artifacts in distant objects, especially when using 16-bit depth buffers. A 24-bit Z-buffer provides 16 million Z-values as opposed to only 64 k with a 16-bit Z-buffer. With lower Z-resolution, two distant overlapping objects may be assigned the same Z-value. As a result, the rendering hardware may have a problem resolving the order of the objects, and the object in the back may appear through the object in the front.

By contrast, when w (or eye-relative z) is used, the buffer bits can be more evenly allocated between the near and far clip planes in world space. The key benefit is that the ratio of far and near is no longer an issue, and allows applications to support a maximum range of miles, yet still get reasonably accurate depth buffering within inches of the eye point. The selection of depth buffer size is relatively independent of the color buffer. A 16-bit Z/W or 24-bit Z/W buffer can be selected with a 16-bit color buffer. Z buffer is not supported in 8-bit mode.

5.4.3.9 Stencil Buffer

The Raster engine provides 8-bit stencil buffer storage in 32-bit mode and the ability to perform stencil testing. Stencil testing controls 3D drawing on a per pixel basis and conditionally eliminates a pixel on the outcome of a comparison between a stencil reference value and the value in the stencil buffer at the location of the source pixel being processed. They are typically used in multipass algorithms to achieve special effects, such as decals, outlining, shadows, and constructive solid geometry rendering.

One of three possible stencil operations is performed when stencil testing is enabled. The stencil operation specifies how the stencil buffer is modified when a fragment passes or fails the stencil test. The selection of the stencil operation to be performed is based upon the result of the stencil test and the depth test. A stencil write mask is also included that controls the writing of particular bits into the stencil buffer. It selects between the destination value and the updated value on a per-bit basis. The mask is 8-bit wide.

5.4.3.10 Projective Textures

The GMCH supports two simultaneous projective textures at full rate processing. These textures require three floating-point texture coordinates to be included in the FVF format. Projective textures enable special effects such as projecting spot light textures obliquely onto walls, etc.

5.4.4 GMCH 2D Engine

The GMCH provides an extensive set of 2D instructions and 2D HW acceleration for block transfers of data (BLTs). The BLT engine provides the ability to copy a source block of data to a destination and perform operations (e.g., ROP1, ROP2, and ROP3) on the data using a pattern, and/or another destination. The Stretch BLT engine is used to move source data to a destination that need not be the same size, with source transparency. Performing these common tasks in hardware reduces processor load, and thus improves performance.

5.4.4.1 256-Bit Pattern Fill and BLT Engine

Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft Windows*. The GMCH BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between system memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between system memory locations
- Data Alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between system memory locations. Data to be transferred can consist of regions of system memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8-bits, 16-bits, or 32-bits per pixel.

The GMCH BLT engine has the ability to expand monochrome data into a color depth of 8-bits, 16-bits, or 32-bits. BLTs can be either opaque or transparent. Opaque transfers, move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source system memory location, the GMCH can specify which area in system memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.

The GMCH has instructions to invoke BLT operations, permitting software to set up instruction buffers and use batch processing as described in the Instruction Processing Section. The GMCH can perform hardware clipping during BLTs.

5.4.4.2 Alpha Stretch BLT

The stretch BLT function can stretch source data in the X and Y directions to a destination larger or smaller than the source. Stretch BLT functionality expands a region of system memory into a larger or smaller region using replication and interpolation. The stretch BLT function also provides format conversion and data alignment.

5.4.5 GMCH Planes and Engines

The GMCH display can be functionally delineated into Planes and Engines (Pipes and Ports). A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces, which are rectangular system memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

A pipe consists of a set of planes that will be combined and a timing generator. A port is the destination for the result of the pipe. Therefore, planes are associated with pipes and pipes are associated with ports.

5.4.5.1 Dual Pipe Independent Display Functionality

The display consists of two display pipes, A and B. Pipes have a set of planes that are assigned to them as sources. The analog display port may only use Pipe A or Pipe B, DVOB and DVO C port may use either Pipe A or Pipe B, and the LFP LVDS interface may only use Pipe B. This limits the resolutions available on a digital display when an analog CRT is active.

Table 42. Dual Display Usage Model

Display Pipe A	Display Pipe B
CRT	LFP (Internal LVDS)
DVO B or DVO C or both	CRT
CRT	DVO B or DVO C or both (Simultaneous Scan)
DVO B or DVO C or both	LFP (Internal LVDS)
CRT/DVO B or DVO C or both	LFP (Internal LVDS)

5.4.6 Hardware Cursor Plane

The GMCH supports two hardware cursors. The cursor plane is one of the simplest display planes. With a few exceptions, has a fixed size of 64 x 64 and a fixed Z-order (top). In legacy modes, cursor can cause the display data below it to be inverted. In the alpha blend mode, true color cursor data can be alpha blended into the display stream. It can be assigned to either display pipe A or display pipe B and dynamically flipped from one to the other when both are running.

5.4.6.1 Cursor Color Formats

Color data can be in an indexed format or a true color format. Indexed data uses the entries in the four-entry cursor palette to convert the two-bit index to a true color format before being passed to the blenders. The index can optionally specify that a cursor pixel be transparent or cause an inversion of the pixel value below it or one of two colors from the cursor palette. Blending of YUV or RGB data is only supported with planes that have data of the same format.

5.4.6.2 Popup Plane (Second Cursor)

The popup plane is used for control functions in mobile applications. Only the hardware cursor has a higher Z-order precedence over the hardware icon. In standard modes (non-VGA) either cursor A or cursor B can be used as a Popup Icon. For VGA modes, 32-bpp data format is not supported.

5.4.6.3 Popup Color Formats

Source color data for the popup is in an indexed format. Indexed data uses the entries in the four-entry cursor palette to convert the two-bit index to a true color format before being passed to the blenders. Blending of color data is only supported with data of the same format.

5.4.7 Overlay Plane

The overlay engine provides a method of merging either video capture data (from an external Video Capture device) or data delivered by the processor, with the graphics data on the screen.

5.4.7.1 Multiple Overlays (Display C)

A single overlay plane and scalar is implemented. This overlay plane can be connected to the primary display, secondary display or in bypass mode. In the default mode, it appears on the primary display. The overlay may be displayed in a multi-monitor scenario for single-pipe simultaneous displays only. Picture-in-Picture feature is supported via software through the arithmetic stretch blitter.

5.4.7.2 Source/Destination Color/Chromakeying

Overlay source/destination chromakeying enables blending of the overlay with the underlying graphics background. Destination color-/chromakeying can be used to handle occluded portions of the overlay window on a pixel-by-pixel basis that is actually an underlay. Destination color keying supports a specific color (8-bit or 15-bit) mode as well as 32-bit alpha blending.

Source color/chromakeying is used to handle transparency based on the overlay window on a pixel-by-pixel basis. This is used when “blue screening” an image to overlay the image on a new background later.

5.4.7.3 Gamma Correction

To compensate for overlay color intensity loss, the overlay engine supports independent gamma correction. This allows the overlay data to be converted to linear data or corrected for the display device when not blending.

5.4.7.4 YUV to RGB Conversion

The format conversion can be bypassed in the case of RGB source data.

5.4.7.5 Color Control

Color control provides a method of changing the color characteristics of the pixel data. It is applied to the data while in YUV format and uses input parameters such as brightness, saturation, hue (tint) and contrast. This feature is supplied for the overlay only and works in YUV formats only.

5.4.7.6 Dynamic Bob and Weave

Interlaced data that originates from a video camera creates two fields that are temporally offset by 1/60 of a second. There are several schemes to de-interlace the video stream: line replication, vertical filtering, field merging, and vertical temporal filtering. Field merging takes lines from the previous field and inserts them into the current field to construct the frame – this is known as weaving. This is the best solution for images with little motion; however, showing a frame that consists of the two fields will have serration or feathering of moving edges when there is motion

in the scene. Vertical filtering or “Bob” interpolates adjacent lines rather replicating the nearest neighbor. This is the best solution for images with motion however, it will have reduced spatial resolution in areas that have no motion and introduce jaggies. In absence of any other de-interlacing, these form the baseline and are supported by the GMCH.

5.4.8 Video Functionality

The GMCH supports MPEG-2 decoding hardware, sub-picture support and DTV all format decode.

5.4.8.1 MPEG-2 Decoding

The GMCH MPEG2 Decoding supports Hardware Motion Compensation (HWMC). The GMCH can accelerate video decoding for the following video coding standards:

- MPEG-2 support
- MPEG-1: Full feature support
- H.263 support
- MPEG-4: Only supports some features in the simple profile.

The GMCH HWMC interface is optimized for the Microsoft Direct VA* API. Hardware Video Acceleration API (HVA) is a generic DirectDraw* and DirectShow* interface supported in Windows 2000 and Windows 98 Millennium to provide video decoding acceleration. Direct VA is the open standard implementation of HVA, which is natively supported by the GMCH hardware.

5.4.8.2 Hardware Motion Compensation

The Hardware Motion Compensation (HWMC) process consists of reconstructing a new picture by predicting (either forward, backward, or bi-directional) the resulting pixel colors from one or more reference pictures. The GMCH receives the video stream and implements Motion Compensation and subsequent steps in hardware. Performing Motion Compensation in hardware reduces the processor demand of software-based MPEG-2 decoding, and thus improves system performance.

5.4.8.3 Sub-picture Support

Sub-picture is used for two purposes: Subtitles for movie captions, which are superimposed on a main picture, and for menus to provide some visual operation environments for the user.

DVD allows movie subtitles to be recorded as sub-pictures. On a DVD disc, it is called “Subtitle” because it has been prepared for storing captions. Since the disc can have a maximum of 32 tracks for Subtitles, they can be used for various applications, for example, as Subtitles in different languages.

There are two kinds of menus, the system menus and other In-Title menus. First, the system menus are displayed and operated at startup of or during the playback of the disc or from the stop state. Second, In-Title menus can be programmed as a combination of sub-picture and highlight commands to be displayed during playback of the disc.

The GMCH supports sub-picture for DVD and DBS by mixing the two video streams via alpha blending. Unlike color keying, alpha blending provides a softer effect and each pixel that is displayed is a composite between the two video stream pixels. The GMCH can utilize four methods when dealing with sub-pictures. This flexibility means that the GMCH can work with all sub-picture formats.

5.5 Display Interface

The GMCH has four dedicated display interfaces, the analog port, the LFP LVDS interface, and the DVO B/C interface. The DVO B and DVO C interface can support TV-out encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device. The data that is sent out the display port is selected from one of the two possible sources; display pipe A or display pipe B.

5.5.1 Analog Display Port Characteristics

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector.

5.5.1.1 Integrated RAMDAC

The display function contains a 350-MHz integrated 24-bit RAM-based Digital-to-Analog Converter (RAMDAC) that transforms up to 2048 x 1536 digital pixels from the graphics and video subsystems to a maximum pixel analog data for the CRT monitor at a maximum refresh rate of 75-Hz for the Intel 852GME GMCH. Three, 8-bit DACs provide the R, G, and B signals to the monitor.

5.5.1.2 DDC (Display Data Channel)

DDC is defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 1 and 2 is implemented.

5.5.2 Digital Display Interface

5.5.2.1 Dedicated LFP LVDS Interface

The GMCH has a dedicated ANSI/TIA/EIA –644-1995 Specification compliant dual channel LFP LVDS interface that can support TFT panel resolutions up to UXGA with a maximum pixel format of 18-bpp, and with SSC supported frequency range from 25-MHz to 112-MHz (single channel/dual channel).

The display pipe selected by the LVDS display port is programmed with the panel timing parameters that are determined by installed panel specifications or read from an onboard EDID ROM. The programmed timing values are then “locked” into the registers to prevent unwanted

corruption of the values. From that point on, the display modes are changed by selecting a different source size for that pipe, programming the VGA registers, or selecting a source size and enabling the VGA. The timing signals will remain stable and active through mode changes. These mode changes include VGA to VGA, VGA to HiRes, HiRes to VGA, and HiRes to HiRes.

The transmitter can operate in a variety of modes and supports several data formats. The serializer supports 6-bit or 8-bit color and single or dual channel operating modes. The display stream from the display pipe is sent to the LVDS transmitter port at the dot clock frequency, which is determined by the panel timing requirements. The output of LVDS is running at a fixed multiple of the dot clock frequency, which is determined by the mode of operation; single or dual channel.

Depending on configuration and mode, a single channel can take 18 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) and output them on three differential data pair outputs; or 24 bits of RGB plus 3 bits of timing control output on four differential data pair outputs. A dual channel interface converts 36 or 48 bits of color information plus the 3 bits of timing control and outputs it on six or eight sets of differential data outputs.

This display port is normally used in conjunction with the pipe functions of panel scaling and 6-8-bit dither. This display port is also used in conjunction with the panel power sequencing and additional associated functions.

When enabled, the LVDS constant current drivers consume significant power. Individual pairs or sets of pairs can be selected to be powered down when not used. When disabled, individual or sets of pairs will enter a low power state. When the port is disabled all pairs enter a low power mode. The panel power sequencing can be set to override the selected power state of the drivers during power sequencing.

For more details on using the GMCH's LFP LVDS interface for TFT Panel support, please refer to the *Common Panel Interface Specification, Rev 1.6* for details on:

- CPIS Supported Resolutions
- CPIS DC/AC Specifications
- CPIS Pin Lists and Connectors
- CPIS EDID Table Outline
- CPIS Reference EDID Formats (XGA at 60-Hz Refresh Rate)
- Sample CPIS EDID DTD's (Primary Resolution at 60-Hz Refresh Rate)
- Video Serialization Formats
- References and External Standards

5.5.2.2 LVDS Interface Signals

LVDS for flat panel is compatible with the ANSI/TIA/EIA-644 specification. This is an electrical standard only defining driver output characteristics and receiver input characteristics. There are two LVDS transmitter channels (channel A and channel B) in the LVDS interface. Each channel consists of 4-data pairs and a clock pair. The interface consists of a total of ten differential signal

pairs of which eight are data and two are clocks. The phase locked transmit clock is transmitted in parallel with the data being sent out over the data pairs and over the LVDS clock pair.

Each channel supports transmit clock frequency ranges from 25-MHz to 112-MHz, which provides a throughput of up to 784-Mbps on each data output and up to 112-MP/s on the input. When using both channels, they each operate at the same frequency each carrying a portion of the data. The maximum pixel rate is increased to 224-MP/s but may be limited to less than that due to restrictions elsewhere in the circuit.

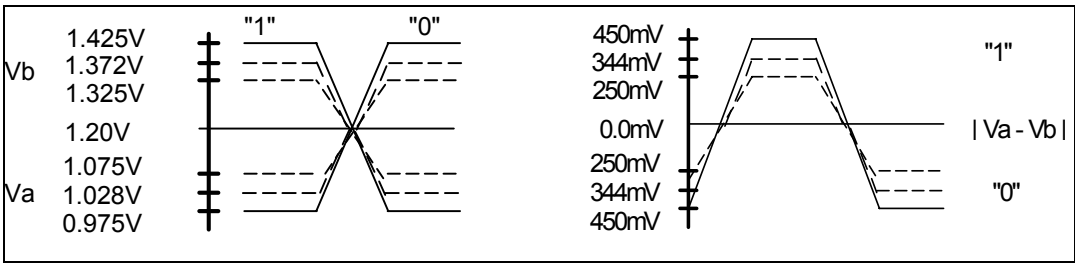
The LVDS Port Enable bit enables or disables the entire LVDS interface. When the port is disabled, it will be in a low power state. Once the port is enabled, individual driver pairs will be disabled based on the operating mode. Disabled drivers can be powered down for reduced power consumption or optionally fixed to forced 0's output.

5.5.2.3 LVDS Data Pairs and Clock Pairs

The LVDS data and clock pairs are identical buffers and differ only in the use defined for that pair. The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals. The pixel bus data to serial data mapping options are specified elsewhere. A single or dual clock pair is used to transfer clocking information to the LVDS receiver. A serial pattern of "1100011" represents 1 cycle of the clock.

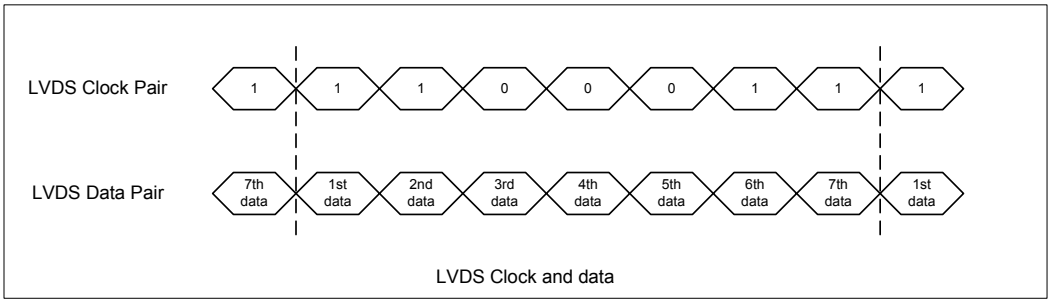
There are two LVDS transmitter channels (channel A and channel B) in the LVDS interface. Each channel contains 1 clock pair and 4-data pair of low voltage differential swing signals. The diagram below shows a pair of LVDS signals and swing voltage.

Figure 10. LVDS Swing Voltage



NOTE: 1's and 0's are represented the differential voltage between the pair of signals.

Figure 11. LVDS Clock and Data Relationship



5.5.2.4 LVDS Pair States

The LVDS pairs can be put into one of five states: powered down tri-state, powered down Zero Volts, common mode, send zeros, or active. When in the active state, several data formats are supported. When in powered down state, the circuit enters a low power state and drives out 0-V or tri-states on both the output pins for the entire channel. The common mode tri-state is both pins of the pair set to the common mode voltage. The common mode state only occurs on B3, A3, or CLKB. These are the signals that optionally get used when driving either 18-bpp panels or dual channel with a single clock. When in the send zeros state, the circuit is powered up but sends only zero for the pixel color data regardless of what the actual data is with the clock lines and timing signals sending the normal clock and timing data.

5.5.2.5 Single Channel versus Dual Channel Mode

Both single channel and dual channel modes are available to allow interfacing to either single or dual channel panel interfaces. This LVDS port can operate in single channel or dual channel mode. Dual channel mode uses twice the number of LVDS pairs and transfers the pixel data at twice the rate of the single channel. In general, one channel will be used for even pixels and the other for odd pixel data. The first pixel of the line is determined by the display enable going active and that pixel will be sent out channel A. All horizontal timings for active, sync, and blank will be limited to two pixel boundaries in the two channel modes.

5.5.2.6 LVDS Channel Skew

When in dual channel mode, the two channels must meet the panel requirements with respect to the inter-channel skew.

5.5.2.7 LVDS PLL

The Display PLL is used to synthesize the clocks that control transmission of the data across the LVDS interface. The three operations that are controlled are the pixel rate, the load rate, and the IO shift rate. These are synchronized to each other and have specific ratios based on single channel or dual channel mode. If the pixel clock is considered the 1x rate, a 7x or 3.5x speed IO_shift clock is needed for the high speed serial outputs setting the data rate of the transmitters. The load clock will have either a 1x or .5x ratio to the pixel clock.

5.5.2.8 SSC Support

The GMCH is designed to tolerate a 0.6%-2.5% down/center spread at a modulation rate range from 30-50 kHz triangle. By using an external SSC clock synthesizer to provide the 66-MHz reference clock into the GMCH Pipe B PLL, spectrally spread 7X, 3.5X, and 1X LVDS clocking is output from the GMCH Pipe B PLL.

5.5.2.9 Panel Power Sequencing

This section provides details for the power sequence timing relationship of the panel power, the backlight enable and the LVDS data timing delivery. In order to meet the panel power timing specification requirements, two signals, PANELVDDEN and PANELBKLTEN are provided to control the timing sequencing function of the panel and the backlight power supplies.

5.5.2.9.1 Panel Power Sequence States

A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state and the LVDS clock and data lines are all managed by an internal power sequencer.

A requested power-up sequence is only allowed to begin after the power cycle delay time requirement T4 is met. This is programmed in the Power Cycle Delay bits (Panel Power Cycle Delay and Reference Divider Register address offset 61210-61213h, bits 0-4).

Figure 12. Panel Power Sequencing

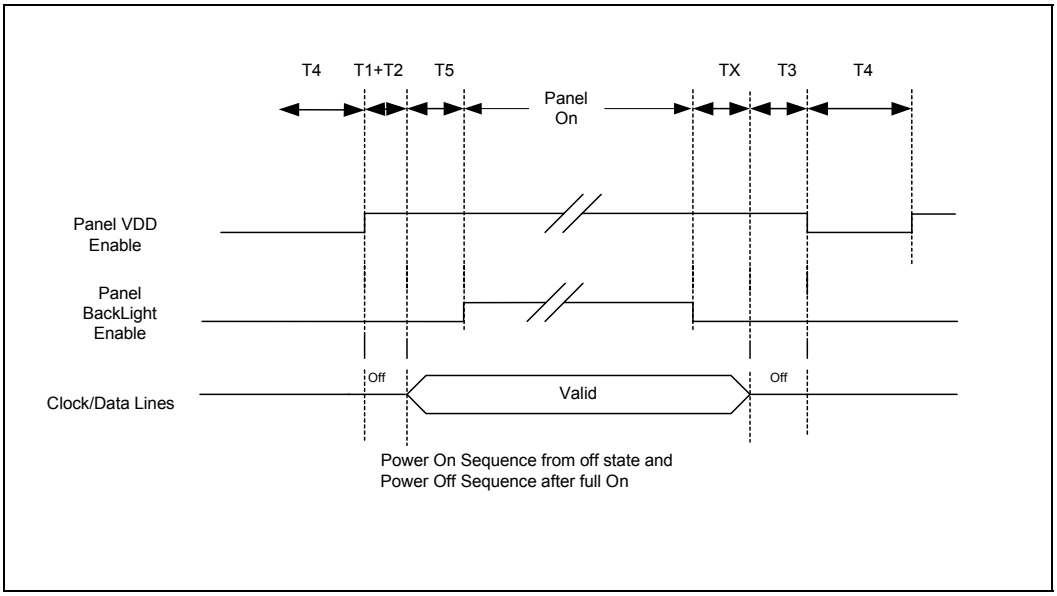


Table 43. Display Configuration Space

Name	Panel Power Sequence Timing Parameters			Min	Max	Units
	Spec Name	From	To			
T1+T2	**Vdd On to LVDS Active** Panel Vdd must be on for a minimum time before the LVDS data stream is enabled.	0.1 Vdd	LVDS Active	0	60	ms
T5	**Backlight** LVDS data must be enabled for a minimum time before the backlight is turned on.	LVDS Active	Backlight on	200		ms
TX	**Backlight State** Backlight must be disabled for a minimum time before the LVDS data stream is stopped.	Backlight Off	LVDS off	X	X	ms
T3	**LVDS State** Data must be off for a minimum time before the panel VDD is turned off.	LVDS Off	Start power off	0	50	ms
T4	**Power cycle Delay** When panel VDD is turned from On to Off, a minimum wait must be satisfied before the panel VDD is enabled again.	Power Off	Power On Sequence Start	400	X	ms

5.5.2.10 Back Light Inverter Control

The GMCH offers integrated PWM for TFT panel Backlight Inverter control. Other methods of control are specified in the *Common Panel Interface Specification*, Version 1.6.

- PWM – based Backlight Brightness Control
- SMBus-based Backlight Brightness Control
- DBL (Display Brightness Link) –to- VDL (Video Data Link) Power Sequencing

5.5.2.11 Digital Display Channel – DVOB and DVOC

The GMCH has the capability to support additional digital display devices (e.g. TMDS transmitter, LVDS transmitter or TV-out encoder) through its digital video output port. DVO B and DVOC can each deliver a 165-MHz dot clock on their 12-bit interface or deliver a 330-MHz dot clock on a combined 24-bit interface.

The digital display port consists of a digital data bus, VSYNC, HSYNC, and BLANK# signals. The data bus can operate in a 12-bit or 24-bit mode. Embedded sync information or HSYNC and VSYNC signals can optionally provide the basic timing information to the external device and the BLANK# signal indicates which clock cycles contain valid data. The BLANK# signal can be optionally selected to include the border area of the timing. The VSYNC and HSYNC signals can be disabled when embedded sync information is to be used or to support DPMS. SYNC polarity can be adjusted using the VGA polarity selection bits or the port configuration bits. Optionally a STALL signal can cause the next line of data to not be sent until the STALL signal is removed. Optionally the FIELD pin can indicate to the overlay which field is currently being displayed at the display device.

5.6 AGP Interface Overview

The GMCH/MCH supports 1.5-V AGP 1x/2x/4x devices. The AGP signal buffers are 1.5-V drive/receive (buffers are not 3.3-volt tolerant). The GMCH/MCH supports 2x/4x source synchronous clocking transfers for read and write data, and sideband addressing. The GMCH/MCH also supports 2x and 4x clocking for Fast Writes initiated from the GMCH/MCH (on behalf of the processor).

AGP PIPE# or SBA[7:0] transactions to DRAM do not get snooped and are, therefore, not coherent with the processor caches. AGP FRAME# transactions to DRAM are snooped. AGP PIPE# and SBA[7:0] accesses to and from the hub interface are not supported. AGP FRAME# access from an AGP master to the hub interface is also not supported. Only the AGP FRAME memory writes from the hub interface are supported.

5.6.1 AGP Target Operations

As an initiator, the GMCH does not initiate cycles using AGP enhanced protocols. The GMCH/MCH supports AGP cycles targeting interface to main memory only. The GMCH supports interleaved AGP PIPE#] and AGP FRAME#, or AGP SBA[7:0] and AGP FRAME# transactions.

Table 44. Display Configuration Space

AGP Command	C/BE[3:0]# Encoding	GMCH/MCH Host Bridge Max	
		Cycle Destination	Response as PCIx Target
Read	0000	Main Memory	Low Priority Read
	0000	The hub interface	Complete locally with random data; does not go to the hub interface
Hi-Priority Read	0001	Main Memory	High Priority Read
	0000	The hub interface	Complete locally with random data; does not go to the hub interface
Reserved	0010	N/A	No Response
Reserved	0011	N/A	No Response
Write	0100	Main Memory	Low Priority Write

AGP Command	C/BE[3:0]# Encoding	GMCH/MCH Host Bridge Max	
		Cycle Destination	Response as PCIx Target
	0100	The hub interface	Cycle goes to DRAM with BE's inactive; does not go to the hub interface
Hi-Priority Write	0101	Main Memory	High Priority Write
	0101	The hub interface	Cycle goes to DRAM with BE's inactive; does not go to the hub interface
Reserved	0110	N/A	No Response
Reserved	0111	N/A	No Response
Long Read	1000	Main Memory	Low Priority Read
		The hub interface	Complete locally with random data; does not go to the hub interface
Hi-Priority Long Read	1001	Main Memory	High Priority Read
		The hub interface	Complete locally with random data; does not go to the hub interface
Flush	1010	GMCH	Complete with QW of Random Data
Reserved	1011	N/A	No Response
Fence	1100	GMCH	No Response - Flag inserted in GMCH request queue
Reserved	1101	N/A	No Response
Reserved	1110	N/A	No Response
Reserved	1111	N/A	No Response

NOTE: N/A refers to a function that is not applicable.

As a target of an AGP cycle, the GMCH/MCH supports all the transactions targeted at main memory (summarized in the table above). The GMCH/MCH supports both normal and high-priority read and write requests. The GMCH/MCH does not support AGP cycles to the hub interface. PIPE# and SBA cycles are assumed not to require coherency management and all AGP initiator accesses to main memory using AGP PIPE# or SBA protocol are treated as non-snoopable cycles. These accesses are directed to the AGP aperture in main memory that is programmed as either uncacheable (UC) memory or write combining (WC) in the processor's MTRRs.

5.6.2 AGP Transaction Ordering

The GMCH observes transaction ordering rules as defined by the *AGP Interface Specification Rev 2.0*.

5.6.3 AGP Signal Levels

The GMCH/MCH supports 1x/2x/4X data transfers using 1.5-V signaling levels.

5.6.4 4x AGP Protocol

In addition to the 1x and 2x AGP protocol, the GMCH/MCH supports 4x AGP read and write data transfers and 4x sideband address generation. The 4x operation is compliant with the AGP 2.0 specification.

The GMCH/MCH indicates that it supports 4x data transfers through RATE[2] (bit 2) of the AGP Status Register. When DATA_RATE[2] of the AGP Command Register is set to 1 during system initialization, the GMCH/MCH performs AGP read/write data transactions using 4x protocol. This bit is not dynamic. Once this bit is set during initialization, the data transfer rate will not change.

The 4x data rate transfer provides 1.06 GB/s transfer rates. The control signal protocol for the 4x data transfer protocol is identical to 1x/2x protocol. In 4x mode 16 bytes of data are transferred on every 66-MHz clock edge. The minimum throttleable block size remains four 66-MHz clocks, which means 64 bytes of data are transferred per block. Three additional signal pins are required to implement the 4x data transfer protocol. These signal pins are complementary data transfer strobes for the AD bus (2) and the SBA bus (1).

5.6.4.1 Fast Writes

The GMCH/MCH supports 2x and 4x Fast Writes from the GMCH/MCH to the graphics controller on AGP. The Fast Write operation is compliant with the AGP 2.0 specification.

The GMCH/MCH will not generate Fast Back to Back (FB2B) cycles in 1x mode, but will generate FB2B cycles in 2x and 4x Fast Write modes.

To use the Fast Write protocol, the Fast Write Enable configuration bit, AGPCMD[FWEN] (bit 4 of the AGP Command Register), must be set to 1.

Memory writes originating from the host or from the hub interface use the Fast Write protocol when it is both capability enabled and enabled. The data rate used to perform the Fast Writes is dependent on the bits set in the AGP Command Register bits 2:0 (DATA_RATE).

- If bit 2 of the AGPCMD[DATA_RATE] field is 1, the data transfers occur using 4x strobing.
- If bit 1 of AGPCMD[DATA_RATE] field is 1, the data transfers occur using 2x strobing.
- If bit 0 of AGPCMD[DATA_RATE] field is 1, Fast Writes are disabled and data transfers occur using standard PCI protocol.

Note that only one of the three DATA_RATE bits may be set by initialization software. This is summarized in the following table.

Table 45. Fast Write Initialization

FWEN	DATA_RATE [2]	DATA_RATE [1]	DATA_RATE [0]	GMCH =>AGP Master Write Protocol
0	X	x	x	1x
1	0	0	1	1x
1	0	1	0	2x Strobing
1	1	0	0	4x Strobing

5.6.4.2 AGP FRAME# Transactions on AGP

The GMCH/MCH accepts and generates AGP FRAME# transactions on the AGP bus. The GMCH/MCH guarantees that AGP FRAME# accesses to DRAM are kept coherent with the processor caches by generating snoops to the host bus. LOCK#, SERR#, and PERR# signals are not supported.

GMCH/MCH Initiator and Target Operations

Table 54 summarizes GMCH/MCH target operation for AGP FRAME# initiators. The cycles can be either destined for main memory or the hub interface.

Table 46. PCI Commands Supported by the GMCH/MCH When Acting as a FRAME# Target

PCI Command	C/BE[3:0]# Encoding	GMCH/MCH	
		Cycle Destination	Response as A FRAME# Target
Interrupt Acknowledge	0000	N/A	No Response
Special Cycle	0001	N/A	No Response
I/O Read	0010	N/A	No Response
I/O Write	0011	N/A	No Response
Reserved	0100	N/A	No Response
Reserved	0101	N/A	No Response
Memory Read	0110	Main Memory	Read
	0110	The hub interface	No Response
Memory Write	0111	Main Memory	Posts Data
	0111	The hub interface	No Response
Reserved	1000	N/A	No Response
Reserved	1001	N/A	No Response
Configuration Read	1010	N/A	No Response

PCI Command	C/BE[3:0]# Encoding	GMCH/MCH	
		Cycle Destination	Response as A FRAME# Target
Configuration Write	1011	N/A	No Response
Memory Read Multiple	1100	Main Memory	Read
	1100	The hub interface	No Response
Dual Address Cycle	1101	N/A	No Response
Memory Read Line	1110	Main Memory	Read
	1110	The hub interface	No Response
Memory Write and Invalidate	1111	Main Memory	Posts Data
	1111	The hub interface	No Response

NOTE: N/A refers to a function that is not applicable.

As a target of an AGP FRAME# cycle, the GMCH/MCH only supports the following transactions:

- *Memory Read, Memory Read Line, and Memory Read Multiple*. These commands are supported identically by the GMCH/MCH. The GMCH/MCH does not support reads of the hub interface bus from AGP.
- *Memory Write and Memory Write and Invalidate*. These commands are aliased and processed identically. The GMCH/MCH does not support writes to the hub interface bus from AGP.
- *Other Commands*. Other commands such as I/O R/W and Configuration R/W are not supported by the GMCH as a target and result in master abort.
- *Exclusive Access*. The GMCH/MCH does not support PCI locked cycles as a target.
- *Fast Back-to-Back Transactions*. GMCH/MCH as a target supports fast back-to-back cycles from an AGP FRAME# initiator.

As an initiator of AGP FRAME# cycle, the GMCH/MCH only supports the following transactions:

- *Memory Read and Memory Read Line*. GMCH/MCH supports reads from host to AGP. GMCH/MCH does not support reads from the hub interface to AGP.
- *Memory Read Multiple*. This command is not supported by the GMCH/MCH as an AGP FRAME# initiator.
- *Memory Write*. GMCH/MCH initiates AGP FRAME# cycles on behalf of the host or the hub interface. GMCH/MCH does not issue Memory Write and Invalidate as an initiator. GMCH/MCH does not support write merging or write collapsing. GMCH/MCH allows non-snoopable write transactions from the hub interface to the AGP bus.
- I/*O Read and Write*. I/O read and write from the host are sent to the AGP bus. I/O base and limit address range for AGP bus are programmed in AGP FRAME# configuration registers.

All other accesses that do not correspond to this programmed address range are forwarded to the hub interface.

- *Exclusive Access*. GMCH/MCH does not issue a locked cycle on the AGP bus on behalf of either the host or the hub interface. The hub interface and host locked transactions to AGP are initiated as unlocked transactions by the GMCH/MCH on the AGP bus.
- *Configuration Read and Write*. Host Configuration cycles to AGP are forwarded as Type 1 Configuration Cycles.
- *Fast Back-to-Back Transactions*. GMCH/MCH as an initiator does not perform fast back-to-back cycles.

GMCH Retry/Disconnect Conditions

The GMCH generates retry/disconnect according to the AGP Specification rules when being accessed as a target from the AGP FRAME# device.

Delayed Transaction

When an AGP FRAME#-to-DRAM read cycle is retried by the GMCH, it is processed internally as a Delayed Transaction.

The GMCH/MCH supports the Delayed Transaction mechanism on the AGP target interface for the transactions issued using AGP FRAME# protocol. This mechanism is compatible with the PCI 2.1 Specification. The process of latching all information required to complete the transaction, terminating with Retry, and completing the request without holding the master in wait-states is called a Delayed Transaction. The GMCH/MCH latches the Address and Command when establishing a Delayed Transaction. The GMCH/MCH generates a Delayed Transaction on the AGP only for AGP FRAME# to DRAM read accesses. The GMCH/MCH does not allow more than one Delayed Transaction access from AGP at any time.

5.7 Power and Thermal Management

The Intel 852GME GMCH and Intel 852PM MCH are intended to be compliant with the following specifications and technologies:

- APM Rev 1.2
- PCI Power Management Rev 1.0
- PC’99, Rev 1.0, PC’99A, and PC’01, Rev 1.0
- ACPI 1.0b and 2.0 support
- ACPI S0, S1-M, S3, S4, S5, C0, C1, C2, C3 states
- Internal Graphics Adapter D0, D1, D3 (Hot/Cold)
- On Die Thermal sensor, enabling core and system memory write thermal throttling for prevention of catastrophic thermal conditions
- External Thermal sensor input pin
- Enabling SO-DIMM Thermal throttling

- The GMCH also reduces I/O power dynamically, by disabling sense amps on input buffers, as well as tri-stating output buffers when possible
- Dynamic Clock Power Down reduces power in all modes of operation
- Enhanced Intel SpeedStep technology
- Flat Panel Power Sequencing

5.8 General Description of Supported CPU States

C0 (Full On): This is the only state that runs software. All clocks are running, STPCLK is deasserted, and the processor core is active. The processor can service snoops and maintain cache coherency in this state.

C1 (Auto Halt): The first level of power reduction occurs when the processor executes an Auto-Halt instruction. This stops the execution of the instruction stream and reduces the processor's power consumption. The processor can service snoops and maintain cache coherency in this state.

C2 (Stop Grant): To enter this low power state, STPCLK is asserted. The processor can still service snoops and maintain cache coherency in this state.

C3 (Sleep or Deep Sleep): In these states the processor clock is stopped. The GMCH/MCH assumes that no hub interface cycles (except special cycles) will occur while the GMCH/MCH is in this state. The processor cannot snoop its caches to maintain coherency while in the C3 state. The GMCH/MCH will transition from the C0 state to the C3 state when software reads the Level 3 Register. This is an ACPI defined register but BIOS or APM (via BIOS) can use this facility when entering a low power state. The Host Clock PLL within the GMCH/MCH can be programmed to be shut off for increased power savings and the GMCH uses the DPSLP signal input for this purpose.

C4 (Deeper Sleep): The C4 state appears to the GMCH/MCH as identical to the C3 state, but in this state the processor core voltage is lowered. There are no internal events in GMCH/MCH for the C4 state that differ from the C3 state.

5.9 General Description of ACPI States

Internal Graphics Adapter:

- D0 Full on, display active
- D1 Low power state, low latency recovery. No display, system memory retained
- D3 Hot - All states lost other than PCI configuration. system memory lost (optionally)
- D3 Cold - Power off

CPU:

- C0 Full On

- C1 Auto Halt
- C2 Stop Clock. Clock to CPU still running. Clock stopped to CPU core.
- C3 Deep Sleep. Clock to CPU stopped.
- C4 Deeper Sleep. Same as C3 with reduced voltage on the CPU.

System States:

- G0/S0 Full On
- G1/S1-M Power On Suspend (POS). System Context Preserved
- G1/S2 Not supported.
- G1/S3 Suspend to RAM (STR). Power and context lost to chipset.
- G1/S4 Suspend to Disk (STD). All power lost (except wakeup on ICH4-M)
- G2/S5 Soft off. Total reboot.

5.10 Enhanced Intel SpeedStep Technology Overview

With Enhanced Intel SpeedStep technology the processor core voltage changes and allows true CPU core frequency changes versus only clock throttling.

Table 47. Enhanced Intel SpeedStep Technology Overview

CPU	Intel Celeron processor, mobile Intel Pentium 4 processor
Benefit Over Non-power Managed CPU	Additional lower voltages and frequencies
Transition Prompt	OS based on CPU load demand, thermal control, or user event based
CPU Availability	CPU unavailability can be restricted to ~10 µs (CPU dependent) by s/w

5.11 External Thermal Sensor Input

An External Thermal sensor with a serial interface may be placed next to DDR SDRAM SO-DIMM (or any other appropriate platform location), or a remote Thermal Diode may be placed next to the SO-DIMM (or any other appropriate platform location) and connected to the External Thermal sensor. Intel advises that the External Thermal sensor contains some form of hysteresis, since none is provided by the GMCH/MCH hardware.

The external sensor can be connected to the ICH4-M via the SMBus interface to allow programming and setup by BIOS software over the serial interface. The External sensor's output should include an Active-Low Open-Drain signal indicating an Over-Temp condition, which remains asserted for as long as the Over-Temp Condition exists, and deasserts when temperature has returned to within normal operating range. This External sensor output will be connected to the GMCH/MCH input (EXTTS_0) and will trigger a Preset Interrupt and/or Read-Throttle on a level-sensitive basis.

Additional External Thermal sensor’s outputs, for multiple sensors, can be wire-OR'ed together to allow signaling from multiple sensors located physically separately. Software can, if necessary, distinguish which SO-DIMM(s) is the source of the over-temp through the serial interface. However, since the SO-DIMM(s) will be located on the same system memory bus data lines, any GMCH/MCH-based Read Throttle will apply equally.

Note: The use of external sensors that include an internal pull-up resistor on the open-drain Thermal trip output is discouraged. However, it may be possible, depending on the size of the pull-up and the voltage of the sensor.

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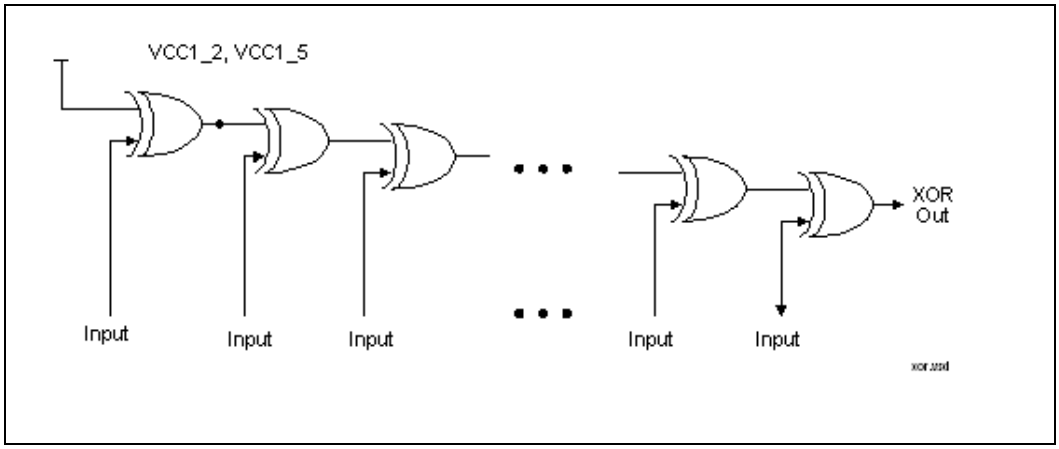
6 Testability

In the Intel 852GME GMCH and Intel 852PM MCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates, each with one input pin connected to it. The XOR Chain test mode is used by product engineers during manufacturing and OEMs during board level connectivity tests. The main purpose of this test mode is to detect connectivity shorts between adjacent pins and to check proper bonding between I/O pads and I/O pins.

Figure 13. XOR-Tree Chain



The algorithm used for in–circuit test is as follows:

1. Drive all input pins to an initial logic level 1. Observe the output corresponding to scan chain being tested.
2. Toggle pins one at a time starting from the first pin in the chain, continuing to the last pin, from its initial logic level to the opposite logic level. Observe the output changes with each pin toggle.

6.1 XOR Chain Differential Pairs

Table 48 provides differential signals in the XOR chains that must be treated as pairs. Pin1and Pin2 as shown need to always drive to the opposite value.

Table 48. Differential Signals in the XOR Chains

Pin1	Pin2	XOR Chain
DVOCCLK#	DVOCCLK	DVO XOR 2
HLSTB#	HLSTB	HUB XOR

6.2 XOR Chain Exclusion List

Table 49 provides a list of pins that are not included in the XOR chains (excluding all VCC/VSS/VTT).

Note: Connectivity column is used to identify what need to be driven on that particular pin during XOR chain test mode.

Table 49. XOR Chains Exclusion list

Item#	IN/OUT	Ball	Pin/VHDL	I/O Type	Voltage	Connectivity
1	IN	Y3	GCLKIN	PLL CLK	3.3	0
2	-	W1	HLVREF	Analog	1/3 VCCHL	0.4
3	-	T2	HLRCOMP	Analog	N/A	N/A
4	-	U2	PSWING	Analog	N/A	N/A
5	-	F1	GVREF	Analog	1/2 VCCDVO	0.75
6	-	D1	DVORCOMP	Analog	N/A	N/A
7	IN	J11	PWROK	CMOS	3.3	N/A
8	IN	B7	DREFCLK	PLL CLK	3.3	0
9	-	E8	REFSET	Analog	N/A	N/A
10	-	C9	BLUE	Analog	N/A	N/A
11	-	D9	BLUE#	Analog	N/A	N/A
12	-	C8	GREEN	Analog	N/A	N/A
13	-	D8	GREEN#	Analog	N/A	N/A
14		A7	RED	Analog	N/A	N/A
15	-	A8	RED#	Analog	N/A	N/A
16	-	D12	LVREFH	Analog	1.1	1.1
17	-	A10	LIBG	Analog	N/A	N/A
18	-	B12	LVBG	Analog	N/A	N/A
19	-	F12	LVREFL	Analog	1.1	1.1
20	IN	B17	DREFSSCLK	PLL CLK	3.3	0
21	-	J17	HDVREF[2]	Analog	2/3 VTTLF	1.0
22	-	B20	HXRCOMP	Analog	N/A	N/A
23	-	B18	HXSWING	Analog	N/A	N/A
24	-	J21	HDVREF[1]	Analog	2/3 VTTLF	1.0
25	IN	AD29	BCLK#	Diff	0.7	0
26	IN	AE29	BCLK	Diff	0.7	0.7
27	-	K21	HDVREF[0]	Analog	2/3 VTTLF	1.0
28	-	Y28	HCCVREF	Analog	2/3 VTTLF	1.0

Item#	IN/OUT	Ball	Pin/VHDL	I/O Type	Voltage	Connectivity
29	-	Y22	HAVREF	Analog	2/3 VTTLF	1.0
30	-	H28	HYRCOMP	Analog	N/A	N/A
31	-	K28	HYSWING	Analog	N/A	N/A
32	IN	D28	RSTIN#	CMOS	3.3	N/A
33	-	AJ24	SMVREF_0	Analog	1/2 VCCSM	1.25
34	-	AB1	SMRCOMP	Analog	N/A	N/A

6.3 XOR Chain Connectivity/Ordering

The following tables contain the ordering for all of the Intel 852GME GMCH and Intel 852PM MCH XOR chains and pin to ball mapping information:

Table 50. XOR Mapping

XOR Chain DVO 1					
XOR Out	DVO IN/OUT	Ball	Pin/VHDL	I/O Type	Voltage
	OUT	AB5	SMA[12]	SSTL_2	2.5
1	INOUT	T6	RSVD	DVO	1.5
2	INOUT	T5	RSVD	DVO	1.5
3	INOUT	T7	MDDCDATA	DVO	1.5
4	INOUT	R3	RSVD	DVO	1.5
5	INOUT	R4	RSVD	DVO	1.5
6	INOUT	R6	RSVD	DVO	1.5
7	INOUT	R5	RSVD	DVO	1.5
8	INOUT	P2	RSVD	DVO	1.5
9	INOUT	P4	RSVD	DVO	1.5
10	INOUT	P3	RSVD	DVO	1.5
11	INOUT	P6	RSVD	N/A	N/A
12	INOUT	P5	RSVD	N/A	N/A
13	INOUT	N2	RSVD	N/A	N/A
14	INOUT	N3	RSVD	N/A	N/A
15	INOUT	M1	RSVD	N/A	N/A
16	INOUT	N5	RSVD	N/A	N/A
17	INOUT	M2	RSVD	N/A	N/A
18	INOUT	M5	RSVD	N/A	N/A

19	INOUT	M3	DVOBCCLKINT	DVO	1.5
20	INOUT	L2	RSVD	N/A	N/A
21	INOUT	P7	MDDCCLK	DVO	1.5
22	INOUT	N6	MI2CDATA	DVO	1.5
23	INOUT	M6	MDVIDATA	DVO	1.5
24	INOUT	N7	MDVICLK	DVO	1.5
25	INOUT	L7	DVODETECT	DVO	1.5
26	INOUT	K7	MI2CCLK	DVO	1.5
27	OUT	B2	RSVD	N/A	N/A
28	IN	B3	RSVD	N/A	N/A
XOR Chain DVO 2					
XOR Out	**DVO IN/OUT**	**Ball**	**Pin/VHDL**	**I/O Type**	**Voltage**
	OUT	AD5	SMA[11]	SSTL_2	2.5
1	INOUT	L3	DVOCBLANK#	DVO	1.5
2	INOUT	K1	DVOCD[1]	DVO	1.5
3	INOUT	L4	RSVD	DVO	N/A
4	INOUT	L5	DVOCVSYNC	DVO	1.5
5	INOUT	K2	DVOCD[3]	DVO	1.5
6	INOUT	K5	DVOCD[0]	DVO	1.5
7	INOUT	K3	DVOCD[2]	DVO	1.5
8	INOUT	J2	DVOCCLK#	DVO	1.5
9	INOUT	J3	DVOCCLK	DVO	1.5
10	INOUT	H2	DVOCD[6]	DVO	1.5
11	INOUT	J5	DVOCD[5]	DVO	1.5
12	INOUT	H1	DVOCD[7]	DVO	1.5
13	INOUT	J6	DVOCD[4]	DVO	1.5
14	INOUT	K6	DVOCHSYNC	DVO	1.5
15	INOUT	H4	DVOCD[9]	DVO	1.5
16	INOUT	H3	DVOCD[8]	DVO	1.5
17	INOUT	H5	DVOCFLDSTL	DVO	1.5
18	INOUT	H6	DVOCD[10]	DVO	1.5
19	INOUT	G2	DVOBCINT#	DVO	1.5
20	INOUT	G3	DVOCD[11]	DVO	1.5
21	IN	D2	RSVD	N/A	N/A
22	IN	D3	RSVD	N/A	N/A
23	IN	F4	ADDID[5]	DVO	1.5

24	IN	F5	ADDID[1]	DVO	1.5
25	IN	F6	ADDID[7]	DVO	1.5
26	IN	E2	ADDID[3]	DVO	1.5
27	IN	E5	ADDID[0]	DVO	1.5
28	IN	F3	RSVD	N/A	N/A
29	IN	F2	RSVD	N/A	N/A
30	OUT	C2	RSVD	N/A	N/A
31	IN	E3	ADDID[2]	DVO	1.5
32	OUT	C3	GST[1]	DVO	1.5
33	OUT	C4	GST[0]	DVO	1.5
34	IN	G5	ADDID[4]	DVO	1.5
35	IN	G6	ADDID[6]	DVO	1.5
36	IN	D5	DPMS	DVO	1.5
XOR Chain PSB 1					
XOR Out	**IN/OUT**	**Ball**	**Pin**	**I/O Type**	**Voltage**
	OUT	AC19	SMA[10]	SSTL_2	2.5
1	INOUT	D16	HD[62]#	AGTL+	1.5
2	INOUT	C16	HD[60]#	AGTL+	1.5
3	INOUT	G16	HD[58]#	AGTL+	1.5
4	INOUT	C17	HD[55]#	AGTL+	1.5
5	INOUT	E17	HD[61]#	AGTL+	1.5
6	INOUT	E16	HD[59]#	AGTL+	1.5
7	INOUT	F17	HD[56]#	AGTL+	1.5
8	INOUT	B19	HD[57]#	AGTL+	1.5
9	INOUT	E18	HDSTBP[3]#	AGTL+	1.5
10	INOUT	D18	HDSTBN[3]#	AGTL+	1.5
11	INOUT	C18	HD[63]#	AGTL+	1.5
12	INOUT	G17	HD[51]#	AGTL+	1.5
13	INOUT	C19	HD[54]#	AGTL+	1.5
14	INOUT	D20	HD[52]#	AGTL+	1.5
15	INOUT	E20	HD[50]#	AGTL+	1.5
16	INOUT	E19	HD[49]#	AGTL+	1.5
17	INOUT	G19	DINV[3]#	AGTL+	1.5
18	INOUT	F19	HD[53]#	AGTL+	1.5
19	INOUT	G18	HD[48]#	AGTL+	1.5
20	INOUT	B21	HD[32]#	AGTL+	1.5

21	INOUT	C20	HD[46]#	AGTL+	1.5
22	INOUT	C23	HD[35]#	AGTL+	1.5
23	INOUT	B23	HD[43]#	AGTL+	1.5
24	INOUT	B22	HD[42]#	AGTL+	1.5
25	INOUT	B25	DINV[2]#	AGTL+	1.5
26	INOUT	D22	HD[36]#	AGTL+	1.5
27	INOUT	C24	HD[34]#	AGTL+	1.5
28	INOUT	C21	HD[47]#	AGTL+	1.5
29	INOUT	E21	HDSTBP[2]#	AGTL+	1.5
30	INOUT	E22	HDSTBN[2]#	AGTL+	1.5
31	INOUT	D24	HD[39]#	AGTL+	1.5
32	INOUT	C25	HD[37]#	AGTL+	1.5
33	INOUT	F21	HD[45]#	AGTL+	1.5
34	INOUT	E24	HD[38]#	AGTL+	1.5
35	INOUT	E23	HD[41]#	AGTL+	1.5
36	INOUT	G21	HD[33]#	AGTL+	1.5
37	INOUT	F23	HD[44]#	AGTL+	1.5
38	INOUT	G20	HD[40]#	AGTL+	1.5
39	OUT	M27	RS[2]#	AGTL+	1.5
40	OUT	P28	BPRI#	AGTL+	1.5
41	OUT	AA22	DPWR#	AGTL+	1.5
42	INOUT	AA26	HADSTB[1]#	AGTL+	1.5
XOR Chain PSB 2					
XOR Out	**IN/OUT**	**Ball**	**Pin**	**I/O Type**	**Voltage**
	OUT	AC5	SMA[9]	SSTL_2	2.5
1	INOUT	E25	DINV[1]#	AGTL+	1.5
2	INOUT	B26	HD[26]#	AGTL+	1.5
3	INOUT	C26	HD[28]#	AGTL+	1.5
4	INOUT	B27	HD[18]#	AGTL+	1.5
5	INOUT	B28	HD[31]#	AGTL+	1.5
6	INOUT	G23	HD[30]#	AGTL+	1.5
7	INOUT	E26	HD[9]#	AGTL+	1.5
8	INOUT	D26	HDSTBP[1]#	AGTL+	1.5
9	INOUT	C27	HDSTBN[1]#	AGTL+	1.5
10	INOUT	G22	HD[27]#	AGTL+	1.5
11	INOUT	G24	HD[24]#	AGTL+	1.5

12	INOUT	C28	HD[25]#	AGTL+	1.5
13	INOUT	E27	HD[20]#	AGTL+	1.5
14	INOUT	F2	HD[17]#	AGTL+	1.5
15	INOUT	D27	HD[23]#	AGTL+	1.5
16	INOUT	G25	HD[21]#	AGTL+	1.5
17	INOUT	F25	HD[16]#	AGTL+	1.5
18	INOUT	H23	HD[19]#	AGTL+	1.5
19	INOUT	F28	HD[22]#	AGTL+	1.5
20	INOUT	K23	HD[11]#	AGTL+	1.5
21	INOUT	J23	HD[14]#	AGTL+	1.5
22	INOUT	H25	HD[10]#	AGTL+	1.5
23	INOUT	G27	HD[12]#	AGTL+	1.5
24	INOUT	K22	HD[0]#	AGTL+	1.5
25	INOUT	H26	HD[15]#	AGTL+	1.5
26	INOUT	G28	HD[5]#	AGTL+	1.5
27	INOUT	H27	HD[1]#	AGTL+	1.5
28	INOUT	J24	HD[9]#	AGTL+	1.5
29	INOUT	L23	HD[7]#	AGTL+	1.5
30	INOUT	K25	HD[2]#	AGTL+	1.5
31	INOUT	K27	HDSTBP[0]#	AGTL+	1.5
32	INOUT	J28	HDSTBN[0]#	AGTL+	1.5
33	INOUT	J25	DINV[0]#	AGTL+	1.5
34	INOUT	K26	HD[13]#	AGTL+	1.5
35	INOUT	L24	HD[3]#	AGTL+	1.5
36	INOUT	L25	HD[8]#	AGTL+	1.5
37	INOUT	L27	HD[6]#	AGTL+	1.5
38	INOUT	J27	HD[4]#	AGTL+	1.5
39	OUT	M28	DEFER#	AGTL+	1.5
40	OUT	N23	RS[0]#	AGTL+	1.5
41	OUT	P26	RS[1]#	AGTL+	1.5
42	INOUT	T26	HADSTB[0]#	AGTL+	1.5
XOR Chain PSB 3					
XOR Out	**IN/OUT**	**Ball**	**Pin**	**I/O Type**	**Voltage**
	OUT	AC6	SMA[8]	SSTL_2	2.5
1	OUT	F15	CPURST#	AGTL+	1.5
2	IN	Y23	DPSLP#	CMOS	1.5

3	INOUT	N27	HIT#	AGTL+	1.5
4	INOUT	N28	HITM#	AGTL+	1.5
5	INOUT	N25	BNR#	AGTL+	1.5
6	INOUT	N24	DRDY#	AGTL+	1.5
7	IN	P27	HLOCK#	AGTL+	1.5
8	INOUT	M23	BREQ0#	AGTL+	1.5
9	OUT	M25	HTRDY#	AGTL+	1.5
10	INOUT	M26	DBSY#	AGTL+	1.5
11	INOUT	L28	ADS#	AGTL+	1.5
12	INOUT	R28	HREQ[0]#	AGTL+	1.5
13	INOUT	P25	HREQ[1]#	AGTL+	1.5
14	INOUT	T28	HA[5]#	AGTL+	1.5
15	INOUT	R27	HA[6]#	AGTL+	1.5
16	INOUT	R23	HREQ[2]#	AGTL+	1.5
17	INOUT	R24	HA[9]#	AGTL+	1.5
18	INOUT	T27	HA[13]#	AGTL+	1.5
19	INOUT	U28	HA[10]#	AGTL+	1.5
20	INOUT	P23	HA[3]#	AGTL+	1.5
21	INOUT	T25	HA[4]#	AGTL+	1.5
22	INOUT	R25	HREQ[3]#	AGTL+	1.5
23	INOUT	V27	HA[14]#	AGTL+	1.5
24	INOUT	U27	HA[12]#	AGTL+	1.5
25	INOUT	V28	HA[11]#	AGTL+	1.5
26	INOUT	T23	HREQ[4]#	AGTL+	1.5
27	INOUT	U24	HA[8]#	AGTL+	1.5
28	INOUT	U23	HA[7]#	AGTL+	1.5
29	INOUT	V26	HA[16]#	AGTL+	1.5
30	INOUT	U25	HA[15]#	AGTL+	1.5
31	INOUT	V25	HA[18]#	AGTL+	1.5
32	INOUT	Y26	HA[30]#	AGTL+	1.5
33	INOUT	W28	HA[28]#	AGTL+	1.5
34	INOUT	W25	HA[20]#	AGTL+	1.5
35	INOUT	V23	HA[19]#	AGTL+	1.5
36	INOUT	W27	HA[25]#	AGTL+	1.5
37	INOUT	Y25	HA[21]	AGTL+	1.5
38	INOUT	W24	HA[23]#	AGTL+	1.5
39	INOUT	Y27	HA[26]#	AGTL+	1.5

40	INOUT	Y24	HA[17]#	AGTL+	1.5
41	INOUT	AA27	HA[22]#	AGTL+	1.5
42	INOUT	W23	HA[24]#	AGTL+	1.5
43	INOUT	AB28	HA[31]#	AGTL+	1.5
44	INOUT	AB27	HA[29]#	AGTL+	1.5
45	INOUT	AA28	HA[27]	AGTL+	1.5
XOR Chain GPIO					
XOR Out	**IN/OUT**	**Ball**	**Pin**	**I/O Type**	**Voltage**
	OUT	AD7	SMA[7]	SSTL_2	2.5
1	OUT	G8	PANELBKLTCTL	CMOS	3.3
2	OUT	F8	PANELBKLTEN	CMOS	3.3
3	OUT	C6	LCLKCTLB	CMOS	3.3
4	IN	D6	EXTTS_0	CMOS	3.3
5	OUT	F7	AGPBUSY#	CMOS	3.3
6	IN	D7	RSVD	N/A	N/A
7	INOUT	C5	DDCPDATA	CMOS	3.3
8	INOUT	B4	DDCPCLK	CMOS	3.3
9	OUT	H10	HSYNC	CMOS	3.3
10	OUT	A5	PANELVDDEN	CMOS	3.3
11	INOUT	B6	DDCACLK	CMOS	3.3
12	OUT	J9	VSYNC	CMOS	3.3
13	INOUT	G9	DDCADATA	CMOS	3.3
14	OUT	H9	LCLKCTLA	CMOS	3.3
XOR Chain HUB					
XOR Out	**IN/OUT**	**Ball**	**Pin**	**I/O Type**	**Voltage**
	OUT	AD8	SMA[6]	SSTL_2	2.5
1	INOUT	W2	HL[4]	HL1.5	1.2
2	INOUT	W6	HL[5]	HL1.5	1.2
3	INOUT	W7	HL[7]	HL1.5	1.2
4	INOUT	V6	HL[6]	HL1.5	1.2
5	INOUT	W3	HLSTB	HL1.5	1.2
6	INOUT	V2	HLSTB#	HL1.5	1.2
7	IN	V5	Hl[9]	HL1.5	1.2
8	INOUT	V4	HL[10]	HL1.5	1.2
9	INOUT	V3	HL[3]	HL1.5	1.2
10	INOUT	U4	HL[1]	HL1.5	1.2

11	INOUT	U3	HL[2]	HL1.5	1.2
12	INOUT	U7	HL[0]	HL1.5	1.2
13	OUT	T3	HL[8]	HL1.5	1.2
XOR Chain LVDS					
XOR Out	**IN/OUT**	**Ball**	**Pin**	**I/O Type**	**Voltage**
	OUT	AD17	SMA[3]	SSTL_2	2.5
1	INOUT	F10	ICLKBP	LVDS	1.5
2	INOUT	E10	ICLKBM	LVDS	1.5
3	INOUT	G10	IYBP[3]	LVDS	1.5
4	INOUT	G11	IYBM[3]	LVDS	1.5
5	INOUT	G12	IYBP[0]	LVDS	1.5
6	INOUT	H12	IYBM[0]	LVDS	1.5
7	INOUT	E11	IYBP[1]	LVDS	1.5
8	INOUT	E12	IYBM[1]	LVDS	1.5
9	INOUT	C11	IYBP[2]	LVDS	1.5
10	INOUT	C12	IYBM[2]	LVDS	1.5
11	INOUT	E13	ICLKAP	LVDS	1.5
12	INOUT	D14	ICLKAM	LVDS	1.5
13	INOUT	B13	IYAP[3]	LVDS	1.5
14	INOUT	C13	IYAM[3]	LVDS	1.5
15	INOUT	F14	IYAP[0]	LVDS	1.5
16	INOUT	G14	IYAM[0]	LVDS	1.5
17	INOUT	C14	IYAP[2]	LVDS	1.5
18	INOUT	C15	IYAM[2]	LVDS	1.5
19	INOUT	E14	IYAP[1]	LVDS	1.5
20	INOUT	E15	IYAM[1]	LVDS	1.5
XOR Chain SM1					
XOR Out	**DDR SDRAM IN/OUT**	**Ball**	**Pin**	**I/O Type**	**Voltage**
	OUT	AD23	SCS[0]#	SSTL_2	2.5
1	INOUT	AE27	SDQ[62]	SSTL_2	2.5
2	INOUT	AD27	SDQ[63]	SSTL_2	2.5
3	INOUT	AF26	SDQ[61]	SSTL_2	2.5
4	INOUT	AG26	SDQ[60]	SSTL_2	2.5
5	OUT	AC25	SCS[3]#	SSTL_2	2.5
6	OUT	AD24	SDM[6]	SSTL_2	2.5

7	INOUT	AH24	SDQS[6]	SSTL_2	2.5
8	OUT	AD25	SWE#	SSTL_2	2.5
9	OUT	AC18	SMA[0]	SSTL_2	2.5
10	INOUT	AH17	SDQS[4]	SSTL_2	2.5
11	OUT	AD19	SDM[4]	SSTL_2	2.5
12	CLK	AC26	SCK[1]	SSTL_2	2.5
13	CLK	AB23	SCK[4]	SSTL_2	2.5
14	CLK	AA3	SCK[5]	SSTL_2	2.5
15	CLK	AC2	SCK[3]	SSTL_2	2.5
16	CLK	AB2	SCK[0]	SSTL_2	2.5
17	CLK	AC3	SCK[2]	SSTL_2	2.5
18	OUT	AH15	SDM[8]	SSTL_2	2.5
19	INOUT	AF17	RSVD	N/A	N/A
20	INOUT	AF16	RSVD	N/A	N/A
21	INOUT	AG16	RSVD	N/A	N/A
22	INOUT	AE15	RSVD	N/A	N/A
23	INOUT	AH14	RSVD	N/A	N/A
24	INOUT	AE17	RSVD	N/A	N/A
25	INOUT	AD15	SDQS[8]	SSTL_2	2.5
26	INOUT	AE14	RSVD	N/A	N/A
27	INUT	AG14	RSVD	N/A	N/A
28	INOUT	AH8	SDQS[2]	SSTL_2	2.5
29	OUT	AE9	SDM[2]	SSTL_2	2.5
30	OUT	AC7	SCKE[0]	SSTL_2	2.5
31	INOUT	AG2	SDQS[0]	SSTL_2	2.5
32	OUT	AE5	SDM[0]	SSTL_2	2.5
XOR Chain SM2					
XOR Out	**DDR SDRAM IN/OUT**	**Ball**	**Pin**	**I/O Type**	**Voltage**
	OUT	AD26	SCS[1]#	SSTL_2	2.5
1	INOUT	AF28	SDQ[59]	SSTL_2	2.5
2	INOUT	AG28	SDQ[58]	SSTL_2	2.5
3	INOUT	AH27	SDQS[7]	SSTL_2	2.5
4	OUT	AH28	SDM[7]	SSTL_2	2.5
5	INOUT	AE26	SDQ[57]	SSTL_2	2.5
6	INOUT	AH26	SDQ[56]	SSTL_2	2.5

7	INOUT	AH25	SDQ[51]	SSTL_2	2.5
8	INOUT	AG25	SDQ[55]	SSTL_2	2.5
9	INOUT	AF25	SDQ[54]	SSTL_2	2.5
10	INOUT	AE24	SDQ[50]	SSTL_2	2.5
11	INOUT	AH23	SDQ[49]	SSTL_2	2.5
12	INOUT	AF23	SDQ[53]	SSTL_2	2.5
13	INOUT	AE23	SDQ[48]	SSTL_2	2.5
14	INOUT	AG23	SDQ[52]	SSTL_2	2.5
15	INOUT	AE21	SDQS[5]	SSTL_2	2.5
16	OUT	AD21	SDM[5]	SSTL_2	2.5
17	OUT	AD20	SBA[1]	SSTL_2	2.5
18	OUT	AD22	SBA[0]	SSTL_2	2.5
19	OUT	AC21	SRAS#	SSTL_2	2.5
20	OUT	AC15	RCVENOUT#	SSTL_2	2.5
21	INOUT	AC16	RCVENIN#	SSTL_2	2.5
22	CLK	AB24	SCK[4]#	SSTL_2	2.5
23	CLK	AB25	SCK[1]#	SSTL_2	2.5
24	CLK	AB4	SCK[5]#	SSTL_2	2.5
25	CLK	AA2	SCK[0]#	SSTL_2	2.5
26	CLK	AD2	SCK[3]#	SSTL_2	2.5
27	CLK	AD4	SCK[2]#	SSTL_2	2.5
28	OUT	AD10	SMAB[5]	SSTL_2	2.5
29	OUT	AD14	SMA[1]	SSTL_2	2.5
30	OUT	AD16	SMAB[1]	SSTL_2	2.5
31	OUT	AD13	SMA[2]	SSTL_2	2.5
32	OUT	AF11	SMAB[4]	SSTL_2	2.5
33	OUT	AC12	SMAB[2]	SSTL_2	2.5
34	OUT	AC13	SMA[5]	SSTL_2	2.5
35	INOUT	AE12	SDQS[3]	SSTL_2	2.5
36	OUT	AH12	SDM[3]	SSTL_2	2.5
37	OUT	AD11	SMA[4]	SSTL_2	2.5
38	OUT	AC10	SCKE[3]	SSTL_2	2.5
39	OUT	AE6	SDM[1]	SSTL_2	2.5
40	INOUT	AH5	SDQS[1]	SSTL_2	2.5
41	OUT	AC9	SCKE[2]	SSTL_2	2.5
42	OUT	AB7	SCKE[1]	SSTL_2	2.5

XOR Chain SM 3					
XOR Out	**DDR SDRAM IN/OUT**	**Ball**	**Pin**	**I/O Type**	**Voltage**
	OUT	AC22	SCS[2]#	SSTL_2	2.5
1	OUT	AC24	SCAS#	SSTL_2	2.5
2	INOUT	AG22	SDQ[47]	SSTL_2	2.5
3	INOUT	AH22	SDQ[43]	SSTL_2	2.5
4	INOUT	AF22	SDQ[42]	SSTL_2	2.5
5	INOUT	AG20	SDQ[41]	SSTL_2	2.5
6	INOUT	AF20	SDQ[44]	SSTL_2	2.5
7	INOUT	AH21	SDQ[46]	SSTL_2	2.5
8	INOUT	AH19	SDQ[45]	SSTL_2	2.5
9	INOUT	AH20	SDQ[40]	SSTL_2	2.5
10	INOUT	AH16	SDQ[32]	SSTL_2	2.5
11	INOUT	AD18	SDQ[36]	SSTL_2	2.5
12	INOUT	AG19	SDQ[39]	SSTL_2	2.5
13	INOUT	AH18	SDQ[38]	SSTL_2	2.5
14	INOUT	AF19	SDQ[34]	SSTL_2	2.5
15	INOUT	AE18	SDQ[37]	SSTL_2	2.5
16	INOUT	AG17	SDQ[33]	SSTL_2	2.5
17	INOUT	AE20	SDQ[35]	SSTL_2	2.5
18	INOUT	AG13	SDQ[26]	SSTL_2	2.5
19	INOUT	AF14	SDQ[27]	SSTL_2	2.5
20	INOUT	AF13	SDQ[30]	SSTL_2	2.5
21	INOUT	AH13	SDQ[31]	SSTL_2	2.5
22	INOUT	AD12	SDQ[29]	SSTL_2	2.5
23	INOUT	AH10	SDQ[24]	SSTL_2	2.5
24	INOUT	AH11	SDQ[25]	SSTL_2	2.5
25	INOUT	AG11	SDQ[28]	SSTL_2	2.5
26	INOUT	AF10	SDQ[22]	SSTL_2	2.5
27	INOUT	AE11	SDQ[23]	SSTL_2	2.5
28	INOUT	AG10	SDQ[19]	SSTL_2	2.5
29	INOUT	AF8	SDQ[16]	SSTL_2	2.5
30	INOUT	AH9	SDQ[18]	SSTL_2	2.5
31	INOUT	AD9	SDQ[21]	SSTL_2	2.5
32	INOUT	AH7	SDQ[20]	SSTL_2	2.5

33	INOUT	AG8	SDQ[17]	SSTL_2	2.5
34	INOUT	AF7	SDQ[14]	SSTL_2	2.5
35	INOUT	AG7	SDQ[10]	SSTL_2	2.5
36	INOUT	AE8	SDQ[11]	SSTL_2	2.5
37	INOUT	AH6	SDQ[15]	SSTL_2	2.5
38	INOUT	AF5	SDQ[12]	SSTL_2	2.5
39	INOUT	AD6	SDQ[8]	SSTL_2	2.5
40	INOUT	AH4	SDQ[13]	SSTL_2	2.5
41	INOUT	AG5	SDQ[9]	SSTL_2	2.5
42	INOUT	AH2	SDQ[3]	SSTL_2	2.5
43	INOUT	AF4	SDQ[2]	SSTL_2	2.5
44	INOUT	AG4	SDQ[6]	SSTL_2	2.5
45	INOUT	AH3	SDQ[7]	SSTL_2	2.5
46	INOUT	AF2	SDQ[0]	SSTL_2	2.5
47	INOUT	AD3	SDQ[4]	SSTL_2	2.5
48	INOUT	AE3	SDQ[1]	SSTL_2	2.5
49	INOUT	AE2	SDQ[5]	SSTL_2	2.5

6.4 VCC/VSS Voltage Groups

Table 51. Voltage Levels and Ball Out for Voltage Groups

Name	Voltage Level	Ball out
VCC	1.2	H14,J15,N14,N16,P13,P15,P17,R14,R16,T13,T15, T17,U14,U16,W21,AA15,AA17,AA19
VCCADAC	1.5	A9,B9
VCCDVO	1.5	E1,E4,E6,H7,J1,J4,J8,K9,L8,M4,M8,M9,N1,N8,P9,R8
VCCASM	1.2	AD1,AF1
VCCDLVDS	1.5	B14,B15,G13,J13
VCCGPIO	3.3	A3,A4
VCCHL	1.2	U6,U8,V1,V7,V9,W5,W8,Y1
VCCQSM	2.5	AJ6,AJ8
VCCSM	2.5	Y4,Y7,Y9,AA6,AA8,AA11,AA13,AB3,AB6,AB8,AB10, AB12,AB14,AB16,AB18,AB20,AB22,AC1,AC29,AF3, AF6,AF9,AF12,AF15,AF18,AF21,AF24,AF27,AF29, AG1,AG29,AJ5,AJ9,AJ13,AJ17,AJ21,AJ25
VCCTXLVDS	2.5	A12,B10,D10,F9

Name	Voltage Level	Ball out
VTTHF	1.5	A22,A24,H29,M29,V29
VTTLF	1.5	A18,A20,A26,F29,G15,H16,H18,H20,H22,J19,K29,L21, M22,N21,P22,R21,T22,U21,V22,Y29,AB29
VSS	0	A13,A17,A19,A21,A23,A25,A27,B5,B24,C1,C7,C10,C22,C29, D4,D11,D13,D15,D17,D19,D21,D23,D25,D28,E7,E9,E28,E29, F11,F13,F16,F18,F20,F22,F24,F27,G1,G4,G7,G26,G29,H8,H11, H13,H15,H17,H19,H21,H24,J7,J10,J12,J14,J16,J18,J20,J22,J26, J29,K4,K8,K24,L1,L6,L9,L22,L26,L29,M7,M21,M24,N4,N9,N13, N15,N17,N22,N26,N29,P8,P14,P16,P21,P24,R2,R7,R9,R13,R15, R17,R22,R26,T4,T8,T9,T14,T16,T21,T24,U1,U5,U9,U13,U15, U17,U22,U26,U29,V8,V21,V24,W4,W9,W22,W26,W29,Y5,Y6, Y8,Y21,AA1,AA4,AA7,AA10,AA12,AA14,AA16,AA18,AA20, AA21,AA23,AA24,AA25,AA29,AB9,AB11,AB13,AB15,AB17, AB19,AB21,AB26,AC4,AC8,AC11,AC14,AC17,AC20,AC23, AC27,AC28,AE1,AE4,AE7,AE10,AE13,AE16,AE19,AE22,AE25, AE28,AG3,AG6,AG9,AG12,AG15,AG18,AG21,AG24,AG27,AJ1, AJ3,AJ7,AJ10,AJ11,AJ12,AJ18,AJ20,AJ23,AJ26,AJ27

6.5 Power Sequence Recommendation

Power supplies on Intel 852GME GMCH and Intel 852PM MCH:

PSB	VTT (mobile Intel Pentium 4 processor, Intel Celeron processor)
Core	1.5 V
Hub Interface	1.5V
DVO	1.5 V (Intel 852GME GMCH Only)
DAC	1.5 V (Intel 852GME GMCH Only)
Internal Thermal Sensor	1.5 V
LVDS	2.5 V and 1.5 V (Intel 852GME GMCH Only)
DDR	2.5 V
SDRAM	3.3 V
GPIO	3.3 V

Table 52. State of Power Planes in C/S States

Power	C0-C2	C3 GV1/C4	S1	S3	S4/S4+
SDRAM I/O	On	On	On	On	Off
HUB I/O	On	On	On	Off	Off
DVO I/O	On	On	On	Off	Off
PSB I/O	On	On	On	Off	Off
CORE	On	On	On	Off	Off
LVDS I/O	On	On	Off	Off	Off
GPIO	On	On	On	Off	Off

For further details, refer to the *Mobile Intel® Pentium® 4 Processor with 533 MHz System Bus Datasheet* and the *Intel® Celeron® Processor Datasheet.*

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7 Intel 852GME GMCH and 852PM MCH Strap Pins

7.1 Strapping Configuration Table

Table 53. Strapping Signals and Configuration

Pin Name	Strap Description	Configuration	I/F Type	Buffer Type
LCLKCTLB	CPU Strap	*Low=(default) High = Mobile Intel Pentium 4 processor /Intel Celeron processor	GPIO	OUT
HSYNC	XOR Chain Test	Low = Normal Ops (Default) High = XOR Test On	GPIO	OUT
VSYNC	ALL Z Test	Low = Normal Ops (Default) High = AllZ Test On	GPIO	OUT
DVODETECT	§DVO Select (If DVODETECT=0 during Reset, ADDID[7:0] is latched to the ADDID Register)	Low = DVO (Default)	DVO	BI
GPAR	DVO/AGP Select (Reserved)	Low = DVO (Default) High = AGP	AGP	BI
GSBA[7:0]	8-bit ADD Identifier Straps SBA[0] = ID Bit_0 … SBA[7] = ID Bit_7	No default	AGP	IN
GST[2] **Note:** Intel 852GME GMCH Only	§Clock Config: Bit_2 PSB 400 = 0 PSB 533 = 1	];	DVO	Hi-Z
§	External pull-ups/downs will be required on the board to enable the non-default state of the straps.			

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8 Ballout and Package Information

Figure 14. Intel 852GME GMCH Ballout Diagram (Top View)

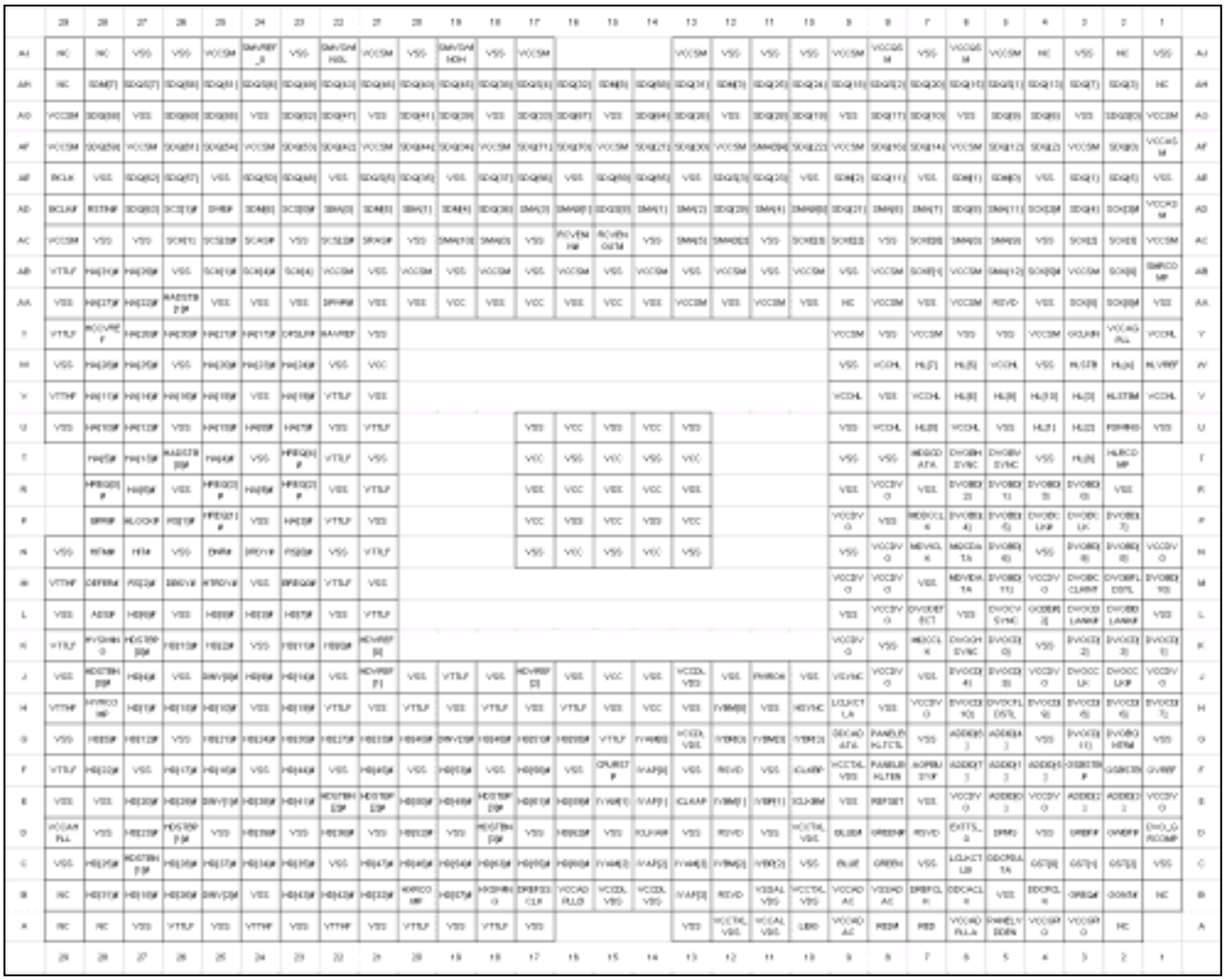


Table 54. Intel 852GME GMCH Ballout Table

Row	Column	Signal Name
L	7	DVODETECT
E	5	ADDID[0]
F	5	ADDID[1]
E	3	ADDID[2]
E	2	ADDID[3]
G	5	ADDID[4]
F	4	ADDID[5]
G	6	ADDID[6]
F	6	ADDID[7]
L	28	ADS#
F	7	AGPBUSY#
AE	29	BCLK
AD	29	BCLK#
C	9	BLUE
D	9	BLUE#
N	25	BNR#
P	28	BPRI#
F	15	CPURST#
M	26	DBSY#
B	6	DDCACLK
G	9	DDCADATA
B	4	DDCPCLK
C	5	DDCPDATA
M	28	DEFER#
J	25	DINV[0]#
E	25	DINV[1]#
B	25	DINV[2]#
G	19	DINV[3]#
D	5	DPMS
Y	23	DPSLP#
AA	22	DPWR#
N	24	DRDY#
B	7	DREFCLK

Row	Column	Signal Name
B	17	DREFSSCLK
L	2	DVOBBLANK#
M	3	DVOBCCLKINT
G	2	DVOBCINTR#
P	3	DVOBCLK
P	4	DVOBCLK#
R	3	DVOBD[0]
R	5	DVOBD[1]
M	1	DVOBD[10]
M	5	DVOBD[11]
R	6	DVOBD[2]
R	4	DVOBD[3]
P	6	DVOBD[4]
P	5	DVOBD[5]
N	5	DVOBD[6]
P	2	DVOBD[7]
N	2	DVOBD[8]
N	3	DVOBD[9]
M	2	DVOBFLDSTL
T	6	DVOBHSYNC
T	5	DVOBVSYNC
L	3	DVOCBLANK#
J	3	DVOCCLK
J	2	DVOCCLK#
K	5	DVOCD[0]
K	1	DVOCD[1]
H	6	DVOCD[10]
G	3	DVOCD[11]
K	3	DVOCD[2]
K	2	DVOCD[3]
J	6	DVOCD[4]
J	5	DVOCD[5]
H	2	DVOCD[6]

Row	Column	Signal Name
H	1	DVOCD[7]
H	3	DVOCD[8]
H	4	DVOCD[9]
H	5	DVOCFLDSTL
K	6	DVOCHSYNC
L	5	DVOCVSYNC
D	1	DVO_GRCOMP
D	6	EXTTS_0
Y	3	GCLKIN
C	8	GREEN
D	8	GREEN#
F	1	GVREF
U	28	HA[10]#
V	28	HA[11]#
U	27	HA[12]#
T	27	HA[13]#
V	27	HA[14]#
U	25	HA[15]#
V	26	HA[16]#
Y	24	HA[17]#
V	25	HA[18]#
V	23	HA[19]#
W	25	HA[20]#
Y	25	HA[21]#
AA	27	HA[22]#
W	24	HA[23]#
W	23	HA[24]#
W	27	HA[25]#
Y	27	HA[26]#
AA	28	HA[27]#
W	28	HA[28]#
AB	27	HA[29]#
P	23	HA[3]#
Y	26	HA[30]#
AB	28	HA[31]#

Row	Column	Signal Name
T	25	HA[4]#
T	28	HA[5]#
R	27	HA[6]#
U	23	HA[7]#
U	24	HA[8]#
R	24	HA[9]#
T	26	HADSTB[0]#
AA	26	HADSTB[1]#
Y	22	HAVREF
Y	28	HCCVREF
K	22	HD[0]#
H	27	HD[1]#
H	25	HD[10]#
K	23	HD[11]#
G	27	HD[12]#
K	26	HD[13]#
J	23	HD[14]#
H	26	HD[15]#
F	25	HD[16]#
F	26	HD[17]#
B	27	HD[18]#
H	23	HD[19]#
K	25	HD[2]#
E	27	HD[20]#
G	25	HD[21]#
F	28	HD[22]#
D	27	HD[23]#
G	24	HD[24]#
C	28	HD[25]#
B	26	HD[26]#
G	22	HD[27]#
C	26	HD[28]#
E	26	HD[29]#
L	24	HD[3]#
G	23	HD[30]#

Row	Column	Signal Name
B	28	HD[31]#
B	21	HD[32]#
G	21	HD[33]#
C	24	HD[34]#
C	23	HD[35]#
D	22	HD[36]#
C	25	HD[37]#
E	24	HD[38]#
D	24	HD[39]#
J	27	HD[4]#
G	20	HD[40]#
E	23	HD[41]#
B	22	HD[42]#
B	23	HD[43]#
F	23	HD[44]#
F	21	HD[45]#
C	20	HD[46]#
C	21	HD[47]#
G	18	HD[48]#
E	19	HD[49]#
G	28	HD[5]#
E	20	HD[50]#
G	17	HD[51]#
D	20	HD[52]#
F	19	HD[53]#
C	19	HD[54]#
C	17	HD[55]#
F	17	HD[56]#
B	19	HD[57]#
G	16	HD[58]#
E	16	HD[59]#
L	27	HD[6]#
C	16	HD[60]#
E	17	HD[61]#
D	16	HD[62]#

Row	Column	Signal Name
C	18	HD[63]#
L	23	HD[7]#
L	25	HD[8]#
J	24	HD[9]#
J	28	HDSTBN[0]#
C	27	HDSTBN[1]#
E	22	HDSTBN[2]#
D	18	HDSTBN[3]#
K	27	HDSTBP[0]#
D	26	HDSTBP[1]#
E	21	HDSTBP[2]#
E	18	HDSTBP[3]#
K	21	HDVREF[0]
J	21	HDVREF[1]
J	17	HDVREF[2]
N	27	HIT#
N	28	HITM#
U	7	HL[0]
U	4	HL[1]
V	4	HL[10]
U	3	HL[2]
V	3	HL[3]
W	2	HL[4]
W	6	HL[5]
V	6	HL[6]
W	7	HL[7]
T	3	HL[8]
V	5	HL[9]
P	27	HLOCK#
W	3	HLSTB
V	2	HLSTB#
W	1	HLVREF
T	2	HLRCOMP
R	28	HREQ[0]#
M	23	BREQ0#

Row	Column	Signal Name
P	25	HREQ[1]#
R	23	HREQ[2]#
R	25	HREQ[3]#
T	23	HREQ[4]#
H	10	HSYNC
M	25	HTRDY#
B	20	HXRCOMP
B	18	HXSWING
H	28	HYRCOMP
K	28	HYSWING
D	14	ICLKAM
E	13	ICLKAP
E	10	ICLKBM
F	10	ICLKBP
G	14	IYAM[0]
E	15	IYAM[1]
C	15	IYAM[2]
C	13	IYAM[3]
F	14	IYAP[0]
E	14	IYAP[1]
C	14	IYAP[2]
B	13	IYAP[3]
H	12	IYBM[0]
E	12	IYBM[1]
C	12	IYBM[2]
G	11	IYBM[3]
G	12	IYBP[0]
E	11	IYBP[1]
C	11	IYBP[2]
G	10	IYBP[3]
H	9	LCLKCTLA
C	6	LCLKCTLB
A	10	LIBG
P	7	MDDCCLK
T	7	MDDCDATA

Row	Column	Signal Name
N	7	MDVICLK
M	6	MDVIDATA
K	7	MI2CCLK
N	6	MI2CDATA
AJ	29	NC
AH	29	NC
B	29	NC
A	29	NC
AJ	28	NC
A	28	NC
AA	9	NC
AJ	4	NC
AJ	2	NC
A	2	NC
AH	1	NC
B	1	NC
G	8	PANELBKLTCTL
F	8	PANELBKLTEN
A	5	PANELVDDEN
U	2	PSWING
J	11	PWROK
A	7	RED
A	8	RED#
E	8	REFSET
N	23	RS[0]#
P	26	RS[1]#
M	27	RS[2]#
AD	28	RSTIN#
F	12	RSVD
D	12	RSVD
B	12	RSVD
AA	5	RSVD
L	4	GCBE#[2]
C	4	GST[0]
F	3	GSBSTB#

Row	Column	Signal Name
D	3	GRBF#
C	3	GST[1]
B	3	GREQ#
F	2	GSBSTB
D	2	GWBF#
C	2	GST[2]
B	2	GGNT#
AD	22	SBA[0]
AD	20	SBA[1]
AC	24	SCAS#
AB	2	SCK[0]
AA	2	SCK[0]#
AC	26	SCK[1]
AB	25	SCK[1]#
AC	3	SCK[2]
AD	4	SCK[2]#
AC	2	SCK[3]
AD	2	SCK[3]#
AB	23	SCK[4]
AB	24	SCK[4]#
AA	3	SCK[5]
AB	4	SCK[5]#
AC	7	SCKE[0]
AB	7	SCKE[1]
AC	9	SCKE[2]
AC	10	SCKE[3]
AD	23	SCS[0]#
AD	26	SCS[1]#
AC	22	SCS[2]#
AC	25	SCS[3]#
AE	5	SDM[0]
AE	6	SDM[1]
AE	9	SDM[2]
AH	12	SDM[3]
AD	19	SDM[4]

Row	Column	Signal Name
AD	21	SDM[5]
AD	24	SDM[6]
AH	28	SDM[7]
AH	15	SDM[8]
AF	2	SDQ[0]
AE	3	SDQ[1]
AG	7	SDQ[10]
AE	8	SDQ[11]
AF	5	SDQ[12]
AH	4	SDQ[13]
AF	7	SDQ[14]
AH	6	SDQ[15]
AF	8	SDQ[16]
AG	8	SDQ[17]
AH	9	SDQ[18]
AG	10	SDQ[19]
AF	4	SDQ[2]
AH	7	SDQ[20]
AD	9	SDQ[21]
AF	10	SDQ[22]
AE	11	SDQ[23]
AH	10	SDQ[24]
AH	11	SDQ[25]
AG	13	SDQ[26]
AF	14	SDQ[27]
AG	11	SDQ[28]
AD	12	SDQ[29]
AH	2	SDQ[3]
AF	13	SDQ[30]
AH	13	SDQ[31]
AH	16	SDQ[32]
AG	17	SDQ[33]
AF	19	SDQ[34]
AE	20	SDQ[35]
AD	18	SDQ[36]

Row	Column	Signal Name
AE	18	SDQ[37]
AH	18	SDQ[38]
AG	19	SDQ[39]
AD	3	SDQ[4]
AH	20	SDQ[40]
AG	20	SDQ[41]
AF	22	SDQ[42]
AH	22	SDQ[43]
AF	20	SDQ[44]
AH	19	SDQ[45]
AH	21	SDQ[46]
AG	22	SDQ[47]
AE	23	SDQ[48]
AH	23	SDQ[49]
AE	2	SDQ[5]
AE	24	SDQ[50]
AH	25	SDQ[51]
AG	23	SDQ[52]
AF	23	SDQ[53]
AF	25	SDQ[54]
AG	25	SDQ[55]
AH	26	SDQ[56]
AE	26	SDQ[57]
AG	28	SDQ[58]
AF	28	SDQ[59]
AG	4	SDQ[6]
AG	26	SDQ[60]
AF	26	SDQ[61]
AE	27	SDQ[62]
AD	27	SDQ[63]
AG	14	SDQ[64]
AE	14	SDQ[65]
AE	17	SDQ[66]
AG	16	SDQ[67]
AH	14	SDQ[68]

Row	Column	Signal Name
AE	15	SDQ[69]
AH	3	SDQ[7]
AF	16	SDQ[70]
AF	17	SDQ[71]
AD	6	SDQ[8]
AG	5	SDQ[9]
AG	2	SDQS[0]
AA	17	VCC
T	17	VCC
P	17	VCC
U	16	VCC
R	16	VCC
N	16	VCC
AA	15	VCC
T	15	VCC
P	15	VCC
J	15	VCC
U	14	VCC
R	14	VCC
N	14	VCC
H	14	VCC
T	13	VCC
P	13	VCC
B	9	VCCADAC
A	9	VCCADAC
A	6	VCCADPLLA
B	16	VCCADPLLB
Y	2	VCCAGPLL
D	29	VCCAHPLL
A	11	VCCALVDS
AF	1	VCCASM
AD	1	VCCASM
B	15	VCCDLVDS
B	14	VCCDLVDS
J	13	VCCDLVDS

Row	Column	Signal Name
G	13	VCCDLVDS
P	9	VCCDVO
M	9	VCCDVO
K	9	VCCDVO
R	8	VCCDVO
N	8	VCCDVO
M	8	VCCDVO
L	8	VCCDVO
J	8	VCCDVO
H	7	VCCDVO
E	6	VCCDVO
M	4	VCCDVO
J	4	VCCDVO
E	4	VCCDVO
N	1	VCCDVO
J	1	VCCDVO
E	1	VCCDVO
A	4	VCCGPIO
A	3	VCCGPIO
V	9	VCCHL
W	8	VCCHL
U	8	VCCHL
V	7	VCCHL
U	6	VCCHL
W	5	VCCHL
Y	1	VCCHL
V	1	VCCHL
AJ	8	VCCQSM
AJ	6	VCCQSM
AG	29	VCCSM
AF	29	VCCSM
AC	29	VCCSM
AF	27	VCCSM
AJ	25	VCCSM
AF	24	VCCSM

Row	Column	Signal Name
AB	22	VCCSM
AJ	21	VCCSM
AF	21	VCCSM
AB	20	VCCSM
AF	18	VCCSM
AB	18	VCCSM
AJ	17	VCCSM
AB	16	VCCSM
AF	15	VCCSM
AB	14	VCCSM
AJ	13	VCCSM
AA	13	VCCSM
AF	12	VCCSM
AB	12	VCCSM
AA	11	VCCSM
AB	10	VCCSM
AJ	9	VCCSM
AF	9	VCCSM
Y	9	VCCSM
AB	8	VCCSM
AA	8	VCCSM
Y	7	VCCSM
AF	6	VCCSM
AB	6	VCCSM
AA	6	VCCSM
AJ	5	VCCSM
Y	4	VCCSM
AF	3	VCCSM
AB	3	VCCSM
AG	1	VCCSM
AC	1	VCCSM
A	12	VCCTXLVDS
D	10	VCCTXLVDS
B	10	VCCTXLVDS
F	9	VCCTXLVDS

Row	Column	Signal Name
AA	29	VSS
W	29	VSS
U	29	VSS
N	29	VSS
L	29	VSS
J	29	VSS
G	29	VSS
E	29	VSS
C	29	VSS
AE	28	VSS
AC	28	VSS
E	28	VSS
D	28	VSS
AJ	27	VSS
AG	27	VSS
AC	27	VSS
F	27	VSS
A	27	VSS
AJ	26	VSS
AB	26	VSS
W	26	VSS
U	26	VSS
R	26	VSS
N	26	VSS
L	26	VSS
J	26	VSS
G	26	VSS
AE	25	VSS
AA	25	VSS
D	25	VSS
A	25	VSS
AG	24	VSS
AA	24	VSS
V	24	VSS
T	24	VSS

Row	Column	Signal Name
P	24	VSS
M	24	VSS
K	24	VSS
H	24	VSS
F	24	VSS
B	24	VSS
AJ	23	VSS
AC	23	VSS
AA	23	VSS
D	23	VSS
A	23	VSS
AE	22	VSS
W	22	VSS
U	22	VSS
R	22	VSS
N	22	VSS
L	22	VSS
J	22	VSS
F	22	VSS
C	22	VSS
AG	21	VSS
AB	21	VSS
AA	21	VSS
Y	21	VSS
V	21	VSS
T	21	VSS
P	21	VSS
M	21	VSS
H	21	VSS
D	21	VSS
A	21	VSS
AJ	20	VSS
AC	20	VSS
AA	20	VSS
J	20	VSS

Row	Column	Signal Name
F	20	VSS
AE	19	VSS
AB	19	VSS
H	19	VSS
D	19	VSS
A	19	VSS
AJ	18	VSS
AG	18	VSS
AA	18	VSS
J	18	VSS
F	18	VSS
AC	17	VSS
AB	17	VSS
U	17	VSS
R	17	VSS
N	17	VSS
H	17	VSS
D	17	VSS
A	17	VSS
AE	16	VSS
AA	16	VSS
T	16	VSS
P	16	VSS
J	16	VSS
F	16	VSS
AG	15	VSS
AB	15	VSS
U	15	VSS
R	15	VSS
N	15	VSS
H	15	VSS
D	15	VSS
AC	14	VSS
AA	14	VSS
T	14	VSS

Row	Column	Signal Name
P	14	VSS
J	14	VSS
AE	13	VSS
AB	13	VSS
U	13	VSS
R	13	VSS
N	13	VSS
H	13	VSS
F	13	VSS
D	13	VSS
A	13	VSS
AJ	12	VSS
AG	12	VSS
AA	12	VSS
J	12	VSS
AJ	11	VSS
AC	11	VSS
AB	11	VSS
H	11	VSS
F	11	VSS
D	11	VSS
AJ	10	VSS
AE	10	VSS
AA	10	VSS
J	10	VSS
C	10	VSS
AG	9	VSS
AB	9	VSS
W	9	VSS
U	9	VSS
T	9	VSS
R	9	VSS
N	9	VSS
L	9	VSS
E	9	VSS

Row	Column	Signal Name
AC	8	VSS
Y	8	VSS
V	8	VSS
T	8	VSS
P	8	VSS
K	8	VSS
H	8	VSS
AJ	7	VSS
AE	7	VSS
AA	7	VSS
R	7	VSS
M	7	VSS
J	7	VSS
G	7	VSS
E	7	VSS
C	7	VSS
AG	6	VSS
Y	6	VSS
L	6	VSS
Y	5	VSS
U	5	VSS
B	5	VSS
AE	4	VSS
AC	4	VSS
AA	4	VSS
W	4	VSS
T	4	VSS
N	4	VSS
K	4	VSS
G	4	VSS
D	4	VSS
AJ	3	VSS
AG	3	VSS
R	2	VSS
AJ	1	VSS

Row	Column	Signal Name
AE	1	VSS
AA	1	VSS
U	1	VSS
L	1	VSS
G	1	VSS
C	1	VSS
B	8	VSSADAC
B	11	VSSALVDS
J	9	VSYNC
V	29	VTTHF
M	29	VTTHF
H	29	VTTHF
A	24	VTTHF
A	22	VTTHF
AB	29	VTTLF
Y	29	VTTLF
K	29	VTTLF
F	29	VTTLF
A	26	VTTLF
V	22	VTTLF
T	22	VTTLF
P	22	VTTLF
M	22	VTTLF
H	22	VTTLF
U	21	VTTLF
B	7	DREFCLK
B	17	DREFSSCLK
L	2	DVOBBLANK#
M	3	DVOBCCLKINT
G	2	DVOBCINTR#
P	3	DVOBCLK
P	4	DVOBCLK#
R	3	DVOBD[0]
R	5	DVOBD[1]
M	1	DVOBD[10]

Row	Column	Signal Name
M	5	DVOBD[11]
R	6	DVOBD[2]
R	4	DVOBD[3]
P	6	DVOBD[4]
P	5	DVOBD[5]
N	5	DVOBD[6]
P	2	DVOBD[7]
N	2	DVOBD[8]
N	3	DVOBD[9]
M	2	DVOBFLDSTL
T	6	DVOBHSYNC
T	5	DVOBVSYNC
L	3	DVOCBLANK#
J	3	DVOCCLK
J	2	DVOCCLK#
K	5	DVOCD[0]
K	1	DVOCD[1]
H	6	DVOCD[10]
G	3	DVOCD[11]
K	3	DVOCD[2]
K	2	DVOCD[3]
J	6	DVOCD[4]
AB	28	HA[31]#
T	25	HA[4]#
T	28	HA[5]#
R	27	HA[6]#
U	23	HA[7]#
U	24	HA[8]#
R	24	HA[9]#
T	26	HADSTB[0]#
AA	26	HADSTB[1]#
Y	22	HAVREF
Y	28	HCCVREF
K	22	HD[0]#
H	27	HD[1]#

Row	Column	Signal Name
H	25	HD[10]#
K	23	HD[11]#
G	27	HD[12]#
K	26	HD[13]#
J	23	HD[14]#
H	26	HD[15]#
F	25	HD[16]#
F	26	HD[17]#
B	27	HD[18]#
H	23	HD[19]#
K	25	HD[2]#
E	27	HD[20]#
G	25	HD[21]#
F	28	HD[22]#
D	27	HD[23]#
G	24	HD[24]#
C	28	HD[25]#
B	26	HD[26]#
G	22	HD[27]#
C	26	HD[28]#
E	26	HD[29]#
L	24	HD[3]#
G	23	HD[30]#
L	23	HD[7]#
L	25	HD[8]#
J	24	HD[9]#
J	28	HDSTBN[0]#
C	27	HDSTBN[1]#
E	22	HDSTBN[2]#
D	18	HDSTBN[3]#
K	27	HDSTBP[0]#
D	26	HDSTBP[1]#
E	21	HDSTBP[2]#
E	18	HDSTBP[3]#
K	21	HDVREF[0]

Row	Column	Signal Name
J	21	HDVREF[1]
J	17	HDVREF[2]
N	27	HIT#
N	28	HITM#
U	7	HL[0]
U	4	HL[1]
V	4	HL[10]
U	3	HL[2]
V	3	HL[3]
W	2	HL[4]
W	6	HL[5]
V	6	HL[6]
W	7	HL[7]
T	3	HL[8]
V	5	HL[9]
P	27	HLOCK#
W	3	HLSTB
V	2	HLSTB#
W	1	HLVREF
T	2	HLRCOMP
R	28	HREQ[0]#
M	23	BREQ0#
P	25	HREQ[1]#
R	23	HREQ[2]#
N	6	MI2CDATA
AJ	29	NC
AH	29	NC
B	29	NC
A	29	NC
AJ	28	NC
A	28	NC
AA	9	NC
AJ	4	NC
AJ	2	NC
A	2	NC

Row	Column	Signal Name
AH	1	NC
B	1	NC
G	8	PANELBKLTCTL
F	8	PANELBKLTEN
A	5	PANELVDDEN
U	2	PSWING
J	11	PWROK
A	7	RED
A	8	RED#
E	8	REFSET
N	23	RS[0]#
P	26	RS[1]#
M	27	RS[2]#
AD	28	RSTIN#
F	12	RSVD
D	12	RSVD
B	12	RSVD
AA	5	RSVD
L	4	GCBE#[2]
C	4	GST[0]
F	3	GSBSTB#
D	3	GRBF#
C	3	GST[1]
B	3	GREQ#
F	2	GSBSTB
AE	3	SDQ[1]
AG	7	SDQ[10]
AE	8	SDQ[11]
AF	5	SDQ[12]
AH	4	SDQ[13]
AF	7	SDQ[14]
AH	6	SDQ[15]
AF	8	SDQ[16]
AG	8	SDQ[17]
AH	9	SDQ[18]

Row	Column	Signal Name
AG	10	SDQ[19]
AF	4	SDQ[2]
AH	7	SDQ[20]
AD	9	SDQ[21]
AF	10	SDQ[22]
AE	11	SDQ[23]
AH	10	SDQ[24]
AH	11	SDQ[25]
AG	13	SDQ[26]
AF	14	SDQ[27]
AG	11	SDQ[28]
AD	12	SDQ[29]
AH	2	SDQ[3]
AF	13	SDQ[30]
AH	13	SDQ[31]
AH	16	SDQ[32]
AG	17	SDQ[33]
AF	19	SDQ[34]
AE	20	SDQ[35]
AD	18	SDQ[36]
AE	18	SDQ[37]
AH	18	SDQ[38]
AG	19	SDQ[39]
AD	3	SDQ[4]
AH	20	SDQ[40]
AG	20	SDQ[41]
AH	5	SDQS[1]
AH	8	SDQS[2]
AE	12	SDQS[3]
AH	17	SDQS[4]
AE	21	SDQS[5]
AH	24	SDQS[6]
AH	27	SDQS[7]
AD	15	SDQS[8]
AC	18	SMA[0]

Row	Column	Signal Name
AD	14	SMA[1]
AC	19	SMA[10]
AD	5	SMA[11]
AB	5	SMA[12]
AD	13	SMA[2]
AD	17	SMA[3]
AD	11	SMA[4]
AC	13	SMA[5]
AD	8	SMA[6]
AD	7	SMA[7]
AC	6	SMA[8]
AC	5	SMA[9]
AD	16	SMAB[1]
AC	12	SMAB[2]
AF	11	SMAB[4]
AD	10	SMAB[5]
AB	1	SMRCOMP
AJ	24	SMVREF_0
AJ	19	SMVSWINGH
AJ	22	SMVSWINGL
AC	21	SRAS#
AC	16	RCVENIN#
AC	15	RCVENOUT#
D	7	RSVD
AD	25	SWE#
W	21	VCC
AA	19	VCC
J	8	VCCDVO
H	7	VCCDVO
E	6	VCCDVO
M	4	VCCDVO
J	4	VCCDVO
E	4	VCCDVO
N	1	VCCDVO
J	1	VCCDVO

Row	Column	Signal Name
E	1	VCCDVO
A	4	VCCGPIO
A	3	VCCGPIO
V	9	VCCHL
W	8	VCCHL
U	8	VCCHL
V	7	VCCHL
U	6	VCCHL
W	5	VCCHL
Y	1	VCCHL
V	1	VCCHL
AJ	8	VCCQSM
AJ	6	VCCQSM
AG	29	VCCSM
AF	29	VCCSM
AC	29	VCCSM
AF	27	VCCSM
AJ	25	VCCSM
AF	24	VCCSM
AB	22	VCCSM
AJ	21	VCCSM
AF	21	VCCSM
AB	20	VCCSM
AF	18	VCCSM
AB	18	VCCSM
AJ	17	VCCSM
AB	16	VCCSM
AF	15	VCCSM
AC	28	VSS
E	28	VSS
D	28	VSS
AJ	27	VSS
AG	27	VSS
AC	27	VSS
F	27	VSS

Row	Column	Signal Name
A	27	VSS
AJ	26	VSS
AB	26	VSS
W	26	VSS
U	26	VSS
R	26	VSS
N	26	VSS
L	26	VSS
J	26	VSS
G	26	VSS
AE	25	VSS
AA	25	VSS
D	25	VSS
A	25	VSS
AG	24	VSS
AA	24	VSS
V	24	VSS
T	24	VSS
P	24	VSS
M	24	VSS
K	24	VSS
H	24	VSS
F	24	VSS
B	24	VSS
AJ	23	VSS
AC	23	VSS
AA	23	VSS
D	23	VSS
A	23	VSS
AB	17	VSS
U	17	VSS
R	17	VSS
N	17	VSS
H	17	VSS
D	17	VSS

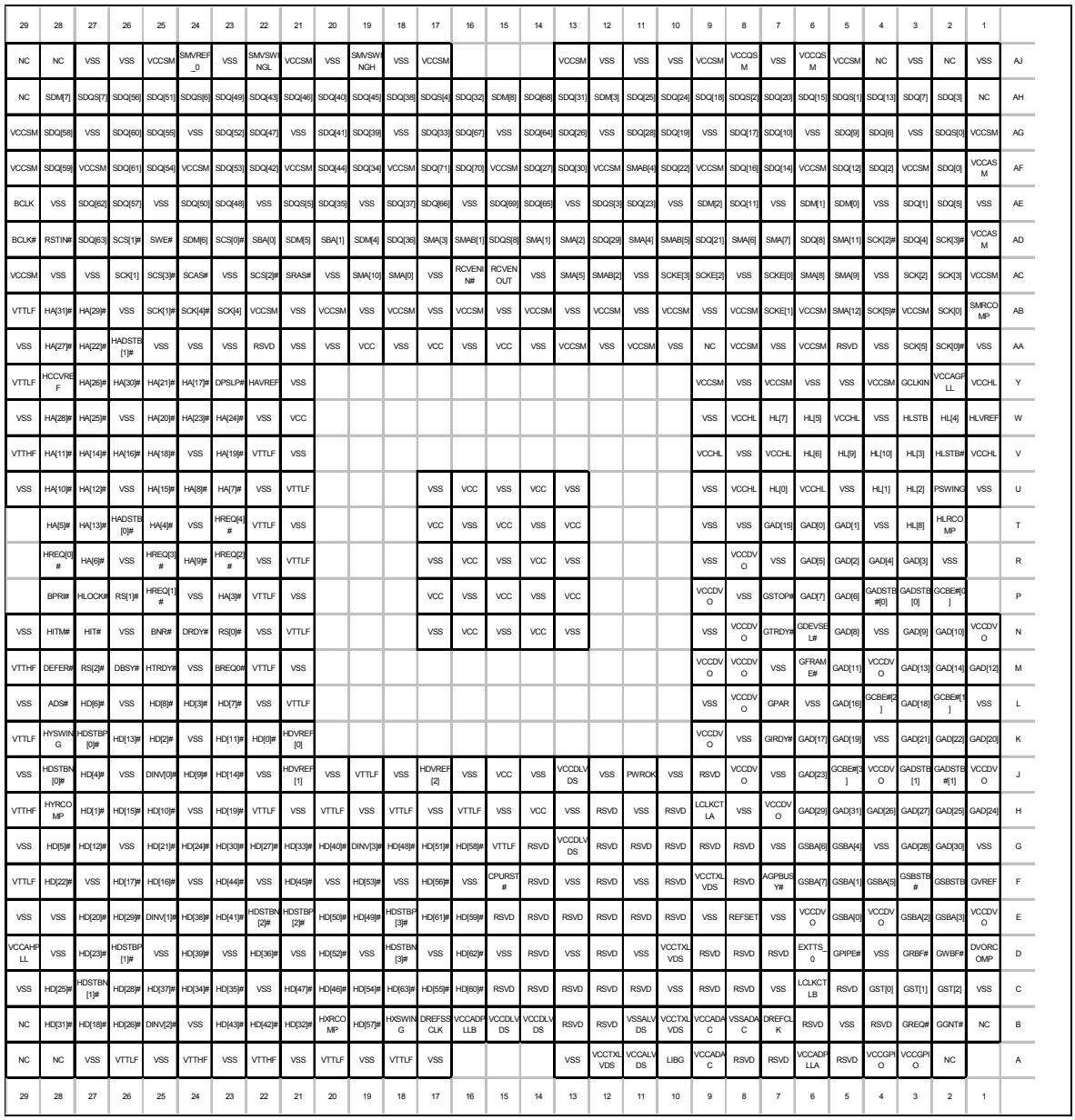
Row	Column	Signal Name
A	17	VSS
AE	16	VSS
AA	16	VSS
T	16	VSS
P	16	VSS
J	16	VSS
F	16	VSS
AG	15	VSS
AB	15	VSS
U	15	VSS
R	15	VSS
N	15	VSS
H	15	VSS
D	15	VSS
AC	14	VSS
AA	14	VSS
T	14	VSS
P	14	VSS
J	14	VSS
AE	13	VSS
AB	13	VSS
U	13	VSS
R	13	VSS
N	13	VSS
H	13	VSS
F	13	VSS
D	13	VSS
A	13	VSS
AJ	12	VSS
AG	12	VSS
E	7	VSS
C	7	VSS
AG	6	VSS
Y	6	VSS
L	6	VSS

Row	Column	Signal Name
Y	5	VSS
U	5	VSS
B	5	VSS
AE	4	VSS
AC	4	VSS
AA	4	VSS
W	4	VSS
T	4	VSS
N	4	VSS
K	4	VSS
G	4	VSS
D	4	VSS
AJ	3	VSS
AG	3	VSS
R	2	VSS
AJ	1	VSS
AE	1	VSS
AA	1	VSS
U	1	VSS
L	1	VSS
G	1	VSS
C	1	VSS
B	8	VSSADAC
B	11	VSSALVDS
J	9	VSYNC
V	29	VTTHF
M	29	VTTHF
H	29	VTTHF
A	24	VTTHF
A	22	VTTHF
AB	29	VTTLF
R	21	VTTLF
N	21	VTTLF
L	21	VTTLF
H	20	VTTLF

Row	Column	Signal Name
A	20	VTTLF
J	19	VTTLF
H	18	VTTLF

Row	Column	Signal Name
A	18	VTTLF
H	16	VTTLF
G	15	VTTLF

Figure 15. Intel 852PM MCH Ballout Diagram (Top View)



29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
NC	NC	VSS	VSS	VCCSM	SMVREF_0	VSS	SMVSWINGL	VCCSM	VSS	SMVSWINGH	VSS	VCCSM				VCCSM	VSS	VSS	VSS	VCCSM	VCCQSM	VSS	VCCQSM	VCCSM	NC	VSS	NC	VSS	AJ
NC	SDM[7]	SDQS[7]	SDQ[56]	SDQ[51]	SDQS[6]	SDQ[49]	SDQ[43]	SDQ[46]	SDQ[40]	SDQ[45]	SDQ[38]	SDQS[4]	SDQ[32]	SDM[8]	SDQ[68]	SDQ[31]	SDM[3]	SDQ[25]	SDQ[24]	SDQ[18]	SDQS[2]	SDQ[20]	SDQ[15]	SDQS[1]	SDQ[13]	SDQ[7]	SDQ[3]	NC	AH
VCCSM	SDQ[58]	VSS	SDQ[60]	SDQ[55]	VSS	SDQ[52]	SDQ[47]	VSS	SDQ[41]	SDQ[39]	VSS	SDQ[33]	SDQ[67]	VSS	SDQ[64]	SDQ[26]	VSS	SDQ[28]	SDQ[19]	VSS	SDQ[17]	SDQ[10]	VSS	SDQ[9]	SDQ[6]	VSS	SDQS[0]	VCCSM	AG
VCCSM	SDQ[59]	VCCSM	SDQ[61]	SDQ[54]	VCCSM	SDQ[53]	SDQ[42]	VCCSM	SDQ[44]	SDQ[34]	VCCSM	SDQ[71]	SDQ[70]	VCCSM	SDQ[27]	SDQ[30]	VCCSM	SMAB[4]	SDQ[22]	VCCSM	SDQ[16]	SDQ[14]	VCCSM	SDQ[12]	SDQ[2]	VCCSM	SDQ[0]	VCCASM	AF
BCLK	VSS	SDQ[62]	SDQ[57]	VSS	SDQ[50]	SDQ[48]	VSS	SDQS[5]	SDQ[35]	VSS	SDQ[37]	SDQ[66]	VSS	SDQ[69]	SDQ[65]	VSS	SDQS[3]	SDQ[23]	VSS	SDM[2]	SDQ[11]	VSS	SDM[1]	SDM[0]	VSS	SDQ[1]	SDQ[5]	VSS	AE
BCLK#	RSTIN#	SDQ[63]	SCS[1]#	SWE#	SDM[6]	SCS[0]#	SBA[0]	SDM[5]	SBA[1]	SDM[4]	SDQ[36]	SMA[3]	SMAB[1]	SDQS[8]	SMA[1]	SMA[2]	SDQ[29]	SMA[4]	SMAB[5]	SDQ[21]	SMA[6]	SMA[7]	SDQ[8]	SMA[11]	SCK[2]#	SDQ[4]	SCK[3]#	VCCASM	AD
VCCSM	VSS	VSS	SCK[1]	SCS[3]#	SCAS#	VSS	SCS[2]#	SRAS#	VSS	SMA[10]	SMA[0]	VSS	RCVENIN#	RCVENOUT	VSS	SMA[5]	SMAB[2]	VSS	SCKE[3]	SCKE[2]	VSS	SCKE[0]	SMA[8]	SMA[9]	VSS	SCK[2]	SCK[3]	VCCSM	AC
VTTLF	HA[31]#	HA[29]#	VSS	SCK[1]#	SCK[4]#	SCK[4]	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	SCKE[1]	VCCSM	SMA[12]	SCK[5]#	VCCSM	SCK[0]	SMRCOMP	AB
VSS	HA[27]#	HA[22]#	HADSTB[1]#	VSS	VSS	VSS	RSVD	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCCSM	VSS	VCCSM	VSS	NC	VCCSM	VSS	VCCSM	RSVD	VSS	SCK[5]	SCK[0]#	VSS	AA
VTTLF	HCCVREF	HA[26]#	HA[30]#	HA[21]#	HA[17]#	DPSLP#	HAVREF	VSS												VCCSM	VSS	VCCSM	VSS	VSS	VCCSM	GCLKIN	VCCAGPLL	VCCHL	Y
VSS	HA[28]#	HA[25]#	VSS	HA[20]#	HA[23]#	HA[24]#	VSS	VCC												VSS	VCCHL	HL[7]	HL[5]	VCCHL	VSS	HLSTB	HL[4]	HLVREF	W
VTTHF	HA[11]#	HA[14]#	HA[16]#	HA[18]#	VSS	HA[19]#	VTTLF	VSS												VCCHL	VSS	VCCHL	HL[6]	HL[9]	HL[10]	HL[3]	HLSTB#	VCCHL	V
VSS	HA[10]#	HA[12]#	VSS	HA[15]#	HA[8]#	HA[7]#	VSS	VTTLF				VSS	VCC	VSS	VCC	VSS				VSS	VCCHL	HL[0]	VCCHL	VSS	HL[1]	HL[2]	PSWING	VSS	U
	HA[5]#	HA[13]#	HADSTB[0]#	HA[4]#	VSS	HREQ[4]#	VTTLF	VSS				VCC	VSS	VCC	VSS	VCC				VSS	VSS	GAD[15]	GAD[0]	GAD[1]	VSS	HL[8]	HLRCOMP		T
	HREQ[0]#	HA[6]#	VSS	HREQ[3]#	HA[9]#	HREQ[2]#	VSS	VTTLF				VSS	VCC	VSS	VCC	VSS				VSS	VCCDVO	VSS	GAD[5]	GAD[2]	GAD[4]	GAD[3]	VSS		R
	BPRI#	HLOCK#	RS[1]#	HREQ[1]#	VSS	HA[3]#	VTTLF	VSS				VCC	VSS	VCC	VSS	VCC				VCCDVO	VSS	GSTOP#	GAD[7]	GAD[6]	GADSTB#[0]	GADSTB[0]	GCBE#[0]		P
VSS	HITM#	HIT#	VSS	BNR#	DRDY#	RS[0]#	VSS	VTTLF				VSS	VCC	VSS	VCC	VSS				VSS	VCCDVO	GTRDY#	GDEVSEL#	GAD[8]	VSS	GAD[9]	GAD[10]	VCCDVO	N
VTTHF	DEFER#	RS[2]#	DBSY#	HTRDY#	VSS	BREQ0#	VTTLF	VSS												VCCDVO	VCCDVO	VSS	GFRAME#	GAD[11]	VCCDVO	GAD[13]	GAD[14]	GAD[12]	M
VSS	ADS#	HD[6]#	VSS	HD[8]#	HD[3]#	HD[7]#	VSS	VTTLF												VSS	VCCDVO	GPAR	VSS	GAD[16]	GCBE#[2]	GAD[18]	GCBE#[1]	VSS	L
VTTLF	HYSWING	HDSTBP[0]#	HD[13]#	HD[2]#	VSS	HD[11]#	HD[0]#	HDVREF[0]												VCCDVO	VSS	GIRDY#	GAD[17]	GAD[19]	VSS	GAD[21]	GAD[22]	GAD[20]	K
VSS	HDSTBN[0]#	HD[4]#	VSS	DINV[0]#	HD[9]#	HD[14]#	VSS	HDVREF[1]	VSS	VTTLF	VSS	HDVREF[2]	VSS	VCC	VSS	VCCDLVDS	VSS	PWROK	VSS	RSVD	VCCDVO	VSS	GAD[23]	GCBE#[3]	VCCDVO	GADSTB[1]	GADSTB#[1]	VCCDVO	J
VTTHF	HYRCOMP	HD[1]#	HD[15]#	HD[10]#	VSS	HD[19]#	VTTLF	VSS	VTTLF	VSS	VTTLF	VSS	VTTLF	VSS	VCC	VSS	RSVD	VSS	RSVD	LCLKCTLA	VSS	VCCDVO	GAD[29]	GAD[31]	GAD[26]	GAD[27]	GAD[25]	GAD[24]	H
VSS	HD[5]#	HD[12]#	VSS	HD[21]#	HD[24]#	HD[30]#	HD[27]#	HD[33]#	HD[40]#	DINV[3]#	HD[48]#	HD[51]#	HD[58]#	VTTLF	RSVD	VCCDLVDS	RSVD	RSVD	RSVD	RSVD	RSVD	VSS	GSBA[6]	GSBA[4]	VSS	GAD[28]	GAD[30]	VSS	G
VTTLF	HD[22]#	VSS	HD[17]#	HD[16]#	VSS	HD[44]#	VSS	HD[45]#	VSS	HD[53]#	VSS	HD[56]#	VSS	CPURST#	RSVD	VSS	RSVD	VSS	RSVD	VCCTXLVDS	RSVD	AGPBUSY#	GSBA[7]	GSBA[1]	GSBA[5]	GSBSTB#	GSBSTB	GVREF	F
VSS	VSS	HD[20]#	HD[29]#	DINV[1]#	HD[38]#	HD[41]#	HDSTBN[2]#	HDSTBP[2]#	HD[50]#	HD[49]#	HDSTBP[3]#	HD[61]#	HD[59]#	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VSS	REFSET	VSS	VCCDVO	GSBA[0]	VCCDVO	GSBA[2]	GSBA[3]	VCCDVO	E
VCCAHPLL	VSS	HD[23]#	HDSTBP[1]#	VSS	HD[39]#	VSS	HD[36]#	VSS	HD[52]#	VSS	HDSTBN[3]#	VSS	HD[62]#	VSS	RSVD	VSS	RSVD	VSS	VCCTXLVDS	RSVD	RSVD	RSVD	EXTTS_0	GPIPE#	VSS	GRBF#	GWBF#	DVORCOMP	D
VSS	HD[25]#	HDSTBN[1]#	HD[28]#	HD[37]#	HD[34]#	HD[35]#	VSS	HD[47]#	HD[46]#	HD[54]#	HD[63]#	HD[55]#	HD[60]#	RSVD	RSVD	RSVD	RSVD	RSVD	VSS	RSVD	RSVD	VSS	LCLKCTLB	RSVD	GST[0]	GST[1]	GST[2]	VSS	C
NC	HD[31]#	HD[18]#	HD[26]#	DINV[2]#	VSS	HD[43]#	HD[42]#	HD[32]#	HXRCOMP	HD[57]#	HXSWING	DREFSSCLK	VCCADPLLB	VCCDLVDS	VCCDLVDS	RSVD	RSVD	VSSALVDS	VCCTXLVDS	VCCADAC	VSSADAC	DREFCLK	RSVD	VSS	RSVD	GREQ#	GGNT#	NC	B
NC	NC	VSS	VTTLF	VSS	VTTHF	VSS	VTTHF	VSS	VTTLF	VSS	VTTLF	VSS				VSS	VCCTXLVDS	VCCALVDS	LIBG	VCCADAC	RSVD	RSVD	VCCADPLLA	RSVD	VCCGPIO	VCCGPIO	NC		A
29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 55. Intel 852PM MCH Ballout Table

Row	Column	Signal Name
E	5	ADDID[0]
F	5	ADDID[1]
E	3	ADDID[2]
E	2	ADDID[3]
G	5	ADDID[4]
F	4	ADDID[5]
G	6	ADDID[6]
F	6	ADDID[7]
L	28	ADS#
F	7	AGPBUSY#
AE	29	BCLK
AD	29	BCLK#
C	9	BLUE
D	9	BLUE#
N	25	BNR#
P	28	BPRI#
M	23	BREQ0#
F	15	CPURST#
M	26	DBSY#
B	6	DDCACLK
G	9	DDCADATA
B	4	DDCPCLK
C	5	DDCPDATA
M	28	DEFER#
J	25	DINV[0]#
E	25	DINV[1]#
B	25	DINV[2]#
G	19	DINV[3]#
D	5	DPMS
Y	23	DPSLP#
N	24	DRDY#
B	7	DREFCLK
B	17	DREFSSCLK

Row	Column	Signal Name
L	2	DVOBBLANK#
M	3	DVOBCCLKINT
G	2	DVOBCINTR#
P	3	RSVD
P	4	RSVD
R	3	RSVD
R	5	RSVD
M	1	RSVD
M	5	RSVD
R	6	RSVD
R	4	RSVD
P	6	RSVD
P	5	RSVD
N	5	RSVD
P	2	RSVD
N	2	RSVD
N	3	RSVD
M	2	RSVD
T	6	RSVD
T	5	RSVD
L	7	DVODETECT
D	1	DVORCOMP
D	6	EXTTS_0
Y	3	GCLKIN
C	8	GREEN
D	8	GREEN#
F	1	GVREF
U	28	HA[10]#
V	28	HA[11]#
U	27	HA[12]#
T	27	HA[13]#
V	27	HA[14]#
U	25	HA[15]#

Row	Column	Signal Name
V	26	HA[16]#
Y	24	HA[17]#
V	25	HA[18]#
V	23	HA[19]#
W	25	HA[20]#
Y	25	HA[21]#
AA	27	HA[22]#
W	24	HA[23]#
W	23	HA[24]#
W	27	HA[25]#
Y	27	HA[26]#
AA	28	HA[27]#
W	28	HA[28]#
AB	27	HA[29]#
P	23	HA[3]#
Y	26	HA[30]#
AB	28	HA[31]#
T	25	HA[4]#
T	28	HA[5]#
R	27	HA[6]#
U	23	HA[7]#
U	24	HA[8]#
R	24	HA[9]#
T	26	HADSTB[0]#
AA	26	HADSTB[1]#
Y	22	HAVREF
Y	28	HCCVREF
K	22	HD[0]#
H	27	HD[1]#
H	25	HD[10]#
K	23	HD[11]#
G	27	HD[12]#
K	26	HD[13]#
J	23	HD[14]#
H	26	HD[15]#

Row	Column	Signal Name
F	25	HD[16]#
F	26	HD[17]#
B	27	HD[18]#
H	23	HD[19]#
K	25	HD[2]#
E	27	HD[20]#
G	25	HD[21]#
F	28	HD[22]#
D	27	HD[23]#
G	24	HD[24]#
C	28	HD[25]#
B	26	HD[26]#
G	22	HD[27]#
C	26	HD[28]#
E	26	HD[29]#
L	24	HD[3]#
G	23	HD[30]#
B	28	HD[31]#
B	21	HD[32]#
G	21	HD[33]#
C	24	HD[34]#
C	23	HD[35]#
D	22	HD[36]#
C	25	HD[37]#
E	24	HD[38]#
D	24	HD[39]#
J	27	HD[4]#
G	20	HD[40]#
E	23	HD[41]#
B	22	HD[42]#
B	23	HD[43]#
F	23	HD[44]#
F	21	HD[45]#
C	20	HD[46]#
C	21	HD[47]#

Row	Column	Signal Name
G	18	HD[48]#
E	19	HD[49]#
G	28	HD[5]#
E	20	HD[50]#
G	17	HD[51]#
D	20	HD[52]#
F	19	HD[53]#
C	19	HD[54]#
C	17	HD[55]#
F	17	HD[56]#
B	19	HD[57]#
G	16	HD[58]#
E	16	HD[59]#
L	27	HD[6]#
C	16	HD[60]#
E	17	HD[61]#
D	16	HD[62]#
C	18	HD[63]#
L	23	HD[7]#
L	25	HD[8]#
J	24	HD[9]#
J	28	HDSTBN[0]#
C	27	HDSTBN[1]#
E	22	HDSTBN[2]#
D	18	HDSTBN[3]#
K	27	HDSTBP[0]#
D	26	HDSTBP[1]#
E	21	HDSTBP[2]#
E	18	HDSTBP[3]#
K	21	HDVREF[0]
J	21	HDVREF[1]
J	17	HDVREF[2]
N	27	HIT#
N	28	HITM#
U	7	HL[0]

Row	Column	Signal Name
U	4	HL[1]
V	4	HL[10]
U	3	HL[2]
V	3	HL[3]
W	2	HL[4]
W	6	HL[5]
V	6	HL[6]
W	7	HL[7]
T	3	HL[8]
V	5	HL[9]
P	27	HLOCK#
T	2	HLRCOMP
W	3	HLSTB
V	2	HLSTB#
W	1	HLVREF
R	28	HREQ[0]#
P	25	HREQ[1]#
R	23	HREQ[2]#
R	25	HREQ[3]#
T	23	HREQ[4]#
H	10	HSYNC
M	25	HTRDY#
B	20	HXRCOMP
B	18	HXSWING
H	28	HYRCOMP
K	28	HYSWING
D	14	ICLKAM
E	13	ICLKAP
E	10	ICLKBM
F	10	ICLKBP
G	14	IYAM[0]
E	15	IYAM[1]
C	15	IYAM[2]
C	13	IYAM[3]
F	14	IYAP[0]

Row	Column	Signal Name
E	14	IYAP[1]
C	14	IYAP[2]
B	13	IYAP[3]
H	12	IYBM[0]
E	12	IYBM[1]
C	12	IYBM[2]
G	11	IYBM[3]
G	12	IYBP[0]
E	11	IYBP[1]
C	11	IYBP[2]
G	10	IYBP[3]
H	9	LCLKCTLA
C	6	LCLKCTLB
A	10	LIBG
P	7	MDDCCLK
T	7	MDDCDATA
N	7	MDVICLK
M	6	MDVIDATA
K	7	MI2CCLK
N	6	MI2CDATA
AJ	29	NC
AH	29	NC
B	29	NC
A	29	NC
AJ	28	NC
A	28	NC
AA	9	NC
AJ	4	NC
AJ	2	NC
A	2	NC
AH	1	NC
B	1	NC
G	8	PANELBKLTCTL
F	8	PANELBKLTEN
A	5	PANELVDDEN

Row	Column	Signal Name
U	2	PSWING
J	11	PWROK
AC	16	RCVENIN#
AC	15	RCVENOUT
A	7	RED
A	8	RED#
E	8	REFSET
N	23	RS[0]#
P	26	RS[1]#
M	27	RS[2]#
AD	28	RSTIN#
AA	22	RSVD
L	3	DVOCBLANK#
J	3	DVOCCLK
J	2	DVOCCLK#
K	5	DVOCD[0]
K	1	DVOCD[1]
H	6	DVOCD[10]
G	3	DVOCD[11]
K	3	DVOCD[2]
K	2	DVOCD[3]
J	6	DVOCD[4]
J	5	DVOCD[5]
H	2	DVOCD[6]
H	1	DVOCD[7]
H	3	DVOCD[8]
H	4	DVOCD[9]
H	5	DVOCFLDSTL
K	6	DVOCHSYNC
L	5	DVOCVSYNC
F	12	RSVD
D	12	RSVD
B	12	RSVD
AA	5	RSVD
L	4	RSVD

Row	Column	Signal Name
C	4	GST[0]
F	3	RSVD
D	3	RSVD
C	3	GST[1]
B	3	RSVD
F	2	RSVD
D	2	RSVD
C	2	RSVD
B	2	RSVD
D	7	RSVD
AD	22	SBA[0]
AD	20	SBA[1]
AC	24	SCAS#
AB	2	SCK[0]
AA	2	SCK[0]#
AC	26	SCK[1]
AB	25	SCK[1]#
AC	3	SCK[2]
AD	4	SCK[2]#
AC	2	SCK[3]
AD	2	SCK[3]#
AB	23	SCK[4]
AB	24	SCK[4]#
AA	3	SCK[5]
AB	4	SCK[5]#
AC	7	SCKE[0]
AB	7	SCKE[1]
AC	9	SCKE[2]
AC	10	SCKE[3]
AD	23	SCS[0]#
AD	26	SCS[1]#
AC	22	SCS[2]#
AC	25	SCS[3]#
AE	5	SDM[0]
AE	6	SDM[1]

Row	Column	Signal Name
AE	9	SDM[2]
AH	12	SDM[3]
AD	19	SDM[4]
AD	21	SDM[5]
AD	24	SDM[6]
AH	28	SDM[7]
AH	15	SDM[8]
AF	2	SDQ[0]
AE	3	SDQ[1]
AG	7	SDQ[10]
AE	8	SDQ[11]
AF	5	SDQ[12]
AH	4	SDQ[13]
AF	7	SDQ[14]
AH	6	SDQ[15]
AF	8	SDQ[16]
AG	8	SDQ[17]
AH	9	SDQ[18]
AG	10	SDQ[19]
AF	4	SDQ[2]
AH	7	SDQ[20]
AD	9	SDQ[21]
AF	10	SDQ[22]
AE	11	SDQ[23]
AH	10	SDQ[24]
AH	11	SDQ[25]
AG	13	SDQ[26]
AF	14	SDQ[27]
AG	11	SDQ[28]
AD	12	SDQ[29]
AH	2	SDQ[3]
AF	13	SDQ[30]
AH	13	SDQ[31]
AH	16	SDQ[32]
AG	17	SDQ[33]

Row	Column	Signal Name
AF	19	SDQ[34]
AE	20	SDQ[35]
AD	18	SDQ[36]
AE	18	SDQ[37]
AH	18	SDQ[38]
AG	19	SDQ[39]
AD	3	SDQ[4]
AH	20	SDQ[40]
AG	20	SDQ[41]
AF	22	SDQ[42]
AH	22	SDQ[43]
AF	20	SDQ[44]
AH	19	SDQ[45]
AH	21	SDQ[46]
AG	22	SDQ[47]
AE	23	SDQ[48]
AH	23	SDQ[49]
AE	2	SDQ[5]
AE	24	SDQ[50]
AH	25	SDQ[51]
AG	23	SDQ[52]
AF	23	SDQ[53]
AF	25	SDQ[54]
AG	25	SDQ[55]
AH	26	SDQ[56]
AE	26	SDQ[57]
AG	28	SDQ[58]
AF	28	SDQ[59]
AG	4	SDQ[6]
AG	26	SDQ[60]
AF	26	SDQ[61]
AE	27	SDQ[62]
AD	27	SDQ[63]
AG	14	SDQ[64]
AE	14	SDQ[65]

Row	Column	Signal Name
AE	17	SDQ[66]
AG	16	SDQ[67]
AH	14	SDQ[68]
AE	15	SDQ[69]
AH	3	SDQ[7]
AF	16	SDQ[70]
AF	17	SDQ[71]
AD	6	SDQ[8]
AG	5	SDQ[9]
AG	2	SDQS[0]
AH	5	SDQS[1]
AH	8	SDQS[2]
AE	12	SDQS[3]
AH	17	SDQS[4]
AE	21	SDQS[5]
AH	24	SDQS[6]
AH	27	SDQS[7]
AD	15	SDQS[8]
AC	18	SMA[0]
AD	14	SMA[1]
AC	19	SMA[10]
AD	5	SMA[11]
AB	5	SMA[12]
AD	13	SMA[2]
AD	17	SMA[3]
AD	11	SMA[4]
AC	13	SMA[5]
AD	8	SMA[6]
AD	7	SMA[7]
AC	6	SMA[8]
AC	5	SMA[9]
AD	16	SMAB[1]
AC	12	SMAB[2]
AF	11	SMAB[4]
AD	10	SMAB[5]

Row	Column	Signal Name
AB	1	SMRCOMP
AJ	24	SMVREF_0
AJ	19	SMVSWINGH
AJ	22	SMVSWINGL
AC	21	SRAS#
AD	25	SWE#
W	21	VCC
AA	19	VCC
AA	17	VCC
T	17	VCC
P	17	VCC
U	16	VCC
R	16	VCC
N	16	VCC
AA	15	VCC
T	15	VCC
P	15	VCC
J	15	VCC
U	14	VCC
R	14	VCC
N	14	VCC
H	14	VCC
T	13	VCC
P	13	VCC
B	9	VCCADAC
A	9	VCCADAC
A	6	VCCADPLLA
B	16	VCCADPLLB
Y	2	VCCAGPLL
D	29	VCCAHPLL
A	11	VCCALVDS
AF	1	VCCASM
AD	1	VCCASM
B	15	VCCDLVDS
B	14	VCCDLVDS

Row	Column	Signal Name
J	13	VCCDLVDS
G	13	VCCDLVDS
P	9	VCCDVO
M	9	VCCDVO
K	9	VCCDVO
R	8	VCCDVO
N	8	VCCDVO
M	8	VCCDVO
L	8	VCCDVO
J	8	VCCDVO
H	7	VCCDVO
E	6	VCCDVO
M	4	VCCDVO
J	4	VCCDVO
E	4	VCCDVO
N	1	VCCDVO
J	1	VCCDVO
E	1	VCCDVO
A	4	VCCGPIO
A	3	VCCGPIO
V	9	VCCHL
W	8	VCCHL
U	8	VCCHL
V	7	VCCHL
U	6	VCCHL
W	5	VCCHL
Y	1	VCCHL
V	1	VCCHL
AJ	8	VCCQSM
AJ	6	VCCQSM
AG	29	VCCSM
AF	29	VCCSM
AC	29	VCCSM
AF	27	VCCSM
AJ	25	VCCSM

Row	Column	Signal Name
AF	24	VCCSM
AB	22	VCCSM
AJ	21	VCCSM
AF	21	VCCSM
AB	20	VCCSM
AF	18	VCCSM
AB	18	VCCSM
AJ	17	VCCSM
AB	16	VCCSM
AF	15	VCCSM
AB	14	VCCSM
AJ	13	VCCSM
AA	13	VCCSM
AF	12	VCCSM
AB	12	VCCSM
AA	11	VCCSM
AB	10	VCCSM
AJ	9	VCCSM
AF	9	VCCSM
Y	9	VCCSM
AB	8	VCCSM
AA	8	VCCSM
Y	7	VCCSM
AF	6	VCCSM
AB	6	VCCSM
AA	6	VCCSM
AJ	5	VCCSM
Y	4	VCCSM
AF	3	VCCSM
AB	3	VCCSM
AG	1	VCCSM
AC	1	VCCSM
A	12	VCCTXLVDS
D	10	VCCTXLVDS
B	10	VCCTXLVDS
F	9	VCCTXLVDS
AA	29	VSS
W	29	VSS
U	29	VSS
N	29	VSS
L	29	VSS
J	29	VSS
G	29	VSS
E	29	VSS
C	29	VSS
AE	28	VSS
AC	28	VSS
E	28	VSS
D	28	VSS
AJ	27	VSS
AG	27	VSS
AC	27	VSS
F	27	VSS
A	27	VSS
AJ	26	VSS
AB	26	VSS
W	26	VSS
U	26	VSS
R	26	VSS
N	26	VSS
L	26	VSS
J	26	VSS
G	26	VSS
AE	25	VSS
AA	25	VSS
D	25	VSS
A	25	VSS
AG	24	VSS
AA	24	VSS
V	24	VSS

Row	Column	Signal Name
T	24	VSS
P	24	VSS
M	24	VSS
K	24	VSS
H	24	VSS
F	24	VSS
B	24	VSS
AJ	23	VSS
AC	23	VSS
AA	23	VSS
D	23	VSS
A	23	VSS
AE	22	VSS
W	22	VSS
U	22	VSS
R	22	VSS
N	22	VSS
L	22	VSS
J	22	VSS
F	22	VSS
C	22	VSS
AG	21	VSS
AB	21	VSS
AA	21	VSS
Y	21	VSS
V	21	VSS
T	21	VSS
P	21	VSS
M	21	VSS
H	21	VSS
D	21	VSS
A	21	VSS
AJ	20	VSS
AC	20	VSS
AA	20	VSS

Row	Column	Signal Name
J	20	VSS
F	20	VSS
AE	19	VSS
AB	19	VSS
H	19	VSS
D	19	VSS
A	19	VSS
AJ	18	VSS
AG	18	VSS
AA	18	VSS
J	18	VSS
F	18	VSS
AC	17	VSS
AB	17	VSS
U	17	VSS
R	17	VSS
N	17	VSS
H	17	VSS
D	17	VSS
A	17	VSS
AE	16	VSS
AA	16	VSS
T	16	VSS
P	16	VSS
J	16	VSS
F	16	VSS
AG	15	VSS
AB	15	VSS
U	15	VSS
R	15	VSS
N	15	VSS
H	15	VSS
D	15	VSS
AC	14	VSS
AA	14	VSS

Row	Column	Signal Name
T	14	VSS
P	14	VSS
J	14	VSS
AE	13	VSS
AB	13	VSS
U	13	VSS
R	13	VSS
N	13	VSS
H	13	VSS
F	13	VSS
D	13	VSS
A	13	VSS
AJ	12	VSS
AG	12	VSS
AA	12	VSS
J	12	VSS
AJ	11	VSS
AC	11	VSS
AB	11	VSS
H	11	VSS
F	11	VSS
D	11	VSS
AJ	10	VSS
AE	10	VSS
AA	10	VSS
J	10	VSS
C	10	VSS
AG	9	VSS
AB	9	VSS
W	9	VSS
U	9	VSS
T	9	VSS
R	9	VSS
N	9	VSS
L	9	VSS

Row	Column	Signal Name
E	9	VSS
AC	8	VSS
Y	8	VSS
V	8	VSS
T	8	VSS
P	8	VSS
K	8	VSS
H	8	VSS
AJ	7	VSS
AE	7	VSS
AA	7	VSS
R	7	VSS
M	7	VSS
J	7	VSS
G	7	VSS
E	7	VSS
C	7	VSS
AG	6	VSS
Y	6	VSS
L	6	VSS
Y	5	VSS
U	5	VSS
B	5	VSS
AE	4	VSS
AC	4	VSS
AA	4	VSS
W	4	VSS
T	4	VSS
N	4	VSS
K	4	VSS
G	4	VSS
D	4	VSS
AJ	3	VSS
AG	3	VSS
R	2	VSS

Row	Column	Signal Name
AJ	1	VSS
AE	1	VSS
AA	1	VSS
U	1	VSS
L	1	VSS
G	1	VSS
C	1	VSS
B	8	VSSADAC
B	11	VSSALVDS
J	9	VSYNC
V	29	VTTHF
M	29	VTTHF
H	29	VTTHF
A	24	VTTHF
A	22	VTTHF
AB	29	VTTLF
Y	29	VTTLF
K	29	VTTLF
F	29	VTTLF
A	26	VTTLF
V	22	VTTLF
T	22	VTTLF
P	22	VTTLF
M	22	VTTLF
H	22	VTTLF
P	3	RSVD
P	4	RSVD
R	3	RSVD
R	5	RSVD
M	1	RSVD
M	5	RSVD
R	6	RSVD
R	4	RSVD
P	6	RSVD
P	5	RSVD

Row	Column	Signal Name
N	5	RSVD
P	2	RSVD
N	2	RSVD
N	3	RSVD
M	2	RSVD
T	6	RSVD
T	5	RSVD
L	7	DVODETECT
D	1	DVORCOMP
D	6	EXTTS_0
Y	3	GCLKIN
C	8	GREEN
D	8	GREEN#
F	1	GVREF
U	28	HA[10]#
V	28	HA[11]#
U	27	HA[12]#
T	27	HA[13]#
V	27	HA[14]#
U	25	HA[15]#
V	26	HA[16]#
Y	24	HA[17]#
V	25	HA[18]#
V	23	HA[19]#
W	25	HA[20]#
E	27	HD[20]#
G	25	HD[21]#
F	28	HD[22]#
D	27	HD[23]#
G	24	HD[24]#
C	28	HD[25]#
B	26	HD[26]#
G	22	HD[27]#
C	26	HD[28]#
E	26	HD[29]#

Row	Column	Signal Name
L	24	HD[3]#
G	23	HD[30]#
B	28	HD[31]#
B	21	HD[32]#
G	21	HD[33]#
C	24	HD[34]#
C	23	HD[35]#
D	22	HD[36]#
C	25	HD[37]#
E	24	HD[38]#
D	24	HD[39]#
J	27	HD[4]#
G	20	HD[40]#
E	23	HD[41]#
B	22	HD[42]#
B	23	HD[43]#
F	23	HD[44]#
F	21	HD[45]#
C	20	HD[46]#
C	21	HD[47]#
G	18	HD[48]#
E	19	HD[49]#
G	28	HD[5]#
E	20	HD[50]#
G	17	HD[51]#
V	6	HL[6]
W	7	HL[7]
T	3	HL[8]
V	5	HL[9]
P	27	HLOCK#
T	2	HLRCOMP
W	3	HLSTB
V	2	HLSTB#
W	1	HLVREF
R	28	HREQ[0]#

Row	Column	Signal Name
P	25	HREQ[1]#
R	23	HREQ[2]#
R	25	HREQ[3]#
T	23	HREQ[4]#
H	10	HSYNC
M	25	HTRDY#
B	20	HXRCOMP
B	18	HXSWING
H	28	HYRCOMP
K	28	HYSWING
D	14	ICLKAM
E	13	ICLKAP
E	10	ICLKBM
F	10	ICLKBP
G	14	IYAM[0]
E	15	IYAM[1]
C	15	IYAM[2]
C	13	IYAM[3]
F	14	IYAP[0]
E	14	IYAP[1]
C	14	IYAP[2]
B	13	IYAP[3]
H	12	IYBM[0]
E	12	IYBM[1]
C	12	IYBM[2]
G	11	IYBM[3]
N	23	RS[0]#
P	26	RS[1]#
M	27	RS[2]#
AD	28	RSTIN#
AA	22	RSVD
L	3	DVOCBLANK#
J	3	DVOCCLK
J	2	DVOCCLK#
K	5	DVOCD[0]

Row	Column	Signal Name
K	1	DVOCD[1]
H	6	DVOCD[10]
G	3	DVOCD[11]
K	3	DVOCD[2]
K	2	DVOCD[3]
J	6	DVOCD[4]
J	5	DVOCD[5]
H	2	DVOCD[6]
H	1	DVOCD[7]
H	3	DVOCD[8]
H	4	DVOCD[9]
H	5	DVOCFLDSTL
K	6	DVOCHSYNC
L	5	DVOCVSYNC
F	12	RSVD
D	12	RSVD
B	12	RSVD
AA	5	RSVD
L	4	RSVD
C	4	GST[0]
F	3	RSVD
D	3	RSVD
C	3	GST[1]
B	3	RSVD
F	2	RSVD
D	2	RSVD
AE	3	SDQ[1]
AG	7	SDQ[10]
AE	8	SDQ[11]
AF	5	SDQ[12]
AH	4	SDQ[13]
AF	7	SDQ[14]
AH	6	SDQ[15]
AF	8	SDQ[16]
AG	8	SDQ[17]

Row	Column	Signal Name
AH	9	SDQ[18]
AG	10	SDQ[19]
AF	4	SDQ[2]
AH	7	SDQ[20]
AD	9	SDQ[21]
AF	10	SDQ[22]
AE	11	SDQ[23]
AH	10	SDQ[24]
AH	11	SDQ[25]
AG	13	SDQ[26]
AF	14	SDQ[27]
AG	11	SDQ[28]
AD	12	SDQ[29]
AH	2	SDQ[3]
AF	13	SDQ[30]
AH	13	SDQ[31]
AH	16	SDQ[32]
AG	17	SDQ[33]
AF	19	SDQ[34]
AE	20	SDQ[35]
AD	18	SDQ[36]
AE	18	SDQ[37]
AH	18	SDQ[38]
AG	19	SDQ[39]
AD	3	SDQ[4]
AH	20	SDQ[40]
AG	20	SDQ[41]
AE	3	SDQ[1]
AG	7	SDQ[10]
AE	8	SDQ[11]
AF	5	SDQ[12]
AH	4	SDQ[13]
AF	7	SDQ[14]
AH	6	SDQ[15]
AF	8	SDQ[16]

Row	Column	Signal Name
AG	8	SDQ[17]
AH	9	SDQ[18]
AG	10	SDQ[19]
AF	4	SDQ[2]
AH	7	SDQ[20]
AD	9	SDQ[21]
AF	10	SDQ[22]
AE	11	SDQ[23]
AH	10	SDQ[24]
AH	11	SDQ[25]
AG	13	SDQ[26]
AF	14	SDQ[27]
AG	11	SDQ[28]
AD	12	SDQ[29]
AH	2	SDQ[3]
AF	13	SDQ[30]
AH	13	SDQ[31]
AH	16	SDQ[32]
AG	17	SDQ[33]
AF	19	SDQ[34]
AE	20	SDQ[35]
AD	18	SDQ[36]
AE	18	SDQ[37]
AH	18	SDQ[38]
AG	19	SDQ[39]
AD	3	SDQ[4]
AH	20	SDQ[40]
AG	20	SDQ[41]
AG	2	SDQS[0]
AH	5	SDQS[1]
AH	8	SDQS[2]
AE	12	SDQS[3]
AH	17	SDQS[4]
AE	21	SDQS[5]
AH	24	SDQS[6]

Row	Column	Signal Name
AH	27	SDQS[7]
AD	15	SDQS[8]
AC	18	SMA[0]
AD	14	SMA[1]
AC	19	SMA[10]
AD	5	SMA[11]
AB	5	SMA[12]
AD	13	SMA[2]
AD	17	SMA[3]
AD	11	SMA[4]
AC	13	SMA[5]
AD	8	SMA[6]
AD	7	SMA[7]
AC	6	SMA[8]
AC	5	SMA[9]
AD	16	SMAB[1]
AC	12	SMAB[2]
AF	11	SMAB[4]
AD	10	SMAB[5]
AB	1	SMRCOMP
AJ	24	SMVREF_0
AJ	19	SMVSWINGH
AJ	22	SMVSWINGL
AC	21	SRAS#
AD	25	SWE#
W	21	VCC
AA	19	VCC
AA	17	VCC
H	7	VCCDVO
E	6	VCCDVO
M	4	VCCDVO
J	4	VCCDVO
E	4	VCCDVO
N	1	VCCDVO
J	1	VCCDVO

Row	Column	Signal Name
E	1	VCCDVO
A	4	VCCGPIO
A	3	VCCGPIO
V	9	VCCHL
W	8	VCCHL
U	8	VCCHL
V	7	VCCHL
U	6	VCCHL
W	5	VCCHL
Y	1	VCCHL
V	1	VCCHL
AJ	8	VCCQSM
AJ	6	VCCQSM
AG	29	VCCSM
AF	29	VCCSM
AC	29	VCCSM
AF	27	VCCSM
AJ	25	VCCSM
AF	24	VCCSM
AB	22	VCCSM
AJ	21	VCCSM
AF	21	VCCSM
AB	20	VCCSM
AF	18	VCCSM
AB	18	VCCSM
AJ	17	VCCSM
AB	16	VCCSM
AF	15	VCCSM
AB	14	VCCSM
AC	28	VSS
E	28	VSS
D	28	VSS
AJ	27	VSS
AG	27	VSS
AC	27	VSS

Row	Column	Signal Name
F	27	VSS
A	27	VSS
AJ	26	VSS
AB	26	VSS
W	26	VSS
U	26	VSS
R	26	VSS
N	26	VSS
L	26	VSS
J	26	VSS
G	26	VSS
AE	25	VSS
AA	25	VSS
D	25	VSS
A	25	VSS
AG	24	VSS
AA	24	VSS
V	24	VSS
T	24	VSS
P	24	VSS
M	24	VSS
K	24	VSS
H	24	VSS
F	24	VSS
B	24	VSS
AJ	23	VSS
AC	23	VSS
AA	23	VSS
D	23	VSS
AC	17	VSS
AB	17	VSS
U	17	VSS
R	17	VSS
N	17	VSS
H	17	VSS

Row	Column	Signal Name
D	17	VSS
A	17	VSS
AE	16	VSS
AA	16	VSS
T	16	VSS
P	16	VSS
J	16	VSS
F	16	VSS
AG	15	VSS
AB	15	VSS
U	15	VSS
R	15	VSS
N	15	VSS
H	15	VSS
D	15	VSS
AC	14	VSS
AA	14	VSS
T	14	VSS
P	14	VSS
J	14	VSS
AE	13	VSS
AB	13	VSS
U	13	VSS
R	13	VSS
N	13	VSS
H	13	VSS
F	13	VSS
D	13	VSS
A	13	VSS
AJ	12	VSS
J	7	VSS
G	7	VSS
E	7	VSS
C	7	VSS
AG	6	VSS

Row	Column	Signal Name
Y	6	VSS
L	6	VSS
Y	5	VSS
U	5	VSS
B	5	VSS
AE	4	VSS
AC	4	VSS
AA	4	VSS
W	4	VSS
T	4	VSS
N	4	VSS
K	4	VSS
G	4	VSS
D	4	VSS
AJ	3	VSS
AG	3	VSS
R	2	VSS
AJ	1	VSS
AE	1	VSS
AA	1	VSS
U	1	VSS
L	1	VSS
G	1	VSS
C	1	VSS
B	8	VSSADAC
B	11	VSSALVDS
J	9	VSYNC
V	29	VTTHF
M	29	VTTHF
H	29	VTTHF
U	21	VTTLF
R	21	VTTLF
N	21	VTTLF
L	21	VTTLF
H	20	VTTLF

Row	Column	Signal Name
A	20	VTTLF
J	19	VTTLF
H	18	VTTLF

Row	Column	Signal Name
A	18	VTTLF
H	16	VTTLF
G	15	VTTLF

8.1 Package Mechanical Information

The following figures provide details on the package information and dimensions of the Intel® 852GME GMCH and Intel 852PM MCH chipsets. The GMCH/MCH comes in a Micro-FCBGA package similar to the mobile processors. The package consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive. The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keepout area, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

Figure 16. Intel 852GME GMCH and Intel 852PM MCH Micro-FCBGA Package Dimensions (Top View)

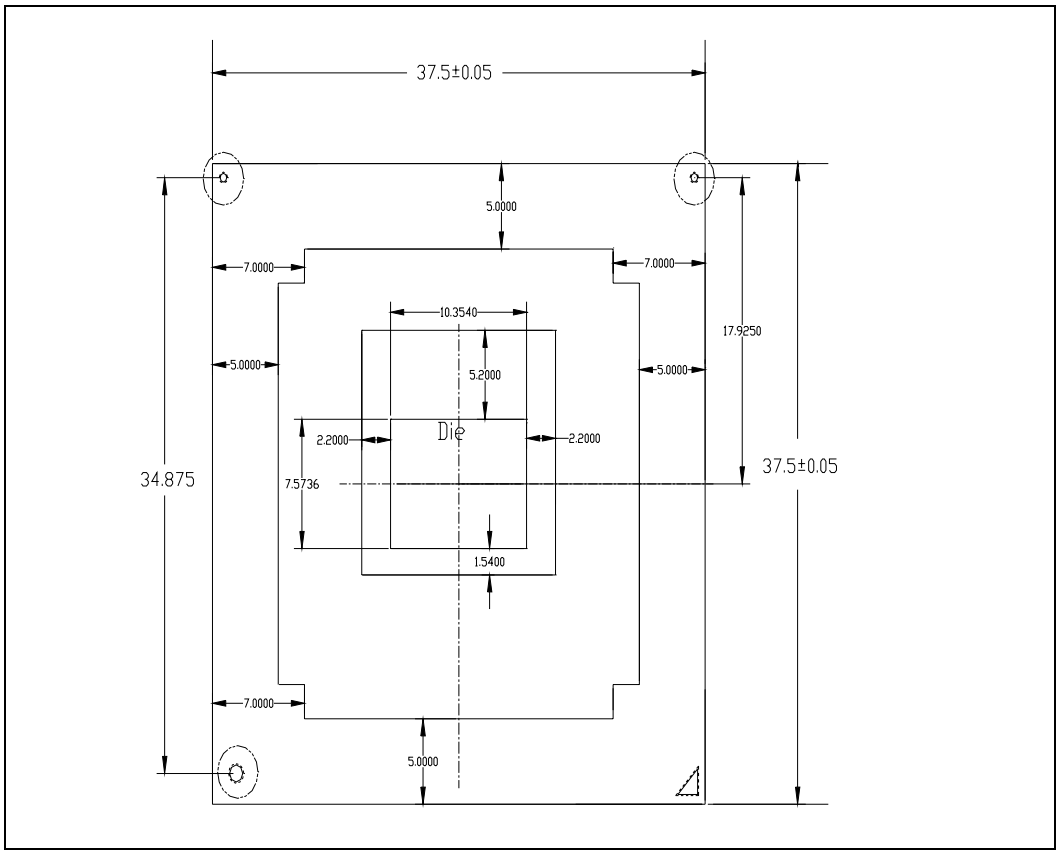


Figure 17. Intel 852GME GMCH and Intel 852PM MCH Micro-FCBGA Package Dimensions (Side View)