Intel® LXT3108

Octal T1/E1/J1 Long Haul/Short Haul Line Interface Unit

Datasheet

The Intel® LXT3108 is an octal 3.3 V Long Haul/Short Haul (LH/SH) T1/E1/J1 Line interface unit (LIU). This flexible LIU allows the design of T1/E1/J1 LH/SH multi-service cards with a single design and one bill of materials. The Intel® LXT3108 can be configured on a per-port basis through software. Intel's proven design makes the Intel® LXT3108 the perfect device for high-density T1/E1/J1 applications. To increase network reliability, the Intel® LXT3108 incorporates a DSP-based architecture with features such as Intel® Hitless Protection Switching (Intel® HPS) and Intel® Pulse Template Matching (Intel® PTM). The DSP-based architecture is less sensitive to power supply and temperature variations and allows the LIU to adapt to varying line conditions. Intel® HPS allows the design of 1+1 redundant cards without the use of relays as well as the ability to switch from one card to another without a loss of frame synchronization. Intel® PTM software allows the transmitter to shape the output pulse to meet various board conditions, without the need to change any external components.

Applications

- Voice over packet gateways
- Integrated Multi-service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse multiplexing for ATM (IMA)
- Wireless base stations
- Routers
- Frame relay access devices
- CSU/DSU equipment

Product Features

- Intel® HPS for 1+1 protection without relays
- Intel® PTM software for pulse output adjustment through software without component or board change
- Interfaces with the Intel® IXF3208, Octal T1/E1/J1 Framer with Intel® On-Chip Performance Report Messaging (Intel® On-Chip PRM)
- T1 (100 Ohm), E1 (75 and 120 Ohm), J1 (110 Ohm) termination and LH/SH selectable per port through software without component change
- Receiver sensitivity exceeds 36 dB @ 772 KHz and 43 dB @ 1024 KHz of cable attenuation providing margin for board and cable variations
- 3.3 V power supply with 5 V tolerant inputs
- On chip Clock Adaptor (CLAD) that allows one master clock for T1/E1/J1 applications (1X, 2X, 4X or 8X T1 or E1 clock)
- 16-bit BPV/Excess Zero counters per port
- B8ZS/HDB3 encoders and decoders, and unipolar/bipolar I/O modes selectable per port
- Digital Jitter Attenuator (DJA) in either receive or transmit path
- Meets or exceeds specifications in ANSI T1.102, T1.403 and T1.408; ITU I.431, CTR12/13, G.703, G.736, G.775 and G.823; ETSI 300-166 and 300-233; and AT&T Pub 62411
- Available in a 17 x 17 mm 256 PBGA (LXT3108 BE) or 28 x 28 mm 208 QFP (LXT3108 HE) package

Order Number: 249543-004
May 2002

Contents

Figures

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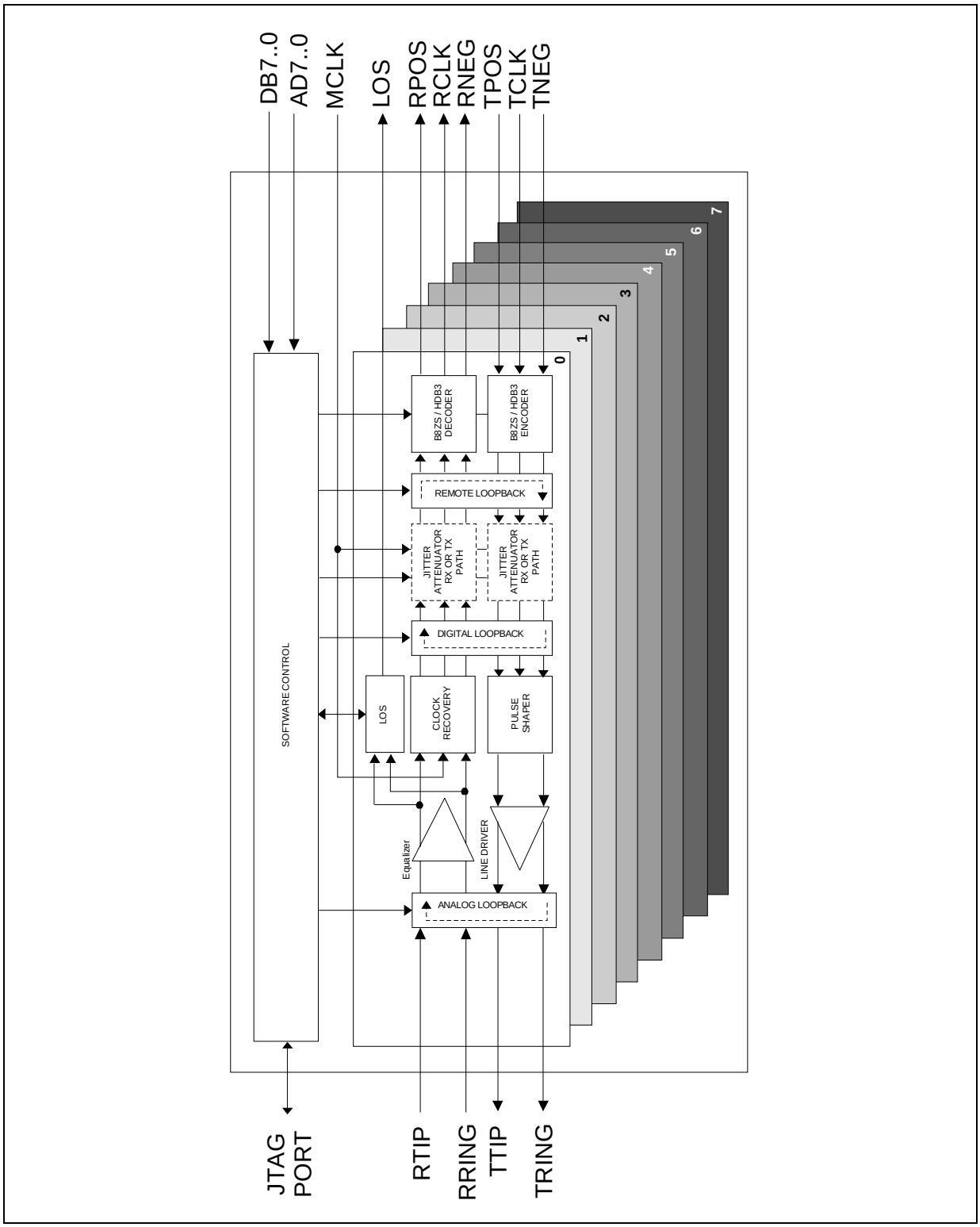
Revision History

Date	Revision	Description
May 2002	-004	Modified Figure: 2, 3, 5, 6, 7, 10, 32, 33, 34, 35 Modified Tables: 1, 4, 6, 8, 11, 12, 13, 14, 15, 18, 23, 24, 25, 26, 30, 44, 52, 63, 64, 66 Modified Section: 3.0, 4.0, 5.0, 6.0, 8.0, 9.0, 9.2, 10.1.2.1, 11.3.1, 11.3.2.1, 14.1.1, 14.1.2, Added Table: 43
Janyary 2002	-003	Modified Figures: 1 - 3, 5 - 7, 10, 14, 15, 32 - 36, and 38. Modified Tables: 1, 5, 9 - 11, 14 - 18, 20, 22, 23, 26, 29 - 31, 33 - 36, 39, 40, 45, 47, 48, 50 - 55, 61 - 63, 65, and 66. Modified Sections: 8.1, 8.2, 9.0, 9.2.1, 10.1, 10.2, 10.2.1, 10.3.1, 10.3.2, 11.0, 12.1.5, 12.3.2, 12.3.3.1, 12.3.3.2, 12.3.4, 13.0, 13.1, 13.2, 13.2.1, and 16.2. Deleted Section: 16.1 and 16.1.1 - 4. Deleted Tables: 58 - 61.
July 2001	-002	Modified Pages: 1, 22 - 28, and 30. Modified Tables: 1, 2, 44 - 53. Modified Figures:1-3, 5-7, 10, 11, 15, 26, 38 & 39. Modified: TOC, LOF and LOT. Added glossary.

Figure 1. Intel® LXT3108 LIU Block Diagram



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1.0 Pin Assignments

Figure 2. Intel® LXT3108 HE 208 Pin Assignment

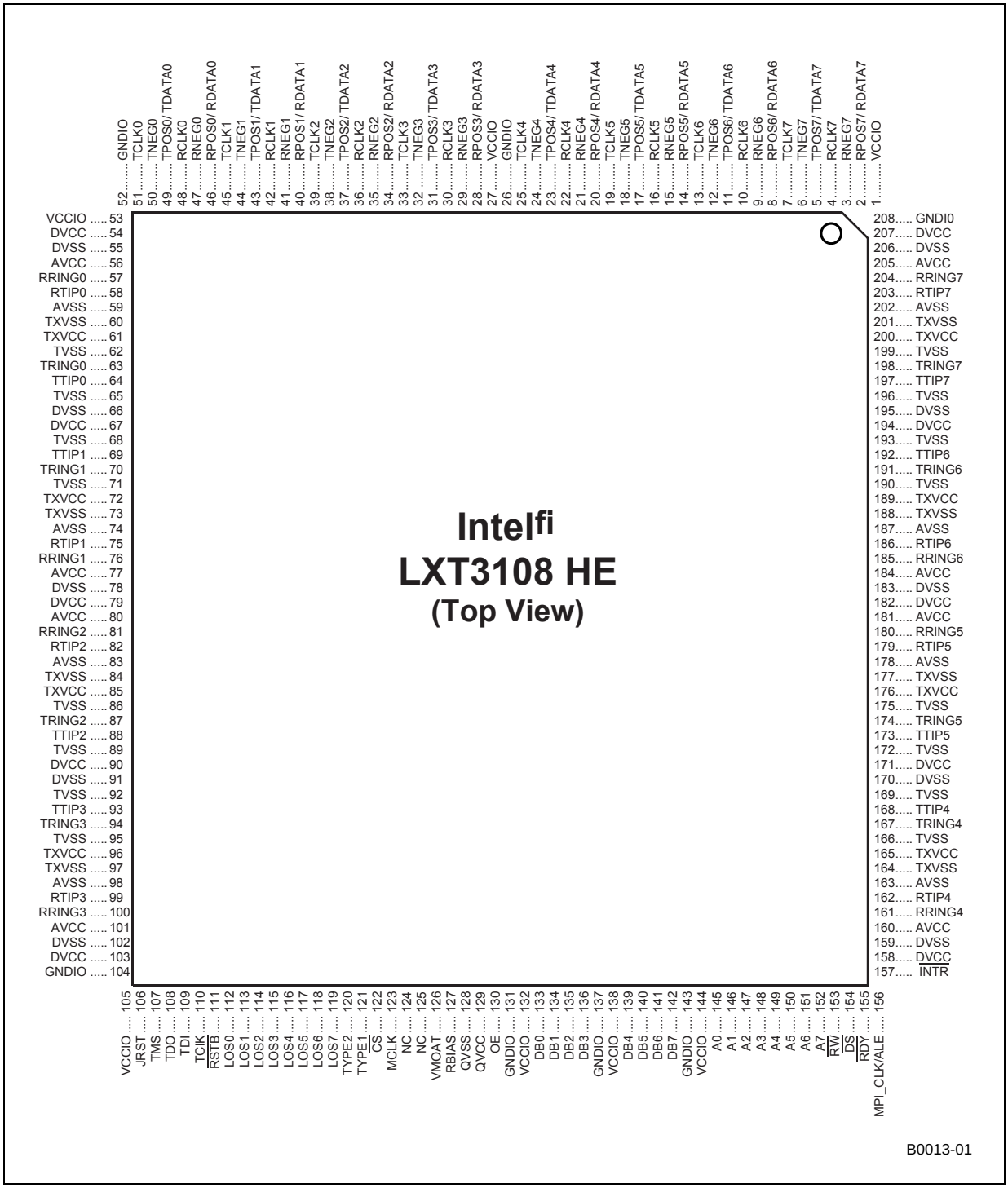
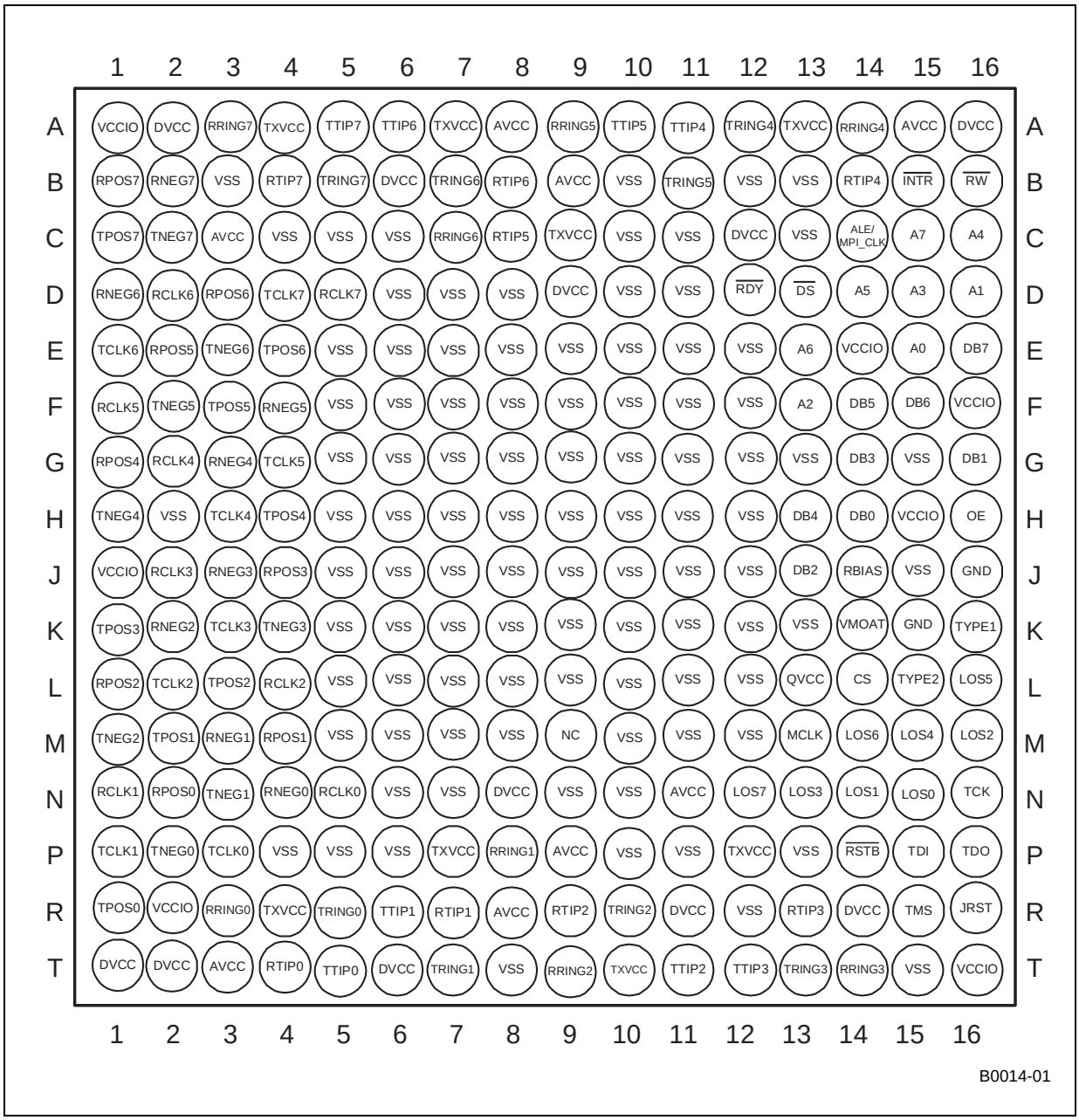


Figure 3. Intel® LXT3108 BE 256 Plastic Ball Grid Array (PBGA) Assignments



2.0 Signal Descriptions

Table 1. LXT3108 Pin Description (Sheet 1 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
1	A1	VCCIO	S	**Power (I/O).**	
2	B1	RPOS7/ RDATA7	DO	**Receive Positive Data/Receive Data Output (Port. 7).**	
				Acts as the positive side of the bipolar data output pair, RPOS7 and RNEG7, recovered from the line interface. RPOS7 acts as an active high NRZ receive data output. A High signal on RPOS7 corresponds to receipt of a positive pulse on RTIP/RRING. A High signal on RNEG7 corresponds to receipt of a negative pulse on RTIP/RRING. As default this signal along with RNEG7 is valid on the falling edge of RCLK7. The LXT3108 can be programmed to validate the RPOS7 and RNEG7data on the rising edge of the RCLK7. This rule applies to all ports (0 through 7).	RDATA7 digital framer interface pin acts as a single Non-Return-to-Zero (NRZ) output of the data recovered from the line interface.
3	B2	RNEG7/ RBPV7	DO	**Receive Negative Data (Port. 7).**	
				This digital framer interface pin acts as the negative side of the bipolar data output pair, RPOS7 and RNEG7, recovered from the line interface. RNEG7 acts as an active high NRZ receive signal output. A High signal on RNEG7 corresponds to receipt of a negative pulse on RTIP/RRING. This signal along with RPOS7 is valid on the falling edge of RCLK7.	RBPV7 indicates a receive BiPolar Violation (BPV). It goes High on receipt of a bipolar violation at the receiver. This is a NRZ output, valid by default on the falling edge of the RCLK. The clock edge validating this signal can be changed from falling edge to rising edge by software. This description applies to ports 0 through 7.
4	D5	RCLK7	DO	**Receive Clock Output (Port. 7).** This digital framer interface pin provides the recovered clock from the signal received at RTIP7 and RRING7. Under LOS conditions there is a transition from the RCLK7 signal (derived from the recovered data) to an internal clock (synthesized from the MCLK signal by CLAD circuitry) at the RCLK7 output.	

Table 1. LXT3108 Pin Description (Sheet 2 of 13)

<table>
<tr><th rowspan="2">QFP</th><th rowspan="2">PBGA</th><th rowspan="2">Symbol</th><th rowspan="2">I/O</th><th colspan="2">Description</th></tr>
<tr><th>Bipolar Mode</th><th>Unipolar Mode</th></tr>
<tr><td rowspan="2">5</td><td rowspan="2">C1</td><td rowspan="2">TPOS7/
TDATA7</td><td rowspan="2">DI</td><td colspan="2">Transmit Positive Data/Transmit Data Input (Port. 7)</td></tr>
<tr><td>Digital framer interface pin acts as the positive side of the bipolar data input pair, TPOS7 and TNEG7, which controls the signal transmitted to the line interface.
TPOS7 is an active high NRZ input that operates together with TNEG7. TPOS7 starts the transmission of a positive pulse on TTIP7/TRING7, whereas TNEG7 starts the transmission of a negative pulse on TTIP7/TRING7.
<table>
<tr><th>TPOS7</th><th>TNEG7</th><th>Selection</th></tr>
<tr><td>0</td><td>0</td><td>Space</td></tr>
<tr><td>1</td><td>0</td><td>Positive Mark</td></tr>
<tr><td>0</td><td>1</td><td>Negative Mark</td></tr>
<tr><td>1</td><td>1</td><td>Space</td></tr>
</table>
</td><td>TDATA7 acts as a single NRZ data input controlling the signal transmitted to the line interface.</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">C2</td><td rowspan="2">TNEG7</td><td rowspan="2">DI</td><td colspan="2">Transmit Negative Data (Port 7).</td></tr>
<tr><td>This digital framer interface pin acts as the negative side of the bipolar data input pair, TPOS7 and TNEG7, which controls the signal transmitted to the line interface.</td><td>Tie TNEG7 to ground in unipolar mode.</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">D4</td><td rowspan="2">TCLK7</td><td rowspan="2">DI</td><td colspan="2">Transmit Clock Input (Port 7).</td></tr>
<tr><td colspan="2">During normal operation TCLK7 toggles at the line rate, which is 1.544 MHz for T1/J1 operation, and 2.048 MHz for E1 operation. TPOS7 and TNEG7, or TDATA7, are sampled on the falling edge of TCLK7.
<table>
<tr><th>TCLK</th><th>Operating Mode</th></tr>
<tr><td>Clocked</td><td>Normal operation</td></tr>
<tr><td>L</td><td>Driver outputs three stated, but powered on for redundancy.</td></tr>
<tr><td>H</td><td>Driver outputs three stated and powered down for reduced power draw.</td></tr>
</table>
NOTE: The Transmit All Ones (TAOS) generator uses MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability.</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">D3</td><td rowspan="2">RPOS6/
RDATA6</td><td rowspan="2">DO</td><td colspan="2">Receive Positive Data/Receive Data Output (Port 6).</td></tr>
<tr><td>RPOS6 acts as the positive side of the bipolar data output pair, RPOS6 and RNEG6, recovered from the line interface.</td><td>RDATA6 acts as a single NRZ output of the data recovered from the line interface.</td></tr>
</table>

Table 1. LXT3108 Pin Description (Sheet 3 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
9	D1	RNEG6/ RBPV6	DO	**Receive Negative Data (Port 6).**	
				RNEG6 acts as the negative side of the bipolar data output pair, RPOS6 and RNEG6, recovered from the line interface.	RBPV6 indicates receive BPV for port 6.
10	D2	RCLK6	DO	**Receive Clock Output (Port 6)**. This digital framer interface pin provides the recovered clock from the signal received at RTIP6 and RRING6. Under LOS conditions there is a transition from the RCLK6 signal (derived from the recovered data) to an internal clock (synthesized from the MCLK signal by CLAD circuitry) at the RCLK6 output.	
11	E4	TPOS6/ TDATA6	DI	**Transmit Positive Data/Transmit Data Input (Port 6).**	
				TPOS6 acts as the positive side of the bipolar data input pair, TPOS6 and TNEG6, which controls the signal transmitted to the line interface.	TDATA6 acts as a single NRZ input data controlling the signal transmitted to the line interface.
12	E3	TNEG6	DI	**Transmit Negative Data (Port 6).**	
				TNEG6 acts as the negative side of the bipolar data input pair, TPOS6 and TNEG6, which controls the signal transmitted to the line interface.	Tie TNEG6 to ground in unipolar mode.
13	E1	TCLK6	DI	**Transmit Clock Input (Port 6).**	
14	E2	RPOS5/ RDATA5	DO	**Receive Positive Data/Receive Data Output (Port 5).**	
				RPOS5 acts as the positive side of the bipolar data output pair, RPOS5 and RNEG5, recovered from the line interface.	RDATA5 acts as a single NRZ output of the data recovered from the line interface.
15	F4	RNEG5/ RBPV5	DO	**Receive Negative Data (Port 5).**	
				RNEG5 acts as the negative side of the bipolar data output pair, RPOS5 and RNEG5, recovered from the line interface.	RBPV5 indicates Receive BPV for port 5.
16	F1	RCLK5	DO	**Receive Clock Output (Port 5).**	
17	F3	TPOS5/ TDATA5	DI	**Transmit Positive Data/Transmit Data Input (Port 5).**	
				TPOS5 acts as the positive side of the bipolar data input pair, TPOS5 and TNEG5, which controls the signal transmitted to the line interface.	TDATA5 acts as a single NRZ input data controlling the signal transmitted to the line interface.
18	F2	TNEG5	DI	**Transmit Negative Data (Port 5).**	
				TNEG5 acts as the negative side of the bipolar data input pair, TPOS5 and TNEG5, which controls the signal transmitted to the line interface.	Tie TNEG5 to ground in unipolar mode.
19	G4	TCLK5	DI	Transmit Clock Input (Port 5).	
20	G1	RPOS4/ RDATA4	DO	**Receive Positive Data/Receive Data Output (Port 4).**	
				RPOS4 acts as the positive side of the bipolar data output pair, RPOS4 and RNEG4, recovered from the line interface.	RDATA4 acts as a single NRZ output of the data recovered from the line interface.

Table 1. LXT3108 Pin Description (Sheet 4 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
21	G3	RNEG4/ RBPV4	DO	**Receive Negative Data (Port 4).**	
				RNEG4 acts as the negative side of the bipolar data output pair, RPOS4 and RNEG4, recovered from the line interface.	RBPV4 indicates Receive BPV for port 4.
22	G2	RCLK4	DO	Receive Clock Output (Port 4).	
23	H4	TPOS4/ TDATA4	DI	**Transmit Positive Data/Transmit Data Input (Port 4).**	
				TPOS4 acts as the positive side of the bipolar data input pair, TPOS4 and TNEG4, which controls the signal transmitted to the line interface.	TDATA4 acts as a single NRZ input data controlling the signal transmitted to the line interface.
24	H1	TNEG4	DI	**Transmit Negative Data (Port 4).**	
				TNEG4 acts as the negative side of the bipolar data input pair, TPOS4 and TNEG4, which controls the signal transmitted to the line interface.	Tie TNEG4 to ground in unipolar mode.
25	H3	TCLK4	DI	**Transmit Clock Input (Port 4).**	
26	H2	GNDIO	S	Ground (I/O).	
27	J1	VCCIO	S	Power (I/O).	
28	J4	RPOS3/ RDATA3	DO	**Receive Positive Data/Receive Data Output (Port 3).**	
				RPOS3 acts as the positive side of the bipolar data output pair, RPOS3 and RNEG3, recovered from the line interface.	RDATA3 acts as a single NRZ output of the data recovered from the line interface.
29	J3	RNEG3/ RBPV3	DO	**Receive Negative Data (Port 3).**	
				RNEG3 acts as the negative side of the bipolar data output pair, RPOS3 and RNEG3, recovered from the line interface.	This output indicates Receive BPV for port 3.
30	J2	RCLK3	DO	Receive Clock Output (Port 3).	
31	K1	TPOS3/ TDATA3	DI	**Transmit Positive Data/Transmit Data Input (Port 3).**	
				TPOS3 acts as the positive side of the bipolar data input pair, TPOS3 and TNEG3, which controls the signal transmitted to the line interface.	TDATA3 acts as a single NRZ input data controlling the signal transmitted to the line interface.
32	K4	TNEG3	DI	**Transmit Negative Data (Port 3).**	
				TNEG3 acts as the negative side of the bipolar data input pair, TPOS3 and TNEG3, which controls the signal transmitted to the line interface.	Tie TNEG3 to ground in unipolar mode.
33	K3	TCLK3	DI	Transmit Clock Input (Port 3).	
				Receive Positive Data/Receive Data Output (Port 2).	
34	L1	RPOS2/ RDATA2	DO	RPOS2 acts as the positive side of the bipolar data output pair, RPOS2 and RNEG2, recovered from the line interface.	RDATA2 acts as a single NRZ output of the data recovered from the line interface.

Table 1. LXT3108 Pin Description (Sheet 5 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
35	K2	RNEG2/ RBPV2	DO	**Receive Negative Data (Port 2).**	
				RNEG2 acts as the negative side of the bipolar data output pair, RPOS2 and RNEG2, recovered from the line interface.	This output indicates Receive BPV for port 2.
36	L4	RCLK2	DO	Receive Clock Output (Port 2).	
37	L3	TPOS2/ TDATA2	DI	**Transmit Positive Data/Transmit Data Input (Port 2).**	
				TPOS2 acts as the positive side of the bipolar data input pair, TPOS2 and TNEG2, which controls the signal transmitted to the line interface.	TDATA2 acts as a single NRZ input data controlling the signal transmitted to the line interface.
38	M1	TNEG2	DI	**Transmit Negative Data (Port 2).**	
				TNEG2 acts as the negative side of the bipolar data input pair, TPOS2 and TNEG2, which controls the signal transmitted to the line interface.	Tie TNEG2 to ground in unipolar mode.
39	L2	TCLK2	DI	Transmit Clock Input (port 2).	
40	M4	RPOS1/ RDATA1	DO	**Receive Positive Data/Receive Data Output (Port 1).**	
				RPOS1 acts as the positive side of the bipolar data output pair, RPOS1 and RNEG1, recovered from the line interface.	RDATA1 acts as a single NRZ output of the data recovered from the line interface.
41	M3	RNEG1/ RBPV1	DO	**Receive Negative Data (Port 1).**	
				RNEG1 acts as the negative side of the bipolar data output pair, RPOS1 and RNEG1, recovered from the line interface.	This output indicates Receive BPV for port 0.
42	N1	RCLK1	DO	**Receive Clock Output (Port 1).** This digital framer interface pin provides the recovered clock from the signal received at RTIP1 and RRING1. Under LOS conditions there is a transition from the RCLK1 signal (derived from the recovered data) to an internal clock (synthesized from the MCLK signal by CLAD circuitry) at the RCLK1 output.	
43	M2	TPOS1/ TDATA1	DI	**Transmit Positive Data/Transmit Data Input (Port 1).**	
				TPOS1 acts as the positive side of the bipolar data input pair, TPOS1 and TNEG1, which controls the signal transmitted to the line interface.	TDATA1 acts as a single NRZ input data controlling the signal transmitted to the line interface.
44	N3	TNEG1	DI	**Transmit Negative Data (Port 1).**	
				TNEG1 acts as the negative side of the bipolar data input pair, TPOS1 and TNEG1, which controls the signal transmitted to the line interface.	Tie TNEG1 to ground in unipolar mode.
45	P1	TCLK1	DI	Transmit Clock Input (Port 1).	
46	N2	RPOS0/ RDATA0	DO	**Receive Positive Data/Receive Data Output (Port 0).**	
				RPOS0 acts as the positive side of the bipolar data output pair, RPOS0 and RNEG0, recovered from the line interface.	RDATA0 acts as a single NRZ output of the data recovered from the line interface.

Table 1. LXT3108 Pin Description (Sheet 6 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
47	N4	RNEG0/ RBPV0	DO	**Receive Negative Data (Port 0).**	
				RNEG0 acts as the negative side of the bipolar data output pair, RPOS0 and RNEG0, recovered from the line interface.	This output indicates Receive BPV for port 0.
48	N5	RCLK0	DO	**Receive Clock Output (Port 0).** This digital framer interface pin provides the recovered clock from the signal received at RTIP0 and RRING0. Under LOS conditions there is a transition from the RCLK0 signal (derived from the recovered data) to an internal clock (synthesized from the MCLK signal by CLAD circuitry) at the RCLK0 output.	
49	R1	TPOS0/ TDATA0	DI	**Transmit Positive Data/Transmit Data Input (Port 0).**	
				TPOS0 acts as the positive side of the bipolar data input pair, TPOS0 and TNEG0, which controls the signal transmitted to the line interface.	TDATA0 acts as a single NRZ input data controlling the signal transmitted to the line interface.
50	P2	TNEG0	DI	**Transmit Negative Data (Port 0).**	
				TNEG0 acts as the negative side of the bipolar data input pair, TPOS0 and TNEG0, which controls the signal transmitted to the line interface.	Tie TNEG0 to ground in unipolar mode.
51	P3	TCLK0	DI	Transmit Clock Input (Port 0).	
52	P4	GNDIO	S	Ground (I/O).	
53	R2	VCCIO	S	Power (I/O).	
54	T1	DVCC	S	Digital Power 3.3V.	
55	L6	DVSS	S	Digital Ground.	
56	T3	AVCC	S	Analog Power 3.3V.	
57	R3	RRING0	AI	**Receive Ring Input (Port 0).** RRING0 is one of the pair of inputs, RRING0/ RTIP0, to the differential line receiver at the line interface for the port. Data and clock are recovered and output at the digital framer interface output pins.	
58	T4	RTIP0	AI	**Receive Tip Input (Port 0)**. RTIP0 is one of the pair of inputs, RRING0/ RTIP0, to the differential line receiver at the line interface for the port. Data and clock are recovered and output at the digital framer interface output pins.	
59	P5	AVSS	S	**Analog Ground.**	
60	P6	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.	
61	P7	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.	
62	N6	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
63	R5	TRING0	AO	**Transmit Ring Output (Port 0).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP0/TRING0. TTIP0/TRING0 will be in a high impedance state if the TCLK pin is static or if the OE pin is Low. TTIP0/TRING0 can be in a the high impedance state on a port-by-port basis by writing a '1' to the TXPD bit in "Port Master Control Page Register, 01h" on page 73, or the OES bit in "Transmit Control Page Register, 03h" on page 74. Please refer to "Transmit Idle Operation and Tri-stating Drivers" on page 48 for details.	
64	T5	TTIP0	AO	**Transmit Tip Output (Port 0).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP0/TRING0.	

Table 1. LXT3108 Pin Description (Sheet 7 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
65	N7	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
66	T8	DVSS	S	Digital Ground.	
67	T6	DVCC	S	Digital Power 3.3V	
68	N9	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
69	R6	TTIP1	AO	**Transmit Tip Output (Port 1).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP1/TRING1.	
70	T7	TRING1	AO	**Transmit Ring Output (Port 1).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP1/TRING1.	
71	P10	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
72	R4	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.	
73	P11	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.	
74	G13	AVSS	S	Analog Ground	
75	R7	RTIP1	AI	**Receive Tip Input (Port 1).** RTIP1 is one of the pair of inputs, RRING1/ RTIP1, to the differential line receiver at the line interface for the port.	
76	P8	RRING1	AI	**Receive Ring Input (port 1).** RRING1 is one of the pair of inputs, RRING1/ RTIP1, to the differential line receiver at the line interface for the port.	
77	P9	AVCC	S	Analog Power 3.3V.	
78	N10	DVSS	S	Digital Ground.	
79	R11	DVCC	S	Digital Power 3.3V.	
80	R8	AVCC	S	Analog Power 3.3V.	
81	T9	RRING2	AI	Receive Ring Input (Port 2). RRING2 is one of the pair of inputs, RRING2/ RTIP2, to the differential line receiver at the line interface for the port.	
82	R9	RTIP2	AI	Receive Tip Input (port 2). RTIP2 is one of the pair of inputs, RRING2/RTIP2, to the differential line receiver at the line interface for the port.	
83	L5	AVSS	S	Analog Ground.	
84	R12	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.	
85	P12	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.	
86	P13	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
87	R10	TRING2	AO	**Transmit Ring Output (Port 2).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP2/TRING2.	
88	T11	TTIP2	AO	**Transmit Tip Output (Port 2).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP2/TRING2.	
89	T15	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
90	R14	DVCC	S	Digital Power 3.3V.	
91	M11	DVSS	S	Digital Ground.	
92	M12	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
93	T12	TTIP3	AO	**Transmit Tip Output (Port 3).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP3/TRING3.	
94	T13	TRING3	AO	**Transmit Ring Output (Port 3).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP3/TRING3.	

Table 1. LXT3108 Pin Description (Sheet 8 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
95	M10	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
96	T10	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.	
97	M7	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.	
98	M8	AVSS	S	Analog Ground.	
99	R13	RTIP3	AI	**Receive Tip Input (Port 3).** RTIP3 is one of the pair of inputs, RRING3/ RTIP3, to the differential line receiver at the line interface for the port.	
100	T14	RRING3	AI	**Receive Ring Input (Port 3).** RRING3 is one of the pair of inputs, RRING3/ RTIP3, to the differential line receiver at the line interface for the port.	
101	N11	AVCC	S	Analog Power 3.3V.	
102	M6	DVSS	S	Digital Ground.	
103	N8	DVCC	S	Digital Power 3.3V.	
104	M5	GNDIO	S	Ground (I/O).	
105	T16	VCCIO	S	Power (I/O).	
106	R16	JRST	DI	**JTAG Controller Reset Input.** Input is used to reset the JTAG controller. JRST should be tied to ground through a 1K resistor if JTAG is not used. For systems that use JTAG, follow IEEE 1149 standards to initialize this device.	
107	R15	TMS	DI	**JTAG Test Mode Select Input.** Used to control the test logic state machine. Sampled on rising edge of TCK. TMS is pulled up internally and may be left disconnected.	
108	P16	TDO	DO	**JTAG Data Output.** During JTAG operation, TDO is Test Data Output for JTAG. Used for reading all serial configuration and test data from internal test logic. It is updated on falling edge of TCK.	
109	P15	TDI	DI	**JTAG Data Input.** TDI is Test Data input for JTAG. Used for loading serial instructions and data into internal test logic. Sampled on rising edge of TCK. TDI is pulled up internally and may be left disconnected.	
110	N16	TCK	DI	**JTAG Clock Input.** TCK is clock input for JTAG. Connect to GND when not used.	
111	P14	$\overline{\text{RSTB}}$	DI	**Reset.** $\overline{\text{RSTB}}$ is the reset pin for the LXT3108 octal LIU. One microsecond after $\overline{\text{RSTB}}$ goes Low, the internal registers will be restored to their default values.	
112	N15	LOS0	DO	**Loss of Signal Output (Port 0).** When the LOS0 output is High, it indicates a loss of signal at the port's line interface receiver. LOS goes active after the incoming signal has insufficient transitions for a specified time interval, which is determined by the page and global register settings. The LOS condition is cleared and the output pin returns to Low when the incoming signal has a sufficient number of transitions in a specified time interval, as determined by the register settings.	
113	N14	LOS1	DO	Loss of Signal Output (Port 1).	
114	M16	LOS2	DO	Loss of Signal Output (Port 2).	
115	N13	LOS3	DO	Loss of Signal Output (Port 3).	
116	M15	LOS4	DO	Loss of Signal Output (Port 4).	
117	L16	LOS5	DO	Loss of Signal Output (Port 5).	
118	M14	LOS6	DO	Loss of Signal Output (Port 6).	
119	N12	LOS7	DO	Loss of Signal Output (port 7).	

Table 1. LXT3108 Pin Description (Sheet 9 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
120	L15	TYPE2	DI	**Microprocessor Type Select Inputs**. These pins control which microprocessor interface is active: Type2Type1Microprocessor 0 0 MPC860, M68360 0 1 i960, i486 1 0 M68302 1 1 Reserved	
121	K16	TYPE1	DI		
122	L14	$\overline{CS}$	DI	**Chip Select**. This active Low input initiates each access to the parallel microprocessor interface. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.	
123	M13	MCLK	DI	**Master Clock Input.** MCLK is an independent, free-running reference clock. After initialization the frequency can be set to 8, 4, 2 or 1x of the T1/E1/J1 frequency. Refer to CLAD Configuration Register (Address 11h) for MCLK frequency selection. This reference clock is used to generate several internal reference signals: • Timing reference for the integrated clock recovery unit. • Timing reference for the integrated digital jitter attenuator. • Generation of RCLK signal during a loss of signal condition. • Reference clock during a blue alarm transmit all ones (TAOS) condition. • Reference timing for the parallel processor wait state generation logic.	
124	K15	GND		Ground.	
125	J16	GND		Ground.	
126	K14	VMOAT	AI	Substrate Ground.	
127	J14	RBIAS	AI	**Resistor Bias Input.** A 30.1 K Ω, 1% ±100 PPM/°C, resistor must be connected from this pin to analog ground. The Panasonic ERJ-8ENF3012V resistor is recommended.	
128	K13	QVSS	AI	Ground for analog bias circuit.	
129	L13	QVCC	AI	Power for analog bias circuit. 3.3V	
130	H16	OE	DI	**Output Driver Enable Input.** If this pin is asserted low every port's analog driver/transmitter output immediately enters a high impedance state to support redundancy applications without external mechanical relays. All other internal circuitry stays active. TTIP and TRING for each port can also be placed in the high impedance state individually by writing a '1' to the TXPD bit in "Port Master Control Page Register, 01h" on page 73 or the OES bit in the "Transmit Control Page Register, 03h" on page 74. Please refer to "Transmit Idle Operation and Tri-stating Drivers" on page 48 for details.	
131	L12	GNDIO	S	Ground (I/O).	
132	H15	VCCIO	S	**Power (I/O).**	
133 134 135 136	H14 G16 J13 G14	DB0 DB1 DB2 DB3	DI/O DI/O DI/O DI/O	**Data Bus Input/Output.** When a non-multiplexed microprocessor interface is selected, these pins function as a bi-directional 8-bit data bus. When a multiplexed microprocessor interface is selected, these pins carry both bi-directional 8-bit data and address inputs A0 -A7.	
137	J15	GNDIO	S	Ground (I/O).	
138	F16	VCCIO	S	Power (I/O).	

Table 1. LXT3108 Pin Description (Sheet 10 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
139 140 141 142	H13 F14 F15 E16	DB4 DB5 DB6 DB7	DI/O DI/O DI/O DI/O	**Data Bus Input/Output.** When a non-multiplexed microprocessor interface is selected, these pins function as a bi-directional 8-bit data bus. When a multiplexed microprocessor interface is selected, these pins carry both bi-directional 8-bit data and address inputs A0 -A7.	
143	G15	GNDIO	S	Ground (I/O).	
144	E14	VCCIO	S	Power (I/O).	
145 146 147 148 149 150 151 152	E15 D16 F13 D15 C16 D14 E13 C15	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	DI DI DI DI DI DI DI DI	**Address Bus Input.** In non-multiplexed mode these inputs function as address input pins for the microprocessor bus.	
153	B16	$\overline{RW}$	DI	$\overline{RW}$ has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. • **Read/Write Input** (Motorola Mode). • **Write Enable Active Low Input** (Intel mode).	
154	D13	$\overline{DS}$	DII	$\overline{DS}$ has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. • **Data Strobe Input** (Motorola Mode). • **Read Enable Active Low Input** (Intel mode)	
155	D12	$\overline{RDY}$	DO	$\overline{RDY}$ has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. • **Data Transfer Acknowledge Output.** (Motorola Mode). • **Ready Output** (Intel mode). A Low signal on $\overline{RDY}$ during a read operation indicates that the information on the data bus is valid. A Low signal during a write operation acknowledges that a data transfer into the addressed register has been accepted (acknowledge signal).	
156	C14	MPI_CLK/ ALE	DI	This pin has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. **Microprocessor Clock** (Intel i486 Mode and Mot 860 mode). • MPI_CLK is used to input the microprocessor clock in the synchronous i486/ i960 and Mot 860 mode. **Address Latch Enable Input** (Intel Mode). • The address on the multiplexed address/data bus is clocked into the device with the falling edge of ALE.	
157	B15	$\overline{INTR}$	DO	**Interrupt.** This is an active Low output. If the corresponding interrupt enable bit is enabled, $\overline{INTR}$ goes Low to flag the microprocessor when the LXT3108 changes state (see details in the interrupt handling section). The microprocessor interrupt input should be set to level triggering.	
158	A16	DVCC	S	Digital Power 3.3V.	
159	E12	DVSS	S	Digital Ground.	
160	A15	AVCC	S	Analog Power 3.3V.	

Table 1. LXT3108 Pin Description (Sheet 11 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
161	A14	RRING4	AI	Receive Ring Input (Port 4). RRING4 is one of the pair of inputs, RRING4/ RTIP4, to the differential line receiver at the line interface for the port.	
162	B14	RTIP4	AI	Receive Tip Input (Port 4). RTIP4 is one of the pair of inputs, RRING4/RTIP4, to the differential line receiver at the line interface for the port.	
163	C13	AVSS	S	Analog Ground.	
164	D11	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.	
165	A13	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.	
166	B13	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
167	A12	TRING4	AO	**Transmit Ring Output (Port 4).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP4/TRING4.	
168	A11	TTIP4	AO	**Transmit Tip Output (Port 4).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP4/TRING4.	
169	B12	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
170	C11	DVSS	S	Digital Ground.	
171	C12	DVCC	S	Digital Power 3.3V.	
172	D10	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
173	A10	TTIP5	AO	**Transmit Tip Output (Port 5).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP5/TRING5.	
174	B11	TRING5	AO	**Transmit Ring Output (Port 5).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP5/TRING5.	
175	E10	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
176	A7	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.	
177	B10	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.	
178	C10	AVSS	S	Analog Ground.	
179	C8	RTIP5	AI	**Receive Tip Input (Port 5).** RTIP5 is one of the pair of inputs, RRING5/ RTIP5, to the differential line receiver at the line interface for the port.	
180	A9	RRING5	AI	**Receive Ring Input (Port 5).** RRING5 is one of the pair of inputs, RRING5/ RTIP5, to the differential line receiver at the line interface for the port.	
181	A8	AVCC	S	Analog Power 3.3V.	
182	B6	DVCC	S	Digital Power 3.3V.	
183	D6	DVSS	S	Digital Ground.	
184	B9	AVCC	S	Analog Power 3.3V.	
185	C7	RRING6	AI	Receive Ring Input (Port 6). RRING6 is one of the pair of inputs, RRING6/ RTIP6, to the differential line receiver at the line interface for the port.	
186	B8	RTIP6	AI	Receive Tip Input (port 6). RTIP6 is one of the pair of inputs, RRING6/RTIP6, to the differential line receiver at the line interface for the port.	
187	D7	AVSS	S	Analog Ground.	
188	E6	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.	
189	C9	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.	
190	B3	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	

Table 1. LXT3108 Pin Description (Sheet 12 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
191	B7	TRING6	AO	**Transmit Ring Output (Port 6).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP6/TRING6.	
192	A6	TTIP6	AO	**Transmit Tip Output (Port 6).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP6/TRING6.	
193	C4	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
194	A2	DVCC	S	Digital Power 3.3V.	
195	C5	DVSS	S	Digital Ground.	
196	C6	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
197	A5	TTIP7	AO	**Transmit Tip Output (Port 7).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP7/TRING7.	
198	B5	TRING7	AO	**Transmit Ring Output (Port 7).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP7/TRING7.	
199	E5	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.	
200	A4	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.	
201	E8	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.	
202	E7	AVSS	S	Analog Ground.	
203	B4	RTIP7	AI	**Receive Tip Input (Port 7).** RTIP7 is one of the pair of inputs, RRING7/ RTIP7, to the differential line receiver at the line interface for the port.	
204	A3	RRING7	AI	**Receive Ring Input (Port 7).** RRING7 is one of the pair of inputs, RRING7/ RTIP7, to the differential line receiver at the line interface for the port.	
205	C3	AVCC	S	Analog Power 3.3V.	
206	E9	DVSS	S	Digital Ground.	
207	D9	DVCC	S	Digital Power 3.3V.	
208	E11	GNDIO	S	Ground (I/O).	

Table 1. LXT3108 Pin Description (Sheet 13 of 13)

QFP	PBGA	Symbol	I/O	Description	
				Bipolar Mode	Unipolar Mode
	T2	DVCC	S	Digital Power 3.3V.	
	M9			This pin must be left floating.	
	D8, F5, F6, F7, F8, F9, F10, F11, F12, G5, G6, G7, G8, G9, G10, G11, G12, H5, H6, H7, H8, H9, H10, H11, H12, J5, J6, J7, J8, J9, J10, J11, J12, K5, K6, K7, K8, K9, K10, K11, K12, L7, L8, L9, L10, L11, M8	VSS	S	Ground.	

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3.0 T1/E1/J1 Nomenclature

The nomenclature in this document follows telecommunication industry standard conventions, i.e., bit, channel, and frame numbering increase sequentially with time. In the case of bit ordering, unless otherwise stated, the Most Significant Bit (MSB) is transmitted first and is designated Bit 1.

T1 will refer to both T1 and J1 operation throughout this document.

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4.0 Intel® LXT3108 LIU Nomenclature

The Intel® LXT3108 LIU is an octal device, meaning that it supports up to eight T1/E1/J1 ports. The ports are numbered sequentially, beginning with zero and ending with seven.

A port is defined as the standard 4-wire receive/transmit pair T1/E1/J1 interface.

Port and channel are used interchangeably in this document and all related documents.

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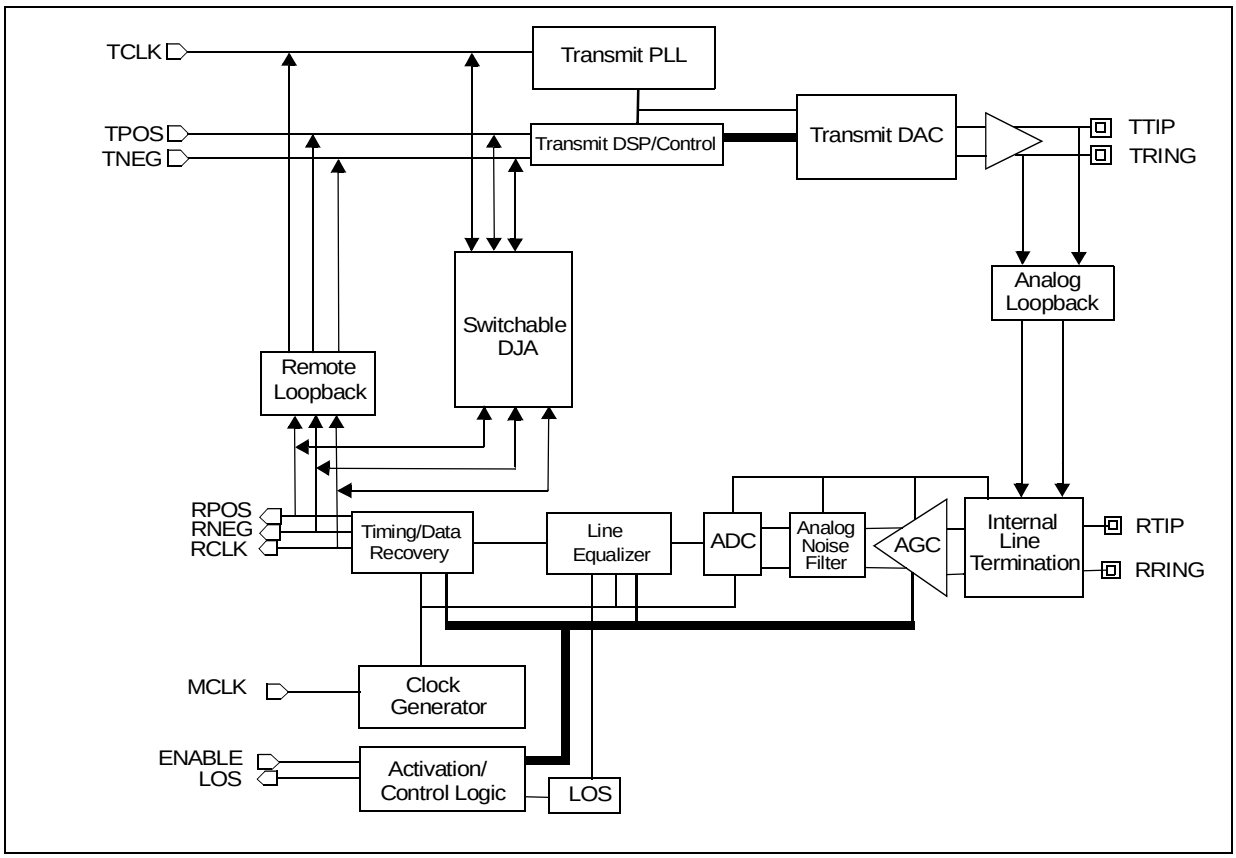
5.0 Functional Description

Each port consists of a transmitter and a receiver with a jitter attenuator switched between each path. Access to the host device is via a microprocessor parallel interface configured in either Intel® or Motorola* mode. JTAG built-in test chains enable on-board verification of digital pins and functions.

Figure 4. T1/E1/J1 LIU Block Diagram



Each of the eight transmitters consists of a current mode output driver, a second-order charge pump Phase Lock Loop (PLL), a simple digital Finite Infinite Response (FIR) filter and a switched-current Digital to Analog Converter (DAC). The FIR filter, in combination with the transmitter DAC, provides shaped pulses fitting the pulse shape to the various T1 and E1 pulse templates. A ROM is used to store coefficients and settings for the digital transmit waveform generator.

Each of the eight receivers' Analog Front Ends (AFE) consists of an Automatic Gain Control (AGC) amplifier, anti-aliasing filter, and Analog to Digital Converter (ADC). The digital section consists of a digital noise filter, a root-f equalizer, a decision feedback equalizer, timing recovery, and adaptation control logic, as shown in Figure 4 on page 31. A ROM is used to store coefficients and settings for the receiver digital filters.

The programmer controls overall device operation of the Intel® LXT3108 LIU through global registers. Each individual LIU is separately controlled by a set of PPRs. There are eight sets of PPRs, one for each port. It is also possible to write to all ports at the same time in the case where all ports need to be set up with the same configuration.

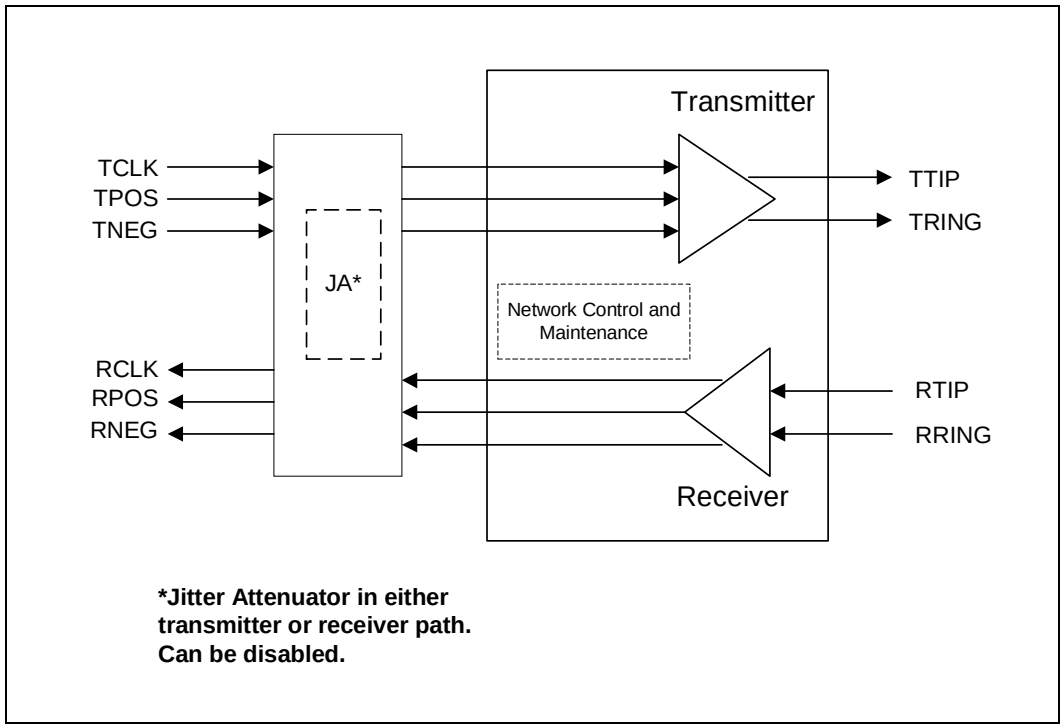
The Intel® LXT3108 LIU jitter attenuator enhances compatibility with the existing network by complying with jitter control standards The jitter performance of the Intel® LXT3108 LIU conforms to the stringent specifications of AT&T* Pub. 62411 and ITU* TBR12/13. The jitter attenuator is completely digital and does not require an external crystal. The Intel® LXT3108 LIU has the capability to insert a Jitter Attenuator (JA) in either the transmit or receive data path individually for each port.

6.0 Port Descriptions

The Intel® LXT3108 LIU is a port-by-port programmable, fully integrated eight-port LIU with jitter attenuator as well as network control and maintenance functions. Each Intel® LXT3108 LIU port is suitable for mixed LH or SH, T1/E1/J1 telecommunications applications allowing full-duplex transmission of digital data over existing cable installations. Under microprocessor control and with a single MCLK source, each port can individually operate:

- at either T1/J1 or E1 line rates
- at separate line termination impedance settings
- with default or programmable transmit signal
- with preset or customized receiver sensitivity
- with the jitter attenuator in either the transmit or receive path, or disabled
- with or without zero suppression line coding

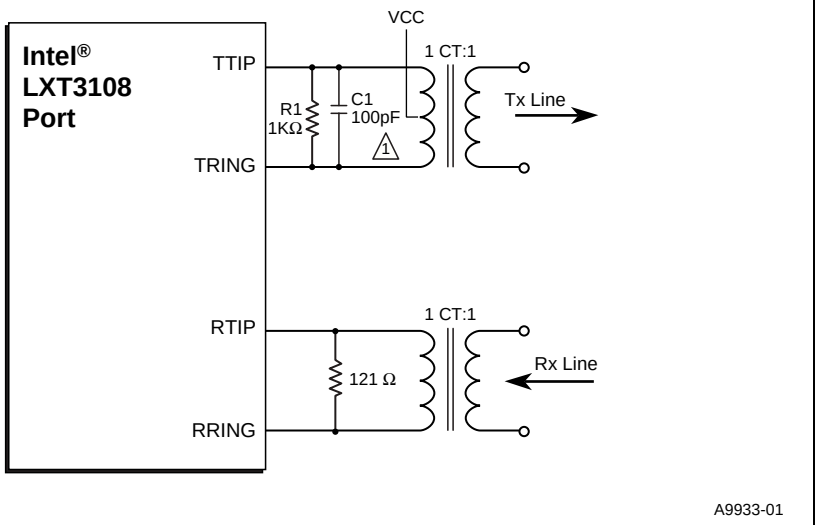
Figure 5. Intel® LXT3108 LIU Port Block Diagram



An eight-bit wide data bus conveys commands from a microprocessor to each port individually or toall ports at the same time by a two-step process. First, writing the port number to the global register described in Table 18, “Port Page Select Register, CPS, 00h” on page 70 chooses the port. The next read or write operation can then reach one of the 32 Port Page Registers (PPRs) adjusting preset port parameters. Besides the PPRs, the designer can also access 48 ATWG registers described in Table 44, “Transmit Coefficient Page Register Range, 40h-6Fh” on page 80.

The Intel® LXT3108 LIU is fully T1/E1/J1 selectable without the need to change any external components for twisted pair applications, allowing the development of a single board design to support T1 and E1 designs. The J1 line rate and transformer configuration are the same for T1 and J1 cable. The line interface to the cables is through standard T1 and E1 telecommunications transformers and resistors. Each LIU front-end interfaces with two twisted pairs: one pair for transmit, and one pair for receive. These two pairs comprise a digital data loop for full duplex operation.

Figure 6. Intel® LXT3108 LIU Port Circuit



1. Actual values of R1 and C1 may vary depending on design.

Framed or unframed data clocked by TCLK to TPOS/TNEG or TDATA inputs activates the wave-shaping and line driver circuits. The port's transmitter will drive T1 or E1 lines from TTIP and TRING pins out to standard telecommunications T1 or E1 transformers. The line driver can handle both LH and SH lines for T1/E1/J1.

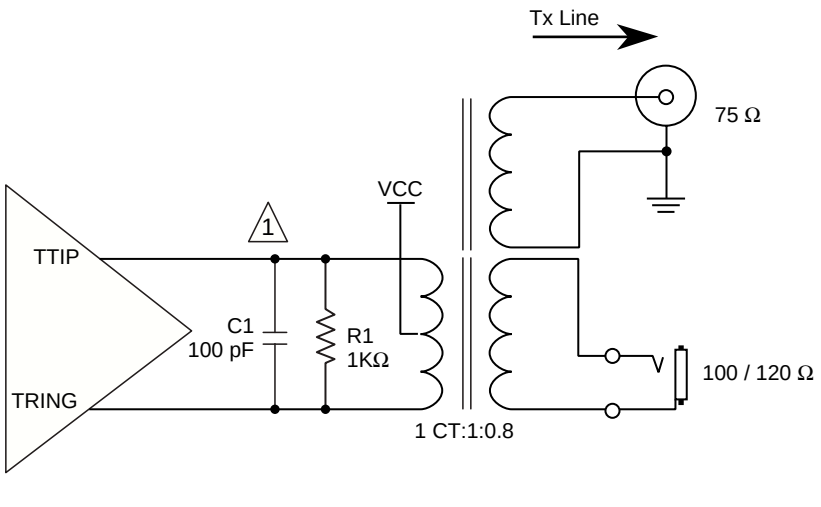
Preset and programmable pulse shaping suits both LH and SH environments. Each port provides eight built-in equalization settings for SH applications and six line build outs for LH applications. In addition, the Intel® PTM software allows the transmitter performance to be tuned for a wide variety of line conditions or special applications. The PTM software provides eight bits of amplitude resolution and either 15 (T1) or 16 (E1) phases of time resolution for up to three Unit Intervals (UI). The combination of proven preset wave-shaping settings and the PTM software means the designer has increased flexibility in meeting the design challenges of copper interfaces.

A simplified transmitter circuit configuration offers:

- Port-by-port programmable line impedance matching.
- Reduced port component count.
- Current limiting for short-circuits.

By programming the internal transmitter termination, matching the line impedance requires no component changes for twisted pair and coaxial cable applications, as shown in Figure 7.

Figure 7. Transmitter Circuit for Twisted Pair and Coaxial Cable



NOTE:
1. Actual values of R1 and C1 may vary depending on design.

Trimming each port's transmitter circuit components to a single transformer and a capacitor increases design flexibility. The transmitter's current mode driver is self-limiting to provide built in short circuit protection. Efficient and flexible line circuit configuration increases designer options and maintains line protection.

A single mandatory clock reference, MCLK, shared between all eight clock recovery circuits, enables each receiver in the Intel® LXT3108 LIU to recover the clock and data signals from the line interface. When selected, after smoothing the recovered signals through the jitter attenuator, RCLK clocks out RDATA or RPOS/RNEG at the port's digital framer interface. Each port's receiver dynamic range is from 0 to -43 dB for E1 operation and 0 to -36 dB for T1 operation. This translates to cable reach of at least 2.5 kilometers on 0.63 mm cables (E1) and at least 6000 feet on 22 AWG cables (T1).

The analog AMI waveform from the E1, T1, or J1 line is transformer-coupled into the port's RTIP and RRING pins through the Intel® LXT3108 LIU's internal receive termination. This programmable input termination can select between 100, 110, or 120 Ω applications, eliminating the need to change external components for twisted-pair cable. The designer has the option of selecting by software the internal receive line termination, or bypassing this option with external terminating resistors. See Figure 7 for operating 75 Ω cable.

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7.0 Software Support

The Intel® LXT3108 LIU comes with a complete set of software support. The various software modules allow the user to:

- **Configure the device through a Graphical User Interface (GUI).** The Intel® LXT3108 LIU GUI software allows you to configure the Intel® LXT3108 LIU without having to worry about which bits to set in a particular register. Configuration of the Intel® LXT3108 LIU can be accomplished by a series of mouse clicks within the GUI. Configurations can be saved as a series of Intel® LXT3108 LIU API messages, which can be used by client applications. Additionally, the Intel® LXT3108 LIU GUI allows the user to monitor the performance of the device as well as poll the interrupts.
- **Develop customized applications using the Intel® LXT3108 LIU Application Programming Interface (API).** The Intel® LXT3108 LIU API is an open source, ANSI C standard library that allows you to develop custom applications for communicating with the device. Programming with the API improves development time by relieving the programmer of having to know the register specifics of the Intel® LXT3108 LIU. The Intel® LXT3108 LIU API complies with the Intel® IXA architecture for compatibility with other Intel® communication building blocks.
- **Fine-tune the pulse shape of the device using the Intel® Pulse Template Matching (Intel® PTM) software.** The Intel® PTM software provides a graphical view of the transmitting pulse shape (T1, J1 or E1) that the Intel® LXT3108 LIU generates. PTM allows you to adjust the pulse shape to fit its respective template, without having to manually manipulate register settings. The PTM software, through the use of graphical controls, automatically adjusts the register settings of the Intel® LXT3108 LIU. This simplifies the process of fine-tuning the pulse shape, which leads to faster development time.

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8.0 Initialization

During power up, the Power-On-Reset (POR) circuit initiates a reset sequence after the power supply reaches threshold of approximately 60% of VCC. On crossing this threshold, the device begins a 32 msec reset cycle to calibrate internal phase lock loops. During power-up, an internal reset places all registers to their default values and resets the status and state machines for LOS and AIS. MCLK is mandatory and must be present at power on for chip operation.

8.1 CLAD Initialization

It is required to initialize the CLAD register (Addr : 0x11) after power on reset, based on the frequency of the MCLK input signal. The following table can be used for programming the CLAD register (refer to Table 21, “CLAD Configuration Register1, 11h” on page 71).

Table 2. CLAD Initialization Options

MCLK Input[1]	Value to be written to CLAD (Addr : 0x11) after power on reset.
8x E1 clock	80
4x E1 clock	88
2x E1 clock	84
1x E1 clock	8c
8x T1 clock	90
4x T1 clock	98
2x T1 clock	94
1x T1 clock	9c
1. E1 clock is 2.048 MHz and T1 clock is 1.544 MHz.	

8.2 Reset Operation

The Intel® LXT3108 LIU can be reset in two ways:

1) Writing to the reset bit as shown in the “Port Page Select Register, CPS, 00h” on page 70. This soft reset initiates a 32 msec reset cycle. The user should not access the internal registers during the reset cycle (register values are undefined). The reset bit does not initialize the CLAD Configuration Register1, 11h on page 71.

2) Asserting the reset pin $\overline{\text{RSTB}}$ low. The reset pulse width must be a minimum of 1 msec. It is recommended to wait for another 32 msec after the reset pulse is de-asserted before performing any read/write access to the port registers. The operation sets all LXT3108 registers to their default values, including the CLAD Configuration Register1, 11h on page 71.

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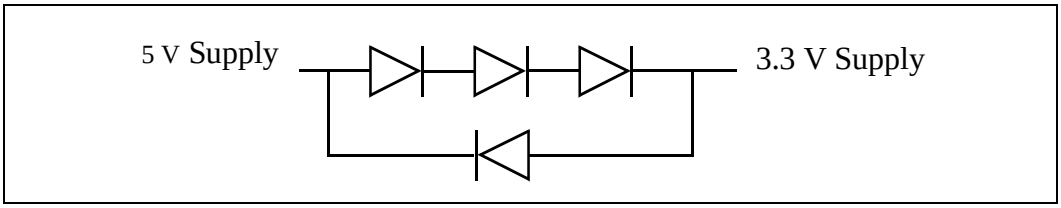
9.0 Power Supply Requirements

9.1 5 V Tolerant I/O Pins

All digital input pins will tolerate 5.0 volts and are compatible with TTL logic. Please note that it is recommended to keep digital input pins less than 2 volts above the analog and digital supplies. The 5.0 V-tolerance of the Intel® LXT3108 LIU is only applicable when the 3.3 V (nominal) supplies are present.

Note: External devices such as pull-up resistors, TTL logic, microprocessors, and system-bus peripherals are potential sources of 5 V signals to the digital pins. Power-cycling and power-supply failure can potentially cause situations where the Intel® LXT3108 LIU is powered down, while external 5 V devices are powered up. When the power supply is not guaranteed to prevent this situation, a diode network can be used as shown in Figure 8. The diodes must be capable of handling the entire load capacity of either the 3.3 V or 5 V supply, whichever is greater.

Figure 8. Diode Protection Network When Inputs Power Up Before Supplies



In the event that the 5 V supply fails, it be will held up to around 2.6 V by the 3.3 V supply. In the event that the 3.3 V supply fails, it will be held up to around 2.9 V by the 5 V supply. Each of these conditions is safe for the 5 V tolerant pins.

9.2 Layout Considerations

This section identifies recommended practice for layout and decoupling of power and ground planes.

Long-term reliability of this device might be compromised when these guidelines are not followed.

9.2.1 Ground Plane

All ground pins should be connected to a solid ground plane with the shortest possible path to minimize inductive effects. All pins with names containing GND, VSS, or SUB are ground pins. The VMOAT pin should also be connected to the ground plane.

9.2.2 Analog Power Supply

The analog supply pins listed below require a 3.3 V (nominal) supply, which should be filtered separately from the digital supply:

— TXVCC

- TVCC
- AVCC
- QVCC

The recommended method is to connect all of the analog pins to a wide PCB trace, and connect one end of the PCB trace to the power plane. Bypass capacitors from the ground plane to the analog supply trace should be placed as close as possible to the following pins:

- A 0.082 µF capacitor between each TXVCC pin and ground.
- A 0.082 µF capacitor between each AVCC pin and ground.
- A 0.082 µF capacitor between each DVCC pin and ground.

It is recommended that analog and digital power comes from the same power supply. To prevent excessive current through the device, due to one of the supplies failing or sequential power-cycling, it is suggested that the supplies be connected back to the same point.

9.2.3 Digital Power Supply

Digital power supply pins, I/O power, and DVCC should be connected to a solid power plane with the shortest possible path. Four 0.01 µF bypass capacitors, one per side, should be placed as close as possible to the Intel® LXT3108 LIU to filter the ground and power planes of the circuit board. In addition, the circuit board should contain 10 µF tantalum and 0.01 µF ceramic capacitors where power is supplied to the board.

As with the analog power supply, it is recommended that analog and digital power come from the same power supply. To prevent excessive current through the device, due to one of the supplies failing or sequential power-cycling, it is suggested that the supplies be connected back to the same point.

10.0 Transmitter

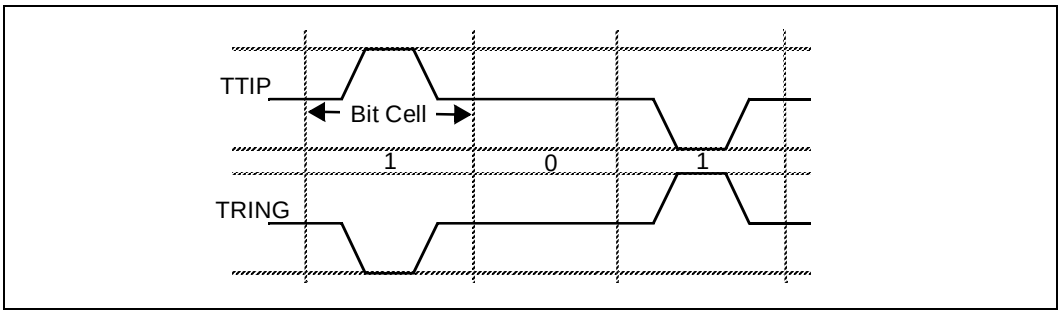
Each of the eight ports' transmitters offers several features when interfacing with the framer device's port transmitter control signals TCLK and TDATA or TPOS/TNEG. With TCLK clocking at the line rate and TDATA or TPOS/TNEG carrying digital traffic, the line driver will output a T1/E1/J1 signal through a center tapped 1:1 transformer to the transmit cable pair.

The eight low power transmitters of the Intel® LXT3108 LIU are identical. Along with fourteen pre-programmed pulse shapes shown in Table 25, "Transmit Control Page Register, 03h" on page 74, the designer may choose the PTM software to tailor pulse shapes to the application. The PTM implements 48 8-bit registers described in Table 44, "Transmit Coefficient Page Register Range, 40h-6Fh" on page 80 that customizes the AMI transmit waveform. The user must assert bit zero, ATWG_EN, of Transmit Control Page Register, 03h on page 74, to enable this feature.

The analog current driver uses programmable internal resistive feedback to synthesize an output impedance of either 100, 110 or 120 Ω for twisted-pair applications. The impedance is programmable through the port page register in Table 27, "Termination Control Page Register, 05h" on page 75. When TCLK is not supplied, the transmitter remains powered down and the TTIP/TRING outputs are held in a high impedance state. All eight transmitters can be simultaneously tri-stated by setting the OE pin low. Also, the programmer can set the port's output enable control bit to individually tri-state port transmitters as shown in "Transmit Control Page Register, 03h" on page 74. Please refer to Section 10.2.1, "Transmit Idle Operation and Tri-stating Drivers" on page 48 for details.

Transmit data is clocked serially into the device at TPOS/TNEG in the bipolar mode or at TDATA in the unipolar mode. The transmit clock (TCLK) supplies the input synchronization. Unipolar I/O is selected by setting the appropriate bits as described in Table 38, "Line Coding Control One Page Register, 1Ch" on page 78. The transmitter samples TPOS/TNEG or TDATA inputs on the falling edge of TCLK. Refer to the Test Specifications Section, Table 55, "Master and Transmit Clock Timing Characteristics" on page 91, for MCLK and TCLK timing characteristics.

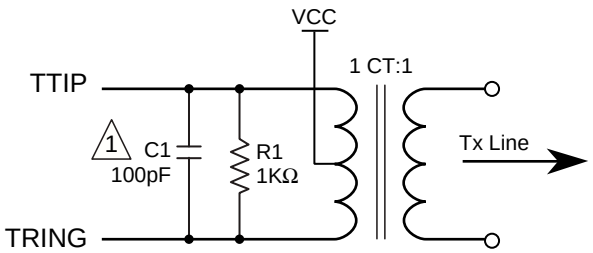
Figure 9. 50% AMI Encoding



10.1 Transmit Line Interface

Each of the eight transmitters has pre-programmed and preset pulse shapes suited for driving T1 and E1 twisted-pair cables in LH or SH applications. The signal from TTIP and TRING of each port is coupled to a 1:1 center-tapped transformer as shown in Figure 10.

Figure 10. Typical Transmitter Interface Connections



NOTE:
1. Actual values of R1 and C1 may vary depending on design.

The 1:1 center-tapped transformer is readily available in many packages as specified below.

Table 3. Transformer Specifications for the Intel® LXT3108 LIU

Tx/Rx	Frequency MHz	Turns Ratio	Primary Inductance µH (minimum)	Leakage Inductance µH (max)	Interwinding Capacitance pF (max)	DCR Ω (maximum)	Dielectric[1] Breakdown V (minimum)
Tx	1.544/2.048	1 CT:1	600	0.80	60	0.70 pri 1.20 sec	1500 V_{RMS}[2]
Rx	1.544/2.048	1:1	600	1.10	60	1.10 pri 1.10 sec	1500 V_{RMS}[2]

1. Some ETSI applications may require a 2.3 kV dielectric breakdown voltage.
2. Some applications require transformers with center tap on the line side of the transformer (LH applications with DC current in the E1/T1 loop).

The programmer can control the following from the Port Page Register Bank:

- Matching line impedance of the transmitter in "Termination Control Page Register, 05h" on page 75.
- LH or SH pulse shape "Transmit Control Page Register, 03h" on page 74.
- T1 or E1 port line clock rate "Port Master Control Page Register, 01h" on page 73.

10.1.1 Transmit Impedance Termination

The Intel® LXT3108 LIU's LIU transmitter will synthesize its output impedance to match either a 100 Ω, a 110 Ω, or a 120 Ω line as set by the TXTERM bits in "Termination Control Page Register, 05h" on page 75.

For 75 Ω E1 coax applications, set the termination to 120 Ω and use a 1 CT: 0.8 transformer. Refer to Figure 7.

Preset pulse shaping controls the transmit pulse equalization to determine the transmitted pulse shape as shown in Table 25, "Transmit Control Page Register, 03h" on page 74. Table 4 provides more detail about the settings. In order for the port to accurately produce the desired pulse, software must:

- Set T1 or E1 line clock rate in Port Master Control Page Register, 01h.
- Set transmit line termination in Termination Control Page Register, 05h.
- Load preset pulse shape setting in Transmit Control Page Register, 03h.

Table 4. Preset Pulse Shaping Settings and Conditions

T1/E1/J1	TCLK Frequency, MHz	Register Bits 3-0 hex	Cable Range in Feet or Line Build Out, LBO	Cable Impedance, W	Cable Attenuation, dB
DSX1	1.544	00	• 0 to 133	100	0 to 0.6
DSX1	1.544	01	• 133 to 266	100	0.6 to 1.2
DSX1	1.544	02	• 266 to 399	100	1.2 to 1.8
DSX1	1.544	03	• 399 to 533	100	1.8 to 2.4
DSX1	1.544	04	• 533 to 655	100	2.4 to 3.0
DS1	1.544	05	• 0dB LBO	100	0 to 36
DS1	1.544	06	• -7.5dB LBO	100	0 to 28.5
DS1	1.544	07	• -15dB LBO	100	0 to 21
DS1	1.544	08	• -22.5dB LBO	100	0 to 13.5
E1	2.048	09	• 0 to 655	75	0 to 3.0
E1	2.048	0A	• 0 to 655	120	0 to 3.0
E1	2.048	0B	• up to 2.5 km	75	0 to 43
E1	2.048	0C	• up to 2.5 km	120	0 to 43
J1	1.544	0D	• 0 - 655 ft.	110	0 to 3.0

10.1.2 Transmit Return Loss Performance

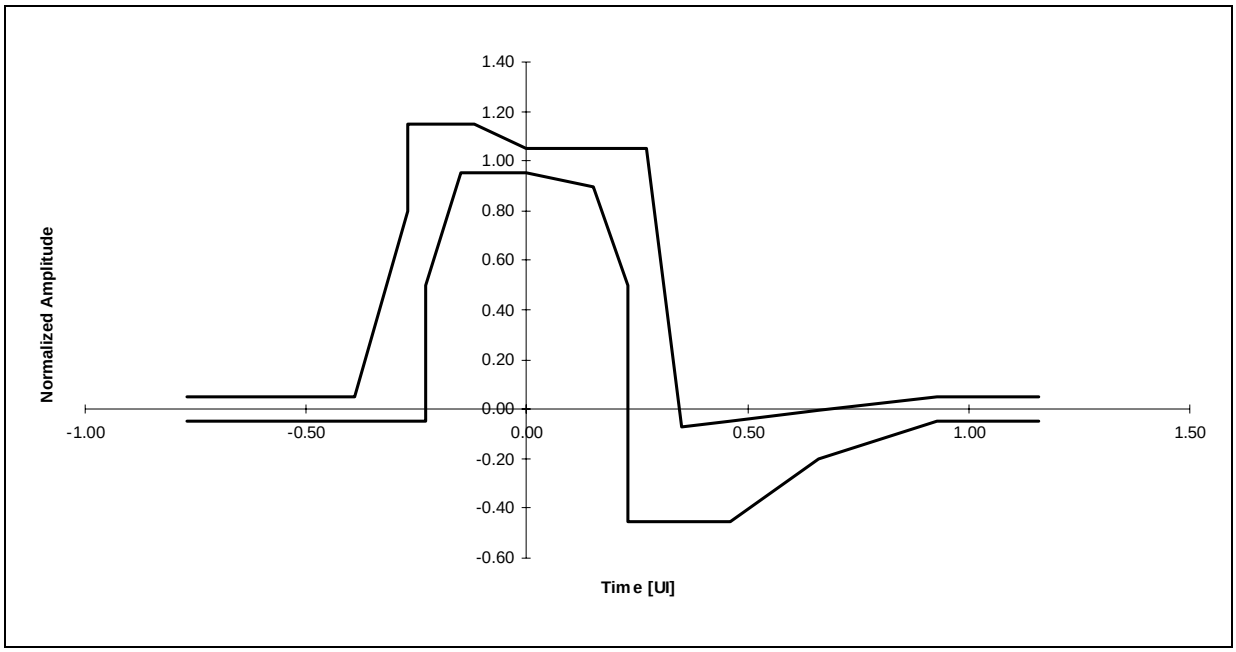
The Intel® LXT3108 LIU transmitter will meet the applicable standard for transmit return loss, but there are several requirements. Because transmit return loss depends on the match between transmitter circuit output impedance and the characteristic cable impedance, ITU limits the reflections due to mismatch by specifying minimum transmit return loss. ANSI currently does not specify this parameter. In order to compare T1 performance to E1 performance, the ITU standard is adapted to show a similar T1 minimum return loss. This is a benchmark that might be suitable for some T1 applications.

By appropriate software control of the internal transmit impedance in Termination Control Page Register, 05h, the transmit return loss will be maximized. There are three standards that can be checked for minimum transmit return loss. For E1 line rate, ITU G.703 recommends ETSI 300166. For T1 line rate, 0 dB is the de facto standard; however, ETSI 300166 can be adapted to 1.544 MHz, as shown in Table 5.

Table 5. Transmit Return Loss Specifications for Frequency Range and Magnitude

T1/E1	Frequency Band	Transmit Return Loss		
		Actual Performance (in dB)	ETS 300 166	Notes
E1	51-102 KHz	16	6 dB	ITU G.703 specification Test with 2^{15}-1 pattern
	102-2048 KHz	9	8 dB	
	2048 - 3072 KHz	9	8 dB	
T1	39-77 KHz	15	6 dB	Test with QRSS pattern.
	77-1544 KHz	12	8 dB	
	1544 - 2316 KHz	9	8 dB	

Figure 11. T1, T1.102 Mask Templates



10.1.2.1 Intel® Pulse Template Matching (Intel® PTM)

Each transmit baud, or UI, is divided into either 16 (E1) or 15 (T1) sub-phases. The pulse amplitude during each phase is described by an 8 bit, 2's complement, byte. Thus, each pulse can be described with a timing resolution of T/16 and an amplitude resolution of Full Scale/128. Up to

48 transmit bytes can be used, allowing each shaped pulse to extend up to three baud. Typically SH pulses use only 15 or 16 bytes, although all 48 bytes are available. LH pulse shaping may extend up to three baud.

To use the PTM, two operations must take place.

- The desired 8-bit bytes must be loaded into the Intel® LXT3108 LIU's local memory. This can be done through a host API. The coding is 2's complement from +127 to -127 where a code of +127 creates a full scale pulse at the output. Each LSB is approximately 1/127 of FS. Care must be taken by the users, as it is possible to create invalid pulse shapes either by mis-coding or by saturating the DAC.
- After the bytes are loaded, assert ATWG_EN by loading value "01h" as shown in "Transmit Control Page Register, 03h" on page 74.

These settings are maintained as long as power is applied to the device and reset is not asserted. They can be overwritten at any time and are not lost when the transmitter is powered-down as shown in Figure 13 on page 48. The contents of the local memory are lost when power is removed from the chip and initialized to all zeros when reset is asserted.

Note: The user must be careful not to assert ATWG_EN when the contents of the local memory have not been properly initialized.

Adjustments to the output signal can be made using the Intel® PTM® software. The Intel® PTM® software simplifies the process of modifying the output signal by handling all of the register manipulation for you.

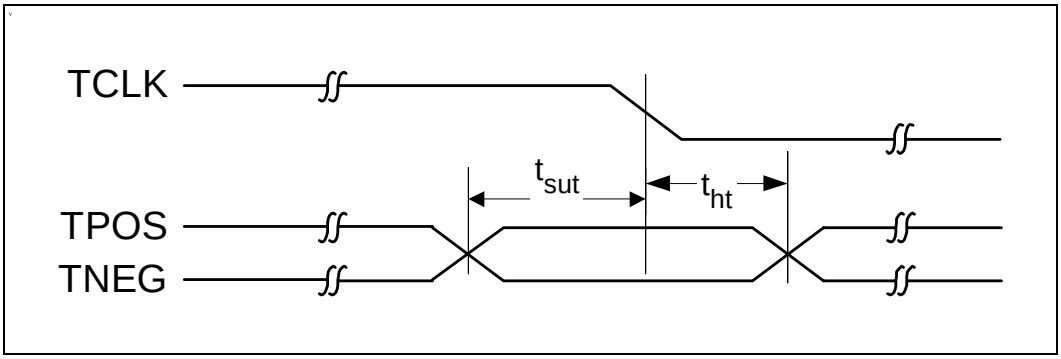
10.2 Transmit Digital Interface

Input data for transmission onto the line is clocked serially into the device at the TCLK rate. TPOS and TNEG are the bipolar data inputs, and TDATA accepts unipolar data. Software controls how input data passes through:

- The jitter attenuator, according to "JA Control Two Page Register, 1Dh" on page 79.
- The B8ZS/HD3 encoder, according to "Line Coding Control One Page Register, 1Ch" on page 78.

Data is clocked on the falling edge of TCLK as shown in Figure 12, "Transmit Interface Timing" on page 47.

Figure 12. Transmit Interface Timing



10.2.1 Transmit Idle Operation and Tri-stating Drivers

When the transmitter is not being used, the designer conserves power by powering down the driver circuit. There are two ways to power down the transmitter:

- Set bit five, Transmit Clock Detect Enable in the Transmit Control Register 03h to 0 and hold TCLK input High for 16 clock cycles.
- Assert the TXPD bit in "Port Master Control Page Register, 01h" on page 73, in software.

In this state, TTIP and TRING are at high impedance, and all of the analog circuitry associated with the transmitter is turned off. After restarting TCLK or clearing the TXPD bit, it may take several milliseconds for the transmitter to achieve steady state performance.

For redundancy applications, it is desirable to tri-state each driver while leaving the transmitter circuitry turned on. In this case, there are three ways to tri-state the drivers:

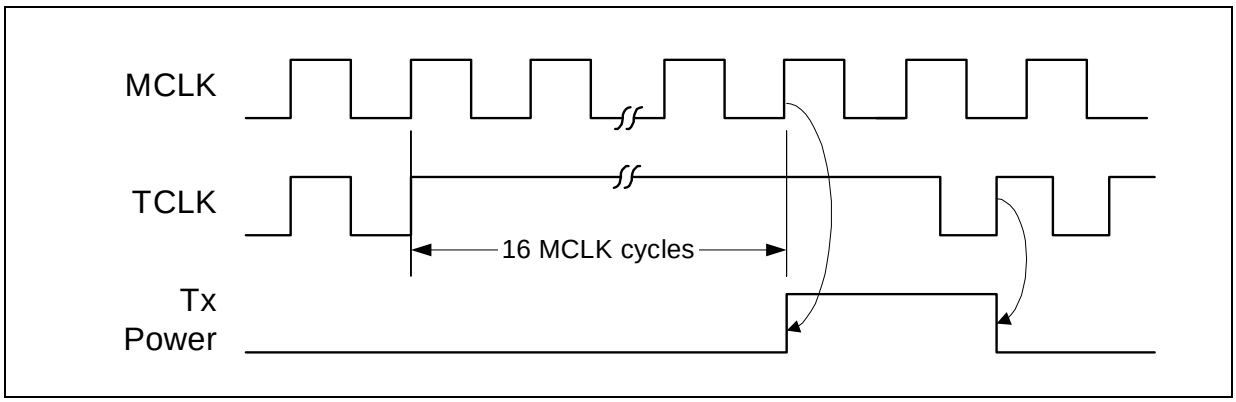
- Set the OE pin low, which affects all eight ports at the same time.
- Set the OES bit high in "Transmit Control Page Register, 03h" on page 74.

In this state, TTIP and TRING will enter a high impedance state. However, in this state the transmitter will remain powered up. This will allow two transmitters to be connected in parallel for redundancy applications.

Table 6. Powering Down the Transmitter with Static TCLK

TXCLK	Effect
TXCLK = 1 > 16 MCLK cycles OR TXPD = 1	Transmitter enters Powered-down State. TTIP & TRING enter high_impedence state.
TXCLK = 0 > 16 MCLK cycles	TTIP & TRING enter high-impedance state.

Figure 13. TCLK Power Down Timing



11.0 Receiver

The eight receivers in the Intel® LXT3108 LIU are identical and operate independently. The following paragraphs describe the operation of one receiver.

The receiver is coupled to the line through a 1:1 transformer. The input common mode level is set on-chip. Recovered data is presented at the port's RPOS/RNEG or RDATA pins. The recovered clock is present at the port's RCLK pin. Upon loss of signal, RCLK is derived from MCLK. Refer to the test specification section for receiver timing.

11.1 Master Reference Clock

The MCLK input to the Intel® LXT3108 LIU requires Master Clock (MCLK) for operation. This clock is used by the on-chip Clock Adapter (CLAD). The MCLK can be one of the following: 1x, 2x, 4x, 8x (T1 or E1). The Intel® LXT3108 LIU requires only one clock (e.g., 2.408 MHz) for all modes (T1/E1/J1). The on-chip CLAD configuration is specified in CLAD_CONFIG1 register in Table 21.

The data and timing recovery circuits provide input jitter tolerance significantly better than is required by AT&T Pub 62411 and ITU G.823. See the Test Specifications section Table 48 to Table 58 and Figure 25 to 31 for more information.

11.2 Receiver Digital Interface

The recovered data goes to the Loss of Signal (LOS) Monitor, and through the Alarm Indication Signal (AIS, Blue Alarm) Monitor. Received data may go through either the B8ZS or HDB3 decoder or neither. Finally, the data is sent to the framer either as unipolar or bipolar data on the RDATA or RPOS/RNEG pins, and the recovered clock drives the RCLK pin. Received data is clocked out of the LIU on the active edge of RCLK. The user can specify either the rising or falling edge of RCLK for clocking out data on RDATA or RPOS/RNEG. The receiver LOS function monitors the received signal level and indicates when the signal drops below the levels given in Table 7. In the unipolar mode, the RNEG output indicates received BPV. BPVs are also counted in the internal BPV counter when BPV count is enabled. Refer to "Monitoring BPV and EXZ Line Coding Violations" on page 64.

11.2.1 Receiver Idle Conditions

The receiver is powered down under either of the following conditions:

- When the RXPD bit described in "Port Master Control Page Register, 01h" on page 73 is set.
- When the CHANEN bit described in "Port Receiver Enable Page Register, 02h" on page 73 is set. This bit also powers down the transmitter when set.

In the powered down condition, the RPOS, RNEG, and RDATA are not defined. The RCLK signal stays at 1.544 MHz when the LIU port is configured in T1 or J1 mode. The RCLK signal stays at 2.048 MHz when the LIU port is configured in E1 mode.

11.3 Receiver Line Interface

The Intel® LXT3108 LIU receiver line interface provides:

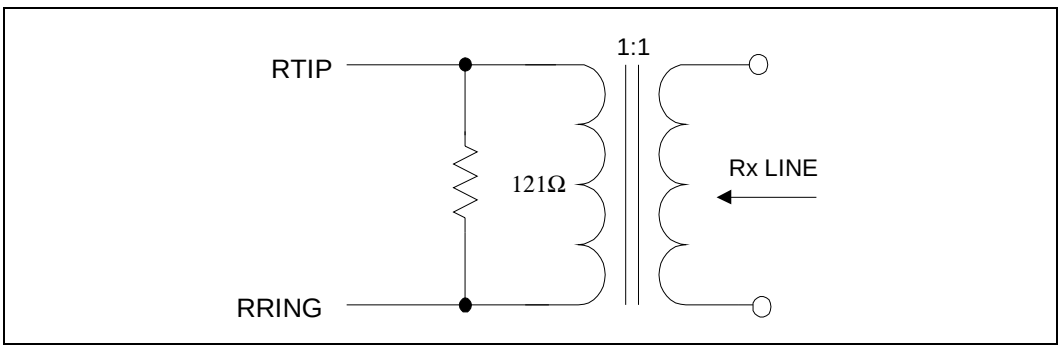
- Programmable line termination described in "Termination Control Page Register, 05h" on page 75.
- Programmable sensitivity described in "Receive Control Page Register, 04h" on page 74.
- Monitor mode, also in Receive Control Page Register, 04h.

The Intel® LXT3108 LIU internally terminates the input line for twisted pair applications with a combination of a single external resistor and programming the termination register to match the line impedance. An advanced DSP- based receiver provides equalization and timing recovery for signals with up to -43 dB of cable loss (E1) or -36 dB of cable loss (T1) in the presence of input noise and jitter as specified in ANSI T1.408. The receiver provides up to -43 dB of sensitivity @ 1024 KHz (E1) or up to 36 dB of sensitivity @ 772 KHz (T1) in steps of approximately 2 db under software control as described in Receive Control Page Register, 04h. The advantage these features provide is industry standard performance without component changes.

11.3.1 Receive Termination Impedance

The receiver is coupled to the line through a 1:1 transformer. In E1 mode, the receiver input impedance is high (above 10 KΩ).

Figure 14. Typical Receiver Interface



For E1 120 Ω, the receiver termination is set by the parallel combination of a precision 121 Ω ± 1% external resistor and the internal impedance. Figure 14 shows a typical receiver interface. The total input impedance can be set by the user by setting the appropriate bits in register RXTERM, address 05h, in the page registers. For T1 100 Ω, the internal resistor value is 580 Ω ± 5%. For J1 110 Ω, the internal resistor value is 1200 Ω ± 5%. For E1 120 Ω, the internal resistance has a value of 10 KΩ or higher.

11.3.2 Receiver Sensitivity Programming

Under some conditions it may be desirable to limit the sensitivity of the receiver. This can be done by programing "Receive Control Page Register, 04h" on page 74. This limits the range of the receiver equalizer to the approximate values shown in Table 7. The designer selects the affected port as described in the "Port Page Select Register, CPS, 00h" on page 70 for all ports simultaneously or for each port individually.

Table 7. Programming Receiver Sensitivity

RXCON RX[4:0] hex	T1/E1	Maximum receiver sensitivity (dB)	T1/E1	Maximum receiver sensitivity (dB)
00	E1	-43	T1	-36
01		-40		-34
02		-38		-32
03		-36		-30
04		-34		-28
05		-32		-26
06		-30		-24
07		-28		-22
08		-26		-20
09		-24		-18
0A		-22		-16
0B		-20		-14
0C		-18		-12
0D		-16		-10
0E		-14		-8
0F		-12		-6
10		-10		-4
11		-8		-2
12		-6		0
13		-4		-36
14		2		-36
15 - 1F		-43		-36

11.3.2.1 Receiver Monitor Mode

The receive equalizer of the Intel® LXT3108 LIU can be used in Monitor Mode applications. Monitor Mode applications require a resistive attenuation of the signal in addition to a small amount of cable attenuation (less than 6 dB). Asserting the MON bit in "Receive Control Page Register, 04h" on page 74 configures the device to work in its Monitor Mode. The device must be in its LH receiver mode for Monitor Mode which, is controlled by the RXSH bit in Receive Control Page Register, 04h.

With the device in Monitor Mode, the receive equalizer handles signals attenuated resistively by 20 to 30 dB, plus 0 to 6 dB of cable attenuation for both E1 and T1 applications.

11.4 Receiver Status Information

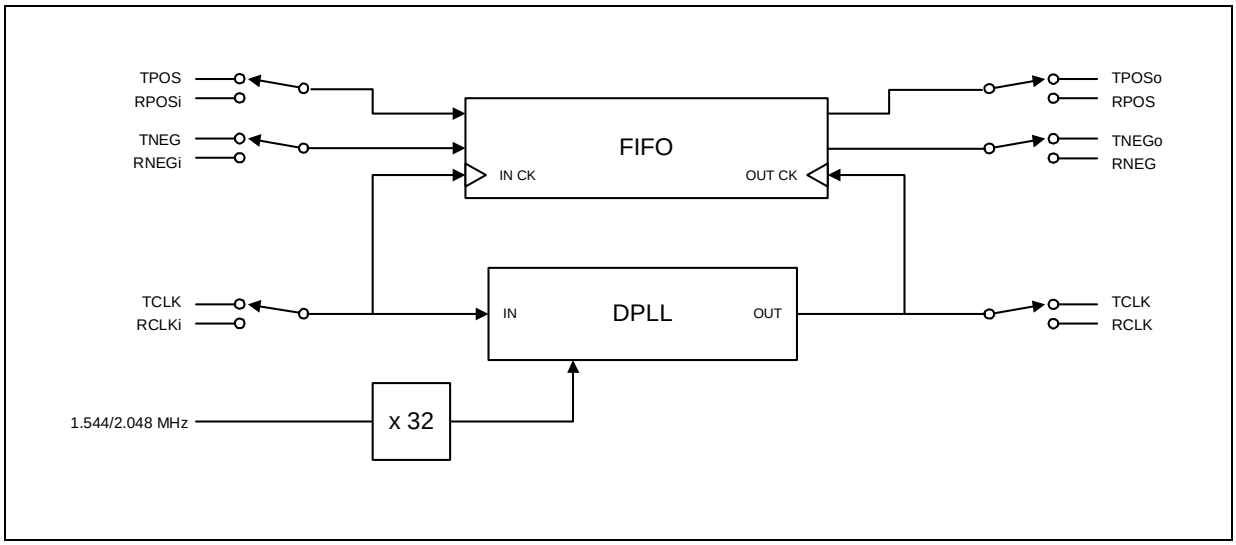
The status of the receiver can be monitored though "Receiver Equalizer Status Zero Page Register, 06h" on page 75, while equalizer settings can be checked with "Receiver Equalizer Status One Page Register, 07h" on page 75 and "Receiver Equalizer Status Two Page Register, 08h" on

page 75. Receiver Equalizer Status Two Page Register, 08h contains status bits that indicate LOS. The contents of Receiver Equalizer Status Zero Page Register, 06hand Receiver Equalizer Status One Page Register, 07h can be used to estimate the line attenuation, which can be translated to line length.

12.0 Jitter Attenuation (JA)

A digital Jitter Attenuation Loop (JAL) combined with an Elastic Store (ES) FIFO provides Jitter attenuation. The FIFO depth is selectable for either 32 or 64 bits, through "JA Control Two Page Register, 1Dh" on page 79. The JAL is internal and does not require an external crystal or a high-frequency (higher than line rate) reference clock. The JA can be placed in either the receive or transmit data path. The JA Control Two Page Register, 1Dh selects JA enabled or disabled, and selects either the receive or the transmit path.

Figure 15. Jitter Attenuation Loop



The FIFO is a 32 x 2-bit or 64 x 2-bit register (selected by the register x1D). Data is clocked into the FIFO with the associated clock signal (TCLK or RCLK) and clocked out of the FIFO with the dejittered JAL clock, as seen in Figure 15. When the FIFO is within two bits of overflowing or underflowing, the FIFO adjusts the output clock by 1/8 of a bit period. The Jitter Attenuator produces a delay of up to 16 or 32 bits in the associated path. Please refer to Test Specifications for details. This advanced digital jitter attenuator meets the latest jitter attenuation specifications shown in Table 8.

Table 8. Jitter Attenuation Specifications

T1	E1
AT&T Pub 62411	ITU-T G.736
GR-253-CORE	ETSI CTR12/13
TR-TSY-000009	

12.1 Digital Jitter Attenuator (DJA) Status

DJA status detection for both underflow and overflow conditions is reported in "Alarm Status One Page Register, 12h" on page 77. Two maskable processor interrupts for the DJA are controlled by "Interrupt Enable Page Register, 11h" on page 77. Details about both types of DJA interrupt status are reported in "Interrupt Status Two Page Register, 13h" on page 78.

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13.0 Network Control and Maintenance Functions

13.1 Diagnostic Modes

The Intel® LXT3108 LIU offers the following diagnostic modes:

- Network Loop (NLOOP) Code Generator/Detector.
- Analog loopback (ALOOP) digital transmitter to analog transmitter/receiver pins back to digital receiver pins.
- Remote loopback (RLOOP) analog receiver to analog transmitter pins.
- Digital loopback (DLOOP) digital transmitter to digital receiver pins.
- Transmit All Ones (TAOS) signal sent by transmitter driver to line.

The Intel® LXT3108 LIU offers three loopback modes for diagnostic purposes: Analog, Remote, and Digital Loopback. Network Loop codes activate Remote Loopback from a pattern contained in the signal traffic passing through the LIU receiver. Loopbacks are selected by writing to the appropriate port's ALOOP bit in "Port Master Control Page Register, 01h" on page 73, or DLOOP, NLOOP or RLOOP bits in "Loopback Enable Page Register, 10h" on page 77. The Transmit All Ones control bit is set in "Transmit Control Page Register, 03h" on page 74.

13.1.1 In-Band Network Loop Up or Down Code Generator/Detector

The LXT3108 can transmit in-band Network Loop Up or Loop Down codes. The Loop Up code is 00001. The Loop Down code is 001. A Loop Up code transmission occurs when the respective bits in the Loopback Enable Page Register, 10h on page 77, are set. A Loop Down code transmission occurs when the respective bits in the Loopback Enable Page Register, 10h on page 77 are set.

Network Loopback (NLOOP) can be initiated only when the Network Loopback detect function is enabled. Writing a "1" to the NLOOP bit in Loopback Enable Page Register, 10henables this mode.

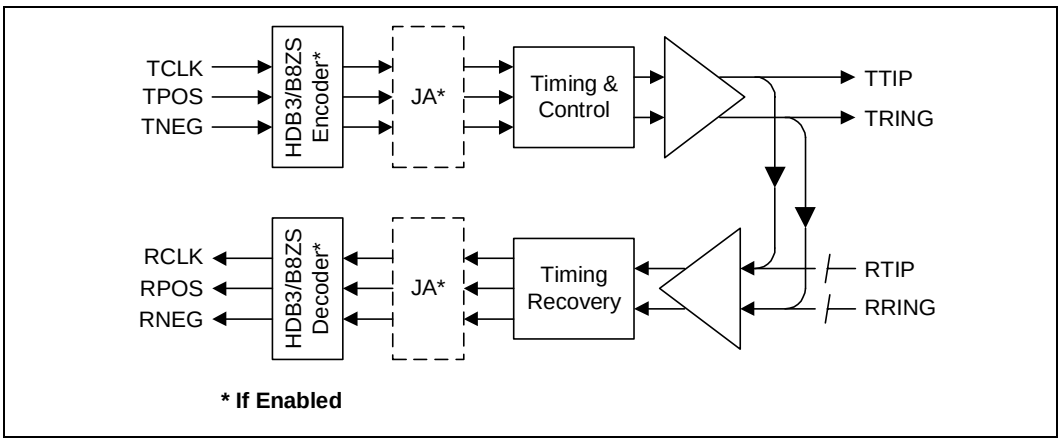
With NLOOP detection enabled, the receiver looks for the NLOOP data patterns (00001 = enable, 001 = disable) in the input data stream. When the receiver detects an NLOOP enable data pattern repeated for a minimum of five seconds, the device enables RLOOP. The device responds to both framed and unframed NLOOP patterns. Once NLOOP detection is enabled at the chip and activated by the appropriate data pattern, it is identical to Remote Loopback (RLOOP). NLOOP is disabled by receiving the 001 pattern for five seconds, or by activating RLOOP or ALOOP, or by disabling NLOOP detection in software.

13.1.2 Analog Loopback

Analog Loopback (ALOOP) exercises the maximum number of functional blocks. ALOOP operation disconnects the RTIP/RRING signal path inputs from the line and routes the transmit outputs back into the receive inputs. This tests the transmitter, receiver and timing recovery sections. The ALOOP function overrides all other loopback modes. When analog loopback is selected the receive line is still terminated by the internal termination. When selected, the transmitter outputs (TTIP & TRING) are connected internally to the receiver inputs (RTIP &

RRING) as shown in Figure 16. Data and clock are output at RCLK, RPOS & RNEG pins for the corresponding LIU. Note that signals on the RTIP & RRING pins are ignored during analog loopback. The ALOOP bit is inLoopback Enable Page Register, 10h.

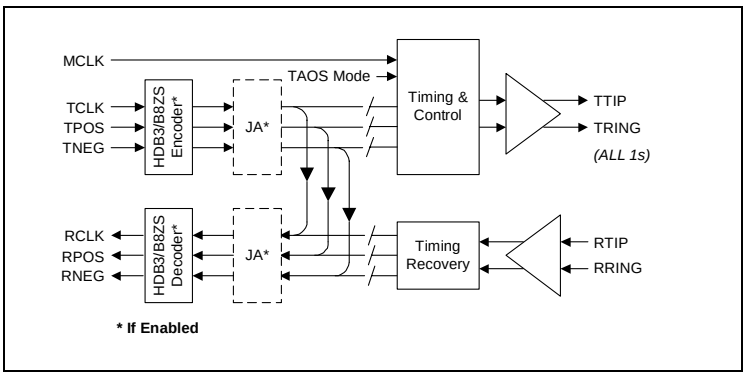
Figure 16. Analog Loopback



13.1.3 Digital Loopback

When digital loopback is selected, the transmit clock and data inputs (TCLK, TPOS & TNEG) are looped back and are output on the RCLK, RPOS and RNEG pins (see Figure 17). The data presented on TCLK, TPOS and TNEG is also output on the TTIP and TRING pins. Note that signals on the RTIP and RRING pins are ignored during digital loopback.

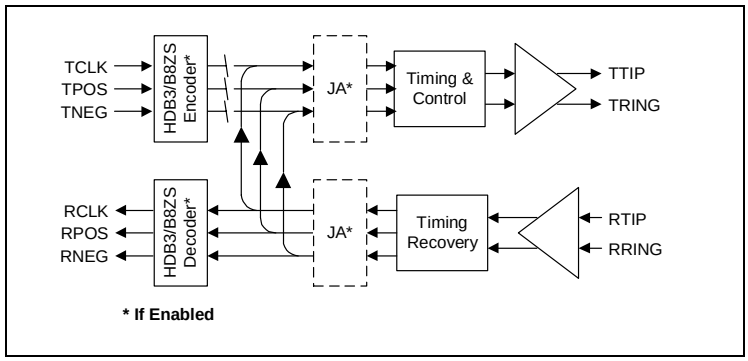
Figure 17. Digital Loopback



13.1.4 Remote Loopback

During remote loopback as shown in Figure 18, the RTIP and RRING inputs are routed to the transmit circuits and are output on the TTIP and TRING pins. Note that input signals on the TCLK, TPOS & TNEG pins are ignored during remote loopback.

Figure 18. Remote Loopback



13.1.5 Transmit All Ones (TAOS)

The TAOS mode is set by asserting the TAOS bit in Transmit Control Page Register, 03h. Note that the TAOS generator uses MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability as shown in Table 55, “Master and Transmit Clock Timing Characteristics” on page 91.

Both DLOOP and ALOOP modes function correctly with TAOS active. However, RLOOP is inhibited when TAOS mode is active.

Figure 19. TAOS Data Path

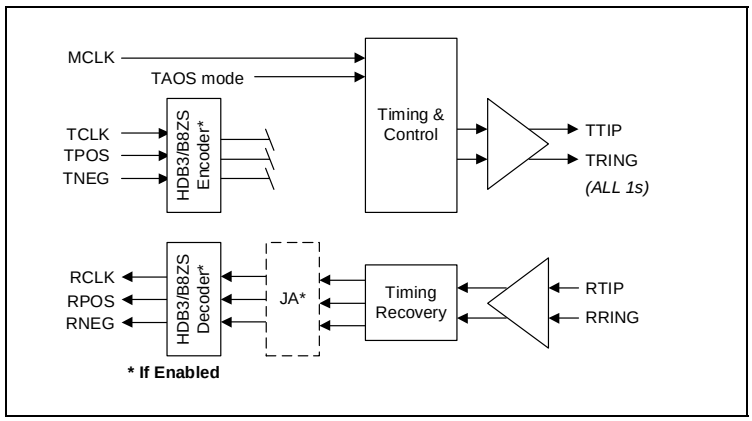


Figure 20. TAOS with Digital Loopback

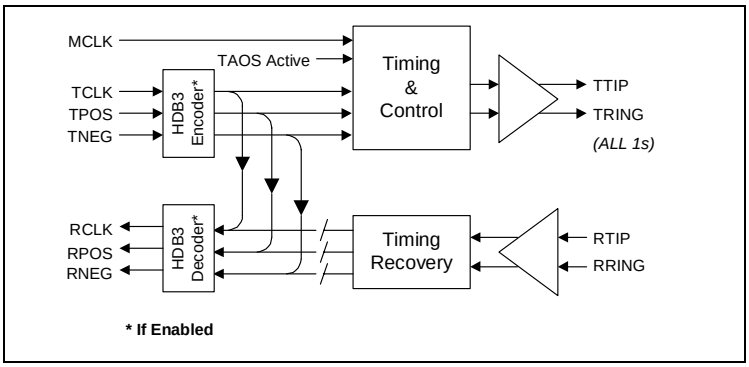
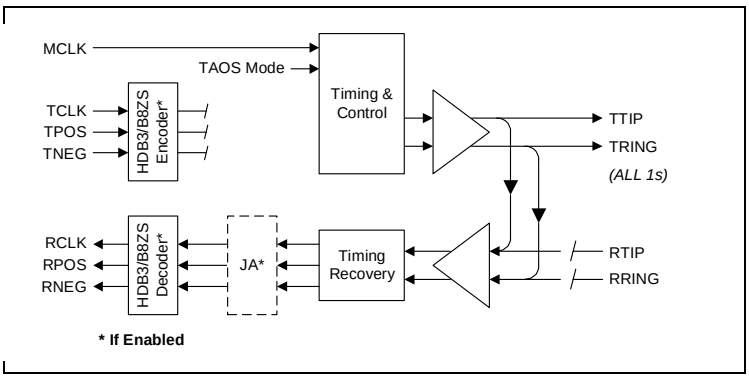


Figure 21. TAOS with Analog Loopback



13.2 Line Coding

This section describes the Intel® LXT3108 LIU functionality related to line coding and monitoring.

The LIU's digital framer interface performs two functions:

- Provides a bipolar or unipolar interface to a framer.
- Offers line coding and decoding of AMI, B8ZS and HDB3.

Each of these functions is described in detail below:

The LIU digital framer interface can be operated in one of two functional modes as described in Table 38, "Line Coding Control One Page Register, 1Ch" on page 78:

- BIPOLAR - Digital Positive/Negative/Clock signals, indicating signal polarity.
- UNIPOLAR - Digital Data/Clock, indicating NRZ data.

13.2.1 Alternate Mark Inversion (AMI)

(per: ITU G.703)

AMI is a Return-to-Zero (RZ) format where a binary “one” (mark) is represented by either a positive or negative going pulse and a binary “zero” (space) is represented by the absence of a pulse. The Intel® LXT3108 LIU supports either of the standards listed below by user selection in Table 38, “Line Coding Control One Page Register, 1Ch” on page 78 as well as Table 31, “LOS Window Page Register, 0Bh” on page 76 through Table 33 on Page 76. AMI coding alone does not provide any method of ensuring compliance to mark/space requirements. The term “AMI coding” is often used to mean that no specific methods are used to suppress excess zeroes in the signal.

— ANSI T1.403:

No more than 15 consecutive zeros.

At least N ones in each and every time window of 8*(N+1) bits, where N = 1 through 23.

— FCC Part 68.318:

No more than 80 consecutive zeroes.

An average ones density of at least 12.5%.

Each consecutive pulse should alternate in polarity (i.e., a positive pulse should always be followed by a negative pulse and a negative pulse should always be followed by a positive pulse) regardless of the number of intervening spaces between the two pulses. AMI comes from this: *alternating marks inversion.* Two consecutive pulses of the same polarity are known as a bipolar violation (BPV). The Intel® LXT3108 LIU actively monitors the line signal and provides a count of detected BPVs for performance monitoring purposes. By definition, *all* T1 line signals use basic AMI line coding. However, because T1 receivers rely on the presence of marks in the signal to recover clocking, various standards specify maximum space and minimum mark density requirements. These are cited below.

13.2.1.1 Bipolar with Eight Zero Substitution (B8ZS)

(per: ANSI T1.102)

The Intel® LXT3108 LIU allows separately controlled transmit and receive B8ZS encoding for each port at T1 line rate described in “Line Coding Control One Page Register, 1Ch” on page 78. The Intel® LXT3108 LIU performs both B8ZS coding (on the T1 transmitted signal) and B8ZS decoding (on the T1 received signal). Received BPVs that are part of the B8ZS pattern are not counted as BPVs in the coding error counter.

B8ZS overcomes limitations of ZCS discussed below and allows the support of clear port (64 kbps) data. It is compatible with all standard T1 framing formats. In B8ZS coding, eight consecutive zeroes in the T1 data stream will be replaced by the B8ZS substitution pattern of “000VB0VB” in which “V” is an intentional BiPolar Violation (BPV) and “B” is a valid bipolar mark. Note that the polarity of the BPVs and marks depends upon the polarity of the last mark before the “eighth zero” occurs. This substitution is made regardless of where the eight consecutive zeroes occur in the datastream, including framing, signaling, and alarm bits. As opposed to ZCS, which operates on data within a DS0 port, B8ZS coding can occur across frame boundaries.

13.2.1.2 High Density Bipolar Three (HDB3)

(per: ITU G.703)

The Intel® LXT3108 LIU allows separately controlled transmit and receive HDB3 encoding for each port at E1 line rates described in “Line Coding Control One Page Register, 1Ch” on page 78.

Receive side HDB3 decoding is selected by setting the decoding bit in Line Coding Control One Page Register, 1Ch. Similarly, transmit side HDB3 encoding is selected by setting the encoding bit in Line Coding Control One Page Register, 1Ch. Received BPVs that are part of the HDB3 pattern are not counted as BPVs in the coding violation error counter.

In HDB3 coding, four consecutive zeroes in the E1 data stream will be replaced by the HDB3 substitution pattern of either “000V” or “B00V, in which “V” is an intentional bipolar violation (BPV) and “B” is a valid bipolar mark. This limits the maximum number of consecutive spaces to three. The choice of substitution pattern is made so that the number of B pulses between consecutive V pulses is odd (i.e., successive V pulses are of alternate polarity). This substitution is made regardless of where the four consecutive zeroes occur in the datastream, including framing, signaling, and alarm bits. The Intel® LXT3108 LIU performs both HDB3 coding on the E1 transmitted signal and HDB3 decoding on the E1 received signal.

13.3 Network Maintenance Functions

13.3.1 Loss Of Signal (LOS)

While LOS appears at each port’s LOS pin, it can be detected by software reading the LOS bit in the “Receiver Equalizer Status Two Page Register, 08h” on page 75. A maskable processor interrupt controlled by “Interrupt Enable Page Register, 11h” on page 77 is available. Details about LOS interrupt status are reported in “Interrupt Status Two Page Register, 13h” on page 78. Depending on whether the port is configured for T1 or E1 service, the LOS will be cleared for the appropriate zeros density after the detection of LOS as discussed below.

Three user registers are provided for customizing the received marks density LOS detector. Users can select:

- The number of consecutive spaces that must be received to declare LOS in “LOS Window Page Register, 0Bh” on page 76.
- The number of marks that must be received within that window to clear LOS “LOS Set Threshold One Page Register, 0Ch” on page 76.
- The number of consecutive zeros that, when received while LOS is asserted, will continue to re-assert LOS in “LOS Reset Threshold Two Page Register, 0Dh” on page 76.

The default values are given in Table 11. Each receiver has a multi-function LOS detector that is used to meet ITU T1.231 or G.775 requirements for T1 or E1 systems.

These detectors monitor both the received signal amplitude and the received marks density according to Table 9.

Users may change these values by setting the USR_LOS bit in “Port Master Control Page Register, 01h” on page 73. When this bit is set, the desired LOS Window, LOS Set, and LOS Reset values must be programmed for proper LOS operation.

For E1 SH operation the LOS operates based on the peak received amplitude during a fixed window. For G.775 the window length can be programmed by LOS Window Page Register, 0Bh.

A minimum data density of 1 in 16 is required to clear LOS.

Table 9. LOS Criteria for Intel® LXT3108 LIU

Standard	LOS Declared	LOS Cleared
T1.231	No pulse transitions for 175 consecutive clock cycles	12.5% mark density in 175 clock cycles and less than 100 consecutive zeroes
T1 ITU I.431	More than 28dB below nominal output level, for 1544 bit periods	Less than 25dB, and 12.5% mark density in a 32-bit window, and less than 15 consecutive zeroes
E1 G.775	More than 18dB below nominal output level, for 32 bit periods	Less than 15dB, and 12.5% mark density in a 32-bit window, and less than 15 consecutive zeroes
E1 ITU I.431	More than 18dB below nominal output level, for 2048 bit periods	Less than 15dB, and 12.5% mark density in a 32-bit window, and less than 15 consecutive zeroes
E1 ETSI 300 233	More than 18dB below nominal output level, for 2048 bit periods	Less than 15dB, and 12.5% mark density in a 32-bit window, and less than 15 consecutive zeroes
E1 long haul	No pulse transitions for 175 consecutive clock cycles	12.5% mark density in a 32-bit window, and less than 15 consecutive zeroes

Table 10. LOS Register Configurations

Reg addr: 01H (master)			04H (rxcon)	LOS Criteria	Description
bit-4 usr_los	bit-3 I431	bit-0 E1/T1	bit-7 rxah		
0	0	0	x	T1.231	Marks density detection
0	1	0	x	I.431	Amplitude detection
0	0	1	1	G.775	Amplitude detection
0	1	1	x	I.431/ETSI	Amplitude detection
0	0	1	0	E1 long haul	Marks density detection
1	0	x	x	User LOS 1	Marks density detection
1	1	x	x	User LOS 2	Amplitude detection

NOTE:
1. x: don't care.

Table 11. LOS Selection Defaults

T1/E1	Window Size	Numer of Marks in Window to Clear LOS	Number of Spaces in Window to Reset the LOS Counter
T1	175	21	100
E1	32	4	16

The receiver monitor loads a digital counter at the RCLK frequency. The counter will increment each time a zero is received, and reset to zero each time a one (mark) is received. Depending on the operation mode, a certain number of consecutive zeros sets the LOS signal. The recovered clock is replaced by MCLK at the RCLK output with a minimum amount of phase errors. (MCLK is

required for receive operation.) When the LOS condition is cleared, the LOS flag is reset and another transition replaces MCLK with the recovered clock at RCLK. RPOS/RNEG will be high during the entire LOS detection period for that port.

13.3.1.1 Operation of USER LOS with Amplitude Detection

LOS will be declared when the received signal level is below the LOSSET for evaluation period of time specified in the LOS Window Page Register, 0Bh on page 76.

LOS will be cleared when the received signal is above the LOSCLR threshold. The receiver makes the decision using marks density criteria of at least 12.5% marks density in 32-bit period. This limits options for the value in the LOS Window Page Register, 0Bh on page 76 to be 04h or higher. Refer to Tables 23, 31, 32, and 33 for more details.

13.3.1.2 Operation of USER LOS with Marks Density Detection

LOS will be declared when no marks has been received during the evaluation period specified in the LOS Window Page Register, 0Bh on page 76. The value in the LOS Window Page Register, 0Bh on page 76 should be 20h or higher.

LOS will be cleared when during the LOS evaluation period, the number of consecutive zeros (spaces) is less than MAXZERO (listed in the LOS Set Threshold One Page Register, 0Ch on page 76). Refer to Tables 23, 31, 32, and 33 for more details.

13.3.2 Alarm Indication Signal (AIS)

Alarm Indication Signal reports all ones signal received at the RTIP and RRING pins. Once AIS is detected, the port status flag is set in "Alarm Status One Page Register, 12h" on page 77. A maskable processor interrupt controlled by "Interrupt Enable Page Register, 11h" on page 77 is available. Details about AIS interrupt status are reported in "Interrupt Status Two Page Register, 13h" on page 78. Depending on whether the port is configured for T1 or E1 service, the AIS will be cleared for the appropriate zeros density after the detection of AIS as shown below.

Table 12. AIS Service Condition Variations

T1/E1	Window Size	Number of Spaces in Window to Clear AIS	Maximum number of spaces within the window to declare AIS.
T1	3 msec.	9	8
E1	512-bit	3	2

(per: ETSI 300233)

E1 AIS is declared when less than three spaces (i.e., 2 or less zeroes) are detected in a 250 µsec period of data (512 bit window). This condition should be reliably detected in the presence of a 1.0E-03 Bit Error Rate (BER), implying that a framed all-ones pattern will not be mistaken as an AIS.

(per ITU G.775)

E1 AIS is detected when less than three spaces are detected in two consecutive 512-bit wide windows. The AIS is cleared when three or more zeros are detected in two consecutive 512-bit wide windows.

(per: ANSI T1.231)

T1 AIS (Blue Alarm) is declared when less than nine spaces (i.e., 8 or less zeros) are detected in a 8192-bit wide window. When AIS is detected, the appropriate bit in the AIS status register is set and a microprocessor interrupt is generated (unless masked). AIS is cleared when 9 or more zeros are detected in a 8192-bit wide window.

13.3.3 NLOOP Status

With NLOOP detection enabled in "Loopback Enable Page Register, 10h" on page 77, the receiver looks for the NLOOP data patterns (00001 = enable, 001 = disable) in the input data stream. When the receiver detects an NLOOP enable data pattern repeated for a minimum of five seconds, the device enables RLOOP and the port status flag is set in "Alarm Status One Page Register, 12h" on page 77. The device responds to both framed and unframed NLOOP patterns. NLOOP is cleared by:

- Receiving the 001 pattern for five seconds.
- Activating RLOOP in "Loopback Enable Page Register, 10h" on page 77 or ALOOP in "Port Master Control Page Register, 01h" on page 73.
- Disabling NLOOP detection in Loopback Enable Page Register, 10h.

A maskable processor interrupt for NLOOP is controlled by "Interrupt Enable Page Register, 11h" on page 77. Details about NLOOP interrupt status are reported in "Interrupt Status Two Page Register, 13h" on page 78.

13.3.3.1 T1 AMI/B8ZS BPVs

In T1 service, only one type of T1 BPV line coding violation is used:

A Bipolar Violation (BPV) is defined as any two consecutive pulses (marks) of the same polarity with AMI coded bit stream. BPVs that are part of the B8ZS zero-substitution coding will not be reported. All other BPVs are reported and counted.

The Intel® LXT3108 LIU actively monitors the line signal for this type of coding violation and increments the BPV counter for performance monitoring purposes. BPVs detected in the receive direction are also reported on RNEG/RBPV output, when the LIU is configured in the unipolar mode of operation.

13.3.3.2 E1 AMI/HDB3 BPVs

Two basic types of E1 line coding violations are defined:

1. ITU G.703 - A BiPolar Violation (BPV) is defined as any two consecutive pulses (marks) of the same polarity with AMI coded bit stream.
2. ITU O.161- An HDB3 coding violation is defined as the occurrence of two consecutive BPVs of the same polarity that are not part of the HDB3 zero substitution coding.

The Intel® LXT3108 LIU actively monitors the line signal for both types coding violations and increments the BPV counter for performance monitoring purposes. Receive BPVs are also reported on the RNEG/RBPV output, when the LIU operates in unipolar mode.

13.3.3.3 Excess Zeroes (EXZ)

The definition of an EXZ depends upon the line coding format, as explained in Table 13. The line signal is monitored for any violations of the maximum space rule as set in "Line Coding Control One Page Register, 1Ch" on page 78. When selected, EXZ occurrences increment the BPV counter for performance monitoring purposes.

Table 13. Excess Zero (EXZ) Definitions

Coding Method	EXZ Definition (ANSI)	EXZ Definition (FCC)
AMI	Any string greater than 15 consecutive zeroes	Any string with greater than 80 consecutive zeroes
HDB3	Any string greater than 3 consecutive zeroes	Any string with greater than 3 consecutive zeroes
B8ZS	Any string greater than 8 consecutive zeroes	Any string with greater than 8 consecutive zeroes

13.3.4 Monitoring BPV and EXZ Line Coding Violations

BPV and EXZ line coding violations are reported on signal traffic received at RTIP and RRING pins. Once a BPV or EXZ condition is detected, the port status flag is set in "Alarm Status One Page Register, 12h" on page 77. The Intel® LXT3108 LIU has two registers that form a 16-bit counter for each port to monitor BPVs and excess zeroes. The counter mode is set by bits 7 through 5 in Line Coding Control One Page Register, 1Ch. The counter can be enabled to count both BPVs and excess zeroes or, for troubleshooting purposes, to count either BPVs or Excess Zeroes only. These counters, BPV Counter High Byte Page Register, 1Eh and BPV Counter Low Byte Page Register, 1Fh, will increment when there is a valid code violation. The counter has a shadow register that is updated at one second intervals. This is done with an internal one second timer. The one second timer is based on the RCLK. Each port uses its own one second timer. The user should read the 16 bit shadow register (addr 1Eh & 1Fh) for BPV count accumulated during the previous one second time frame. The count value stored in the shadow register can be read by the host.

14.0 Host Interface

The microprocessor interface is used to relay configuration, control, status, and data information between the Intel® LXT3108 LIU and an external microprocessor or micro controller.

The microprocessor interface supports MPC860/M68360 (memory like bus), M68302 (standard Motorola bus), the i960®/i486™ processor bus. 8-bit address and data buses are supported. Non-multiplexed address and data busses are supported along with a multiplexed address and data bus mode. The user selects the processor type by tying the MPI_TYPE 1 & 2 pins appropriately. The processor interface can operate up to a bus cycle of 33 Mhz. The MPC860 requires five wait states and the i960® CPU also requires five wait states. Handshaking and automatic wait state generation are supported. The latency of processor access is fixed so the use of the wait state signal is optional.

The Intel® LXT3108 LIU provides extensive interrupt support. All interrupts are independently maskable. One interrupt output is provided.

14.1 Supported Processors and Connections

The Intel® LXT3108 LIU supports direct connection to the MPC860, M68360, M68302 (M68000* family), i486™, and i960® processors. The user selects the type of processor by tying the TYPEx pins to the appropriate GND and Vcc connections. The connections between the processor pins and the MPI_TYPE programming are defined as below.

14.1.1 MPC860

The Intel® LXT3108 LIU host interface address and data pins follow the MPC860 endian fashion. The Intel® LXT3108 LIU requires five wait states from the microprocessor in order to satisfy its internal timing.

Table 14. Interfacing the Intel® LXT3108 LIU to the MPC860 Processor

Intel® LXT3108 LIU Pin	Intel® LXT3108 LIU I/O	Mot MPC860 Pin
TYPE1 = 0	i	-
TYPE2 = 0	I	-
DB(7:0)	I/O	D(31:24)
AD(7:0)	I	A(31:24)
$\overline{CS}$	I	CS
$\overline{DS}$	I	TS
$\overline{RW}$	I	R/W#
MPI_CLK/ALE	I	CLK
$\overline{RDY}$	O	TA

14.1.2 M68302

The M68302 (or the M68000 family) is supported in this mode. Notice that DTACK is not used in this case. The user is required to generate their own internal wait states when needed. The number of wait states needed depends on the clock frequency of the microprocessor. When clock frequency of 16.67 MHz is used, no wait states are needed. When 20 MHz or 25 MHz clock is used, one wait state is needed.

Table 15. Interfacing the Intel® LXT3108 LIU to the M68302 Processor

Intel® LXT3108 LIU Pin	Intel® LXT3108 LIU I/O	M68302 Pin
TYPE1 = 0	I	-
TYPE2 = 1	I	-
DB(7:0)	I/O	D(7:0)
AD(7:0)	I	A(7:0)
$\overline{CS}$	I	CS
$\overline{DS}$	I	LDS
$\overline{RW}$	I	R/W#
MPI_CLK/ALE = 1	I	-

14.1.3 Intel® i960®/i486™

The Intel® i960®/i486™ family is supported in this mode. This is a synchronous bus interface with the timing being derived from the MPI_CLK input. Internally all operations will be performed on the next cycle after ADS is asserted. Five wait states are required.

Table 16. Intel® i960®/i486™ Mode

Pin	i960®/i486™
TYPE1	1
TYPE2	0
DB0	D0
DB1	D1
DB7	D7
AD0	A0
AD7	A7
CS	CS
DS	ADS
RW	W/R#
MPI_CLK	CLKO1
RDY	READY

14.2 Interrupts

There are four interrupt sources:

1. Status change in the Loss of Signal (LOS) bit of Receiver Equalizer Status Two Page Register, 08h. The Intel® LXT3108 LIU's analog/digital LOS processor continuously monitors the receiver signal and updates the specific LOS status bit to indicate presence or absence of a LOS condition.
2. Status change in the AIS (Alarm Indication Signal) bit of Alarm Status One Page Register, 12h. The Intel® LXT3108 LIU's receiver monitors the incoming data stream and updates the specific AIS status bit to indicate presence or absence of an AIS condition.
3. Status change in NLOOP (Network Loop Code) bit of Alarm Status One Page Register, 12h.
4. Elastic Store overflow or underflow (DJA overflow or underflow) bits of Alarm Status One Page Register, 12h. The Intel® LXT3108 LIU jitter attenuator updates these based on DJA response to jitter on incoming signal.

14.2.1 Interrupt Enabling

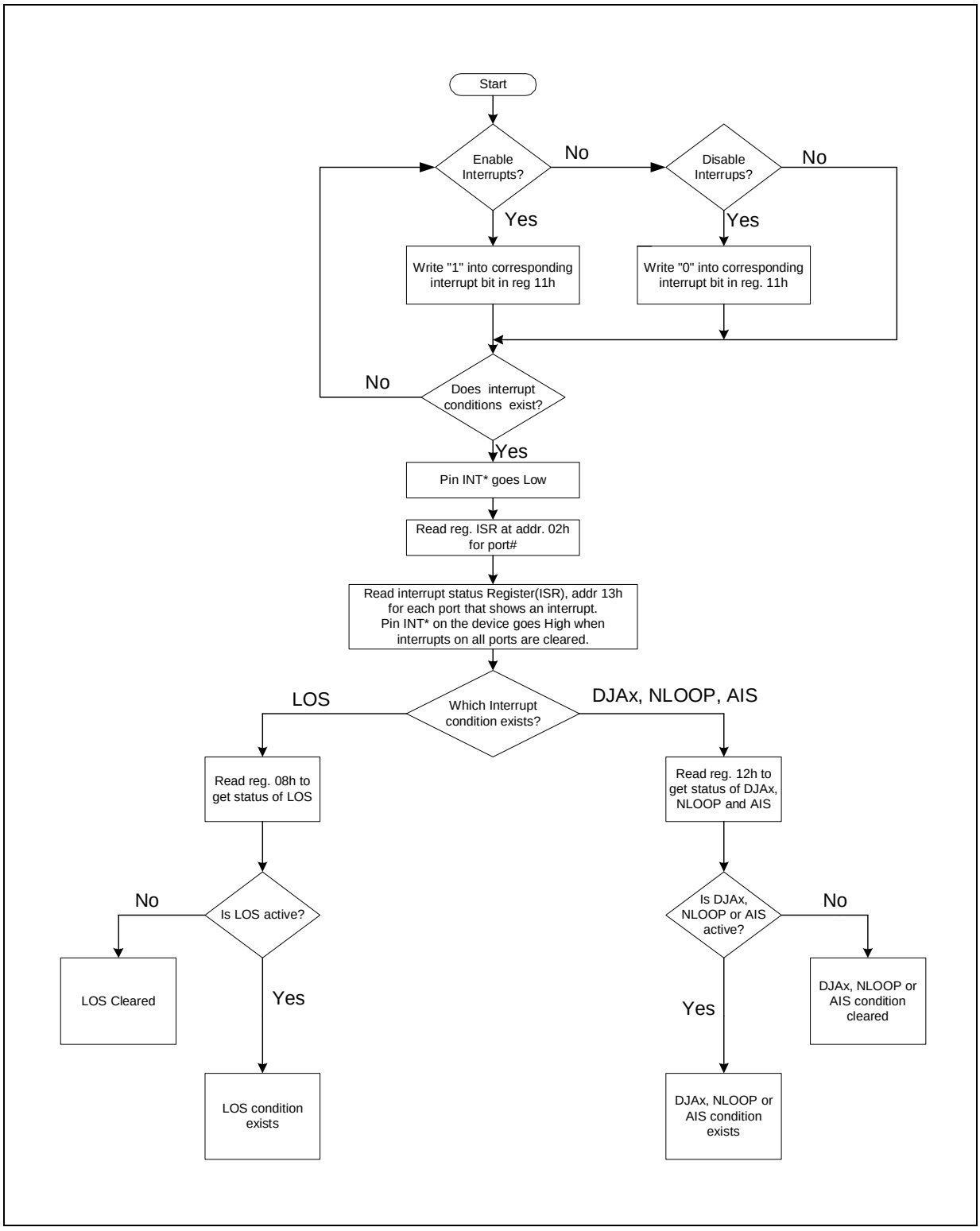
The Intel® LXT3108 LIU provides a latched interrupt output ($\overline{\text{INT}}$). An interrupt occurs any time there is a transition on any enabled bit in the status register. Writing a logic "1" into the enable register will enable the respective bit in the respective Interrupt status register to generate an interrupt. The power-on default value is all zeroes. The setting of the interrupt enable bit does not affect the operation of the status registers.

When there is a transition on any enabled bit in a status register, the associated bit of the interrupt status register is set and an interrupt is generated (when one is not already pending). When an interrupt occurs, the $\overline{\text{INT}}$ pin is asserted Low. The output stage of the $\overline{\text{INT}}$ pin consists only of a pull-down device.

14.2.2 Interrupt Clearing

There are three status registers: LOS (08h), AIS(12h), and NLOOP (12h). Reading either status register will clear the corresponding interrupts with the rising edge of the read or data strobe. When there are no pending interrupts left $\overline{\text{INT}}$ pin will go back high. Refer to Figure 22, "Interrupt Processing FlowChart" on page 68 for details.

Figure 22. Interrupt Processing FlowChart



15.0 Register Definitions

Since the Intel® LXT3108 LIU has both global registers and Page Port Registers (PPRs), the first subsection covers the global registers and the second subsection covers the PPRs. The global registers control parameters affecting operation for the entire device. One set of PPR registers controls parameters affecting operation for a single port. Of the nine sets of PPR registers, there is one for each of the eight ports and there is an additional set that controls all eight ports at the same time.

Because global registers are programmed differently than PPRs, this section describes the differences:

- Access a global register by reading or writing directly to the global register address. This is a single operation to read or write a global register. The CPS register must be set to 00h first.
- Access PPRs by writing to a global register, Port Page Select (PPS) at address 00h, with the selected port number. Immediately following this action, access the PPR for the selected port by reading or writing to the chosen PPR address. This is a double operation, one write access to the PPS with the port number followed by a single read or write to a PPR.

15.1 Global Registers

This subsection is organized with a summary of the global registers in Table 17 followed by a descriptive listing of each global register starting at Table 18 on Page 70 and ending at Table 44 on Page 80. Table 17 includes the global register names and addresses for the Intel® LXT3108 LIU.

Table 17. Global Register Addresses

Name	Symbol	Binary Address A7-A0	HEX Address	Mode
Port Page Select Register	CPS	00000000	00	R/W
ID Register	ID	00000001	01	R
Interrupt Port Register	ICR	00000010	02	R
CLAD Configuration Register 1	CLAD_CONFIG1	00010001	11H	R/W

Table 18. Port Page Select Register, CPS, 00h

Bit	Name	Bit	Function	
7-0	PS4-PS0		Writing to this register selects the index to the page for individual port control registers.	
		7	Soft-reset, resets all ports, and the entire device.	
		6..4	*Not used*	
		3..0	Bits 3..0	*Index/Page*
			0000	Selects Global Register Page
			0001	Selects Page 1 - control registers for Port 0
			0010	Selects Page 2 - control registers for Port 1
			0011	Selects Page 3 - control registers for Port 2
			0100	Selects Page 4 - control registers for Port 3
			0101	Selects Page 5 - control registers for Port 4
			0110	Selects Page 6 - control registers for Port 5
			0111	Selects Page 7 - control registers for Port 6
			1000	Selects Page 8 - control registers for Port 7
			1001	Selects write to all page control registers at one time.
NOTE: When CPS Register value equals 9h. Reading of port page (PPR) registers is disabled.				

Table 19. ID Register, ID, 01h

Bit	Name	Function
7-0	ID7-ID0	This register contains a unique revision code and is mask programmed.

Table 20. Interrupt Port Register, ICR, 02h

Bit	Name	Function
7-0	ICR7-ICR0	A “1” indicates that an interrupt occurred in the respective port. Bit 0 = 1, interrupt occurred on Port 0. Bit 1 = 1, interrupt occurred on Port 1. Bit 2 = 1, interrupt occurred on Port 2. Bit 3 = 1, interrupt occurred on Port 3. Bit 4 = 1, interrupt occurred on Port 4. Bit 5 = 1, interrupt occurred on Port 5. Bit 6 = 1, interrupt occurred on Port 6. Bit 7 = 1, interrupt occurred on Port 7.

Table 21. CLAD Configuration Register1, 11h

Address	Description	Name	Status	Bit	Function
11h[3]	CLAD Configuration Register 1 (CLAD_CONFIG1)	CLAD_PSRST	R/W	7	This bit initializes the CLAD. Default for this bit is “0”. It must be set to “1” for CLAD to work. In the event that a “0” is written into this bit by accident during operation, the CLAD will stop working. A hardware Reset must follow and the CLAD has to be re- initialized.
		CLAD_PWDN		6	RESERVED - write as “0”
		CLAD_CSSEL		5	RESERVED - write as “0”
		CLAD_OT1E1		4	MCLK definition bit. When set, clock applied to MCLK pin must be T1- based. When clear (default) MCLK must be E1- based
		DIV<1:0>		3:2	MCLK definition bits. Bits 4,3, and 2 define MCLK frequency 00 = 8x (T1 or E1) (default) 10 = 4x (T1 or E1) 01 = 2x (T1 or E1) 11 = 1x(T1 or E1)
		CLAD_TFB		1	RESERVED - write as “0”
		CLAD_TRST		0	RESERVED - write as “0”

NOTES:
1. Upon reset, restored default value is 00h.
2. In the event that an accidental write of 1 during normal operation into any of the RESERVED bits occurs, a hardware RESET must be applied and followed by CLAD initialization.
3. This register is not affected by the soft reset bit. The CLAD configuration register should only be written after reset operation initiated by the $\overline{\text{RSTB}}$ pin.

15.2 Port Page Register Bank (PPRB)

Each of the eight LIU ports in the Intel® LXT3108 LIU has independent register control available through its Port Page Register Bank. Reading or writing to each bank of registers is a two-step process:

- Select the port by writing the port number to the global register Port Page Select (CPS), address 00h.
- Program the selected PPRB register or read its status.

There is an additional mode where all eight ports can be set up to the identical settings by first writing to address 00h with a value of 09h.

Table 22 on Page 72 gives an overview of the PPRB structure for each port’s LIU. Each port in the Intel® LXT3108 LIU has an individual PPRB. The registers in the port bank structure are descriptively listed in the range of Table 23 on Page 73 through Table 44 on Page 80.

Table 22. Port Page Register Bank Addresses

Name	Symbol	Binary Address A7-A0	Address	Mode
Port Master Control	MASTER	0000 0001	01h	R/W
Port Receiver Enable	RENEN	0000 0010	02h	R/W
Transmit Control	TXCON	0000 0011	03h	R/W
Receiver Control	RXCON	0000 0100	04h	R/W
Termination Control	TERM	0000 0101	05h	R/W
RX Equalizer Status 0	RXSTATUS0	0000 0110	06h	R
RX Equalizer Status 1	RXSTATUS1	0000 0111	07h	R
RX Equalizer Status 2	RXSTATUS2	0000 1000	08h	R
LOS Window	LOSWINLEN	0000 1011	0Bh	R/W
LOS Set Threshold	LOSTHRES1	0000 1100	0Ch	R/W
LOS Reset Threshold	LOSTHRES2	0000 1101	0Dh	R/W
Loopback Enable Register	LER	0001 0000	10h	R/W
Interrupt Enable Register	IER	0001 0001	11h	R/W
Alarm Status Register 1	SR1	0001 0010	12h	R
Interrupt Status Register 2	SR2	0001 0011	13h	R
Control Register 1	CR1	0001 1100	1Ch	R/W
Control Register 2	CR2	0001 1101	1Dh	R/W
BPV counter High Byte	BPVCTRHB	0001 1110	1Eh	R
BPV counter Low Byte	BPVCTRLB	0001 1111	1F	R
Receiver Control Page Register	RWFCTRL	0011 1100	3Ch	R/W
Transmit Pulse Shape Coefficients	TXCOEF		40h-6Fh	R/W

Table 23. Port Master Control Page Register, 01h

Address	Description	Name	Status	Bit	Description
01h	Port Master Control	MASTER	R/W	7	*Reserved; write as "0"*
				6	TXPD, "1" powers down transmitter section
				5	RXPD, "1" powers down receiver section
				4, 3	BIt 4 Bit 3 0 1 This registers setting enables LOS criteria as defined in I.431 standard. Refer toTable 10 for more details. 1 0 This register setting enables USER LOS with Marks Density Detection (criteria for "Digital LOS"). Refer to Tables 10, 31, 32, and 33 for more details. 1 1 This register setting enables USER LOS with Amplitude Detection (criteria for "Analog LOS"). Refer to Tables 10, 31, 32, and 33 for more details. 0 0 This option must be considered in context with settings of bit 0 and register 04h. Refer to Table 10 for details.
				2	Reserved; write as "0"
				1	ALOOP, "1" enable analog loopback diagnostic mode
				0	T1E1, "0" enables T1, 1.544 MHz operation, while "1" enables E1, 2.048 MHz operation
NOTE: Upon reset, restored default value is 0h.					

Table 24. Port Receiver Enable Page Register, 02h

Address	Description	Name	Status	Function
02h	Port Receiver Enable	RENEN	R/W	When bit 0 is set to 0, port receiver is disabled. When bit 0 is set to 1, port receiver is enabled.
NOTE: Upon reset, restored default value is 0h.				

Table 25. Transmit Control Page Register, 03h

Address	Description	Name	Status	Bit	Function	
03h	Transmit Control	TXCON	R/W	7	Transmit all ones enable (TAOS)	
				6	Transmit output high impedance (OES)	
				5	Transmit Clock Detect Enable TCLK detection is enabled when this bit is set to zero.	
				4..1	Bits 4..1	*Decode bits 4 to 0 for pre-programmed pulse shapes.*
					0h	• T1 SH 0-133 ft.
					1h	• T1 SH 134 -266 ft.
					2h	• T1 SH 267 - 399 ft.
					3h	• T1 SH 400 -533 ft.
					4h	• T1 SH 534 - 655 ft.
					5h	• T1 0dB LH
					6h	• T1 LH -7.5 dB
					7h	• T1 LH -15 dB
					8h	• T1 LH -22.5 dB
					9h	• E1 SH 75 Ω
					Ah	• E1 SH 120 Ω
					Bh	• E1 LH 75 Ω
					Ch	• E1 LH 120 Ω
					Dh	• J1 (no encoded pulse)
					Eh	• Not used
					Fh	• Not used
				0	Bit 0 controls ATWG operation. ATWG is enabled when it 0 is set to 1.	
NOTE: Upon reset, restored default value is 0h.						

Table 26. Receive Control Page Register, 04h

Address	Description	Name	Status	Bit	Function
04h	Receiver Control	RXSH	R/W	7	active high limits receiver to SH operation
		MON_MOD		6	active high enables monitor mode
				5	*Not used*
		RXCON		Bits 4..0	*bits 4 to 0 select receiver sensitivity in dB. Refer to Table 7 for details.*

Table 27. Termination Control Page Register, 05h

Address	Description	Name	Status	Bit	Function	
05h	Termination Control TX/RX	TERM	R/W	7..6	Bits 7..6	*Decode bits 7 to 6 selecting transmit termination control*
					0	• 100 Ω
					1	• 110 Ω
					2	• 120 Ω
					3	• 120 Ω
				5..2	*Bit 5 through 2 are not assigned*	
				1..0	Bits 1..0	*Decode bits 1 to 0 selecting receive termination control*
					0	• 100 Ω
					1	• 110 Ω
					2	• 120 Ω
					3	• 100 Ω
NOTE: Upon reset, restored default value is 0h.						

Table 28. Receiver Equalizer Status Zero Page Register, 06h

Address	Description	Name	Status	Bit	Function
06h	RX Equalizer Status0	RXSTATUS0	R	7..0	*Reserved*
NOTE: Upon reset, restored default value is 0h.					

Table 29. Receiver Equalizer Status One Page Register, 07h

Address	Description	Name	Status	Bit	Function
07h	RX Equalizer Status1	RXSTATUS1	R	7..4	*Reserved*
				3..0	Decode AGC state settings. Bits 0 through 3 can be used to determine the cable/attenuation length.
NOTE: Upon reset, restored default value is 0h.					

Table 30. Receiver Equalizer Status Two Page Register, 08h

Address	Description	Name	Status	Bit	Function
08h	RX Equalizer Status 2	RXSTATUS2	R	7..5	*Reserved*
				4	LOS status bit, 1 = LOS has occurred.
				3	*Not used*
				2	*Reserved*
				1	*Reserved*
				0	*Reserved*
NOTE: Upon reset, restored default value is 0h.					

Table 31. LOS Window Page Register, 0Bh

Address	Description	Name	Status	Function
0Bh	LOS Window for User Programmed LOS. Two modes of operation are available: 1. User LOS with Amplitude Detection. Refer to Table 23. 2. User LOS with Marks Density Detection.	LOSWINLEN	R/W	Evaluation window for LOS detection. Value in this register specifies Evaluation period for LOS declaration. The actual evaluation time (in UI or baud) is eight times the value specified in the register. The value in this register represents the actual evaluation time (in UI or baud) for LOS declaration and LOS clear.
NOTE: Upon reset, restored default value is 0h.				

Table 32. LOS Set Threshold One Page Register, 0Ch

Address	Description	Name	Status	Function
0Ch	LOS Set Threshold	LOSTHRES1	R/W	This register controls two functions: 1. User LOS with Amplitude Detection. Refer to Table 23. In this mode the value in this register represents the maximum level of the received signal (multiply the register decimal value by 4mv) to declare LOS. This variable is named LOSSET. LOSSET must be less or equal than LOSCLR (defined in Table 33). 2. User LOS with Marks Density Detection. Refer to Table 23. In this mode the value in this register represents the upper limit of the number of consecutive zeros allowed during evaluation time (specified in the LOS Window Page Register, 0Bh), before digital LOS is cleared. This variable is named MAXZERO.
NOTE: Upon reset, restored default value is 0h.				

Table 33. LOS Reset Threshold Two Page Register, 0Dh

Address	Description	Name	Status	Function
0Dh	LOS Reset Threshold	LOSTHRES2	R/W	This register controls two functions: 1. User LOS with Amplitude Detection. Refer to Table 23. In this mode the value in register 0Dh represents the minimum level of the received signal (multiply the register decimal value by 4mv) to clear Analog LOS. This variable is named LOSCLR. LOSCLR must be larger than or equal to LOS declare threshold (LOSSET). 2. User LOS with Marks Density Detection (digital LOS). Refer to Table 23. In this mode the register value represents the minimum number of marks required to clear digital LOS. This variable is named MINMARKS.

Table 34. Loopback Enable Page Register, 10h

Address	Description	Name	Status	Bit	Function
10h	Loopback Enable Register	LER	R/W	7	Bit 7 inverts the RCLK, when set to 1.
				6, 5	*Reserved: write as "0"*
				4	DLOOP, Digital loopback, when set to '1'
				3	Transmit network Loop Down code
				2	Transmit network Loop Up code
				1	NLOOP, Network loopback enabled when set to '1', (Receive)
				0	RLOOP, Remote loopback, when set to '1'
NOTE: Upon reset, restored default value is 0h.					

Table 35. Interrupt Enable Page Register, 11h

Address	Description	Name	Status	Bit	Function
11h	Interrupt Enable Register	IER	R/W	7..5	*Reserved: write as "0"*
				4	DJA Underflow Interrupt Enable, when set to '1'
				3	DJA Overflow Interrupt Enable, when set to '1'
				2	NLOOP Interrupt Enable, when set to '1'
				1	AIS Interrupt Enable, when set to '1'
				0	LOS Interrupt Enable, when set to '1'
NOTE: Upon reset, restored default value is 0h.					

Table 36. Alarm Status One Page Register, 12h

Address	Description	Name	Status	Bit	Function
12h	Alarm Status Register 1	SR1	R	7..4	*Bits 7 to 4 not used.*
				3	DJA overflow status
				2	DJA underflow status
				1	NLOOP status
				0	AIS status
NOTE: Upon reset, restored default value is 0h.					

Table 37. Interrupt Status Two Page Register, 13h

Address	Description	Name	Status	Bit	Function
13h	Interrupt Status Register 2	SR2	R	7..5	*Bits 7 to 5 not used.*
				4	LOS interrupt status
				3	DJA overflow interrupt status
				2	DJA underflow interrupt status
				1	NLOOP interrupt status
				0	AIS interrupt status
NOTE: Upon reset, restored default value is 0h.					

Table 38. Line Coding Control One Page Register, 1Ch

Address	Description	Name	Status	Bit	Function	
1Ch	Control Register 1	CR1	R/W	7	ez mode - 0: ANSI, 1: FCC	
				6..5	Bits 6..5	*Decode bits 6 to 5 selecting BPV Counter mode*
					0h	• Enable counting of both BPVs and Excess Zero
					1h	• Enable counting of BPVs only
					2h	• Enable counting of Excess Zeroes only
					3h	• Invalid code
				4	E1AIS_Sel, 0 = ITU G.775, 1 = ETSI 300233	
				3	Transmit B8ZS/HDB3 enable, 1 = HDB3/B8ZS	
				2	Receive B8ZS/HDB3 enable, 1 = HDB3/B8ZS	
				1	Transmit Unipolar/Bipolar select, 0 = Bipolar	
				0	Receive Unipolar/Bipolar select, 0 = Bipolar	
NOTE: Upon reset, restored default value is 0h.						

Table 39. JA Control Two Page Register, 1Dh

Address	Description	Name	Status	Bit	Function
1Dh	Control Register 2	JARES	R/W	7	1 = reset DJA's elastic store
		JARST		6	1 = completely reset DJA
		JAJC		5	0=jamming enabled, 1=jamming disabled
		ES64		4	DJA depth select, 0 = 32 bits, 1 = 64 bits, bits 2, 3, and 4 determine the DJA corner frequency.
		JABW1		3	JABW1, bits 2, 3, and 4 determine the DJA corner frequency. Refer to Table 40.
		JABW0		2	JABW0, bits 2, 3, and 4 determine the DJA corner frequency. Refer to Table 40.
		JA transmit or receive path		1	0 = JA in receive path; 1 = JA in transmit path
		JA enable		0	1 = JA enable
NOTE: Upon reset, restored default value is 0h.					

Table 40. DJA Corner Frequency Selection

T1/E1 Mode	JA Control Register Bit 4	JA Control Register Bit 3	JA Control Register Bit 2	DJA Corner Frequency
T1	0	0	0	3
T1	0	0	1	6
T1	0	1	x	14
T1	1	0	0	3
T1	1	0	1	6
T1	1	1	x	8
E1	0	x	x	3
E1	1	x	x	3

Table 41. BPV Counter High Byte Page Register, 1Eh

Address	Description	Name	Status	Function
1Eh	BPV counter high byte	BPVCTRHB	R	High byte of the 16-bit BPV counter shadow register
NOTE: Upon reset, restored default value is 0h.				

Table 42. BPV Counter Low Byte Page Register, 1Fh

Address	Description	Name	Status	Function
1Fh	BPV counter low byte	BPVCTRLB	R	Low byte of the 16-bit BPV counter shadow register
NOTE: Upon reset, restored default value is 0h.				

Table 43. Receiver Control Page Register, 3Ch

Address	Description	Name	Status	Function
3Ch	Receive Settings	RWFCTRL	R/W	Write value 11h to Enhance receiver performance.
NOTE: Upon reset, restored default value is 0h.				

Table 44. Transmit Coefficient Page Register Range, 40h-6Fh

Address	Description	Name	Status	Function	
40-6F	Transmit Coefficients for pulse shaping	TXCOEF	R/W	**Address**	48 8-bit TX filter coefficients. Allows the user to modify three Unit Intevals of the transmit signal.
				40-4F	Register Controlling coefficients for UI #1
				50-5F	Register Controlling coefficients for UI #2
				60-6F	Register Controlling coefficients for UI #3
NOTE: Upon reset, restored default value is 0h.					

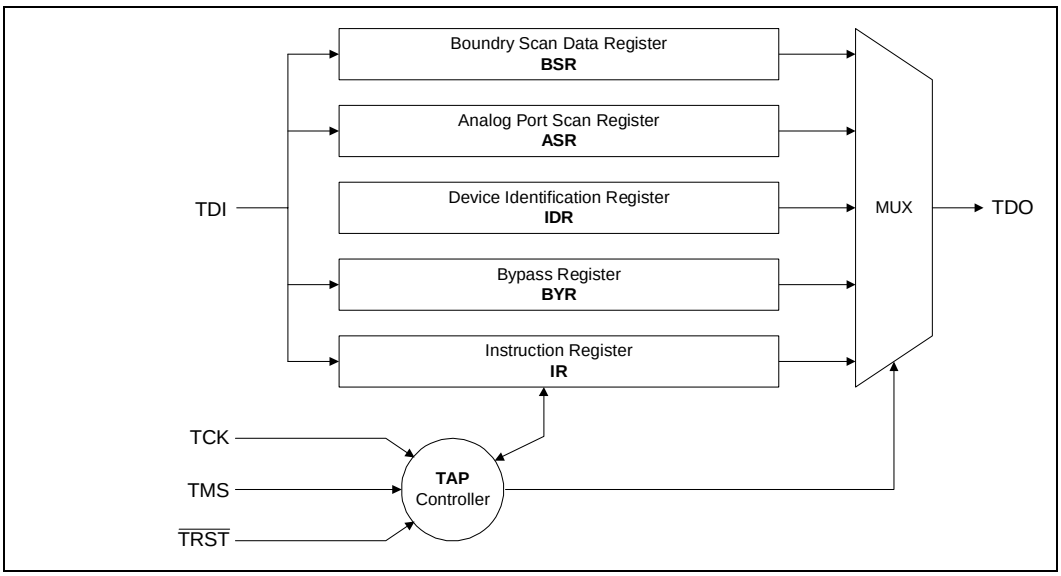
16.0 JTAG Boundary Scan

The Intel® LXT3108 LIU supports IEEE 1149.1 compliant JTAG boundary scan. Boundary scan allows easy access to the interface pins for board testing purposes.

16.1 Architecture

Figure 23 represents the Intel® LXT3108 LIU basic JTAG architecture:

Figure 23. Intel® LXT3108 LIU JTAG Architecture



The Intel® LXT3108 LIU JTAG architecture includes a TAP Test Access Port Controller, data registers and an instruction register. The following paragraphs describe these blocks in detail.

16.2 TAP Controller

The TAP controller is a 16-state synchronous state machine controlled by the TMS input and clocked by TCK (see Figure 24). The TAP controls whether the Intel® LXT3108 LIU is in reset mode, receiving an instruction, receiving data, transmitting data or in an idle state. Table 45 describes in detail each of the states represented in Figure 24.

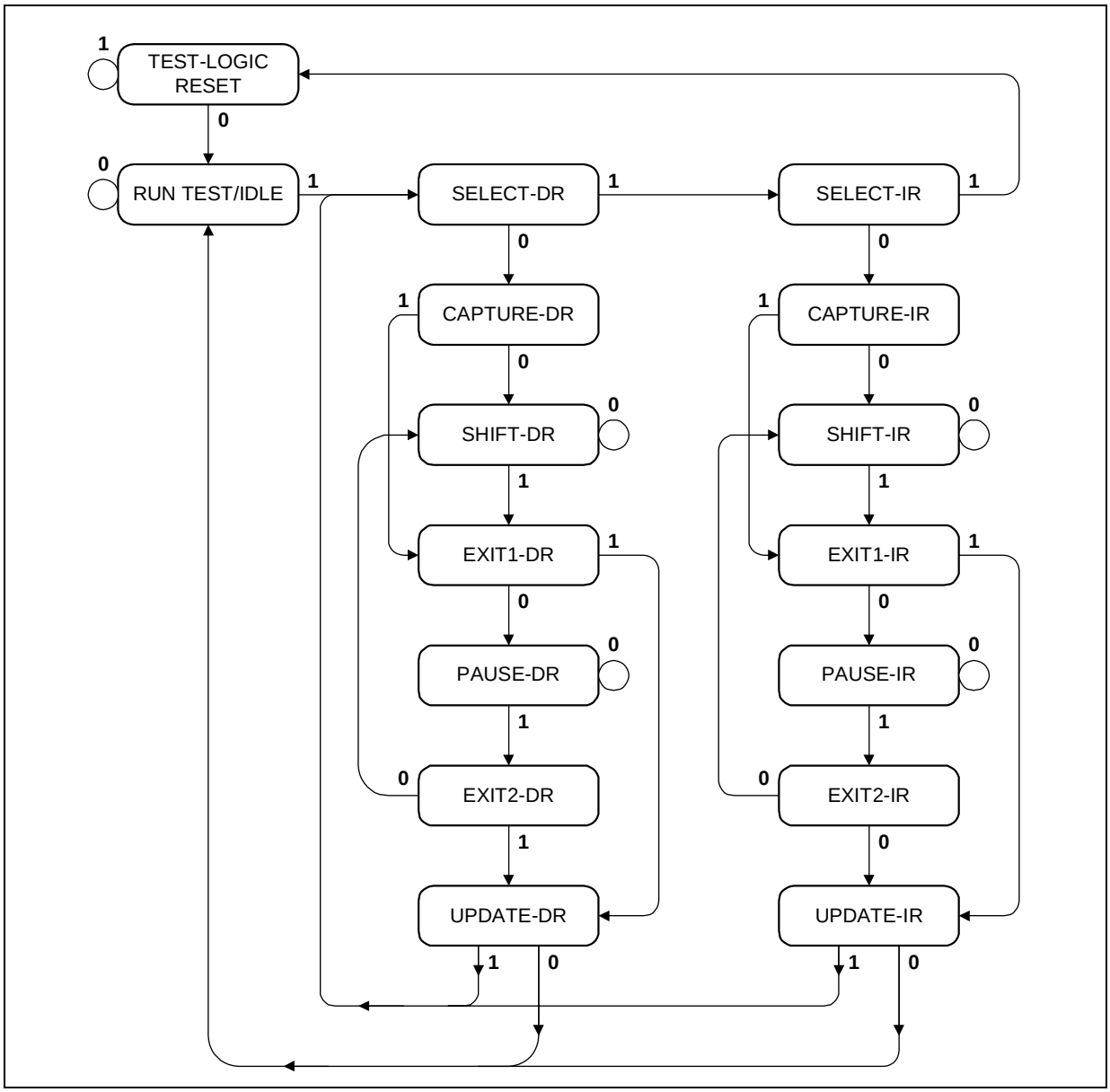
Table 45. TAP State Description (Sheet 1 of 2)

State	Description
Test Logic Reset	In this state the test logic is disabled. The device is set to normal operation mode. While in this state, the instruction register is set to the ICODE instruction.
Run -Test/Idle	The TAP controller stays in this state as long as TMS is low. Used to perform tests.
Capture - DR	The Boundary Scan Data Register (BSR) is loaded with input pin data.
Shift - DR	Shifts the selected test data registers by one stage toward its serial output.

Table 45. TAP State Description (Sheet 2 of 2)

State	Description
Update - DR	Data is latched into the parallel output of the BSR when selected.
Capture - IR	Used to load the instruction register with a fixed instruction.
Shift - IR	Shifts the instruction register by one stage.
Update - IR	Loads a new instruction into the instruction register.
Pause - IR Pause - DR	Momentarily pauses shifting of data through the data/instruction registers.
Exit1 - IR Exit1 - DR Exit2 - IR Exit2 - DR	Temporary states that can be used to terminate the scanning process.

Figure 24. JTAG State Diagram



16.3 JTAG Register Description

The following paragraphs describe each of the registers represented in Figure 23.

16.3.1 Boundary Scan Register (BSR)

The BSR is a shift register that provides access to all the digital I/O pins. The BSR is used to apply and read test patterns to/from the board. Each pin is associated with a scan cell in the BSR register. Bidirectional pins or tristatable pins require more than one position in the register. Data into the BSR is shifted in LSB first.

16.3.2 Device Identification Register (IDR)

The IDR register provides access to the manufacturer number, part number and the Intel® LXT3108 LIU revision. The register is arranged per IEEE 1149.1 and is represented in Table 46. Data into the IDR is shifted in LSB first.

Table 46. Device Identification Register (IDR)

Bit #	Value	Comments
31 - 28	0010	Revision Number “B”
27 - 12	0000110000100100	Part Number = 3108
11 - 1	00000001001	Manufacturer ID
0	1	Set to “1”

16.3.3 Bypass Register (BYR)

The Bypass Register is a 1-bit register that allows direct connection between the TDI input and the TDO output.

16.3.4 Instruction Register (IR)

The IR is a 3-bit shift register that loads the instruction to be performed. The instructions are shifted LSB first. Table 47 shows the valid instruction codes and the corresponding instruction description.

Table 47. Instruction Register (IR) (Sheet 1 of 2)

Instruction	Code #	Comments
EXTEST	000	Connects the BSR to TDI and TDO. Input pins values are loaded into the BSR. Output pins values are loaded from the BSR.
INTEST_ANALOG	010	Connects the ASR to TDI and TDO. Allows voltage forcing/ sensing through AT1 and AT2.

Table 47. Instruction Register (IR) (Sheet 2 of 2)

Instruction	Code #	Comments
SAMPLE/PRELOAD	100	Connects the BSR to TDI and TDO. The normal path between the Intel® LXT3108 LIU logic and the I/O pins is maintained. The BSR is loaded with the signals in the I/O pins.
IDCODE	110	Connects the IDR to the TDO pin.
BYPASS	111	Serial data from the TDI input is passed to the TDO output through the 1 bit Bypass Register.

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17.0 Test Specifications

Table 48. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply (reference to GND)[1]	VCC, TVCC	-0.5	3.6	V
Input voltage, RTIP/RRING	VRX	TBD	TBD	V
Input voltage, any digital pin	VIN	GND-0.5	5.5	V
Input current, any pin	IIN	-10	10	mA
Storage temperature	TSTG	-65	150	°C
Thermal Resistance, junction to ambient, QFP	θJA		16	°C/W
Thermal Resistance, junction to ambient, PBGA	θJA		17.7	°C/W
ESD voltage, any pin[2,3]	VIN	2000	–	V

Caution: Operation at these limits may permanently damage the device. Normal operation at these extremes not guaranteed.

1. TVCC and VCC must not differ by more than 0.3 V during operation. TGND and GND must not differ by more than 0.3 V during operation.
2. Human body model.
3. This is a design target and not a product specification.

Table 49. Recommended Operating Conditions

Parameter			Sym	Min	Typ[1]	Max	Unit	Test Conditions
DC supply [2]			VCC, TVCC	3.135	3.3	3.465	V	3.3 V +/- 5%
Ambient operating temperature			TA	-40	–	85	° C	
Total power dissipation[3, 4]	T1	SH	PD	–	TBD	2.95	W	100% mark density
			PD	–	TBD	2.3	W	50% mark density
		LH	PD	–	TBD	2.5	W	100% mark density
			PD	–	TBD	–	W	50% mark density
	E1	SH/ LH	PD	–	TBD	2.8	W	100% mark density
			PD	–	TBD	2.25	W	50% mark density
Recommended line load to TTIP/ TRING			–	TBD	–	100 110 120	W	For T1 mode. For J1 mode. For E1, 120 Ω twisted pair.

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TVCC and VCC must not differ by more than 0.3 V.
3. Power dissipation specifications are TBD.
4. Power dissipation values include shared circuit.

Table 50. Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
High level input voltage[1]	VIH	2	–	5	V	In idle and power down
Low level input voltage[1]	VIL	–	–	0.8	V	
Output High voltage[2]	VOH	2.4		VCCIO	V	
Output Low voltage[2]	VOL	–	–	0.4	V	
Quiescent current	IDDQ	0	–	±10	µA	
Input leakage current	ILL	0	–	±50	µA	
Three-state leakage current (all outputs)	I3L	0	–	±10	µA	
TTIP/TRING leakage current	ITR	–	–	±10	µA	In idle and power down
Output driver rise time	TR	–	–	10	ns	1 pF load

1. Intel® LXT3108 LIU interface via CMOS logic levels.
2. Output drivers will output TTL logic levels.

Table 51. E1 Transmitter Analog Characteristics

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
Internal transmitter impedance tolerance		–	–	TBD	5	%	Matching line load
Pulse amplitude variation per LSB	CEPT (ITU)	–	TBD	–	TBD	mV	**TBD**
Output pulse amplitude	120 Ω	–	2.7	3.0	3.3	V	Tested at the line side
Peak voltage of a space	120 Ω	–	-0.3	–	0.3	V	
Transmit amplitude variation with supply		–	-1	–	+1	%	
Difference between pulse sequences		–		–	200	mV	For 17 consecutive pulses
Transmit return loss 120 Ω twisted pair cable. Measured with PRBS pattern.[1]	51 kHz to 102 kHz	–	6	16	–	dB	
	102 kHz to 2.048 MHz	–	8	12	–	dB	
	2.048 MHz to 3.072 MHz	–	8	11	–	dB	
Transmit intrinsic jitter; 20 Hz to 100 kHz		–	–	.025	.05	UI	Tx path TCLK is jitter free
Transmit path delay	Bipolar mode	–	TBD	60	–	ns	JA Disabled
	Unipolar mode	–	TBD	60	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 52. E1 Receiver Analog Characteristics

Parameter		Sym	Min.	Typ.[1]	Max.	Unit	Test Condition
Permissible cable attenuation		–	–	–	43	dB	@1024 kHz
Receiver sensitivity @ 1024 kHz (E1 line loss)	(E1 SH/12 dB)	–	-13.6	–	–	dB	Receiver sensitivity @ 1024 kHz
	(E1 LH/43 dB)	–	-43	–	–	dB	
Receiver dynamic range		DR	–	–	–	Vp	
Signal to noise interference margin		S/I	-12	–	–	dB	Per G.703, O.151 @ 6 dB cable Attenuation
Loss of signal threshold		–	–	TBD	–	mV	Programmable
Consecutive zeros before loss of signal		–	–	32	–	–	G.775 recommendation
		–	–	2048	–	–	ETSI 300 233 specification
LOS reset		–	12.5%	–	–	–	1s density
LOS delay time				30		µs	Data recovery mode
LOS reset			10		255	marks	Data recovery mode
Low limit input jitter tolerance [2]	1 Hz	–	37	–	–	U.I	G.823 recommendation Cable Attenuation is 6 dB
	20 Hz to 2.4 kHz	–	1.5	–	–	U.I	
	100 kHz	–	0.2	–	–	U.I	
Differential receiver input impedance		–	–	TBD	TBD	k Ω	@1.024 MHz
Common mode input impedance to ground		–	–	TBD		k Ω	
Input termination resistor tolerance		–	–	–	±1	%	
Input return loss[2]	51 kHz - 102 kHz	–	TBD	–	12	dB	
	102 - 2048 kHz	–	TBD	–	18	dB	
	2048 kHz - 3072 kHz	–	TBD	–	14	dB	
Receive intrinsic jitter, RCLK output		–	–	0.06	0.1	UI	Wide band jitter
Receive path delay	Bipolar mode	–	–	5	–	UI	JA Disabled
	Unipolar mode	–	–	5	–	UI	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 53. T1 Transmitter Analog Characteristics (Sheet 1 of 2)

Parameter		Sym	Min.	Typ.[1]	Max.	Unit	Test Condition
Internal transmitter impedance tolerance		–	–	TBD	–	%	Matching line load
Pulse amplitude variation per LSB	DSX-1, DS1	–	–	30	40	mV	Measured on the line side termination.
Output pulse amplitude		–	2.4	3.0	3.6	V	Measured at the DSX
Peak voltage of a space		–	-0.15	–	+0.15	V	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.
3. Power measured in a 3 KHz bandwidth at the point the signal arrives at the distribution frame for an all 1's pattern.

Table 53. T1 Transmitter Analog Characteristics (Sheet 2 of 2)

Parameter		Sym	Min.	Typ.[1]	Max.	Unit	Test Condition
Transmit amplitude variation with power supply		–	TBD	1	TBD	%	
Difference between pulse sequences		–	–	–	200	mV	For 17 consecutive pulses, GR-499-CORE
Pulse width variation at half amplitude[1]		–	–	–	20	ns	
Line side short circuit current (T1)		–	–	–	150	mA RMS	
Jitter added by Transmitter[2]	10Hz - 8 KHz	–	–	–	0.025	UI_{pk-pk}	AT&T Pub 62411 TCLK is jitter free
	8KHz - 40 KHz	–	–	–	0.025	UI_{pk-pk}	
	10Hz - 40 KHz	–	–	–	0.05	UI_{pk-pk}	
	Wide Band	–	–	–	0.05	UI_{pk-pk}	
Output power levels[3]	@ 772 KHz	–	12.6	–	17.9	dBm	T1.102 - 1993 Referenced to power at 772 KHz
	1544 KHz	–	-29	–	17.9	dBm	
Transmit Return Loss [2]	39 KHz - 77 KHz	–	6	TBD	–	dB	
	77- 1544 KHz	–	8	TBD	–	dB	
	1544 KHz - 2316KHz	–	8	TBD	–	dB	
Transmit path delay	Bipolar mode	–		60	–	ns	JA Disabled
	Unipolar mode	–		60	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.
3. Power measured in a 3 KHz bandwidth at the point the signal arrives at the distribution frame for an all 1's pattern.

Table 54. T1 Receiver Analog Characteristics (Sheet 1 of 2)

Parameter		Sym	Min.	Typ.[1]	Max.	Unit	Test Condition
Permissible cable attenuation		–	–	36	TBD	dB	@ 772 KHz
Receiver sensitivity @ 772 kHz (T1 line loss)	(T1 SH/12 dB)	–	-13.6	–	–	dB	Receiver sensitivity @ 772 kHz (T1 line loss)
	(T1 LH/36 dB)	–	-36	–	–	dB	
Receiver dynamic range		DR	TBD	–	–	Vp	
Signal to noise interference margin		S/I	TBD	–	–	dB	
Loss of signal threshold		–	–	TBD	–	mV	Programmable
Loss of signal Hysteresis				TBD			
Consecutive zeros before loss of signal		–	100	175	250	–	T1.231 - 1993
Low limit input jitter tolerance [2]	1 Hz	–	138	–	–	UI	AT&T Pub. 62411
	10 Hz to 300 Hz	–	28	–	–	UI	
	10 KHz to 100 KHz	–	0.4	–	–	UI	
Differential receiver input impedance		–	–	100	–	Ω	@772 kHz
Common mode input impedance to ground		–	–	120	–	Ω	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 54. T1 Receiver Analog Characteristics (Sheet 2 of 2)

Parameter		Sym	Min.	Typ.[1]	Max.	Unit	Test Condition
Input termination resistor tolerance		–	–	–	±1	%	
Input return loss[1]	39 KHz - 77KHz	–	TBD	–	12	dB	
	77- 1544 KHz	–	TBD	–	18	dB	
	1544 KHz - 2316 KHz	–	TBD	–	14	dB	
Receive intrinsic jitter, RCLK output[2]		–	–	0.03	0.05	UI	Wide band jitter
Receive path delay	Bipolar mode	–	–	TBD	–	UI	JA Disabled
	Unipolar mode	–	–	TBD	–	UI	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 55. Master and Transmit Clock Timing Characteristics

Parameter	Sym	Min	Typ[1]	Max	Unit	Notes
Master clock frequency[2]	MCLK	1.544	–	16.384	MHz	Must be supplied
Master clock tolerance	MCLKt	–	±50	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
T1 Transmit clock frequency	TCLK	–	1.544	–	MHz	
E1 Transmit clock frequency	TCLK	–	2.048	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±50	ppm	
Transmit clock duty cycle	TCLKd	10	–	100	%	
TPOS/TNEG to TCLK setup time	Tsut	10	–	–	ns	
TCLK to TPOS/TNEG hold time	Tht	10	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. MCLK frequency options are listed in Table 2 on page 39.

Figure 25. Transmit Clock Timing Diagram

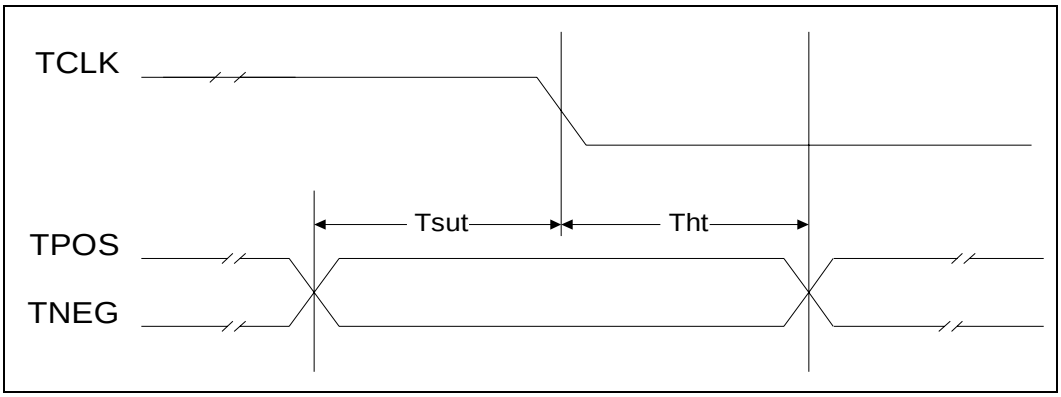


Table 56. Jitter Attenuator Characteristics

Parameter			Min.	Typ.[1]	Max.	Unit	Test Condition
E1 jitter attenuator 3dB corner frequency	JACF=0	32bit FIFO	–	2.5	–	Hz	Sinusoidal jitter modulation
		64bit FIFO	–	3.5	–	Hz	
	JACF=1	32bit FIFO	–	2.5	–	Hz	
		64bit FIFO	–	3.5	–	Hz	
T1 jitter attenuator 3dB corner frequency	JACF=0	32bit FIFO	–	3	–	Hz	
		64bit FIFO	–	3	–	Hz	
	JACF=1	32bit FIFO	–	6	–	Hz	
		64bit FIFO	–	6	–	Hz	
Jitter attenuator 3dB corner frequency[2]		E1	–	3.5	–	Hz	
		T1	–	6	–	Hz	
Data latency delay		32bit FIFO	–	16	–	UI	Delay through the Jitter attenuator only. Add TBD UI for total receive path delay and TBD UI for total transmit path delay.
		64bit FIFO	–	32	–	UI	
Input jitter tolerance before FIFO overflow or underflow		32bit FIFO	–	24	–	UI	
		64bit FIFO	–	56	–	UI	
E1 jitter attenuation	@ 3 Hz	–	-0.5	TBD	–	dB	ITU-T G.736
	@ 40 Hz	–	-0.5	TBD	–	dB	
	@ 400 Hz	–	+19.5	TBD	–	dB	
	@ 100 KHz	–	+19.5	TBD	–	dB	
T1 jitter attenuation	@ 1 Hz	–	0	TBD	–	dB	AT&T Pub. 62411
	@ 20 Hz	–	0	TBD	–	dB	
	@ 1 KHz	–	33.3	TBD	–	dB	
	@ 1.4 KHz	–	40	TBD	–	dB	
	@ 70 KHz	–	40	TBD	–	dB	
Output jitter in remote loopback[2]		–	TBD	TBD	–	UI	ETSI CTR12/13 Output jitter

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 57. Receive Timing Characteristics for T1 Operation

Parameter	Sym	Min	Typ[1]	Max	Unit
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
T1 Receive clock pulse width [2, 3]	tPW	–	648	–	ns
T1 Receive clock pulse width High	tPWH	–	324	–	ns
T1 Receive clock pulse width Low[1,3]	tPWL	260	324	388	ns
RPOS/RNEG to RCLK rising time	tSUR	–	274	–	ns
RCLK rising to RPOS/RNEG hold time	tHR	–	274	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Table 58. Receive Timing Characteristics for E1 Operation

Parameter	Sym	Min	Typ[1]	Max	Unit
E1 Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
E1 Receive clock pulse width [2, 3]	tPW	–	488	–	ns
E1 Receive clock pulse width High	tPWH	–	244	–	ns
E1 Receive clock pulse width Low[1,3]	tPWL	195	244	293	ns
RPOS/RNEG to RCLK rising time	tSUR	–	194	–	ns
RCLK rising to RPOS/RNEG hold time	tHR	–	194	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Figure 26. Receive Clock Timing Diagram

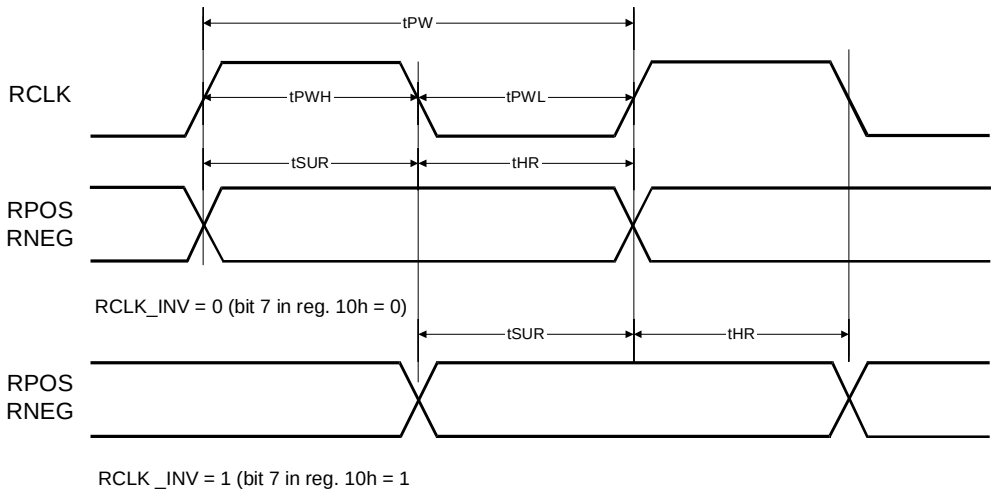


Figure 27. Intel® LXT3108 LIU Output Jitter for CTR12/13 Applications

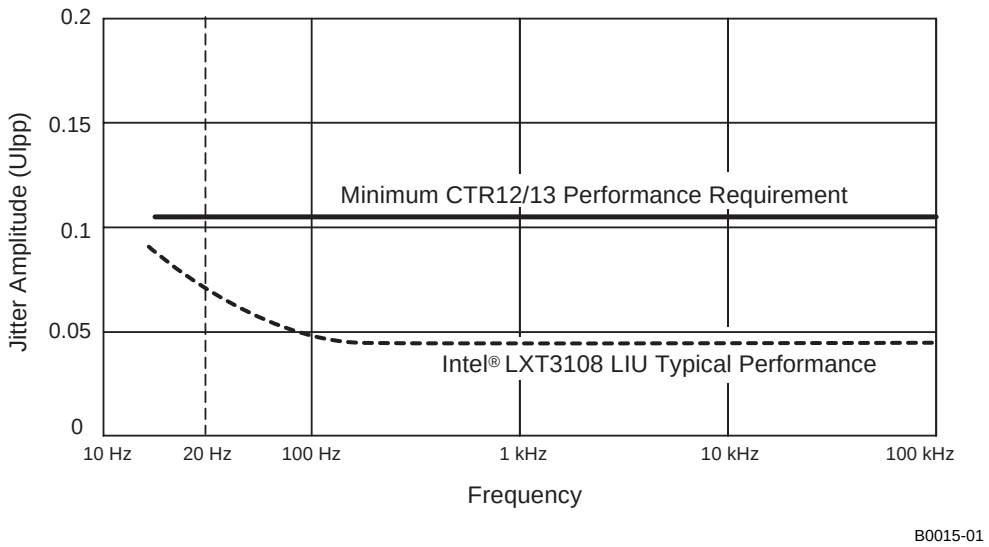


Figure 28. JTAG Timing

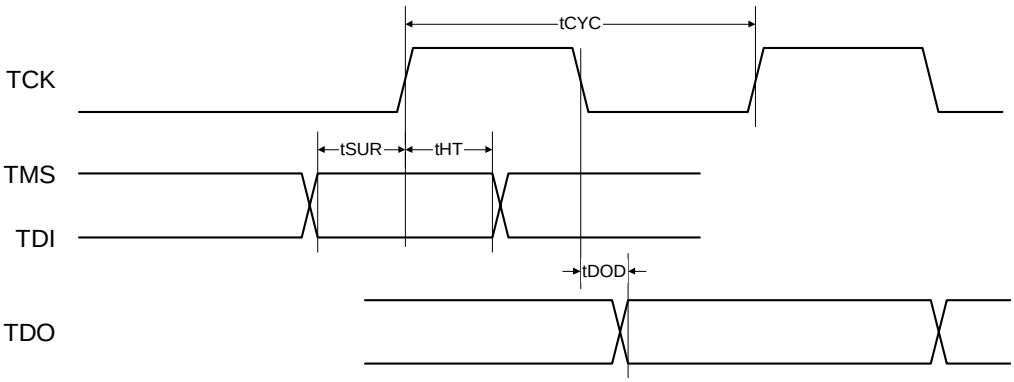


Table 59. JTAG Timing Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Cycle time	Tcyc	200	–	–	ns	
J-TMS/J-TDI to J-TCK rising edge time	Tsut	50	–	–	ns	
J-CLK rising to J-TMS/L-TDI hold time	Tht	50	–	–	ns	
J-TCLK falling to J-TDO valid	Tdod	-	–	50	ns	

Table 60. G.703 2.048 Mbps Pulse Mask Specifications

Parameter	Cable		Unit
	TWP	Coax	
Test load impedance	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Figure 29. E1, G.703 Mask Templates

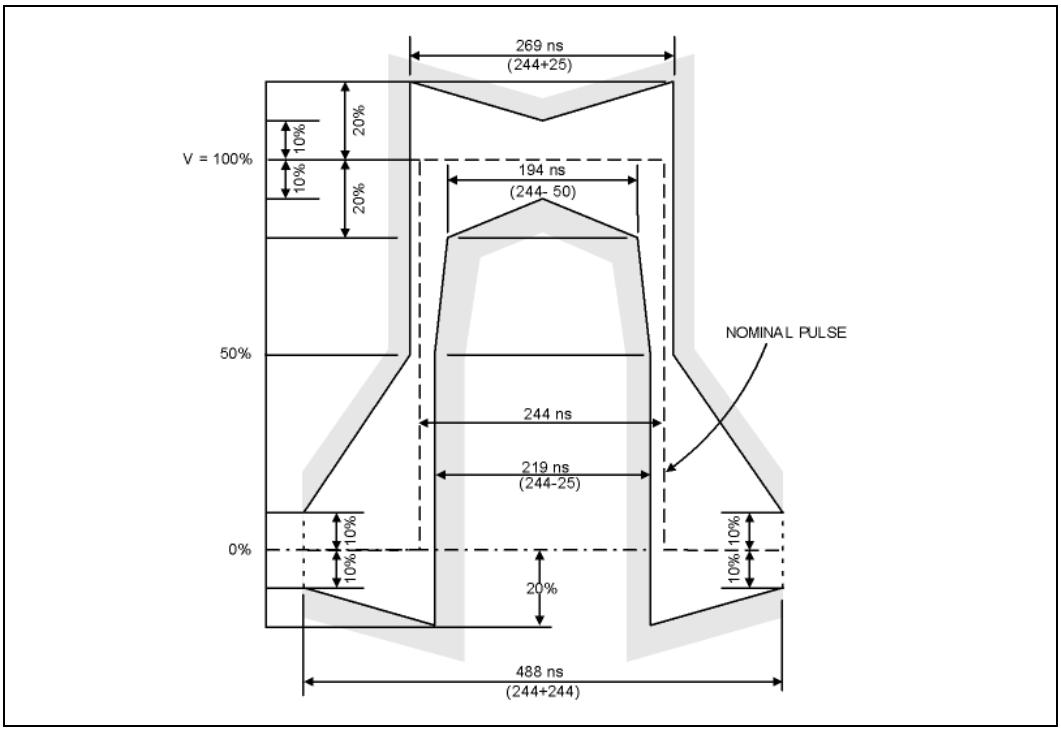


Table 61. T1.102 1.544 Mbps Pulse Mask Specifications

Parameter	Cable	Unit
	TWP	
Test load impedance	100	Ω
Nominal peak mark voltage	3.0	V
Nominal peak space voltage	0 ±0.15	V
Nominal pulse width	324	ns
Ratio of positive and negative pulse amplitudes	95-105	%

Figure 30. Intel® LXT3108 LIU Jitter Tolerance Performance

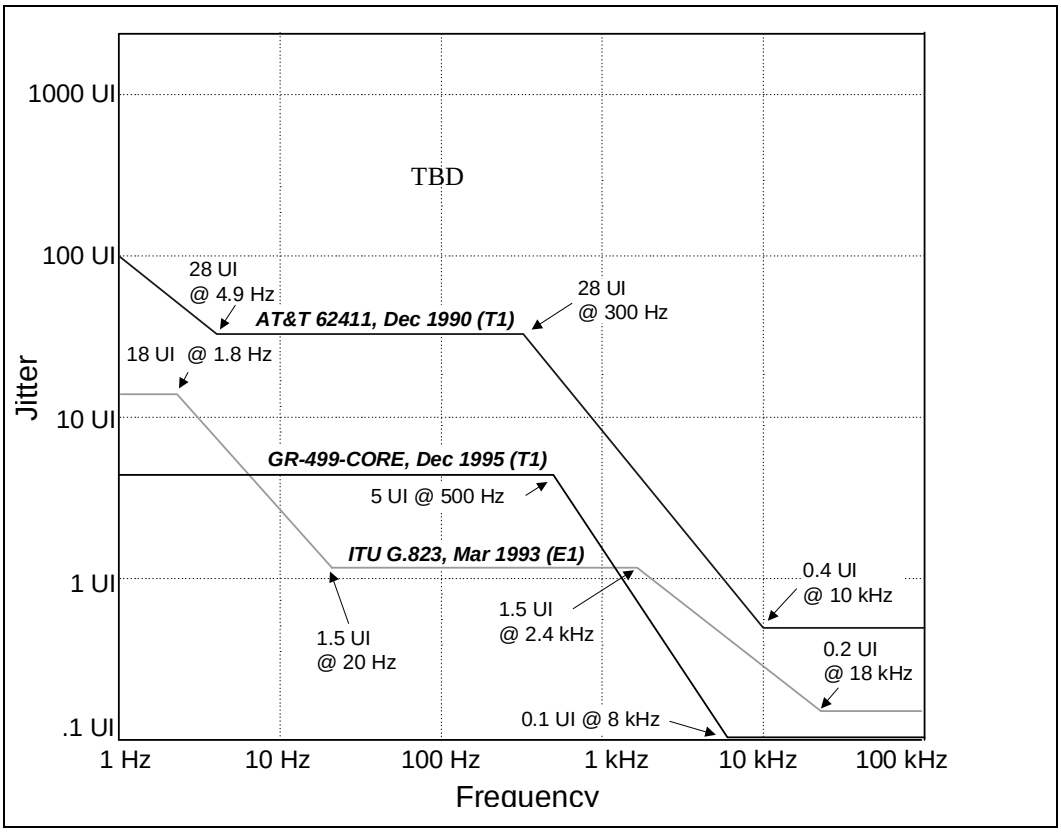
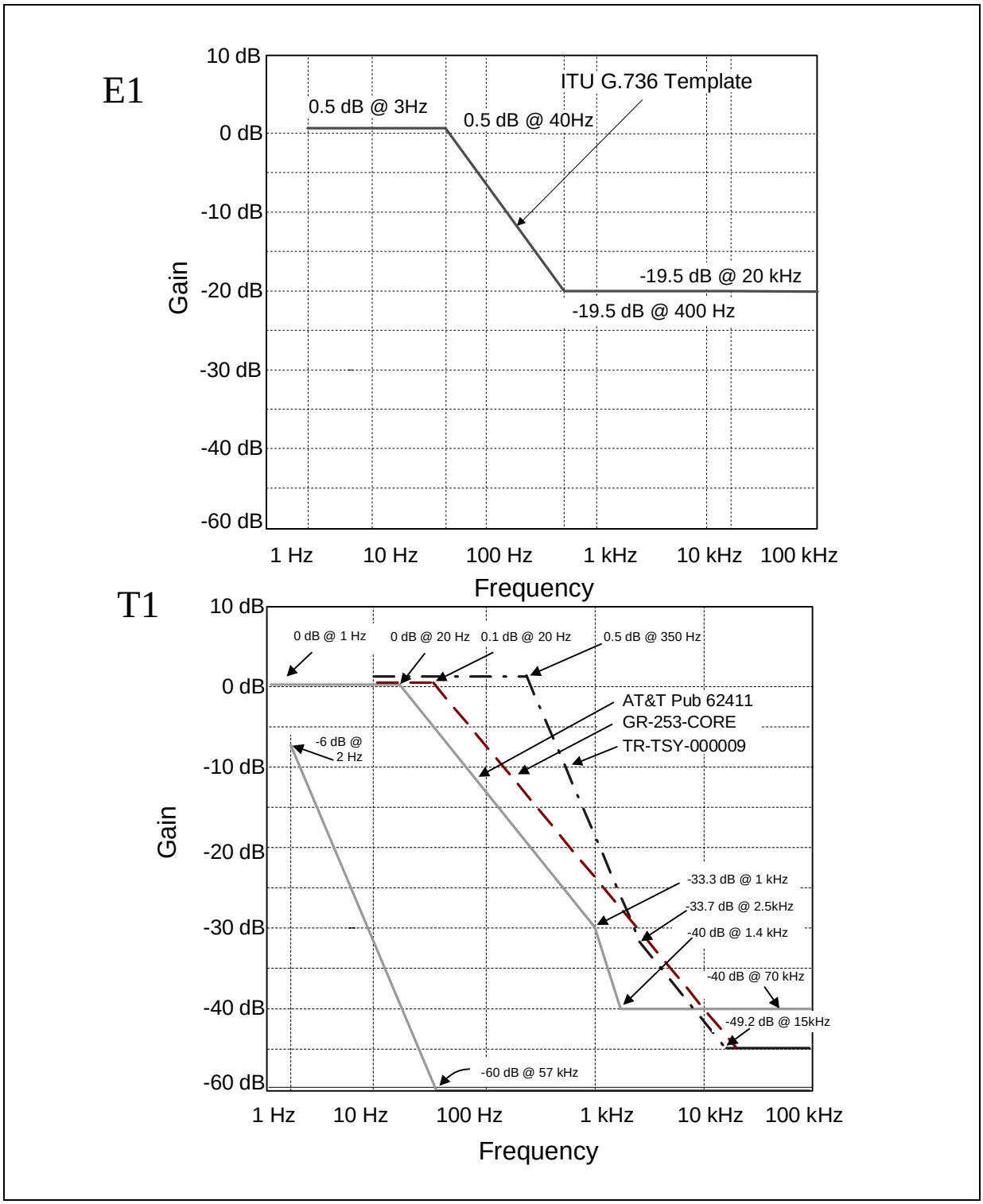


Figure 31. Intel® LXT3108 LIU Jitter Transfer Performance



17.1 Microprocessor Interface Timing Diagrams

Figure 32. MPC860 Write Timing

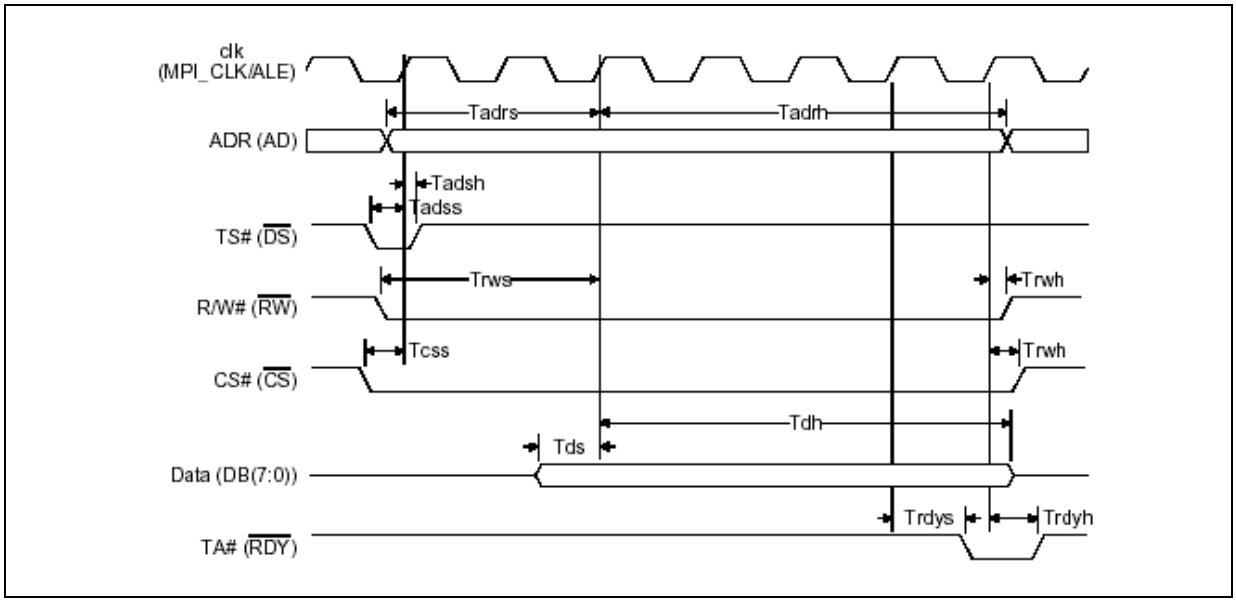


Table 62. MPC860 Write Timing Characteristics

Symbol	Parameter	Min.	Max	Unit
Tadrs	Address setup to clock	15	--	ns
Tadrh	Address hold from clock	13	--	ns
Tadss	TS# setup to clock	6	--	ns
Tadsh	TS# hold from clock	2	--	ns
Trws	R/W# setup to clock	10	--	ns
Tcss	CS# setup to clock	5	--	ns
Trwh	R/W# and CS# hold from clock	0	--	ns
Tds	Data setup to clock	7	--	ns
Tdh	Data hold from clock	16	--	ns
Trdys	clock to TA# asserted	12	16	ns
Trdyh	clock to TA# deasserted	12	16	ns

Figure 33. MPC860 Read Timing

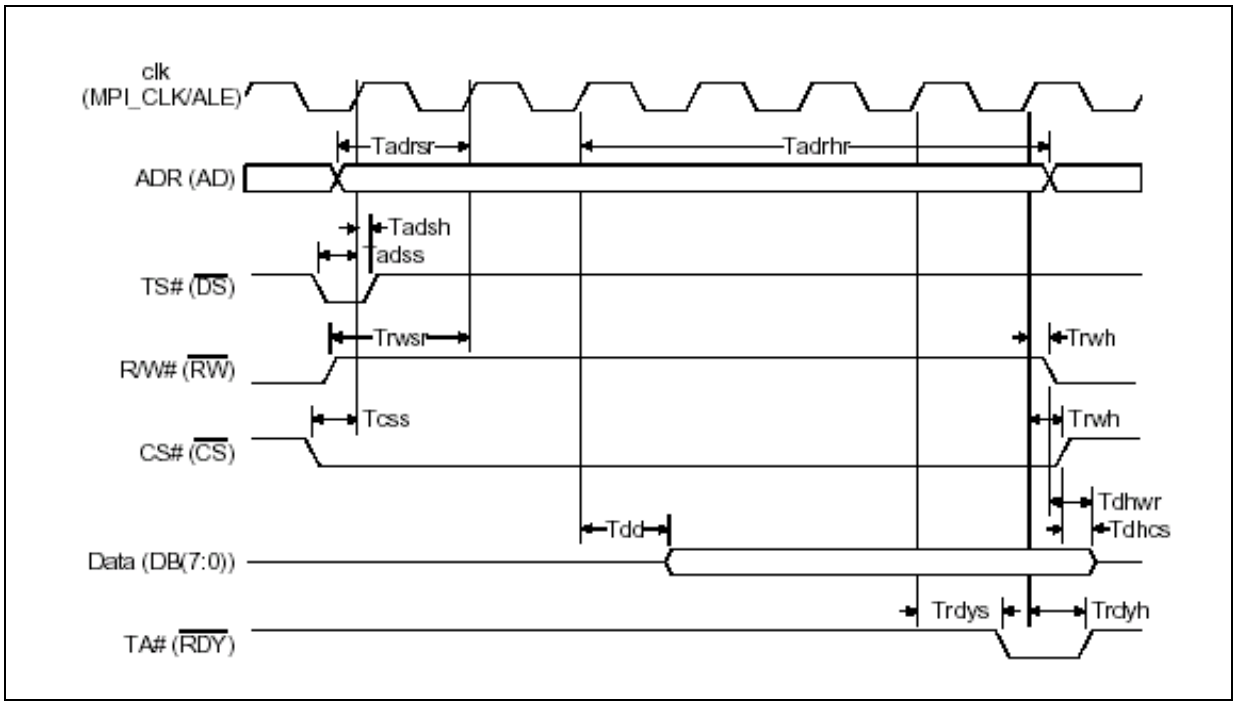


Table 63. MPC860 Read Timing Characteristics

Symbol	Parameter	Min.	Max	Unit
Tadrsr	Address setup to clock	10	--	ns
Tadrhr	Address hold from clock	10	--	ns
Tadss	TS# setup to clock	6	--	ns
Tadsh	TS# hold from clock	2	--	ns
Trwsr	R/W# setup to clock	8	--	ns
Tcss	CS# setup to clock	5	--	ns
Trwh	R/W#, CS hold to clock	0	--	ns
Tdd	clock to data valid	--	41	ns
Tdhwr	Data hold from R/W#	18	26	ns
Tdhcs	Data hold from CS#	16	23	ns
Trdys	clock to TA# asserted	12	16	ns
Trdyh	clock to TA# deasserted	12	16	ns

Figure 34. M68302 Write Timing

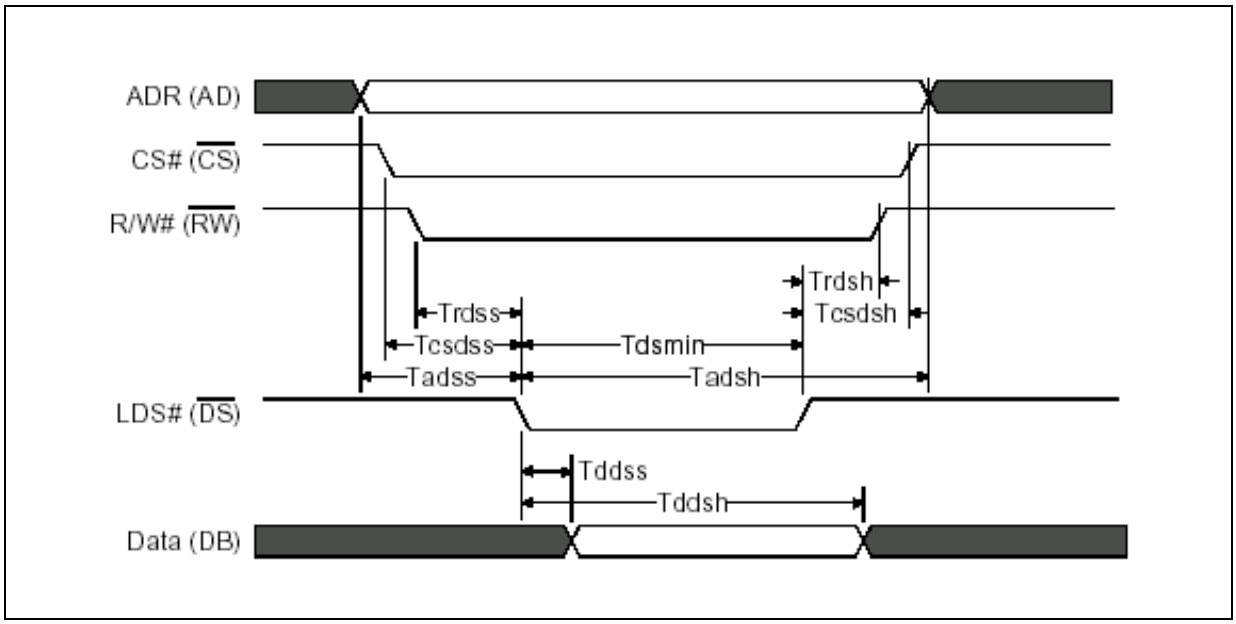


Table 64. M68302 Write Timing Characteristics

Symbol	Parameter	Min.	Max	Unit
Tadss	Address setup to LDS asserted	-8	--	ns
Tadsh	Address hold from LDS asserted	44	--	ns
Trdss	R/W# setup to LDS asserted	0	--	ns
Trdsh	R/W# hold from LDS asserted	0	--	ns
Tddss	Data setup to LDS asserted	-17	--	ns
Tddsh	Data hold from LDS asserted	46	--	ns
Tdsmin	LDS minimum width	60	--	ns
Tcsdss	CS to DS setup	3	--	ns
Tcsdsh	CS to DS hold	4	--	ns

Figure 35. M68302 Read Timing

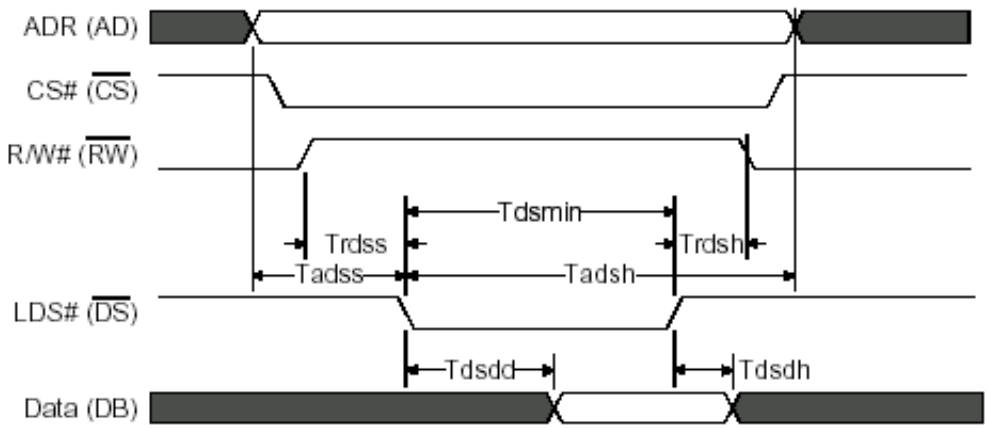


Table 65. M68302 Read Timing Characteristics

Symbol	Parameter	Min.	Max	Unit
Tadss	Address setup to LDS asserted	24	--	ns
Tadsh	Address hold from LDS assserted	41	--	ns
Trdss	R/W# setup to LDS asserted	0	--	ns
Trdsh	R/W# hold from LDS asserted	0	--	ns
Tdsdd	LDS low to data valid	--	71	ns
Tdsdh	Data hold from LDS deasserted	17	--	ns
Tdsmin	LDS minimum width	71	--	ns

Figure 36. Intel® i486™/i960® Non-muxed Mode Write Timing

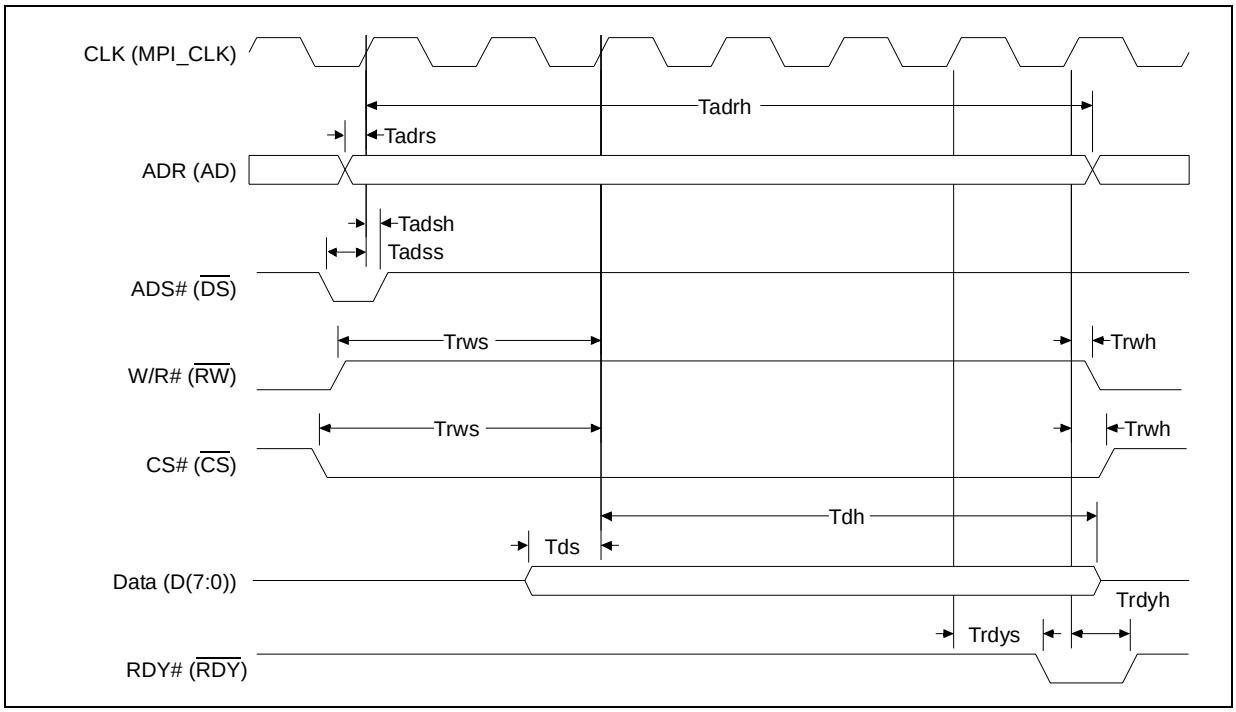


Figure 37. Intel® i960® Muxed Mode Write Timing

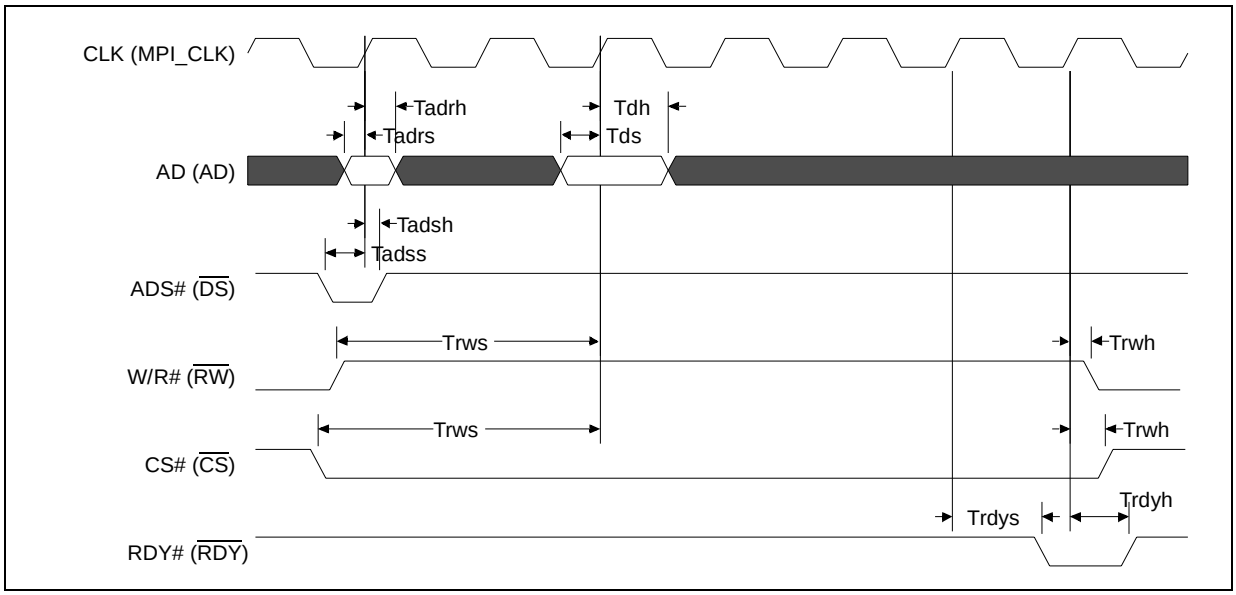


Table 66. Intel® i486™/i960® Write Timing Characteristics

Symbol	Parameter	Min.	Max	Unit
Tadrs	Address setup to clock	7	--	ns
Tadrh	Address hold from clock	5	--	ns
Tadss	ADS setup to clock	6	--	ns
Tadsh	ADS hold from clock	2	--	ns
Trws	W/R# and CS# setup to clock	10	--	ns
Trwh	W/R# and CS# hold from clock	0	--	ns
Tds	Data setup to clock	7	--	ns
Tdh	Data hold from clock	16	--	ns
Trdys	clock to READY# asserted	13	16	ns
Trdyh	clock to READY# deasserted	13	16	ns

Figure 38. Intel® i486™/i960® Non-muxed Mode Read Timing

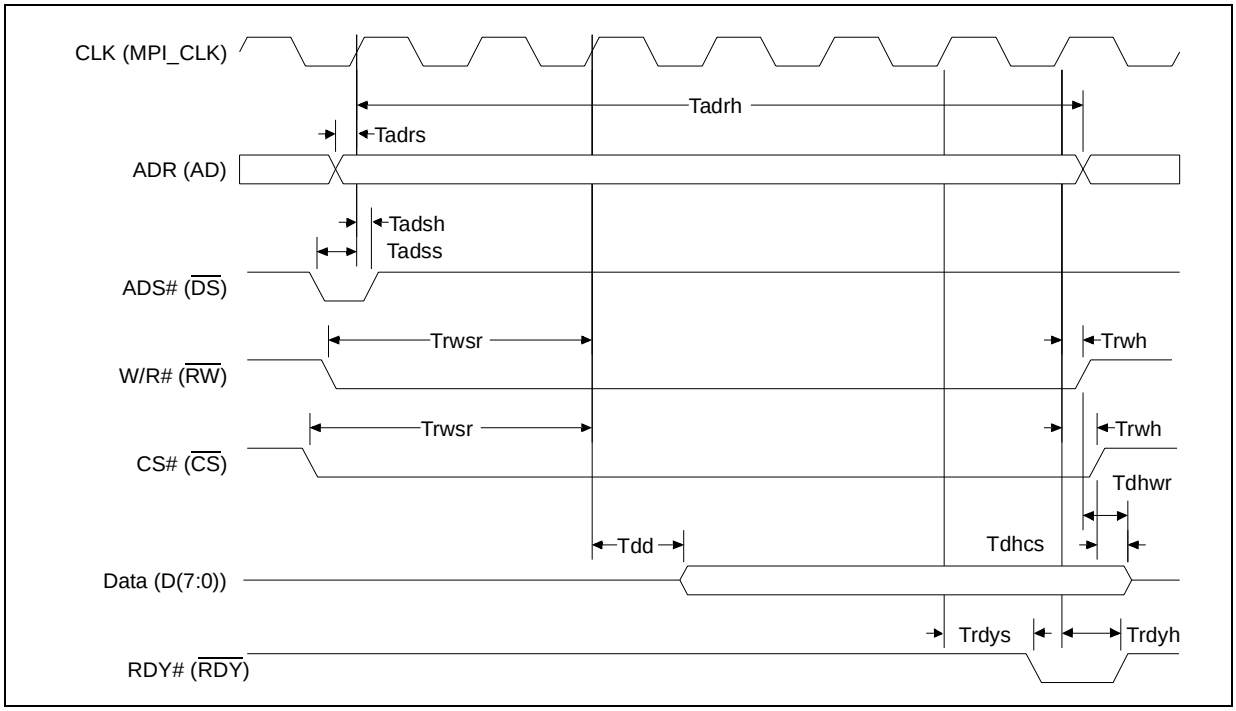


Figure 39. Intel® i960® Muxed Mode Read Timing

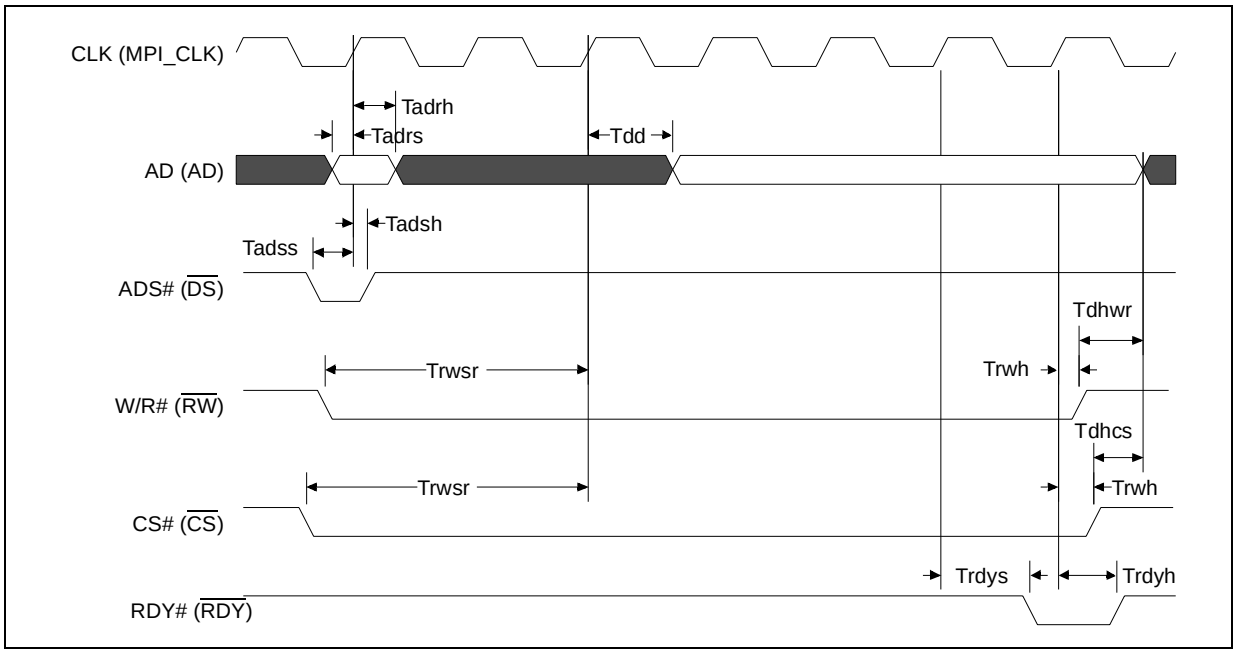


Table 67. Intel® i486™/i960® Read Timing Characteristics

Symbol	Parameter	Min.	Max	Unit
Tadrs	Address setup to clock	7	--	ns
Tadrh	Address hold from clock	5	--	ns
Tadss	ADS setup to clock	6	--	ns
Tadsh	ADS hold from clock	2	--	ns
Trwsr	W/R# and CS setup to clock	8	--	ns
Trwh	W/R# and CS hold from clock	0	--	ns
Tdd	clock to Data valid	--	41	ns
Tdhwr	Data hold from R/W#	18	27	ns
Tdhcs	Data hold from CS#	16	24	ns
Trdys	clock to READY# asserted	13	16	ns
Trdyh	clock to READY# deasserted	13	16	ns

17.2 Referenced Standards

AT&T Pub 62411 Accunet T1.5 Service

Bellcore TR-TSY-000009 Asynchronous Digital Multiplexes Requirements and Objectives

Bellcore GR-253-CORE SONET Transport Systems Common Generic Criteria

Bellcore GR-499-CORE Transport Systems Generic Requirements

ANSI T1.102 - 199X Digital Hierarchy Electrical Interface

ANSI T1.231 -1993 Digital Hierarchy Layer 1 In-Service Digital Transmission Performance Monitoring

ETSI CTR12/13 Business TeleCommunications (BTC): 2048 Kbps Digital Unstructured/ Structured Leased Line.

ETS 300166 Physical and Electrical Characteristics

G.703 Physical/electrical characteristics of hierarchical digital interfaces

G.735 Characteristics of Primary PCM multiplex equipment operating at 2048 kbps and offering digital access at 384 kbps and/or synchronous digital access at 64 kbps

G.736 Characteristics of a synchronous digital multiplex equipment operating at 2048 kbps

G.742 General Aspects of Digital Transmission Systems

G.772 Protected Monitoring Points provided on Digital Transmission Systems

G.775 Loss of signal (LOS) and alarm indication (AIS) defect detection and clearance criteria

G.783 Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks

G.823 The control of jitter and wander within digital networks which are based on the 2048 kbps hierarchy

O.161 In - service code violations monitors for digital systems. Blue Book Fasc.IV.4

BAPT220 Short Circuit Current Requirements

ITU I.431Primary Rate ISDN User-Network Interface - Layer 1

ETS 300 233Integrated Services Digital Network (ISDN); Access digital section for ISDN primary rate.

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18.0 Mechanical Specification

Figure 40. Intel® LXT3108 LIU 256 PBGA Mechanical Specification

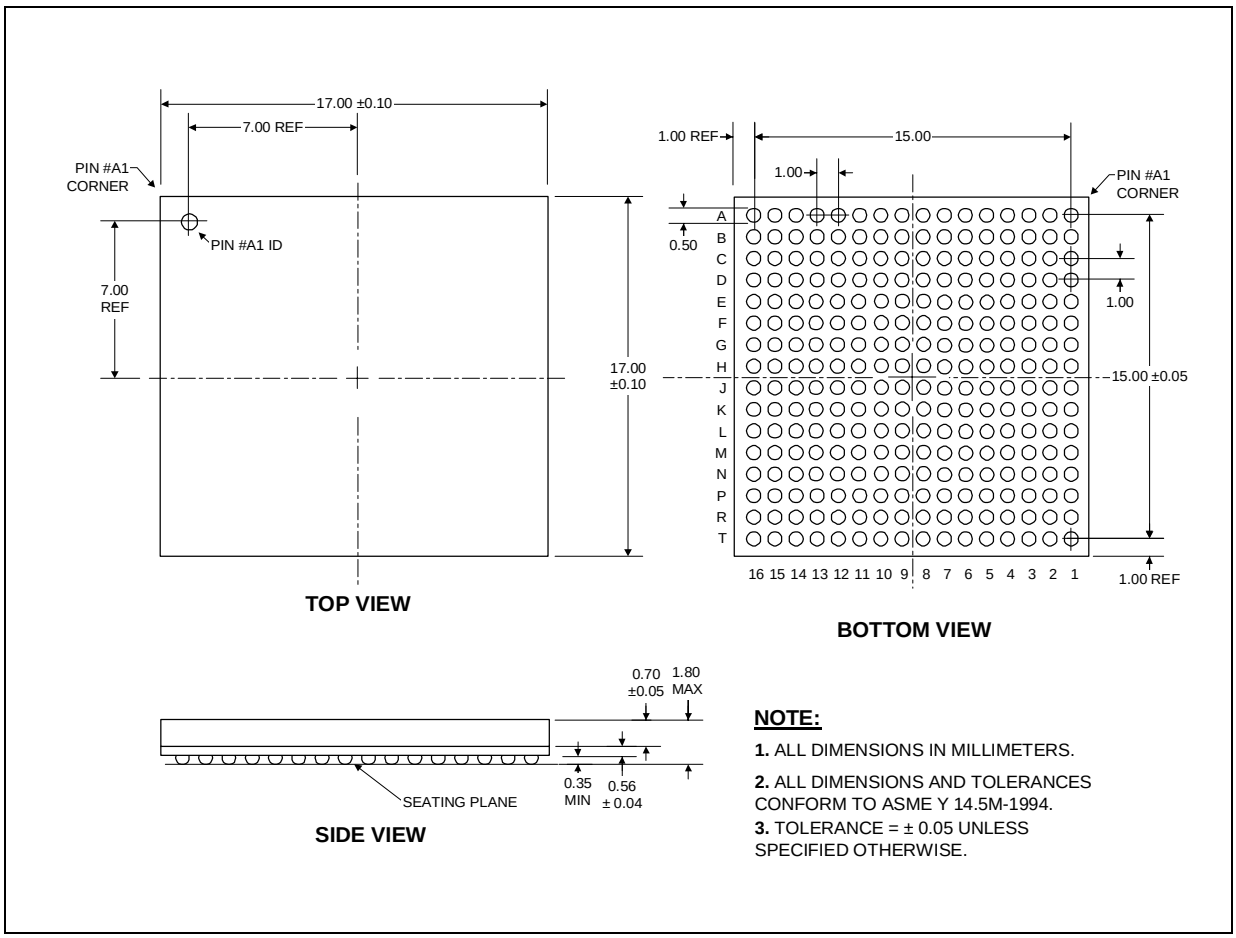
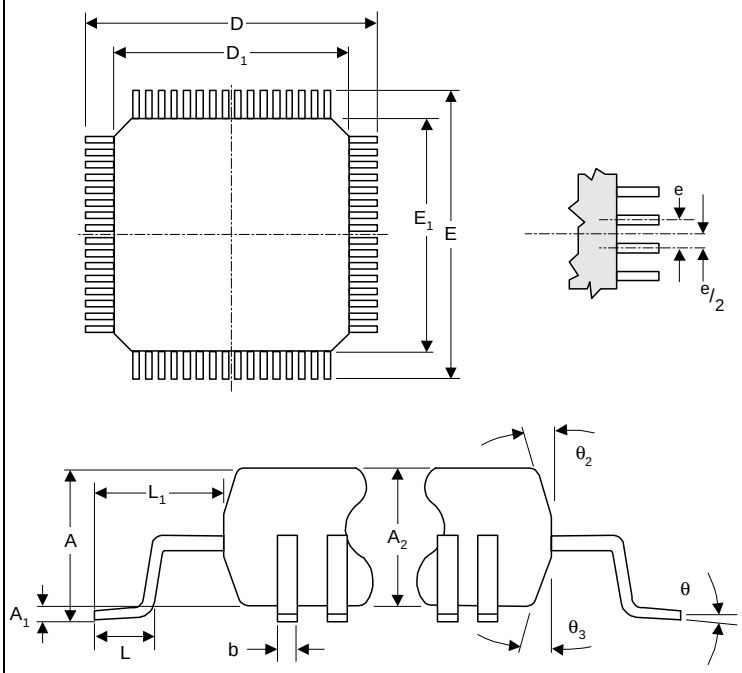


Figure 41. Intel® LXT3108 LIU 208 Pin QFP Mechanical Specifications



Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
θ_1	0°	7°
θ_2	5°	16°
θ_3	5°	16°

19.0 Glossary

Term Categories

Term	Term definition
ADC	Analog to Digital Converter
AFE	Analog Front End
AGC	Automatic Gain Control
ATWG	Arbitrary Transmit Wave Generation
BPV	Bi-Polar Violation
BSR	Boundary Scan Register
BYR	BYpass Register
CLAD	CLock ADapter
DAC	Digital to Analog Converter
DJA	Digital Jitter Attenuator
DSP	Digital Signal Processor
FIR	Finite Infinite Response
GUI	Graphical User Interface
HPS	Intel® Hitless Protection Switching, Intel® HPS
IADs	Integrated Access Devices
IDR	Device Identification Register
IMAPs	Integrated Multi-service Access Platforms
IR	Instruction Register
JTAG	Joint Test Action Group
LIU	Line Interface Unit
LH	Long Haul
LH/SH	Long Haul/Short Haul
LOS	Loss Of Signal
NRZ	Non-Return-to-Zero
PBGA	Plastic Ball Grid Array

POR	Power On Reset
PPR	Port Page Register
PPRB	Port Page Register Bank
PPS	Port Page Select
PTM	Intel® Pulse Template Matching, Intel® PTM
QFP	Quad Flat Pack
SH	Short Haul
TBD	To Be Determined
TAOS	Transmit All Ones
UI	Unit Interval