LXT380

Octal E1 Line Interface Unit

Datasheet

The LXT380 is an octal short haul Pulse Code Modulation (PCM) Line Interface Unit for ITU G.703 2.048 Mbit/sec. transmission systems. It incorporates eight independent receivers and eight independent transmitters in a single LQFP-144 or PBGA-160 package.

The transmit drivers maintain low impedance output during marks and spaces. The drivers also provide constant pulse amplitudes independent of any supply voltage variations. The LXT380 may be configured for unbalanced 75Ω or for balanced 120Ω systems without external component changes and exceeds latest ETSI return loss recommendations. An on chip pulse shaping circuit generates accurate transmit pulses independent of the transmit clock duty cycle.

The LXT380 features a differential data receiver architecture with high noise interference margin and uses peak detection and a variable threshold for reliable data recovery down to 500 mV or up to 12 dB of cable attenuation. The fully digital clock recovery PLL is referenced to a low frequency master clock of 2.048MHz. Each receiver incorporates an analog/digital Loss Of Signal (LOS) processor. The LXT380 features a "smart power" driver failure monitoring circuit in parallel to TTIP and TRING that reports secondary line shorts.

In addition, the LXT380 can be configured as 7 channel transceiver for Synchronous Digital Hierarchy (SDH) tributary port cards with G.772 compliant non intrusive protected monitoring points.

The fast power down mode of all transmitters allows the implementation of Hitless Protection Switching (HPS) application without the use of relays.

Product Features

- Octal E1 short haul transceiver per ITU G.703
- Single rail supply voltage of 3.3V with 5V I/O capability
- Low power consumption of <100mW per channel (typ.)
- 75Ω/120Ω TX operation without component changes
- Hitless Protection Switching (HPS)
- Driver short circuit current limiter (<50 mA RMS)
- Transmit return loss exceeds ETSI ETS 300166
- Selectable transmit pulse shape PLL
- Per channel clock recovery
- Selectable HDB3 line encoder/decoder
- On chip secondary driver short circuit monitoring circuit
- Provides protected monitoring points per ITU G.772
- Analog/digital and remote loopback testing function
- LOS per ITU G.775 and ETS 300 233 (selectable)
- 8 bit parallel or 4 wire serial control interface
- JTAG Boundary Scan test port per IEEE 1149.4
- Small footprint 144 Pin LQFP & 160 Pin PBGA Packages

As of January 15, 2001, this document replaces the Level One document known as *Octal E1 G.703 Transceiver*.

Order Number: 248995-001
January 2001

Datasheet

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Revision History

Revision	Date	Description

Applications

- E1 digital cross connects
- SDH E1 tributary interfaces
- Public switching trunk line interfaces
- Microwave transmission systems

Figure 1. LXT380 Block Diagram

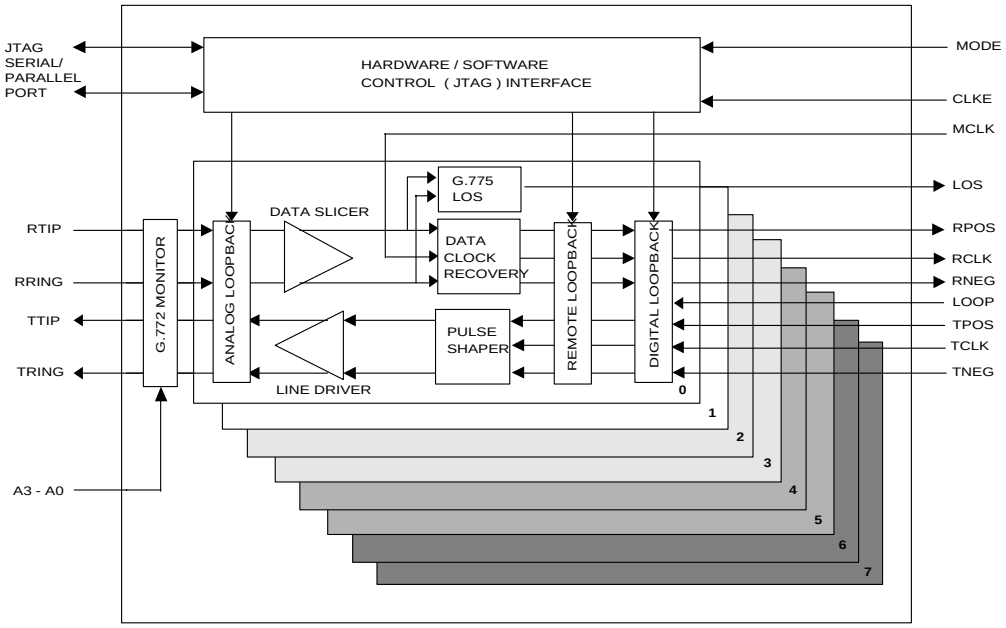
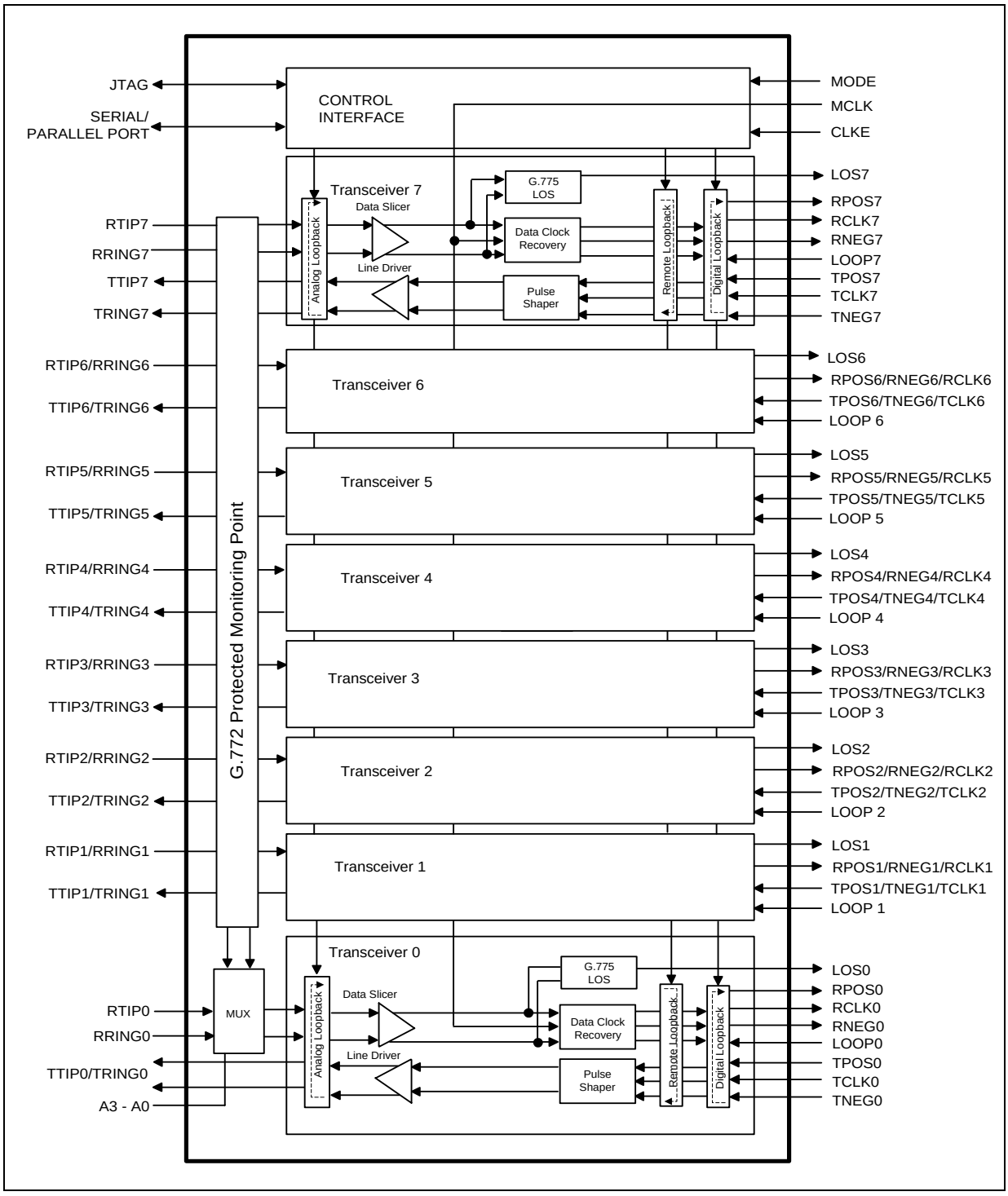
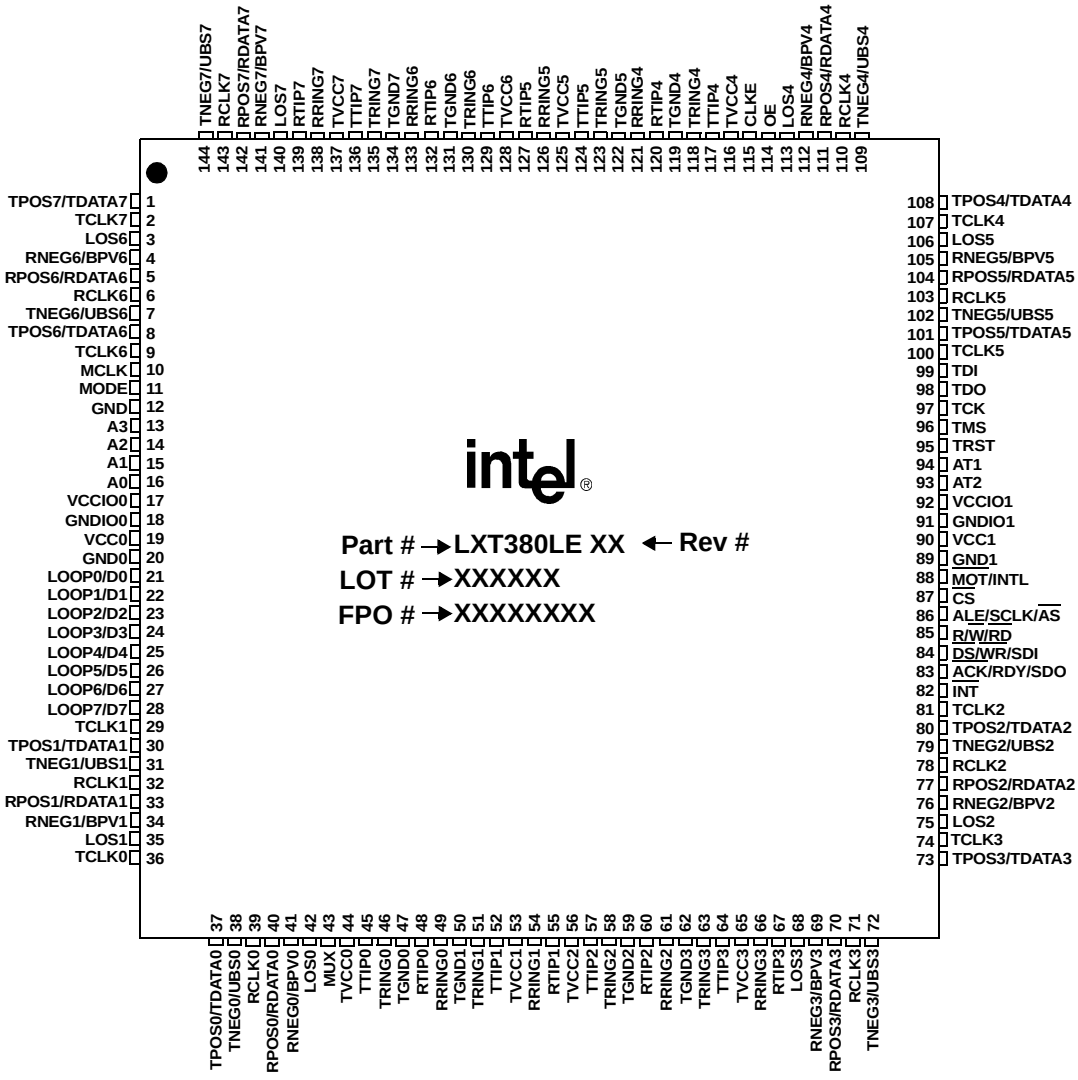


Figure 2. LXT380 Detailed Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 3. LXT380 Low-Profile Quad Flat Package (LQFP) Pin Assignments and Package Markings



Package Topside Markings

Marking	Definition
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Figure 4. LXT380 Plastic Ball Grid Array (PBGA) Package Pin Assignments

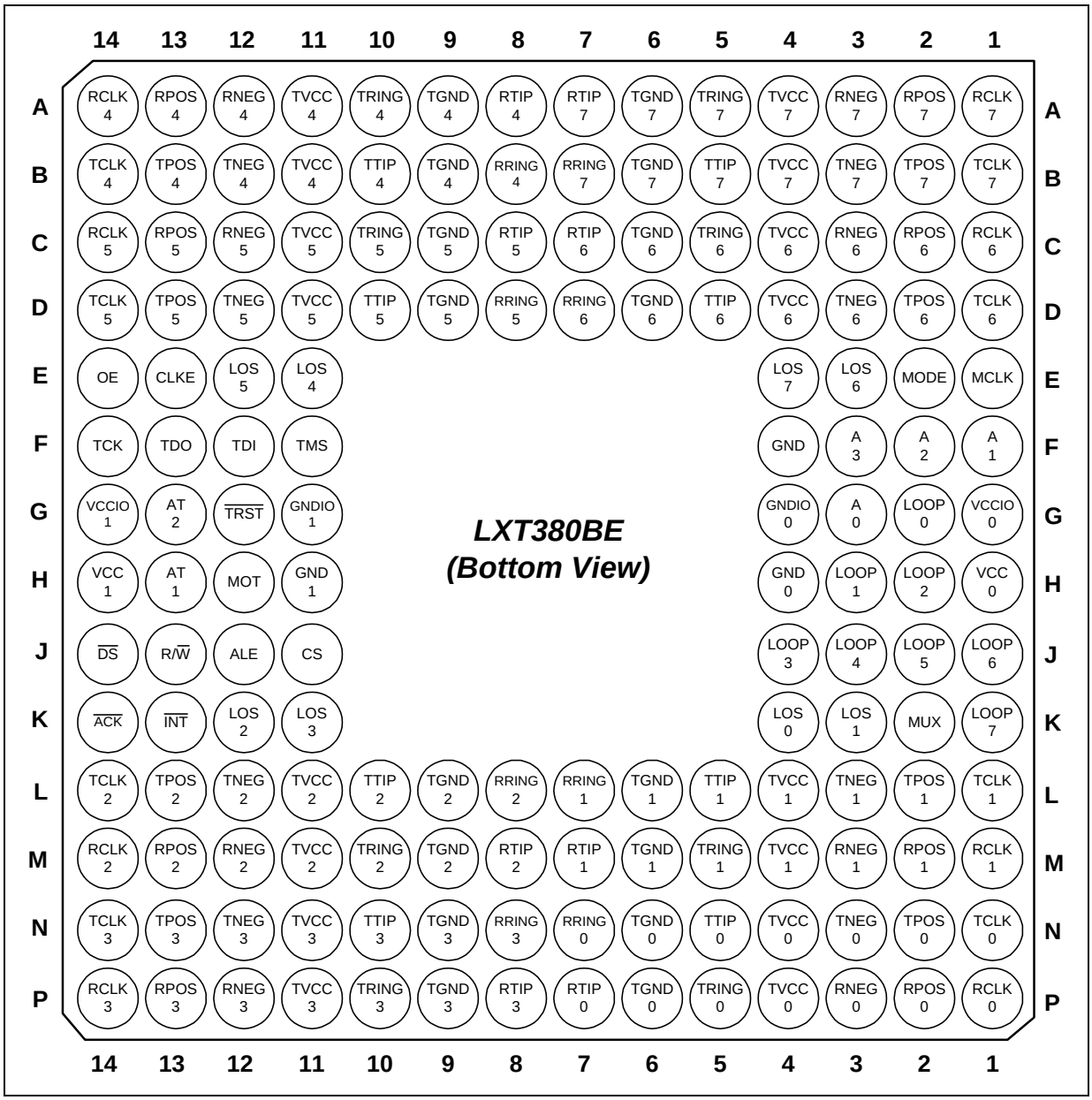


Table 1. LXT380 Pin Description

Pin # LQFP	Pin # PBGA	Symbol	I/O†	Description
1 1	B2 B2	TPOS7 TDATA7	DI DI	**Transmit Positive Data Input.** **Transmit Data Input.**
2	B1	TCLK7	DI	**Transmit Clock Input.** During normal operation, TCLK is active and TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is Low, the output drivers enter a low power High Z mode. If TCLK is High for more than 16 MCLK clock cycles, the pulse shaping circuit is disabled and the transmit output pulse widths are determined by the TPOS and TNEG duty cycles. If MCLK does not exist, an analog timer is used to determine if TCLK is High for at least 12 µ seconds in order to enable the above function. ***TCLK Operating Mode:*** Clocked — Normal operation H — TAOS (if MCLK is supplied) H — Disable transmit PLL (MCLK is not available) L — Driver outputs enter tri-State ***Note:*** The TAOS generator uses MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability.
3	E3	LOS6	DO	**Loss of Signal Output.** LOS output is High, indicating a loss of signal, when the incoming signal has no transitions for a specified time interval. The LOS condition is cleared and the output pin returns to Low when the incoming signal has sufficient number of transitions in a specified time interval. Details are in the LOS functional description.
4 4 5 5	C3 C3 C2 C2	RNEG6 BPV6 RPOS6 RDATA6	DO DO DO DO	**Receive Negative Data Output.** **Bipolar Violation Detect Output.** **Receive Positive Data Output.** **Receive Data Output.** ***Bipolar Mode:*** In clock recovery mode, these pins act as active high bipolar non return to zero (NRZ) receive signal outputs. A High signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. A High signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. These signals are valid on the falling or rising edges of RCLK depending on the CLKE input. In Data recovery Mode these pins act as RZ data receiver outputs. The output polarity is selectable with CLKE. Active High output polarity when CLKE is High and Active Low Polarity when CLKE is Low. RPOS and RNEG will go to the high impedance state when the MCLK pin is Low. ***Unipolar Mode:*** In uni-polar mode, LXT380 asserts BPV High if any in-service Line Code Violation is detected. RDATA acts as the receive data output. During a LOS condition, RPOS and RNEG will remain active.
6	C1	RCLK6	DO	**Receive Clock Output.** This pin provides the recovered clock from the signal received at RTIP and RRING. Under LOS conditions there is a transition from RCLK signal (derived from the recovered data) to MCLK signal at the RCLK output. If MCLK is High, the clock recovery circuit is disabled and RPOS and RNEG are internally connected to an EXOR that is fed to the RCLK output for external clock recovery applications. RCLK will be in high impedance state if the MCLK pin is Low.

† DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT380 Pin Description

Pin # LQFP	Pin # PBGA	Symbol	I/O†	Description
7 7 8 8	D3 D3 D2 D2	TNEG6 UBS6 TPOS6 TDATA6	DI DI DI DI	**Transmit Negative Data Input.** **Unipolar/Bipolar Select Input.** **Transmit Positive Data Input.** **Transmit Data Input.** ***Bipolar Mode:*** TPOS/TNEG are active high NRZ inputs. TPOS indicates the transmission of a positive pulse whereas TNEG indicates the transmission of a negative pulse. TPOS TNEG Selection 0 0 Space 1 0 Positive Mark 0 1 Negative Mark 1 1 Space ***Unipolar Mode:*** When TNEG/UBS is pulled High for more than 16 consecutive TCLK clock cycles, unipolar I/O with HDB3 encode/decode is selected. TDATA is the data input in unipolar I/O mode.
9	D1	TCLK6	DI	**Transmit Clock Input.**
10	E1	MCLK	DI	**Master Clock Input.** This 2.048 Mhz reference clock is used to generate several internal reference signals: • Timing reference for the integrated high performance clock recovery unit • Generation of RCLK signal during a loss of signal condition • REFERENCE clock during a blue alarm transmit all ones condition • Reference timing for the parallel processor wait state generation logic If MCLK is High, the PLL clock recovery circuit is disabled. In this mode the LXT380 operates as simple data receiver. ***Note:*** Wait state generation via RDY/$\overline{ACK}$ is not available in this mode. If MCLK is Low, the complete receive path is powered down and the output pins RCLK, RPOS and RNEG are switched to Tri-state mode. MCLK is not required if the LXT380 is used as simple analog front-end without clock recovery. MCLK should be an independent free-running reference clock.
11	E2	MODE	DI	**Mode Select Input.** This pin is used to select the operating mode of the LXT380. In Hardware Mode, the parallel processor interface is disabled and hardwired pins are used to control configuration and report status. In Parallel Host Mode, the parallel port interface pins are used to control configuration and report status. In Serial Host Mode, the serial interface pins: SDI, SDO, SCLK and $\overline{CS}$ are used. MODE Operating Mode L Hardware Mode H Parallel Mode VCCIO ÷2 Serial Host Mode For Serial Host Mode, this pin should connect to a resistive divider consisting of two 10 kΩ resistors across VCCIO and Ground.
12	F4	GND	DI	**Ground.** This pin must be connected to Ground.

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Table 1. LXT380 Pin Description

<table>
<tr><th>Pin # LQFP</th><th>Pin # PBGA</th><th>Symbol</th><th>I/O†</th><th>Description</th></tr>
<tr><td>13
14
15
16</td><td>F3
F2
F1
G3</td><td>A3
A2
A1
A0</td><td>DI
DI
DI
DI</td><td>Protected Monitoring/Address Select Inputs.
Hardware Mode
In hardware mode, these pins are used to select a specific port for non intrusive monitoring. During protection monitoring receiver 0 inputs are internally connected to a specific transmit or receive port. Receiver 0 routes the data from the selected port to its data and clock recovery circuits. The data on the monitor port can be routed to TTIP0/TRING0 by activating the remote loopback for channel 0. In addition, the recovered clock and data can be observed at the RCLK0/RPOS0/RNEG0 outputs.
If A0, A1, and A2 are Low, the LXT380 is configured as octal line transceiver without monitoring capability.
<table>
<tr><th>A3</th><th>A2</th><th>A1</th><th>A0</th><th>Selection</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>No Protection Monitoring</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Receiver 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Receiver 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Receiver 3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Receiver 4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Receiver 5</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Receiver 6</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Receiver 7</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>No Protection Monitoring</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Transmitter 1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Transmitter 2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Transmitter 3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Transmitter 4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Transmitter 5</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Transmitter 6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Transmitter 7</td></tr>
</table>
Transmitter monitoring is not supported when the respective channel is set to analog loopback mode.
Host Mode
In non-multiplexed host mode, these pins function as non-multiplexed address pins.</td></tr>
<tr><td>17</td><td>G1</td><td>VCCIO0</td><td>S</td><td>Power (I/O).</td></tr>
<tr><td>18</td><td>G4</td><td>GNDIO 0</td><td>S</td><td>Ground (I/O).</td></tr>
<tr><td>19</td><td>H1</td><td>VCC0</td><td>S</td><td>Power (Core).</td></tr>
<tr><td>20</td><td>H4</td><td>GND0</td><td>S</td><td>Ground (Core).</td></tr>
<tr><td colspan="5">† DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.</td></tr>
</table>

Table 1. LXT380 Pin Description

Pin # LQFP	Pin # PBGA	Symbol	I/O†	Description
21 22 23 24 25 26 27 28	G2 H3 H2 J4 J3 J2 J1 K1	LOOP0/ D0 LOOP1/ D1 LOOP2/ D2 LOOP3/ D3 LOOP4/ D4 LOOP5/ D5 LOOP6/ D6 LOOP7/ D7	DI/ O DI/ O DI/ O DI/ O DI/ O DI/ O DI/ O DI/ O	**Loopback Mode Select/Parallel Data bus Input & Output.** ***Host mode:*** When a non-multiplexed microprocessor interface is selected, these pins function as a bi-directional 8-bit data port. When a multiplexed microprocessor interface is selected, these pins carry both bi-directional 8-bit data and address inputs A0–A7. In serial Mode, D0-7 should be grounded. ***Hardware mode:*** These pins are inputs that select the loopback mode for transceiver ports 0-7 respectively as follows: Normal operation (no loopback) is selected when pin is left open (unconnected). Remote loopback mode is selected when pin is Low. In this mode, data on TPOS and TNEG is ignored and data received on RTIP and RRING is looped around and retransmitted on TTIP and TRING. Analog local loopback mode is selected when pin is High. In this mode, data received on RTIP and RRING is ignored and data transmitted on TTIP and TRING is internally looped around and routed back to the receive inputs. ***Note:*** When these inputs are left open, they stay in a high impedance state. Therefore, the layout design should not route signals with fast transitions near the LOOP pins. This practice will minimize capacitive coupling.
29	L1	TCLK1	DI	**Transmit Clock Input.**
30 30 31 31	L2 L2 L3 L3	TPOS1 TDATA1 TNEG1 UBS1	DI DI DI DI	**Transmit Positive Data Input.** **Transmit Data Input.** **Transmit Negative Data Input.** **Unipolar/Bipolar Select Input.**
32	M1	RCLK1	DO	**Receive Clock Output.**
33 33 34 34	M2 M2 M3 M3	RPOS1 RDATA 1 RNEG1 BPV1	DO DO DO DO	**Receive Positive Data Output.** **Receive Data Output.** **Receive Negative Data Output.** **Bipolar Violation Detect Output.**
35	K3	LOS1	DO	**Loss of Signal Output.**
36	N1	TCLK0	DI	**Transmit Clock Input.**
37 37 38 38	N2 N2 N3 N3	TPOS0 TDATA0 TNEG0 UBS0	DI DI DI DI	**Transmit Positive Data Input.** **Transmit Data Input.** **Transmit Negative Data Input.** **Unipolar /Bipolar Select Input.**
39	P1	RCLK0	DO	**Receive Clock Output.**

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Pin # LQFP	Pin # PBGA	Symbol	I/O†	Description
40 40 41 41	P2 P2 P3 P3	RPOS0 RDATA 0 RNEG0 BPV0	DO DO DO DO	**Receive Positive Data.** **Receive Data Output.** **Receive Negative Data.** **Bipolar Violation Detect.**
42	K4	LOS0	DO	**Loss of Signal Output.**
43	K2	MUX	DI	**Multiplexed/Non-Multiplexed Select Input.** When Low, the parallel host interface operates in non-multiplexed mode. When High, the parallel host interface operates in multiplexed mode. MODE Operating Mode L Non-Multiplexed Mode H Multiplexed Mode
44	N4, P4	TVCC0	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
45 46	N5 P5	TTIP0 TRING0	AO AO	**Transmit Tip Output.** **Transmit Ring Output.** These pins are differential line driver outputs designed to drive 75 Ω unbalanced or 120 Ω balanced cables with a 1:2 transformer and two 11 Ω series resistors. TRING and TTIP will be in high impedance state if the TCLK pin is Low.
47	N6, P6	TGND0	S	**Transmit Driver Ground.** Ground pin for the output driver.
48 49	P7 N7	RTIP0 RRING 0	AI AI	**Receive TIP Input.** **Receive Ring Input.** These pins are the inputs to the differential line receiver. Data and clock are recovered and output on the RPOS/RNEG and RCLK pins.
50	L6, M6	TGND1	S	**Transmit Driver Ground.**
51 52	M5 L5	TRING1 TTIP1	AO AO	**Transmit Ring Output.** **Transmit Tip Output.**
53	L4, M4	TVCC1	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
54 55	L7 M7	RRING 1 RTIP1	AI AI	**Receive Ring Input.** **Receive Tip Input.**
56	L11, M11	TVCC2	S	**Transmit Driver Power Supply.**
57 58	L10 M10	TTIP2 TRING2	AO AO	**Transmit Tip Output.** **Transmit Ring Output.**
59	L9, M9	TGND2	S	**Transmit Driver Ground.**
60 61	M8 L8	RTIP2 RRING 2	AI AI	**Receive TIP Input.** **Receive Ring Input.**

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Pin # LQFP	Pin # PBGA	Symbol	I/O†	Description
62	N9, P9	TGND3	S	**Transmit Driver Ground.** Ground pin for the output driver.
63 64	P10 N10	TRING3 TTIP3	AO AO	**Transmit Ring.** **Transmit Tip Output.**
65	N11, P11	TVCC3	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
66 67	N8 P8	RRING 3 RTIP3	AI AI	**Receive Ring Input.** **Receive Tip Input.**
68	K11	LOS3	DO	**Loss of Signal Output.**
69 69 70 70	P12 P12 P13 P13	RNEG3 BPV3 RPOS3 RDATA 3	DO DO DO DO	**Receive Negative Data Output.** **Bipolar Violation Detect Output.** **Receive Positive Data Output.** **Receive Data Output.**
71	P14	RCLK3	DO	**Receive Clock Output.**
72 72 73 73	N12 N12 N13 N13	TNEG3 UBS3 TPOS3 TDATA3	DI DI DI DI	**Transmit Negative Data Input.** **Unipolar/Bipolar Select Input.** **Transmit Positive Data Input.** **Transmit Data Input.**
74	N14	TCLK3	DI	**Transmit Clock Input.**
75	K12	LOS2	DO	**Loss of Signal Output.**
76 76 77 77	M12 M12 M13 M13	RNEG2 BPV2 RPOS2 RDATA 2	DO DO DO DO	**Receive Negative Data Output.** **Bipolar Violation Detect Output.** **Receive Positive Data Output.** **Receive Data Output.**
78	M14	RCLK2	DO	**Receive Clock Output.**
79 79 80 80	L12 L12 L13 L13	TNEG2 UBS2 TPOS2 TDATA2	DI DI DI DI	**Transmit Negative Data Input.** **Unipolar/Bipolar Select Input.** **Transmit Positive Data Input.** **Transmit Data Input.**
81	L14	TCLK2	DI	**Transmit Clock Input.**
82	K13	INT	DO	**Interrupt Output.** This active Low, maskable, open drain output requires an external 10k pull up resistor. $\overline{\text{INT}}$ goes Low to flag the host when the LXT380 changes state. When the status memory registers are read the interrupt is cleared.

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Table 1. LXT380 Pin Description

Pin # LQFP	Pin # PBGA	Symbol	I/O†	Description
83 83 83	K14 K14 K14	ACK RDY SDO	DO DO DO	**Data Transfer Acknowledge Output.** **Ready Output.** **Serial Data Output.** In Motorola Mode a Low signal during a databus read operation indicates that the information is valid. A Low signal during a write operation acknowledges that a data transfer into the addressed register has been accepted (acknowledge signal). In Motorola Mode wait states only occur if a write cycle immediately follows a previous read or write cycle (e.g. read modify write). In Intel mode a High signal acknowledges that a register access operation has been completed (Ready Signal). A Low signal on this pin signals that a data transfer operation is in progress. The pin goes tristate after completion of a bus cycle. In Serial Host mode, if CLKE is High, SDO is valid on the rising edge of SCLK. If SCLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes into high Z state during a serial port write access.
84 84 84	J14 J14 J14	DS WR SDI	DI DI DI	**Data Strobe Input.** **Write Enable Input.** **Serial Data Input.** This pin acts as data strobe in Motorola mode and as Write Enable in Intel mode. In serial mode, this pin is used as Serial Data Input.
85 85	J13 J13	R/W RD	DI DI	**Read/Write Input.** **Read Enable Input.** This pin functions as the read/write signal in Motorola mode and as the Read Enable in Intel mode.
86 86 86	J12 J12 J12	ALE SCLK AS	DI DI DI	**Address Latch Enable Input.** **Shift Clock Input.** **Address Strobe** The address on the multiplexed address/data bus is clocked into the device with the falling edge of ALE. In serial Host mode, this pin acts as serial shift clock. In Motorola mode, this pin acts a an active Low address strobe.
87	J11	$\overline{CS}$	DI	**Chip Select Input**. This active Low input is used to access the serial/parallel interface. For each read or write operation, $\overline{CS}$ must transition from High to Low and remain Low.
88	H12	$\overline{MOT}$/ INTL	DI	**Motorola/Intel Select Input.** When low, the host interface is configured for Motorola microcontrollers. When High, the host interface is configured for Intel microcontrollers. MOT/INTL Operating Mode L Motorola Mode H Intel Mode
89	H11	GND1	S	**Ground (Core).**
90	H14	VCC1	S	**Power (Core).**
91	G11	GNDIO 1	S	**Ground (I/O).**
92	G14	VCCIO1	S	**Power (I/O).**
93	G13	AT2	AO	**JTAG Analog Output Test Port 2.**

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Table 1. LXT380 Pin Description

Pin # LQFP	Pin # PBGA	Symbol	I/O†	Description
94	H13	AT1	AI	**JTAG Analog Input Test Port 1.**
95	G12	$\overline{\text{TRST}}$	DI	**JTAG Controller Reset Input.** Input is used to reset JTAG controller. $\overline{\text{TRST}}$ is pulled up internally and may be left disconnected.
96	F11	TMS	DI	**JTAG Test Mode Select Input.** Used to control the test logic state machine. Sampled on rising edge of TCK. TMS is pulled up internally and may be left disconnected.
97	F14	TCK	DI	**JTAG Clock Input.** Clock input for JTAG. Connect to GND when not used.
98	F13	TDO	DO	**JTAG Data Output.** Test Data Output for JTAG. Used for reading all serial configuration and test data from internal test logic. Updated on falling edge of TCK.
99	F12	TDI	DI	**JTAG Data Input.** Test Data input for JTAG. Used for loading serial instructions and data into internal test logic. Sampled on rising edge of TCK. TDI is pulled up internally and may be left disconnected.
100	D14	TCLK5	DI	**Transmit Clock Input.**
101 101 102 102	D13 D13 D12 D12	TPOS5 TDATA5 TNEG5 UBS5	DI DI DI DI	**Transmit Positive Data Input.** **Transmit Data Input.** **Transmit Negative Data Input.** **Unipolar/Bipolar Select Input.**
103	C14	RCLK5	DO	**Receive Clock Output.**
104 104 105 105	C13 C13 C12 C12	RPOS5 RDATA 5 RNEG5 BPV5	DO DO DO DO	**Receive Positive Data Output.** **Receive Data Output.** **Receive Negative Data Output.** **Bipolar Violation Detect Output.**
106	E12	LOS5	DO	**Loss of Signal Output.**
107	B14	TCLK4	DI	**Transmit Clock Input.**
108 108 109 109	B13 B13 B12 B12	TPOS4 TDATA4 TNEG4 UBS4	DI DI DI DI	**Transmit Positive Data Input.** **Transmit Data Input.** **Transmit Negative Data Input.** **Unipolar/Bipolar Select Input.**
110	A14	RCLK4	DO	**Receive Clock Output.**
111 111 112 112	A13 A13 A12 A12	RPOS4 RDATA 4 RNEG4 BPV4	DO DO DO DO	**Receive Positive Data Output.** **Receive Data Output.** **Receive Negative Data Output.** **Bipolar Violation Detect Output.**
113	E11	LOS4	DO	**Loss of Signal Output.**
114	E14	OE	DI	**Output Driver Enable Input.** If this pin is asserted Low all analog driver outputs immediately enter a high impedance mode to support redundancy applications without external mechanical relays. All other internal circuitry stay active.

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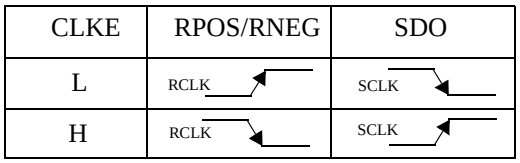
Pin # LQFP	Pin # PBGA	Symbol	I/O†	Description
115	E13	CLKE	DI	**Clock Edge Select Input.** In clock recovery mode, setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK and SDO to be valid on the rising edge of SCLK. Setting CLKE Low makes RPOS and RNEG to be valid on the rising edge of RCLK and SDO to be valid on the falling edge of SCLK. In Data recovery Mode, RPOS/RNEG are active High output polarity when CLKE is High and active low polarity when CLKE is Low. 
116	A11, B11	TVCC4	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
117 118	B10 A10	TTIP4 TRING4	AO AO	**Transmit Tip Output.** **Transmit Ring Output.**
119	A9, B9	TGND4	S	**Transmit Driver Ground.** Ground pin for the output driver.
120 121	A8 B8	RTIP4 RRING 4	AI AI	**Receive Tip Input.** **Receive Ring Input.**
122	C9, D9	TGND5	S	**Transmit Driver Ground.** Ground pin for the output driver.
123 124	C10 D10	TRING5 TTIP5	AO AO	**Transmit Ring Output.** **Transmit Tip Output.**
125	C11, D11	TVCC5	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
126 127	D8 C8	RRING 5 RTIP5	AI AI	**Receive Ring Input.** **Receive Tip Input.**
128	C4, D4	TVCC6	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
129 130	D5 C5	TTIP6 TRING6	AO AO	**Transmit Tip Output.** **Transmit Ring Output.**
131	C6, D6	TGND6	S	**Transmit Driver Ground.** Ground pin for the output driver.
132 133	C7 D7	RTIP6 RRING 6	AI AI	**Receive Tip Input.** **Receive Ring Input.**
134	A6, B6	TGND7	S	**Transmit Driver Ground.** Ground pins for the output driver.
135 136	A5 B5	TRING7 TTIP7	AO AO	**Transmit Ring Output.** **Transmit Tip Output.**
137	A4, B4	TVCC7	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.

† DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT380 Pin Description

Pin # LQFP	Pin # PBGA	Symbol	I/O†	Description
138 139	B7 A7	RRING7 RTIP7	AI AI	**Receive Ring Input.** **Receive Tip Input.**
140	E4	LOS7	DO	**Loss of Signal Output.**
141 141 142 142	A3 A3 A2 A2	RNEG7 BPV7 RPOS7 RDATA7	DO DO DO DO	**Receive Negative Data Output.** **Bipolar Violation Detect Output.** **Receive Positive Data Output.** **Receive Data Output.**
143	A1	RCLK7	DO	**Receive Clock Output.**
144 144	B3 B3	TNEG7 UBS7	DI DI	**Transmit Negative Data Input.** **Unipolar/Bipolar Select Input.**

† DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

2.0 Functional Description

Figure 4 on page 10 is a block diagram of the LXT380. The LXT380 is a fully integrated octal line interface unit designed for G.703 2.048 Mbps applications.

Each transceiver front end interfaces with four lines, one pair for transmit, one pair for receive. These two lines comprise a digital data loop for full duplex transmission.

The LXT380 can be controlled through hard-wired pins (Hardware mode) or by a microprocessor through a serial or parallel interface (Host mode).

The transmitter timing reference is TCLK, and the receiver reference clock is MCLK. The LXT380 is designed to operate without any reference clock when used as an analog front-end (line driver and data recovery). MCLK is mandatory if the on chip clock recovery capability is used. All eight clock recovery circuits share the same reference clock defined by the MCLK input signal.

2.1 Initialization

During power up, the transceiver remains static until the power supply reaches approximately 60% of VCC. During power-up, an internal reset sets all registers to 0 and resets the status and state machines for the LOS.

2.1.1 Reset Operation

Reading or writing the reset register (RES) initiates a 1 microsecond reset cycle. This operation sets all LXT380 registers to their default values.

2.2 Receiver

The eight receivers in the LXT380 are identical. The following paragraphs describe the operation of a single receiver.

The receive signal is input to the LIU via a 1:1 transformer. A peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers to ensure optimum signal-to-noise ratio.

The receiver is capable of accurately recovering signals with up to 12dB of attenuation (from 2.37 V nominal), corresponding to a received signal level of approximately 500 mV. Regardless of received signal level, the peak detectors are held above a minimum level of 150 mV to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data ports, the timing recovery section, and to the receive monitor. The timing recovery circuit provides an input jitter tolerance significantly better than required by G.823 as shown in Figure 31 on page 65.

Recovered data is active High and output at RPOS and RNEG, The recovered clock is output at RCLK. RPOS/RNEG validation is pin selectable (CLKE).

2.2.1 Loss Of Signal Detector

The loss of signal detector in the LXT380 uses a dedicated analog and digital loss of signal detection circuit. It is independent of its internal data slicer comparators. and complies to the latest ITU G.775 recommendations. Under software control, the detector can be configured to comply to the ETSI ETS 300 233 specifications. In hardware mode, the LXT380 supports LOS per G.775.

2.2.1.1 Clock and Data Recovery Mode

The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. In G.775 mode a consecutive sequence of 32 zeros sets the LOS signal. The recovered clock is replaced by MCLK at the RCLK output with a minimum amount of phase errors. (MCLK is required for receive operation).

In G.775 mode a loss of signal is detected if the signal is below 200 mV (typical) for 32 consecutive pulse intervals. When the received signal reaches 12.5% ones density (4 marks in a sliding 32-bit period) with no more than 15 consecutive zeros and the signal level exceeds 250 mV (typical), the LOS flag is reset and another transition replaces MCLK with the recovered clock at RCLK. RPOS/RNEG will reflect the data content at the receiver input during the entire LOS detection period for that channel.

In ETSI 300 233 mode a loss of signal is detected if the signal is below 200mV for 2048 consecutive intervals (1 ms.) The LOS condition is cleared and the output pin returns to Low when the incoming signal has transitions when the signal level is equal or greater than 250mV for more than 32 consecutive pulse intervals.

2.2.1.2 Data Recovery Mode

In data recovery mode, the LOS digital timing is derived from a internal self timed circuit. RPOS/ RNEG stay active during loss of signal. The analog LOS detector complies with ITU-G.775 recommendation. The LXT380 monitors the incoming signal amplitude. Any signal below 200mV for more than 30µs (typical) will assert the corresponding LOS pin. The LOS condition is cleared when the signal amplitude rises above 250mV. The LXT380 requires more than 10 and less than 255 bit periods to declare a LOS condition in accordance to ITU G.775.

2.3 In Service Code Violation Monitoring

In unipolar I/O mode, the LXT380 reports bipolar violations on RNEG/BPV for one RCLK period for every HDB3 code violation that is not part of the zero code substitution rules.

2.4 Transmitter

The eight low power transmitters of the LXT380 are identical.

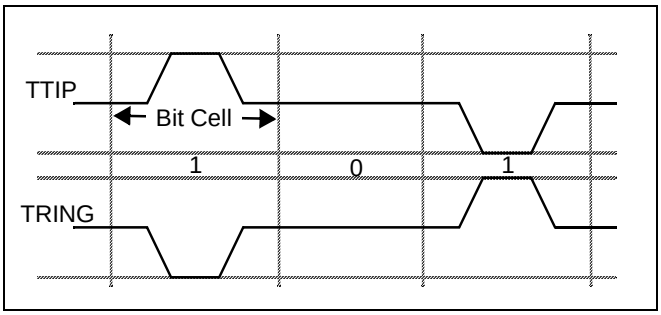
Transmit data applied to TPOS/TNEG is clocked serially into the device. Input synchronization is supplied by the transmit clock (TCLK). The TPOS/TNEG inputs are sampled on the falling edge of TCLK. Refer to MCLK and TCLK timing characteristics.

Unipolar I/O and HDB3 encoding/decoding is selected by pulling TNEG High for more than 16 TCLK clock cycles.

Each output driver is supplied by a separate power supply: TVCC and TGND. This allows each transmitter power supply to be de-coupled independently. The LXT380 transmits data as a 50% AMI line code as shown in Figure 5.

The transmit pulse shaper is bypassed if no MCLK is supplied while TCLK is pulled High. In this case TPOS and TNEG control the pulse width and polarity on TTIP and TRING. With MCLK supplied and TCLK pulled High the driver enters TAOS (Transmit All Ones pattern). TAOS is inhibited during Remote Loopback.

Figure 5. 50% AMI Coding



2.4.1 Transmit Pulse Shaping

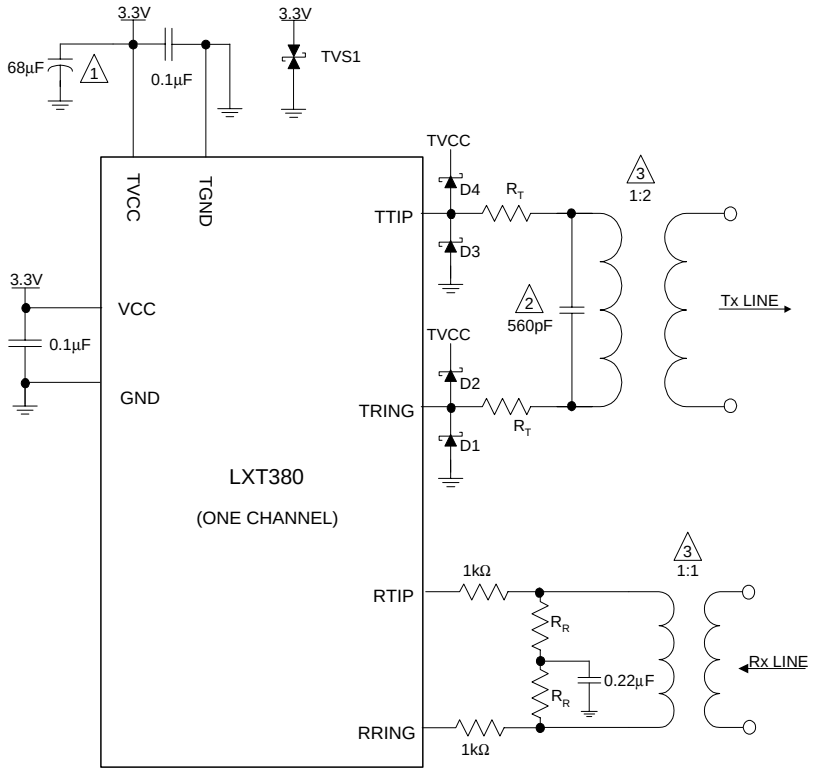
The transmitted pulse shape is internally generated using a high speed D/A converter. Shaped pulses are further applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance regardless of whether it is driving marks, spaces or if it is in transition. This well controlled dynamic impedance provides excellent return loss when used with external precision resistors (± 1% accuracy) in series with the transformer.

The LXT380 produces 2.048 MHz pulses for both 75 Ω coaxial (2.37 V) or 120 Ω shielded twisted-pair (3.0 V) lines through an output transformer with a 1:2 step up pulse transformer and 11 Ω series resistors. No transmit component changes are required in 75 Ω or 120 Ω operation as the output driver dynamically adjusts its output pulse amplitude.

2.5 Line Protection

As shown in Figure 6, the 1 kΩ series resistors protect the receiver against current surges coupled into the device. Due to the high receiver impedance (70 kΩ typical), the resistors do not affect the receiver sensitivity. In the transmit side, Schottky diodes D1-D4 protect the output driver. While not mandatory for normal operation, these protection elements are strongly recommended to improve the design robustness.

Figure 6. External Transmit/Receive Line Circuitry



COMPONENT	APPLICATION	
	75Ω COAX	120Ω TWISTED PAIR
R_T	11 Ω ±1%	11 Ω ±1%
R_R	37.5 Ω ±1%	60 Ω ±1%
D1 - D4	INTERNATIONAL RECTIFIER 11DQ04 or 10BQ060 MOTOROLA MBR0540T1	
TVS1	SGS-THOMSON SMLVT 3V3 3.3V	

1 Common decoupling capacitor for all TVCC and TGND pins.

2 Typical value. Adjust for actual board parasitics to obtain optimum return loss.

3 Transformer turns ratio tolerance is ± 2%. See Test Specifications Section for transformer specifications.

2.6 Driver Failure Monitor

The LXT380 transceiver incorporates a unique internal smart power Driver Failure Monitor (DFM) in parallel with TTIP and TRING that is capable of detecting secondary line shorts. This feature is available in the serial and parallel host modes but not available in the hardware mode of operation.

A capacitor, charged via a measure of the driver output current and discharged by a measure of the maximum allowable current, is used to detect a secondary line short failure. Secondary shorted lines draw excess current, overcharging the cap. When the capacitor charge deviates outside the nominal charge window, a driver short circuit fail (DFM) is reported in the respective register by setting an interrupt. During a long string of spaces, a short-induced overcharge eventually bleeds off, clearing the DFM flag.

Note: Un-terminated lines of adequate length may effectively behave as short-circuits as seen by the driver and therefore trigger the DMF. Under these circumstances, the user should either disable the alarm or ensure that the driver is not transmitting marks.

2.7 Loopbacks

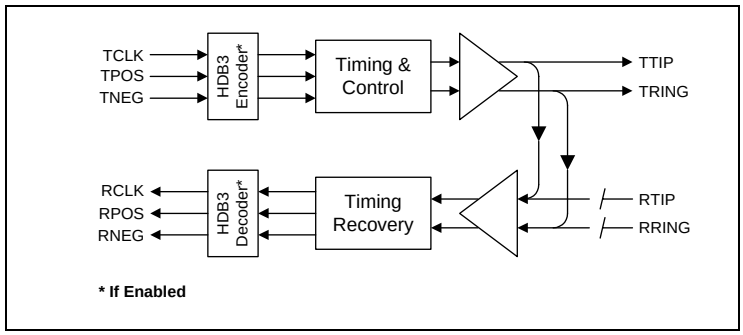
The LXT380 offers three loopback modes for diagnostic purposes. In hardware mode, the loopback mode is selected with the LOOPn pins. In host mode, the ALOOP, DLOOP and RLOOP registers are employed.

2.7.1 Analog Loopback

When selected, the transmitter outputs (TTIP & TRING) are connected internally to the receiver inputs (RTIP & RRING) as shown in Figure 7. Data and clock are output at RCLK, RPOS & RNEG pins for the corresponding transceiver.

Note: Signals on the RTIP & RRING pins are ignored during analog loopback.

Figure 7. Analog Loopback

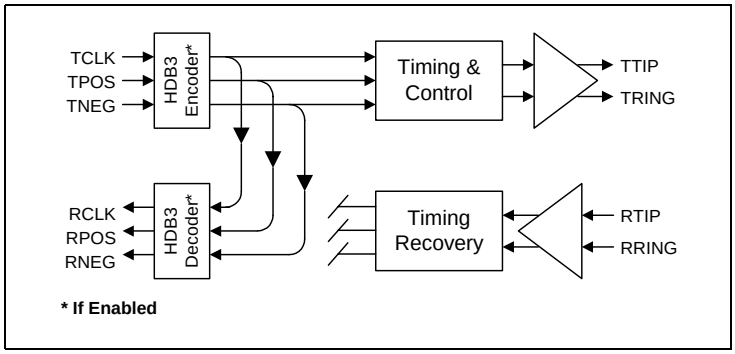


2.7.2 Digital Loopback

The digital loopback function is available in host mode only. When selected, the transmit clock and data inputs (TCLK, TPOS & TNEG) are looped back and output on the RCLK, RPOS & RNEG pins. The data presented on TCLK, TPOS & TNEG is also output on the TTIP & TRING pins.

Note: Signals on the RTIP & RRING pins are ignored during digital loopback. See Figure 8.

Figure 8. Digital Loopback



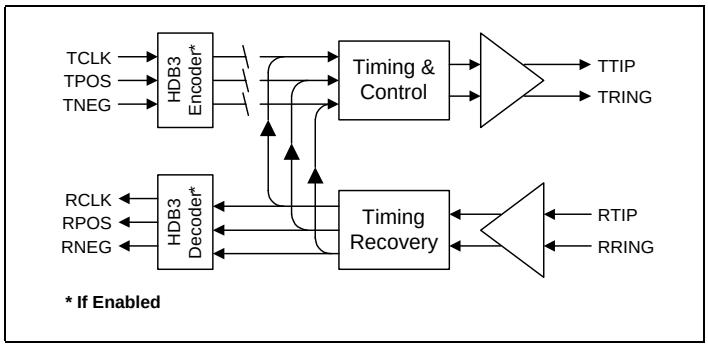
2.7.3 Remote Loopback

During remote loopback, the RCLK, RPOS & RNEG outputs routed to the transmit circuits and output on the TTIP & TRING pins.

Note: Input signals on the TPOS & TNEG pins are ignored during remote loopback.

In clock recovery mode, TCLK will tristate the output driver if held Low. See Figure 9.

Figure 9. Remote Loopback



2.7.4 Transmit All Ones (TAOS)

In Hardware mode, the TAOS mode is set by pulling TCLK High for more than 16 MCLK cycles. In host mode, TAOS mode is set by asserting the corresponding bit in the TAOS Register. In addition, automatic ATS insertion (in case of LOS) may be set using the ATS Register.

Note: The TAOS generator uses MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability.

Figure 10. TAOS Data Path

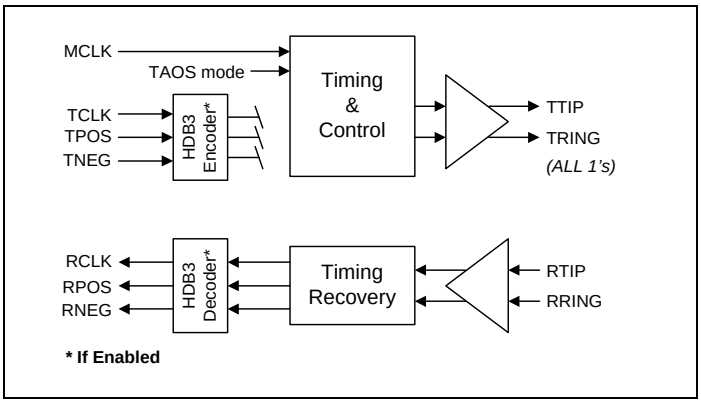


Figure 11. TAOS with Digital Loopback

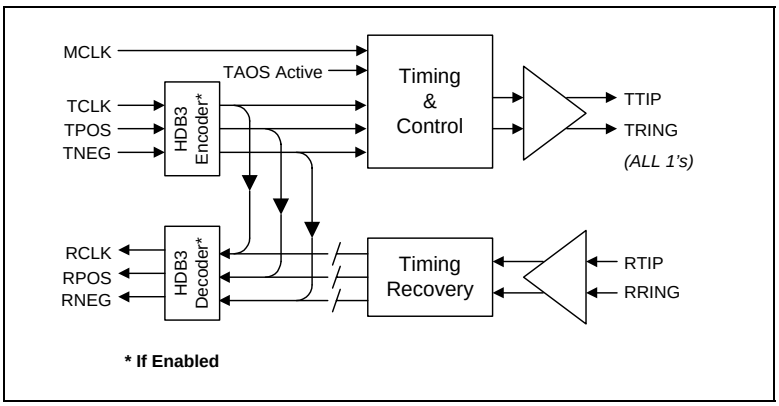
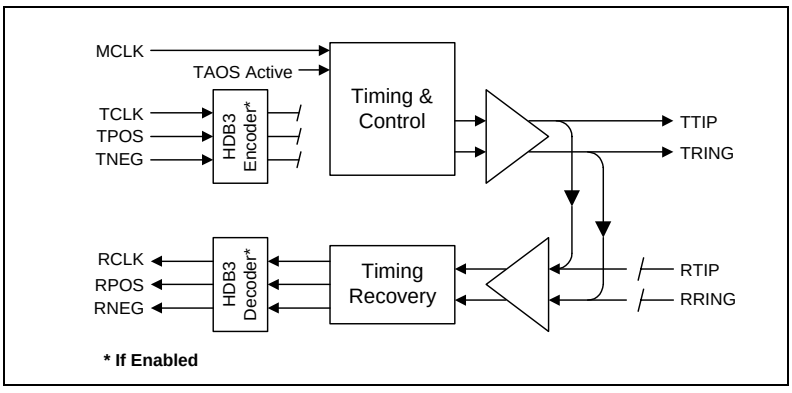


Figure 12. TAOS with Analog Loopback



2.8 G.772 Monitoring

The LXT380 can be configured as an octal line interface unit with all channels working as regular transceivers. In applications using only seven channels, the eight channel can be configured to monitor any of the remaining channels inputs or outputs.

The monitoring is non-intrusive per ITU-T G.772. Figure 2 on page 8 illustrates this concept.

The monitored line signal (input or output) goes through channel 0 clock and data recovery. The signal can be observed digitally at the RCLK/RPOS/RNEG outputs. This feature can also be used to create timing interfaces derived from a E1 signal. Please refer to Application Note: “Timing Interface Using the LXT380.”

In addition, channel 0 can be configured to a Remote Loopback while in monitoring mode. This will output the same data as in the signal being monitored at the channel 0 output (TTIP/TRING). The output signal can then be connected to a standard test equipment with an E1 electrical interface for monitoring purposes (non-intrusive monitoring).

Note: Remote loopback in channel 0 can only work if TCLK for that channel is clocked. The output drivers are tri-stated when TCLK is inactive.

2.9 Hitless Protection Switching (HPS)

The LXT386 transceivers include an output driver tristatability feature for T1/E1 redundancy applications. This feature greatly reduces the cost of implementing redundancy protection by eliminating external relays. Please refer to Application Note for guidelines for implementing redundancy systems for both T1 and E1 operation using the LXT380/1/4/6.

2.10 Operation Mode Summary

Table 2 summarizes all LXT380 hardware settings and corresponding operating modes.

Table 2. Operation Mode Summary

MCLK	TCLK	LOOP†	Receive Mode	Transmit Mode	Loopback
Clocked	Clocked	Open	Data/Clock recovery	Pulse Shaping ON	No Loopback
Clocked	Clocked	L	Data/Clock recovery	Pulse Shaping ON	Remote Loopback
Clocked	Clocked	H	Data/Clock recovery	Pulse Shaping ON	Analog Loopback
Clocked	L	Open	Data/Clock recovery	Power down	No Loopback
Clocked	L	L	Data/Clock Recovery	Power down	No effect on op.
Clocked	L	H	Data/Clock Recovery	Power down	No Analog Loopback
Clocked	H	Open	Data/Clock Recovery	Transmit All Ones	No Loopback
Clocked	H	L	Data/Clock Recovery	Pulse Shaping ON	Remote Loopback
Clocked	H	H	Data/Clock Recovery	Transmit All Ones	No effect on op.
L	Clocked	Open	Power Down	Pulse Shaping ON	No Loopback
† Hardware mode only.					

Table 2. Operation Mode Summary

MCLK	TCLK	LOOP†	Receive Mode	Transmit Mode	Loopback
L	Clocked	L	Power Down	Pulse Shaping ON	No Remote Loopback
L	Clocked	H	Power Down	Pulse Shaping ON	No effect on op.
L	H	Open	Power Down	Pulse Shaping OFF	No Loopback
L	H	L	Power Down	Pulse Shaping OFF	No Remote Loop
L	H	H	Power Down	Pulse Shaping OFF	No effect on op.
L	L	X	Power Down	Power down	No Loopback
H	Clocked	Open	Data Recovery	Pulse Shaping ON	No Loopback
H	Clocked	L	Data Recovery	Pulse Shaping OFF	Remote Loopback
H	Clocked	H	Data Recovery	Pulse Shaping ON	Analog Loopback
H	L	Open	Data Recovery	Power down	No Loopback
H	L	L	Data Recovery	Pulse Shaping OFF	Remote Loopback
H	H	Open	Data Recovery	Pulse Shaping OFF	No Loopback
H	H	L	Data Recovery	Pulse Shaping OFF	Remote Loopback
H	H	H	Data Recovery	Pulse Shaping OFF	Analog Loopback

† Hardware mode only.

2.11 Interfacing with 5V logic

The LXT380 can interface with 5V logic. In this case, the VCCIO pins should connected to a 5V power supply. The VCCIO pins feed the digital I/O pads making the input/output voltage levels consistent with 5V logic. The internal logic will still operate from the 3.3V supply (VCC0 and VCC1) to minimize the power consumption. See Table 28.

2.12 Parallel Host Interface

The LXT380 incorporates a highly flexible 8-bit parallel microprocessor interface. The interface is generic and is designed to support both non-multiplexed and multiplexed address/data bus systems for Motorola and Intel bus topologies. Two pins (MUX and $\overline{\text{MOT}}$/INTL) select four different operating modes. See Table 3.

Table 3. Operating Mode

MUX	$\overline{\text{MOT}}$/INTL	Operating Mode
0	0	Motorola Non-Multiplexed
0	1	Intel Non-Multiplexed
1	0	Motorola Multiplexed
1	1	Intel Multiplexed

The interface includes an address bus (A3–A0) and a data bus (D7–D0) for non-multiplexed operation and an 8-bit address/data bus for multiplexed operation. $\overline{\text{WR}}$, $\overline{\text{RD}}$, R/$\overline{\text{W}}$, $\overline{\text{CS}}$, ALE, $\overline{\text{DS}}$, $\overline{\text{INT}}$ and RDY/$\overline{\text{ACK}}$ are used as control signals. A significant enhancement is an internal wait-state

generator that controls an Intel and Motorola compatible handshake output signal (RDY/$\overline{\text{ACK}}$). In Motorola mode, $\overline{\text{ACK}}$ Low signals valid information is on the data bus. During a write cycle a Low signal acknowledges the acceptance of the write data. In Intel mode, RDY High signals to the controlling processor that the bus cycle can be completed. While Low, the microprocessor must insert wait states. This allows the LXT380 to interface with wait-state capable microcontrollers, independent of the processor bus speed. To activate this function, a reference clock is required on the MCLK pin.

An additional active Low interrupt output signal indicates alarm conditions like LOS and DFM to the microprocessor.

The LXT380 has a 4 bit address bus and provides 15 user accessible 8-bit registers for configuration, alarm monitoring, and control of the chip.

2.12.1 Motorola Interface

The Motorola interface is selected by asserting the $\overline{\text{MOT}}$/INTL pin Low. In non-multiplexed mode the falling edge of $\overline{\text{DS}}$ is used to latch the address information on the address bus. In multiplexed operation the address on the multiplexed address data bus is latched into the device with the falling edge of $\overline{\text{AS}}$. In non-multiplexed mode, $\overline{\text{AS}}$ should be pulled High.

The R/$\overline{\text{W}}$ signal indicates the direction of the data transfer. The $\overline{\text{DS}}$ signal is the timing reference for all data transfers and typically has a duty cycle of 50%. A read cycle is indicated by asserting R/$\overline{\text{W}}$ High with a falling edge on $\overline{\text{DS}}$. A write cycle is indicated by asserting R/$\overline{\text{W}}$ Low with a rising edge on $\overline{\text{DS}}$.

Both cycles require the $\overline{\text{CS}}$ signal to be Low and the Address pins to be actively driven by the microprocessor.

Note: $\overline{\text{CS}}$ and $\overline{\text{DS}}$ can be connected together in Motorola mode.

In a write cycle, the data bus is driven by the microprocessor. In a read cycle the bus is driven by the LXT380.

2.12.2 Intel Interface

The Intel interface is selected by asserting the $\overline{\text{MOT}}$/INTL pin High. The LXT380 supports non-multiplexed interfaces with separate address and data pins when MUX is asserted Low, and multiplexed interfaces when MUX is asserted High. The address is latched in on the falling edge of ALE. In non-multiplexed mode, ALE should be pulled High. R/$\overline{\text{W}}$ is used as the $\overline{\text{RD}}$ signal and $\overline{\text{DS}}$ is used as the $\overline{\text{WR}}$ signal. A read cycle is indicated to the LXT380 when the processor asserts $\overline{\text{RD}}$ Low while the $\overline{\text{WR}}$ signal is held High.

A write operation is indicated to the LXT380 by asserting $\overline{\text{WR}}$ Low while the $\overline{\text{RD}}$ signal is held High. Both cycles require the $\overline{\text{CS}}$ signal to be Low.

2.13 Interrupt Handling

2.13.1 Interrupt Sources

There are two interrupt sources:

1. Status change in the Loss of Signal (LOS) status register (04H.) The LXT380'S analog/digital loss of signal processor continuously monitors the receiver signal and updates the specific LOS status bit to indicate presence or absence of a LOS condition.
2. Status change in the Driver Failure Monitoring (DFM) status register (05H.) The LXT380'S smart power driver circuit continuously monitors the output drivers signal and updates the specific DFM status bit to indicate presence or absence of a secondary driver short circuit condition.

2.13.2 Interrupt Enable

The LXT380 provides a latched interrupt output ($\overline{INT}$). An interrupt occurs any time there is a transition on any enabled bit in the status register. Register 06H is the LOS interrupt enable register and register 07H is the DFM enable register. Writing a logic "1" into the enable register will enable the respective bit in the respective interrupt status register to generate an interrupt. The power-on default value is all zeroes. The setting of the interrupt enable bit does not affect the operation of the status registers.

Registers 08H and 09H are the LOS and DFM (respectively) interrupt status registers. When there is a transition on any enabled bit in a status register, the associated bit of the interrupt status register is set and an interrupt is generated (if one is not already pending). When an interrupt occurs, the $\overline{INT}$ pin is asserted Low. The output stage of the $\overline{INT}$ pin consists only of a pull-down device; an external pull-up resistor of approximately 10k ohm is required to support wired-OR operation.

2.13.3 Interrupt Clear

When an interrupt occurs, the interrupt service routine (ISR) should read both *interrupt status registers* (08H and 09H) to identify the interrupt source. The ISR should then read the corresponding *status monitor register* to obtain the current status of the device.

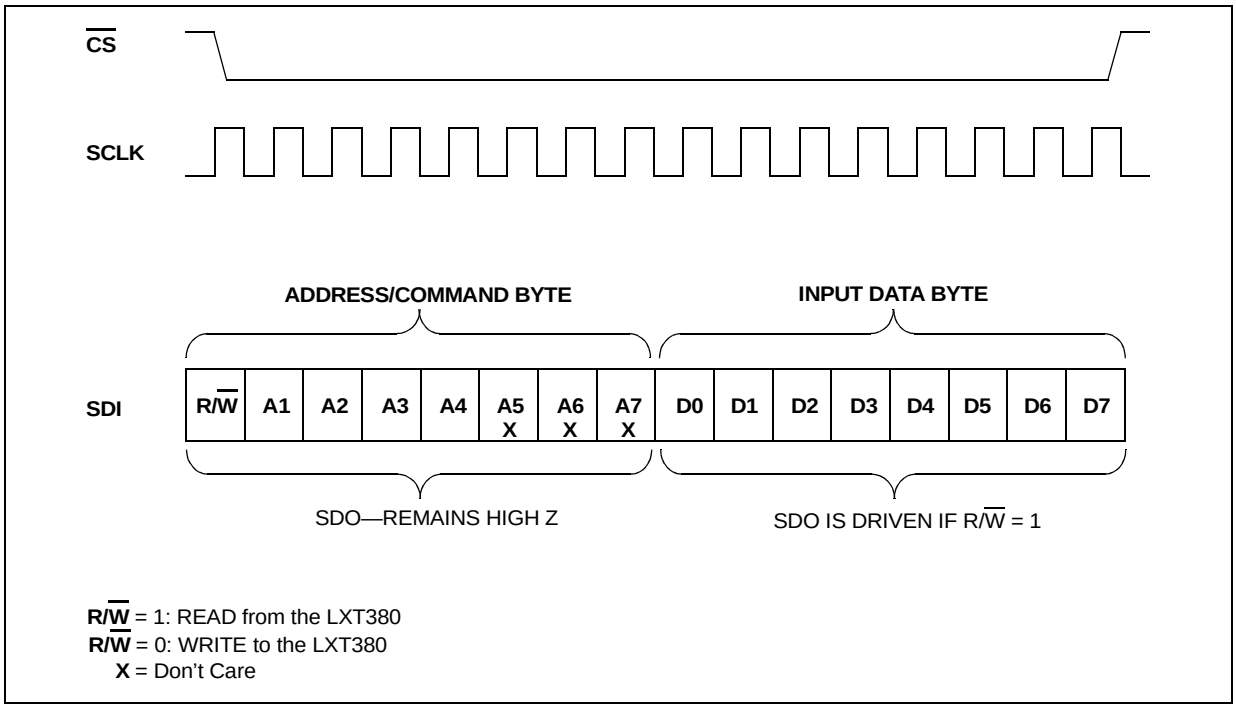
Note: There are two status monitor registers: the LOS (04H) and the DFM (05H).

Reading either status monitors register will clear its corresponding interrupts on the rising edge of the read or data strobe. When all pending interrupts are cleared, will the $\overline{INT}$ pin goes High.

2.14 Serial Host Mode

The LXT380 operates in Serial Host Mode when the MODE pin is left open. Figure 13 shows the SIO data structure. The registers are accessible through a 16bit word: an 8bit Command/Address byte (bits R/$\overline{W}$ and A1-A7) and a subsequent 8 bit data byte (bits D0-7). Bit R/$\overline{W}$ determines whether a read or a write operation occurs. Bits A4-0 in the Command/Address byte address specific registers (the address decoder ignores bits A7-A5). The data byte depends on both the value of bit R/$\overline{W}$ and the address of the register as set in the Command/Address byte.

Figure 13. Serial Host Mode Timing



3.0 Register Descriptions

Table 4. Serial and Parallel Port Register Addresses

Name	Symbol	Address		Mode
		Serial Port A7-A1	Parallel Port A7-A0	
ID Register	ID	xxx0000	xxxx0000	R
Analog Loopback	ALOOP	xxx0001	xxxx0001	R/W
Remote Loopback	RLOOP	xxx0010	xxxx0010	R/W
TAOS Enable	TAOS	xxx0011	xxxx0011	R/W
LOS Status Monitor	LOS	xxx0100	xxxx0100	R
DFM Status Monitor	DFM	xxx0101	xxxx0101	R
LOS Interrupt Enable	LIE	xxx0110	xxxx0110	R/W
DFM Interrupt Enable	DIE	xxx0111	xxxx0111	R/W
LOS Interrupt Status	LIS	xxx1000	xxxx1000	R
DFM Interrupt Status	DIS	xxx1001	xxxx1001	R
Software Reset Register	RES	xxx1010	xxxx1010	R/W
Performance Monitoring	MON	xxx1011	xxxx1011	R/W
Digital Loopback	DL	xxx1100	xxxx1100	R/W
LOS Criteria Selection	LCS	xxx1101	xxxx1101	R/W
Automatic TAOS Select	ATS	xxx1110	xxxx1110	R/W

Table 5. Register Addresses and Bit Names

Register			Bit							
Name	Sym	Mode	7	6	5	4	3	2	1	0
ID Register	ID	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Analog Loopback	ALOOP	R/W	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
Remote Loopback	RLOOP	R/W	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
TAOS Enable	TAOS	R/W	TAOS7	TAOS6	TAOS5	TAOS4	TAOS3	TAOS2	TAOS1	TAOS0
LOS Status Monitor	LOS	R	LOS7	LOS6	LOS5	LOS4	LOS3	LOS2	LOS1	LOS0
DFM Status Monitor	DFM	R	DSM7	DSM6	DSM5	DSM4	DSM3	DSM2	DSM1	DSM0
LOS Interrupt Enable	LIE	R/W	LIE7	LIE6	LIE5	LIE4	LIE3	LIE2	LIE1	LIE0
DFM Interrupt Enable	DIE	R/W	DIE7	DIE6	DIE5	DIE4	DIE3	DIE2	DIE1	DIE0

Table 5. Register Addresses and Bit Names (Continued)

Register			Bit							
Name	**Sym**	**Mode**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOS Interrupt Status	LIS	R	LIS7	LIS6	LIS5	LIS4	LIS3	LIS2	LIS1	LIS0
DFM Interrupt Status	DIS	R	DIS7	DIS6	DIS5	DIS4	DIS3	DIS2	DIS1	DIS0
Software Reset Register	RES	R/W	RES7	RES6	RES5	RES4	RES3	RES2	RES1	RES0
Performance Monitoring	MON	R/W	re-served	re-served	re-served	re-served	A3	A2	A1	A0
Digital Loopback	DL	R/W	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0
LOS Criteria Select	LCS	R/W	LCS7	LCS6	LCS5	LCS4	LCS3	LCS2	LCS1	LCS0
Automatic TAOS Select	ATS	R/W	ATS7	ATS6	ATS5	ATS4	ATS3	ATS2	ATS1	ATS0

Table 6. ID Register (00H)

Bit	Name	Function
7-0	ID7-ID0	This register contains a unique revision code and is mask programmed.

Table 7. Analog Loopback Register (01H)

Bit	Name	Function
7-0	AL7-AL0	Setting a bit to “1” enables analog loopback for transceivers 7–0 respectively.

Table 8. Remote Loopback Register (02H)

Bit	Name	Function
7-0	RL7-RL0	Setting a bit to “1” enables remote loopback for transceivers 7–0 respectively.

Table 9. TAOS Enable Register (03H)

Bit	Name	Function
7-0	TAOS7-TAOS0	Setting a bit to “1” causes a continuous stream of marks to be sent out at the TTIP and TRING pins of the respective transceiver 7–0. MCLK is used as timing reference. If MCLK is not available, the channel TCLK is used as the reference. On power up all register bits are set to “0.”

Table 10. LOS Status Monitor Register (04H)

Bit	Name	Function
7-0	LOS7-LOS0	Respective bit(s) are set to “1” every time the LOS processor detects a valid loss of signal condition in transceivers 7–0. RCLK is used as timing reference. If RCLK is not available an internal timing signal is used to qualify the LOS condition. Any change in the state causes an interrupt. On power up the register is set to “0.” All LOS interrupts are cleared by a single read operation.

Table 11. DFM Status Monitor Register (05H)

Bit	Name	Function
7-0	DFM7-DFM0	Respective bit(s) are set to “1” every time the short circuit monitor detects a valid secondary output driver short circuit condition in transceivers 7–0. On power-up all the register bits are set to “0.” All DFM interrupts are cleared by a single read operation.

Table 12. LOS Interrupt Enable Register (06H)

Bit	Name	Function
7-0	LIE7-LIE0	Transceiver 7–0 LOS interrupts are enabled by writing a “1” to the respective bit. On power-up all the register bits are set to “0”and all interrupts are disabled.

Table 13. DFM Interrupt Enable Register (07H)

Bit	Name	Function
7-0	DIE7-DIE0	Transceiver 7–0 DFM interrupts are enabled by writing a “1” to the respective bit. On power-up all the register bits are set to “0”and all interrupts are disabled.

Table 14. LOS Interrupt Status Register (08H)

Bit	Name	Function
7-0	LIS7-LIS0	These bits are set to “1” every time a LOS status change has occurred since the last cleared interrupt in transceivers 7–0 respectively.

Table 15. DFM Interrupt Status Register (09H)

Bit	Name	Function
7-0	DIS7-DIS0	These bits are set to “1” every time a DFM status change has occurred since the last cleared interrupt in transceivers 7–0 respectively.

Table 16. Software Reset Register (0AH)

Bit	Name	Function
7-0	RES7-RES0	Setting a bit to “1” resets the respective transceiver 7–0 respectively. This does not reset the register (‘0’ clears the reset).

Table 17. Performance Monitoring Register

Bit	Name	Function	Protected Monitoring Select				
			A3	A2	A1	A0	Mode
0	A0	Protected Monitoring Select	0	0	0	0	No protection monitoring
			0	0	0	1	RX1
1	A1		0	0	1	0	RX2
			0	0	1	1	RX3
2	A2		0	1	0	0	RX4
			0	1	0	1	RX5
3	A3		0	1	1	0	RX6
			0	1	1	1	RX7
4	reserved	-	1	0	0	0	No protection monitoring
			1	0	0	1	TX1
5	reserved	-	1	0	1	0	TX2
			1	0	1	1	TX3
6	reserved	-	1	1	0	0	TX4
			1	1	0	1	TX5
7	reserved	-	1	1	1	0	TX6
			1	1	1	1	TX7

Table 18. Digital Loopback Register (0CH)

Bit	Name	Function
7-0	DL7-DL0	Setting a bit to “1” enables digital loopback for the respective transceiver. During digital loopback LOS and TAOS stay active and independent of TCLK, while data received on TPOS/TNEG/TCLK is looped back to RPOS/RNEG/RCLK. On power up all register bits are set to “0.”

Table 19. LOS Criteria Register (0DH)

Bit	Name	Function
7-0	LCS7-LCS0	Setting a bit to “1” selects the ETSI 300233 LOS mode for the respective transceiver. On power-on reset the register is set to “0” and G.775 LOS operation is selected.

Table 20. Automatic TAOS Select Register (0EH)

Bit	Name	Function
7-0	ATS7-ATS0	Setting a bit to “1” enables automatic TAOS generation whenever a LOS condition is detected in the respective transceiver. On power-on reset the register is set to “0.”

4.0 JTAG Boundary Scan

4.1 Overview

The LXT380 supports IEEE 1149.1 compliant JTAG boundary scan. Boundary scan allows easy access to the interface pins for board testing purposes.

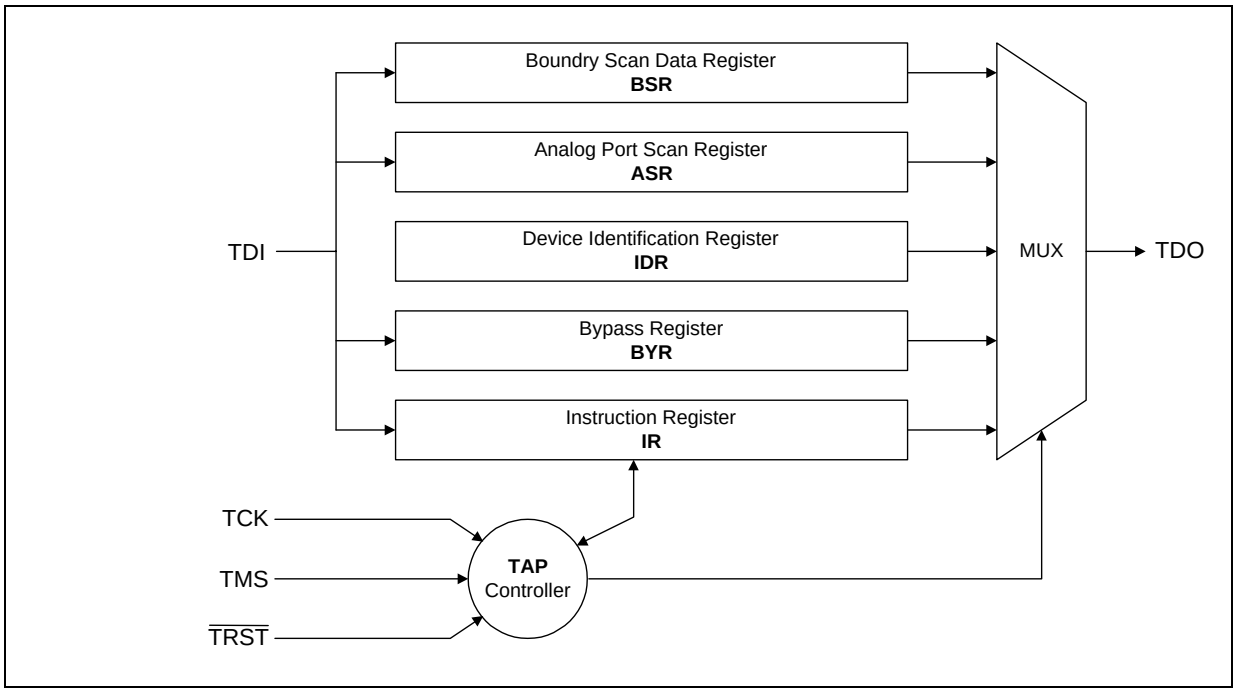
In addition to the traditional IEE1149.1 digital boundary scan capabilities, the LXT380 also includes analog test port capabilities. This feature provides access to the TIP and RING signals in each channel (transmit and receive). This way, the signal path integrity across the primary winding of each coupling transformer can be tested.

4.2 Architecture

Figure 14 represents the LXT380 basic JTAG architecture.

The LXT380 JTAG architecture includes a TAP Test Access Port Controller, data registers and an instruction register. The following paragraphs describe these blocks in detail.

Figure 14. LXT380 JTAG Architecture



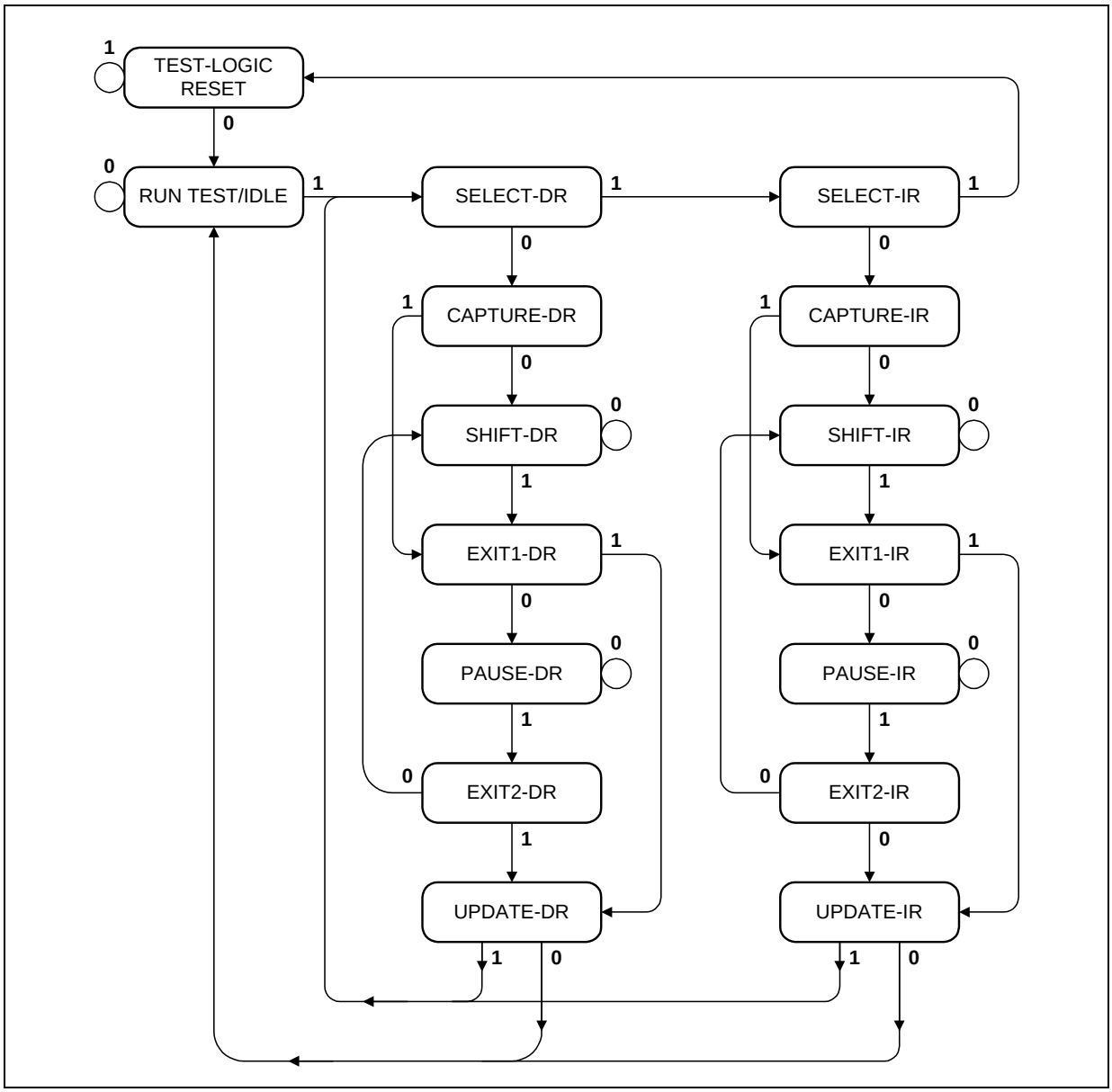
4.3 TAP Controller

The TAP controller is a 16 state synchronous state machine controlled by the TMS input and clocked by TCK. See Figure 15. The TAP controls whether the LXT380 is in reset mode, receiving an instruction, receiving data, transmitting data or in an idle state. Table 21 describes in detail each of the states represented in Figure 15.

Table 21. TAP State Description

State	Description
Test logic reset	In this state the test logic is disabled. The device is set to normal operation mode. While in this state, the instruction register is set to the ICODE instruction.
Run—test/idle	The TAP controller stays in this state as long as TMS is low. Used to perform tests.
Capture—DR	The Boundary Scan Data Register (BSR) is loaded with input pin data.
Shift—DR	Shifts the selected test data registers by one stage toward its serial output.
Update—DR	Data is latched into the parallel output of the BSR when selected.
Capture—IR	Used to load the instruction register with a fixed instruction.
Shift—IR	Shifts the instruction register by one stage.
Update—IR	Loads a new instruction into the instruction register.
Pause—IR Pause—DR	Momentarily pauses shifting of data through the data/instruction registers.
Exit1—IR Exit1—DR Exit2—IR Exit2—DR	Temporary states that can be used to terminate the scanning process.

Figure 15. JTAG State Diagram



4.4 JTAG Register Description

The following paragraphs describe each of the registers represented in Figure 14 on page 37.

4.4.1 Boundary Scan Register, BSR

The BSR is a shift register that provides access to all the digital I/O pins. The BSR is used to apply and read test patterns to/from the board. Each pin is associated with a scan cell in the BSR register. Bidirectional pins or tristatable pins require more than one position in the register. Table 22 shows the BSR scan cells and their functions. Data into the BSR is shifted in LSB first.

Table 22. Boundary Scan Register, BSR

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
0	LOOP0	I/O	PDO0	
1	LOOP0	I/O	PADD0	
2	LOOP1	I/O	PDO1	
3	LOOP1	I/O	PADI1	
4	LOOP2	I/O	PDO2	
5	LOOP2	I/O	PADI2	
6	LOOP3	I/O	PDO3	
7	LOOP3	I/O	PADI3	
8	LOOP4	I/O	PDO4	
9	LOOP4	I/O	PADI4	
10	LOOP5	I/O	PDO5	
11	LOOP5	I/O	PADI5	
12	LOOP6	I/O	PDO6	
13	LOOP6	I/O	PADI6	
14	LOOP7	I/O	PDO7	
15	LOOP7	I/O	PADI7	
16	N/A	-	PDOEN	PDOEN controls the LOOP0 through LOOP7 pins. Setting PDOEN to “1” configures the pins as outputs. The output value to the pin is set in PDO[0..7]. Setting PDOEN to “0” tristates all the pins. The input value to the pins can be read in PADD[0.7].
17	TCLK1	I	TCLK1	
18	TPOS1	I	TPOS1	
19	TNEG1	I	TNEG1	
20	RCLK1	O	RCLK1	
21	RPOS1	O	RPOS1	
22	RNEG1	O	RNEG1	
23	N/A	-	HIZB1	HIZB1 controls the RPOS1, RNEG1 and RCLK1 pins. Setting HIZB1 to “1” enables output on the pins. Setting HIZB1 to “0” tristates the pins.

Table 22. Boundary Scan Register, BSR (Continued)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
24	LOS1	O	LOS1	
25	TCLK0	I	TCLK0	
26	TPOS0	I	TPOS0	
27	TNEG0	I	TNEG0	
28	RCLK0	O	RCLK0	
29	RPOS0	O	RPOS0	
30	RNEG0	O	RNEG0	
31	N/A	-	HIZB0	HIZB0 controls the RPOS0, RNEG0 and RCLK0 pins. Setting HIZB0 to “1” enables output on the pins. Setting HIZB0 to “0” tristates the pins.
32	LOS0	O	LOS0	
33	MUX	I	MUX	
34	LOS3	O	LOS3	
35	RNEG3	O	RNEG3	
36	RPOS3	O	RPOS3	
37	N/A	-	HIZB3	HIZB3 controls the RPOS3, RNEG3 and RCLK3 pins. Setting HIZB3 to “1” enables output on the pins. Setting HIZB3 to “0” tristates the pins.
38	RCLK3	O	RCLK3	
39	TNEG3	I	TNEG3	
40	TPOS3	I	TPOS3	
41	TCLK3	I	TCLK3	
42	LOS2	O	LOS2	
43	RNEG2	O	RNEG2	
44	RPOS2	O	RPOS2	
45	N/A	-	HIZB2	HIZB2 controls the RPOS2, RNEG2 and RCLK2 pins. Setting HIZB2 to “1” enables output on the pins. Setting HIZB2 to “0” tristates the pins.
46	RCLK2	O	RCLK2	
47	TNEG2	I	TNEG2	
48	TPOS2	I	TPOS2	
49	TCLK2	I	TCLK2	
50	INT	O	INTRUPTB	
51	ACK	O	SDORDY	
52	N/A	-	SDORDYEN	SDORDYEN controls the $\overline{\text{ACK}}$ pin. Setting SDORDYEN to “1” enables output on $\overline{\text{ACK}}$ pin. Setting SDORDYEN to “0” tristates the pin.
53	DS	I	WRB	
54	R/$\overline{\text{W}}$	I	RDB	
55	ALE	I	ALE	

Table 22. Boundary Scan Register, BSR (Continued)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
24	LOS1	O	LOS1	
25	TCLK0	I	TCLK0	
26	TPOS0	I	TPOS0	
27	TNEG0	I	TNEG0	
28	RCLK0	O	RCLK0	
29	RPOS0	O	RPOS0	
30	RNEG0	O	RNEG0	
31	N/A	-	HIZB0	HIZB0 controls the RPOS0, RNEG0 and RCLK0 pins. Setting HIZB0 to “1” enables output on the pins. Setting HIZB0 to “0” tristates the pins.
32	LOS0	O	LOS0	
33	MUX	I	MUX	
34	LOS3	O	LOS3	
35	RNEG3	O	RNEG3	
36	RPOS3	O	RPOS3	
37	N/A	-	HIZB3	HIZB3 controls the RPOS3, RNEG3 and RCLK3 pins. Setting HIZB3 to “1” enables output on the pins. Setting HIZB3 to “0” tristates the pins.
38	RCLK3	O	RCLK3	
39	TNEG3	I	TNEG3	
40	TPOS3	I	TPOS3	
41	TCLK3	I	TCLK3	
42	LOS2	O	LOS2	
43	RNEG2	O	RNEG2	
44	RPOS2	O	RPOS2	
45	N/A	-	HIZB2	HIZB2 controls the RPOS2, RNEG2 and RCLK2 pins. Setting HIZB2 to “1” enables output on the pins. Setting HIZB2 to “0” tristates the pins.
46	RCLK2	O	RCLK2	
47	TNEG2	I	TNEG2	
48	TPOS2	I	TPOS2	
49	TCLK2	I	TCLK2	
50	INT	O	INTRUPTB	
51	ACK	O	SDORDY	
52	N/A	-	SDORDYEN	SDORDYEN controls the $\overline{\text{ACK}}$ pin. Setting SDORDYEN to “1” enables output on $\overline{\text{ACK}}$ pin. Setting SDORDYEN to “0” tristates the pin.
53	DS	I	WRB	
54	R/$\overline{\text{W}}$	I	RDB	
55	ALE	I	ALE	

Table 22. Boundary Scan Register, BSR (Continued)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
56	CS	I	CSB	
57	$\overline{\text{MOT}}$/ INTL	I	IMB	
58	TCLK5	I	TCLK5	
59	TPOS5	I	TPOS5	
60	TNEG5	I	TNEG5	
61	RCLK5	O	RCLK5	
62	RPOS5	O	RPOS5	
63	RNEG5	O	RNEG5	
64	N/A	-	HIZB5	HIZB5 controls the RPOS5, RNEG5 and RCLK5 pins. Setting HIZB5 to “1” enables output on the pins. Setting HIZB5 to “0” tristates the pins.
65	LOS5	O	LOS5	
66	TCLK4	I	TCLK4	
67	TPOS4	I	TPOS4	
68	TNEG4	I	TNEG4	
69	RCLK4	O	RCLK4	
70	RPOS4	O	RPOS4	
71	RNEG4	O	RNEG4	
72	N/A	-	HIZB4	HIZB4 controls the RPOS4, RNEG4 and RCLK4 pins. Setting HIZB4 to “1” enables output on the pins. Setting HIZB4 to “0” tristates the pins.
73	LOS4	O	LOS4	
74	OE	I	OE	
75	CLKE	I	CLKE	
76	LOS7	O	LOS7	
77	RNEG7	O	RNEG7	
78	RPOS7	O	RPOS7	
79	N/A	-	HIZB7	HIZB7 controls the RPOS7, RNEG7 and RCLK7 pins. Setting HIZB7 to “1” enables output on the pins. Setting HIZB7 to “0” tristates the pins.
80	RCLK7	O	RCLK7	
81	TNEG7	I	TNEG7	
82	TPOS7	I	TPOS7	
83	TCLK7	I	TCLK7	
84	LOS6	O	LOS6	
85	RNEG6	O	RNEG6	
86	RPOS6	O	RPOS6	
87	N/A	-	HIZB6	HIZB6 controls the RPOS6, RNEG6 and RCLK6 pins. Setting HIZB6 to “1” enables output on the pins. Setting HIZB6 to “0” tristates the pins.

Table 22. Boundary Scan Register, BSR (Continued)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
88	RCLK6	O	RCLK6	
89	TNEG6	I	TNEG6	
90	TPOS6	I	TPOS6	
91	TCLK6	I	TCLK6	
92	MCLK	I	MCLK	
93	MODE	I	MODE	
94	GND	–	A4	
95	A3	I	A3	
96	A2	I	A2	
97	A1	I	A1	
98	A0	I	A0	

4.4.2 Device Identification Register, IDR

The IDR register provides access to the manufacturer number, part number and the LXT380 revision. The register is arranged per IEEE 1149.1 and is represented in Table 23. Data into the IDR is shifted in LSB first.

Table 23. Device Identification Register, IDR

Bit #	Comments
31–28	Revision Number
27–12	Part Number
11–1	Manufacturer Number
0	Set to ‘1’

4.4.3 Bypass Register, BYR

The Bypass Register is a 1 bit register that allows direct connection between the TDI input and the TDO output.

4.4.4 Analog Port Scan Register, ASR

The ASR is a 5 bit shift register used to control the analog test port at pins AT1, AT2. When the INTEST_ANALOG instruction is selected, TDI connects to the ASR input and TDO connects to the ASR output. After 5 TCK rising edges, a 5 bit control code is loaded into the ASR. Data into the ASR is shifted in LSB first.

Table 24 shows the 16 possible control codes and the corresponding operation on the analog port. The Analog Test Port can be used to verify continuity across the coupling transformers primary winding.

Table 24. Analog Port Scan Register, ASR

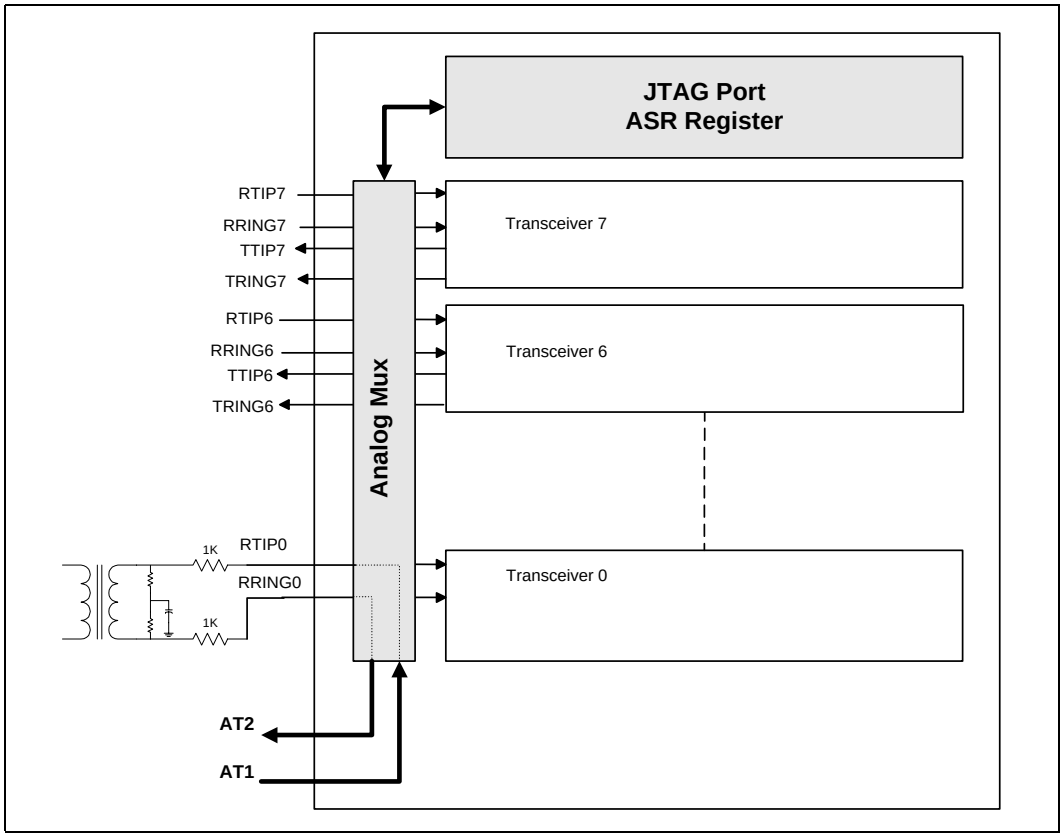
ASR Control Code	AT1 Forces Voltage To:	AT2 Senses Voltage From:
11111	TTIP0	TRING0
11110	TTIP1	TRING1
11101	TTIP2	TRING2
11100	TTIP3	TRING3
11011	TTIP4	TRING4
11010	TTIP5	TRING5
11001	TTIP6	TRING6
11000	RTIP7	RRING7
10111	RTIP0	RRING0
10110	RTIP1	RRING1
10101	RTIP2	RRING2
10100	RTIP3	RRING3
10011	RTIP4	RRING4
10010	RTIP5	RRING5
10001	RTIP6	RRING6
10000	RTIP7	RRING7

The Analog Test Port can be used to verify continuity across the coupling transformer's primary winding. By applying a stimulus to the AT1 input, a known voltage will appear at AT2 for a given load. This, in effect, tests the continuity of a receive or transmit interface. See Figure 16.

4.4.5 Instruction Register, IR

The IR is a 3 bit shift register that loads the instruction to be performed. The instructions are shifted LSB first. Table 25 shows the valid instruction codes and the corresponding instruction description.

Figure 16. Analog Test Port Application



5.0 Test Specifications

Table 25. Instruction Register, IR

Instruction	Code #	Comments
EXTEST	000	Connects the BSR to TDI and TDO. Input pins values are loaded into the BSR. Output pins values are loaded from the BSR.
INTEST_ANALOG	010	Connects the ASR to TDI and TDO. Allows voltage forcing/sensing through AT1 and AT2. Refer to Table 24.
SAMPLE / PRELOAD	100	Connects the BSR to TDI and TDO. The normal path between the LXT380 logic and the I/O pins is maintained. The BSR is loaded with the signals in the I/O pins.
IDCODE	110	Connects the IDR to the TDO pin.
BYPASS	111	Serial data from the TDI input is passed to the TDO output through the 1 bit Bypass Register.

Note: Tables 26 through 41 and Figure 20 through 31 represent the performance specifications of the LXT380 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Tables 28 through 41 are guaranteed over the recommended operating conditions specified in Table 27.

Table 26. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC supply voltage	VCC0, VCC1, TVCC 0-7	-0.5	4.0	V
DC supply voltage	VCCIO0, VCCIO1	-0.5	7.0	V
Input voltage on any digital pin	V_{IN}	GND-0.5 GND-0.5	VCCIO0 + 0.5 VCCIO1 + 0.5	V V
Input voltage on RTIP, RRING[1]	V_{IN}	GND-0.5	VCC0 + 0.5 VCC1 + 0.5	V
ESD voltage on any Pin[2]	V_{IN}	2000		V
Transient latch-up current on any pin	I_{IN}		100	mA
Input current on any digital pin[3]	I_{IN}	-10	10	mA
DC input current on TTIP, TRING[3]	I_{IN}		±100	mA
DC input current on RTIP, RRING[3]	I_{IN}		±100	mA
Storage temperature	T_{STOR}	-65	+150	°C

Caution: Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

NOTES:
1. Referenced to ground.
2. Human body model.
3. Constant input current.

Table 26. Absolute Maximum Ratings (Continued)

Parameter	Symbol	Min	Max	Unit
Maximum package power dissipation	P_P		850	mW
Thermal resistance, junction to ambient, 144 pin LQFP package			28	°C/W
Thermal resistance, junction to ambient, 160 pin PBGA package			28	°C/W

Caution: Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

NOTES:
1. Referenced to ground.
2. Human body model.
3. Constant input current.

Table 27. Recommended Operating Conditions

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
DC supply voltage		VCC	3.135	3.3	3.465	V	3.3V ± 5%
Digital I/O DC supply voltage		VCC	3.135	3.3	5.25	V	
Ambient operating temperature		TA	-40	25	+85	°C	
Average transmitter power supply current[1]	75 Ω, coax cable	I_{TVCC}	–	–	265	mA	100% 1's density
	120 Ω, TWP cable			–	210	mA	100% 1's density
	75 Ω, coax cable			125	–	mA	50% 1's density
	120 Ω, TWP cable			100	–	mA	50% 1's density
Average core power supply current[1]		I_{VCC}	–	80	100	mA	
Average I/O power supply current[1, 2]		I_{VCCIO}		18	25	mA	
Output load at TTIP and TRING		RL	40	–	–	Ω	

NOTES:
1. Current consumption over the full operating temperature and power supply voltage range.
2. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50pF load.

Table 28. DC Characteristics

Parameter	Sym	Min.	Typ.	Max.	Unit	Test Condition
High level input voltage	VIH	2	–	–	V	
Low level input voltage	VIL		–	0.8	V	
High level output voltage[1]	VOH	2.4	–	VCCIO	V	IOUT= 400µA
Low level output voltage[1]	VOL	–	–	0.4	V	IOUT= 1.6mA

Table 28. DC Characteristics (Continued)

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
MODE and LOOP 0-7	Low level input voltage	V_{INL}	–	–	1/ 3VCC- 0.2	V	The VCC supply refers to VCCIO0 or VCCIO1 only.
	Midrange level input voltage	V_{INM}	1/ 3VCC +0.2	1/ 2VCC	2/ 3VCC- 0.2	V	
	High level input voltage	V_{INH}	2/ 3VCC +0.2	–	–	V	
	Low level input current	I_{INL}	–	–	50	µA	
	High level input current	I_{INH}	–	–	50	µA	
Input leakage current		I_{IL}	-10	–	+10	µA	
Tri state leakage current		I_{HZ}	-10	–	+10	µA	
Tri state output current		I_{HZ}		–	1	µA	TTIP, TRING
Line short circuit current		–	–	–	50	mA RMS	2 x 11 Ω series resistors and 1:2 transformer
Input Leakage: TMS TDI $\overline{TRST}$		–	–	–	50	µA	

Table 29. Transmit Transmission Characteristics

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
Output pulse amplitude	75 Ω 120 Ω	–	2.14 2.7	2.37 3.0	2.60 3.3	V V	Tested at the line side
Peak voltage of a space	75 Ω 120 Ω	–	-0.237 -0.3	–	0.237 0.3	V V	
Transmit amplitude variation with supply		–	-1	–	+1	%	
Difference between pulse sequences		–		–	200	mV	For 17 consecutive pulses
Pulse width ratio of the positive and negative pulses		–	0.95	–	1.05	–	At the nominal half amplitude
Transmit transformer turns Ratio for 75/120 Ω characteristic impedance		–		1:2 ± 2%	–	–	Rt = 11 Ω ± 1%
† Guaranteed by design and other correlation methods.							

Table 29. Transmit Transmission Characteristics (Continued)

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
Transmit return loss 75 Ω coaxial†	51kHz to 102 kHz 102 kHz to 2.048 MHz 2.048 MHz to 3.072 MHz	–	15 15 15	17 18 17	–	dB dB dB	Using components in the LXD380 evaluation board
Transmit return loss, 120 Ω twisted pair cable†	51kHz to 102 kHz 102 kHz to 2.048 MHz 2.048 MHz to 3.072 MHz	–	15 15 15	18 19 18	–	dB dB dB	Using components in the LXD380 evaluation board
Transmit intrinsic jitter: 20Hz to 100kHz		–		0.030	0.050	U.I.	Tx path TCLK is jitter free
† Guaranteed by design and other correlation methods.							

Table 30. Receive Transmission Characteristics

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
Permissible cable attenuation		–	–	–	12	dB	@1024 kHz
Receiver dynamic range		DR	0.5	–	–	Vp	
Signal to noise interference margin		S/I	-15	–	–	dB	Per G.703, O.151 @ 6 dB cable attenuation
Data decision threshold		SRE	43	50	57	%	Rel. to peak input voltage
Data receiver squelch level		–	–	150	–	mV	
Loss of signal threshold		–	–	200	–	mV	
LOS hysteresis		–	–	50	–	mV	
Consecutive zeros before loss of signal		–	–	32 2048	–	–	G.775 recommendation ETSI 300 233 specification
LOS reset		–	12.5%	–	–	–	1's density
Low limit input jitter tolerance†	1Hz to 20Hz 20Hz to 2.4kHz 18kHz to 100kHz	–	36 1.5 0.2	–	–	U.I. U.I. U.I.	G.823 recommendation † Cable attenuation is 6 dB
Receiver input impedance		–	–	70	–	k Ω	@ 1.024 MHz
Input termination resistor tolerance		–			±1	%	
Common mode input impedance to ground		–		20		k Ω	
Input return loss†	51 kHz–102 kHz 102–2048 kHz 2048kHz–3072 kHz	–	20 20 20	–	–	dB dB dB	Measured against nominal impedance using components in the LXD380 evaluation board
† Guaranteed by design and other correlation methods.							

Table 30. Receive Transmission Characteristics (Continued)

Parameter	Sym	Min.	Typ.	Max.	Unit	Test Condition
LOS delay time	–	–	30	–	µs	Data recovery mode
LOS reset	–	10	–	255	marks	Data recovery mode
Receive intrinsic jitter	–	–	0.020	0.032	U.I.	
† Guaranteed by design and other correlation methods.						

Table 31. Analog Test Port Characteristics

Parameter	Sym	Min.	Typ.	Max.	Unit	Test Condition
3 dB bandwidth	at13db	–	5	–	MHz	
Input voltage range	at1iv	0	–	VCC0 VCC1	V	
Output voltage range	at2ov	0	–	VCC0 VCC1	V	

Table 32. Transmit Timing Characteristics

Parameter	Sym	Min.	Typ.	Max.	Unit	Test Condition
Master clock frequency	MCLK	–	2.048	–	MHz	
Master clock tolerance	MCLK	-100	–	100	ppm	
Master clock duty cycle		40	–	60	%	
Output pulse width	TW	219	244	269	ns	
Transmit clock frequency	TCLtK	–	2.048	–	MHz	
Transmit clock tolerance	TCLKt	-50	–	+50	ppm	
Transmit clock duty cycle	t_{DC}	10	–	90	%	NRZ mode
TPOS/TNEG pulse width (RZ mode)	t_{MPW}	236	–	252	ns	RZ mode (TCLK = H for >16 clock cycles)
TPOS/TNEG to TCLK setup time	t_{SUT}	20	–	–	ns	
TCLK to TPOS/TNEG hold time	t_{HT}	20	–	–	ns	
Delay time OE Low to driver High Z	t_{OEZ}	–	–	1	µs	
Delay time TCLK Low to driver High Z	t_{TZ}	8	–	15	µs	

Figure 17. Transmit Clock Timing

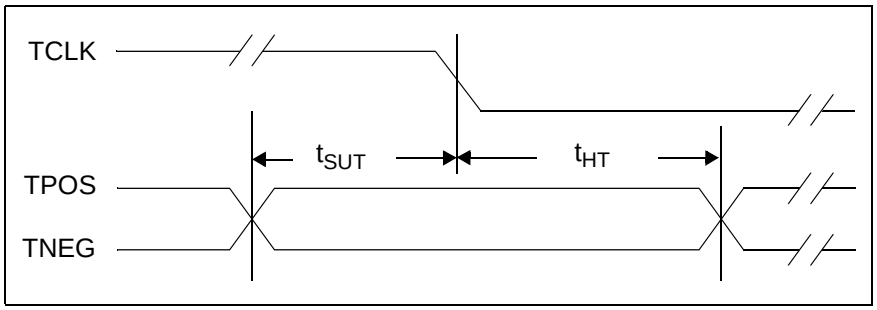


Table 33. Receive Timing Characteristics

Parameter	Sym	Min.	Typ.	Max.	Unit	Test Condition
Receive clock capture range	–	–	±80	–	ppm	
Receive clock duty cycle[1]	RCKd	35	50	65	%	
Receive clock pulse width[1]	tPW	447	488	529	ns	
Receive clock pulse width low time	tPWH	195	244	295	ns	
Receive clock pulse width high time	tPW	195	244	295	ns	
Rise/fall time[4]	Tr	20	–	–	ns	@ CL=15 pF
RPOS/RNEG pulse width (MCLK=H)[2]	tPWL	200	244	300	ns	
RPOS/RNEG to RCLK rising setup time	tSUR	50	203	–	ns	
RCLK rising to RPOS/RNEG hold time	tHR	50	203	–	ns	
Delay time between RPOS/ RNEG and RCLK	–	–	–	5	ns	MCLK = H[3]

NOTES:
1. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2UI displacement for E1 per ITU G.823).
2. Clock recovery is disabled in this mode.
3. If MCLK = H the receive PLLs are replaced by a simple EXOR circuit.
4. For all digital outputs.

Figure 18. Receive Clock Timing Diagram

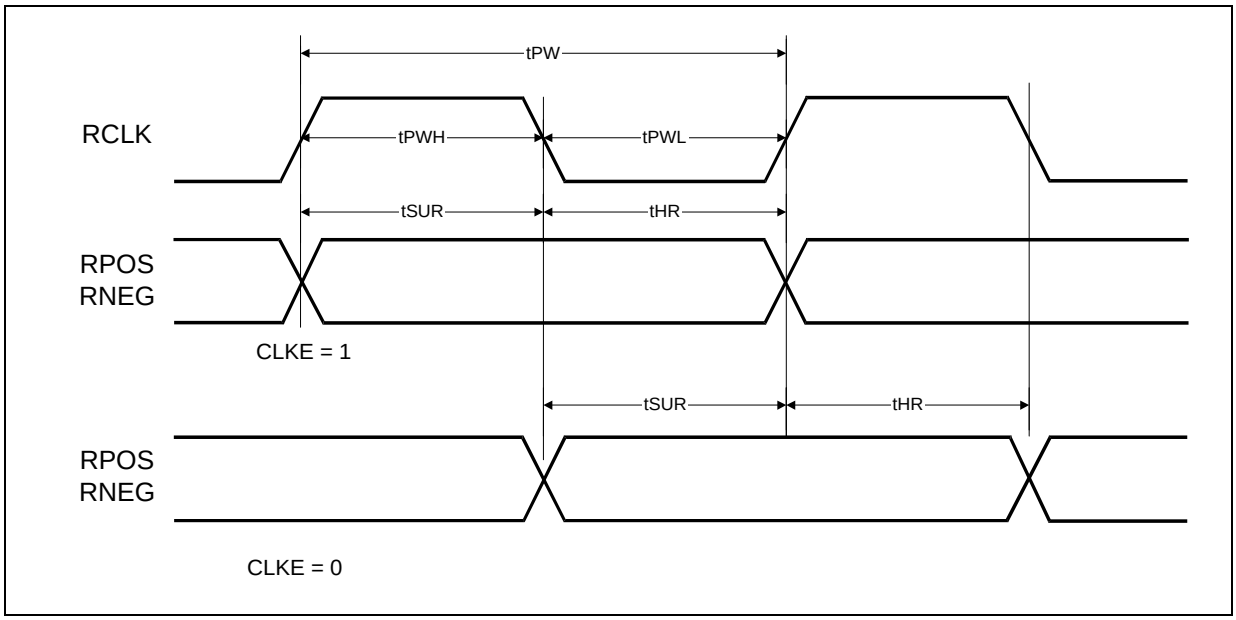


Table 34. JTAG Timing Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Cycle Time	t_{CYC}	200	–	–	ns	
J-TMS/J-TDI to J-TCK rising edge time	t_{SUT}	50	–	–	ns	
J-CLK rising to J-TMS/L-TDI hold time	t_{HT}	50	–	–	ns	
J-TCLK falling to J-TDO valid	t_{DOD}	–	–	50	ns	

Figure 19. JTAG Timing

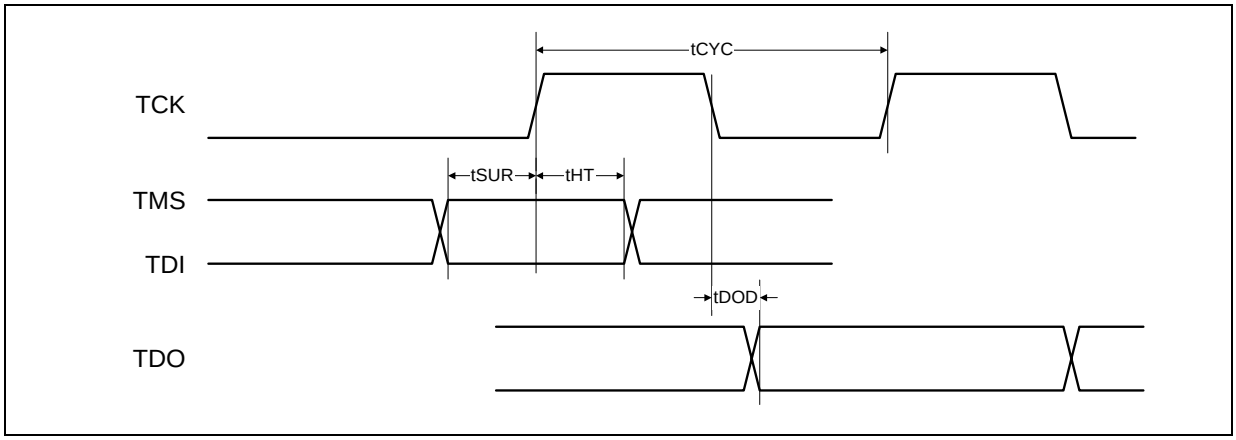


Table 35. Intel Mode Read Timing Characteristics

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to latch	t_{SALR}	10	–	–	ns	
Valid address latch pulse width	t_{VL}	30	–	–	ns	
Latch active to active read setup time	t_{SLR}	10	–	–	ns	
Address setup time to $\overline{RD}$ inactive	Thar	1	–	–	ns	
Address hold time from $\overline{RD}$ inactive	Tsar	5	–	–	ns	
Address hold time from inactive ALE	Thalr	5	–	–	ns	
Chip select setup time to active read	t_{SCSR}	0	–	–	ns	
Chip select hold time from inactive read	t_{HCSR}	0	–	–	ns	
Active read to data valid delay time	t_{PRD}	10	–	50	ns	
Inactive read to data tri-state delay time	t_{ZRD}	3	–	35	ns	
Valid read signal pulse width	t_{VRD}	60	–	–	ns	
Inactive read to inactive $\overline{INT}$ delay time	t_{INT}		–	10	ns	
Active Chip Select to RDY delay time	t_{DRDY}	0	–	12	ns	
Active Ready low time	t_{VRDY}	–	–	24	ns	
Inactive Ready to Tri-state Delay Time	t_{RDYZ}	–	–	3	ns	

NOTES:
1. Typical figures are at 25 C and are for design aid only: not guaranteed and not subject to production testing.
2. C_L= 100pF on D0-D7 All other outputs are loaded with 50pF.

Figure 20. Non-Multiplexed Intel Mode Read Timing

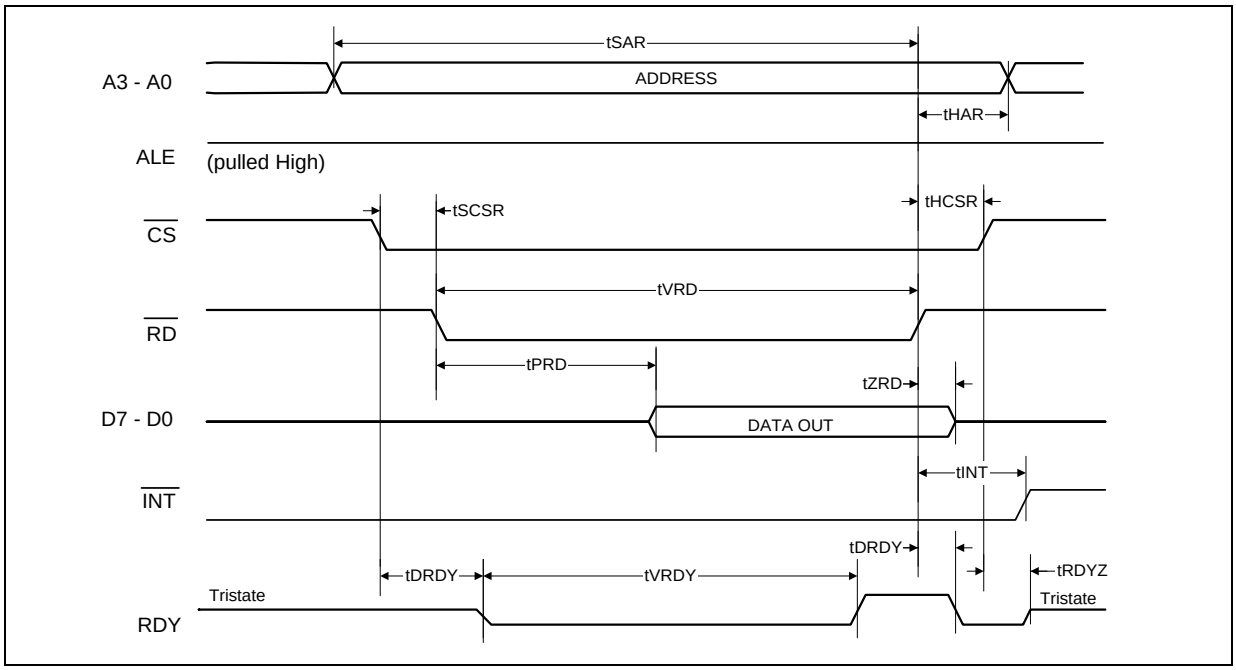


Figure 21. Multiplexed Intel Read Timing

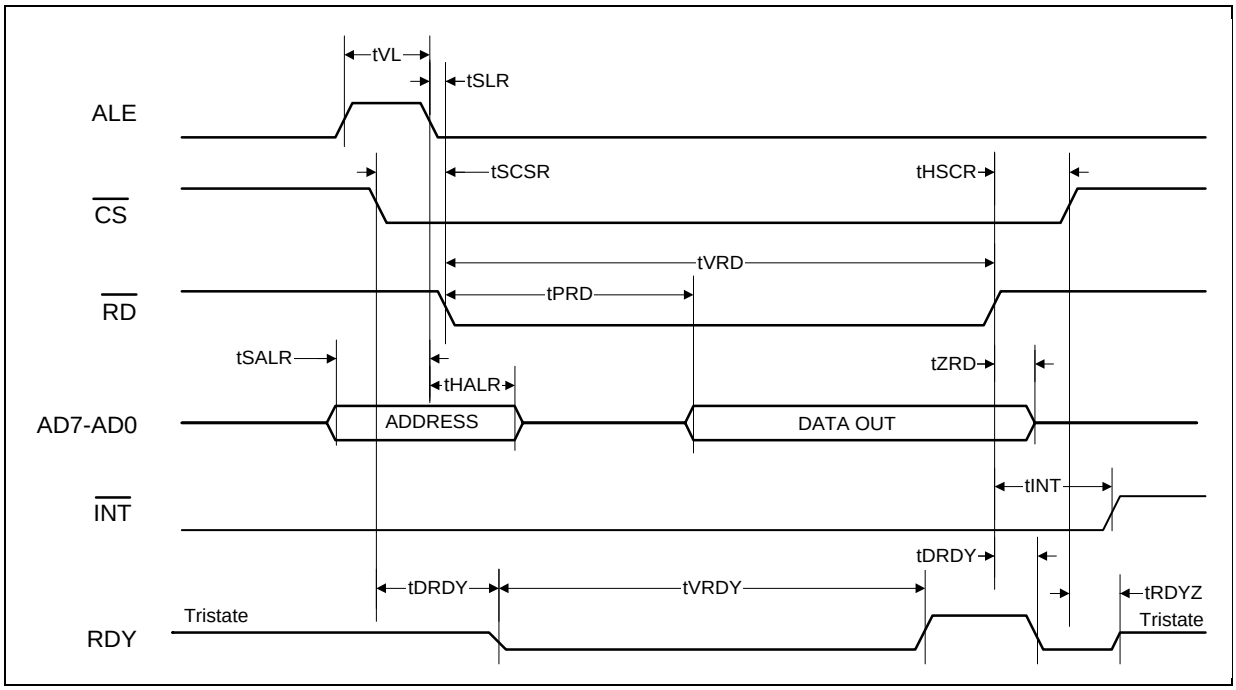


Table 36. Intel Mode Write Timing Characteristics

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to latch	tSALW	10	–	–	ns	
Valid address latch pulse width	tVL	30	–	–	ns	
Latch active to active write setup time	tSLW	10	–	–	ns	
Address setup time to $\overline{WR}$ inactive	Thaw	2	–	–	ns	
Address hold time from $\overline{WR}$ inactive	Tsaw	6	–	–	ns	
Address hold time from inactive ALE	Thalw	5	–	–	ns	
Chip select setup time to active write	tSCSW	0	–	–	ns	
Chip select hold time from inactive write	tHCSW	0	–	–	ns	
Data valid to write active setup time	tSDW	40	–	–	ns	
Data hold time to active write	tHDW	30	–	–	ns	
Valid write signal pulse width	tVWR	60	–	–	ns	
Inactive write to inactive $\overline{INT}$ delay time	tINT	–	–	10	ns	
Chip select to RDY delay time	tDRDY	0	–	12	ns	
Active ready low time	tVRDY	–	–	24	ns	
Inactive ready to Tri-state delay time	tRDYZ	–	–	3	ns	

NOTES:
1. Typical figures are at 25 C and are for design aid only: not guaranteed and not subject to production testing.
2. C_L= 100pF on D0-D7 All other outputs are loaded with 50pF.

Figure 22. Non-Multiplexed Intel Mode Write Timing

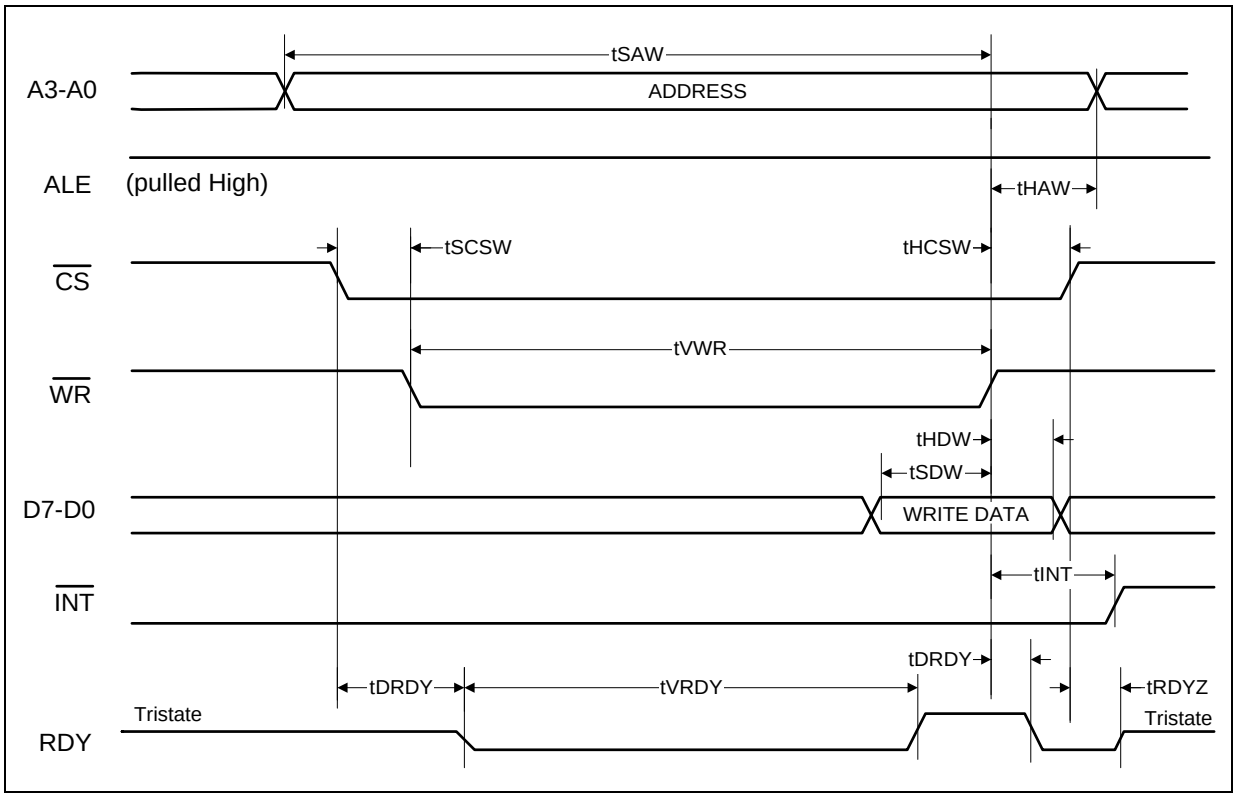


Figure 23. Multiplexed Intel Mode Write Timing

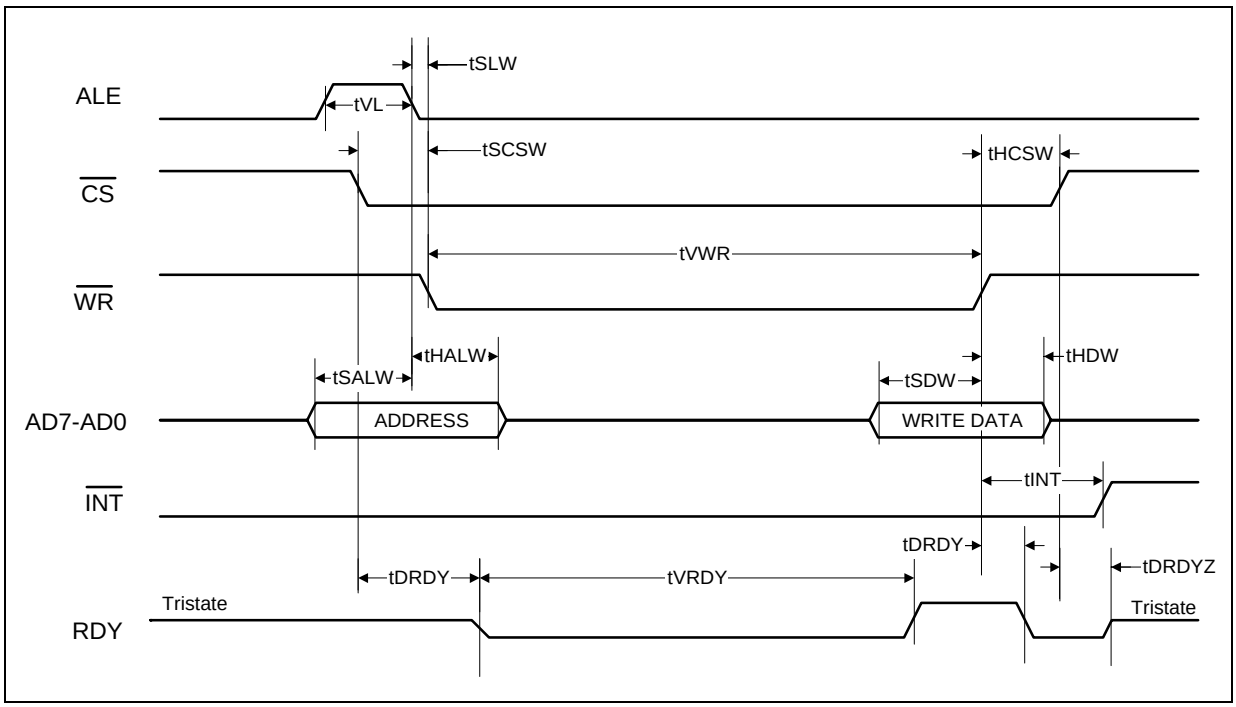


Table 37. Motorola Bus Read Timing Characteristics

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to address or data strobe	t_{SAR}	10	–	–	ns	
Address hold time from address or data strobe	t_{HAR}	5	–	–	ns	
Valid address strobe pulse width	t_{VAS}	95	–	–	ns	
R/$\overline{W}$ setup time to active data strobe	t_{SRW}	10	–	–	ns	
R/$\overline{W}$ hold time from inactive data strobe	t_{HRW}	0	–	–	ns	
Chip select setup time to active data strobe	t_{SCS}	0	–	–	ns	
Chip select hold time from inactive data strobe	t_{HCS}	0	–	–	ns	
Address strobe active to data strobe active delay	t_{ASDS}	20	–	–	ns	
Delay time from active data strobe to valid data	t_{PDS}	3	–	30	ns	
Delay time from inactive data strobe to data High Z	t_{DZ}	3	–	30	ns	
Valid datastrobe pulse width	t_{VDS}	60	–		ns	
Inactive data strobe to inactive $\overline{INT}$ delay time	t_{INT}	–	–	10	ns	
Data strobe inactive to address strobe inactive delay	t_{DSAS}	15	–	–	ns	
$\overline{DS}$ asserted to $\overline{ACK}$ asserted delay	t_{DACKP}	–	–	26	ns	
$\overline{DS}$ deasserted to $\overline{ACK}$ deasserted delay	t_{DACK}	–	–	10	ns	
Active $\overline{ACK}$ to valid data delay	t_{PACK}	–	–	0	ns	Design dependent

NOTES:
1. Typical figures are at 25 C° and are for design aid only: not guaranteed and not subject to production testing.
2. C_L= 100pF on D0-D7 All other outputs are loaded with 50pF.

Figure 24. Non-Multiplexed Motorola Mode Read Timing

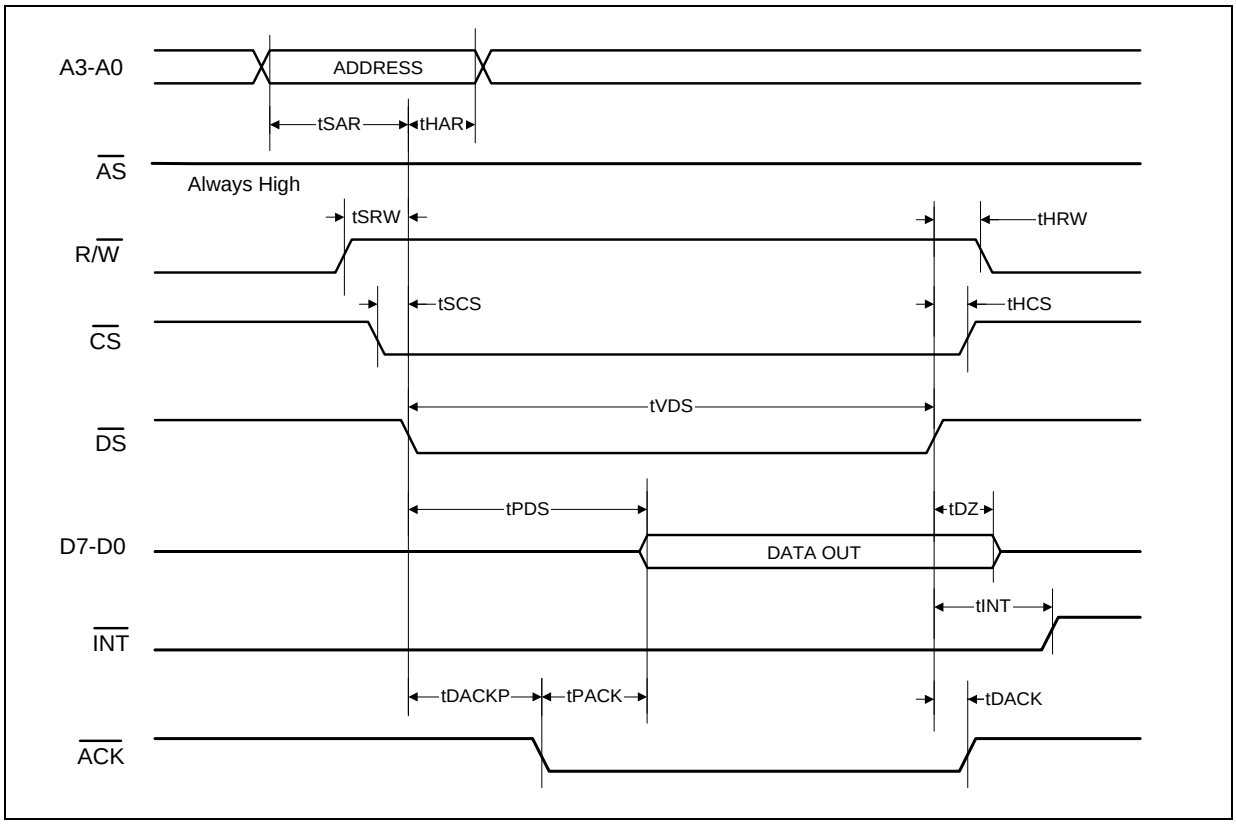


Figure 25. Multiplexed Motorola Mode Read Timing

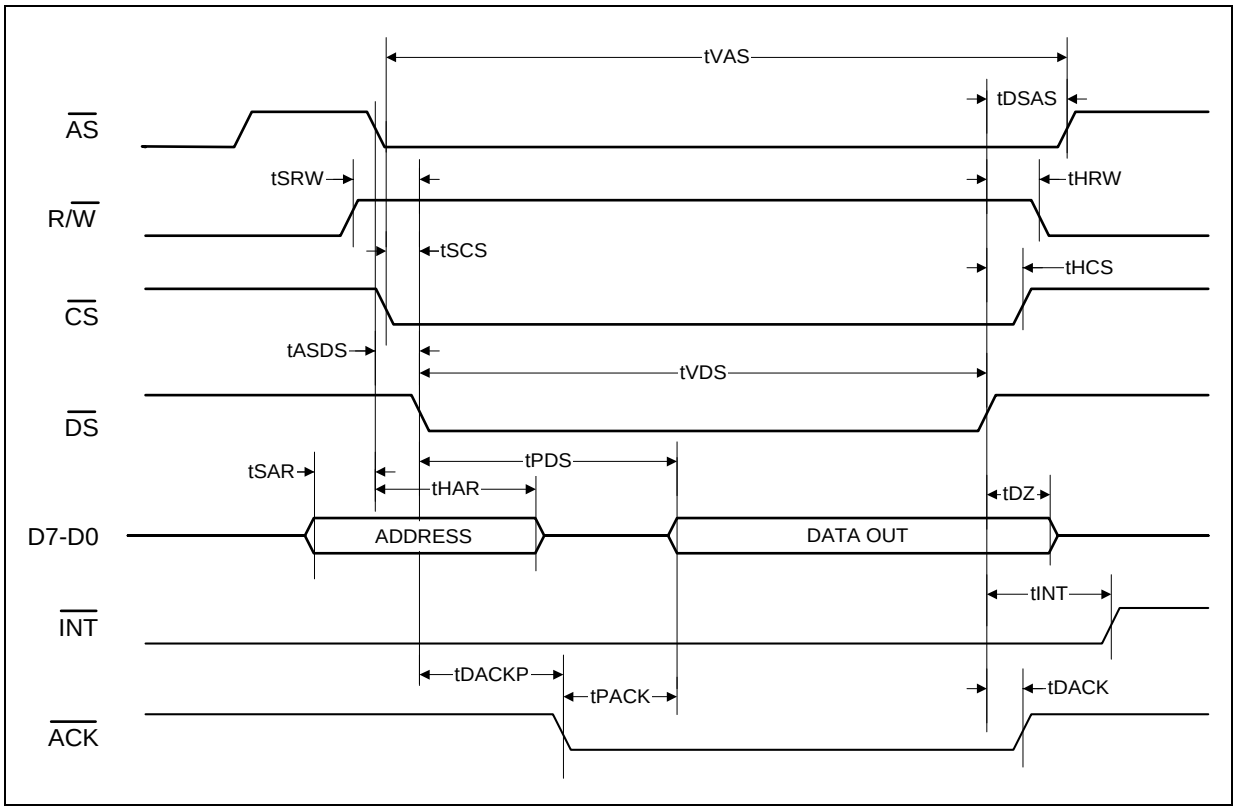


Table 38. Motorola Mode Write Timing Characteristics

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to address strobe	t_{SAS}	10	–	–	ns	
Address hold time to address strobe	t_{HAS}	5	–	–	ns	
Valid address strobe pulse width	t_{VAS}	95	–	–	ns	
R/$\overline{W}$ setup time to active data strobe	t_{SRW}	10	–	–	ns	
R/$\overline{W}$ hold time from inactive data strobe	t_{HRW}	0	–	–	ns	
Chip select setup time to active data strobe	t_{SCS}	0	–	–	ns	
Chip select hold time from inactive data strobe	t_{HCS}	0	–	–	ns	

NOTES:
1. Typical figures are at 25 C and are for design aid only: not guaranteed and not subject to production testing.
2. C_L = 100pF on D0-D7 All other outputs are loaded with 50pF.

Table 38. Motorola Mode Write Timing Characteristics (Continued)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address strobe active to data strobe active delay	tASDS	20	–	–	ns	
Data setup time to $\overline{DS}$ deassertion	tSDW	40	–	–	ns	
Data hold time from $\overline{DS}$ deassertion	tHDW	30	–	–	ns	
Valid datastrobe pulse width	tVDS	60	–	–	ns	
Inactive data strobe to inactive INT delay time	tINT	–	–	10	ns	
Data strobe inactive to address strobe inactive delay	tDSAS	15	–	–	ns	
Active data strobe to $\overline{ACK}$ output enable time	tDACK	0	–	12	ns	
$\overline{DS}$ asserted to $\overline{ACK}$ asserted delay	tDACKP	–	–	26	ns	

NOTES:
1. Typical figures are at 25 C and are for design aid only: not guaranteed and not subject to production testing.
2. C_L= 100pF on D0-D7 All other outputs are loaded with 50pF.

Figure 26. Non-Multiplexed Motorola Mode Write Timing

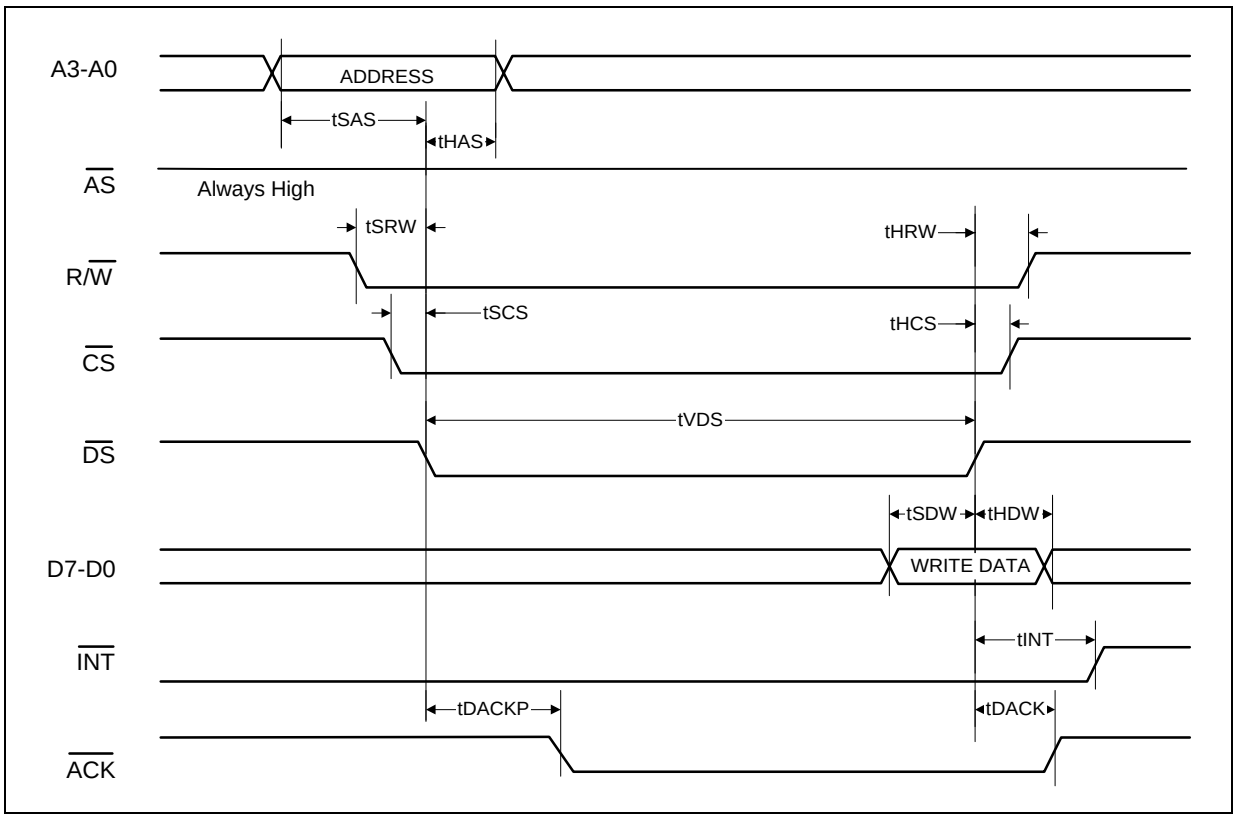


Figure 27. Multiplexed Motorola Mode Write Timing

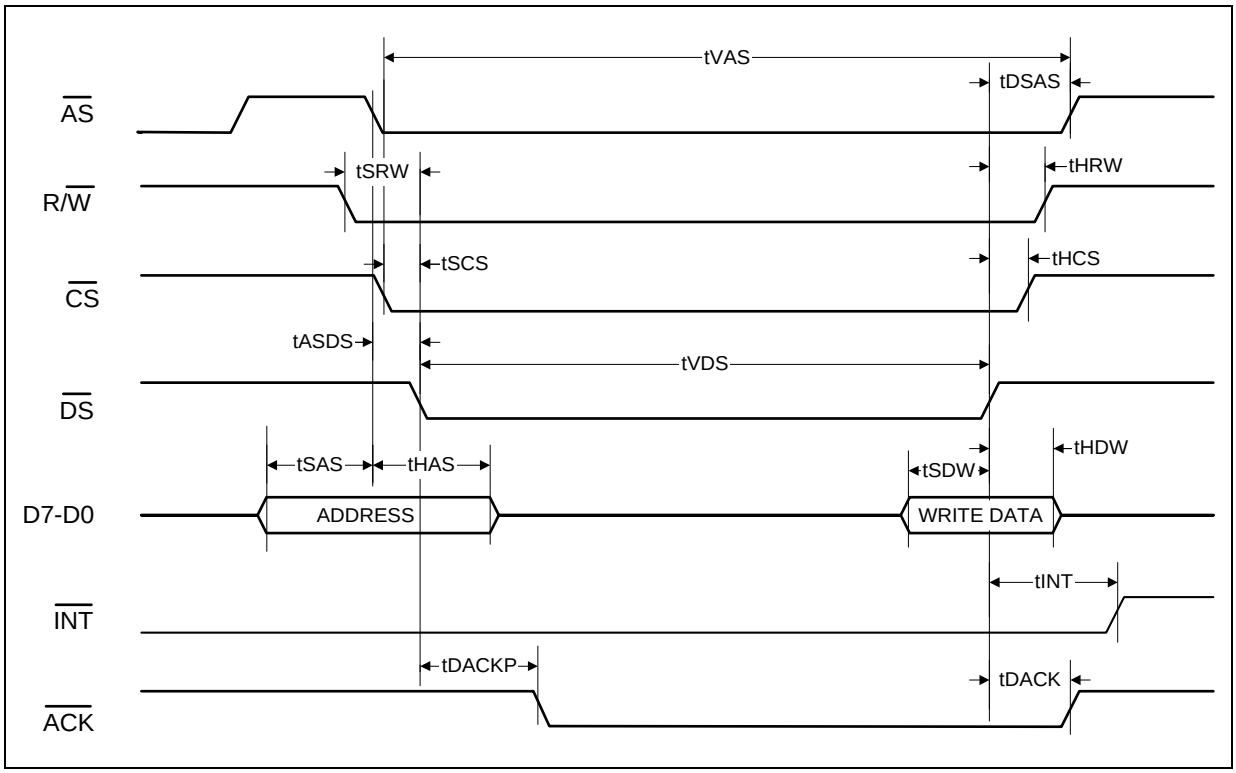


Table 39. Serial I/O Timing Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Condition
Rise/fall time any pin	t_{RF}	–	–	100	ns	Load 1.6mA, 50 pF
SDI to SCLK setup time	t_{DC}	5	–	–	ns	
SCLK to SDI hold time	t_{CDH}	5	–	–	ns	
SCLK Low time	t_{CL}	25	–	–	ns	
SCLK High time	t_{CH}	25	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
$\overline{CS}$ falling egde to SCLK rising edge	t_{CC}	10	–	–	ns	
Last SCLK edge to $\overline{CS}$ rising edge	t_{CCH}	10	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	50	–	–	ns	
SCLK to SDO valid delay time	t_{CDV}	–	–	5	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO High Z	t_{CDZ}	–	10	–	ns	
† Typical figures are at 25 C and are for design aid only: not guaranteed and not subject to production testing.						

Figure 28. Serial Input Timing

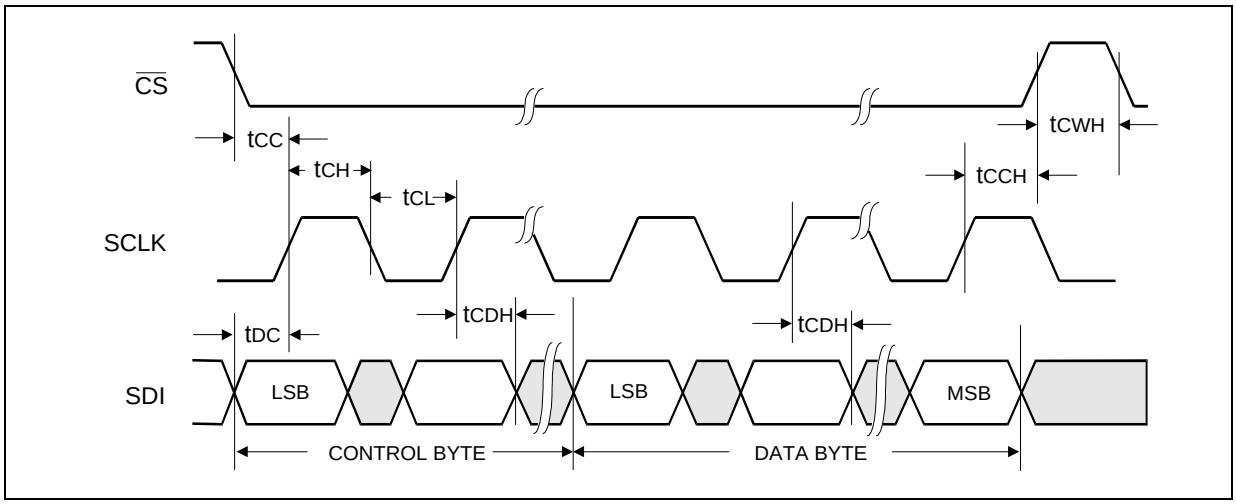


Figure 29. Serial Output Timing

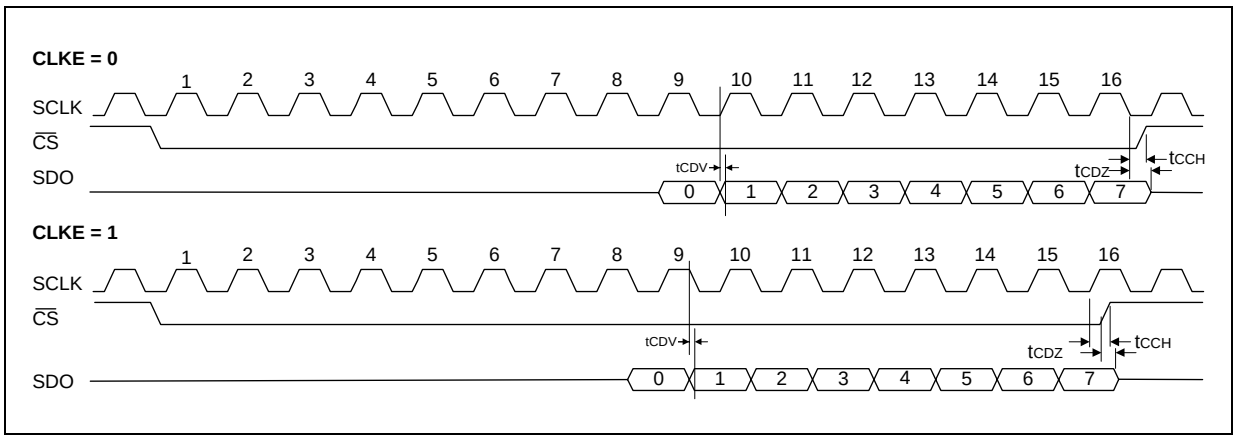


Table 40. Transformer Specifications

Tx/Rx	Turns Ratio	Primary Inductance mH (min.)	Leakage Inductance µH (max.)	Interwinding Capacitance pF (max.)	DCR Ω (max.)	Dielectric Breakdown Voltage V† (min.)
TX	1:2	1.2	0.60	60	0.70 pri 1.20 sec	1500 Vrms
RX	1:1	1.2	0.60	60	1.10 pri 1.10 sec	1500 Vrms

† This parameter is application dependent.

Table 41. G.703 2.048 Mbit/s Pulse Mask Specifications

Parameter	Cable		Unit
	TWP	Coax	
Test load impedancet	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Figure 30. E1 Mask Template

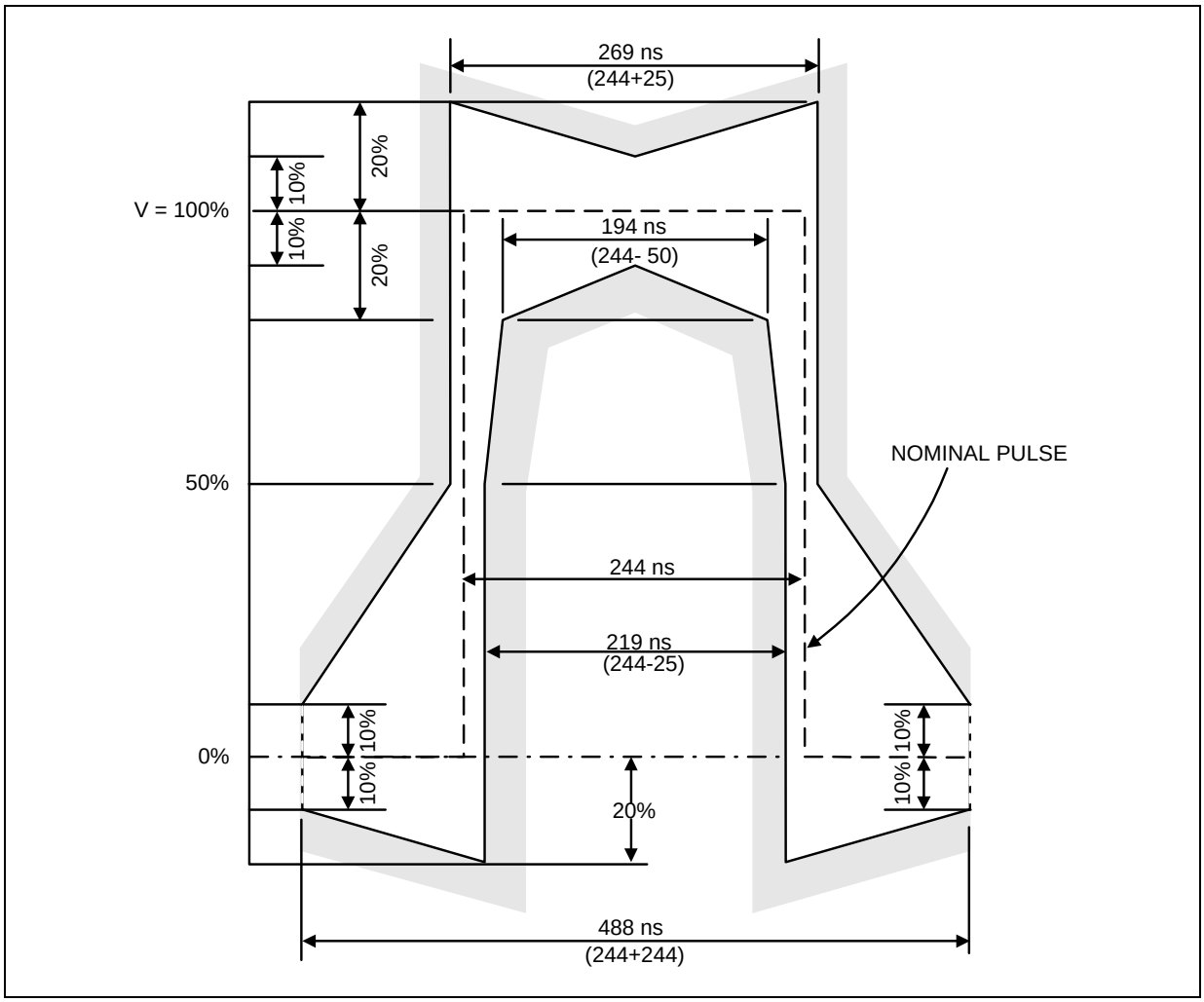
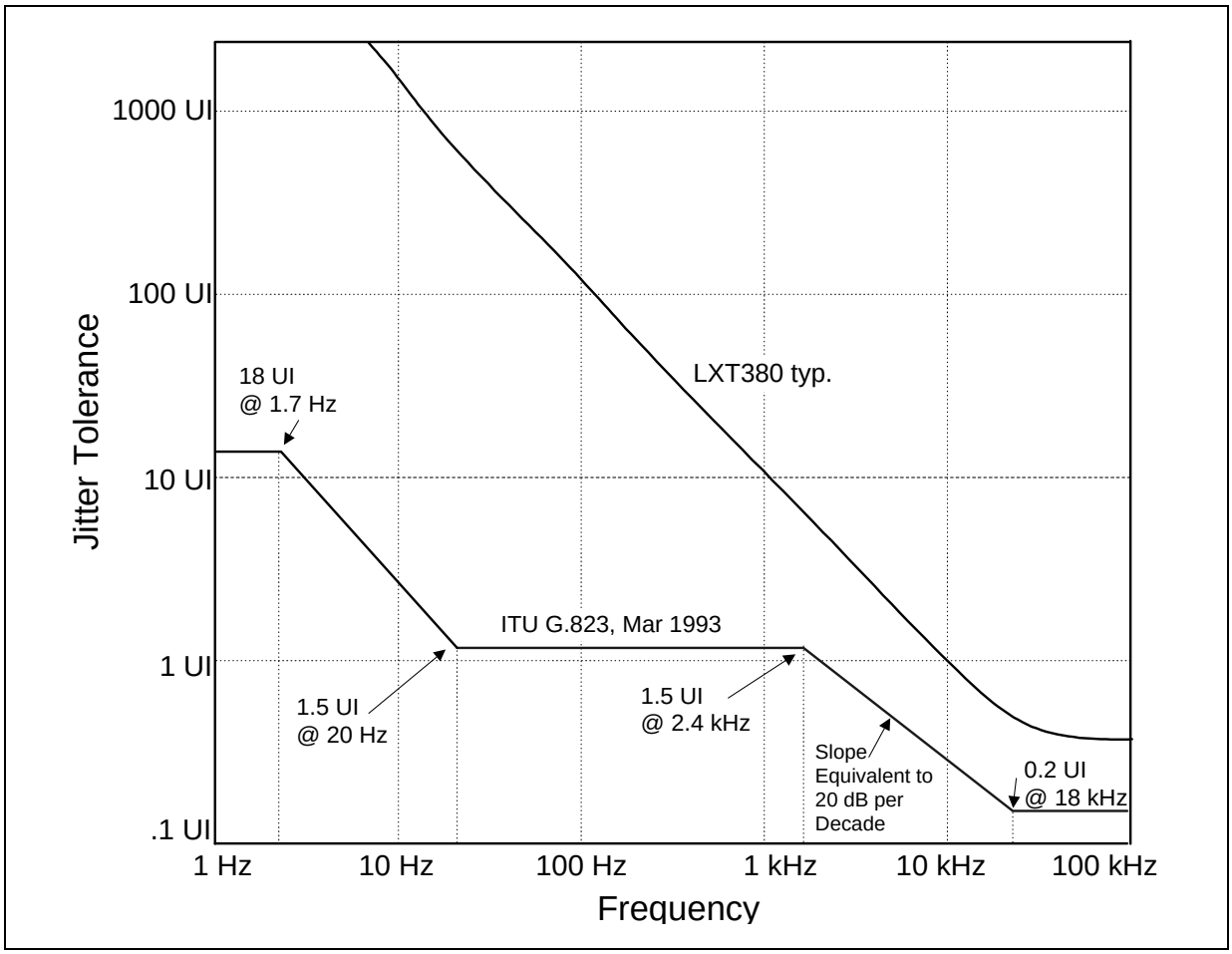


Figure 31. E1 Jitter Tolerance



5.1 Recommendations and Specifications

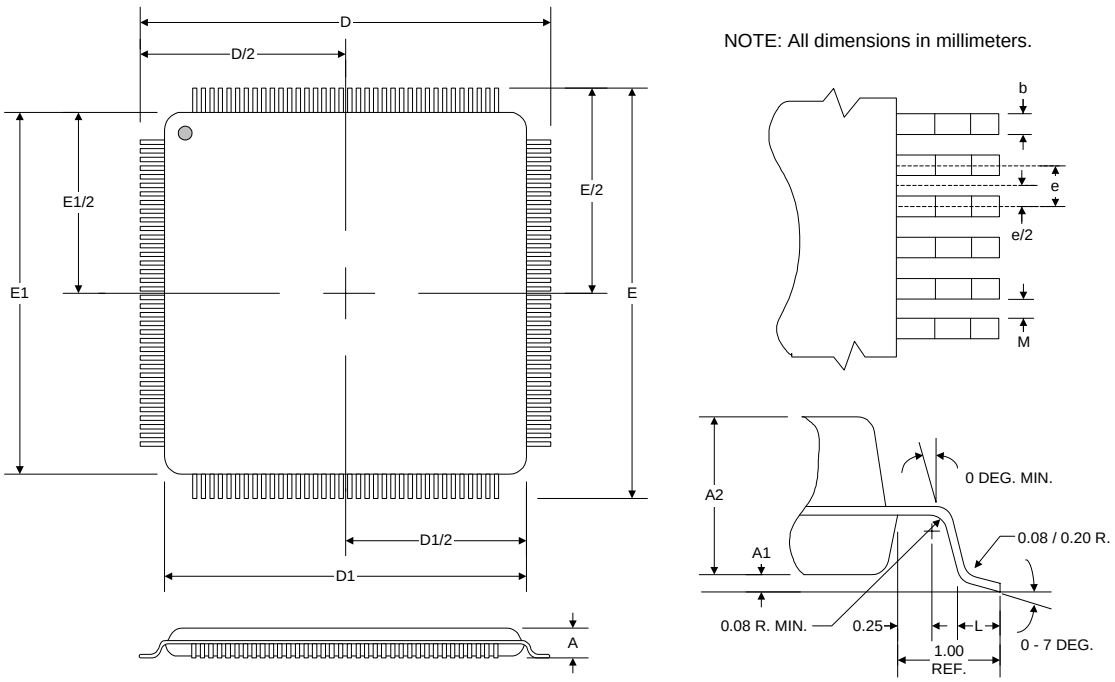
- G.703 Physical/electrical characteristics of hierarchical digital interfaces
- G. 704 functional characteristics of interfaces associated with network nodes
- G.735 characteristics of primary PCM multiplex equipment operating at 2048 kbit/s and offering digital access at 384 kbit/s and/or synchronous digital access at 64 kbit/s
- G.736 characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s
- G.772 protected monitoring points provided on digital transmission systems
- G.775 Loss of Signal (LOS) and Alarm Indication (AIS) defect detection and clearance criteria
- G.823 The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy
- O.151 Specification of instruments to measure error performance in digital systems
- OFTEL OTR-001 Short Circuit Current Requirements
- ETS 300166 Physical and Electrical Characteristics
- ETS 300386-1 Electromagnetic Compatibility Requirement

6.0 Mechanical Specifications

Figure 32. LXT380 144 Pin LQFP Package Dimensions

144-Pin Low-Profile Quad Flat Package

- Part Number LXT380LE
- Extended Temperature Range (-40 °C to 85 °C)



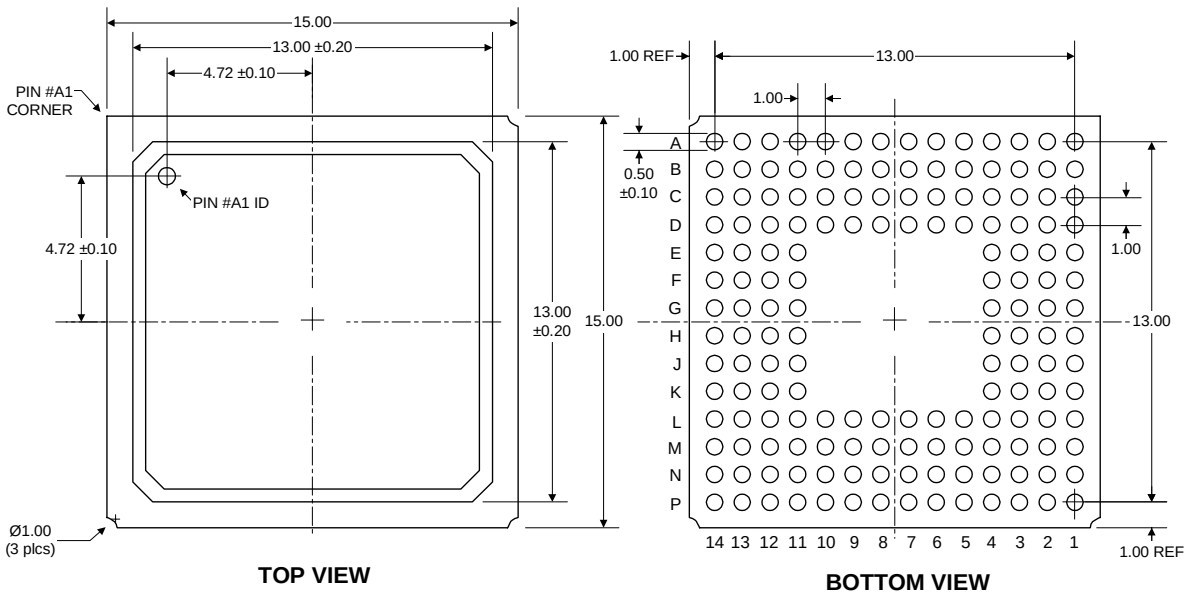
Dimension†	Millimeters		
	Minimum	Nominal	Maximum
A	–	–	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D		22.00 B.S.C.	
D1		20.00 B.S.C.	
E		22.00 B.S.C.	
E1		20.00 B.S.C.	
e		0.50 B.S.C.	
L	0.45	0.60	0.75
M	0.14	–	–

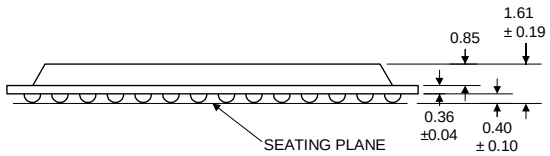
† See JEDEC Publication for additional specifications.

Figure 33. LXT380 160 Pin PBGA Package Dimensions

160-Pin Plastic Ball Grid Array

- Part Number LXT380BE
- Extended Temperature Range (-40 °C to 85 °C)





NOTE:

1. ALL DIMENSIONS IN MILLIMETERS.

2. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y 14.5M-1994.

3. TOLERANCE = ± 0.05 UNLESS SPECIFIED OTHERWISE.