SK70720 and SK70721

Multi-Rate DSL Data Pump Chip Set

Datasheet

The Multi-Rate DSL Data Pump is a complete, variable-rate transceiver that provides full duplex communication on two wires using echo-canceller-with-hybrid and 2B1Q line coding technology. It provides symmetrical line rates from 272 to 784 kbps. Performance specifications are defined at the 272, 400, 528, and 784 kbps data rates which provide a payload of 4, 6, 8, or 12 64 kbps channels with a 16 kbps overhead channel. The MDSL Data Pump also supports applications where the payload is unchannellized.

The MDSL Data Pump chip set consists of two devices:

- SK70720 MDSL Digital Signal Processor (MDSP)
- SK70721 Integrated Analog Front-End (IAFE)

The IAFE is a fully integrated CMOS analog front-end IC which includes transmitter line drivers, filters, and 2B1Q encoding functions along with the receiver hybrid, AGC, A-to-D converter modulator and VCXO functions. The MDSP incorporates all digital signal processing required for A/D conversion, echo-cancellation, data scrambling and adaptive equalization as well as transceiver activation state machine control.

Applications

- High speed residential Internet access
- Extended Range fractional T1/E1 transport
- 4 to 12-channel digital pair-gain
- Wireless base station to switch access
- WAN access for LAN routers
- Video Conferencing

As of January 15, 2001, this document replaces the Level One document *SK70720 and SK70721 — Multi-Rate DSL Data Pump Chip Set*.

Order Number: 249209-001
January 2001

Datasheet

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Revision History

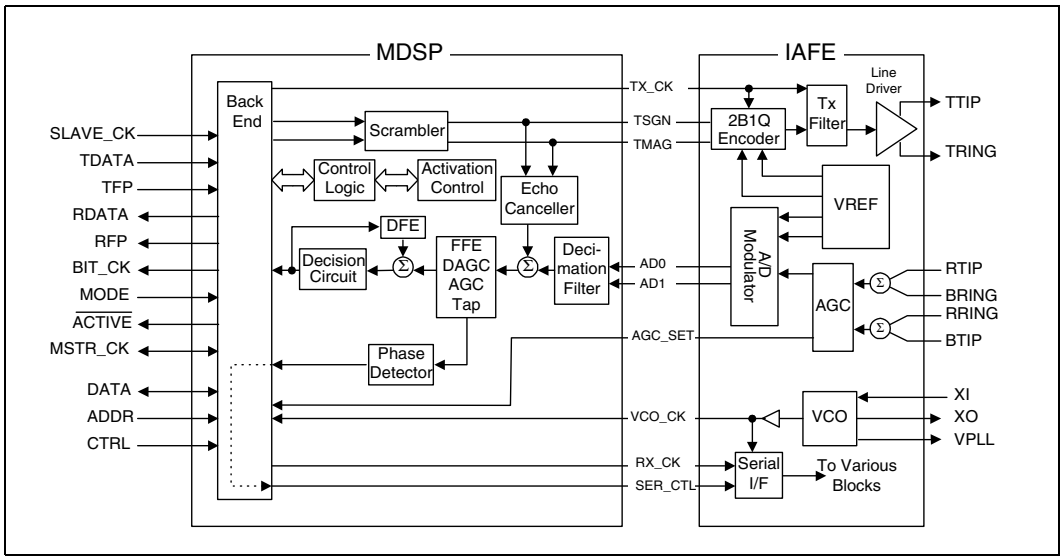
Revision	Date	Description

1.0 Features

- Fully integrated, 2-chip transceiver
- Compliant with the following standards:
  - ITU G.991.1
  - ANSI Committee T1E1 .4-TR28 (T1E1.4/96-006)
  - ETSI ETR -152
- Integrated line drivers, filters and hybrid circuits reduce the number of external components required
- Self-contained activation/start-up control eliminates an external microprocessor in many applications
- Parallel interface for processor control or monitoring
- Single +5V supply
- Typical power dissipation less than 500 mW—good for applications with remote power feeding
- Supports transparent repeater applications without an external processor or glue-logic
- Supports processor directed rate selection driven by receive signal level and noise margin
- Continuously adaptive echo canceller and equalizers maintain excellent transmission performance with changing noise and line characteristics
- Typical noise-free transmission range*:

  272 kbps
  25.3 kft (7.7 km) on #24 AWG (0.5 mm) cable
  17.1 kft (5.2 km) on #26 AWG (0.4 mm) cable
  784 kbps
  19.8 kft (6.0 km) on #24 AWG (0.5 mm) cable
  13.7 kft (4.2 km) on #26 AWG (0.4 mm) cable
  * Refer to AN76 or SK70725/21 data sheet for details.

Figure 1. SK70720 and SK70721 Block Diagram

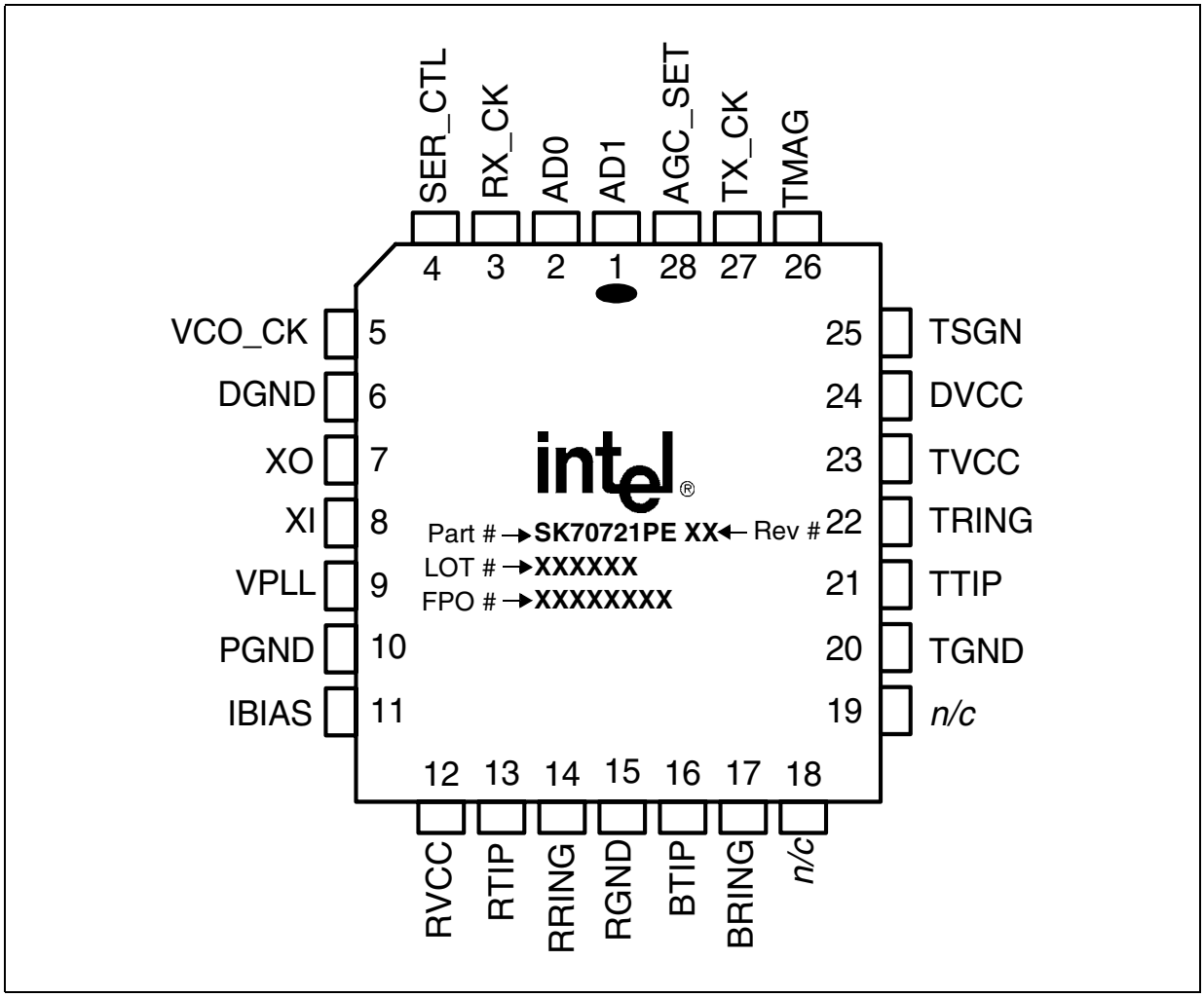


2.0 Pin Assignment and Signal Descriptions

The IAFE is packaged in a 28-pin PLCC. Figure 2 shows the IAFE pin locations and Table 1 lists signal descriptions.

The MDSP device is packaged in a 44-pin PLCC. Figure 3 shows MDSP pin designations and Table 2 lists signal descriptions.

Figure 2. SK70721 IAFE Pin Locations



Package Topside Markings	
Marking	**Definition**
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.

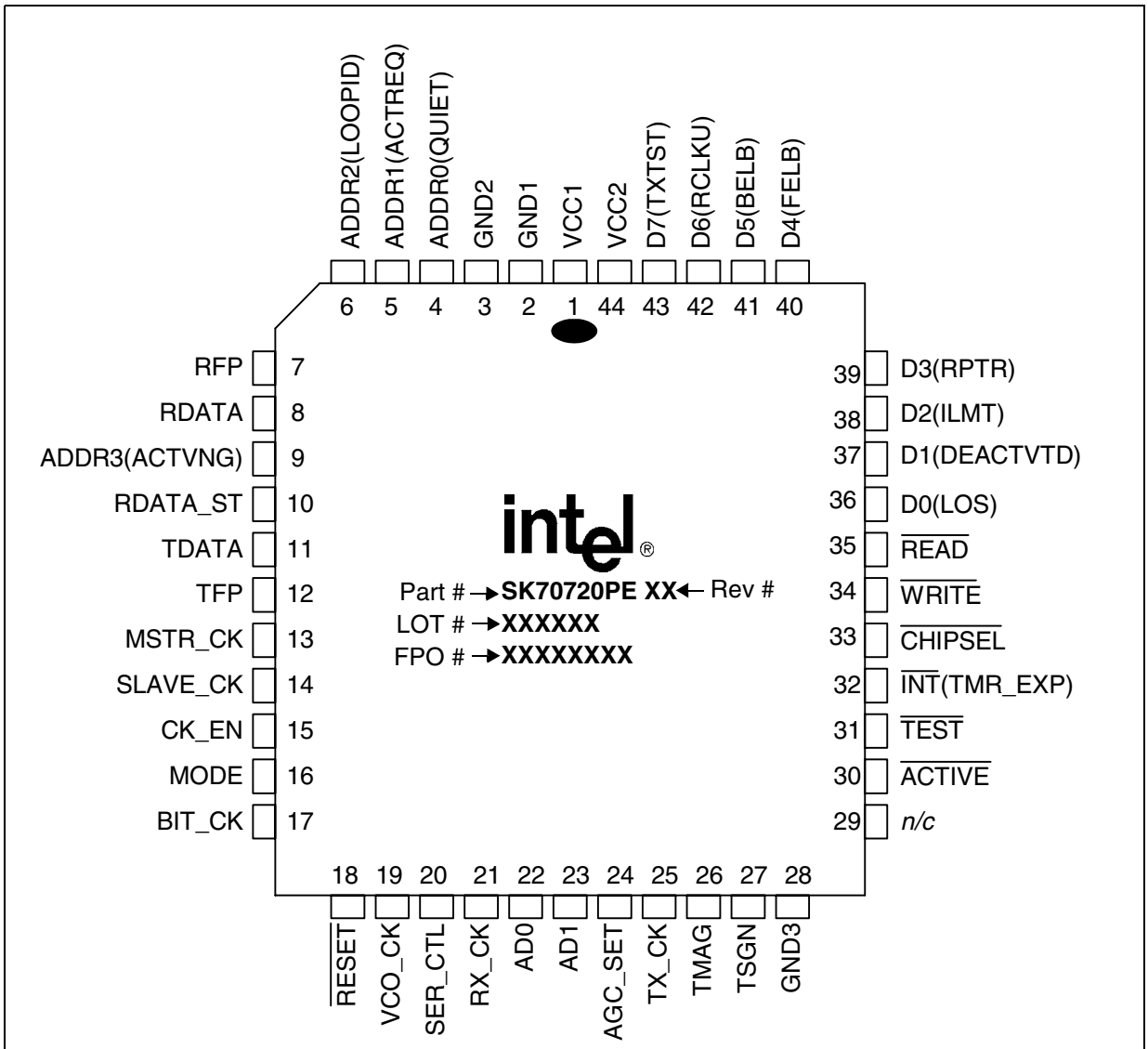
FPO #	Identifies the Finish Process Order.

Table 1. SK70721 IAFE Pin Assignments/Signal Descriptions

Group	Pin #	Symbol	I/O[1]	Description
Line	13	RTIP	AI	**Receive Tip and Ring.** Receiver differential inputs.
	14	RRING	AI	
	16	BTIP	AI	**Receive Balance Tip and Ring.** Receiver hybrid balance inputs.
	17	BRING	AI	
	21	TTIP	AO	**Transmit Tip and Ring.** Line driver outputs.
	22	TRING	AO	
PLL	7	XO	AO	**Crystal Oscillator Input and Output.** Connect a pullable crystal whose frequency is 32 times the bit rate between these two pins. Refer to the Applications Section for crystal specifications.
	8	XI	AI	
	9	VPLL	AO	**PLL Control Voltage.** Control signal for the VCXO.
Power	10	PGND	S	**PLL Ground.** 0 V.
	12	RVCC	S	**Receive Power Supply.** +5 VDC (± 5%).
	23	TVCC	S	**Transmit Power Supply.** +5 VDC (± 5%).
	24	DVCC	S	**Digital Power Supply.** +5 VDC (± 5%).
	6	DGND	S	**DVCC Ground.** 0 V.
	15	RGND	S	**RVCC Ground.** 0 V.
	20	TGND	S	**TVCC Ground.** 0 V.
Clock and Control	3	RX_CK	DI	**Receive Baud Rate Clock Input.**
	4	SER_CTL	DI	**Serial Control Input.**
	5	VCO_CK	DO	**MDSL Reference Clock Output.** Used as the receive timing reference for the MDSP.
	27	TX_CK	DI	**Transmit Symbol Clock Input.** 16 times the transmit symbol rate.
Data Input and Output	28	AGC_SET	DO	**AGC Adjust Output.**
	1	AD1	DO	**A-to-D Converter Data Line 1.**
	2	AD0	DO	**A-to-D Converter Data Line 0.**
	25	TSGN	DI	**Transmit Quat Sign Input.**
	26	TMAG	DI	**Transmit Quat Magnitude.**
Analog Input	11	IBIAS	AI	**Input Bias.** This input sets internal bias currents.
No Connects	18 19	n/c	-	**Not Connected.** No internal connection

1. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Figure 3. SK70720 MDSP Pin Assignments



NOTE: Pin Functions in Hardware Control Mode are shown in parentheses.

Package Topside Markings	
Marking	**Definition**
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 2. SK70720 MDSP Pin Assignments/Signal Descriptions

Group	Pin #	Symbol	I/O[4]	Description
Power	1	VCC1	S	**Logic Power Supply.** (Refer to Table 17).
	44	VCC2	S	**I/O Power Supply.** +5 VDC (± 5%).
	2	GND1	S	**Ground 1.** 0 V.
	3	GND2	S	**Ground 2.** 0 V.
	28	GND3	S	**Ground 3.** 0 V.
Misc	29	n/c	–	No internal connection.
	31	TEST	DI[1]	**Test**. Reserved for factory testing. Tie High for normal operation.
	18	RESET	DI[1]	**Reset.** Pulse Low to initialize internal circuits.
User Port[2]	10	RDATA_ST	DO	**Receive Data Strobe.** RDATA_ST goes High for 18 consecutive BIT_CK periods to indicate four stuffing bits (b4703 - 4706) and 14 frame bits (b1-14) on RDATA.
	16	MODE	DI	**Mode Select.** When MODE is High, the Data Pump operates in Master mode so that it is the link timing source and initiates activation. When MODE is Low, the Data Pump operates in Slave mode. Tied to internal pull-up device. *The MDSP must be reset after the MODE is changed.*
	17	BIT_CK	DO	**Bit Rate Clock.** This clock transfers data into and out of the MDSL data interface at the bit rate. MSTR_CK is the source of BIT_CK in Master Mode. VCO_CK is the source of BIT_CK in Slave Mode.
	30	ACTIVE	DO	**Link Active Indicator.** $\overline{\text{ACTIVE}}$ goes Low upon the receipt of two consecutive frame sync words. $\overline{\text{ACTIVE}}$ goes High when the frame sync word is not detected in six consecutive frames.
	8	RDATA	DO	**MDSL Receive Data Output.** When $\overline{\text{ACTIVE}}$ is Low, the receive data including frame sync and stuff bits are output on RDATA. RDATA is High when $\overline{\text{ACTIVE}}$ is High.
	7	RFP	DO	**Receive Frame Pulse.** Low for one BIT_CK cycle during the last bit of the current MDSL receive frame on RDATA, either b4702 or b4706. RFP is valid when $\overline{\text{ACTIVE}}$ is Low.
	11	TDATA	DI[1]	**MDSL Transmit Data Stream.** When $\overline{\text{ACTIVE}}$ is Low, the Data Pump samples data on TDATA except during frame sync and stuff bits.
	12	TFP	DI[1]	**Transmit Frame Pulse.** TFP should be Low for one BIT_CK cycle the during last bit of the current MDSL frame on TDATA. *If TFP is pulled Low and is Low again three BIT_CK cycles later, RDATA, RFP, RDATA_ST, BIT_CK, CK_EN, and $\overline{\text{ACTIVE}}$ will tri-state until the device is reset.* Tied to an internal pull-up device.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The frame period is 2351 or 2353 baud times. See "Framing" on page 16.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output;
   AI/O = Analog Input/Output; S = Supply.

Table 2. SK70720 MDSP Pin Assignments/Signal Descriptions (Continued)

Group	Pin #	Symbol	I/O[4]	Description
Hardware Interface *(Hardware Control Mode)*	4	QUIET	DI[3]	**Quiet Mode Enable.** Set High to force the MDSP into the Deactivated State. Set Low to enable activation requests (see ACTREQ).
	5	ACTREQ	DI[3]	**Activation Request (Master mode) (no function in Slave mode).** Tie this pin Low in Slave mode. When QUIET is Low, a rising edge on this pin initiates activation. The signal is ignored after activation (see QUIET).
	6	LOOPID	DI[3]/O	**Loop Number Input (Master mode) or Loop Number Indicator (Slave mode).** This indicator is transmitted from the link Master to the slave and can be used for loop identification in systems that multiplex data onto multiple MDSL lines. In Slave mode LOOPID is valid only when $\overline{\text{ACTIVE}}$ is Low.
	9	ACTVNG	DO	**Activating State Indication.** ACTVNG goes High when the MDSP is in the Activating State.
	32	TMR_EXP	DO	**Timer Expiration Indicator.** TMR_EXP goes High to indicate the expiration of the activation timer.
	33	CHIPSEL	DI[3]	**Chip Select** — Assert these three pins Low to activate Hardware Control Mode. When any of them is High, the MDSP reverts immediately to Software Control Mode.
	34	WRITE	DI[3]	**Write Pulse**
	35	READ	DI[3]	**Read Pulse**
	36	LOS *(Master)*	DO	**Loss of Signal Indicator.** In Master mode, LOS goes High when the Data Pump enters the Inactive State. When the Data Pump reaches the Deactivated State from Active-1 or Active-2, it starts the Loss of Signal (LOS) timer after Slave transmission stops. When the LOS timer expires, the Data Pump goes to the Inactive State. When the Data Pump transitions from the Activating State directly to the Deactivated State, it may immediately enter the Inactive State without waiting for Slave transmission to cease (Figure 10).
		LOS *(Slave)*	DO	**Loss of Signal Indicator.** In Slave mode, LOS goes High immediately when loss of signal energy is detected and the data pump enters the Inactive State (Figure 11).
	37	DEACTVTD	DO	**Deactivation Indicator.** DEACTVTD goes High when the Deactivation timer expires and the data pump goes from the Pending Deactivation state to the Deactivated state.
	38	ILMT	DI[1]	**Insertion Loss Measurement Test.** Set High to transmit a framed & scrambled, “all 1s”, 2B1Q pulse sequence. Pulse sequence will have a valid sync word. In the Slave configuration, when the ILMT mode is selected, the Data Pump may begin activation.
	39	RPTR	DI[1]	**Repeater Mode Enable.** When in Master mode, setting RPTR High configures the data pump to derive timing from the MSTR_CK output of an adjacent device for transparent repeater applications. The BIT_CK output phase is aligned to the TFP input pulse width. RPTR is ignored in Slave mode.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The frame period is 2351 or 2353 baud times. See “Framing” on page 16.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output;
   AI/O = Analog Input/Output; S = Supply.

Table 2. SK70720 MDSP Pin Assignments/Signal Descriptions (Continued)

Group	Pin #	Symbol	I/O[4]	Description
Hardware Interface *(Hardware Control Mode) -cont'd*	40	FELB	DI[1]	**Front-End Loopback (Master only).** In the Inactive State, set High to cause the IAFE to loopback. The returned signal activates the MDSP which receives its own transmitted data. The chip set ignores incoming data from the Slave during loopback.
	41	BELB	DI[1]	**Back-End Loopback.** In the Active-1 or Active-2 states, setting BELB High forces an internal, transparent loopback with RDATA connected to TDATA and RFP connected to TFP.
	42	RCLKU	DO	**Receive Baud Rate Clock.** Aligned with BIT_CK in Slave mode, phase synchronous with receive pulse stream, However, during Activating State, the clocks may not be aligned. In the Master mode RCLKU has a constant, arbitrary, phase relationship with BIT_CK in Active State.
	43	TXTST	DI[1]	**Transmit Test.** Set high to enable isolated transmit pulse generation. TDATA controls the sign and TFP controls the magnitude of the transmitted quat pulses according to the 2B1Q encoding rules. In the Slave configuration, when the TXTST mode is selected, the Data Pump may begin activation.
Processor Interface (Software Control Mode)	36	D0	DI[1]/O	**Data bit 0.** Eight-bit, parallel data bus.
	37	D1	DI[1]/O	Data bit 1
	38	D2	DI[1]/O	Data bit 2
	39	D3	DI[1]/O	Data bit 3
	40	D4	DI[1]/O	Data bit 4
	41	D5	DI[1]/O	Data bit 5
	42	D6	DI[1]/O	Data bit 6
	43	D7	DI[1]/O	Data bit 7
	4	ADDR0	DI[3]	**Address bit 0.** Four-bit address, selects read or write register.
	5	ADDR1	DI[3]	Address bit 1
	6	ADDR2	DI[3]	Address bit 2
	9	ADDR3	DI[3]	Address bit 3
	32	INT	DO	**Interrupt Output.** Open drain output. Requires an external 10 kΩ pull up resistor. Goes Low on interrupt.
	33	CHIPSEL	DI[3]	**Chip Select.** Pull Low to read or write to registers.
	34	WRITE	DI[3]	**Write Pulse.** Pull Low to write to registers.
	35	READ	DI[3]	**Read Pulse.** Pull Low to read from registers.

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The frame period is 2351 or 2353 baud times. See "Framing" on page 16.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output;
   AI/O = Analog Input/Output; S = Supply.

Table 2. SK70720 MDSP Pin Assignments/Signal Descriptions (Continued)

Group	Pin #	Symbol	I/O[4]	Description
Clock and Control	14	SLAVE_CK	DI[3]	**Slave Mode Reference Clock.** Mandatory in Slave mode. Tie High or Low in Master Mode. Clock input requires ± 32 ppm accuracy.
	15	CK_EN	DO	**Slave Mode Reference Clock Enable.** Active High enable for the SLAVE_CK clock. In slave mode, this pin goes Low to indicate the PLL is tracking the input signal from the master. Not used in master mode.
	13	MSTR_CK	DI[1] DO	**16x MDSL Reference Clock.** In Master Mode, this clock generates transmit and receive timing and must have ±32 ppm accuracy. In Slave Mode, this output is derived by dividing VCO_CK by two so that it may drive the MSTR_CK input of another data pump configured for Master mode as a repeater (with RPTR High).
	19	VCO_CK	DI	**32x Receive Clock Input.**
	20	SER_CTL	DO	**Serial Control Output.**
	21	RX_CK	DO	**Receive Baud Rate Clock.** Derived from VCO_CK.
	22	AD0	DI	**Analog to Digital Converter Data Line 0.**
	23	AD1	DI	**Analog to Digital Converter Data Line 1.**
	24	AGC_SET	DI	**AGC Adjust Input.**
	25	TX_CK	DO	**Transmit Symbol Clock Output.**
	26	TMAG	DO	**Transmit Quat Magnitude Bit.**
	27	TSGN	DO	**Transmit Quat Sign Bit.**

1. This input is a Schmidt Triggered circuit and includes an internal pull-up device.
2. The frame period is 2351 or 2353 baud times. See "Framing" on page 16.
3. This input is a Schmidt Triggered circuit and includes an internal pull-down device.
4. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output;
   AI/O = Analog Input/Output; S = Supply.

3.0 Functional Description

The MDSL Data Pump (MDP) provides synchronous, full duplex transmission on a single pair of wires using 2B1Q line coding and echo cancellation. The Data Pump supports symmetrical line rates from 272 to 784 kbps and provides complete start up and operation without an external processor. The MDP may be used to transport framed or unframed data which is synchronous, asynchronous, or near-synchronous to the clock rate of the data pump. This section provides an overview of how the MDP data interface functions to support these applications. For a detailed explanation on the how to configure the MDP for a specific application refer to the section entitled "MDSL Data Interface."

Figure 4 illustrates data transport using the MDSL system. Data is clocked into a transmitter, sent over the line, and clocked out of the receiver of the far-end transceiver. Data is transmitted simultaneously in both directions.

3.1 Framing

The MDP embeds a 14-bit frame synchronization word (FSW) in the data stream that divides the data into 4702-bit MDSL frames as shown in Figure 5. The framing signal serves three purposes:

1. It allows automatic activation and deactivation based on receiver frame sync word detection.
2. It allows the average data rate in each direction of transmission to be adjusted while maintaining a constant line rate.
3. It provides an MDSL frame position indicator that may be used in unframed time-division-multiplexed systems to relate time slots in the MDSL frame to those in an application frame. (See Note below)

Note: The MDP frame sync word format and frame length are fully compatible with those defined for 784 kbps HDSL applications in ITU G.991.1, ANSI Committee T1E1.4-TR28 (T1E1.4/96-006), and ETSI ETR-152 standards. The MDP is fully transparent to all data except the frame sync word. It does not provide any other framing functions defined for HDSL.

Each frame contains 4688 payload data bits, and there are no restrictions on the data patterns which can be transmitted in the payload data. The application synchronizes data to the MDP framing by generating a pulse on the transmit frame pulse input, TFP. The transmitter sends the FSW in the first 14 bits following the rising edge of TFP. Application data is not transmitted or buffered during the transmission of the FSW.

Figure 4. MDSL System Data Transport

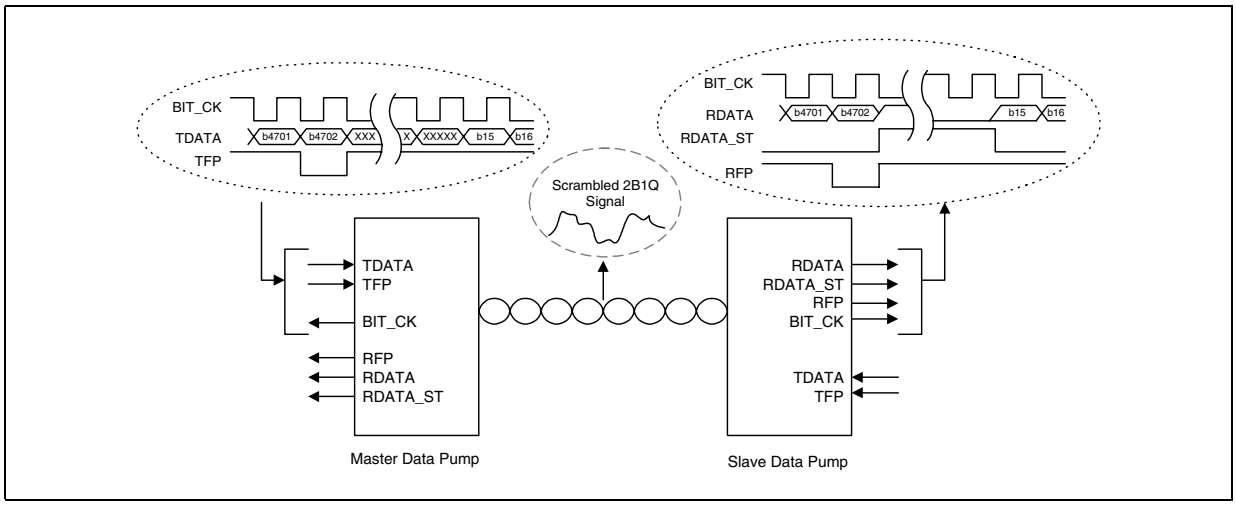
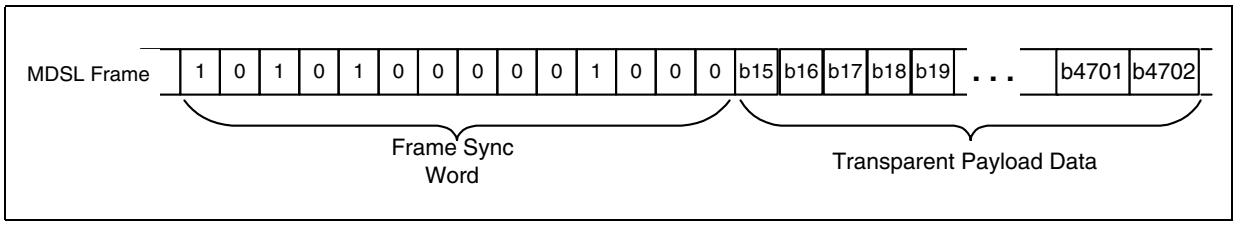


Figure 5. MDSL Frame



The MDP receiver detects the incoming FSW and provides a blanking signal (RDATA_ST) at its output to indicate that payload data is not present during the FSW. The RDATA_ST signal can also be used to gate the receiver clock signal (BIT_CK) so that clock transitions are present only when payload data is available. The resulting gapped clock is similar to that found in many other data transport systems.

The MDP has two modes of operation: Fixed Data Rate and Variable Data Rate.

3.1.1 Fixed Data Rate Mode

In Fixed Data Rate Mode, the MDP transports one data bit for each cycle of the bit clock (BIT_CK) except during the 14-bit FSW at the start of each frame. Data may be either synchronous (one data bit per available clock cycle) or asynchronous (data sent only when available). In both cases, the transmitter samples the transmit data signal (TDATA) on the rising edge of BIT_CK and reproduces that signal at the output of the receiver (RDATA) so that it is valid on the rising edge of the receiver BIT_CK. An external frame counter is required to provide a transmit frame pulse every 4702 BIT_CK cycles to synchronize the Data Pump frame position to the gapped data.

In applications where the data is formatted into logical frames or packets there is no requirement for a fixed mapping between the application frames and MDSL frames since the data contains the framing information required to give it meaning. Unless the application frame size divides evenly into the MDSL frame size, it is best to embed application framing information with the data rather

than to create a fixed mapping between specific time slots in the MDSL and application frames. With unframed, time-division multiplexed data defined relative to an application frame pulse it is necessary to establish a fixed mapping between application frame and MDSL frame boundaries.

Table 3 shows the payload data rate and frame length for some common values of line rates.

Table 3. Data Rate and Frame Length Examples

Line Rate (kbps)	Payload Data Rate (kbps)	Frame Length (ms)
272	271.190	17.287
400	398.809	11.755
528	526.428	8.905
784	781.666	5.997

3.1.2 Variable Data Rate Mode

Some applications require that data be transported at a rate which is externally controlled and varies a small amount from a nominal payload data rate. The MDP has a variable rate operating mode which allows the application to modify the payload data rate without changing the line rate so that each of the payload bits contains a valid data bit. To operate in this mode, the MDP uses a mechanism known as stuffing. By properly choosing the line rate of the MDSL system and using the stuffing mechanism, the application can transmit data at slightly different rates in both directions simultaneously while still using a common, fixed MDSL line rate.

When stuffing is employed, the application inserts an additional four bits not carrying payload data in the data stream between the end of the 4688 payload bits and the beginning of the next FSW as shown in Figure 6. This is accomplished by delaying the TFP pulse by four BIT_CK periods from its normal position. The MDP receiver detects this four bit change in the location of the FSW and adjusts its payload data strobe indicator (RDATA_ST) to indicate that the four additional bits do not contain payload data and should be suppressed along with the FSW which follows them. This mode of operation is frequently used in the transport of T1 signals where the upstream data rate is not identical to the downstream data rate.

Figure 6. Variable Data Rate Mode Framing

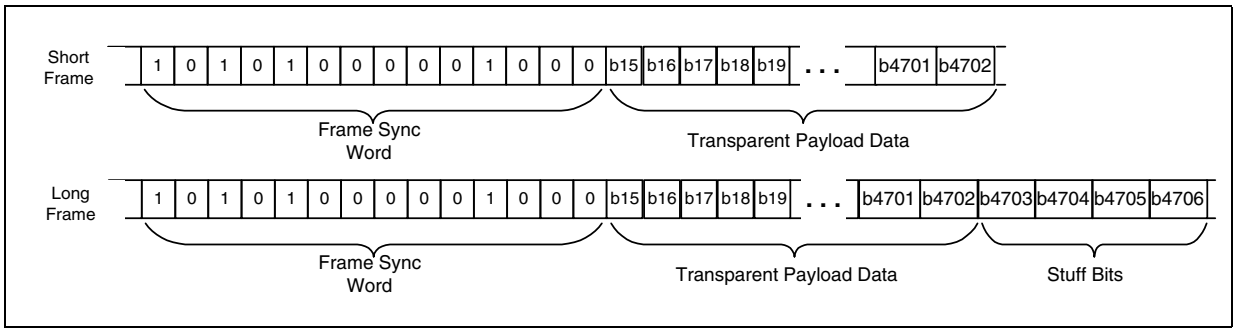


Table 4 provides the minimum and maximum data rates and frame times for several line rates. Although the MDP can only transport data at either of these two instantaneous rates, it can support any average data rate between them by adjusting the ratio of frames with stuffing to those without stuffing. When 50% stuffing is used the MDP will transport data at the nominal rate shown below. If necessary, a PLL tracking the receive frame pulse output (RFP) can be used to create a continuous (i.e., not gapped) clock whose frequency follows the average receive data rate.

3.2 Component Description

The following paragraphs describe the chip set components individually with reference to internal functions and the interfaces between Data Pump components.

3.2.1 Integrated Analog Front End (IAFE)

The IAFE incorporates the following analog functions:

- the transmit driver
- transmit and receive filters
- Phase-Locked Loop (PLL)
- hybrid circuitry analog-to-digital converter

The IAFE provides the complete analog front end for the MDSL Data Pump. It includes transmit pulse shaping, line driver, receive A/D modulator, and the VCO portion of the receiver PLL function. Transmit and receive controls are implemented through the serial port. The IAFE line interface uses a single twisted pair line for both transmit and receive. Table 5 lists the IAFE pin descriptions. Refer to Test Specifications for IAFE electrical and timing specifications.

3.2.1.1 IAFE Transmitter

The IAFE performs the pulse shaping and driving functions. The IAFE transmitter generates a 4-level output defined by TMAG and TSGN. Table 5 lists 2B1Q pulse coding parameters. Refer to Test Specifications for frequency and voltage templates.

3.2.1.2 IAFE Receiver

The IAFE receiver is a sophisticated sigma-delta converter. It sums the differential signal at RTIP/RRING minus the signal at BTIP/BRING. The first A/D signal comes out of AD0 at the rate of 64 times the 2B1Q symbol rate. The second stage of the A/D samples the noise of the first and generates the AD1 bit stream at the rate of 64 times the symbol rate.

Receiver gain is controlled by the MDSP via the AGC2-0 bits in the SER_CTL serial control stream. The AGC_SET output from the IAFE is normally Low. It goes High when the signal level in the sigma delta A/D is approaching its clipping level, signaling the MDSP to lower the gain.

The VCO is part of a phase-locked loop (PLL) locked to the receive data. The VCO frequency is varied by pulling an external crystal with varactor diodes that are biased by the VPLL output. The VPLL output is, in turn, controlled by the serial port PLL bits.

3.2.2 MDSL Digital Signal Processor (MDSP)

The MDSP incorporates the following digital functions:

- bit-rate transmit and receive signal-processing
- adaptive Echo-Cancelling (EC)
- adaptive decision feedback-equalization (DFE) using the receive quat stream and the internal error signal

- fixed and adaptive digital-filtering functions
- activation/start-up control and the microprocessor interface

The MDSP also provides the digital data interface. A simple, parallel 8-bit microprocessor interface on the MDSP allows high-speed access to control, status and filter coefficient words. Table 6 lists the MDSP pin descriptions. Refer to Test Specifications for MDSP electrical and timing specifications.

The microprocessor interface on the MDSP provides bit flags for signal presence, synchronization, activation completion. Single-byte words representing receive signal level and the noise margin of the transceiver are also available on the microprocessor interface. One control bit allows the user to start the Data Pump activation sequence. The MDSP controls the complete activation/start-up sequence.

Table 4. Minimum and Maximum Data Rate/Frame Time Examples

Line Rate (kbps)	Frame Length (ms) 4702 bit Frame	Frame Length (ms) 4706 bit Frame	Min. Payload Data Rate (kbps)	Nominal Rate (kbps) (50% stuffing)	Max. Payload Data Rate (kbps)
272	17.287	17.301	270.960	271.075	271.190
400	11.755	11.765	398.470	398.640	398.809
528	8.905	8.913	525.980	526.204	526.428
784	5.997	6.003	781.001	781.333	781.666

Table 5. IAFE Transmit Control

TSGN	TMAG	Output Symbol (quat)
1	0	+3
1	1	+1
0	1	-1
0	0	-3

3.2.3 MDSP/IAFE Interface

The IAFE provides the receiver recovered clock, VCO_CK, to the MDSP. The serial control stream framing signal RX_CK is sampled inside the IAFE with the VCO_CK rising edge. The serial control stream, SER_CTL, is sampled inside the IAFE by the rising edge of an internally-generated clock at f(VCO_CK)/2. This IAFE internal clock has the same phase relationship with a similar clock inside the MDSP, as established by the RX_CK signal. In the MDSP, the half-rate clock VCO_CK/2 and RX_CK transition on the rising edge of VCO_CK, and SER_CTL transitions coincide with the falling edge of VCO_CK/2. The output MSTR_CK in Slave Mode is equal to VCO_CK/2.

A/D converter outputs (AD0 and AD1) are clocked out of the IAFE with VCO_CK, having transitions coincident with the rising edge of VCO_CK/2. The MDSP samples AD0 and AD1 with the falling edge of its internal VCO_CK/2.
Transmit data, represented by TSGN and TMAG, is clocked from the MDSP using the falling edge of TX_CK, the transmit clock. The IAFE uses the rising edge of TX_CK to sample TSGN and TMAG. TSGN and TMAG change state at the baud rate, or every 8 cycles of TX_CK. Figure 7 shows relative timing for the MDSP/IAFE interface.

3.2.3.1 MDSP/IAFE Serial Port

The MDSP continually writes to the IAFE serial port. This serial stream consists of two 16-bit words as shown in Table 6. The data flows from the MDSP to the IAFE at a rate of f(VCO_CK)/2. Refer to the Test Specifications section for serial port timing relationships and electrical parameters.

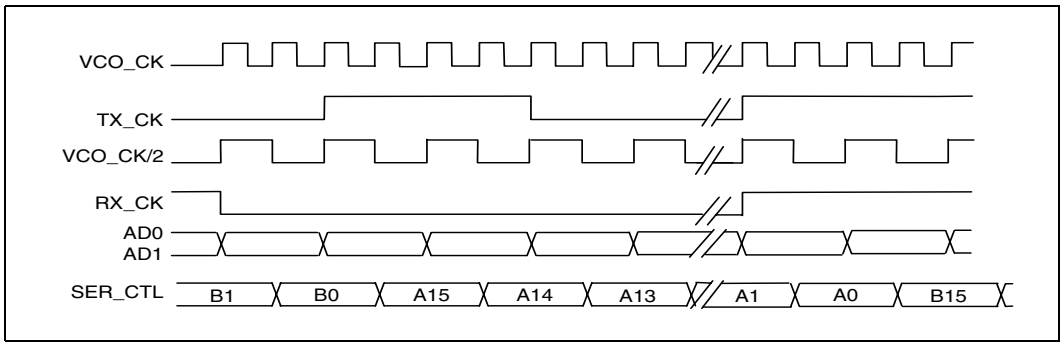
3.3 Line Interface

The Data Pump line interface consists of three differential pairs. The transmit outputs TTIP and TRING, receive inputs RTIP and RRING, and the balance inputs BTIP and BRING, all connect through a common transformer to a single twisted-pair line (Figure 14 and Figure 15). The transmit outputs require resistors in series with the transformer. A passive prefilter is required for the receive inputs. The balance inputs feed the transmit signals back to the Data Pump providing passive echo cancellation. Protection circuitry should be inserted between all Data Pump line interface pins and the transformer. Refer to the Applications section for typical schematics.

Table 6. MDSP/IAFE Serial Port Word Bit Definitions (Figure 7)

Bit	Word A (on SER_CTL)	Word B (on SER_CTL)
15	INIT	COR4
14	n/a	COR3
13	*n/a*	COR2
12	TXOFF	COR1
11	TXDIS	COR0
10	TXTST	VCO2
9	AGC2	VCO1
8	AGC1	VCO0
7	AGC0	PLL7
6	FELB	PLL6
5	*n/a*	PLL5
4	PTR4	PLL4
3	PTR3	PLL3
2	PTR2	PLL2
1	PTR1	PLL1
0	PTR0	PLL0

Figure 7. MDSP/IAFE Interface – Relative Timing



3.4 MDSL Data Interface

This section provides detailed information on the operation of the data interface and how it is configured to support variable data rate and fixed data rate applications.

3.4.1 Clock Distribution

Figure 8 shows an MDSL link between a master and slave transceiver. This figure illustrates the clock/timing architecture of the data pump in both modes. Link activation is initiated by the master mode device which also operates as the MDSL timing source. The slave mode device responds to an activation request and is “loop-timed” (i.e., it recovers the MDSL clock from the master and uses this clock to transmit upstream).

In the master mode, the data pump derives its line transmit clock and data interface BIT_CK by dividing the clock supplied at the MSTR_CK input by 16. MSTR_CK also provides a ±32 ppm accurate local training reference for the receiver clock recovery VCXO before activation. When active, the master data pump uses this VCXO in a PLL for data recovery from the line, but an internal FIFO is provided so that the receive data can be clocked out using the BIT_CK divided down from the MSTR_CK.

In the slave mode after activation, the data pump derives its line transmit clock and data interface BIT_CK from the receiver PLL. In this mode, the clock supplied at the SLAVE_CK input is only used to train the VCXO frequency within ±32 ppm before activation. To minimize switching noise, the SLAVE_CK can be turned off when CK_EN is Low.

To select the clock and crystal frequencies required for a specific application, the required line rate must first be calculated from the specified payload data rate. This process is outlined below for fixed data rate and variable data rate configurations.

3.4.2 Fixed Data Rate Operation

For fixed data rate operation, the line rate is calculated from the payload data rate as follows:

line_rate = data_rate (4702/4688).

The time required to transmit a complete frame is:

frame_time = 4702 / line_rate.

The Master transceiver requires a clock frequency of:

MSTR_CK = 16 (line_rate).

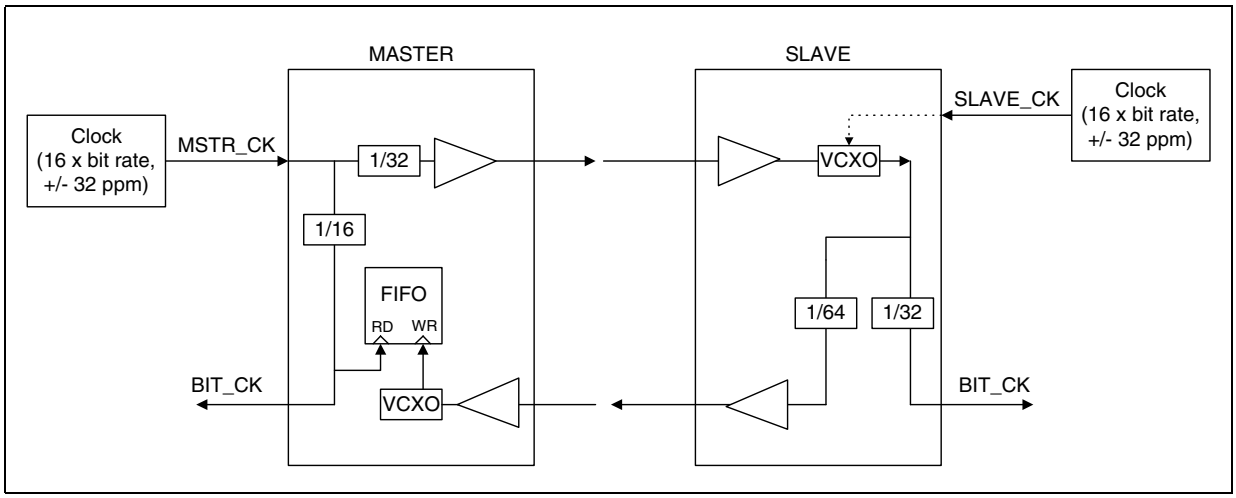
The slave transceiver requires a clock frequency of:

SLAVE_CK = 16 (line_rate).

Both transceivers require a VCXO crystal frequency of:

fxtal = 32 (line_rate).

Figure 8. MDSL Clock Distribution In Master and Slave Modes



3.4.3 Variable Data Rate Operation

For variable data rate operation, the line rate is calculated from the payload data rate as shown below:

line_rate = average_data_rate (4704/4688).

At this line rate the data pump will transport data at the specified average data rate when 50% stuffing is used, however it will always operate at one of the instantaneous data rates given by the following two equations. By adjusting the number of BIT_CK cycles between TFP pulses an external controller may adjust the frame length to control the average data rate between the minimum and maximum instantaneous rates:

max_data_rate = line_rate (4688/4702), and

min_data_rate = line_rate (4688/4706).

The time required to transmit a complete frame is:

frame_time (min) = 4702 / line_rate, or

frame_time (max) = 4706 / line_rate.

The Master transceiver requires a clock frequency of:

MSTR_CK = 16 (line_rate).

The slave transceiver requires a clock frequency of:

SLAVE_CK = 16 (line_rate).

Both transceivers require a VCXO crystal frequency of:

fxtal = 32 (line_rate).

3.4.4 Data Interface Timing

The MDSL data interface provides for the transfer of binary data to and from the transceiver using the 272 to 784 kHz clock, BIT_CK, generated by data pump. Figure 9 shows the timing for the data interface. In the receive direction, the binary data output on RDATA contains the 14-bit frame sync word (b1-b14), the transparent payload data (b15-b4702) and optional stuff bits (b4703-b4706). During the activation process, RDATA is held High until $\overline{\text{ACTIVE}}$ goes Low to indicate link activation has been completed and recovered data is available. The data strobe signal RDATA_ST is High during the frame sync word and stuff bits and Low during payload data. RDATA_ST can be used to create a gapped receive payload data clock by suppressing BIT_CK cycles when RDATA_ST is High. RFP is the receive frame sync output that goes Low during the first bit of every MDSL frame. In variable data rate applications the original data timing can be recovered from RFP using a synthesizer PLL.

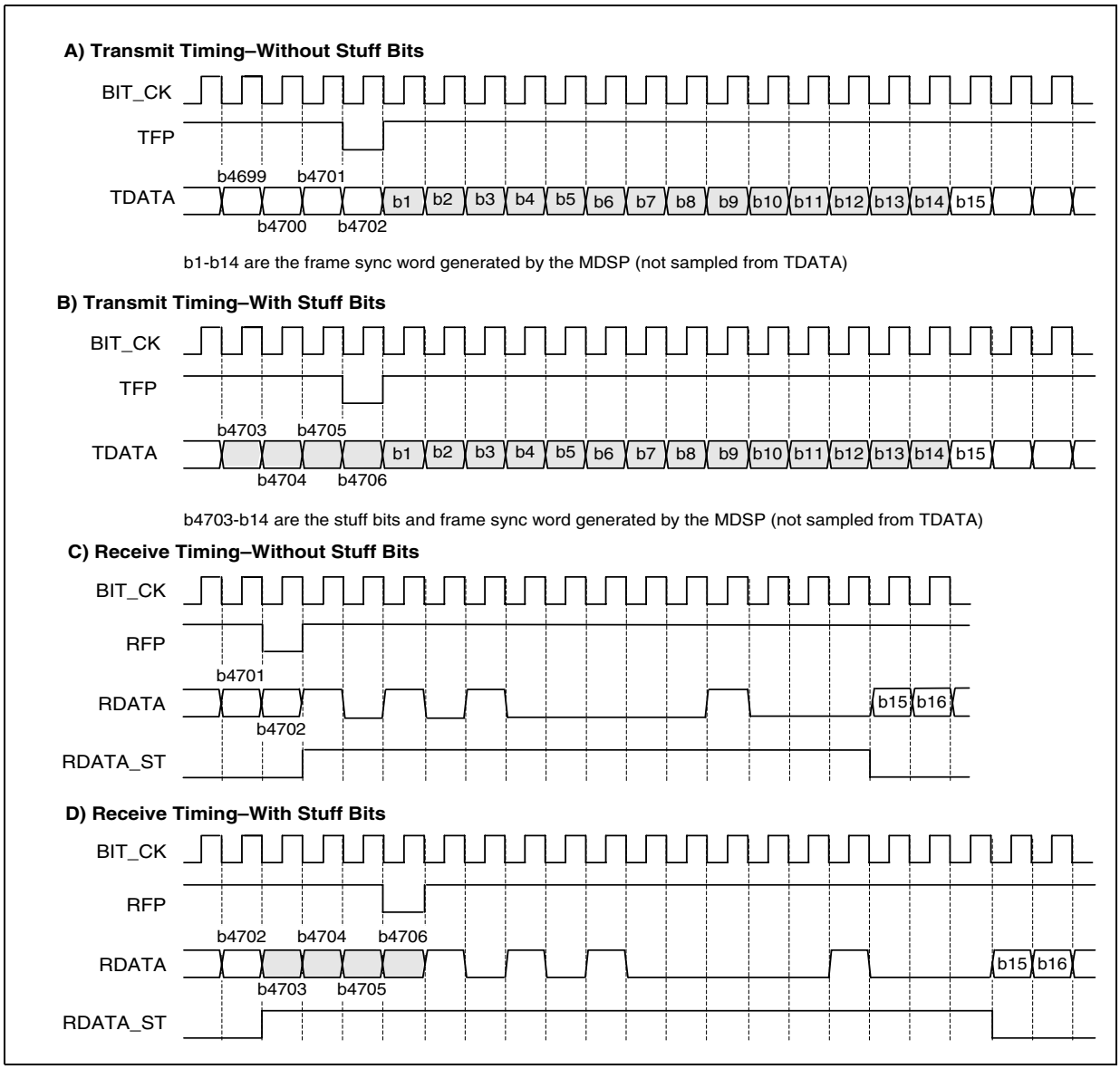
In the transmit direction, payload data is sampled from TDATA during bits b15-b4702 of each frame. Frame sync word bits (b1-b14) are internally generated in the MDSP and not sampled from TDATA, so any data supplied during b1-b14 is ignored. During the activation process, transmit data is internally generated by the MDSP and TDATA is not sampled until $\overline{\text{ACTIVE}}$ goes Low to indicate link activation has been completed. For fixed data rate applications an external counter is used to generate a one BIT_CK cycle long Low pulse for the TFP input. This frame sync pulse establishes the start of an MDSL frame and is needed to establish a gap in the payload data during the time the data pump internally generates the frame sync word. In variable rate applications stuffing control logic adjusts the time between TFP pulses to match the average data rate transmitted by the data pump to the rate at which it is supplied by the external source. In both cases, the TFP signal should be valid prior to an activation request for the Master Data Pump. A valid TFP signal should be generated after power-up, before or immediately after LOS goes Low for the Slave Data Pump. During initialization and anytime thereafter TFP must not be held low for more than 2 BIT_CK cycles or the data interface output signals will be disabled. Also, if the TFP signal is inactive (always High or unconnected) when activation starts, then the Data Pump may activate but will inject stuff bits in the TDATA stream in every other frame and sync bits in every frame. Since the Data Pump will not be synchronized to the data source these internally generated bits will overwrite payload data. If the phase of TFP jumps the Data Pump will immediately reset the transmit frame alignment, typically causing loss of alignment at the other end.

3.4.5 Loopbacks

The data pump provides data loopbacks toward the line and toward the digital interface. Front End Loopback (FELB) is the loopback toward the digital interface inside the IAFE and is available only in Master mode. FELB is initiated by bringing the FELB and ACTREQ signals High in hardware mode, or by setting the FELB and ACTREQ bits to 1 in the processor control mode. In FELB the data pump receiver activates with its own transmit data and ignores a signal at the IAFE receiver analog line interface. Data is transmitted on the line during FELB.

Back End Loopback (BELB) is a data loopback toward the analog line interface inside the MDSP. BELB is available in both Master and Slave modes after activation is complete. BELB is initiated by bringing the BELB signal High in hardware mode, or by setting the BELB bit to 1 in the processor control mode. In BELB the data pump receive data and frame pulse signals are supplied to the transmitter which ignores the TDATA and TFP inputs. Receive Data is output on RDATA during BELB.

Figure 9. MDSP Digital Data Interface Timing



3.5 Microprocessor Interface (MDSP)

Three primary control pins, $\overline{\text{CHIPSEL}}$ (Chip Select), $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$, select the Software Mode which also uses an interrupt output pin to report status changes. Four additional pins are used for the parallel bus addressing and eight pins for data I/O. Refer to Test Specifications for microprocessor interface timing in Software Mode.

3.5.1 Control Pins

Chip Select: The Chip Select ($\overline{\text{CHIPSEL}}$) pin requires an active Low signal to enable Data Pump read or write transfers over the data bus. To enable Hardware Mode hold this pin Low, along with $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$.

Data Read: The Data Read pin ($\overline{\text{READ}}$) requires an active Low pulse to enable a read transfer on the data bus. When $\overline{\text{READ}}$ is pulled Low, the Data Pump data bus lines go from tristate to active and output the data from the register addressed by ADDR0-ADDR3. To avoid reading data during register updates, reads should be synchronized to the falling edge of RX_CK. Alternatively, each read should be repeated until the same data is read twice within one baud time.

Data Write: The Data Write pin ($\overline{\text{WRITE}}$) requires an active Low pulse to enable a write transfer on the data bus. Data transfer is triggered by the rising edge of the $\overline{\text{WRITE}}$ pulse. To ensure data is written to the register addressed by ADDR0-ADDR3, valid data must be present on the MDSP data bus lines before $\overline{\text{WRITE}}$ goes High.

Interrupt: The Interrupt pin ($\overline{\text{INT}}$) is an open drain output requiring an external pull-up resistor. The $\overline{\text{INT}}$ output is pulled active Low when an internal interrupt condition occurs. $\overline{\text{INT}}$ is latched and held until Main Status Register RD0 is read. An internal interruption results from a Low-to-High transition in any of four status indicators: ACTIVE, $\overline{\text{ACTIVE}}$, DEACTVTD or TMR_EXP. Any transition on LOS will also generate an interrupt. If an interrupt mask bit in register WR2 is set, any transition of the corresponding status bit will not trigger the $\overline{\text{INT}}$ output.

3.5.2 Register Definitions

Refer to "Register Definitions" on page 52 for detailed description of the data pump register set.

3.5.3 Register Access

3.5.3.1 Write

To write to an MDSP register, proceed as follows:

1. Drive $\overline{\text{CHIPSEL}}$ Low.
2. Drive an address (0000, 0010, or 0011) onto ADDR0-ADDR3.
3. Observe address setup time.
4. Set 8-bit input data word on D0-D7.
5. Pull $\overline{\text{WRITE}}$ Low, observing minimum pulse width.
6. Pull $\overline{\text{WRITE}}$ High, observing hold time for data and address lines.

3.5.3.2 Read

Procedures for reading the MDSP registers vary according to the particular register. Accessing registers RD0, RD1, RD2, RD5 and RD6 is relatively simple. Reading registers RD3 and RD4 is more complex. Unless parallel port reads are synchronized with the falling edge of RX_CK, all read operations should be repeated until the same data is read twice within one baud time.

To read register RD0, RD1, RD2, RD5 or RD6 proceed as follows:

1. Drive $\overline{\text{CHIPSEL}}$ Low.
2. Drive the desired address onto ADDR0-ADDR3.
3. Pull $\overline{\text{READ}}$ Low, observing minimum pulse width.
4. Pull $\overline{\text{READ}}$ High to complete the read cycle.

Registers RD3 and RD4 hold the coefficient values from the DFE, EC, FFE and AGC as shown in Table 27. Register RD3 holds the lower byte value and register RD4 holds the upper byte value. To reconstruct the complete 16-bit word, concatenate the least significant and most significant bytes.

To read registers RD3 and RD4 proceed as follows:

1. Select the desired coefficient by writing the appropriate code from Table 27 to register WR3.
2. Enable the Coefficient Read Register by writing a 1 to bit b0 (CRD1) in register WR2.
3. Perform standard register read procedure listed in steps 1 through 6 above to read the lower byte from RD3 and the upper byte from RD4.
4. Concatenate the RD3 and RD4 to obtain the complete 16-bit word.

3.6 Activation

The MDSL Data Pump integrates all logic required to manage link activation and deactivation. Figure 10 illustrates the Activation State Machine for the Master mode. Figure 11 illustrates the Slave mode state machine. In software mode, the ST*n* bits in Read Register 6 (ADDR 0110) show the current status of the state machine.

3.6.1 Master Mode Activation Sequence

When the Master Data Pump is powered up and reset is applied, the chip set is in the Inactive State as shown at the top of Figure 10. Starting at the Inactive State, the device progresses in a clockwise direction through the Activating, Active-1, Active-2, Pending Deactivation and Deactivated States. In the hardware mode when the Data Pump is in the Inactive State and the QUIET pin is Low, a Low-to-High transition on the ACTREQ pin initiates activation of the link (Table 7). In the software mode when the Data Pump is in the Inactive State and the QUIET bit is set to 0, setting the ACTREQ bit to 1 initiates activation of the link. Because the ACTREQ control bit is level sensing, to generate a single request, ACTREQ should be set to 1 and then reset to 0 again before the Activation Timer period elapses.

During the Activating State, the echo canceller, equalizers and timing recovery circuits are all adapting during the simultaneous transmission and reception of the framed, scrambled-ones data transmitted first as a two-level code (S0) and then as a four-level code (S1). If the receive frame sync word is not detected in two consecutive frames before the activation timer expires the device moves to the Deactivated State and ceases transmission. After reaching the Deactivated state this way, it will then immediately transition to the Inactive State (setting LOS regardless of whether Slave transmission ended). The next activation request should not be generated for one activation timer period to allow the Slave to time-out, detect LOS and move from the Deactivated to the Inactive State. Microprocessor-based systems may reduce this time by resetting the Slave data pump from the Activating State when no Master signal is present.

Successful detection of the sync word drives the State machine to the Active-1 State. This is indicated by a 0-to-1 transition of the ACTIVE bit or High to Low transition of the $\overline{\text{ACTIVE}}$ pin. If the Master Data Pump remains locked to the sync word until the activation timer expires, the device transitions to the Active-2 (fully active) State. If sync is lost, as indicated by a 0-to-1 transition on the $\overline{\text{ACTIVE}}$ pin, the Master Data Pump transitions to the Pending Deactivation State.

In Pending Deactivation, the Master Data Pump progresses to the Deactivated and Inactive States with the expiration of the respective timers. If the sync word is detected before the Pending Deactivation timer expires, the Master Data Pump returns to either Active-1 or Active-2. (The Master Data Pump returns to which ever state it occupied before transitioning to Pending Deactivation.)

The Master Data Pump will exit the Active-2 State in one of two ways. A Low-to-High transition on the QUIET pin (Hardware Mode) or the QUIET bit (Software Mode), forces the Master Data Pump directly to the Deactivated State. The only other means of exiting the Active State is through a loss of receive sync word. $\overline{\text{ACTIVE}}$ goes Low when six consecutive frames occur without a sync word match sending the Master Data Pump into the Pending Deactivation State.

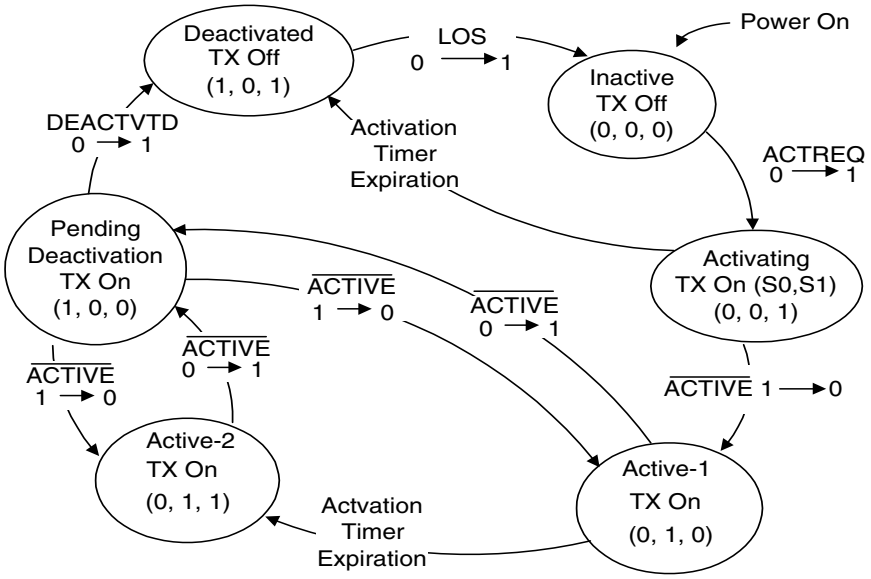
The Master Data Pump remains in the Pending Deactivation State for a maximum of two seconds. If a sync word is detected within the time limit, the Master Data Pump re-enters the Active State. If not, DEACTVTD goes High and the chip set goes to the Deactivated State. When the Deactivated State is reached from Pending Deactivation, the Master Data Pump returns to the Inactive State and declares LOS when it detects no signal from the Slave for one second. The Data Pump waits in the Inactive State before another activation attempt (Table 7).

Table 7. State Machine Timer Durations (Figure 10 and Figure 11)

Timer	Nominal Timer Duration (seconds)				Description
	272 kbps	400 kbps	528 kbps	784 kbps	
Activation Timer[1]	86.5	59.0	44.5	30.0	**Master Mode**: Starts with an activation request. Restarts when a signal is detected from the Slave. **Slave Mode**: Starts when a signal is detected from the Master.
Deactivation Timer[2,3]	6.0	4.0	3.0	2.0	Starts due to Loss of Sync Word for 6 consecutive frames, triggering the Pending Deactivation state.
LOS Timer[4]	3.0	2.0	1.5	1.0	**Master Mode**: Starts in Deactivated state once the Slave is quiet. **Slave Mode**: not used.
Delay required before next activation request	86.5	59.0	44.5	30.0	The amount of time the Master must be in the Inactive state before another activation request can be made after the Data Pump deactivates directly from the Activating State.

1. If time elapses and data pump has not moved to Active-1 state, the data pump enters the Deactivated State.
2. Pending Deactivation can be reached from either Active-1 or Active-2 states, if loss of sync word occurs for 6 frames.
3. If sync word detection does not occur before time elapses, the data pump deactivates.
4. When the data pump fails to activate in the Activating state, there is no waiting period in the Deactivated state; the data pump immediately goes Inactive.

Figure 10. Master Mode Activation State Machine



NOTE: (n, n, n) indicates the status of bits ST2, ST1 and ST0 respectively.

3.6.2 Slave Mode Activation Sequence

Figure 11 and Figure 12 represent the Slave Data Pump Activation State Machine and the Slave MDSL Framer State Machine. The activation state machines for Slave and Master devices are similar. Both Data Pump machines start at the Inactive State and progress clockwise through the Activating, Active-1, Active-2, Pending Deactivation, and Deactivated States. One difference between them is in the initial condition required to exit from the Inactive State. The Master Data Pump responds to the Activation Request (ACTREQ) signal. The Slave device responds only to the presence of signal energy on the link. Thus, only an active Master device can bring up the link. Once the Master begins transmitting, the Slave device will automatically activate and attempt synchronization.

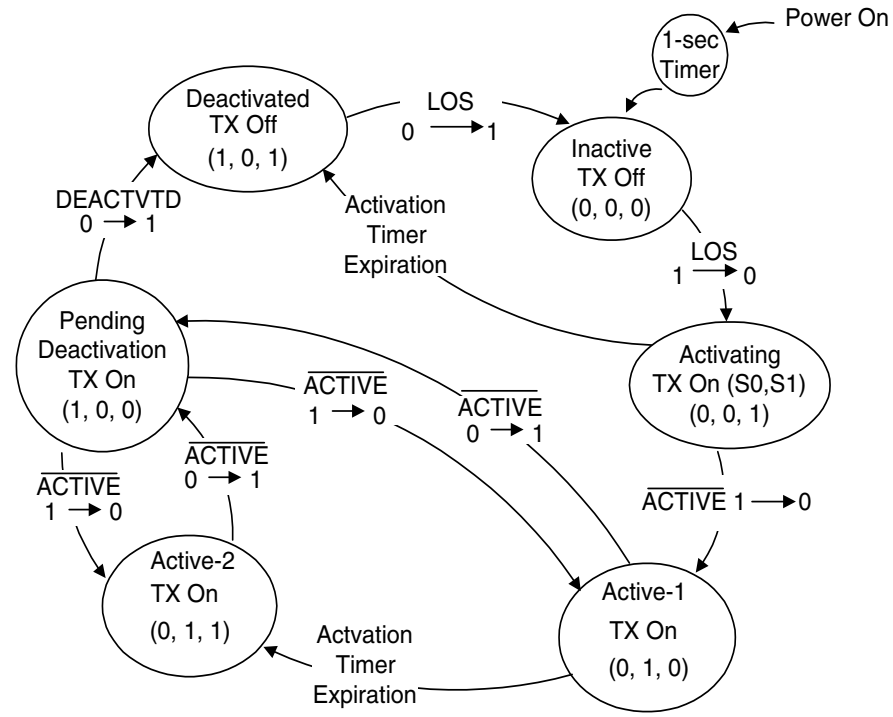
The other difference between the Data Pump state machines is the impetus for the change from the Deactivated to the Inactive State. In the Master Data Pump, expiration of a one-second loss of signal timer (after far end signal energy ceases) will cause the transition. In the Slave the transition occurs immediately on Loss of Signal (LOS).

Table 8. Data Pump Activation States

ST2	ST1	ST0	Data Pump State
0	0	0	Inactive
0	0	1	Activating – Activation timer running
0	1	0	Active – Activation timer running (Active-1)[1]
0	1	1	Active – Activation timer expired (Active-2)[1]
1	0	0	Pending Deactivation[1]
1	0	1	Deactivated
1	1	0	*unused*
1	1	1	*unused*

1. The data pump samples the TDATA input for all transmit data except the 14 sync bits at the start of each frame during states 010, 011 and 100.

Figure 11. Slave Mode Activation State Machine



NOTE: (n, n, n) indicates the status of bits ST2, ST1 and ST0 respectively.

3.6.3 Synchronization State Machine

Figure 12 shows the MDSL Synchronization State Machine incorporated in the MDSP. It applies to both Master and Slave devices. Table 9 lists the correspondence between the Synchronization states and Activation states. The Sync state machine is clocked by the receive signal framing. Starting at the initial Out-of-Sync condition (State 0), the device progresses in a clockwise direction through State 1 until Sync is declared in State 2. Two consecutive frame sync word matches are required to achieve synchronization.

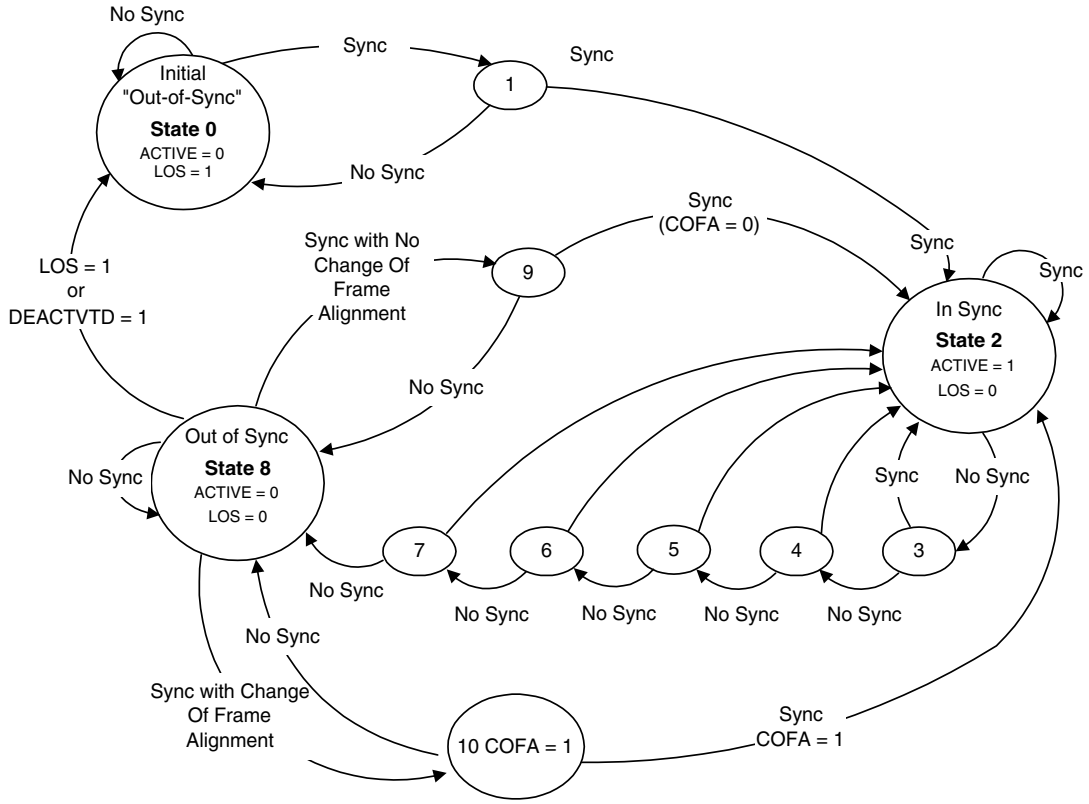
Once the In-Sync condition is declared, six consecutive frame sync mismatches will cause the device to transition through States 3 through 7 and declare an Out-of-Sync condition in State 8. From State 8, the device will return either to State 2 or to State 0. If the Pending Deactivation timer expires without re-establishing frame sync or if the receive signal energy is no longer detected, the device returns directly to State 0.

If frame sync is re-established, the device will return to the In-Sync condition (State 2) through State 9 if two consecutive frames are received without any change of frame alignment (COFA = 0). If a change of frame alignment does occur (COFA = 1), two consecutive matches are required to transition through State 10 back to State 2.

Table 9. Activation and Synchronization States

Activation State	Synchronization States
Inactive	State 0
Activating	State 1
Active	States 2, 3, 4, 5, 6, and 7
Pending Deactivation	States 8, 9, and 10

Figure 12. MDSL Synchronization State Machine



NOTES:
1. “Sync” = Frame Sync Word Match. “No Sync” = Frame Sync Word Mismatch.
2. A 0-to-1 transition on QUIET will set the Sync State Machine from any State to State 0.
3. Expiration of the Activation Timer will set the Sync State Machine from State 1 to State 0.

4.0 Application Information

4.1 PCB Layout

Refer to Figure 13, Figure 14 and Figure 15, and Table 10. The following are general considerations for PCB layout using the MDSL Data Pump chip set:

1. Use a four-layer or more PCB layout, with embedded power and ground planes
2. Bring the digital power and ground planes down to include pins 1-6 and 24-28 of the IAFE
3. Break up the power and ground planes into the following regions. Tie these regions together at the common point where power connects to the circuit:
   — Digital Region
   — Analog Region
   — VCXO subregion
   — IAFE, Line I/F, and IBIAS subregion
4. Use larger feedthroughs (“vias”) and tracks for connecting the power and ground planes to the power and ground pins of the ICs than for signal connection
5. Place the decoupling capacitors right at the feed-through power/ground plane ties or on the tracks to the IC power/ground pins as close to the pins as possible
6. On the User Interface Connector, route digital signals to avoid proximity to the TIP, RING, and CT lines
7. Provide at least 100 µF or more of bulk power supply decoupling at the point where power is connected to the Data Pump circuit

4.1.1 Digital Section

The following are considerations for PCB layout of digital signals:

1. Keep all digital traces separated from the analog region of the Data Pump layout
2. Provide high frequency decoupling capacitors (0.01 µF ceramic or monolithic) around the MDSP as shown in Figure 14 and Figure 15.
3. The capacitor on the MDSP VCC1 pin (pin 1) should be on the IC side of the diode
4. It is possible to replace the NAND gate (shown in Figure 14) with an AND gate

4.1.2 Analog Section

The analog section of the PCB consists of the following subsections:

- IAFE and power supply decoupling capacitors.
- Bias Current Generator.
- Voltage Controlled Crystal Oscillator.
- Line Interface Circuit.

The following are considerations for PCB layout of analog signals:

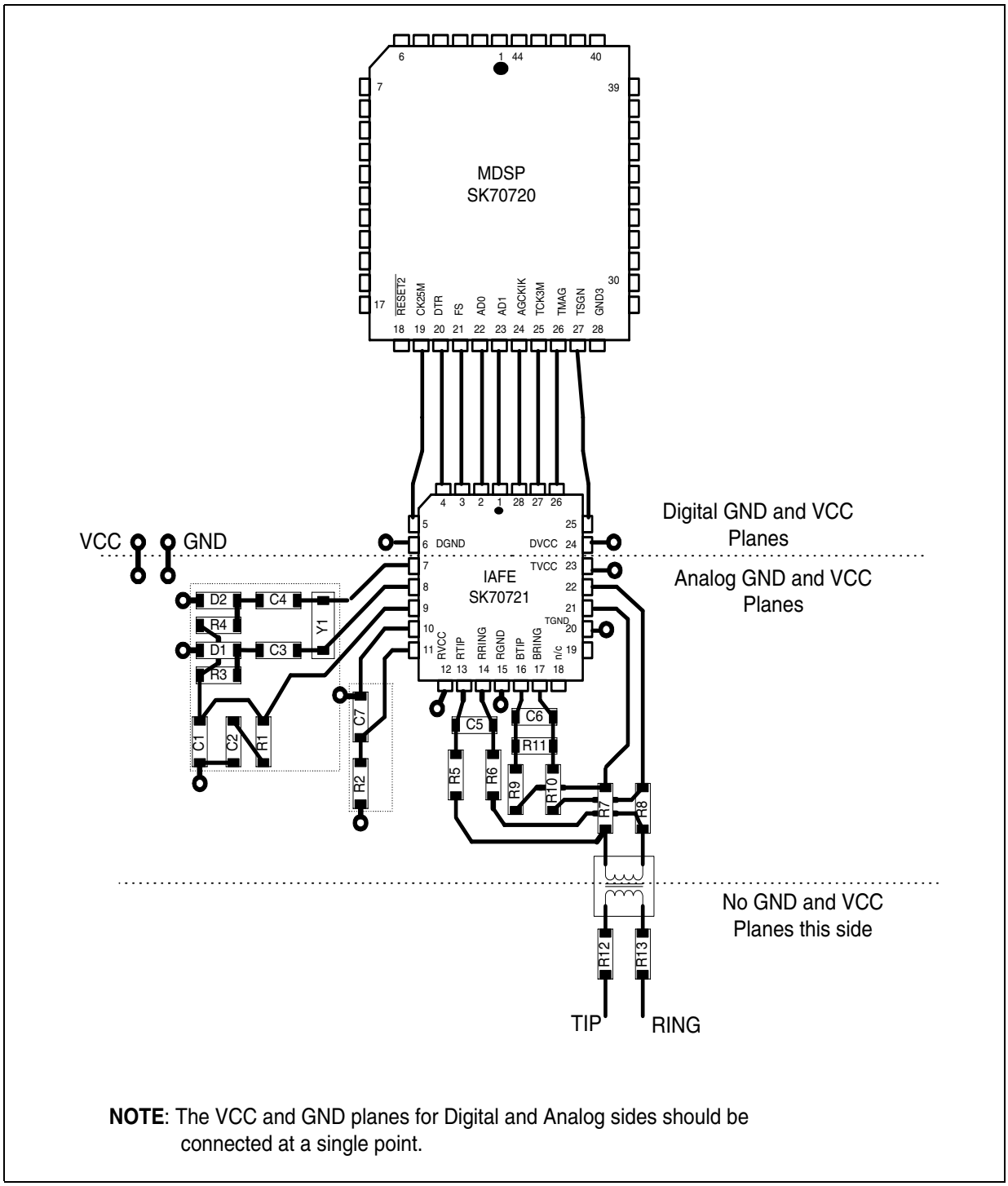
1. Route digital signals AD0, AD1, RX_CK, SER_CTL, TSGN, TMAG, TX_CK, and AGC_SET on the solder side of the PCB
2. route all analog signals on the component side as much as possible
3. Route the following signal pairs as adjacent traces, but keep the pairs separated from each other as much as possible:

   TTIP/TRING

   BTIP/BRING

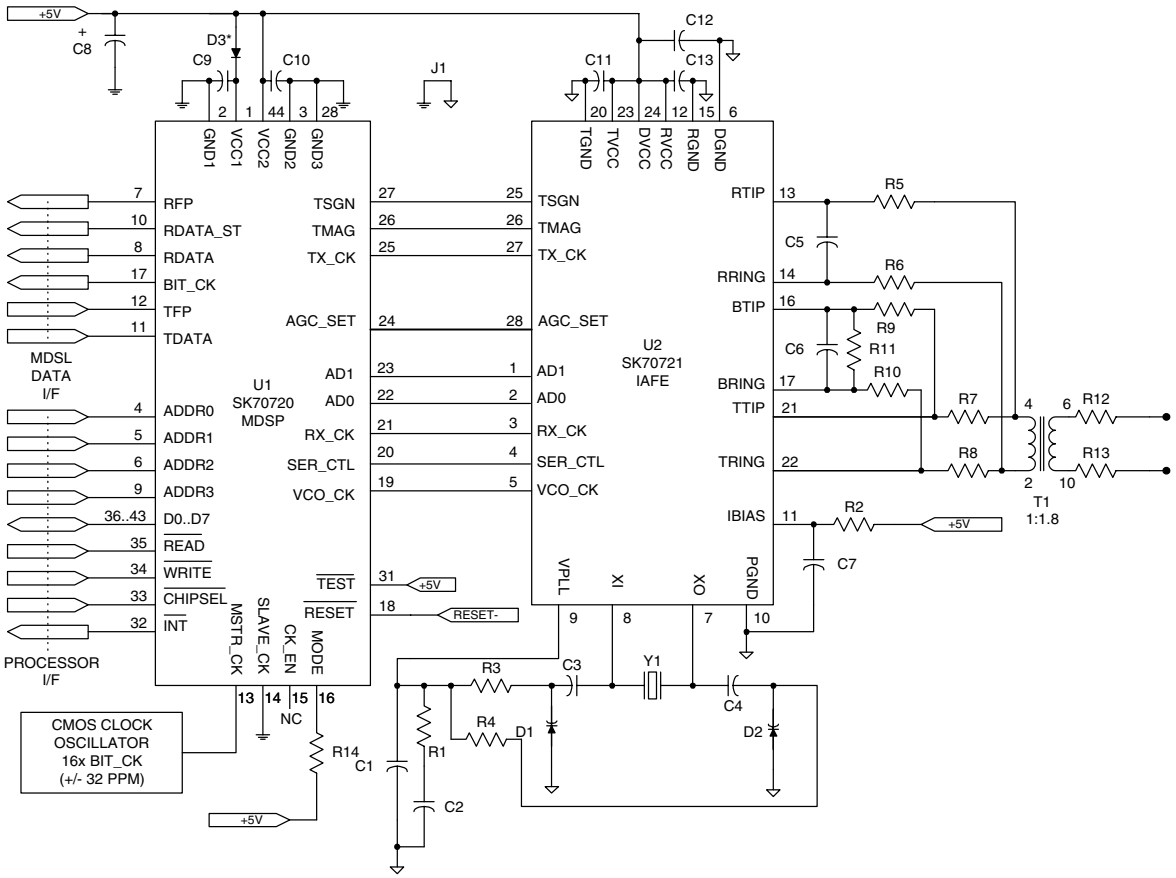
   RTIP/RRING
4. Do not run the analog ground plane under the transformer line side to maximize high voltage isolation
5. The IAFE should be placed such that pin 1 is near pin 23 of the MDSP
6. pins 12-18 are near the edge of the PCB, with the line transformer and connector

Figure 13. PCB Layout Guidelines



NOTE: The VCC and GND planes for Digital and Analog sides should be connected at a single point.

Figure 14. Typical Application for Master Mode Operation (Microprocessor Interface Mode)



NOTES:
1. Diode D3 is optional.
2. The MDSP and IAFE should have independent ground planes connected at a single point near pin 5 of the IAFE.
3. Refer to AN76 or SK70725/SK70721 Data Sheet for improved line interface circuit.

Table 10. Components for Suggested Circuitry (Figure 14 and Figure 15)

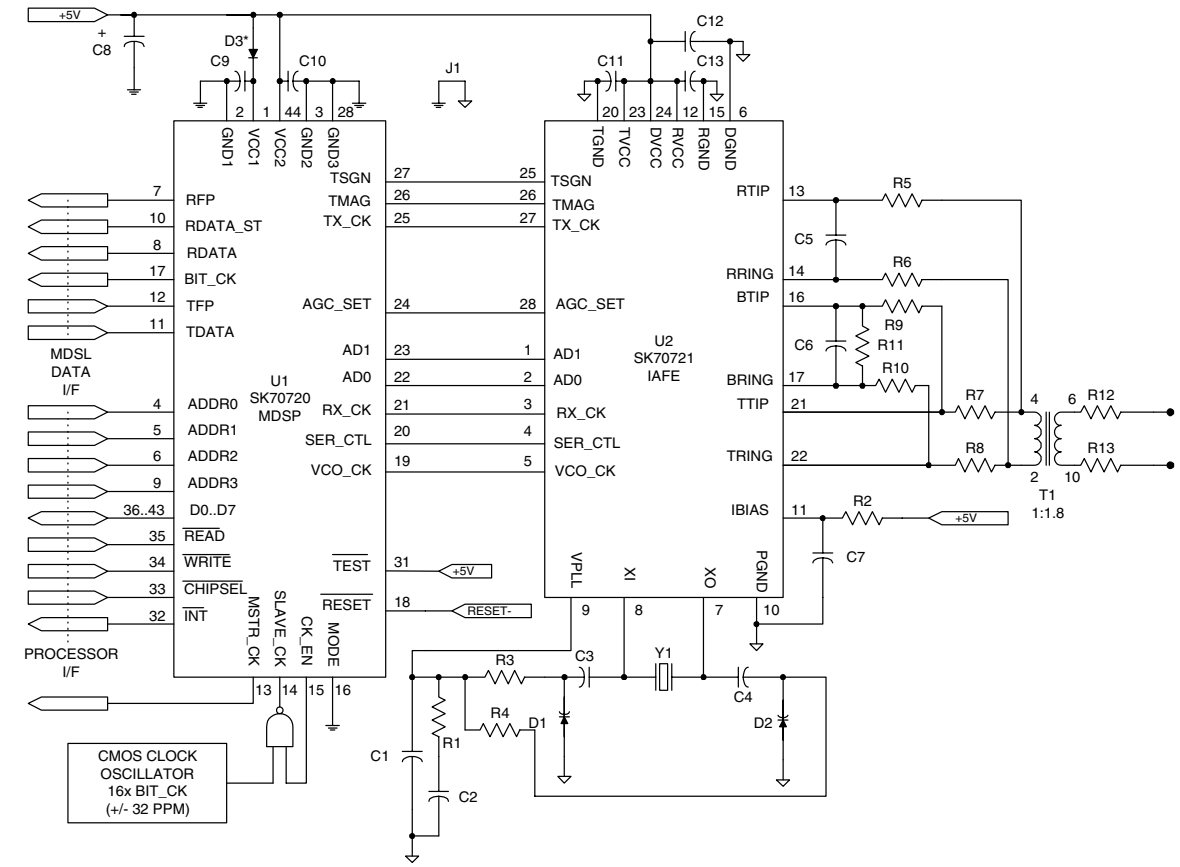
Ref	Description	Ref	Description	Ref	Description
C1, 9, 10	0.01 µF, ceramic, 10%	R1	5.11 kΩ, 1%	R12, 13	5.6 Ω, line feed fuse resistor (ALFR-2-5.6-1 IRC)
C2	100 µF, electrolytic, 20% low leakage ≤5 µA @ 25° C	R2	35.7 kΩ, 1%		
		R3, 4	20.0 kΩ, 1%	D1, 2	Varicap diode (Motorola MV209)
C3, 4	1000 pF, ceramic, 20%	R5, 6	499 Ω, 1%	D3	Silicon rectifier diode (1N4001)
1. R7, R8 should be 20 Ω, when R12 and R13 (the 5.6 Ω fuse links) are not used.					

Table 10. Components for Suggested Circuitry (Figure 14 and Figure 15) (Continued)

Ref	Description	Ref	Description	Ref	Description
C5, 6	470 pF, COG or mica, 10%	R7, 8[1]	18.2 Ω, 1%	Y1	Pullable Crystal 784 kbps: 25.088 MHz (pn:80546/1) 528 kbps: 16.896 MHz (pn:81522/1) 400 kbps: 12.800 MHz (pn:80546/5) 272 kbps: 8.704 MHz (pn:81523/1) (Hy-Q International)
C7, 11-13	0.1 µF, ceramic, 10%	R9, 10	806 Ω, 1%		
C8	100 µF, electrolytic, 20%	R11	2.49 kΩ, 1%	T1	1:1.8 Transformer ≥ 400 kbps: Midcom 671-7376 or Pulse Engineering PE-68614 < 400 kbps: Midcom 50109

1. R7, R8 should be 20 Ω, when R12 and R13 (the 5.6 Ω fuse links) are not used.

Figure 15. Typical Application for Slave Mode Operation



NOTES:
1. Diode D3 is optional.
2. The MDSP and IAFE should have independent ground planes connected at a single point near pin 5 of the IAFE.
3. Refer to AN76 or SK70725/SK70721 Data Sheet for improved line interface circuit.

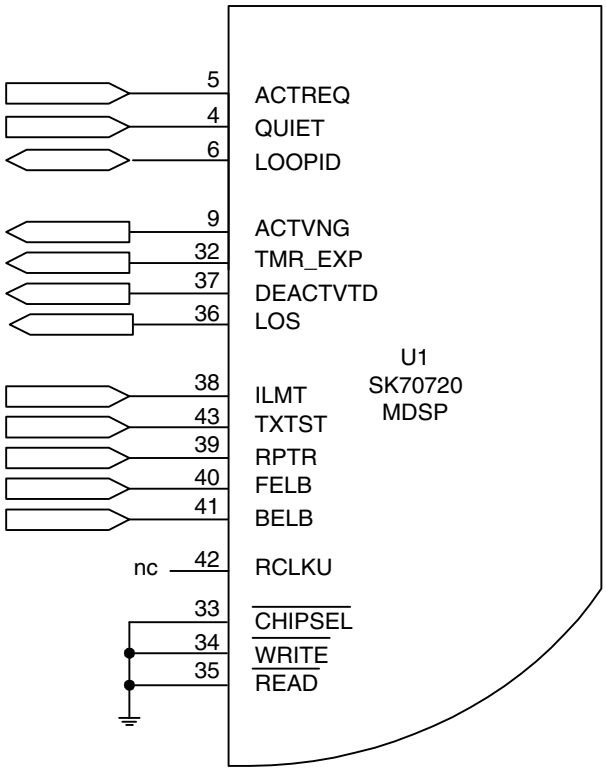
Table 11. Transformer Specifications
(Figure 14 and Figure 15, Reference T1)

Measure	Value	Tolerance
Turns Ratio (IC:Line)	1:1.8	±1%
Line Side Inductance ≥ 400 kbps < 400 kbps	 2.8 mH 11.7 mH	±10%
Leakage Inductance	≤ 50 µH	-
Interwinding Capacitance	≤ 70 pF	-
THD	≤ -70 dB	-
Longitudinal Balance	≥ 50 dB	5-196 kHz
Return Loss	≥ 20 dB	40-200 kHz
Isolation	1500 VRMS	-
Primary DC Resistance	≤ 3.2 Ω	-
Secondary DC Resistance	≤ 6.0 Ω	-
Operating Temperature	-40 to +85° C	-

Table 12. Crystal Specifications
(Figure 14 and Figure 15, Reference Y1)

Measure	Value	Offset
Frequency @C_L = 20 pF	8.704 to 25.088 MHz	-0, +40 ppm
Mode	Fundamental, Parallel Resonance	
Pullability (C_L = 24 pF ⇨ 16 pF)	≥ +160 ppm	-
Operating Temperature	-40 to +85 ° C	-
Temperature Drift	≤ ±30 ppm	-
Aging Drift	≤ 5 ppm/year	-
Series Resistance	≤ 15 Ω	-
Drive Level	0.5 mW	-

Figure 16. MDSP Control and Status Signals (Stand-alone Mode)



NOTE: This figure illustrates the MDSP control and status signals in stand-alone mode. All other MDSP and IAFE signals are connected as shown in Figure 14 and Figure 15.

5.0 Test Specifications

Note: The minimum and maximum values in Table 13 through Table 23 and Figure 17 through Figure 24 represent the performance specifications of the Data Pump and are guaranteed by test, except where noted by design.

Table 13. IAFE Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage[1] (reference to ground[2])	TVCC, RVCC, DVCC	-0.3	+6.0	V
Input voltage[2, 3], any input pin	TVCC, RVCC, DVCC	- 0.3V	VCC + 0.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	TSTOR	-65	+150	° C

Caution: Operations at the limits shown may result in permanent damage to the Integrated Analog Front End. Normal operation at these limits is neither implied nor guaranteed.

1. No supply input may have a maximum potential of more than ±0.3 V from any other supply input.
2. TGND = 0V; RGND = 0V; DGND = 0V.
3. TVCC = RVCC = DVCC = VCC.

Table 14. IAFE Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
DC supply	TVCC, DVCC, RVCC	4.75	5.0	5.25	V
Ambient operating temperature	TA	-40	+25	+85	° C

Table 15. IAFE DC Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current (full operation)	ICC	–	80	120	mA	83 Ω resistor across TTIP and TRING
Input low voltage	VIL	–	–	0.5	V	
Input high voltage	VIH	4.5	–	–	V	
Output low voltage[2]	VOL	–	–	0.2	V	IOL < 1.6 mA
Output high voltage[3]	VOH	4.5	–	–	V	IOH < 40 µA
Input leakage current[4]	IIL	–	–	±50	µA	0 < VIN < VCC
Input capacitance (individual pins)	CIN	–	12	–	pF	
Load capacitance (MSTR_CK output)	CLREF	–	–	20	pF	

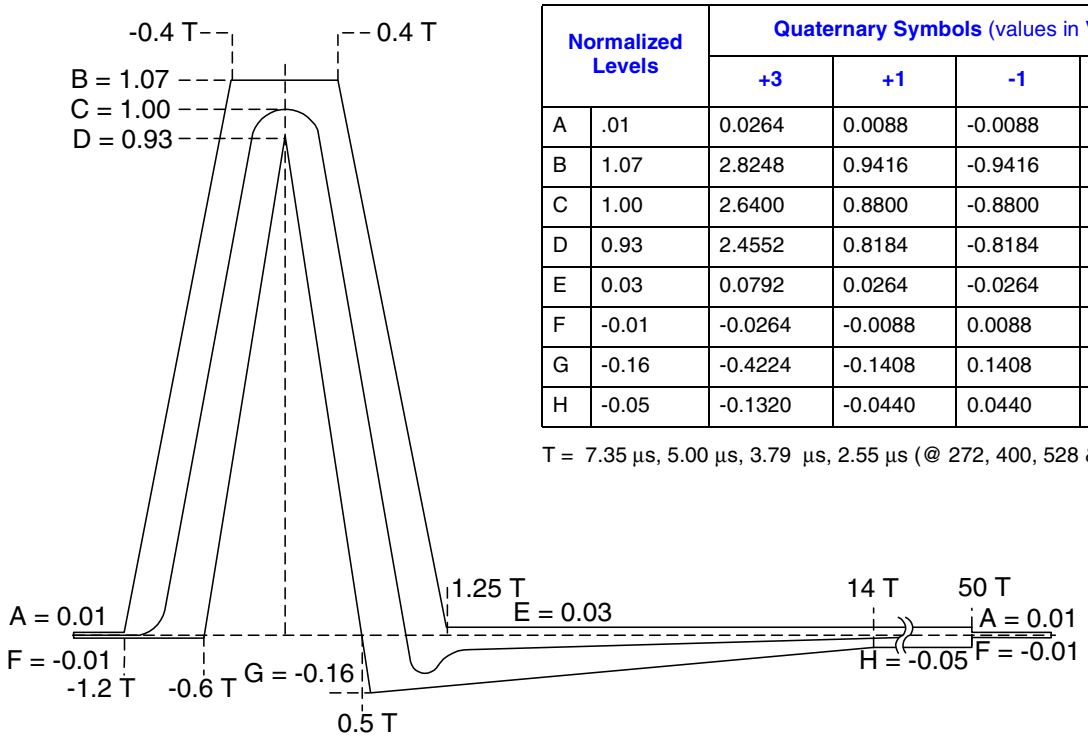
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. IOL is sinking current.
3. IOH is sourcing current.
4. Applies to pins 3, 4, 25, 26 and 27.

Table 16. IAFE Transmitter Electrical Parameters (Over Recommended Range)

Parameters	Sym	Min	Typ	Max	Unit	Test Conditions
Isolated pulse height at TTIP, TRING	–	+2.455	+2.640	+2.825	Vp	TDATA High, TFP Low (+3)
	–	-2.825	-2.640	-2.455	Vp	TDATA Low, TFP Low (-3)
	–	+0.818	+0.880	+0.941	Vp	TDATA High, TFP High (+1)
	–	-0.941	-0.880	-0.818	Vp	TDATA Low, TFP High (-1)
Setup time (TSGN, TMAG)	t_{TSMSU}	5	–	–	ns	
Hold time (TSGN, TMAG)	t_{TSMH}	12	–	–	ns	

1. Pulse amplitude measured across a 135 Ω resistor on the line side of the transformer using the application circuit shown in Figure 14 and Table 11.

Figure 17. IAFE Normalized Pulse Amplitude Transmit Template



Normalized Levels		Quaternary Symbols (values in Volts)			
		+3	+1	-1	-3
A	.01	0.0264	0.0088	-0.0088	-0.0264
B	1.07	2.8248	0.9416	-0.9416	-2.8248
C	1.00	2.6400	0.8800	-0.8800	-2.6400
D	0.93	2.4552	0.8184	-0.8184	-2.4552
E	0.03	0.0792	0.0264	-0.0264	-0.0792
F	-0.01	-0.0264	-0.0088	0.0088	0.0264
G	-0.16	-0.4224	-0.1408	0.1408	0.4224
H	-0.05	-0.1320	-0.0440	0.0440	0.1320

T = 7.35 µs, 5.00 µs, 3.79 µs, 2.55 µs (@ 272, 400, 528 & 784 kbps)

NOTE: Pulse amplitude measured across a 135 Ω resistor on the line side of the transformer using the application circuit shown in Figure 14 and Table 11.

Figure 18. Transmit Power Spectral Density—Upper Bound

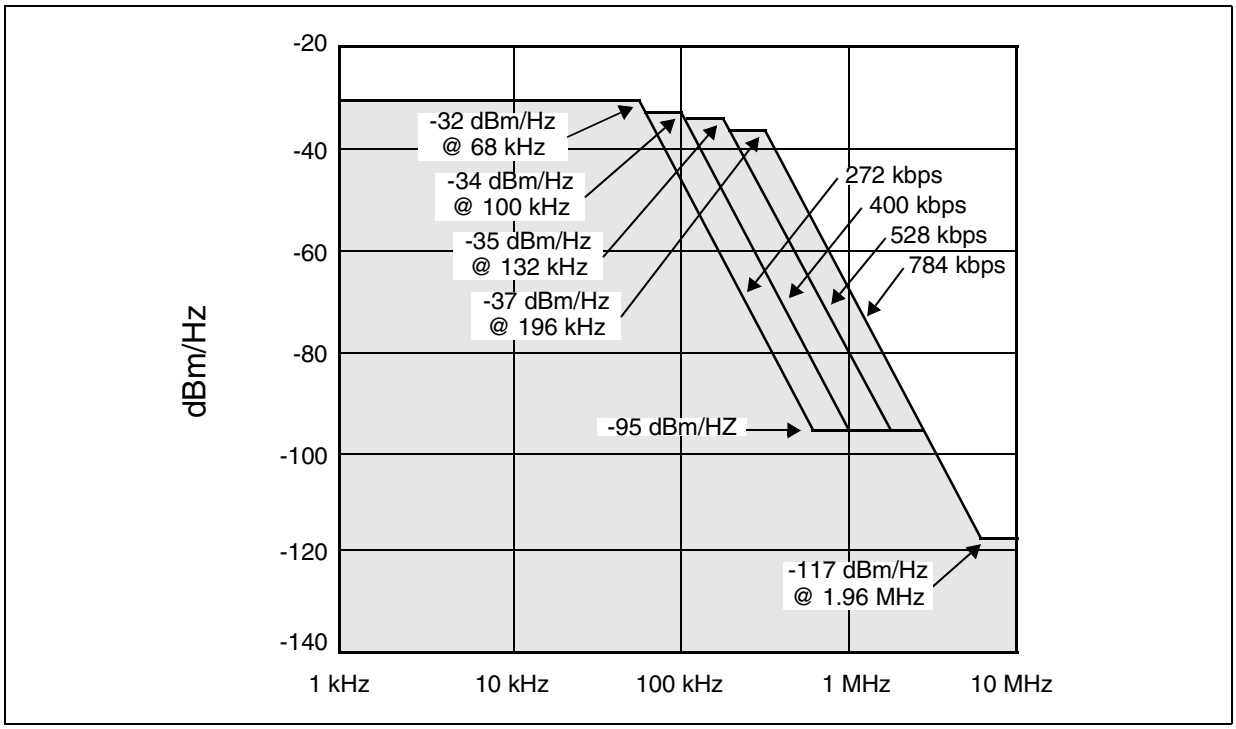


Table 17. IAFE Receiver Electrical Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Propagation delay (AD0, AD1)	tADD	–	–	25	ns	
Total harmonic distortion	–	–	-80	–	dB	V(RTIP, RRING) = 3 Vpp @ 50 kHz
RTIP, RRING, to BTIP, BRING gain ratio	–	–	1.0	1.01	V/V	

Figure 19. IAFE Receiver Syntax and Timing

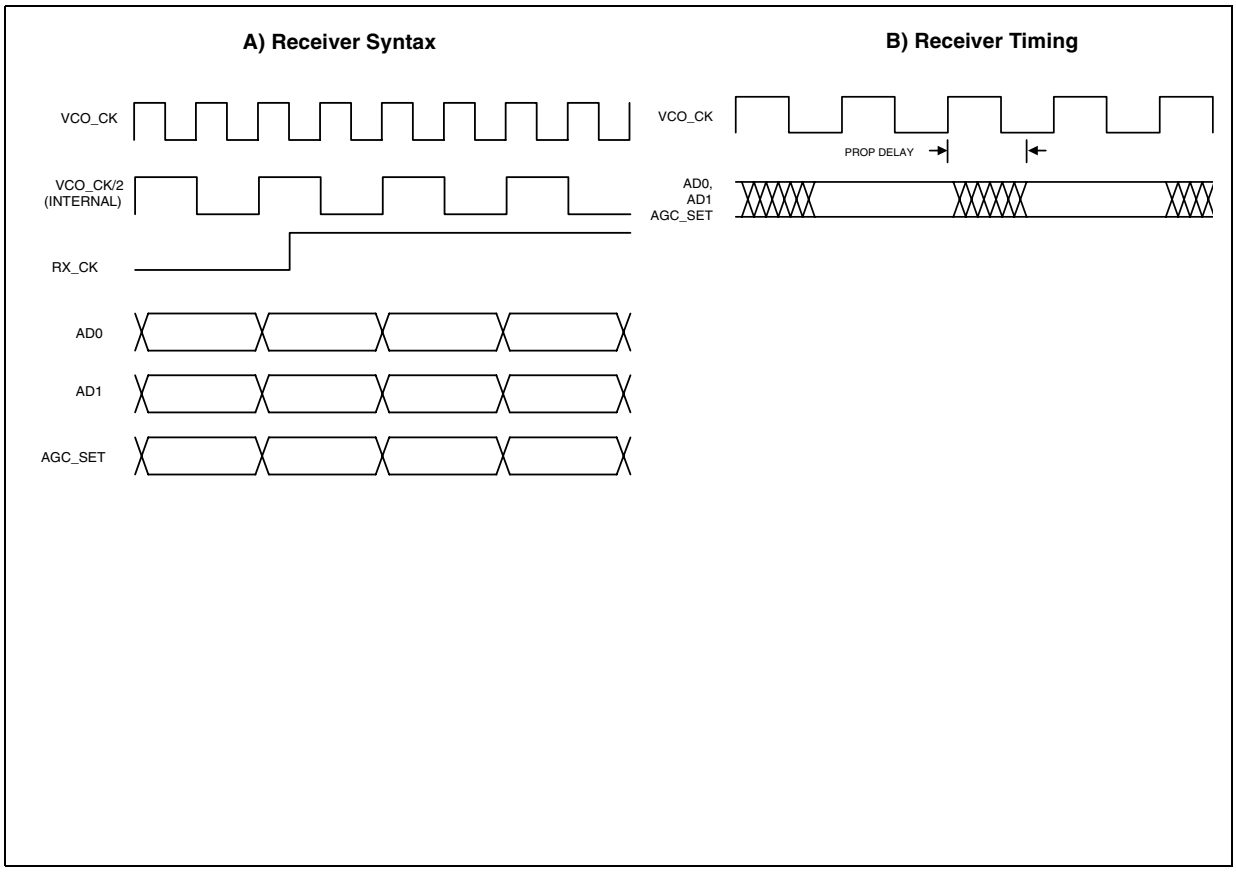
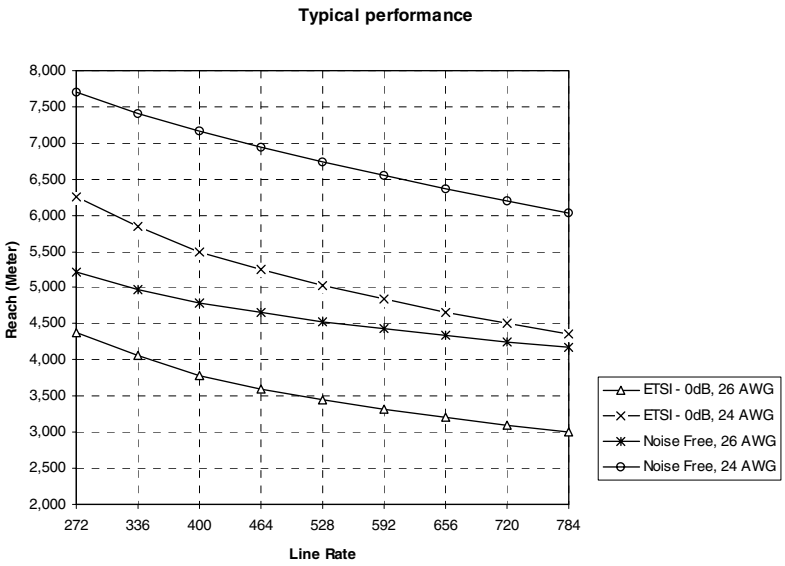
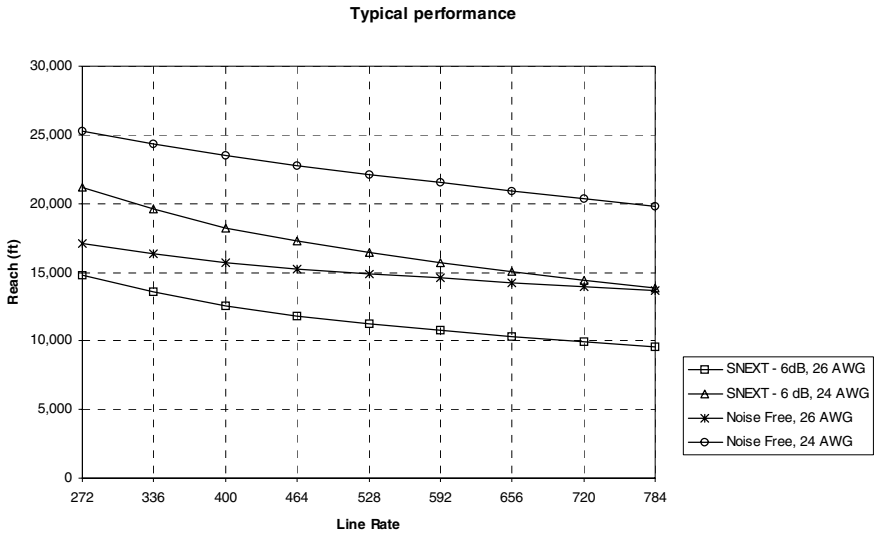


Figure 20. Typical Performance vs. Line Rate and Cable Gauge (Metric)



NOTES:
1. Noise-free range is specified with a Bit Error Rate (BER) less than or equal to 1.0×10^{-7}.
2. The range with ETSI shaped noise corresponds to a 0 dB margin with a BER less than or equal to 1.0×10^{-7}. The power spectral density for ETSI standard noise is defined in ETSI ETR-152 section 6.3.3.1.
3. Refer to AN76 or SK70725/SK70721 Data Sheet for improved line interface circuit.

Figure 21. Typical Performance vs. Line Rate and Cable Gauge (English)



NOTES:
1. Noise-free range is specified with a Bit Error Rate (BER) less than or equal to 1.0×10^{-7}.
2. There are no generally accepted noise models for MDSL systems. Performance simulations using ANSI Near End Cross Talk (NEXT) noise models indicate worst case performance degradation should be less than 2 kft (0.6 km) from the noise-free performance.
3. Refer to AN76 or SK70725/SK70721 Data Sheet for improved line interface circuit.

Table 18. MDSP Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage[1] (reference to ground[2])	VCC2, VCC1	-0.3	+6.0	V
Input voltage[2], any input pin	–	- 0.3	VCC2 + 0.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	TSTOR	-65	+150	° C

Table 19. MDSP Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
DC supply[1]		VCC1[2]	3.95	5.0	5.25	V
		VCC2	4.75	5.0	5.25	V
		VCC2-VCC1	-0.25	–	+0.9	V
Ambient operating temperature	SK70720PE	TA	-40		+85	° C

1. To derive this supply, a 1N4001 (or equivalent) diode may be connected between VCC2 and VCC1 as shown in Figure 14 and Figure 15.
2. If a diode is used, it should be selected to meet VCC1 minimum specifications.

Table 20. MDSP DC Electrical Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current	272 kbps 400 kbps 528 kbps 784 kbps	ICC	– – – –	35 48 62 100	45 60 80 135	mA	
Input low voltage		VIL	–	–	0.5	V	
Input high voltage		VIH	4.0	–	–	V	
Output low voltage[2]		VOL	–	–	GND +0.3	V	IOL < 1.6 mA
Output high voltage[3]		VOH	VCC2 - 0.5	–	–	V	I_{OH} < 40 µA
Input leakage current[4]		IIL	–	–	±50	µA	0 < V_{IN} < V_{CC_2}
Tristate leakage current[5]		ITOL	–	–	±30	µA	0 < V < V_{CC_2}
Input capacitance (individual pins)		CIN	–	12	–	pF	
Load capacitance (MSTR_CK output)		CLREF	–	–	15	pF	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. IOL is sinking current.
3. IOH is sourcing current.
4. Applies to pins 4, 5, 11, 12, 14, 16, 18, 19, 22, 23, 24, 29, 31, 33, 34 and 35. Applies to pins 5, 6, 9, 13, and 36-43, when configured as inputs.
5. Applies to pins 7, 8, 10, 15, 17, 30, 32 and 36-43, when tristated.

Table 21. MDSL Data Interface Timing Specifications (Figure 22)

Parameter	Symbol	Min	Typ[1]	Max	Unit
BIT_CK frequency	fBIT_CK	272	–	784	kHz
MSTR_CK frequency	fREFCK	4.352	–	12.544	MHz
MSTR_CK frequency tolerance (Master Mode)	tolRCK	-32	0	+32	ppm
SLAVE_CK frequency tolerance (Slave Mode)[2]	tolSLAVE_CK	-32	0	+32	ppm
BIT_CK pulse width high 272 kbps 400 kbps 528 kbps 784 kbps	tIPW	– – – –	1.840 1.250 0.950 0.638	– – – –	µσ
Transition time on any digital output[3]	tTO	–	5	10	ns
Transition time on any digital input	tTI	–	–	25	ns
TDATA, TFP setup time to BIT_CK rising edge	tTSU	100	–	–	ns
TDATA, TFP hold time from BIT_CK rising edge	tTH	100	–	–	ns
RDATA, RFP, RDATA_ST delay from BIT_CK falling edge	tTD	0	–	150	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. SLAVE_CK must meet this tolerance about a frequency of 16 times the BIT_CK frequency in slave mode.
3. Measured with 15 pF load.
4. These parameters apply only to the master mode data pump programmed for repeater applications as shown in Figure 22.
5. The values are for minimum line rate 272 Kbps.
6. The values are for minimum line rate 784 Kbps.

Table 21. MDSL Data Interface Timing Specifications (Figure 22) (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Unit
TFP pulse width[4]	tTFPW	3677[5]	–	1276[6]	ns
TFP falling edge to BIT_CK rising edge[4]	tTFIR	1838[5]	–	638[6]	ns
TFP set-up time to MSTR_CK rising edge	tTSUR	25	–	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. SLAVE_CK must meet this tolerance about a frequency of 16 times the BIT_CK frequency in slave mode.
3. Measured with 15 pF load.
4. These parameters apply only to the master mode data pump programmed for repeater applications as shown in Figure 22.
5. The values are for minimum line rate 272 Kbps.
6. The values are for minimum line rate 784 Kbps.

Figure 22. MDSL Data Interface Timing

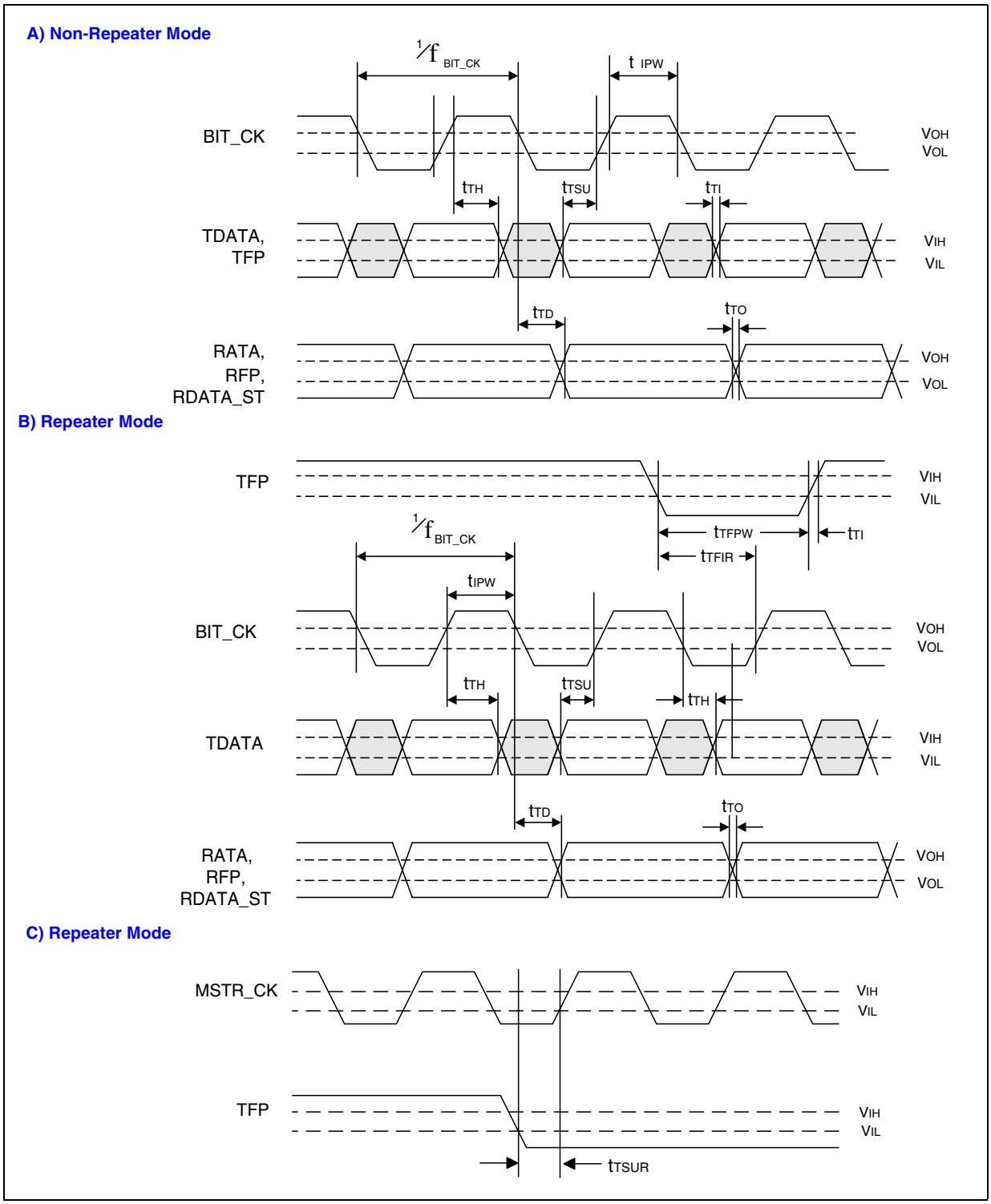


Table 22. MDSP/Microprocessor Interface Timing Specifications (Figure 19 & Figure 20)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ pulse width Low	tRPWL	0.1	–	5	s
$\overline{\text{RESET}}$ to $\overline{\text{INT}}$ clear (10 kΩ resistor from $\overline{\text{INT}}$ to VCC2)	tINTH	–	–	300	ns
$\overline{\text{RESET}}$ to data tristate on D0-7	tDTHZ	–	–	100	ns
$\overline{\text{CHIPSEL}}$ pulse width Low	tCSPWL	200	–	–	ns
$\overline{\text{CHIPSEL}}$ Low to data active on D0-7	tCDLZ	–	–	80	ns
$\overline{\text{CHIPSEL}}$ High to data tristate on D0-7	tCDHZ	–	–	80	ns
$\overline{\text{READ}}$ pulse width Low	tRSPWL	100	–	–	ns
$\overline{\text{READ}}$ Low to data active	tRDLZ	–	–	80	ns
$\overline{\text{READ}}$ High to data tristate	tRDHZ	–	–	80	ns
Address to Valid Data	tPRD	–	–	80	ns
Address setup to $\overline{\text{WRITE}}$ rising edge	tASUW	20	–	–	ns
Address hold from $\overline{\text{WRITE}}$ rising edge	tAHW	10	–	–	ns
$\overline{\text{WRITE}}$ pulse width Low	tWPWL	100	–	–	ns
Data setup to $\overline{\text{WRITE}}$ rising edge	tDSUW	20	–	–	ns
Data hold from $\overline{\text{WRITE}}$ rising edge	tDHW	10	–	–	ns
$\overline{\text{READ}}$ High to $\overline{\text{INT}}$ clear when reading register RD0	tINTR	–	–	400	ns

1. Timing for all outputs assumes a maximum load of 30 pF.
2. “Address” refers to input signals $\overline{\text{CHIPSEL}}$, A0, A1, A2, and A3. “Data” refers to I/O signals D0, D1, D2, D3, D4, D5, D6, and D7.

Table 23. General System and Hardware Mode Timing

Parameter		Min	Typ[1]	Max	Unit
Throughput delay	TDATA to TTIP/TRING				
	272 kbps	–	29.4	36.8	
	400 kbps	–	20.0	25.0	
	528 kbps	–	15.2	18.9	µs
	784 kbps	–	10.2	12.5	
	RTIP/RRING to RDATA				
	272 kbps	–	154	206	
	400 kbps	–	105	140	
	528 kbps	–	79.6	106	µs
	784 kbps	–	53.6	72	
Hardware Mode	“ACTREQ” input transitional pulse width (High or Low)	5	–	–	µs
	“QUIET” transitional pulse width (High-to-Low)	5	–	–	µs

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 23. RESET and INTERRUPT Timing (µP Control Mode)

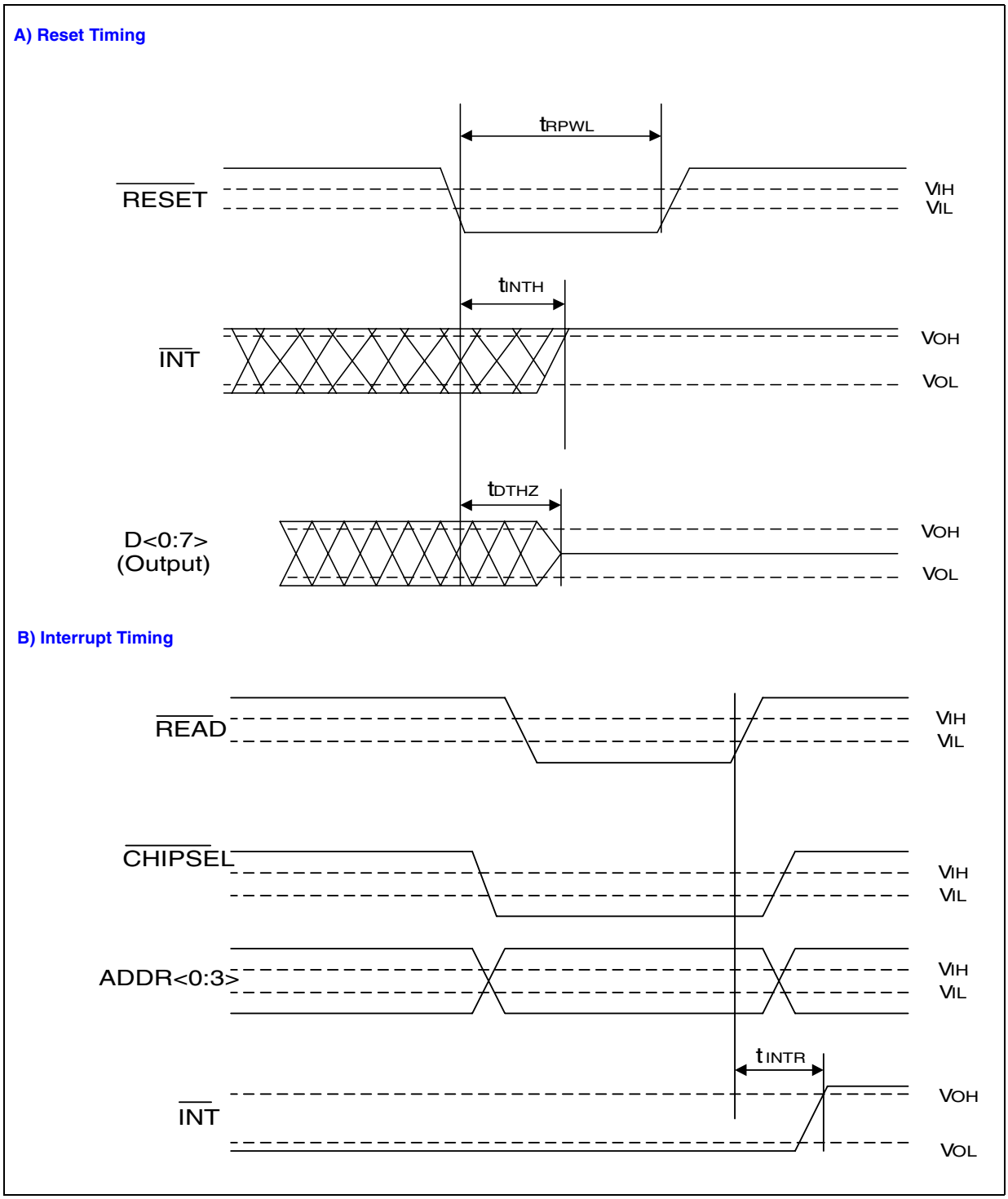
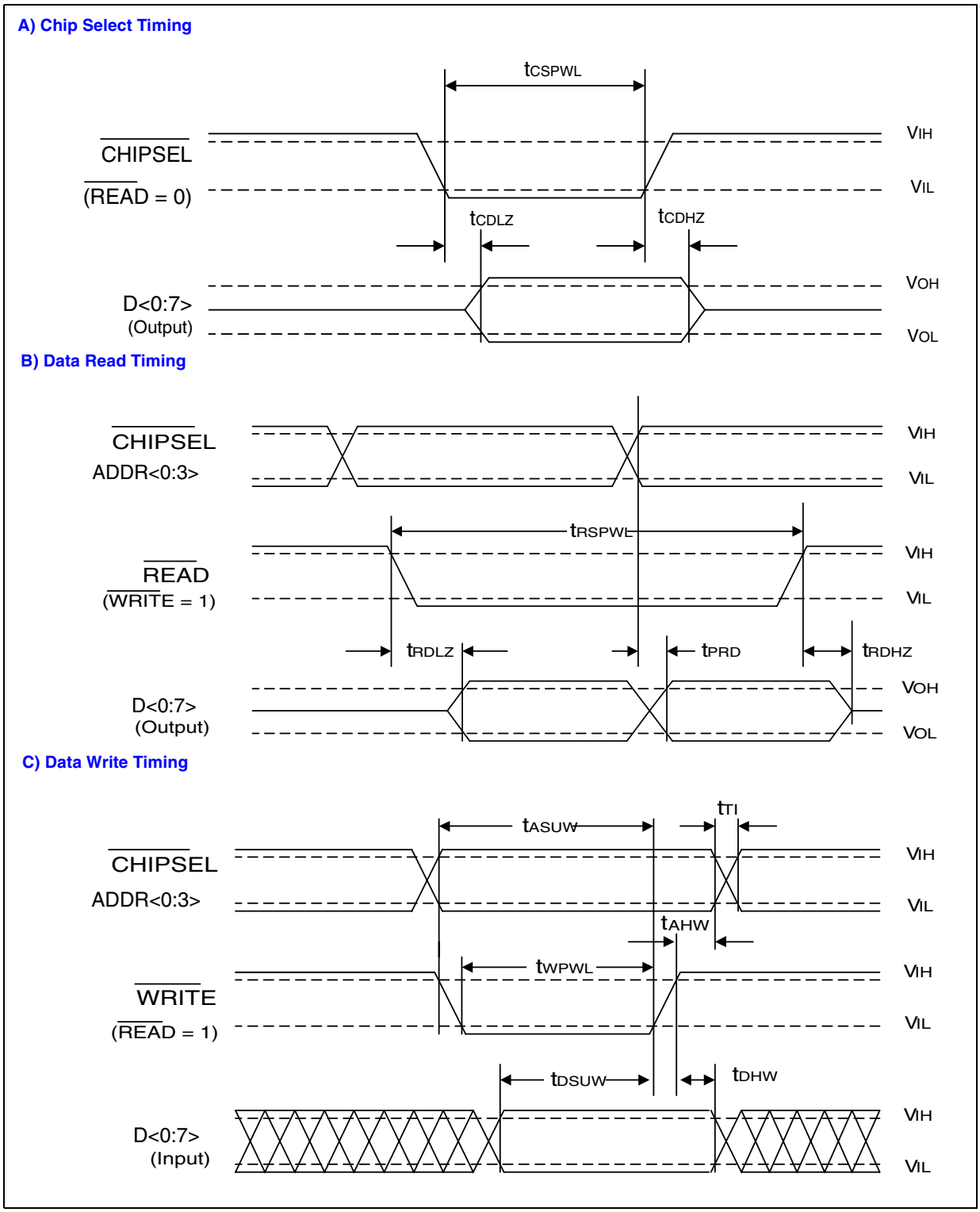


Figure 24. Parallel Data Channel Timing



6.0 Register Definitions

Three write registers and seven read registers are available to the user. Table 24 lists these registers and the following paragraphs describe them in greater detail.

Some of the registers contain *reserved* bits. Software must deal correctly with reserved fields. For reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. In some cases, software must program reserved bit positions to a particular value. This value is defined in the individual bit descriptions.
After asserting the $\overline{\text{RESET}}$ signal, the Data Pump initializes its registers to the default value.

Table 24. Register Summary

Address	Write Registers			Read Registers		
A3-A0	WR#	Name	Table	RD#	Name	Table
0000	WR0	Main Control	25	RD0	Main Status	28
0001	-	*reserved*	-	RD1	Receiver Gain Word	29
0010	WR2	Interrupt Mask	26	RD2	Noise Margin	30
0011	WR3	Read Coefficient Select	27	RD3	Coefficient Read Register (lower byte)	31
0100	-	*reserved*	-	RD4	Coefficient Read Register (upper byte)	31
0101	-	*reserved*	-	RD5	Activation Status	32
0110	-	*reserved*	-	RD6	Receiver AGC and FFE Step Gain	33
0111-1001	-	*reserved*	-	-	*reserved*	-

6.0.1 WR0—Main Control Register

Address: A<3:0> = 0000
Default: 00h
Attributes: Write Only

Control Register bits serve the same purpose in Software Mode as the like-named individual pins in Hardware Mode. Table 25 lists bit assignments for the WR0 register.

Table 25. Main Control Register WR0

Bit	Description
7	**Transmit Test Pattern Enable (TXTST).** Set TXTST to 1 to enable isolated transmit pulse generation. One symbol is output every 4702 or 4706 BIT_CK cycles. TDATA controls the sign and TFP controls the magnitude of the transmitted symbols according to the 2B1Q encoding rules. In the Slave mode when the TXTST mode is selected, the Data Pump may begin activation.
6	**Back-End Loop Back (BELB).** In the Active State, set BELB to 1 to enable an internal, transparent loopback of the MDSP RDATA to TDATA and RFP to TFP.
5	**Front End Loop Back (FELB).** In the Master mode with the Data Pump in the Inactive State, set FELB to 1 to enable an IAFE front-end loopback. The Data Pump will begin activation and transmission on the line, but will ignore any signal from the Slave instead synchronizing to its own transmit signal.
4	**Repeater Mode (RPTR).** The RPTR bit is set to 1 and the MODE pin is pulled High to program the Data Pump for operation on the side of the MDSL repeater driving a remote slave. RPTR is set to 0 and the Master pin is tied Low to program the Data Pump for operation on the side of the repeater driven by the Master.

Table 25. Main Control Register WR0 (Continued)

Bit	Description
3	**Loop Number (LOOPID).** In two loop MDSL applications, LOOPID is set at the Master end of the loop to select the frame sync word format to encode the loop number.
2	**Insertion Loss Measurement Test (ILMT).** Set ILMT to 1 to enable transmission of a scrambled all ones insertion loss measurement test pattern. In the Slave configuration when the ILMT mode is selected, the Data Pump may begin activation.
1	**Quiet Mode (QUIET).** Set QUIET to 1 to force the Data Pump into the Deactivated State with the transmitter silent. Setting QUIET to 0 will not cause the Data Pump to reactivate. In the Slave mode, the Data Pump will not respond to a signal from the Master when QUIET is set to 1, but may activate after QUIET is set to 0 even if the Master transmission has already ceased.
0	**Activation Request (ACTREQ).** In the Master mode when the Data Pump is in the Inactive State and Quiet is set to 0, setting the ACTREQ bit to 1 will initiate an activation sequence. Because ACTREQ is a level- rather than an edge-triggered signal, it should be reset to 0 again within approximately 25 seconds to prevent the immediate start of another activation cycle if the current activation attempt fails. If an activation attempt fails, the processor should allow the Data Pump to remain in the Inactive State where the transmitter is silent for the Activation Timer duration (Table 7) before generating another activation request. This delay will allow the Slave to return to the Inactive State. It is possible to shorten this quiet period following a failed activation by implementing additional algorithms described in the section entitled “Activation State Machines.”

6.0.2 WR2—Interrupt Mask Register

Address: A<3:0> = 0010
Default: 00h
Attributes: Write Only

Table 26 shows the various interrupt masks provided in register WR2.

Table 26. Interrupt Mask Register WR2

Bit	Description
7:6	***Reserved**. Must be set to 0.*
5	**LOSMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the LOS condition.
4	**DEACTMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the DEACTVTD condition.
3	**ACTBMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the $\overline{\text{ACTIVE}}$ condition.
2	**ACTMSK.** 1=Masked. 0=Not Masked. Interrupt mask for the TMR_EXP condition and the ACTIVE condition.
1	***Reserved.** Must be set to 0.*
0	**Enable coefficient read register (CRD1).** 1=Enable. 0=Disable. Used in conjunction with WR3 for reading coefficient values.

6.0.3 WR3—Read Coefficient Select Register

Address: A<3:0> = 0011
Default: 00h
Attributes: Write Only

Table 27 lists the bit maps used to select the coefficient read from the MDSP.

Table 27. Read Coefficient Select Register WR3

Hex Value	Selected Registers	Description
00-07	DFE1-DFE8	DFE coefficients
08-0F	EC1-EC8	Echo Cancellation
10-15	FFE1-FFE6	FFE coefficients 1-6
16-19	*reserved*	–
1A	AGC Tap	AGC Tap
1B-FF	*reserved*	–

6.0.4 RD0—Main Status Register

Address: A<3:0> = 0000
Default: xxh (x = undefined)
Attributes: Read Only

Status Register bits serve the same purpose in Software Mode as the like-named individual pins in Hardware mode. Table 28 lists the bit assignments in this register.

Table 28. Main Status Register RD0

Bit	Active Description
7	**Timer Expiry (TMR_EXP).** Set to 1 to indicate Activation timer expiration. • Causes interrupt on changing from 0 to 1; masked by ACTMSK = 1 • Latched event; reset on read, with persistence while in the Active State
6	**TIP/RING polarity reversed ($\overline{\text{INVERT}}$).** 0 = polarity reversal. Valid only in Active-1 or Active-2 states.
5	**Change Of Frame Alignment (COFA).** Indicates that re-acquisition of frame sync is in a different position with respect to the last frame position. Does not cause interrupt. Latched event; reset on read.
4	**Loss Of Signal (Slave).** 1 = loss of line signal energy detected and entry into the Inactive state.
	Loss of Signal (Master). 1 = loss of signal for 1 second on entering Inactive State. • Causes interrupt on transitions from 0 to 1 or 1 to 0 that are masked by LOSMSK = 1 • LOS/LOS is not a latched event
3	**Loop Number Control (LOOPID).** 0 = loop 1; 1 = loop 2. Valid only in Active States, 0 in all others.
2	**Deactivation Indicator (DEACTVTD).** 1 = expiration of the Deactivation timer and the transition from the Pending Deactivation state to the Deactivated state. • Causes interrupt on changing from 0 to 1; masked when DEACTMSK = 1 • Latched event; reset on read; with persistence while in the Deactivated State
1	**Link Active Indicator, ($\overline{\text{ACTIVE}}$), active Low.** 1 = entry into the Pending Deactivation state. • Causes interrupt on changing from 0 to 1; masked by ACTBMSK = 1 • Latched event; reset on read; with persistence while in the Pending Deactivation State
0	**Link Active Indicator, (ACTIVE), active High.** 1 = Completion of layer 1 activation and entry into the Active-1 state. • Causes interrupt on changing from 0 to 1; masked by ACTMSK = 1 • Latched event; reset on read with persistence if still in the Active State

6.0.5 RD1—Receiver Gain Word Register

Address: A<3:0> = 0001
Default: xxh (x = undefined)
Attributes: Read Only

The 8-bit word in this register is the eight most significant bits of the main FFE AGC tap, which, along with the AGC and DAGC values (RD6), represent the receiver gain required to compensate for line loss, and to normalize the receive 2B1Q pulses to a fixed threshold. Bit b7 (sign bit, always 0) is the MSB with bit b0 the LSB. The AGC tap value is determined as follows:

Table 29. Receiver Gain Word Register

Bit	Description
7:0	FFE AGC Tap Value (eight most significant bits).

6.0.6 RD2—Noise Margin Register

Address: A<3:0> = 0010
Default: xxh (x = undefined)
Attributes: Read Only

The noise margin of the received signal is an input to the MDSL framer's Activation State Machine. The noise margin must reach a threshold level before the MDSL framer can transition to the fully Active State. The MDSP provides a calculated, logarithmic noise margin value used by the MDSL framer. This eight-bit word, stored in register RD2, is available every baud, although updated only every 64 baud. Table 30 shows the noise margin coding. To calculate the SNR, use this equation:

$$SNR = \text{Noise Margin} + 21.5\ dB.$$

Error propagation in the DFE and de-scrambler may introduce some fractional errors in this formula, however, the relationship between the SNR and the noise margin remains valid as long as the noise follows a Gaussian distribution.

Since the average period of the calculation is very short (64 bauds), the recommended procedure for evaluating transmission quality is to average at least 1000 samples.

Table 30. Noise Margin Register RD2
(Noise Margin Coding)

MSB	Bit						LSB	Noise Margin[1]
7	6	5	4	3	2	1	0	
0	0	1	1	0	1	0	1	+26.5
0	0	1	0	1	1	1	1	+23.5
0	0	1	0	1	0	1	1	+21.5
0	0	1	0	1	0	0	1	+20.5
0	0	1	0	0	1	1	1	+19.5
0	0	1	0	0	1	0	1	+18.5

1. Accuracy of noise margin is ±1 dB.

Table 30. Noise Margin Register RD2 (Continued)
(Noise Margin Coding)

MSB	Bit						LSB	Noise Margin[1]
7	6	5	4	3	2	1	0	
0	0	1	0	0	1	0	0	+18.0
0	0	1	0	0	0	1	0	+17.0
0	0	1	0	0	0	0	0	+16.0
0	0	0	1	1	1	1	0	+15.0
0	0	0	1	1	1	0	0	+14.0
0	0	0	1	1	0	1	0	+13.0
0	0	0	1	1	0	0	0	+12.0
0	0	0	1	0	1	1	0	+11.0
0	0	0	1	0	1	0	0	+10.0
0	0	0	1	0	0	1	0	+9.0
0	0	0	1	0	0	0	0	+8.0
0	0	0	0	1	1	1	0	+7.0
0	0	0	0	1	1	0	0	+6.0
0	0	0	0	1	0	1	0	+5.0
0	0	0	0	1	0	0	0	+4.0
0	0	0	0	0	1	1	0	+3.0
0	0	0	0	0	1	0	0	+2.0
0	0	0	0	0	0	1	0	+1.0
0	0	0	0	0	0	0	0	0.0
1	1	1	1	1	1	1	0	-1.0
1	1	1	1	1	1	0	0	-2.0
1	1	1	1	1	0	1	0	-3.0
1	1	1	1	1	0	0	0	-4.0
1	1	1	1	0	1	1	0	-5.0
1	1	1	1	0	1	0	0	-6.0

1. Accuracy of noise margin is ±1 dB.

6.0.7 RD3 (LSB), RD4 (MSB)—Coefficient Read Register

Address: RD3 (A<3:0> = 0011)
RD4 (A<3:0> = 0100)
Default: xxh (x = undefined)
Attributes: Read Only

Coefficient Read Word (read from the MDSP) comes from the location configured in the Read Coefficient Select Register (WR3, Address A<3:0> = 0011). The MDSP updates this word on the rising edge of the receive clock, RX_CK. Read register RD3 is the lower byte, and RD4 is the upper byte.

Table 31. Coefficient Read Register

Bit	Description
7:0	**Coefficient Word Value.** RD3 contains the lower byte; RD4 the upper byte.

6.0.8 RD5—Activation Status Register

Address: A<3:0> = 0101
Default: xxh (x = undefined)
Attributes: Read Only

The ACT bits indicate the current state of the MDSP transceiver during the Activating State as listed in Table 32. For any state other than the Activating State, the ACT bits will be "0000."

Table 32. Activation Status Register RD5

ACT Bits 3:0	State in Master Mode	State in Slave Mode
0000	Inactive	Inactive
0001	Pre-AGC	Wait
0010	Pre-EC	AAGC
0011	SIGDET	EC
0100	AAGC	PLL1
0101	EC	PLL2
0110	PLL	4LVLDET
0111	4LVLDET	FRMDET
1000	FRMDET	–

6.0.9 RD6—Receive Step Gain Register

Address: A<3:0> = 0110
Default: xxh (x = undefined)
Attributes: Read Only

This 8-bit register represents AGC and FFE gain coefficients (GAGC and GFFE, respectively). Bit assignments are listed in Table 33. The approximate line loss (LL) can be determined using these values in the following equation:

$$LL = 20\log_{10}(GFFE * AGC\ tap) + GAGC + 28\ dB.$$

GFFE corresponds to DAGC in the MDSP and GAGC is from the IAFE. Bits ST0-ST2 indicate the Data Pump activation states as shown in Figure 10, Figure 11, and Table 8.

Table 33. Receiver AGC and FFE Step Gain Register RD6

Bit	Description
7	**ST2.** Data Pump Activation State–bit 2.
6	**ST1.** Data Pump Activation State–bit 1.
5:4	**GFFE1, GFFE0.** Digital Gain Word–bit 1 and Digital Gain Word–bit 0. **Bits <5:4>GFFE Value** 00 = 2^0 = 1 01 = 2^1 = 2 10 = 2^2 = 4 11 = 2^3 = 8
3	**ST0.** Data Pump Activation State–bit 0.
2:0	**GAGC2-GAGC0.** Analog Gain Word–bit 2,1 and 0. **Bits <2:0>GAGC Value (dB)** 000 = -12 001 = -10 010 = -8 011 = -6 100 = -4 101 = -2 110 = 0 111 = +2

7.0 Mechanical Specifications

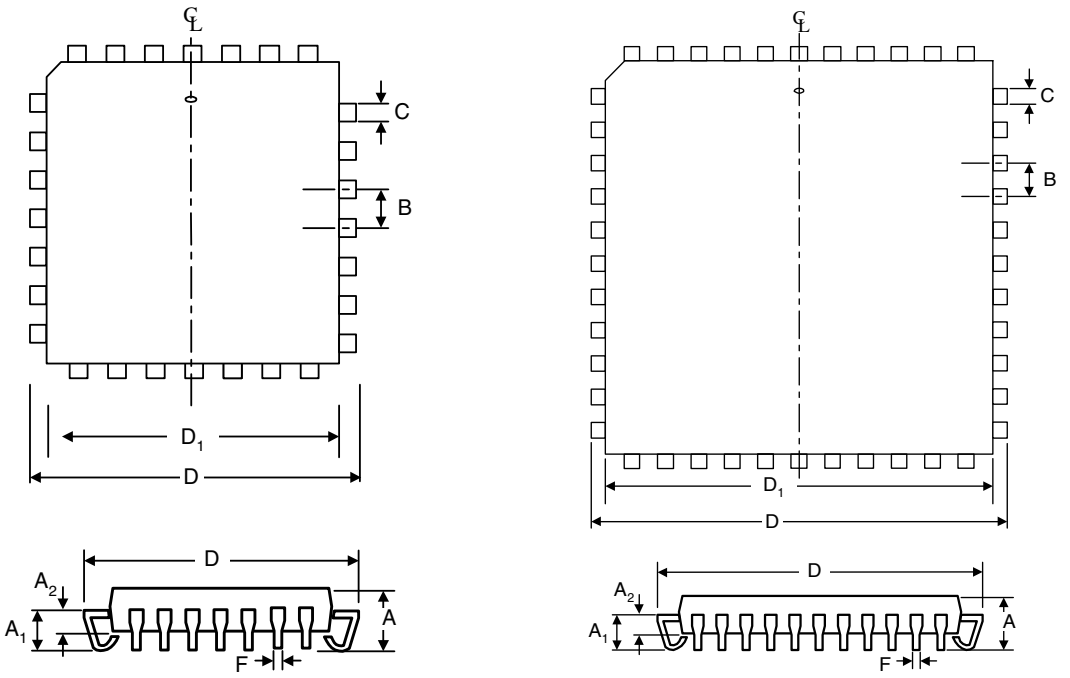
Figure 25. Data Pump Package Specifications

Integrated Analog Front End (IAFE)

- 28-pin PLCC
- P/N SK70721PE
- Extended Temperature Range (-40° to + 85° C)

MDSL Digital Transceiver (MDSP)

- 44-pin PLCC
- P/N SK70720PE
- Extended Temperature Range (-40° to + 85° C)



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	.050 BSC[1] (nominal)		1.27 BSC[1] (nominal)	
C	0.026	0.032	0.660	0.813
D	0.485	0.495	12.319	12.573
D1	0.450	0.456	11.430	11.582
F	0.013	0.021	0.330	0.533

1. BSC—Basic Spacing between Centers.

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	.050 BSC[1] (nominal)		1.27 BSC[1] (nominal)	
C	0.026	0.032	0.660	0.813
D	0.685	0.695	17.399	17.653
D1	0.650	0.656	16.510	16.662
F	0.013	0.021	0.330	0.533

1. BSC—Basic Spacing between Centers.