SIEMENS

ICs for Communications

Framing and Line Interface Component for PCM 30 and PCM 24 FALC54

PEB 2254 Version 1.3

Data Sheet 11.96

T2254-XV13-D1-7600

PEB 2254 **Revision History:**	**Current Version: 11.96**	
Previous Version:	04.96	
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
–	52, 53, 108	Extended CRC4 to Non-CRC4 interworking
–	42, 108	Selected CMI precoding
–	102, 251	Receive/transmit timeslot offset shift in steps of each SCLKR/X (8 MHz) cycles
69, 70, 218, 219	70, 71, 216, 217	Calculation of receive/transmit timeslot offset programming
–	87, 236	Status change interrupt capability
–	113, 261	Loss of signal recovery conditions
–	55, 108, 132, 133	SA6 bit detection according to ETS 300233
–	17, 108	Enable CAS Freeze Output
–	187, 188, 268, 281	Receive pulse density detection
143	141	400 msec time out available in all multiframe formats
296, 300, 303, 307-312, 314	289, 293, 296, 300-305, 307	Electrical specification
145, 293	143, 286	Version status register

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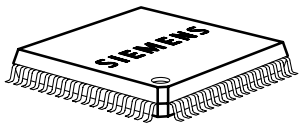
SIEMENS

Framing and Line Interface Component FALC54

PEB 2254

CMOS

FALC54 in PCM 30 Mode



P-MQFP-80-1

1 General Features E1

Line Interface

- Analog receive and transmit circuitry for E1 signals
- Data and clock recovery using an integrated digital phase locked loop
- Low transmitter output impedance for a high return loss with reasonable protection resistors
- Tri-state function of the analog Transmit Line Outputs
- Programmable transmit pulse shape using a minimum number of external components
- Jitter specifications of ITU-T I.431 and G.703 met
- Wander and jitter attenuation/compensation clock smoothing
- Dual rail or single rail digital inputs and outputs
- Unipolar NRZ or CMI for interfacing fibre optical transmission routes
- Selectable line codes (HDB3, AMI)
- Loss of signal indication with programmable thresholds according to ITU-T G.775
- Clock generator for jitter free system clocks and transmit clock using an digital phase locked loop
- Transmit line monitor
- Local loop and remote loop for diagnostic purposes
- Only one type of transformer (ratio1:$\sqrt{2}$) for CEPT 75/120 Ω and T1 100 Ω

Frame Aligner

- Frame alignment/synthesis for 2048 kbit/s according to ITU-T G.704
- Meets newest ITU-T Rec's, ETSI Rec’s.
- Programmable formats for Doubleframe, CRC Multiframe
- Selectable conditions for loss of frame alignment
- CRC4 to Non-CRC4 Interworking of ITU-T G. 706 Annex B
- Error checking via CRC4 procedures according to ITU-T G. 706

Type	Version	Ordering Code	Package
PEB 2254-H	V1.3	Q67103-H6813	P-MQFP-80 (SMD)

- Performance monitoring
  16 bit counter for CRC-, framing errors, code violations, Error monitoring via E bit and SA6 bit
- Insertion and extraction of alarms (AIS, Remote (Yellow) Alarm, AUXP …)
- IDLE code insertion for selectable channels
- 8192 kHz System clock frequency different for receiver and transmitter
- Selectable 2048/4096 kbit/s backplane interface with programmable receive/transmit shifts
  Programmable tri-state function of 4096 kbit/s output via RDO
- Two-frame elastic store for receive route clock wander and jitter compensation (can be reduced to one-frame length for master-slave applications); controlled slip capability and slip indication
- Flexible transparent modes
- Channel loop back, Payload loop back capabilities

Signaling Controller

- HDLC controller
  Bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions, programmable preamble
- CAS controller
- Multiframe synchronization and synthesis ITU-T G.732
- Alarm insertion and detection (AIS and LOS in Timeslot 16)
- Transparent Mode
- FIFO buffers (64 bytes deep) for efficient transfer of data packets.
- Time-slot assignment
  Any combination of time slots selectable for data transfer independent of signaling mode.
- Time-slot 0 SA_{8-4} bit handling via FIFO buffers

MP Interface

- 8/16 bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte or word access)
- Extended interrupt capabilities

General

- Boundary Scan Standard IEEE 1149.1
- Advanced CMOS technology
- P-MQFP-80 Package

The FALC’s power consumption is mainly determined by the line length and type of the cable and typical 450 mW.

1.1 Pin Configuration of FALC
(top view)

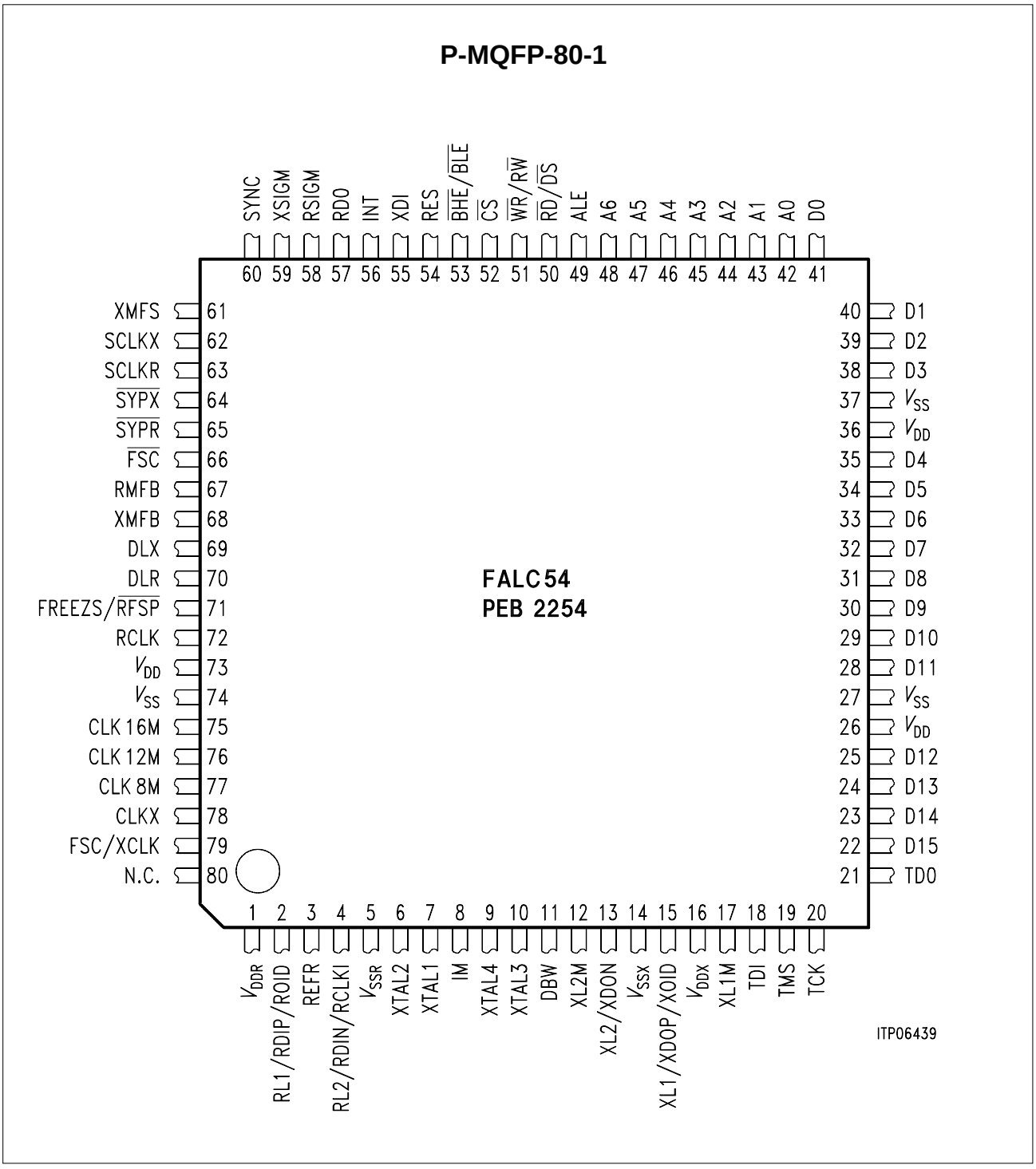


Figure 1

Note: All unused input pins including pin 80 have to be connected to a defined level.

1.2 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
42 … 48	A0 … A6	I	**Address Bus** These inputs interface with seven bits of the system's address bus to select one of the internal registers for read or write.
41 … 38 35 … 28 25 … 22	D0 … D3 D4 … D11 D12 … D15	I/O	**Data Bus** Bi-directional three-state data lines which interface with the system's data bus. Their configuration is controlled by the level of pin DBW: – 8-bit mode (DBW = 0): D0 … D7 are active. D8 … D15 are in high impedance and have to be connected to V_{DD} or V_{SS}. – 16-bit mode (DBW = 1): D0 … D15 are active. In case of byte transfers, the active half of the bus is determined by A0 and $\overline{BHE}$/$\overline{BLE}$ and the selected bus interface mode (via pin IM). The unused half is in high impedance. For detailed information, refer to **chapter 1.6**.
49	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address/data bus. The address information provided on lines A0 … A6 is internally latched with the falling edge of ALE. This function allows the FALC54 to be directly connected to a multiplexed address/data bus. In this case, pins A0 … A6 must be externally connected to the Data Bus pins. In case of demultiplexed mode this pin has to be connected directly to ground or VDD. For detailed information, refer to **chapter 1.6**.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
50	$\overline{RD}$/$\overline{DS}$	I	**Read Enable** (Siemens/Intel bus mode) This signal indicates a read operation. When the FALC54 is selected via $\overline{CS}$ the $\overline{RD}$ signal enables the bus drivers to output data from an internal register addressed via A0 … A6 on to Data Bus. For more information about control/ status register and FIFO access in the different bus interface modes refer to **chapter 1.6**. **Data Strobe** (Motorola bus mode) This pin serves as input to control read/write operations.
51	$\overline{WR}$/R$\overline{W}$	I	**Write Enable** (Siemens/Intel bus mode) This signal indicates a write operation. When $\overline{CS}$ is active the FALC54 loads an internal register with data provided via the Data Bus. For more information about control/status register and FIFO access in the different bus interface modes refer to **chapter 1.6**. **Read/Write Enable** (Motorola bus mode) This signal distinguishes between read and write operation.
52	$\overline{CS}$	I	**Chip Select** A low signal selects the FALC54 for read/write operations.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
54	RES	I	**Reset** A high signal on this pin forces the FALC54 into reset state. During Reset the FALC54 needs active clocks on pins SCLKR, SCLKX and XTAL1 (XTAL3 only if xslicer mode selectable by LIM1.JATT/RL =10) will be used. During Reset – all uni-directional output stages are in high-impedance state, except pins CLK16M, CLK12M, CLK8M, CLKX, $\overline{\text{FSC}}$, XCLK and RCLK – all bi-directional output stages (data bus) are in high-impedance state if signal $\overline{\text{RD}}$ is "high", "output" XTAL2/4 is in high-impedance if input XTAL1/3 is "high".
53	$\overline{\text{BHE}}$/$\overline{\text{BLE}}$	I	**Bus High Enable** (Siemens/Intel bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus (D8 … D15). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}. Refer to **chapter 1.6** for detailed information. **Bus Low Enable** (Motorola bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus (D0 … D7). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}. Refer to **chapter 1.6** for detailed information.
11	DBW	I	**Data Bus Width** (Bus Interface Mode) A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{\text{BHE}}$/$\overline{\text{BLE}}$.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
56	INT	O/oD	**Interrupt Request** INT serves as general interrupt request which may include all interrupt sources. These interrupt sources can be masked via registers IMR0 … 4. Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR0 … 3. Output characteristics (push-pull active low/ high, open drain) are determined by programming the IPC register.
8	IM	I	**Interface Mode** The level at this pin defines the bus interface mode: A low signal on this input selects the INTEL interface mode. A high signal on this input selects the Motorola interface mode.
1	V_{DDR}	I	**Positive Power Supply** for the analog receiver.
2	RL1	I	**Line Receiver 1** Analog Input from the external transformer. Selected if LIM1.DRS = 0.
	RDIP	I	**Receive Data Input Positive** Digital input for received dual rail PCM(+) route signal which will be latched with the internal generated Receive Route Clock. An internal DPLL will extract the Receive Route Clock from the incoming data pulse. The Duty cycle of the receiving signal has to be closely to 50 %. The Dual Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input sense is selected by bit RC0.RDIS (after Reset: active low).
	ROID	I	**Receive Optical Interface Data** Unipolar data received from fibre optical interface with 2048 kbit/s. Latching of data is done with the falling edge of RCLKI. Input sense is selected by bit RC0.RDIS. The Single Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 0.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
3	REFR	O	**Reference Resistance** of 12K ± 1 % connected to V_{SS}
4	RL2	I	**Line Receiver** 2 Analog Input from the external transformer. Selected if LIM1.DRS = 0.
	RDIN	I	**Receive Data Input Negative** Input for received dual rail PCM(-) route signal which will be latched with the internal generated Receive Route Clock. An internal DPLL will extract the Receive Route Clock from the incoming data pulse. The Duty cycle of the receiving signal has to be closely to 50 %. The dual rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input sense is selected by bit RC0.RDIS (after Reset: active low).
	RCLKI	I	**Receive Clock Input** Receive clock input for the optical interface if LIM1.DRS = 1 and FMR0.RC1/0 = 00. Clock frequency: 2048 kHz
5	V_{SSR}	I	**Power Ground Supply** for analog receiver
6 7	XTAL2 XTAL1	O I	**Crystal Connection 16.384 MHz** When an external clock is used, normally if the bit LIM0.MAS is set, the FALC54 functions as a master.
9 10	XTAL4 XTAL3	O I	**Crystal Connection 16.384 MHz** A crystal has only to be connected to these pins to generate the transmit clock if XSLICER-Mode (LIM1.JATT=1 and LIM1.RL=0) is selected.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
13	XL2	O	**Transmit Line 2** Analog output for the external transformer. Selected if LIM1.DRS = 0. After Reset this pin is in a high impedance state until register FMR0.XC1 is set to one.
	XDON	O	**Transmit Data Output Negative** This digital output for transmitted dual rail PCM(-) route signals can provide – half bauded signals with 50% duty cycle (LIM0.XFB = 0) or – full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output sense is selected by bit LIM0.XDOS (after Reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
14	V_{SSX}	I	**Ground** for analog transmitter

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
15	XL1	O	**Transmit Line 1** Analog output for the external transformer. Selected if LIM1.DRS = 0. After Reset this pin is in a high impedance state until register FMR0.XC1 is set to one.
	XDOP	O	**Transmit Data Output Positive** This digital output for transmitted dual rail PCM(+) route signals can provide – half bauded signals with 50% duty cycle (LIM0.XFB = 0) or – full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output sense is selected by bit LIM0.XDOS (after Reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
	XOID	O	**Transmit Optical Interface Data** Unipolar data sent to fibre optical interface with 2048 kbit/s which will be clocked off on the positive transitions of XCLK. Clocking off data in NRZ code is done with 100 % duty cycle. Data in CMI code are shifted out with 50 % or 100 % duty cycle according to the CMI coding. Output sense is selected by bit LIM0.XDOS (after Reset: Data are sent active high). The single rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 0. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
17	XL1M	I	**Transmit Line 1 Monitor** Analog input from the external transmit transformer (XL1). This pin must be connected otherwise the XL1 pin could be set in a high impedance state. If digital inputs are selected (LIM1.DRS = 1) this input has to be switched to V_{SSX}.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
12	XL2M	I	**Transmit Line 2 Monitor** Analog input from the external transmit transformer (XL2). This pin must be connected otherwise the XL2 pin could be set in a high impedance state. If digital inputs are selected via LIM1.DRS = 1 this input has to be switched to V_{SSX}.
16	V_{DDX}	I	**Positive Power Supply** for analog transmitter
79	XCLK FSC	O O	**Transmit Clock** Transmit clock frequency: 2048 kHz. Derived from the SCLKX or RCLK or internally generated. If LIM1.EFSC is set high an **8-kHz Frame Synchronization Pulse** is output via this pin. The synchronization pulse is active high for one 2 MHz cycle (pulse width = 488 ns) and derived from clock supplied by pin XTAL1.
80	N.C.		Not connected. For further application this pin should be connected to V_{SS}.
66	$\overline{\text{FSC}}$	O	**8-kHz Frame Synchronization Pulse** is active low for one 2 MHz cycle (pulse width = 488 ns) and derived from the clock supplied by pin XTAL1.
75	CLK16M	O	**System Clock** 16.384 MHz
76	CLK12M	O	**System Clock** 16.384 MHz only if a crystal or an oscillator is connected to XTAL3/4.
77	CLK8M	O	**System Clock** 8.192 MHz The frequency is derived from the clock supplied by pin XTAL1.
78	CLKX	O	**System Clock Output** Output frequencies are: 2.048 MHz or 4.096 MHz inverted or non-inverted. The frequency and sense on this pin is selectable via LIM0.SCL1/0 and is derived from the clock supplied by pin XTAL1.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
60	SYNC	I	**Clock Synchronization** If a clock is detected at the SYNC pin the FALC54 synchronizes to this 2.048 MHz clock. This pin has to be connected to V_{SS} if no clock is supplied.
72	RCLK	O	**Receive Clock** Extracted from the incoming data pulses Clock frequency: 2048 kHz If LIM0.ELOS is set, the RCLK is set high in case of loss of signal (FRS0.LOS=1).
57	RDO	O	**Receive Data Out** Received data which is sent to the system internal highway with 4096 kbit/s or 2048 kbit/s (bit FMR1.IMOD). In 4096 kbit/s mode data is shifted out in that channel phase which is selected by register RC0.SICS.The other channel phase is set in tri-state. Clocking off data is done with the falling edge of SCLKR. The delay between the beginning of time-slot 0 and the initial edge of SCLKR (after $\overline{\text{SYPR}}$ goes active) is determined by the values of Receive Time-slot Offset RC1.RTO5 … 0, Receive Clock-slot Offset RC0.RCO2 … 0 and RC0.RCOS.
71	$\overline{\text{RFSP}}$	O	**Receive Frame Synchronous Pulse** (active low) Framing pulse derived from the received PCM route signal. During loss of synchronization (bit FRS0.LFA), this pulse is suppressed (not influenced during alarm simulation). Pulse frequency: 8 kHz Pulse width: 488 ns Setting of FMR3.CFRZ the status of the CAS synchronizer will be output via this pin. It is set high if the CAS controller is in the asynchronous state.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
70	DLR	O	**Data Link Bit Receive** Marks the SA8-4 bits within the data stream on RDO. The SA8-4 bit positions in time-slot 0 of every frame not containing the frame alignment signal are selected by register XC0.SA8E-SA4E.
68	XMFB	O	No function
59	XSIGM	O	**Transmit Signaling Marke**r Marks the transmit time-slots which are defined by register TTR1-4 of every frame transmitted via port XDI. In 4096 kbit/s mode XSIGM is active only during the channel phase which is selected by RC0.SICS.
65	$\overline{\text{SYPR}}$	I	**Synchronous Pulse Receive** Defines the beginning of time-slot 0 at system highway port RDO in conjunction with the values of registers RC0.RCO, RC1.RTO and RC0.RCOS. Sampling is done with the falling edge of the SCLKR clock. Pulse Cycle: Integer multiple of 125 µs.
64	$\overline{\text{SYPX}}$	I	**Synchronous Pulse Transmit** Defines the beginning of time-slot 0 at system highway port XDI in conjunction with the values of registers XC0.XCO, XC1.XTO and XC1.XCOS. Sampling is done with the falling edge of the SCLKX clock. Pulse Cycle: Integer multiple of 125 µs.
63	SCLKR	I	**System Clock Receive** Working clock for the FALC54 with a frequency of 8192 kHz.
62	SCLKX	I	**System Clock Transmit** Working clock for the FALC54 with a frequency of 8192 kHz.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
55	XDI	I	**Transmit Data In** Transmit data received from the system internal highway with 4096 kbit/s or 2048 kbit/s (bit FMR1.IMOD). Latching of data is done with negative transitions of SCLKX. In 4096 kbit/s mode data is sampled in the first channel phase if RC0.SICS is low. If RC0.SICS is high data is sampled in the second channel phase. The delay between the beginning of time-slot 0 and the initial edge of SCLKX (after $\overline{\text{SYPX}}$ goes active) is determined by the values of transmit time-slot offset XC1.XTO5 … 0, transmit clock-slot offset XC0.XCO2 … 0 and XC1.XCOS.
69	DLX	O	**Data Link Bit Transmit** Marks the SA8-4 bits within the data stream on XDI. The SA8-4 bit positions in time-slot 0 of every frame not containing the frame alignment signal are selected by register XC0.SA8E-SA4E.
58	RSIGM	O	**Receive Signaling Marker** Marks the time-slots which are defined by register RTR1-4 of every received frame at port RDO. In 4096 kbit/s mode RSIGM is active high only during the channel phase which is selected by RC0.SICS.
67	RMFB	O	**Receive Multiframe Begin** RMFB marks the beginning of every received multiframe (RDO). First Bit of the FAS word in frame 1 of the multiframe. RMFB is always active high for one 2048 kbit/s period. In 4096 kbit/s mode RMFB is active during the first two bits of the multiframe.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
61	XMFS	I	**External Transmit Multiframe Synchronization** This port operates as an input for External Transmit Multiframe Synchronization which defines frame 1 of the Multiframe on XDI. Minimum pulse length is 244 ns. Latching is done equivalent to latching data via XDI. The signal has to be issued during frame 1 and has to be reset at least one bit before begin of frame 2. Recommended: XMFS begins with the first bit of time-slot 0, frame 1 of XDI. **Note:** A new multiframe position has been settled at least one multiframe after pulse XMFS has been supplied.
27, 37, 74	V_{SS}	I	**Power Ground** Supply for digital subcircuits (0 V) For correct operation, all three pins have to be connected to ground.
26, 36, 73	V_{DD}	I	**Positive Power Supply** for the digital subcircuits (5 V) For correct operation, all three pins have to be connected to positive power supply.
18	TDI	I	**Test Data Input** for Boundary Scan acc. to IEEE Std. 1149.1
21	TDO	O	**Test Data Output** for Boundary Scan
19	TMS	I	**Test Mode Select** for Boundary Scan
20	TCK	I	**Test Clock** for Boundary Scan

1.3 Logic Symbol

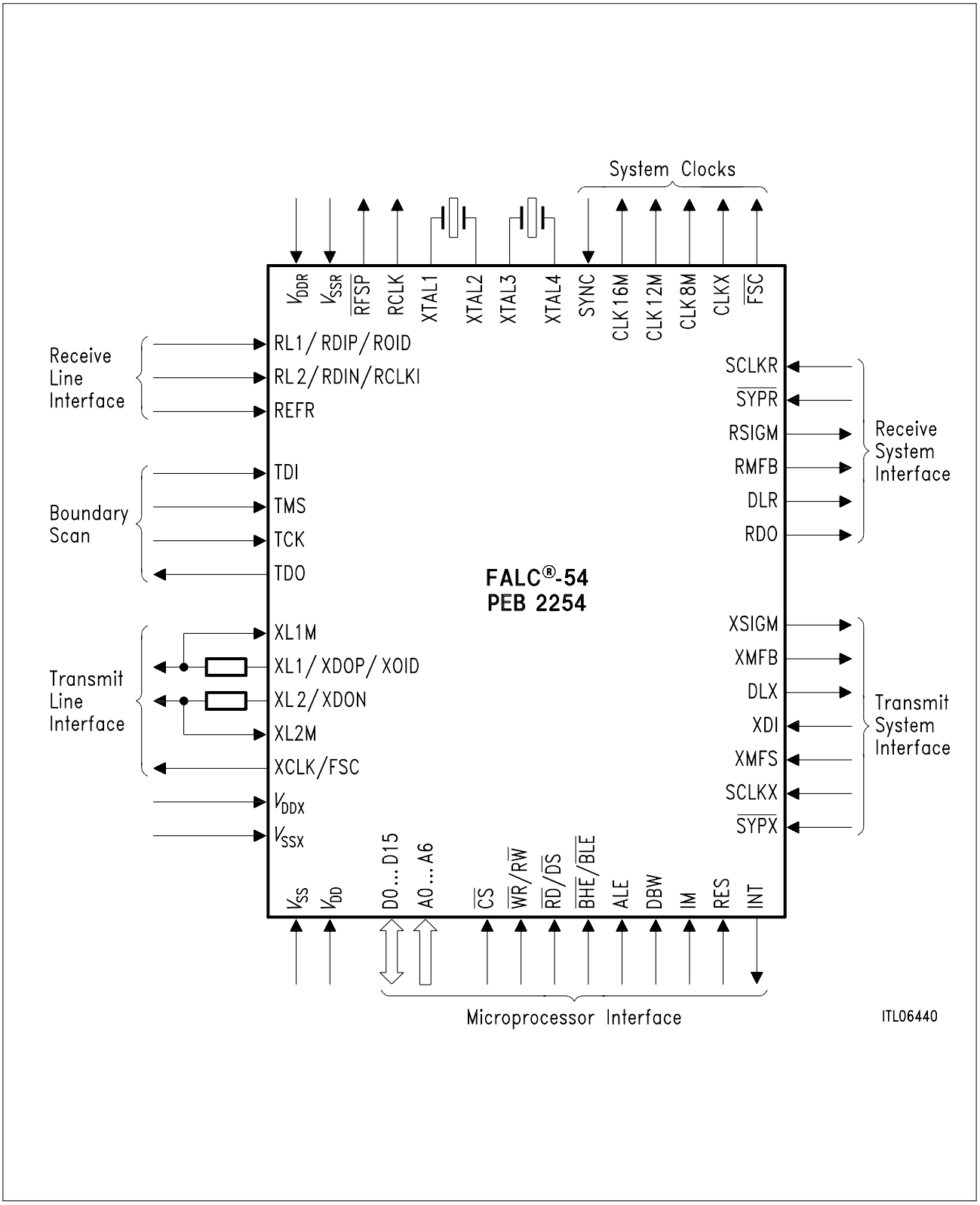


Figure 2
FALC54 Logic Symbol

1.4 Functional Block Diagram

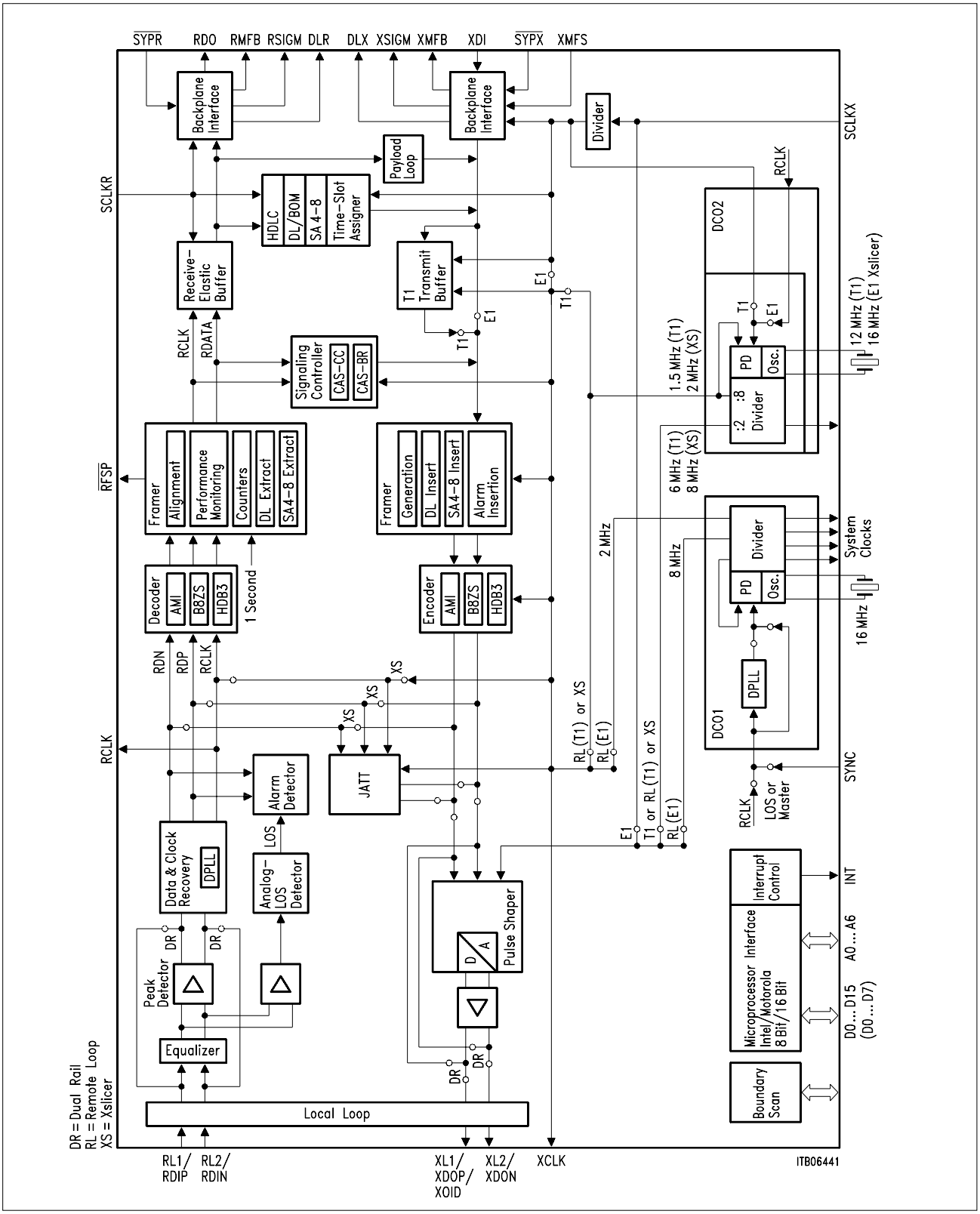


Figure 3
Functional Block Diagram PEB 2254

1.5 System Integration

The figures below show a multiple link application and a NT application.

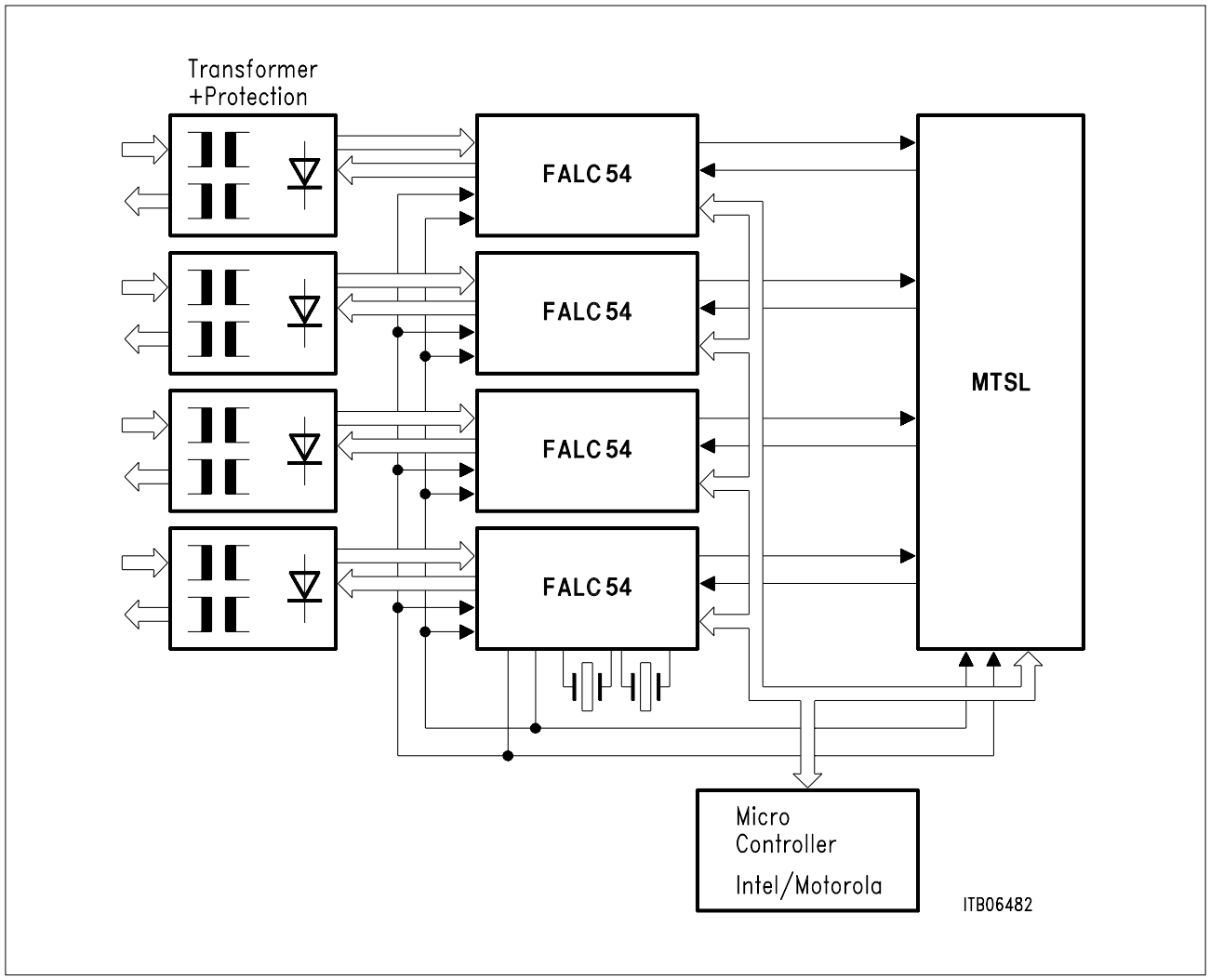


Figure 4
Multiple Link Application

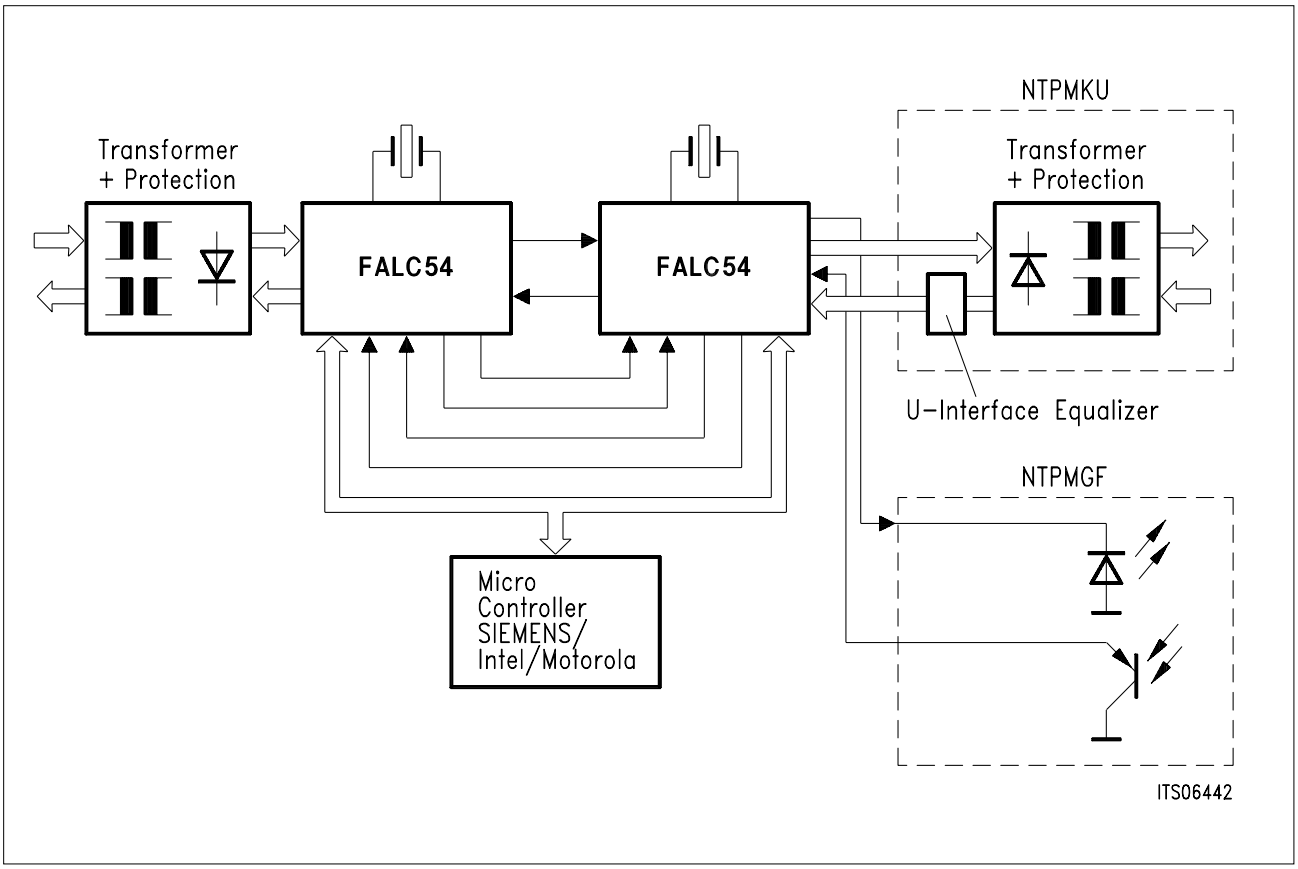


Figure 5
NT - Application

1.6 Microprocessor Interface

The communication between the CPU and the FALC54 is done via a set of directly accessible registers. The interface may be configured as Siemens/Intel or Motorola type with a selectable data bus width of 8 or 16 bits.

The CPU transfers data to/from the FALC54 (via 64 byte deep FIFOs per direction and channel), sets the operating modes, controls function sequences, and gets status information by writing or reading control/status registers. All accesses can be done as byte or word accesses if enabled. If 16-bit bus width is selected, access to lower/upper part of the data bus is determined by address line A0 and signal $\overline{\text{BHE}}/\overline{\text{BLE}}$ as shown in **table 1** and **2**.

In **table 3** is shown how the ALE (address latch enable) line is used to control the bus structure and interface type. The switching of ALE allows the FALC54 to be directly connected to a multiplexed address/data bus.

Mixed Byte/Word Access to the FIFOs

Reading from or writing to the internal FIFOs (RFIFO and XFIFO of each channel) can be done using a 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. Randomly mixed byte/word access to the FIFOs is allowed without any restrictions.

Table 1
Data Bus Access (16-Bit Intel Mode)

$\overline{\text{BHE}}$	A0	Register Access	FALC54 Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D0 – D15
0	1	Register byte access (odd addresses)	D8 – D15
1	0	Register byte access (even addresses)	D0 – D7
1	1	No transfer performed	None

Table 2
Data Bus Access (16-Bit Motorola Mode)

BLE	A0	Register Access	FALC54 Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D0 – D15
0	1	Register byte access (odd addresses)	D0 – D7
1	0	Register byte access (even addresses)	D8 – D15
1	1	No transfer performed	None

Table 3
Selectable Bus and Microprocessor Interface Configuration

ALE	IM	Microprocessor interface	Bus Structure
GND/VDD	1	Motorola	demultiplexed
GND/VDD	0	Intel	demultiplexed
switching	0	Intel	multiplexed

The assignment of registers with even/odd addresses to the data lines in case of 16-bit register access depends on the selected microprocessor interface mode:

Siemens/Intel	(Adr. n + 1)	(Adr. n)
Motorola	(Adr. n)	(Adr. n + 1)

Data Lines	D15	D8	D7	D0

n: even address

Complete information concerning register functions is provided in – Detailed Register Description.

FIFO Structure

In transmit and receive direction of the signaling controller 64-byte deep FIFOs are provided for the intermediate storage of data between the system internal highway and the CPU interface. The FIFOs are divided into two halves of 32-bytes. Only one half is accessible to the CPU at any time.

In case 16-bit data bus width is selected by fixing pin DBW to logical ‘1’ word access to the FIFOs is enabled. Data output to bus lines D0-D15 as a function of the selected interface mode is shown in **figure 6** and **7**. Of course, byte access is also allowed.The effective length of the accessible part of RFIFO can be changed from 32 bytes (RESET value) down to 2 bytes.

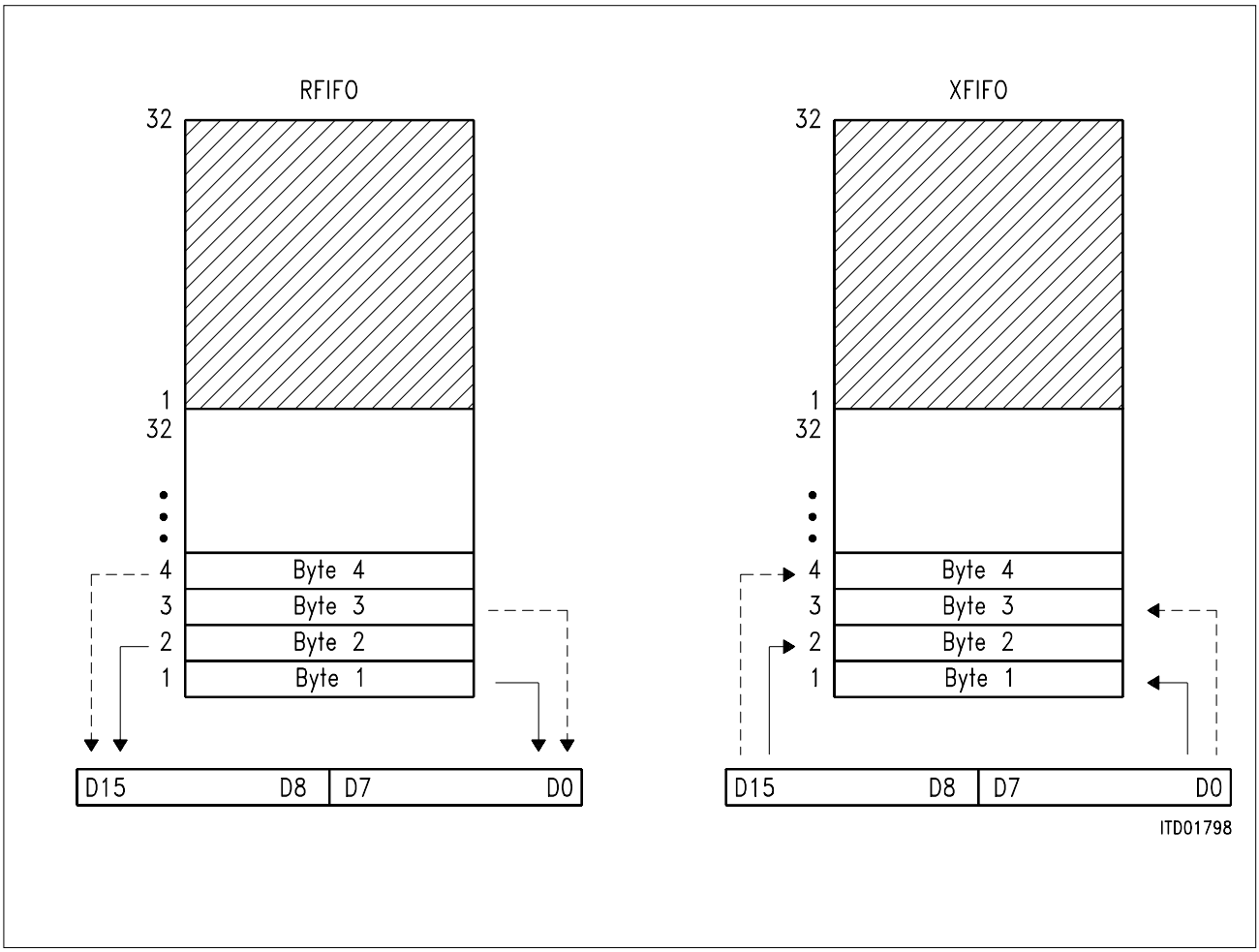


Figure 6
FIFO Word Access (Intel Mode)

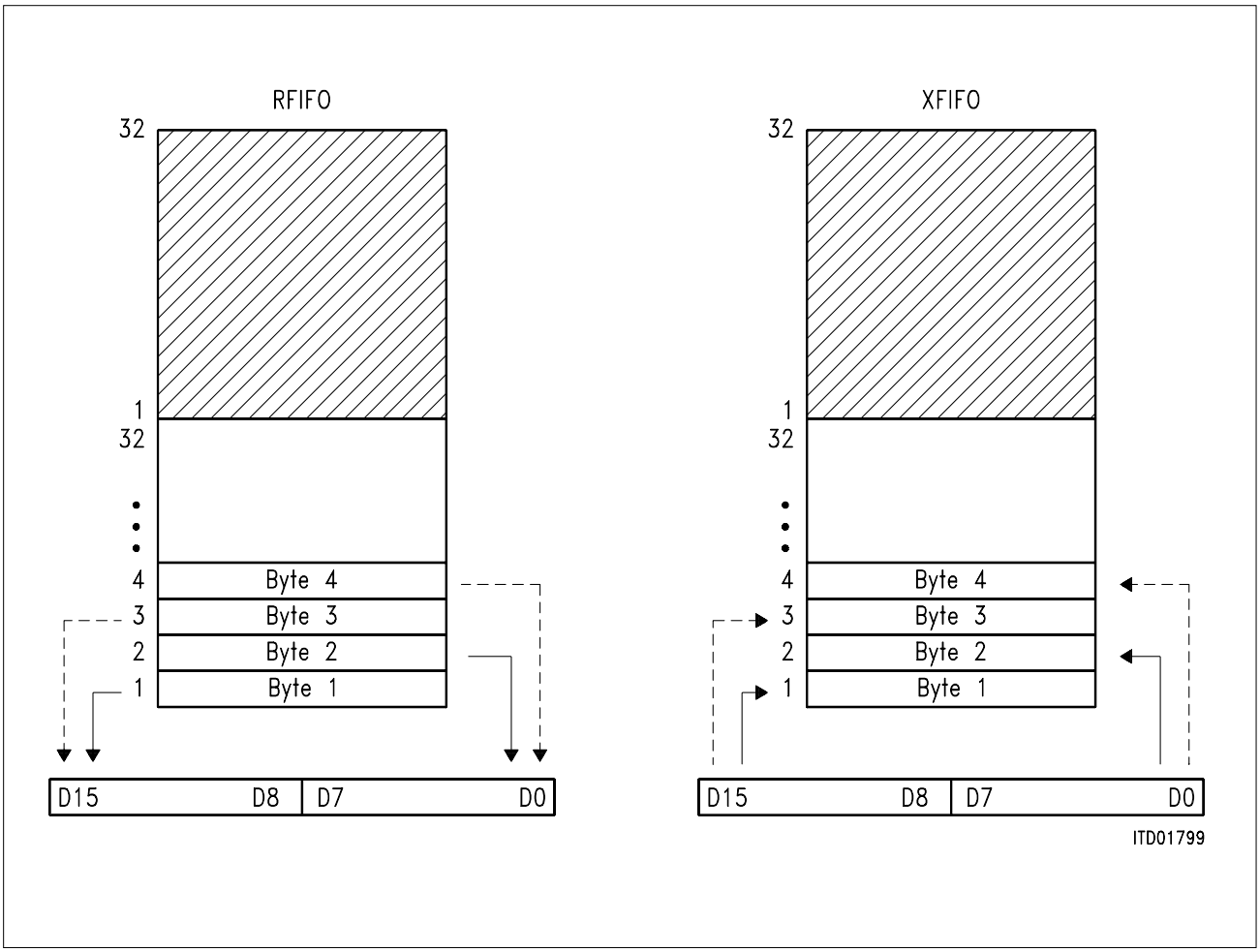


Figure 7
FIFO Word Access (Motorola Mode)

Interrupt Interface

Special events in the FALC54 are indicated by means of a single interrupt output with programmable characteristics (open drain, push-pull; IPC register), which requests the CPU to read status information from the FALC, or to transfer data from/to FALC.

Since only one INT request output is provided, the cause of an interrupt must be determined by the CPU by reading the FALC's interrupt status registers (GIS, ISR0, ISR1, ISR2, ISR3) that means the interrupt at pin INT and the interrupt status bits are reset by reading the interrupt status registers. Register ISR0-3 are from type "Clear on Read".

The structure of the interrupt status registers is shown in **figure 8**.

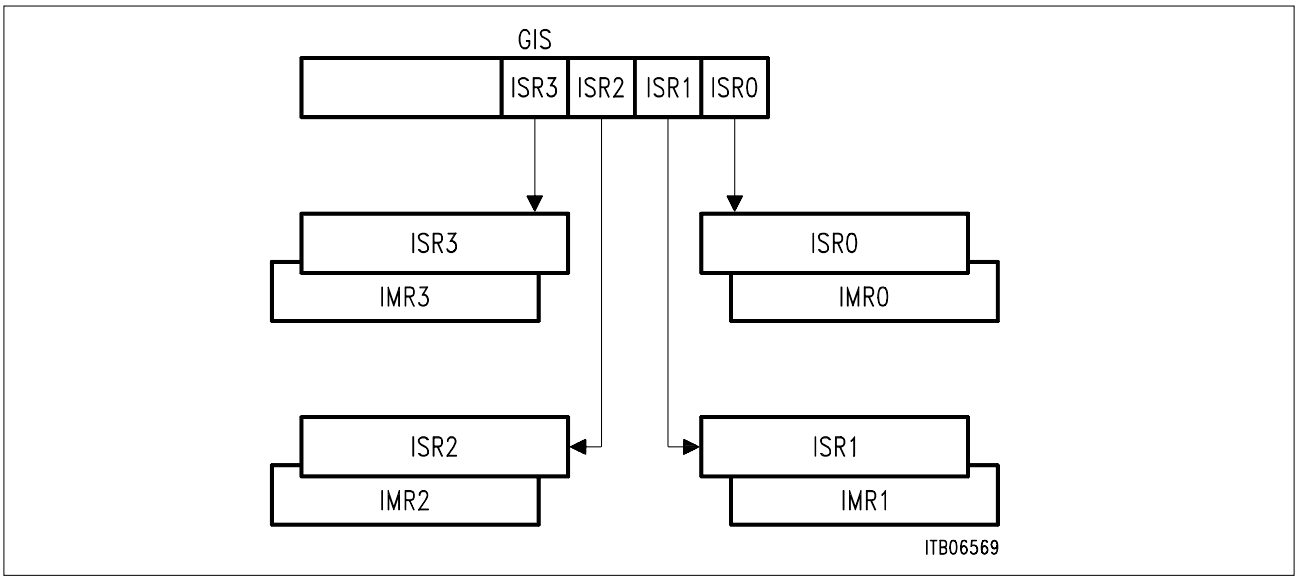


Figure 8
FALC54 Interrupt Status Registers

Each interrupt indication of registers ISR0, ISR1, ISR2 and ISR3 can be selectively masked by setting the corresponding bit in the corresponding mask registers IMR0, IMR1, IMR2, IMR3. If the interrupt status bits are masked they neither generate an interrupt at INT nor are they visible in ISR0-3.

GIS, the non-maskable Global Interrupt Status Register, serves as pointer to pending channel related interrupts. After the FALC54 has requested an interrupt by activating its INT pin, the CPU should first read the Global Interrupt Status register GIS to identify the requesting interrupt source register. After reading the assigned interrupt status registers ISR0- ISR3, the pointer in register GIS is cleared or updated if another interrupt requires service.

If **all** pending interrupts are acknowledged by reading (GIS is reset), pin INT goes inactive.

Updating of interrupt status registers ISR0…3 and GIS is only prohibited during read access.

Masked Interrupts Visible in Status Registers

The Global Interrupt Status register (GIS) indicates those interrupt status registers with active interrupt indications (GIS.ISR0-3).

An additional mode can be selected via bit IPC.VIS.

In this mode, masked interrupt status bits neither generate an interrupt at pin INT nor are they visible in GIS, **but are displayed in the respective interrupt status register(s) ISR0..3**.

This mode is useful when some interrupt status bits are to be polled in the individual interrupt status registers.

Notes:

- *In the visible mode, all active interrupt status bits, whether the corresponding actual interrupt is masked or not, are reset when the interrupt status register is read. Thus, when polling of some interrupt status bits is desired, care must be taken that unmasked interrupts are not lost in the process.*
- *All unmasked interrupt statuses are treated as before.*

Please note that whenever polling is used, all interrupt status registers concerned have to be polled individually (no “hierarchical” polling possible), since GIS only contains information on actually generated - i.e. unmasked-interrupts.

2 General Functions and Device Architecture E1

2.1 Functional Description E1

2.1.1 Receive Path

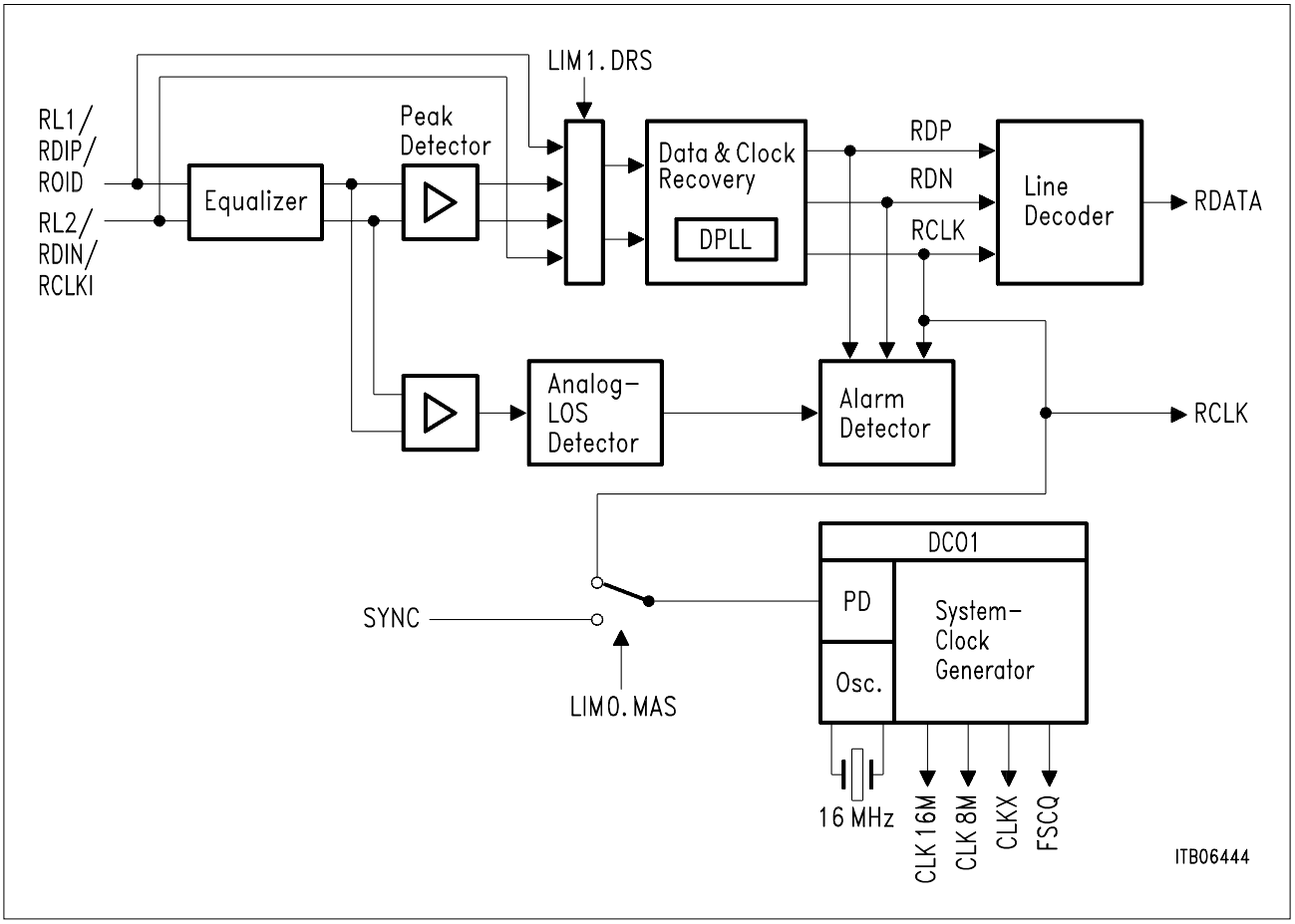


Figure 9
Receive Clock System

Receive Line Interface

For data input, three different data types are supported:

- Ternary coded signals received at multifunction ports RL1 and RL2 from a 6 dB ternary interface. The ternary interface is selected if LIM1.DRS is reset.
- Digital dual rail signals received at ports RDIP and RDIN. The dual rail interface is selected if LIM1.DRS and FMR0.RC1 is set.
- Unipolar data at port ROID received from a fibre optical interface. The optical interface is selected if LIM1.DRS is set and FMR0.RC1 is reset.

Receive Clock and Data Recovery

The analog received signal at port RL1/2 is equalized and then peak-detected to produce a digital signal. The digital received signal at port RDIP/N is directly forwarded to the DPLL. The receive clock and data recovery extracts the route clock RCLK from the data stream received at the RL1/2, RDIP/RDIN or ROID lines and converts the data stream into a single rail, unipolar bit stream. The clock and data recovery works with the frequency supplied by XTAL1 and XTAL2. Normally the clock that is output via pin RCLK is the recovered clock from the signal provided by RL1/2 or RDIP/N has a duty cycle close to 50 %. The free run frequency is defined by XTAL1/2 devided by 8 in periods with no signal.

Receive Line Coding

The HDB3 line code or the AMI coding is provided for the data received from the ternary or the dual rail interface. In case of the optical interface a selection between the NRZ code and the CMI Code (1T2B) with HDB3 postprocessing is provided. If CMI code (1T2B) is selected the receive route clock will be recovered from the data stream. The 1T2B decoder does not correct any errors. In case of NRZ coding data will be latched with the falling edge of pin RCLKI. The HDB3 code is used along with double violation detection or extended code violation detection (selectable). In AMI code all code violations will be detected.
The detected errors increment the code violation counter (16 bits length).

When using the optical interface with NRZ coding, the decoder is by-passed and no code violations will be detected.

Additionally, the receive line interface comprises the alarm detection for Alarm Indication Signal AIS, the Loss of Signal LOS and the Auxiliary Pattern AUXP (unframed and continuous bitstream of alternating ONEs and ZEROs).

The signal at the ternary interface is received at both ends of a transformer.

The operating modes 75 or 120 Ω are selectable by switching resistors in parallel. This selection does not require changing transformers.

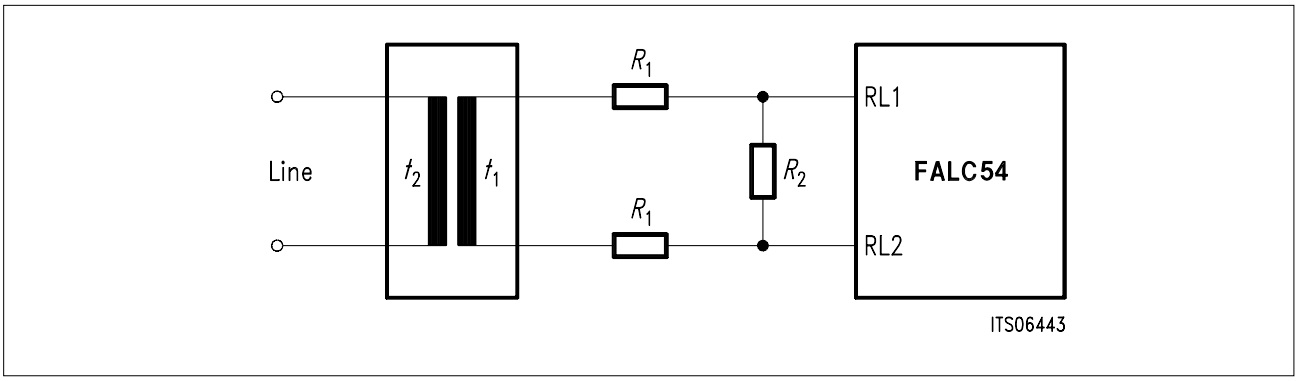


Figure 10
Receiver Configuration

Recommended Receiver Configuration Values

Parameter	Characteristic Impedance [Ω]	
	120	**75**
R_1 (± 2.5 %) [Ω]	25	0
$t_2 : t_1$	$1 : \sqrt{2}$	$1 : \sqrt{2}$
R_2 (± 2.5 %) [Ω]	190	150

Jitter free system clocks (16 / 8 / 4 / 2 MHz and 8 kHz) are generated by the internal PLL circuit DCO1. The DCO1 can work in two different modes:

- Slave mode
  In Slave mode, the DCO1 will be synchronized on the recovered route clock. In case of LOS the DCO1 switches automatically to Master mode.
- Master mode
  In Master mode the oscillator is in free running mode if pin SYNC is connected to VSS. If there is a frequency of 2.048 MHz at the SYNC input the DCO1 is then synchronized to this input.

Loss of Signal Detection

There are different definitions for detecting Loss of Signal (LOS) alarms in the ITU-T G.775 and ETS 300233. The FALC54 covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable via register IPC.SCI.

- Detection:
  An alarm will be generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” in the digital receive interface means a logical zero on pins RDIP/RDIN/ROID. A pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS=0). The receive signal level Q is programmable via three control bits LIM1.RIL2-0 in a range of about 1400 to 200 mV differential voltage between pins RL1/2. The number N can be set via an 8 bit register PCD. The contents of the PCD register will be multiplied by 16, which results in the number of pulse periods or better, the time which has to suspend until the alarm has to be detected. The range results therefore from 16 to 4096 pulse periods. ETS300233 requires detection intervals of at least 1 ms. This time period results always in a LFA (Loss of Frame Alignment) before a LOS will be detected.
- Recovery:
  In general the recovery procedure starts after detecting a logical ‘one’ (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM1.RIL2-0) of the nominal pulse. The value in the 8 bit register PCR

defines the number of pulses (1 to 255) to clear the LOS alarm. Additional recovery conditions may be programmed by register LIM2.

Jitter Attenuator

Together with a PLL and a tunable crystal attenuation of received input jitter is done in the clock- and data-recovery and either in the received elastic buffer (2 frames) or in the jitter attenuator “JATT“ block of figure 3. The attenuator consists of a 288 Bit FIFO. The FIFO is placed in the transmitter and will be active if bit LIM1.JATT=1 , Remote Loop or Xslicer mode active.
The jitter attenuator meets the jitter transfer requirements of the Rec. I.431 and G.735/736 (refer to **figure 11**).

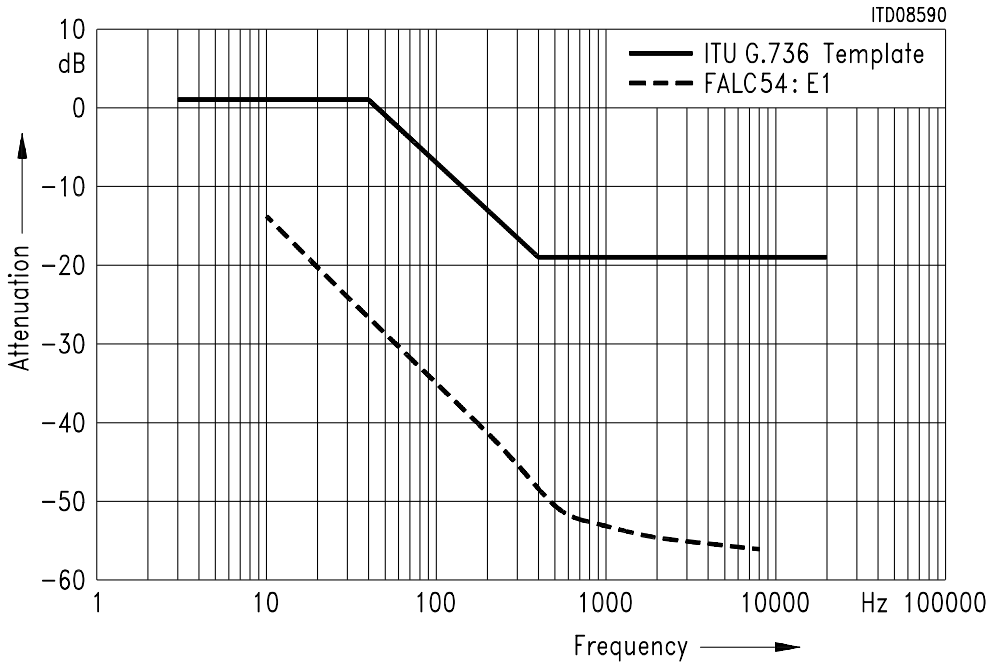


Figure 11
Jitter Attenuation Performance

Also the requirements of ETSI TBR12/13 will be satisfied. Insuring adequate margin against TBR12/13 output jitter limit with 15 UI input at 20 Hz the FALC54 will start jitter attenuation at nearly 2 Hz.

Jitter Tolerance

The FALC54 receiver's tolerance to input jitter complies to ITU for CEPT application.

Figure 12 shows the curves of different input jitter specifications stated above as well as the FALC54 performance.

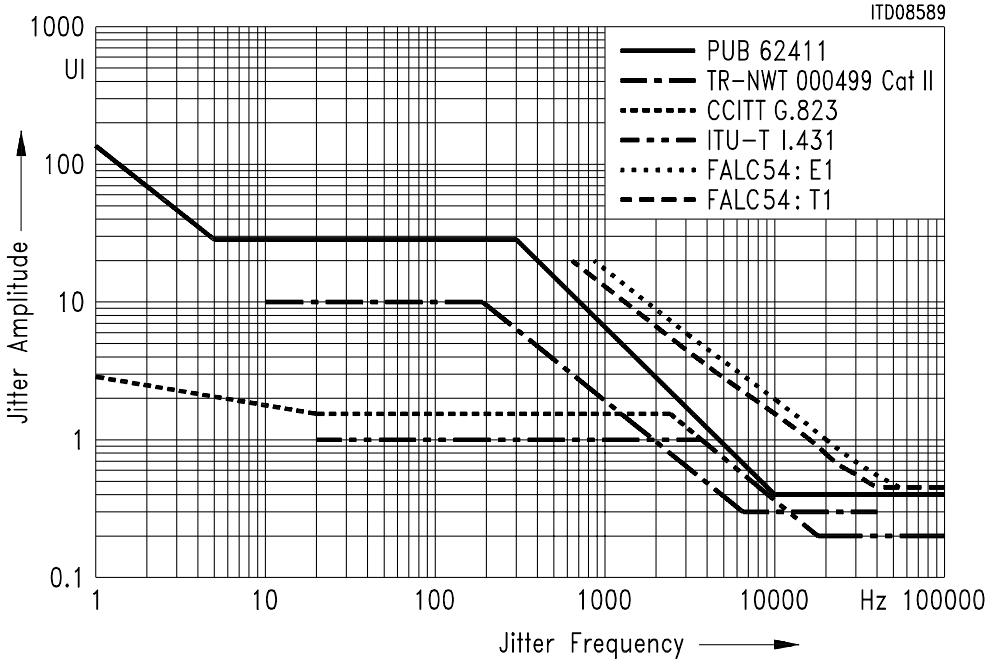


Figure 12
Jitter Tolerance

Output Jitter

In the absence of any input jitter the FALC54 generates the output jitter, which is specified in table below.

Specification	Measurement Filter Bandwidth		Output Jitter (UI peak to peak)
	Lower Cutoff	Upper Cutoff	
I.431	20 Hz	100 kHz	< 0.015
	700 Hz	100 kHz	< 0.015

Clock Generation and Clock Modes

The high performance integrated Clock Generator meets the recommendations of ITU-T G.735, G824 and I.431 in case of input jitter tolerance, jitter transfer characteristic and output jitter. The following table shows the clock modes with the corresponding synchronization sources.

Mode	Internal LOS Active	SYNC Input	System Clocks
Master	no	GND	Free Running (oscillator centered)
Master	no	2 MHz	Synchronized on SYNC input (external 2 MHz)
Slave	no	GND	Synchronized on Line (RCLK)
Slave	no	2 MHz	Synchronized on Line (RCLK)
Slave	yes	GND	Free Running (oscillator centered)
Slave	yes	2 MHz	Synchronized on SYNC input (external 2 MHz)

The clock generator unit fulfills two main tasks. One is, to provide jitter free system clocks either derived from the line or from an external input. The other task is either smoothing the SCLKX input in ATM, SONET or SDH applications (Xslicer mode) or to ensure output jitter characteristics in case jittered SCLKX clock.

The system clocks are provided by the DCO1 (16 M, 8 M, 4/2 M, 8 k). The recovered route clock is directly forwarded to the PLL circuit (in Slave Mode).

The main task of DCO2 is to generate a jitter free transmit clock if the Xslicer function is enabled. In this case a 16.384 MHz crystal has to be connected to pins XTAL3/4.

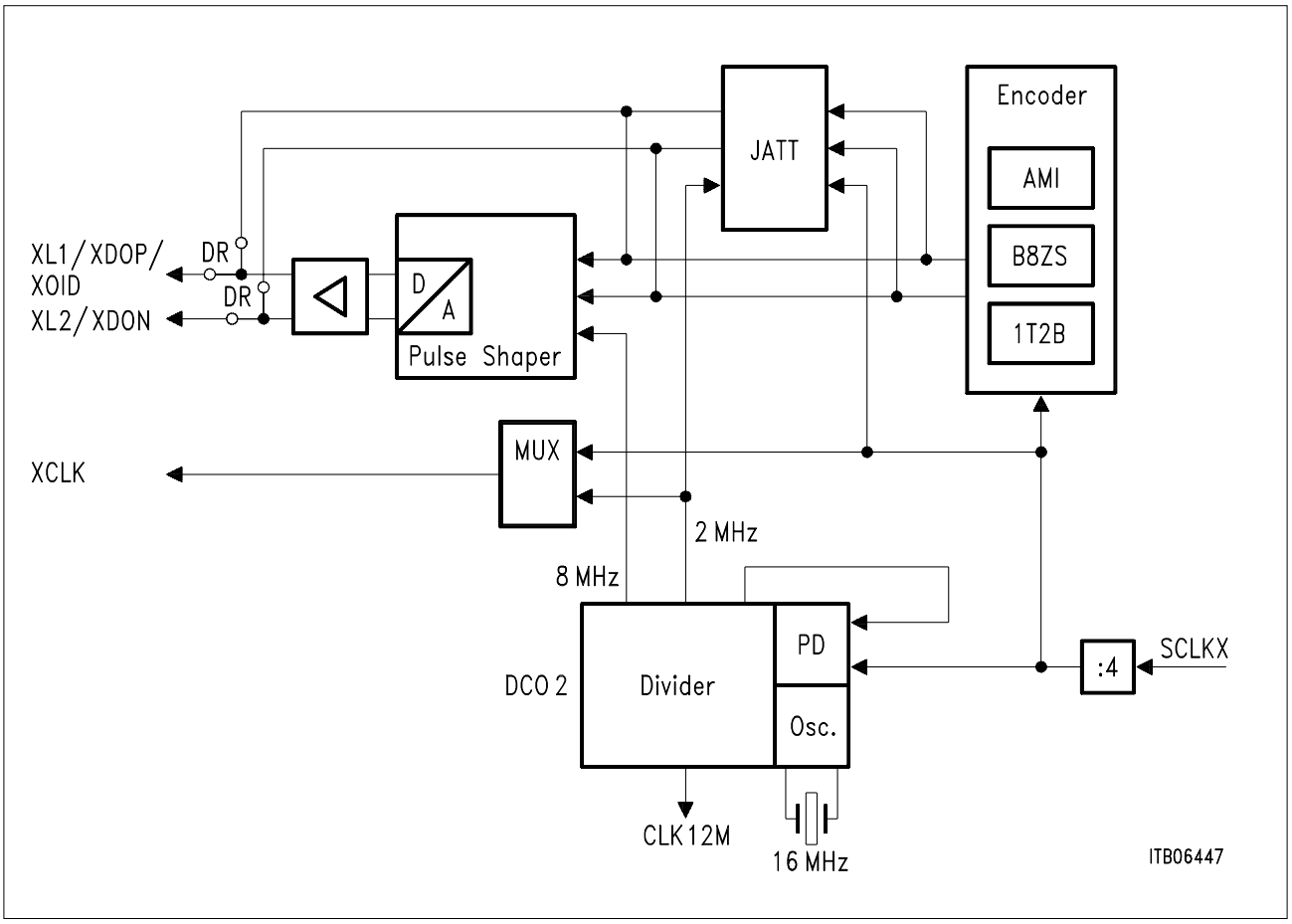


Figure 13
Transmit Clock System

Framer/Synchronizer

The following functions are performed:

- Synchronization on pulse frame
- Synchronization on multiframe
- Error indication when synchronization is lost. In this case, AIS is automatically sent to the system side and Remote Alarm to the remote end if en/disabled.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This may be automatically done by the FALC54, or user controlled via the microprocessor interface.
- Detection of remote alarm indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in special status registers.
- Generation of various interrupt statuses of the receiver functions. These interrupts can be masked.
- Generation of control signals to synchronize the CRC checker, and the receive elastic store write control unit.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC submultiframe according to the CRC 4 procedure (**refer to ITU-T Rec. G704**). These bits are compared with those check bits that are received during the next CRC submultiframe. If there is at least one mismatch, the CRC error counter (16 bit) will be incremented.

Receive Elastic Store

The received bit stream is stored in the receive elastic store. The memory is organized as a two-frame elastic buffer with a size of 64 $\times$ 8 bit.

The functions are:

- Clock adaption between system clock (SCLKR) and internally generated route clock (RCLK).
- Compensation of input wander and jitter. Maximum of wander amplitude (peak-to-peak):
  190 UI (1 UI = 488 ns)
- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel, channel-serial data which is circularly written to the elastic store using internally generated Receive Route Clock (RCLK).

Reading of stored data is controlled by the System Clock (SCLKR) and the Synchronous Pulse ($\overline{\text{SYPR}}$) in conjunction with the programmed offset values for the receive time-slot/clock-slot counters. After conversion into a serial data stream, the data is given out via port RDO.

Two bit rates (2048/4096 kbit/s) are selectable via the microprocessor interface.
In 4096 kbit/s interface mode each channel will be sent out on two different channel-phases. Each channel-phase which should be tri-stated is programmable.

Figure 14 gives an idea of operation of the receive elastic store:
A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the write pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (the next received frame is skipped) or a positive slip (the previous received frame is read out twice) is performed at the system interface, depending on the difference between RCLK and SCLKR/4, i.e. on the position of pointer R and W within the memory.

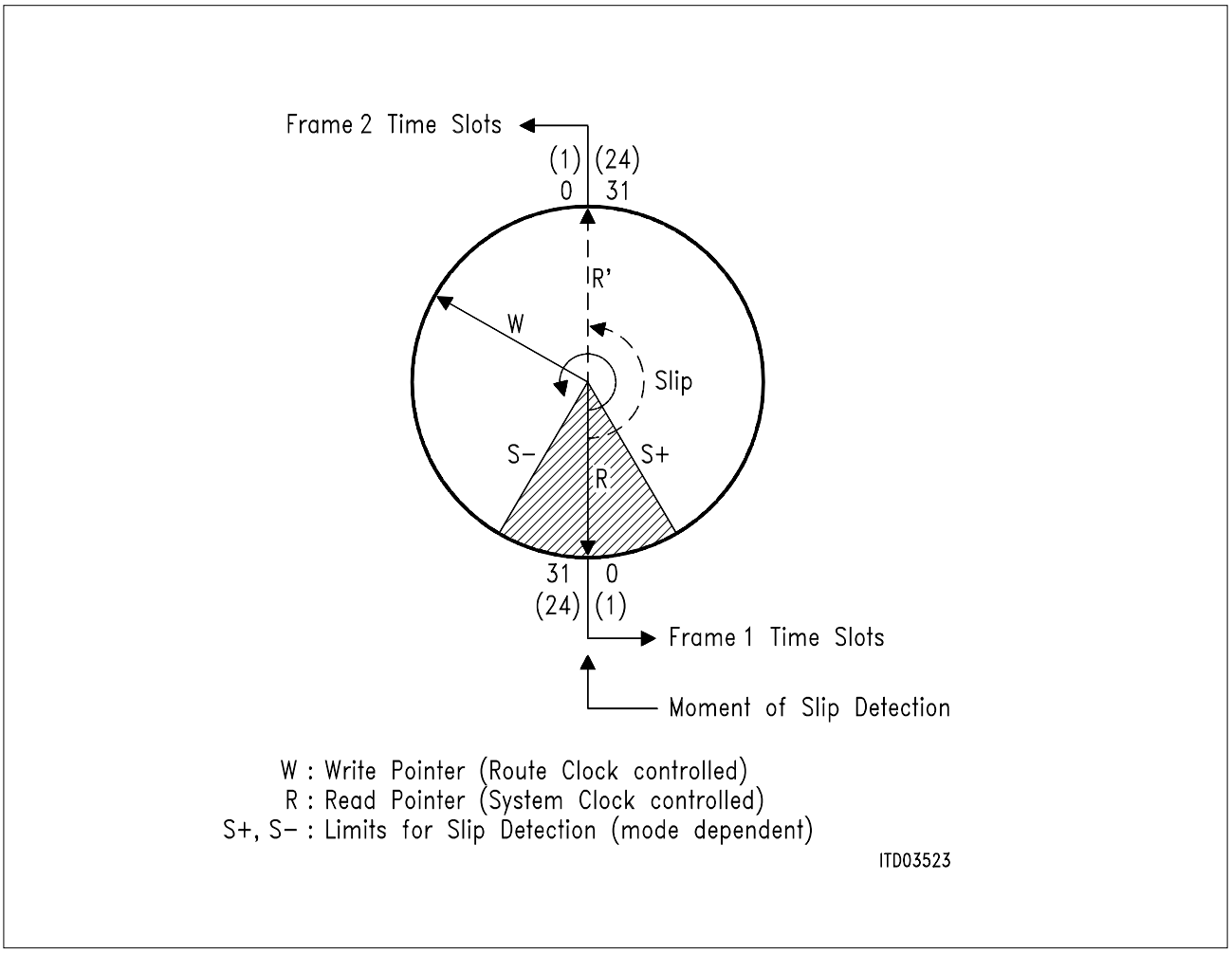


Figure 14
The Receive Elastic Store as Circularly Organized Memory

Additionally the receive elastic store can be switched to one frame length (LOOP.SFM). This feature is useful for master-slave applications to reduce the delay between line interface and system interface. For correct operation, System Clock SCLKR has to be connected to pin CLK8M and Synchronous Pulse $\overline{\text{SYPR}}$ has to be connected to the pin $\overline{\text{FSC}}$ of the FALC54. In single frame mode, however, it is not possible to perform a slip after the slip condition has been detected. Thus, values of receive time-slot/clock-slot offset (RC0, RC1) have to be specified great enough to prevent too great approach of frame begin (line side) and frame begin (system side).

Receive Signaling Controller

The receive signaling controller can be programmed to operate in various signaling modes. The FALC54 will perform the following signaling and data link methods:

- Message Oriented Signaling also called Common Channel Signaling CCS
- Channel Associated Signaling CAS

The signaling information is carried in time-slot 16 (TS16).

The signaling controller samples the bit stream which is output on pin RDO.

In case of channel associated signaling data is sampled on the receive line side clocked with the extracted receive route clock and stored in registers RS1-16. The signaling procedure will be done as it is described in ITU-T G.704 and G.732.

The main functions are:

- Synchronization to a CAS multiframe
- Detection of AIS and Remote Alarm in CAS multiframes
- Separation of CAS Service bits X1-X3
- Storing of received signaling data in registers RS1-16.

Updating of the received signaling information is inhibited if the TS0 or TS16 multiframe alignment is lost.

In case of common channel signaling the signaling procedure HDLC/SDLC will be supported. The received data flow and the address recognition features can be performed in very flexible way, to satisfy almost any practical requirements. Depending on the selected address mode, the FALC54 can perform a 1 or 2 byte address recognition. All frames with valid addresses are forwarded directly via the Receive FIFO (RFIFO) to the system memory. The HDLC control-field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. The HDLC control-field and additional information can also be read from special registers.

In extended transparent mode, fully transparent data reception without HDLC framing is performed, i.e. without FLAG recognition, CRC checking or bit-stuffing. This allows the user specific protocol variations. The received data are stored in the RFIFO.

The FALC54 offers the flexibility to extract data during certain time-slots which are defined via registers RTR1-4 or to extract the S_a bits enabled via XC0.SA8E-4E. Any combination of time-slots or S_a bits can be programmed.

2.1.2 Transmit Path

The inverse functions are performed for the transmit direction.

The PCM data is received from the system internal highway at port XDI with 2048 kbit/s or 4096 kbit/s. The channel assignment is equivalent to the receive direction.

The contents of selectable channels (time-slots) can be overwritten by the pattern defined via register IDLE. The selection of “idle channels” is done by programming the four-byte registers ICB1 … ICB4.

Latching of data is controlled by the System Clock (SCLKX) and the Synchronous Pulse ($\overline{\text{SYPX}}$) in conjunction with the programmed offset values for the Transmit Time-slot/Clock-slot Counters.

The clock for the transmit data is internal derived directly from the system clock (SCLKX). Consequently, the data received from the system interface is switched through.

Transmit Signaling Controller

Similar to the receive signaling controller the same signaling methods and the same time-slot assignment are provided. The signaling information has to be written in the Transmit FIFO (XFIFO). With a Transmit Frame command the signaling information will be sent in the corresponding time-slots. The signaling will be internally multiplexed with the data at port XDI.

If the extended transparent mode is selected, the FALC54 supports the continuous transmission of the contents of the XFIFO. The cyclic transmission continuous until the Transmitter Reset command (CMDR.SRES) is issued or CMDR.XREP is reset.

In case of channel associated signaling the complete CAS multiframe have to be written to the XS1-16 registers. The contents of these registers will be sent in TS16.

In case of CCS the signaling procedure HDLC/SDLC is supported with generation of Preambles and FLAGs, CRC generation and bit-stuffing.

In transmit direction the FALC54 offers the flexibility to insert data during certain time-slots which are defined via registers TTR1-4 or to insert the S_a bits enabled via XC0.SA8E-4E. Any combination of time-slots bits can be programmed independent for the receive and transmit direction.

If the FALC54 is optioned for no signaling, the channels in the data stream from the system interface will pass the FALC54 undisturbed.

Transmitter

The serial bit stream is then processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the two selectable framing formats
- Insertion of service and data link information
- AIS generation (Alarm indication signal)
- Remote alarm generation
- Auxiliary pattern generation
- CRC generation and insertion of CRC bits
  CRC bits inversion in case of a previously received CRC error

The multiframe boundries of the transmitter may be externally synchronized by using the XMFS pin. This feature is required if signaling- and service- bits are routed through the switching network and are inserted in transmit direction via the system interface.

Transmit Line Interface

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided by the digital transmitter.

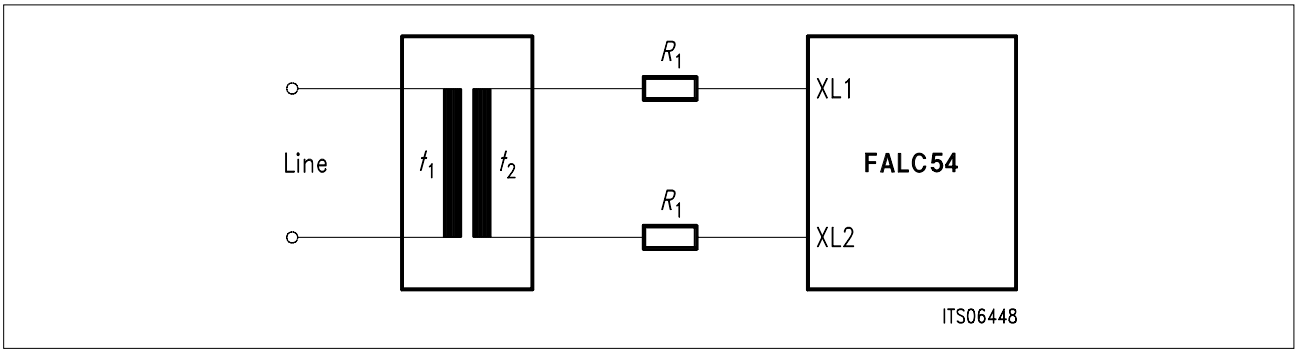


Figure 15
Transmitter Configuration

Recommended Transmitter Configuration Values

Parameter	Characteristic Impedance [Ω]	
	120	**75**
R_1 (± 2.5 %) [Ω]	18	18
$t_2 : t_1$	$1 : \sqrt{2}$	$1 : \sqrt{2}$

Similar to the receive line interface three different data types are supported:

- Ternary Signal
  Single rail data is converted into a ternary signal which is output on pins XL1 and XL2. The HDB3 and AMI line code is employed. Selected by FMR0.XC1/0 and LIM1.DRS = 0.
- Dual rail data PCM(+), PCM(–) at multifunction ports XDOP/ XDON with 50 % or 100 % duty cycle and with programmable polarity. Line coding is done in the same way as in the ternary interface. Selected by FMR0.XC1/0 and LIM1.DRS = 1.
- Unipolar data at port XOID will be transmitted either in NRZ (Non Return to Zero) with 100 % duty cycle or in CMI (Code Mark Inversion or known as 1T2B) Code with or without (FMR3.CMI) preprocessed HDB3 coding to a fibre optical interface. Clocking off data is done with the rising edge of the transmit clock XCLK (2048 kHz) and with a programmable polarity. Selection is done by FMR0.XC1 = 0 and LIM1.DRS = 1.

The analog transmitter includes a programmable pulse shaper to satisfy the requirements of ITU-T I.431. The amplitude of pulse shaper is programmable via the microprocessor interface to allow a maximum of different pulse templates.

The transmitter requires an external step up transformer to drive the line.

Transmit Line Monitor

The transmit line monitor compares the transmit line pulses on XL1 and XL2 with the transmit input signals received on pins XL1M and XL2M. The monitor detects faults on the primary side of the transformer and protects the device from damage by setting the transmit line driver XL1/2 automatically in a high impedance state. Faults on the secondary side may not be detected. To detect a short the configuration in **figure 15** and the reset values of register XPM0-2 has to be fulfilled. Otherwise the short detection could not be guaranteed. Two conditions will be detected by the monitor: Transmit Line ones density (more than 31 consecutive zeroes) and Transmit Line Shorted. In both cases a transmit line monitor status change interrupt will be provided.

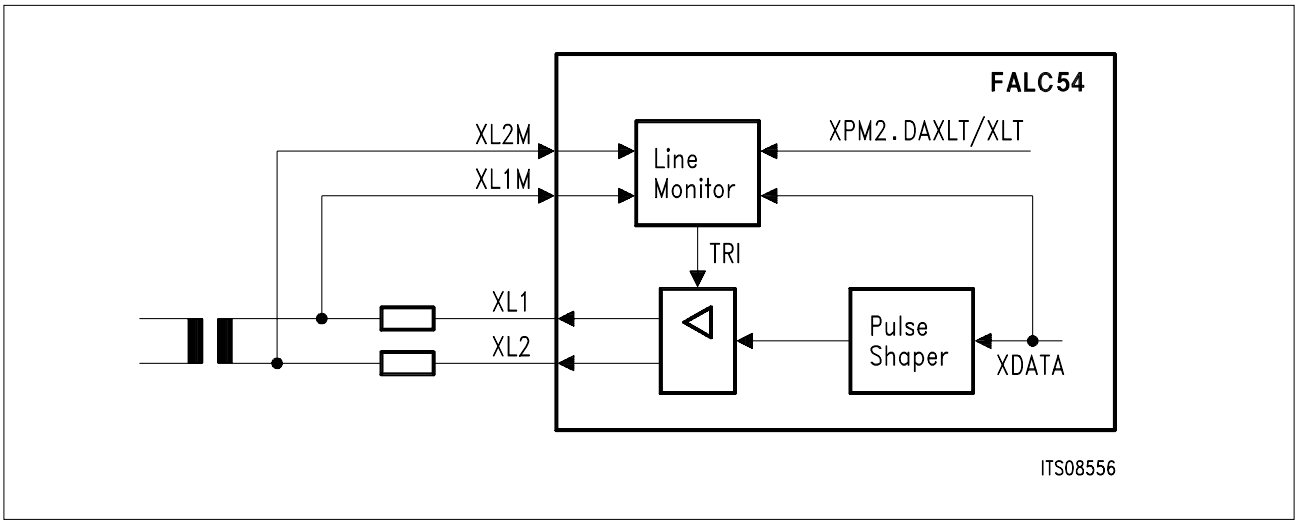


Figure 16
Transmit Line Monitor Configuration

2.1.3 Additional Functions

Idle Code Insertion

In transmit direction, the contents of selectable channels can be overwritten by the pattern defined via register IDLE. The selection of “idle channels” is done by programming the four-byte registers ICB1 … ICB4.

Transparent Mode

The described transparent modes are useful for loopbacks or for routing signaling information through the system interface.

In receive direction, transparency for ternary or dual / single rail unipolar data is always achieved if the receiver is in the synchronous state. In asynchronous state the data can be transparently switched through if bit FMR2.DAIS and bit FMR2.RTM are set. However, correct time-slot assignment can not be guaranteed due missing frame alignment between line and system side.

Transparency in transmit direction can be achieved by activating the time-slot 0 transparent mode (bit XSP.TT0 or TSWM.7-0). If XSP.TT0 = 1 all internal information of the FALC54 (framing, CRC, Sa/Si bit signaling, remote alarm) will be ignored. With register TSWM the Si-bits, A-bit or the Sa4-8 bits could be selectively enabled to send data transparent from port XDI to the far end. Only HDB3 data encoding is still provided. For complete transparency the internal signaling controller and Payload Loop Back has to be disabled.

System Clocks and System Pulses for Transmitter and Receiver

The FALC54 offers a flexible feature for system designers where different system clocks and system pulses are necessary. The interface to the receive system highway will be clocked via pin SCLKR, while the interface to the transmit system highway is clocked via pin SCLKX. The frequency on pin SCLKR/X must fixed 8.192 MHz.

The signals on pin $\overline{\text{SYPR}}$ in conjunction with the assigned timeslot offset in register RC0 and RC1 will define the beginning of a frame on the receive system highway.The signal on pin $\overline{\text{SYPX}}$ in conjunction with the assigned timeslot offset in register XC0 and XC1 will define the beginning of a frame on the transmit system highway.

Error Performance Monitoring

The FALC54 supports the error performance monitoring by detecting following alarms in the received data.

- Framing errors
- CRC errors
- Code violations
- Loss of frame alignment
- Loss of signal
- Alarm indication signal
- E bit error
- Slip

With a programmable interrupt mask (register IMR4) all these error events could generate an Errored Second interrupt (ES) if enabled. Additionally a one Second interrupt could be generated to indicate that the ES interrupt has to be read. If the ES interrupt is set the enabled alarm status bits or the error counters have to be examined.

Automatic Remote Alarm Access

If the receiver has lost its synchronization a remote alarm could be sent if enabled via bit FMR2.AXRA to the distant end. The remote alarm bit will be automatically set in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit will be removed.

2.1.4 Operating Modes E1

General

Bit: FMR1.PMOD = 0

PCM line bit rate : 2048 kbit/s
Single frame length : 256 bit, No. 1 … 256
Framing frequency : 8 kHz
HDLC controller :
Organization : 32 time-slots, No. 0 … 31
with 8 bits each, No. 1 … 8

The operating mode of the FALC54 is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme.

The FALC54 implements all of the standard and/or common framing structures for PCM 30 (CEPT, 2048 kbit/s) carriers. These are summarized in **table 4**, along with the signaling types applicable in each of the multiframe formats. “General signaling” refers to the support the FALC54 provides for handling the service bits, as the case may be, in the multiframe.

Table 4
Summary of FALC54 Framing and Supported Signaling Modes

	Double-Frame	**CRC-Multi-Frame**
CRC	**–**	**CRC4**
Signaling		
CCS	e.g. TS16	e.g. TS16
CAS-CC	e.g. TS16	e.g. TS16
CAS-BR	–	–
General Signaling	S bits	S bits

CCS = Common Channel Signaling
CAS-CC = Channel Associated Signaling (Common Channel)

For CCS and CAS-CC, different types of support are provided.

Note: The internal HDLC- or CAS Controller supports all signaling procedures like signaling frame synchronization / synthesis and signaling alarm detection.

The next pages give a general description of the assigned framing formats. After RESET, the FALC54 is switched into doubleframe format automatically.

Time-slot 0 is reserved for frame alignment word and service information. Switching between the two applicable framing formats (doubleframe/CRC-multiframe) is done via bit FMR2.RFS1/0 for the receiver and FMR1.XFS for the transmitter.

Line Interfacing

- Dual rail data with AMI or HDB3 coding in conjunction with double violation detection or extended code violation detection (FMR0.EXTD). Errors can be counted by the Code Violation Counter CVC with 16 bit length.
- Single rail unipolar data (FMR0.XC1/0) with NRZ or CMI Code.
- General Alarms
- AIS: Detection is flagged by bit FRS0.AIS. Transmission is enabled via bit FMR1.XAIS.
- LOS: Detection is flagged by bit FRS0.LOS.
- RAI: Remote Alarm Indication is flagged by bit FRS0.RRA and RSW.RRA. Transmission is enabled via bit XSW.XRA.
- AUXP: Detection is flagged by bit FRS1.AUXP. Transmission is enabled via bit XSP.XAP.

Channel Assignment

The channel (time-slot) assignment from the PCM line to the system internal highway is performed without any changes of channel numbering (TS0 $\leftrightarrow$ TS0, … , TS31 $\leftrightarrow$ TS31). In receive direction, the contents of time-slot 0 are switched through transparently. In transmit direction, contents of time-slot 0 of the outgoing PCM frame are normally generated by the FALC54. Additionally, one transparent mode (XSP.TT0) can be selected to achieve transparency for the complete time-slot 0. With the Transparent Service Word Mask register (TSWM) the Si-bits, A-bit and the SA4-8 bits could be selectively switched through transparently.

General Signaling

- S_a bits in accordance with ITU-T G.704 and ETS 300233.
- E bits in accordance with ITU-T G.704 and ETS 300233.

Signaling

- CCS
  For Common Channel Signaling the use of time-slot 16 is recommended. The use of CCS is allowed with both the doubleframe and the CRC-multiframe format.
- CAS-CC
  For Channel Associated Signaling the use of time-slot 16 is recommended. The autonomous CAS multiframe structure is not related to a doubleframe or a CRC-multiframe structure (refer to **ITU-T G.704**).
  The FALC54 support CAS multiframe synchronization and synthesis.

2.1.4.1 Doubleframe Format

The framing structure is defined by the contents of time-slot 0 (refer to **table 5**).

Table 5
Allocation of Bits 1 to 8 of Time-Slot 0

Alternate Frames / Bit Number	1	2	3	4	5	6	7	8
Frame Containing the Frame Alignment Signal	S_i	0	0	1	1	0	1	1
	Note 1	Frame Alignment Signal						
Frame not Containing the Frame Alignment Signal	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	Note 1	Note 2	Note 3	Note 4				

Note:

1. *S_i bits: reserved for international use. If not used, these bits should be fixed to '1'. Access to received information via bits RSW.RSI and RSP.RSIF. Transmission is enabled via bits XSW.XSIS and XSP.XSIF.*
2. *Fixed to '1'. Used for synchronization.*
3. *Remote alarm indication: In undisturbed operation '0'; in alarm condition '1'.*
4. *S_a bits: Reserved for national use. If not used, they should be fixed at '1'. Access to received information via bits RSW.RY0 … RY4. Transmission is enabled via bits XSW.XY0 … XY4. HDLC-signaling in bits Sa4- Sa8 is selectable. (*)*

Note: (*) As a special extension for double frame format, the S_a -bit registers RSA4-8 / XSA4-8 may be used optionally.

For transmit direction, contents of time-slot 0 are additionally determined by the selected transparent mode:

	Transparent Source for			
Mode	**Framing**	**A Bit**	**S_a Bits**	**S_i Bits**
–	(int. generated)	XSW.XRA[1)]	XSW.XY0 … 4[2)]	XSW.XSIS, XSP.XSIF
XSP.TT0	via pin XDI	via pin XDI	via pin XDI	via pin XDI
TSWM.TSIF	(int. generated)	XSW.XRA	XSW.XY0 … 4	via pin XDI
TSWM.TSIS	(int. generated)	XSW.XRA	XSW.XY0 … 4	via pin XDI
TSWM.TRA	(int. generated)	via pin XDI	XSW.XY0 … 4	XSW.XSIS, XSP.XSIF
TSWM.TSA4-8	(int. generated)	XSW.XRA	via pin XDI	XSW.XSIS, XSP.XSIF

1) Additionally, automatic transmission of the A-bit is selectable

2) As a special extension for double frame format, the Sa-bit register may be used optionally.

Synchronization Procedure

Synchronization status is reported via bit FRS0.LFA. Framing errors are counted by the Framing Error Counter (FEC). Asynchronous state is reached after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (bit 2 = 0 in time-slot 0 of every other frame not containing the frame alignment word), the selection is done via bit RC1.ASY4. Additionally, the service word condition can be disabled. When the framer lost its synchronization an interrupt status bit ISR2.LFA is generated.

In asynchronous state, counting of framing errors will be stopped and AIS is automatically sent to the system internal highway (can be disabled via bit FMR2.DAIS).

The resynchronization procedure starts automatically after reaching the asynchronous state. Additionally, it may be invoked user controlled via bit: FMR0.FRS (Force Resynchronization: the FAS word detection is interrupted. In connection with the above conditions this will lead to asynchronous state. After that, resynchronization starts automatically).

Synchronous state is established after detecting:

– a correct FAS word in frame n,
– the presence of the correct service word (bit 2 = 1) in frame n + 1,
– a correct FAS word in frame n + 2.

If the service word in frame n + 1 or the FAS word in frame n + 2 or both are not found searching for the next FAS word will be start in frame n + 2 just after the previous frame alignment signal.

Reaching the synchronous state causes a frame alignment recovery interrupt status ISR2.FAR if enabled. Undisturbed operation starts with the beginning of the next doubleframe.

A-Bit Access

If the FALC54 detects a remote alarm indication in the received data stream the interrupt status bit ISR2.RA will be set.

By setting FMR2.AXRA the FALC54 automatically transmit the remote alarm bit = 1 in the outgoing data stream if the receiver detects a loss of frame alignment FRS0.LFA = 1. If the receiver is in synchronous state FRS0.LFA = 0 the remote alarm bit will be reset.

Note: The A-bit may be processed via the system interface. Setting bit TSWM.TRA enables transparency for the A bit in transmit direction (refer to **table 6**).

S_a - Bit Access

As an extension for access to the S_a-bits via registers RSA4-8/XSA4-8 an option is implemented to allow the usage of internal S_a-bit registers RSA4-8/XSA4-8 in doubleframe format.

This function is enabled by setting FMR1.ENSA = 1 for the transmitter and FMR1.RFS1/0 = 01 for the receiver. The FALC54 works then internally with a 16-frame structure but no CRC multiframe alignment/generation is performed. For more details refer to **chapter 2.1.4.2**.

2.1.4.2 CRC-Multiframe

The multiframe structure shown in **table 6** is enabled by setting bit: FMR1.RFS1 for the receiver and FMR1.XFS for the transmitter.

Multiframe	:	2 submultiframes = 2 × 8 frames
Frame alignment	:	refer to section Doubleframe Format
Multiframe alignment	:	bit 1 of frames 1, 3, 5, 7, 9, 11 with the pattern ‘001011’
CRC bits	:	bit 1 of frames 0, 2, 4, 6, 8, 10, 12, 14
CRC block size	:	2048 bit (length of a submultiframe)
CRC procedure	:	CRC4, according to ITU-T Rec. G.704, G.706

Table 6
CRC-Multiframe Structure

	Sub-Multiframe	Frame Number	Bits 1 to 8 of the Frame							
			1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Multiframe	I	0	C_1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a61}	S_{a7}	S_{a8}
		2	C_2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a62}	S_{a7}	S_{a8}
		4	C_3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a63}	S_{a7}	S_{a8}
		6	C_4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a64}	S_{a7}	S_{a8}
	II	8	C_1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a61}	S_{a7}	S_{a8}
		10	C_2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a62}	S_{a7}	S_{a8}
		12	C_3	0	0	1	1	0	1	1
		13	E*	1	A	S_{a4}	S_{a5}	S_{a63}	S_{a7}	S_{a8}
		14	C_4	0	0	1	1	0	1	1
		15	E*	1	A	S_{a4}	S_{a5}	S_{a64}	S_{a7}	S_{a8}

E: Spare bits for international use. Access to received information via bits RSP.RS13 and RSP.RS15. Transmission is enabled via bits XSP.XS13 and XSP.XS15. Additionally, automatic transmission for submultiframe error indication is selectable.

S_a: Spare bits for national use. Additionally, Sa bit access via registers RSA4 … 8 and XSA4 … 8 is provided. HDLC-signaling in bits Sa4- Sa8 is selectable.

C_1 … C_4: Cyclic redundancy check bits.

A: Remote alarm indication. Additionally, automatic transmission of the A-bit is selectable.

For transmit direction, contents of time-slot 0 are additionally determined by the selected transparent mode:

	Transparent Source for			
Mode	**Framing + CRC**	**A Bit**	**Sa Bits**	**E Bits**
–	(int. generated)	XSW.XRA[1)]	XSW.XY0 … 4[2)]	XSP.XS13/XS15[3)]
XSP.TT0	via pin XDI	via pin XDI	via pin XDI	via pin XDI
TSWM.TSIF	(int. generated)	XSW.XRA[1)]	XSW.XY0 … 4[2)]	(int. generated)
TSWM.TSIS	(int. generated)	XSW.XRA[1)]	XSW.XY0 … 4[2)]	via pin XDI
TSWM.TRA	(int. generated)	via pin XDI	XSW.XY0 … 4[2)]	XSP.XS13/XS15[3)]
TSWM.TSA4–8	(int. generated)	XSW.XRA[1)]	via pin XDI	XSP.XS13/XS15[3)]

[1)] Automatic transmission of the A-bit is selectable

[2)] The S_a-bit register XSA4-8 may be used optionally

[3)] Additionally, automatic transmission of submultiframe error indication is selectable

The CRC procedure is automatically invoked when the multiframe structure is enabled. CRC errors in the received data stream are counted by the 16 bit CRC Error Counter CEC (one error per submultiframe, maximum).

Additionally a CRC4 error interrupt status ISR0.CRC4 can be generated if enabled via IMR0.CRC4.

All CRC bits of one outgoing submultiframe are automatically inverted in case a CRC error is flagged for the previous received submultiframe. This function is enabled via bit RC0.CRCI. Setting the bit RC0.XCRCI will invert the CRC bits before transmission to the distant end. The function of RC0.XCRCI and RC0.CRCI are logically ored.

Synchronization Procedure

Multiframe alignment is assumed to have been lost if doubleframe alignment has been lost (flagged at status bits FRS0.LFA and FRS0.LMFA). The rising edge of these bits will cause an interrupt status bits ISR2.LFA + ISR2.LMFA.

The multiframe resynchronization procedure starts when Doubleframe alignment has been regained which is indicated by an interrupt status bit ISR2.FAR. For Doubleframe synchronization refer to section Doubleframe Format. It may also be invoked by the user by setting

– bit FMR0.FRS for complete Doubleframe **and** multiframe re-synchronization
– bit FMR1.MFCS for multiframe re-synchronization only.

The CRC checking mechanism will be enabled after the first correct multiframe pattern has been found. However, CRC errors will not be counted in asynchronous state.

The multiframe synchronous state is established after detecting two correct multiframe alignment signals at an interval of n × 2 ms (n = 1, 2, 3 …). The Loss of multiframe alignment flag FRS0.LMFA will be reset. Additionally an interrupt status multiframe alignment recovery bit ISR2.MFAR is generated with the falling edge of bit FRS0.LMFA.

Automatic Force Resynchronization

In addition, a search for Doubleframe alignment is automatically initiated if two multiframe pattern with a distance of n × 2 ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained (bit FMR1.AFR). The research for frame alignment will be started just after the previous frame alignment signal.

Floating Multiframe Alignment Window

After reaching doubleframe synchronization a 8 ms timer is started. If a multiframe alignment signal is found during the 8 ms time interval the internal timer will be reset to remaining 6 ms in order to find the next multiframe signal within this time. If the multiframe signal is not found for a second time an interrupt status ISR0. T8MS will be provided. This interrupt will usually occur every 8 ms until multiframe synchronization is achieved.

CRC4 Performance Monitoring

In the synchronous state checking of multiframe pattern is disabled. However, with bit FMR2.ALMF an automatic multiframe resynchronization mode can be activated. If 915 out of 1000 errored CRC submultiframes are found then a false frame alignment will be assumed and a search for double- and multiframe pattern is initiated. The new search for frame alignment will be started just after the previous basic frame alignment signal. The internal CRC4 resynchronization counter will be reset when the multiframe synchronization has been regained.

Modified CRC4 Multiframe Alignment Algorithm

The modified CRC4 multiframe alignment algorithm allows an automatic interworking between framers with and without a CRC4 capability. The interworking is realized as it is described in ITU-T G.706 Appendix B.

If doubleframe synchronization is consistently present but CRC4 multiframe alignment is not achieved within 400 ms it is assumed that the distant end is initialized to doubleframe format. The CRC4 - Non CRC4 interworking is enabled via FMR2.RFS1/0 = 11 and is activated only if the receiver has lost its synchronization. If doubleframe alignment (basic frame alignment) is established a 400 ms timer and searching for multiframe alignment will be started. A research for basic frame alignment will be initiated if the CRC4 multiframe synchronization could not be achieved within 8 ms and will be started just after the previous frame alignment signal. The research of the basic frame alignment is done in parallel and is independent of the synchronization procedure of the primary basic

frame alignment signal. During the parallel search all receiver functions are based on the primary frame alignment signal, like framing errors, Sa-, Si-, A-bits …). All subsequent multiframe searches are associated with each basic framing sequence found during the parallel search.

If the CRC4 multiframe alignment sequence was not found within the time interval of 400 ms, the receiver will be switched into a Non CRC4 mode indicated by setting the bit FRS0.NMF (No Multiframing Found) and ISR2.T400MS. In this mode checking of CRC bits is disabled and the received E-bits are forced to low. The transmitter framing format will not be changed. Even if multiple basic FAS resynchronizations have been established during the parallel search, the receiver will be maintained to the initially determined primary frame alignment signal location.

However, if the CRC4 multiframe alignment could be achieved within the 400 ms time interval assuming a CRC4 to CRC4 interworking, then the basic frame alignment sequence associated to the CRC4 multiframe alignment signal will be chosen. If necessary, the primary frame alignment signal location will be adjusted according to the multiframe alignment signal. The CRC4 performance monitoring will be started if enabled via FMR2.ALMF and the received E-bits will be processed in accordance with ITU-T G.704.

Switching into the doubleframe format (non CRC4) mode after 400 msec can be disabled by setting of FMR3.EXTIW. In this mode the FALC54 still searches the multiframing further on.

A-Bit Access

If the FALC54 detects a remote alarm indication (bit 2 in TS0 not containing the FAS word) in the received data stream the interrupt status bit ISR2.RA will be set. With the deactivation of the remote alarm the interrupt status bit ISR2.RAR is generated.

By setting FMR2.AXRA the FALC54 automatically transmits the remote alarm bit = 1 in the outgoing data stream if the receiver detects a loss of frame alignment (FRS0.LFA = 1). If the receiver is in synchronous state (FRS0.LFA = 0) the remote alarm bit will be reset in the outgoing data stream.

Additionally, if bit FMR3.EXTIW is set and the multiframesynchronous state could not be achieved within the 400 msec after finding the primary basic framing, the A-bit will be transmitted active high to the remote end until the multiframing is found.

*Note: The A-bit may be processed via the system interface. Setting bit TSWM.TRA enables transparency for the A bit in transmit direction (refer to **table 6**).*

S_a - Bit Access

Due to signaling procedures using the five S_a bits (S_{a4} … S_{a8}) of every other frame of the CRC multiframe structure, three possibilities of access via the microprocessor are implemented.

- The standard procedure allows reading/writing the S_a-bit registers RSW, XSW without further support. The S_a-bit information will be updated every other frame.
- The advanced procedure, enabled via bit FMR1.ENSA, allows reading/writing the S_a-bit registers RSA4 … 8, XSA4 … 8.

  A transmit or receive multiframe begin interrupt (ISR0.RMB or ISR1.XMB) is provided.

  Registers RSA4-8 contains the service word information of the previously received CRC-multiframe or 8 doubleframes (bitslots 4-8 of every service word). These registers will be updated with every multiframe begin interrupt ISR0.RMB.

  With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of this registers XSA4-8 will be copied into shadow registers. The contents will subsequently sent out in the service words of the next outgoing CRC multiframe (or doubleframes) if none of the time-slot 0 transparent modes is enabled. The transmit multiframe begin interrupt XMB request that these registers should be serviced. If requests for new information will be ignored, current contents will be repeated.
- The extended access via the receive and transmit FIFOs of the signaling controller. In this mode it is possible to transmit / receive a HDLC frame or a transparent bit stream in any combination of the S_a bits. Enabling is done by setting of bit CCR1.EITS and the corresponding bits XC0.SA8E-4E / TSWM.TSA8-4 and resetting of registers TTR1-4, RTR1-4 and FMR1.ENSA. The access to and from the FIFOs is supported by ISR0.RME,RPF and ISR1.XPR,ALS.

SA6-Bit Detection according to ETS 300233

Four consecutive received SA6-bits are checked on the by ETS 300233 defined SA6-bit combinations. The FALC54 will detect following fixed SA6-bit combinations: SA61,SA62,SA63,SA64 = 1000; 1010; 1100; 1110; 1111. All other possible 4 bit combinations are grouped to status “X”.

A valid SA6-bit combination must occur three times in a row. The corresponding status bit in register RSA6S will be set. Register RSA6S is from type “Clear on Read”. With any change of state of the SA6-bit combinations an interrupt status ISR0.SA6SC will be generated.

During the basicframe asynchronous state updating of register RSA6S and interrupt status ISR0.SA6SC is disabled. In multiframe format the detection of the SA6-bit combinations can be done either synchronous or asynchronous to the submultiframe (FMR3.SA6SY). In synchronous detection mode updating of register RSA6S is done in the multiframe synch. state (FRS0.LMFA=0). In asynchr. detection mode updating is independent to the multiframe synchronous state.

Sa6 Bit Error Indication Counters

The Sa6 bit error indication counter CRC2L/H (16 bits) counts the received Sa6 bit sequence 0001 or 0011 in every CRC submultiframe.In the primary rate access digital section this counter option gives information about CRC errors reported from the TE via Sa6 bit. Incrementing is only possible in the multiframe synchronous state.

The Sa6 bit error indication counter CRC3L/H (16 bits) counts the received Sa6 bit sequence 0010 or 0011 in every CRC submultiframe. In the primary rate access digital section this counter option gives information about CRC errors detected at T-reference point and reporting them via the Sa6 bit. Incrementing is only possible in the multiframe synchronous state.

E-Bit Access

Due to signaling requirements, the E bits of frame 13 and frame 15 of the CRC multiframe can be used to indicate received errored submultiframes:

Submultiframe I status E- Bit located in frame 13
Submultiframe II status E- Bit located in frame 15

no CRC error: : E = 1

CRC error: : E = 0

Standard Procedure

After reading the Submultiframe Error Indication RSP.SI1 and RSP.SI2, the microprocessor has to update contents of register XSP (XS13, XS15). Access to these registers has to be synchronized to Transmit or Receive Multiframe Begin Interrupts (ISR0.RMB or ISR1.XMB).

In the double- and multiframe asynchronous state the E-bits are set to zero. However they can be set to one in the async. state if enabled via bit XSP.EBP. In the multiframe sync. state the E-bits are processed according to ITU-T G.704 independent of bit XSP.EBP.

Automatic Mode

By setting bit XSP.AXS status information of received submultiframes is automatically inserted in E-bit position of the outgoing CRC Multiframe without any further interventions of the microprocessor.

Submultiframe Error Indication Counter

The EBC (E-Bit) Counter EBCL and EBCH (16 bits) counts zeros in E-bit position of frame 13 and 15 of every received CRC Multiframe. This counter option gives information about the outgoing transmit PCM line if the E bits are used by the remote end for submultiframe error indication. Incrementing is only possible in the multiframe synchronous state.

*Note: E-bits may be processed via the system interface. Setting bit TSWM.TSIS enables transparency for E bits in transmit direction (refer to **table 6**).*

2.1.4.3 Test Functions

There are two types of monitoring/testing functions:

- Active tests which partly degrade the functionality (e.g. Payload Loop, Remote Loop, Local Loop, test loop for a single channel).
- Diagnostics, during which the device is not operational (e.g. diagnostic loop of an entire trunk).

Single Channel Loop Back

Each of the 32 channels may be selected for loopback from the system PCM input (XDI) to the system PCM output (RDO). This loopback is programmed for one channel at a time selected by register LOOP. During loopback, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route channel.

For the channel test, sending sequences of test patterns like a 1 kHz check signal should be avoided. Otherwise, an increased occurrence of slips in the tested channel will disturb testing. These slips do not influence the other channels and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

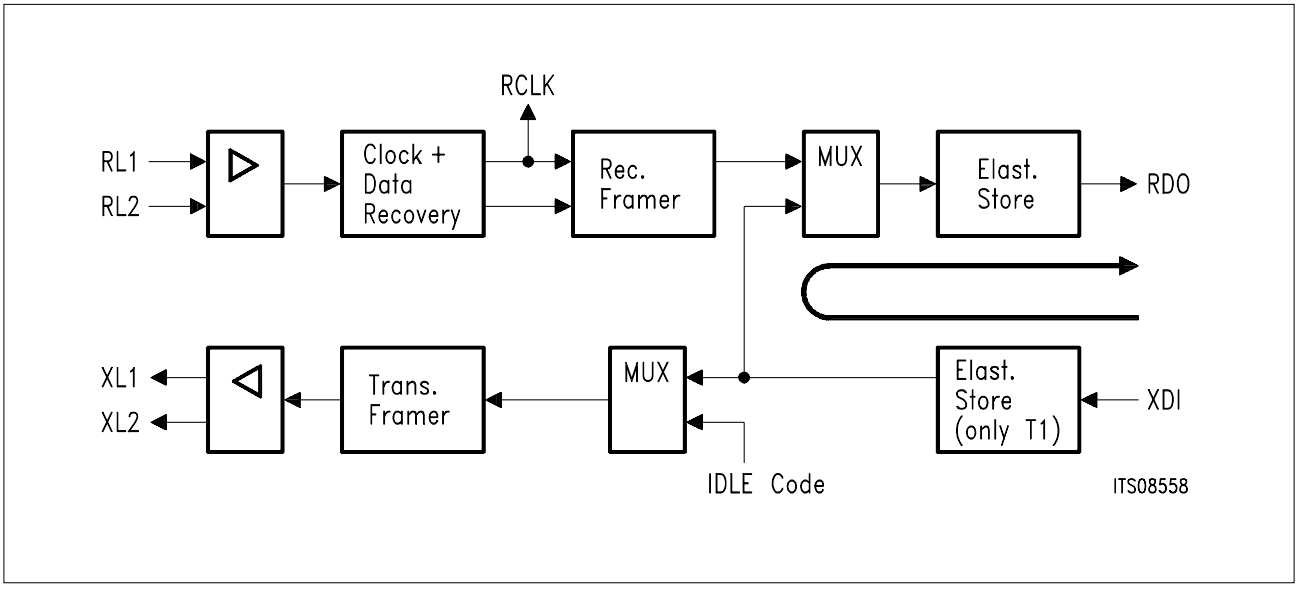


Figure 17
Single Channel Loopback

Payload Loop Back

To perform an effective circuit test a payload loop is implemented. The payload loop back (FMR2.PLB) will loop the data stream from the receiver section back to transmitter section. The looped data will pass the complete receiver including the wander and jitter compensation in the receive elastic store and were output on pin RDO. Instead of the data an AIS (FMR2.SAIS) could be sent to the system interface.

The framing bits, CRC4 and Spare bits are not looped. They are originated by the FALC54 transmitter. When the PLB is enabled the transmitter and the data on pins XL1/2 or XDOP/XDON are clocked with SCLKR instead of SCLKX. Data on pin XDI are ignored. All the received data are processed normally.

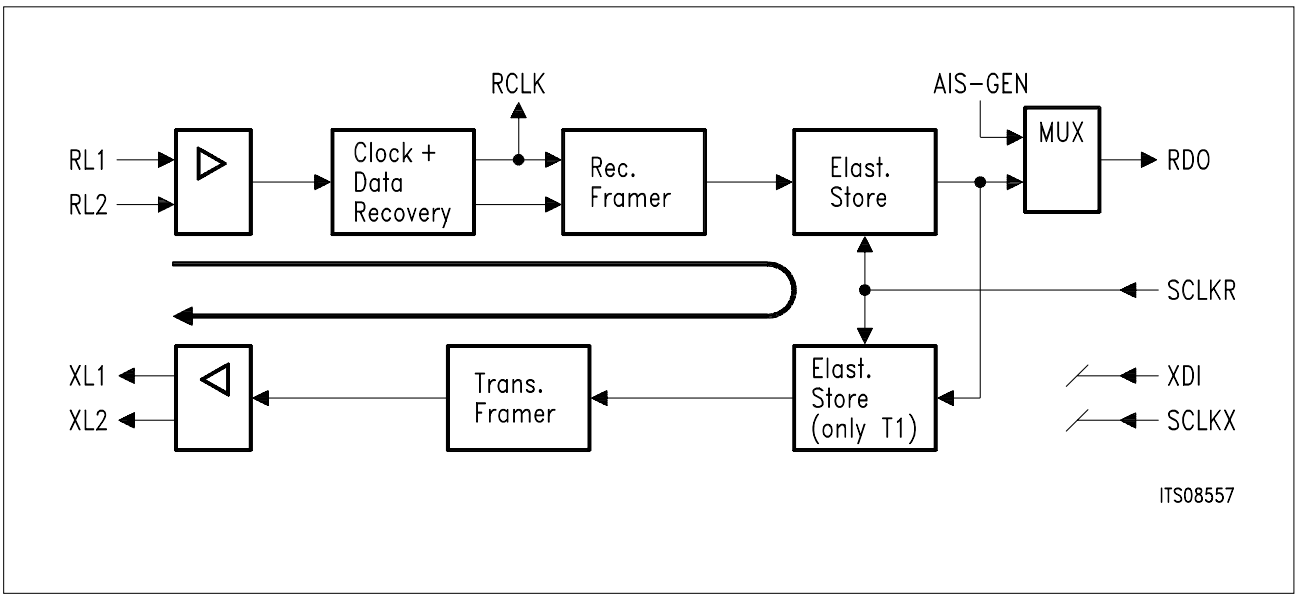


Figure 18
Payload Loop

Local Loop

The local loopback mode, selected by LIM0.LL = 1, disconnects the receive lines RL1/2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. However, the bit stream will be undisturbed transmitted on the line. However an AIS to the distant end could be enabled by setting FMR1.XAIS without influencing the data looped back to the system interface.

Note that enabling the local loop will usually invoke an out of frame error until the receiver can resync to the new framing. The serial code from the transmitter and receiver has to be programmed identically.

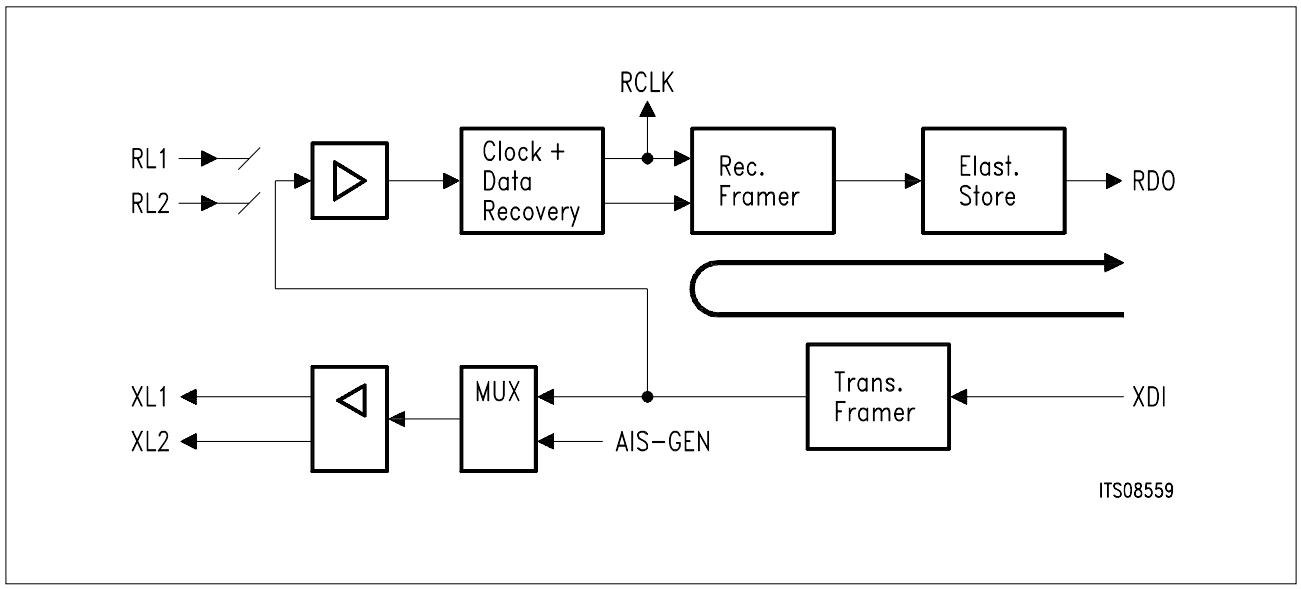


Figure 19
Local Loop

Remote Loop

In the remote loopback mode the clock and data recovered from the line inputs RL1/2 or RDIP/RDIN are routed back to the line outputs XL1/2 or XDOP/XDON via the analog or digital transmitter. As in normal mode they are also processed by the synchronizer and then sent to the system interface.The remote loopback mode is selected by setting the respective control bits LIM1.RL+JATT. Received data may be looped with or without the transmit jitter attenuator (FIFO).

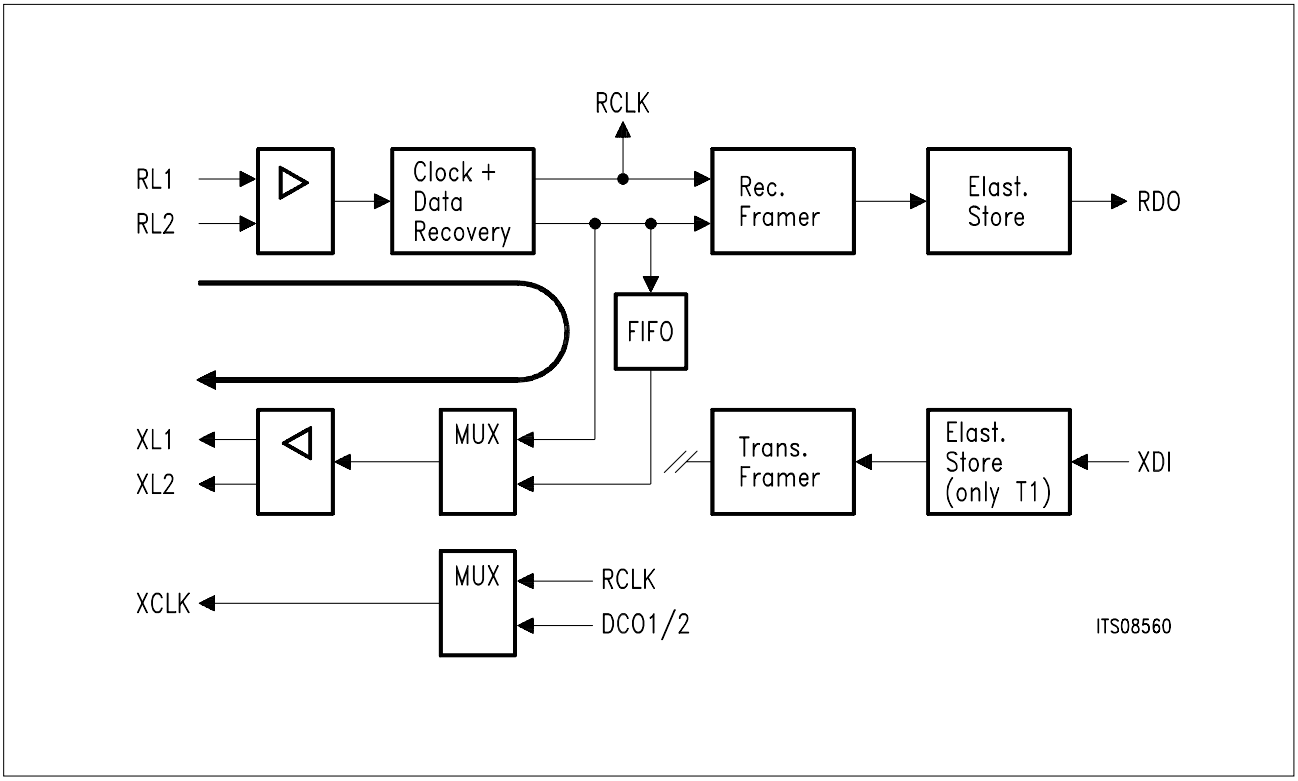


Figure 20
Remote Loop

Alarm Simulation

Alarm simulation does not affect the normal operation of the device, i.e. all channels remain available for transmission. However, possible ‘real’ alarm conditions are not reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit FMR0.SIM. The following alarms are simulated:

- Loss of Signal
- Alarm Indication Signal (AIS)
- Auxiliary pattern
- Loss of pulse frame
- Remote alarm indication
- Receive slip indication
- Framing error counter
- Code violation counter (HDB3 Code)
- CRC4 error counter
- E-Bit error counter
- CEC2 counter
- CEC3 counter

Some of the above indications are only simulated if the FALC54 is configured in a mode where the alarm is applicable (e.g. no CRC4 error simulation when doubleframe format is enabled).

– Setting of the bit FMR0.SIM initiates alarm simulation, interrupt status bits will be set. Error counting and indication will occurs while this bit is set. After it is reset all simulated error conditions disappear, but the generated interrupt statuses are still pending until the corresponding interrupt status register is read. Alarms like AIS and LOS are cleared automatically. Interrupt status register and error counters are automatically cleared on read.

2.2 Signaling Controller

Operating Modes

The HDLC controller can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be performed in a very flexible way, to satisfy almost any practical requirements.

There are 4 different operating modes which can be set via the MODE register.

2.2.1 HDLC Mode

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Depending on the selected address mode, the FALC54 can perform a 1 or 2 byte address recognition (MODE.MDS0).

If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R) and will be excluded from the address comparison.

Similarly, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the FALC54 can be called (addressed) with 6 different address combinations. HDLC frames with address fields that do not match any of the address combinations, are ignored by the FALC.

In case of a 1-byte address, RAL1 and RAL2 will be used as compare registers. The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. Additional information can also be read from register RSIS.

As defined by the HDLC protocol, the FALC54 perform the zero bit insertion/deletion (bit-stuffing) in the transmit/receive data stream automatically. That means, it is guaranteed that at least after 5 consecutive “1”-s a “0” will appear.

Non-Auto Mode (MODE.MDS2-1=01)

Characteristics: address recognition, FLAG - and CRC generation/check, bit-stuffing

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Transparent Mode 1 (MODE.MDS2-0=101)

Characteristics: address recognition, FLAG - and CRC generation/check, bit-stuffing

Only the high byte of a 2-byte address field will be compared with registers RAH1/2. The whole frame excluding the first address byte will be stored in RFIFO.

Transparent Mode 0 (MODE.MDS2-0=100)

Characteristics: FLAG - and CRC generation/check, bit-stuffing

No address recognition is performed and each frame will be stored in the RFIFO.

2.2.2 Extended Transparent Mode

Characteristics: fully transparent

In extended transparent mode, fully transparent data transmission/reception without HDLC framing is performed, i.e. without FLAG generation/recognition, CRC generation/check, or bit-stuffing. This feature can be profitably used e.g for:

- Specific protocol variations
- Test purposes

Data transmission is always performed out of the XFIFO. In transparent mode, the receive data are shifted into the RFIFO.

Receive Data Flow

The following figure gives an overview of the management of the received HDLC frames in the different operating modes.

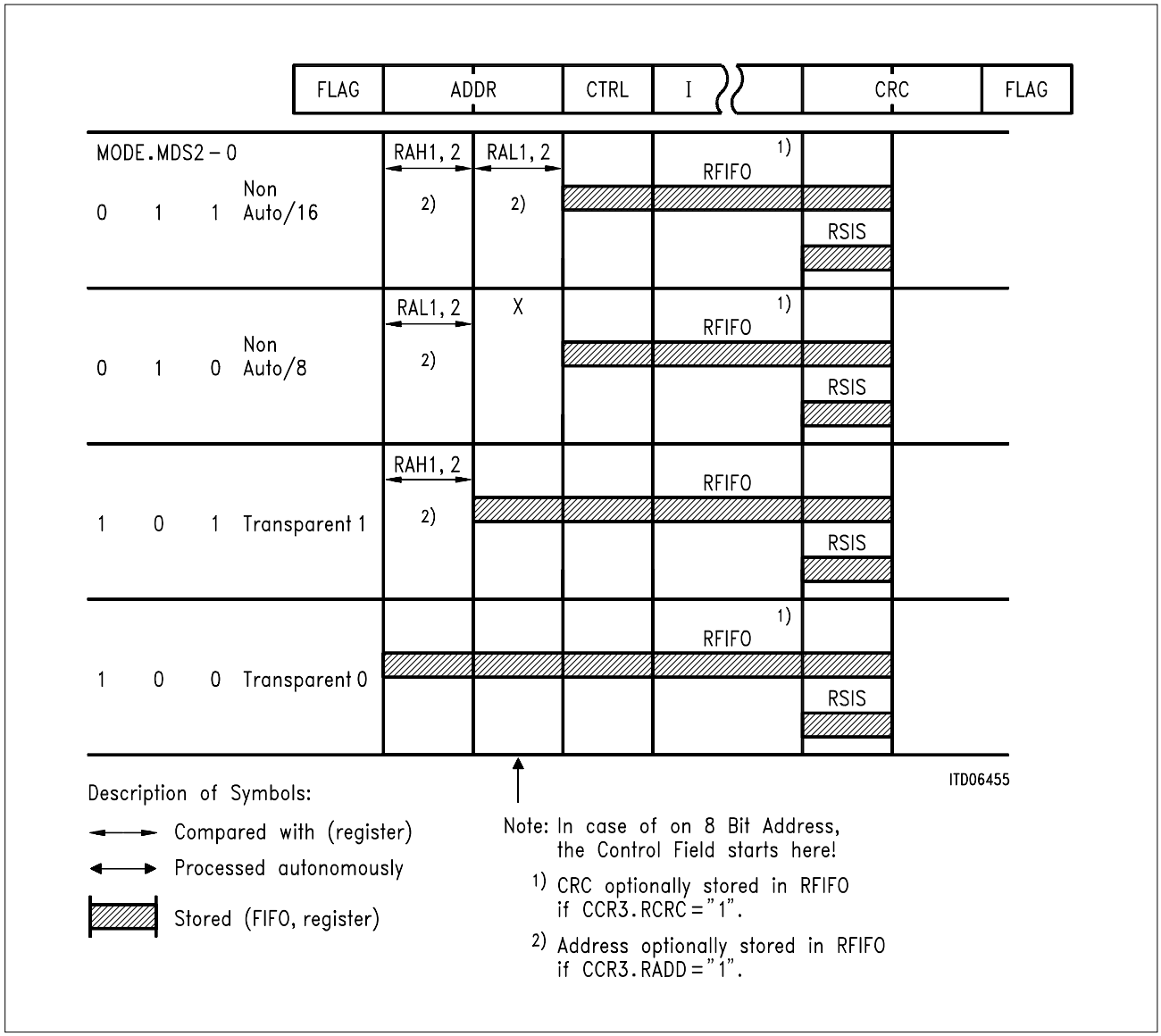


Figure 23
Receive Data Flow of FALC

Transmit Data Flow

The frames can be transmitted as shown below.

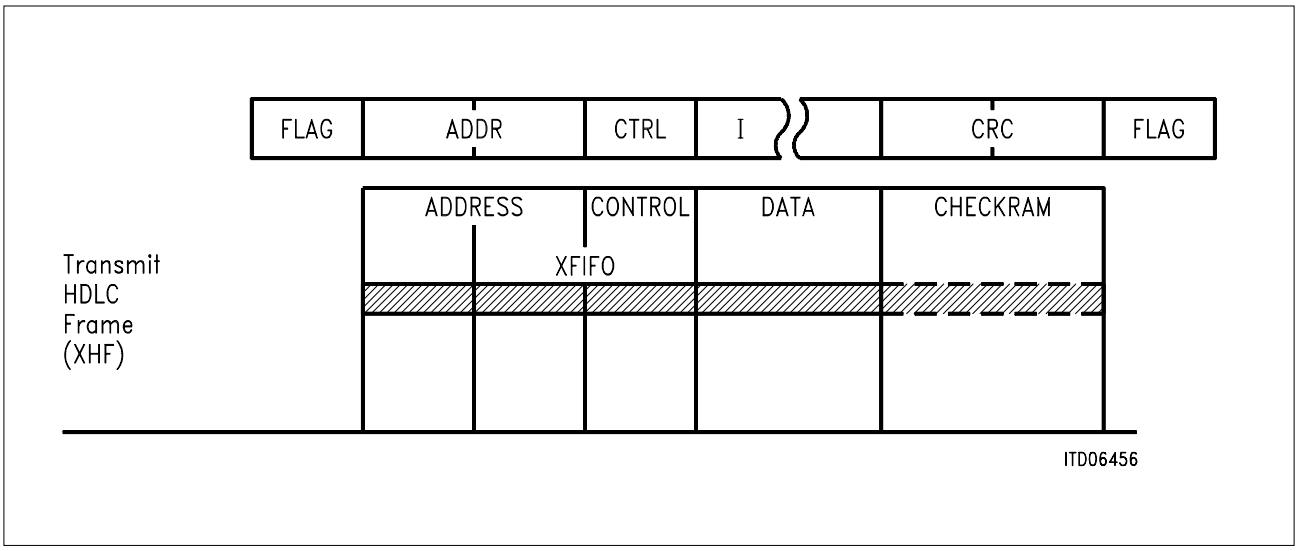


Figure 24
Transmit Data Flow of FALC54

Transmitting a HDLC frame via register CMDR.XTF, the address, the control fields and the data field have to be entered in the XFIFO.

2.2.3 Special Functions

Shared Flags

The closing Flag of a previously transmitted frame simultaneously becomes the opening Flag of the following frame if there is one to be transmitted. The Shared Flag feature is enabled by setting bit SFLG in control register CCR1.

Preamble Transmission

If enabled via register CCR3, a programmable 8-bit pattern (register PRE) is transmitted with a selectable number of repetitions after Interframe Timefill transmission is stopped and a new frame is ready to be sent out.

Zero Bit Insertion is disabled during preamble transmission. To guarantee correct function the programmed preamble value should be different from Receive Address Byte values.

Transparent Transmission and Reception

When programmed in the extended transparent mode via the MODE register (MDS2-0 = 111), the FALC54 performs fully transparent data transmission and reception without HDLC framing, i.e. without

- FLAG insertion and deletion
- CRC generation and checking
- Bit-stuffing

In order to enable fully transparent data transfer, bit MODE.HRAC has to be set and FF_H has to be written to RAH2.

Data transmission is always performed out of XFIFO by directly shifting the contents of

XFIFO in the outgoing datastream. Transmission is initiated by setting CMDR.XTF (04_H). A synch-byte FF_H is automatically sent before the first byte of the XFIFO will be transmitted.

Received data is always shifted into RFIFO.

Cyclic Transmission (fully transparent)

If the extended transparent mode is selected, the FALC54 supports the continuous transmission of the contents of the transmit FIFO.

After having written 1 to 32 bytes to XFIFO, the command XREP.XTF via the CMDR register (bit 7 … 0 = '00100100' = 24_H) forces the FALC54 to repeatedly transmit the data stored in XFIFO to the remote end.

The cyclic transmission continues until a reset command (CMDR. SRES) is issued or with resetting CMDR.XREP, after which continuous '1'-s are transmitted.

Note: During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

CRC ON/OFF Features

As an option in HDLC mode the internal handling of received and transmitted CRC checksum can be influenced via control bits CCR3.RCRC and CCR3.XCRC.

Receive Direction

The received CRC checksum is always assumed to be in the 2 (CRC-ITU) last bytes of a frame, immediately preceding a closing flag. If CCR3.RCRC is set, the received CRC checksum will be written to RFIFO where it precedes the frame status byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If HDLC mode is selected, the limits for 'Valid Frame' check are modified (refer to description of bit RSIS.VFR).

Transmit Direction

If CCR3.XCRC is set, the CRC checksum is not generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame will only be closed automatically with a (closing) flag.

The FALC54 does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

Receive Address Pushed to RFIFO

The address field of received frames can be pushed to RFIFO (first one/two bytes of the frame). This function is especially useful in conjunction with the extended address recognition. It is enabled by setting control bit CCR3.RADD.

2.2.4 Time-Slot Assigner

The FALC54 offers the flexibility to extract or insert data during certain time-slots which are defined via registers RTR1-4 and TTR1-4. Any combination of time-slots can be programmed independent for the receive and transmit direction.

Table 7
Time-Slot Assigner

		Time-Slots
Receive Time-Slot Register	**Transmit Time-Slot Register**	
RTR1.7	TTR1.7	0
RTR1.6	TTR1.6	1
RTR1.5	TTR1.5	2
RTR1.4	TTR1.4	3
RTR1.3	TTR1.3	4
RTR1.2	TTR1.2	5
RTR1.1	TTR1.1	6
RTR1.0	TTR1.0	7
RTR2.7	TTR2.7	8
RTR2.6	TTR2.6	9
RTR2.5	TTR2.5	10
RTR2.4	TTR2.4	11
RTR2.3	TTR2.3	12
RTR2.2	TTR2.2	13
RTR2.1	TTR2.1	14
RTR2.0	TTR2.0	15
RTR3.7	TTR3.7	16
RTR3.6	TTR3.6	17
RTR3.5	TTR3.5	18
RTR3.4	TTR3.4	19
RTR3.3	TTR3.3	20
RTR3.2	TTR3.2	21
RTR3.1	TTR3.1	22
RTR3.0	TTR3.0	23
RTR4.7	TTR4.7	24
RTR4.6	TTR4.6	25
RTR4.5	TTR4.5	26
RTR4.4	TTR4.4	27
RTR4.3	TTR4.3	28
RTR4.2	TTR4.2	29
RTR4.1	TTR4.1	30
RTR4.0	TTR4.0	31

2.2.5 S_a bit Access

The FALC54 supports the S_a bit signaling of time-slot 0 of every other frame in several ways. The access via registers RSW/XSW, the access via registers R/XSA8-4, capable of storing the information for a complete multiframe, and the most effective one is the access via the 64 byte deep receive/transmit FIFO of the integrated signaling controller.

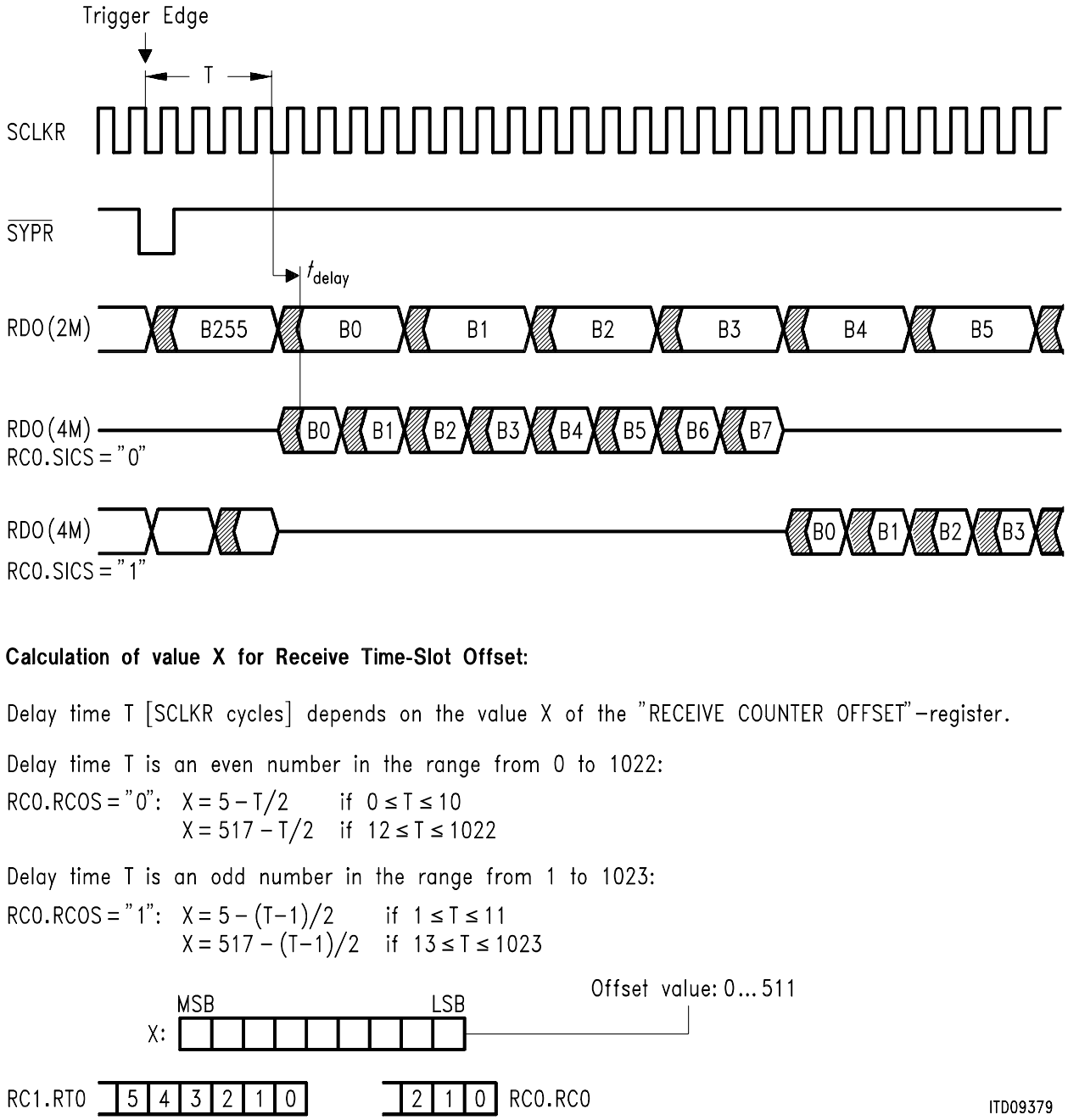
The extended S_a bit access gives the opportunity to transmit/receive a transparent bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Enabling is done by setting of bit CCR1.EITS and resetting of registers TTR1-4, RTR1-4 and FMR1.ENSA.

The data written to the XFIFO will subsequently transmit in the S_a bit positions defined by register XC0.SA8E-4E and the corresponding bits of TSWM.TSA8-4. Any combination of S_a bits can be selected. After the data have been completely sent out an “all ones” or Flags (CCR1.ITF) will be transmitted. The continuous transmission of a transparent bit stream, which is stored in the XFIFO, can be enabled.

With the setting of bit MODE.HRAC the received S_a bits can be forwarded to the receive FIFO.

The access to and from the FIFOs is supported by ISR0.RME,RPF and ISR1.XPR,ALS.

2.2.6 Interface to System Internal Highway



Calculation of value X for Receive Time-Slot Offset:

Delay time T [SCLKR cycles] depends on the value X of the "RECEIVE COUNTER OFFSET"-register.

Delay time T is an even number in the range from 0 to 1022:

RC0.RCOS = "0": $X = 5 - T/2$ if $0 \le T \le 10$

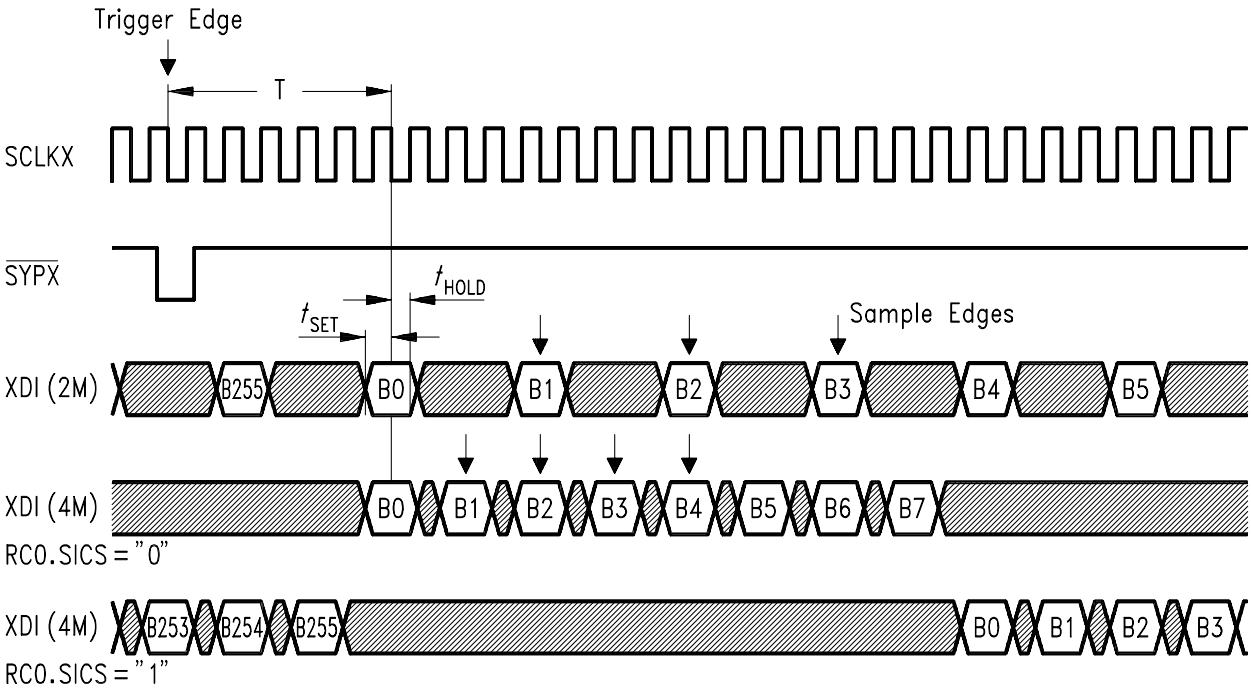
$X = 517 - T/2$ if $12 \le T \le 1022$

Delay time T is an odd number in the range from 1 to 1023:

RC0.RCOS = "1": $X = 5 - (T-1)/2$ if $1 \le T \le 11$

$X = 517 - (T-1)/2$ if $13 \le T \le 1023$

Figure 25
Data on RDO



Calculation of value X for Transmit Time-Slot Offset:

Delay time T [SCLKX cycles] depends on the value X of the "TRANSMIT COUNTER OFFSET"-register.

Delay time T is an even number in the range from 0 to 1022:

XC1.XCOS = "0": $X = 498 - T/2$ if $0 \le T \le 996$

$X = 1010 - T/2$ if $998 \le T \le 1022$

Delay time T is an odd number in the range from 1 to 1023:

XC1.XCOS = "1": $X = 498 - (T-1)/2$ if $1 \le T \le 997$

$X = 1010 - (T-1)/2$ if $999 \le T \le 1023$

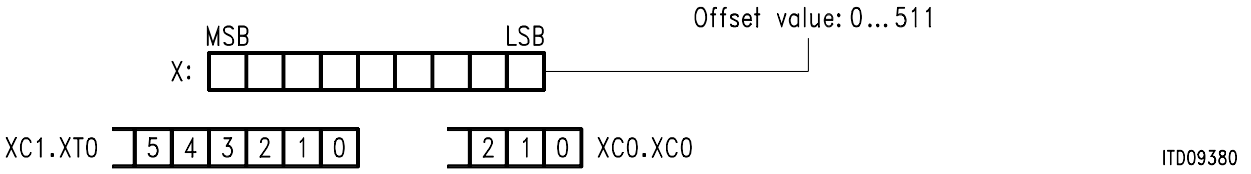


Figure 26
Data on XDI

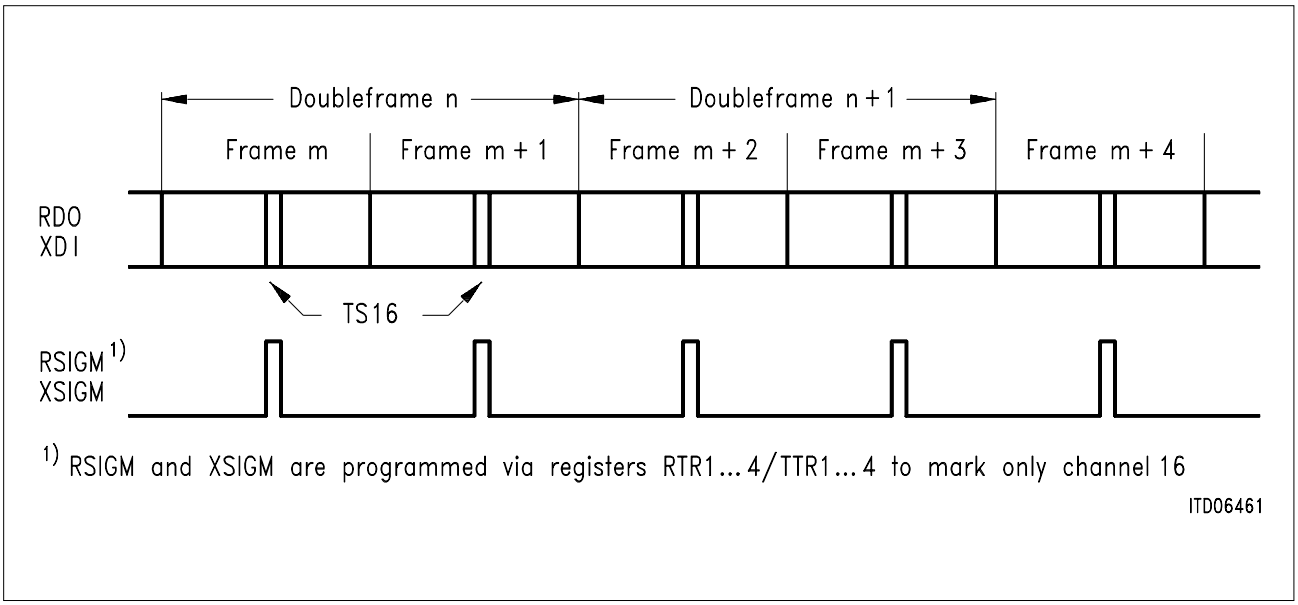


Figure 27
Supporting Signals for CCS/CAS-CC Applications

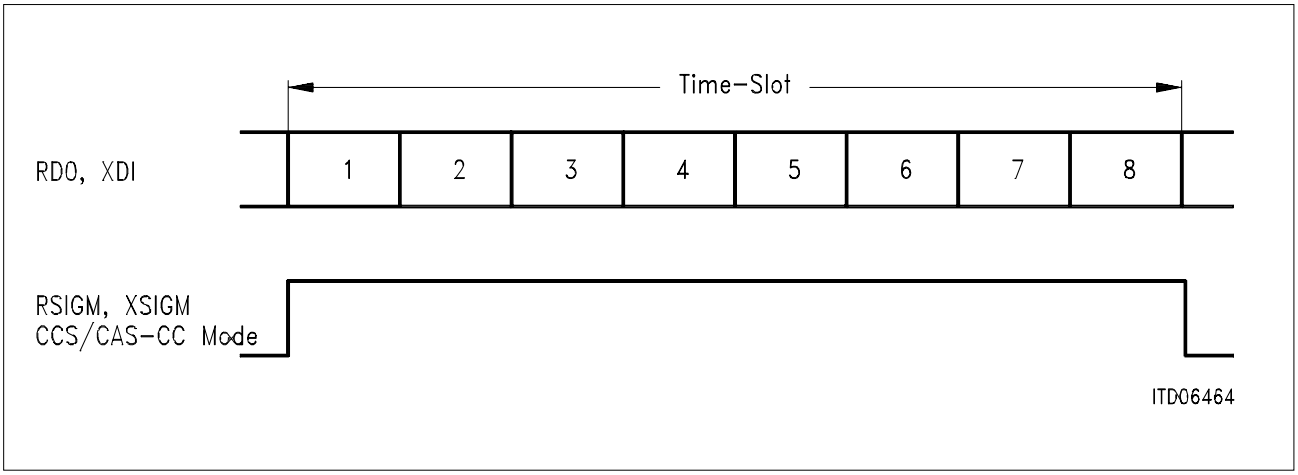


Figure 28
2-Mbyte/s Interface Mode

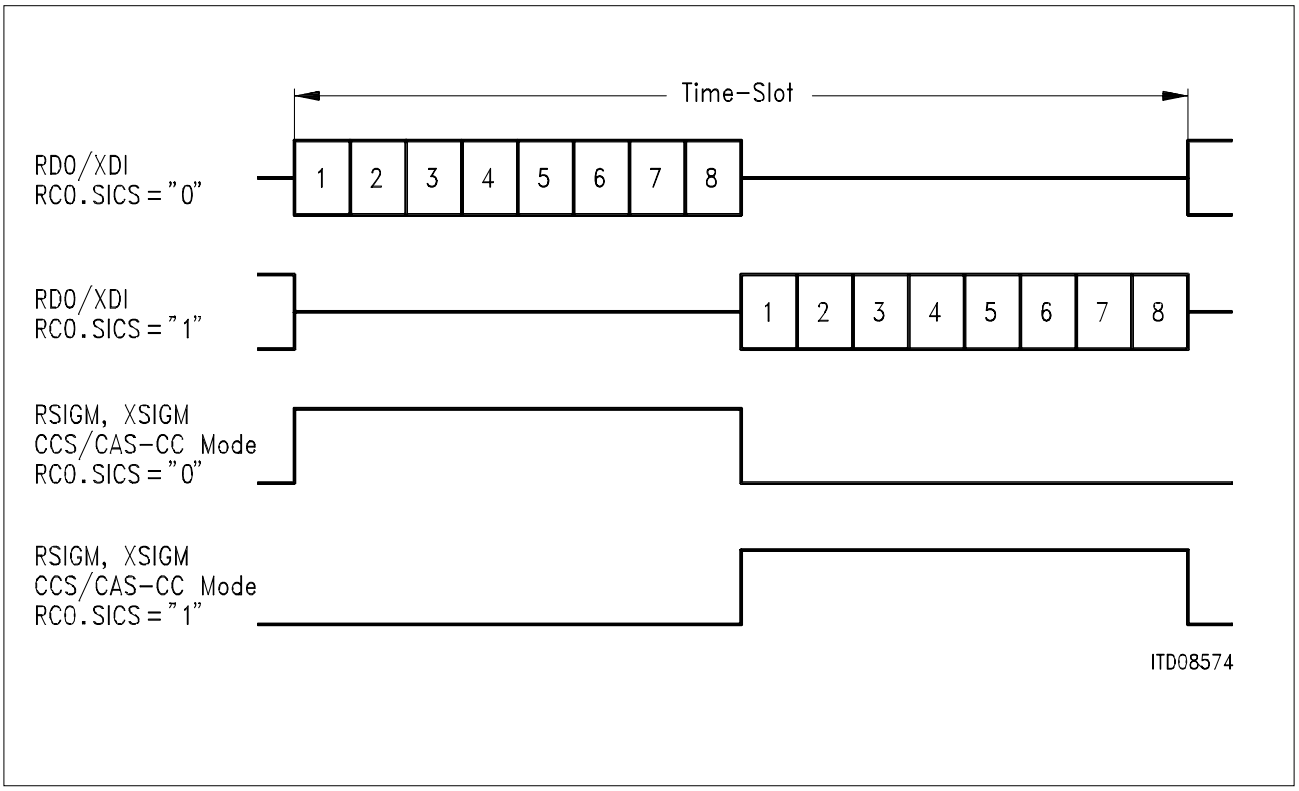


Figure 29
4-Mbyte System Interface Mode

3 Operational Description E1

Reset

The FALC54 is forced to the reset state if a high signal is input at port RES for a minimum period of 20 µs. During RESET, all output stages except CLK16M, CLK12M, CLK8M, CLKX, $\overline{FSC}$, XCLK and RCLK are in a high impedance state, all internal flip-flops are reset and most of the control registers are initialized with default values.

After RESET, the FALC54 is initialized for doubleframe format with register values listed in **table 8**.

Table 8
Initial Values after RESET

Register	Reset Value	Meaning
FMR0	00_H	NRZ Coding, No alarm simulation.
FMR1 FMR2	00_H	PCM 30 – doubleframe format, 4 Mbit/s system interface mode, no AIS transmission to remote end or system interface, Payload Loop off
LOOP XSW XSP TSWM	00_H 40_H 00_H 00_H	Channel loop back and single frame mode are disabled. All bits of the transmitted service word are cleared (bit 2 excl.). Spare bit values are cleared. No transparent mode active
XC0 XC1	00_H 00_H	The transmit clock offset is cleared. The transmit time-slot offset is cleared.
RC0 RC1	00_H 00_H	The receive clock slot offset is cleared. The receive time-slot offset is cleared.
IDLE ICB 1…4	00_H 00_H	Idle channel code is cleared. Normal operation (no ‘Idle Channel’ selected).
LIM0	00_H	Slave Mode, Local Loop off, frequency on pin CLKX: 2.048 MHz, no LOS indication on pin RCLK
LIM1 PCD PCR	00_H 00_H 00_H	Analog interface selected, Remote Loop off Pulse Count for LOS Detection cleared Pulse Count for LOS Recovery cleared
XPM2-0	$9c_H$,03_H,00_H	Transmit Pulse Mask
IMR1-4	FF_H	All interrupts are disabled
RTR1-4 TTR1-4	00_H	No time-slots selected

Table 8
Initial Values after RESET (cont'd)

Register	Reset Value	Meaning
MODE	00_H	Signaling controller disabled
PRE	00_H	Preamble cleared
RAH1/2	FD_H,FF_H	Compare register for receive address cleared
RAL1/2	FF_H,FF_H	

Operational Phase

The FALC54 is programmable via a microprocessor interface which enables access to 69 control and 48 status registers.

After RESET the FALC54 first must be initialized. General guidelines for initialization are described in section Initialization.

The status registers are read-only and are continuously updated. Normally, the processor periodically reads the status registers to analyze the alarm status and signaling data.

Initialization

For a correct start up of the Primary Access Interface a set of parameters specific to the system and hardware environment must be programmed after RESET goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T and ETSI recommendations (e.g. Fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 9** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, may be programmed simultaneously. The bit FMR1.PMOD should always be kept low.

Table 9
Initialization Parameters

Basic Set Up	PCM 30
Mode Select	FMR1.PMOD = 0
Specification of Line interface and clock generation	LIM0, LIM1, XPM2-0
Line interface coding	FMR0.XC1/0, FMR0.RC1/0
Loss of Signal detection / recovery conditions	PCD, PCR,LIM1
System interface mode	FMR1.IMOD
Transmit offset counters	XC0.XCO, XC1.XTO
Receive offset counters	RC0.RCO, RC1.RTO
AIS to system interface	FMR2.DAIS/SAIS

Operational Set Up	PCM 30
Select framing	FMR2.RFS1/0, FMR1.XFS
Framing additions	RC1.ASY4, RC1.SWD
Synchronization mode	FMR1.AFR
Signaling mode	XSP, XSW, FMR1.ENSA, XSA8-4, TSWM, MODE, CCR1, CCR3, PRE, RAH1/2, RAL1/2

Features like channel loop back, idle channel activation, extensions for signaling support, alarm simulation, …may be activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Note: Read access to unused register addresses: value should be ignored.
Write access to unused register addresses: should be avoided, or set to '00' hex.
All control registers (except XFIFO, XS1-16, CMDR, DEC) are of type: Read/Write.

HDLC Data Transmission

In transmit direction 2x32 byte FIFO buffers are provided. After checking the XFIFO status by polling the bit SIS.XFW or after an interrupt ISR1.XPR (Transmit Pool Ready), up to 32 bytes may be entered by the CPU to the XFIFO.

The transmission of a frame can be started by issuing a XTF or XHF command via the command register. If enabled, a specified number of preambles (register PRE) are optionally sent out before transmission of the current frame starts. If the transmit command does not include an end of message indication (CMDR.XME), the FALC54 will repeatedly request for the next data block by means of a XPR interrupt as soon as no more than 32 bytes are stored in the XFIFO, i.e. a 32-byte pool is accessible to the CPU.

This process will be repeated until the CPU indicates the end of message per XME command, after which frame transmission is finished correctly by appending the CRC and closing flag sequence. Consecutive frames may be share a flag (enabled via CCR1.SFLG), or may be transmitted as back-to-back frames, if service of XFIFO is quick enough.

In case no more data is available in the XFIFO prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence and the CPU is notified per interrupt ISR1.XDU. The frame may be aborted per software CMDR.SRES.

The data transmission sequence, from the CPU’s point of view, is outlined in **figure 30**.

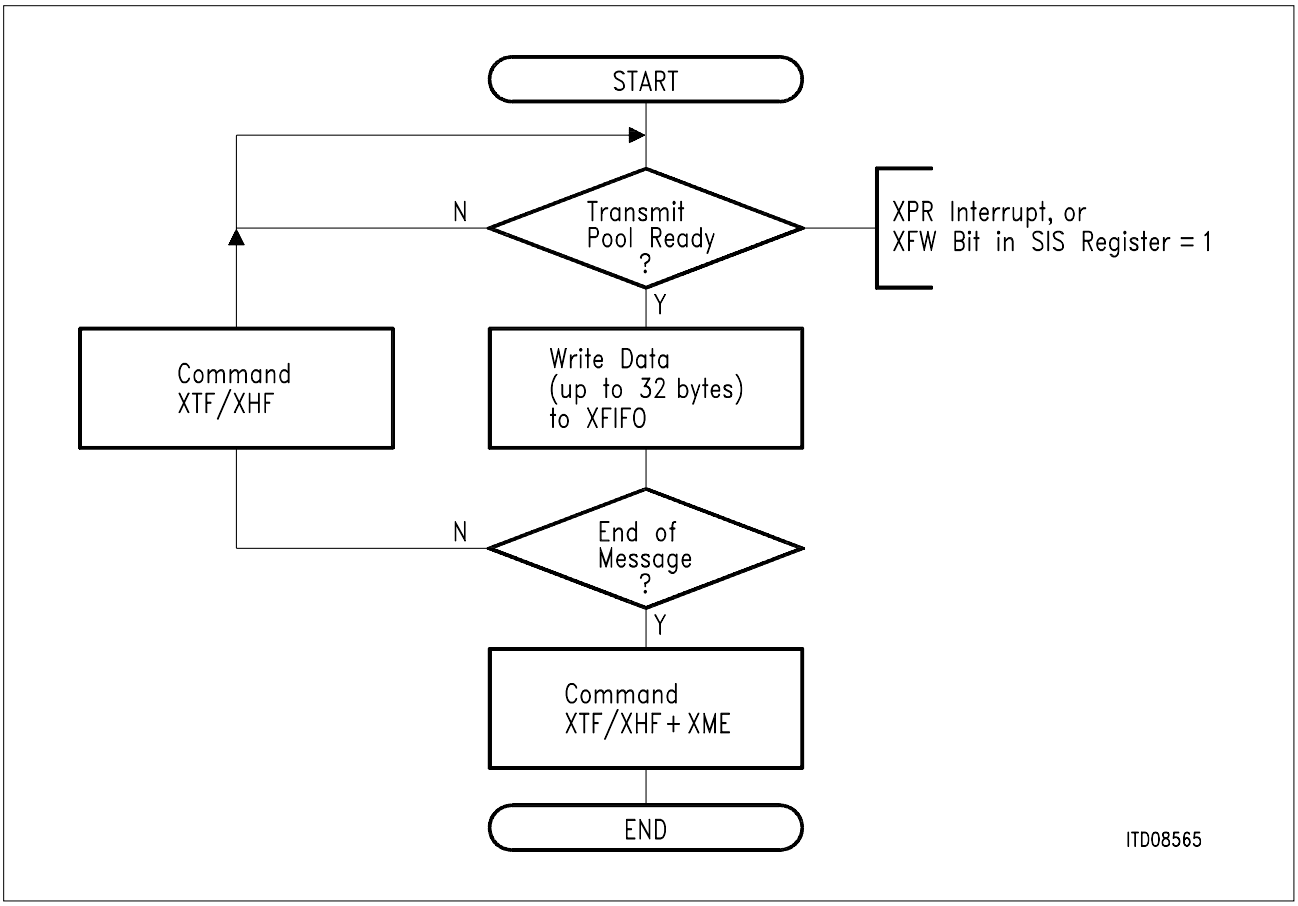


Figure 30
Interrupt Driven Data Transmission (flow diagram)

The activities at both serial and CPU interface during frame transmission (supposed frame length = 70 bytes) is shown in **figure 31**.

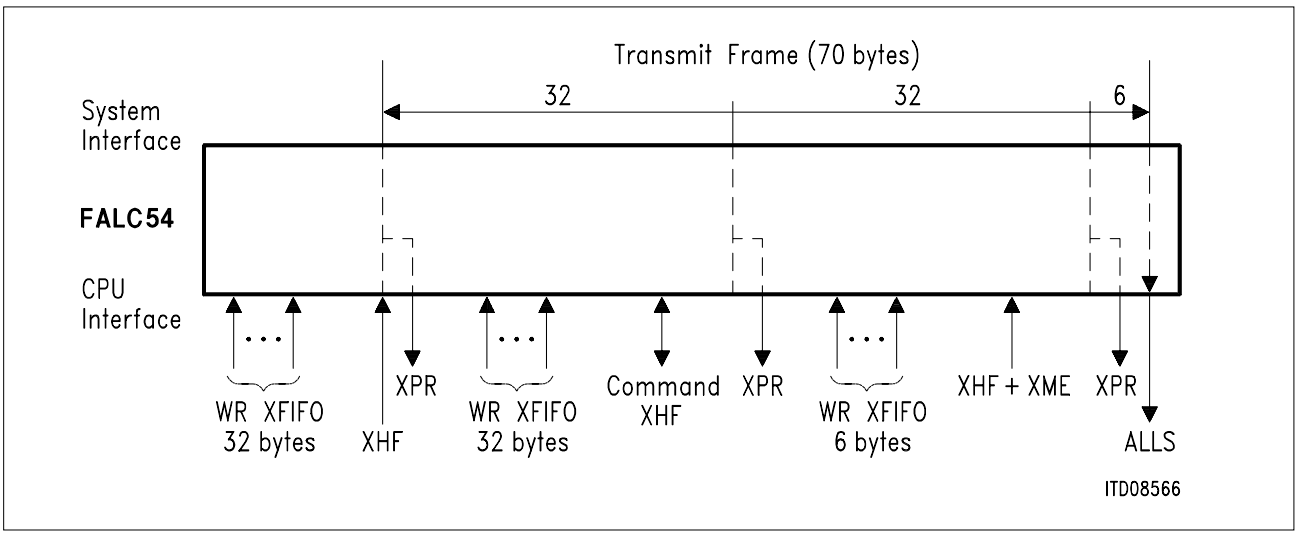


Figure 31
Interrupt Driven Transmission Sequence Example

Data Reception

Also 2x32 byte FIFO buffers are provided in receive direction. There are different interrupt indications concerned with the reception of data:

HDLC

RPF (Receive Pool Full) interrupt, indicating that a 32-byte-block of data can be read from RFIFO and the received message is not yet complete.

RME (Receive Message End) interrupt, indicating that the reception of one message is completed.

The following **figure 32** gives an example of a reception sequence, assuming that a “long” frame (66 bytes) followed by two short frames (6 bytes each) are received.

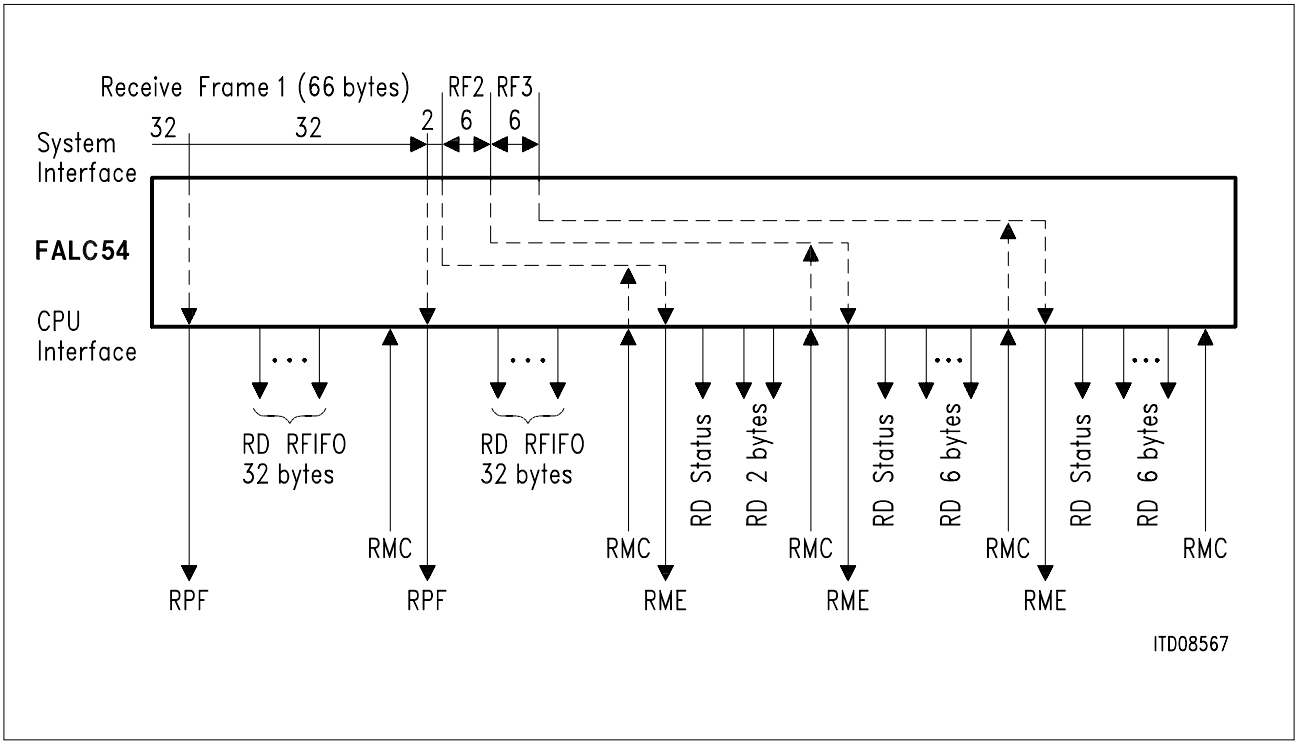


Figure 32
Interrupt Driven Reception Sequence Example

3.1 Detailed Register Description E1

3.1.1 Control Register Description

Table 10
Control Register Address Arrangement

Address	Register	Type	Comment
00	XFIFO	W	Transmit FIFO
01	XFIFO	W	Transmit FIFO
02	CMDR	W	Command Register
03	MODE	R/W	Mode Register
04	RAH1	R/W	Receive Address High 1
05	RAH2	R/W	Receive Address High 2
06	RAL1	R/W	Receive Address Low 1
07	RAL2	R/W	Receive Address Low 2
08	IPC	R/W	Interrupt Port Configuration
09	CCR1	R/W	Common Configuration Register 1
0A	CCR3	R/W	Common Configuration Register 3
0B	PRE	R/W	Preamble Register
0C	RTR1	R/W	Receive Timeslot Register 1
0D	RTR2	R/W	Receive Timeslot Register 2
0E	RTR3	R/W	Receive Timeslot Register 3
0F	RTR4	R/W	Receive Timeslot Register 4
10	TTR1	R/W	Transmit Timeslot Register 1
11	TTR2	R/W	Transmit Timeslot Register 2
12	TTR3	R/W	Transmit Timeslot Register 3
13	TTR4	R/W	Transmit Timeslot Register 4
14	IMR0	R/W	Interrupt Mask Register 0
15	IMR1	R/W	Interrupt Mask Register 1
16	IMR2	R/W	Interrupt Mask Register 2
17	IMR3	R/W	Interrupt Mask Register 3
18	IMR4	R/W	Interrupt Mask Register 4
19			
1A	FMR0	R/W	Framer Mode Register 0

Table 10
Control Register Address Arrangement (cont'd)

Address	Register	Type	Comment
1B	FMR1	R/W	Framer Mode Register 1
1C	FMR2	R/W	Framer Mode Register 2
1D	LOOP	R/W	Channel Loop Back
1E	XSW	R/W	Transmit Service Word
1F	XSP	R/W	Transmit Spare Bits
20	XC0	R/W	Transmit Control 0
21	XC1	R/W	Transmit Control 1
22	RC0	R/W	Receive Control 0
23	RC1	R/W	Receive Control 1
24	XPM0	R/W	Transmit Pulse Mask 0
25	XPM1	R/W	Transmit Pulse Mask 1
26	XPM2	R/W	Transmit Pulse Mask 2
27	TSWM	R/W	Transparent Service Word Mask
28	TEST	R/W	Manufacturer Test Register
29	IDLE	R/W	Idle Channel Code
2A	XSA4	R/W	Transmit SA4 Bit Register
2B	XSA5	R/W	Transmit SA5 Bit Register
2C	XSA6	R/W	Transmit SA6 Bit Register
2D	XSA7	R/W	Transmit SA7 Bit Register
2E	XSA8	R/W	Transmit SA8 Bit Register
2F	FMR3	R/W	Framer Mode Register 3
30	ICB1	R/W	Idle Channel Register 1
31	ICB2	R/W	Idle Channel Register 2
32	ICB3	R/W	Idle Channel Register 3
33	ICB4	R/W	Idle Channel Register 4
34	LIM0	R/W	Line Interface Mode 0
35	LIM1	R/W	Line Interface Mode 1
36	PCD	R/W	Pulse Count Detection
37	PCR	R/W	Pulse Count Recovery
38	LIM2	R/W	Line Interface Mode 2

Table 10
Control Register Address Arrangement (cont'd)

Address	Register	Type	Comment
60	DEC	W	Disable Error Counter
62	TEST	W	Manufacturer Test Register
70	XS1	W	Transmit CAS Register 1
71	XS2	W	Transmit CAS Register 2
72	XS3	W	Transmit CAS Register 3
73	XS4	W	Transmit CAS Register 4
74	XS5	W	Transmit CAS Register 5
75	XS6	W	Transmit CAS Register 6
76	XS7	W	Transmit CAS Register 7
77	XS8	W	Transmit CAS Register 8
78	XS9	W	Transmit CAS Register 9
79	XS10	W	Transmit CAS Register 10
7A	XS11	W	Transmit CAS Register 11
7B	XS12	W	Transmit CAS Register 12
7C	XS13	W	Transmit CAS Register 13
7D	XS14	W	Transmit CAS Register 14
7E	XS15	W	Transmit CAS Register 15
7F	XS16	W	Transmit CAS Register 16

After 'RESET' all control registers except the XFIFO and XS1-16 are initialized to defined values.

The status registers are only readable and are updated by the FALC.

Transmit FIFO (WRITE) XFIFO

	7							0	
XFIFO	XF7							XF0	(00/01)

Up to 32 bytes/16 words of received data can be read from the RFIFO following a RPF or a RME interrupt.
Writing data to XFIFO can be done in 8-bit (byte) or 16-bit (word) access. The LSB is transmitted first.

Up to 32 bytes/16 words of transmit data can be written to the XFIFO following a XPR (or ALLS) interrupt.

Command Register (Write)

Value after RESET: 00_H

	7							0	
CMDR	RMC	RRES	XREP	XRES	XHF	XTF	XME	SRES	(02)

RMC… **Receive Message Complete**

Confirmation from CPU to FALC54 that the current frame or data block has been fetched following a RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

RRES… **Receiver Reset**

The receive line interface except the clock and data recovery unit (DPLL), the receive framer, the one second timer and the receive signaling controller are reset. However the contents of the control registers will not be deleted.

XREP… **Transmission Repeat**

If XREP is set to one together with XTF (write 24_H to CMDR), the FALC54 repeatedly transmits the contents of the XFIFO (1 … 32 bytes) without HDLC framing fully transparently, i.e. without FLAG,CRC.

The cyclic transmission is stopped with a SRES command or by resetting XREP.

Note: During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

XRES… **Transmitter Reset**

The transmit framer and transmit line interface excluding the system clock generator and the pulse shaper will be reset. However the contents of the control registers will not be deleted.

XHF… **Transmit HDLC Frame**

After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a HDLC frame.

XTF… **Transmit Transparent Frame**

Initiates the transmission of a transparent frame without HDLC framing.

XME… **Transmit Message End**

Indicates that the data block written last to the transmit FIFO completes the current frame. The FALC54 can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

SRES… **Signaling Transmitter Reset**

The transmitter of the signaling controller will be reset. XFIFO is cleared of any data and an abort sequence (seven 1's) followed by interframe time fill is transmitted. In response to XRES a XPR interrupt is generated.

This command can be used by the CPU to abort a frame currently in transmission.

Note: The maximum time between writing to the CMDR register and the execution of the command depends on FMR1.IMOD. If FMR1.IMOD is set it takes 10 SCLKX cycles and 5 SCLKX cycles if FMR1.IMOD is cleared. Therefore, if the CPU operates with a very high clock rate in comparison with the FALC's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.

Mode Register (Read/Write)

Value after RESET: 00_H

	7							0	
MODE	MDS2	MDS1	MDS0		HRAC				(03)

MDS2-0… **Mode Select**

The operating mode of the HDLC controller is selected.

000… Reserved

001… Reserved

010… 1 byte address comparison mode (RAL1,2)

011… 2 byte address comparison mode (RAH1,2 and RAL1,2)

100… No address comparison

101… 1 byte address comparison mode (RAH1,2)

110… Reserved

111… No HDLC framing mode

HRAC… **HDLC Receiver Active**

Switches the HDLC receiver to operational or inoperational state.

0… Receiver inactive

1… Receiver active

Receive Address Byte High Register 1 (Read/Write)

Value after RESET: FD_H

	7							0	
RAH1							0		(04)

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individually programmable values in RAH1 and RAH2.

RAH1… **Value of the First Individual High Address Byte**

Bit 1 (C/R-bit) is excluded from address comparison.

Receive Address Byte High Register 2 (Read/Write)

Value after RESET: FF_H

	7							0	
RAH2									(05)

RAH2… **Value of Second Individual High Address Byte**

Receive Address Byte Low Register 1 (Read/Write)

Value after RESET: FF_H

	7							0	
RAL1									(06)

RAL1… **Value of First Individual Low Address Byte**

Receive Address Byte Low Register 2 (Read/Write)

Value after RESET: FF_H

	7							0	
RAL2									(07)

RAL2... **Value of the second individually programmable low address byte.**

Interrupt Port Configuration (READ/WRITE)

Value after RESET: 00_H

	7							0	
IPC	VIS					SCI	IC1	IC0	(08)

Note: Unused bits have to be set to logical ‘0’.

VIS… **Masked Interrupts Visible**

0… Masked interrupt status bits are not visible.

1… Masked interrupt status bits are visible.

SCI… **Status Change Interrupt**

0… Interrupts will be generated either on coming or going of the internal interrupt source.

1… The following interrupts will be activated if enabled with detecting and recovering of the internal interrupt source:
ISR2.LOS; ISR2.AIS
ISR3.API; ISR3.LMFA16

IC0, IC1… **Interrupt Port Configuration**

These bits define the function of the interrupt output stage (pin INT):

IC1	IC0	Function
X	0	Open drain output
0	1	Push/pull output, active low
1	1	Push/pull output, active high

Common Configuration Register 1 (READ/WRITE)

Value after RESET: 00_H

	7						0		
CCR1	SFLG	XTS16RA	CASM	EITS	ITF		RFT1	RFT0	(09)

SFLG… **Enable Shared Flags**

If this bit is set, the closing FLAG of a preceding frame simultaneously becomes the opening FLAG of the following frame.

XTS16RA… **Transmit Time-Slot 16 Remote Alarm**

0… Standard operation

1… Sends remote alarm in time-slot 16 towards remote end by setting the Y-bit in the CAS multiframe alignment word. This bit is logically ored with the contents of register XS1.2

CASM… **CAS Synchronization Mode**

Determines the synchronization mode of the channel associated signaling multiframe alignment.

0… Synchronization is done in accordance to ITU-T G. 732

1… Synchronization is established when two consecutively correct multiframe alignment pattern are found.

EITS… **Enable Internal Time-Slot 0-31 Signaling**

0… Internal signaling in time-slots 0-31 defined via registers RTR1-4 or TTR1-4 is disabled.

1… Internal signaling in time-slots 0-31 defined via registers RTR1-4 or TTR1-4 is enabled.

ITF… **Interframe Time Fill**

Determines the idle (= no data to send) state of the transmit data coming from the signaling controller.

0… Continuous logical ‘1’ is output

1… Continuous FLAG sequences are output (‘01111110’ bit patterns)

RFT1, RFT0…RFIFO Threshold Level

The size of the accessible part of RFIFO can be determined by programming these bits. The number of valid bytes after a RPF interrupt is given in the following table:

RFT1	RFT0	Size of Accessible Part of RFIFO
0	0	32 bytes (RESET value)
0	1	16 bytes
1	0	4 bytes
1	1	2 bytes

The value of RFT1, 0 can be changed dynamically.

– If reception is not running or

– after the current data block has been read, but before the command CMDR.RMC is issued (interrupt controlled data transfer). See **Note**.

Note: It is seen that changing the value of RFT1, 0 is possible even during the reception of one frame. The total length of the received frame can be always read directly in RBCL, RBCH

after a RPF interrupt, except when the threshold is increased during reception of that frame. The real length can then be inferred by noting which bit positions in RBCL are reset by a RMC command (see table below):

RFT1	RFT0	Bit Positions in RBCL Reset by a CMDR.RMC Command
0	0	RBC4 …. 0
0	1	RBC3 … 0
1	0	RBC1,0
1	1	RBC0

Common Configuration Register 3 (READ/WRITE)

Value after RESET: 00_H

	7							0	
CCR3	PRE1	PRE0	EPT	RADD		RCRC	XCRC		(0A)

Note: Unused bits have to be set to logical '0'.

PRE1, PRE0… **Number of Preamble Repetition**

If Preamble transmission is initiated, the Preamble defined via register PRE is transmitted

00…1 times

01…2 times

10…4 times

11…8 times.

EPT… **Enable Preamble Transmission**

This bit enables transmission of a preamble. The preamble is started after Interframe Timefill transmission has been stopped and a new frame is to be transmitted. The preamble consists of a 8-bit pattern repeated a number of times. The pattern is defined via register PRE, the number of repetitions is selected by bits PRE0 and PRE1.

Note: The "Shared Flag" feature is not influenced by preamble transmission. Zero Bit Insertion is disabled during preamble transmission.

RADD… **Receive Address Pushed to RFIFO**

If this bit is set to ‘1’, the received HDLC address information (1 or 2 bytes, depending on the address mode selected via MODE.MDS0) is pushed to RFIFO. This function is applicable in non-auto mode.

RCRC… **Receive CRC ON/OFF**

Only applicable in non-auto mode.

If this bit is set to ‘1’, the received CRC checksum will be written to RFIFO (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO by the status information byte (contents of register RSIS). The received CRC checksum will additionally be checked for correctness. If non-auto mode is selected, the limits for “Valid Frame” check are modified (**refer to RSIS.VFR**).

XCRC… **Transmit CRC ON/OFF**

If this bit is set to ‘1’, the CRC checksum will not be generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO). The transmitted frame will be closed automatically with a closing flag.

Note: The FALC54 does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

Preamble Register (Read/Write)

Value after RESET: 00_H

	7		0	
PRE	PRE7		PRE0	(0B)

PRE0...PRE7... **Preamble Register**

This register defines the pattern which is sent out during preamble transmission (refer to register CCR3). LSB is sent first.

Note: It should be taken into consideration that Zero Bit Insertion is disabled during preamble transmission.

Receive Timeslot Register 1-4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
RTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(0C)
RTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(0D)
RTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(0E)
RTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(0F)

TS0…TS31… **Timeslot Register**

These bits define the received channels (time-slots) to be extracted. Additionally this registers will control the RSIGM marker which can be forced high during the respective time-slots independent of bit CCR1.EITS.
A one in the RTR1-4 bits will sample the corresponding time-slot from the data which are output on pin RDO, if bit CCR1.EITS is set.

Assignments:
TS0 → time-slot 0

.

.

.
TS31 → time-slot 31

0 … Normal operation.

1… The contents of the selected time-slot will be stored in the RFIFO. This function will only become active if bits CCR1.EITS is set.
The corresponding time-slot will be forced high on pin RSIGM.

Transmit Timeslot Register 1-4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
TTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(10)
TTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(11)
TTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(12)
TTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(13)

TS0…TS31… **Transmit Timeslot Register**

These bits define the transmit channels (time-slots) to be inserted. Additionally this registers will control the XSIGM marker which can be forced high during the respective time-slots independent of bit CCR1.EITS.
A one in the TTR1-4 bits will insert the corresponding time-slot in the data received on pin XDI, if bit CCR1.EITS is set.

Assignments:
TS0 → time-slot 0

.

.

.
TS31 → time-slot 31

0 … Normal operation.

1… The contents of the selected time-slot will be inserted in the outgoing data stream. This function will only become active if bits CCR1.EITS is set.
The corresponding time-slot will be forced high on pin XSIGM.

Interrupt Mask Register 0 ... 4

Value after RESET: FF_H, FF_H, FF_H, FF_H, FF_H

	7							0	
IMR0	RME	RFS	T8MS	RMB	CASC	CRC4	SA6SC	RPF	(14)
IMR1		RDO	ALLS	XDU	XMB		XLSC	XPR	(15)
IMR2	FAR	LFA	MFAR	T400MS	AIS	LOS	RAR	RA	(16)
IMR3	ES	SEC	LMFA16	AIS16	RA16	API	SLN	SLP	(17)
IMR4	LFA	FER	CER	AIS	LOS	CVE	SLIP	EBE	(18)

IMR0...IMR4... Interrupt Mask Register

Each interrupt source can generate an interrupt signal at port INT (characteristics of the output stage are defined via register IPC). A ‘1’ in a bit position of IMR0 ... 4 sets the mask active for the interrupt status in ISR0 ... 3. Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they will

– not be displayed in the Interrupt Status Register if bit IPC.VIS is set to ‘0’

– be displayed in the Interrupt Status Register if bit IPC.VIS is set to ‘1’.

*Note: After RESET, all interrupts are **dis**abled.*

Framer Mode Register 0 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR0	XC1	XC0	RC1	RC0	EXTD	ALM	FRS	SIM	(1A)

XC1... XC0… Transmit Code

Serial code transmitter is different programmable from the receiver.

00... NRZ (optical interface)

01... CMI (1T2B + HDB3), (optical interface)

10... AMI (ternary or digital dual rail interface)

11... HDB3 Code (ternary or digital dual rail interface)

RC1... RC0… Receive Code

Serial code receiver is different programmable from the transmitter.

00... NRZ (optical interface)

01... CMI (1T2B+HDB3), (optical interface)

10... AMI (ternary or digital dual rail interface)

11... HDB3 Code (ternary or digital dual rail interface)

EXTD… Extended HDB3 Error Detection

Selects error detection mode.

0… Only double violations are detected.

1… Extended code violation detection: 0000 strings are detected additionally. Thereafter, incrementation of Code Violation Counter CVC is first done after receiving an additional four zeros.

ALM… Alarm Mode

Selects the AIS alarm detection mode.

0 ... The AIS alarm will be detected according to ETS300233.
Detection: An AIS alarm will be detected if the incoming data stream contains less than 3 zeros within a period of 512 bits and a Loss of Frame Alignment is indicated.
Recovery: The alarm will be cleared if 3 or more zeros within 512 bits will be detected or the FAS word is found.

1 ... The AIS alarm will be detected according to ITU-T G.775
Detection: An AIS alarm will be detected if the incoming data stream contains for two consecutive doubleframe periods (1024 bits) less than 3 zeros for each doubleframe period (512 bits).
Recovery: The alarm will be cleared if within two consecutive doubleframe periods 3 or more zeros for each period of 512 bits will be detected.

FRS… Force Resynchronization

A transition from low to high will initiate a resynchronization procedure of the pulse frame and the CRC-multiframe (if enabled via bit FMR2.RFS1) starting directly after the old framing candidate.

SIM… **Alarm Simulation**

0… Normal operation.

1… Initiates internal error simulation of AIS, loss of signal, loss of synchronization, auxiliary pattern indication, slip, framing errors, CRC errors, and code violations. The error counters FEC, CVC, CEC1 will be incremented.

Framer Mode Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR1	MFCS	AFR	ENSA	PMOD	XFS	ECM	IMOD	XAIS	(1B)

MFCS… **Multiframe Force Resynchronization**

Only valid if CRC multiframe format is selected (FMR2.RFS1/0=10).

A transition from low to high will initiate the resynchronization procedure for CRC-multiframe alignment without influencing doubleframe synchronous state. In case, “Automatic Force Resynchronization” (FMR1.AFR) is enabled and multiframe alignment can not be regained, a new search of doubleframe (and CRC multiframe) is automatically initiated.

AFR… **Automatic Force Resynchronization**

Only valid if CRC multiframe format is selected (FMR2.RFS1/0=10).

If this bit is set, a search of doubleframe alignment is automatically initiated if two multiframe patterns with a distance of n $\times$ 2 ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained or command FMR1.MFCS has been issued.

ENSA… **Enable S_a-Bit Access via Register XSA4-8**

Only applicable if FMR1.XFS is set to one.

0… Normal operation. The S_a-bit information will be taken from bits XSW.XY0…4 and written to bits RSW.RY0…4.

1… S_a-bit register access. The S_a-bit information will be taken from the registers XSA4-8. In addition, the received information will be written to registers RSA4-8. Transmitting contents of registers XSA4-8 will be disabled if one of time-slot 0 transparent modes is enabled (XSP.TT0 or TSWM.SA4-8).

PMOD… **PCM Mode**

For E1 application this bit must be set low.

0... PCM30 mode.

1... PCM24 mode.

XFS… **Transmit Framing Select**

Selection of the transmit framing format could be done independent of the receive framing format.

0… Doubleframe format enabled.

1… CRC4-multiframe format enabled.

ECM… **Error Counter Mode**

The function of the error counters will be determined by this bit.

0… Before reading an error counter the corresponding bit in the Disable Error Counter register (DEC) has to be set. In 8 bit access the low byte of the error counter should always be read before the high byte. The error counters will be reset with the rising edge of the corresponding bits in the DEC register.

1… Every second the error counter will be latched and then automatically be reset. The latched error counter state should be read within the next second. Reading the error counter during updating should be avoided.

IMOD… **System Interface Mode**

0… 4 Mbit/s mode.

1… 2 Mbit/s mode.

XAIS… **Transmit AIS Towards Remote End**

Sends AIS via ports XL1, XL2, XOID towards the remote end. The outgoing data stream which could be looped back via the Local Loop to the system interface will not be affected.

Framer Mode Register 2 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR2	RFS1	RFS0	RTM	DAIS	SAIS	PLB	AXRA	ALMF	(1C)

RFS1... RFS0... Receive Framing Select

00 ... Doubleframe format

01 ... Doubleframe format

10 ... CRC4 Multiframe format

11 ... CRC4 Multiframe format with modified CRC4 Multiframe alignment algorithm (Interworking according to ITU-T G.706 Annex B). Setting of FMR3.EXTIW changes the reaction after the 400 msec timeout.

RTM… Receive Transparent Mode

Setting this bit disconnects control of the internal elastic store from the receiver. The elastic store is now in a “free running” mode without any possibility to actualize the time slot assignment to a new frame position in case of re-synchronization of the receiver. This function can be used in conjunction with the “disable AIS to system interface” feature (FMR2.DAIS) to realize undisturbed transparent reception.

DAIS… Disable AIS to System Interface

0… AIS is automatically inserted into the data stream to RDO if FALC54 is in asynchronous state.

1… Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit FMR2.SAIS.

SAIS… Send AIS Towards System Interface

Sends AIS via output RDO towards system interface. This function is not influenced by bit FMR2.DAIS.

PLB… Payload Loopback

0… Normal operation

1... The payload loopback will loop the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received at port XDI, $\overline{\text{SYPX}}$ and XMFS will be ignored. With XSP.TT0=1 timeslot 0 will also be looped. If XSP.TT0=0 timeslot 0 will be generated internally. AIS is sent immediately on port RDO by setting the FMR2.SAIS bit.

AXRA… **Automatic Transmit Remote Alarm**

0 ... Normal operation

1 ... The Remote Alarm bit will be automatically set in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit will be reset. Additionally in multiframe format FMR2.RFS1=1 and FMR3.EXTIW =1 and the 400 msec timeout has elapsed, the remote alarm bit will be active in the outgoing data stream. In multiframe synchronous state the outgoing remote alarm bit is cleared.

ALMF… **Automatic Loss of Multiframe**

0 ... Normal operation

1 ... The receiver will search a new basic- and multiframing if more than 914 CRC errors have been detected in a time interval of one second. The internal 914 CRC error counter will be reset if the multiframe synchronization is found. Incrementing the counter is only enabled in the multiframe synchronous state.

Channel Loop Back (Read/Write)

Value after RESET: 00_H

SFM… **Single Frame Mode**

Setting this bit reduces the receive speech memory from two to one frame length. In this case, clocks SCLKR and RCLK have to be phase locked to avoid slip conditions. However, slip detection still works but without any influence on data transmission.

ECLB… **Enable Channel Loop Back**

0 ... Disables the channel loop back.

1 ... Enables the channel loop back selected by this register.

CLA4…CLA0… **Channel Address For Loop Back**

CLA = 0…31 selects the channel.

During looped back the contents of the assigned outgoing channel at ports XL1/XDOP/XOID and XL2/XDON is equal to the idle channel code programmed at register IDLE.

Transmit Service Word Pulseframe (Read/Write)

Value after RESET: 00_H

	7							0	
XSW	XSIS		XRA	XY0	XY1	XY2	XY3	XY4	(1E)

XSIS… **Spare Bit For International Use**

First bit of the service word. Only significant in doubleframe format. If not used, this bit should be fixed to '1'. If one of the time-slot 0 transparent modes is enabled (bit XSP.TT0, or TSWM.TSIS), bit XSW.XSIS will be ignored.

XRA… **Transmit Remote Alarm**

0… Normal operation.

1… Sends remote alarm towards remote end by setting bit 3 of the service word. If time-slot 0 transparent mode is enabled via bit XSP.TT0 or TSWM.TRA bit is set, bit XSW.XRA will be ignored.

XY0…XY4… **Spare Bits For National Use (Y-Bits, S_n-Bits, S_a-Bits)**

These bits are inserted in the service word of every other pulseframe if S_a-bit register access is disabled (FMR1.ENSA = 0). If not used, they should be fixed to '1'.

If one of the time-slot 0 transparent modes is enabled (bit XSP.TT0 or TSWM.TSA4-8), bits XSW.XY0…4 will be ignored.

Transmit Spare Bits (Read/Write)

Value after RESET: 00_H

	7							0	
XSP	XAP	CASEN	TT0	EBP	AXS	XSIF	XS13	XS15	(1F)

XAP… **Transmit Auxiliary Pattern Towards Remote End**

0… Normal operation.

1… A one in this bit position will cause the transmitter to send an alternating pattern 101010... towards the remote end. FMR1.XAIS = 1 will overwrite the alternating pattern by a continuous one bitstream.

CASEN… **Channel Associated Signaling Enable**

0… Normal operation.

1… A one in this bit position will cause the transmitter to send the CAS information stored in the XS1-16 registers in the corresponding time slots.

TT0… **Time-Slot 0 Transparent Mode**

0… Normal operation.

1… All information for time-slot 0 at port XDI will be inserted in the outgoing pulseframe. All internal information of the FALC54 (framing, CRC, S_a/S_i bit signaling, remote alarm) will be ignored. This function is mainly useful for system test applications (test loops). Priority sequence of transparent modes: XSP.TTO > TSWM.

EBP… **E- Bit Polarity**

0… In the basic - or multiframe asynchronous state the E-bit will be set to zero.

1… In the basic - or multiframe asynchronous state the E-bit will be set to one.

If automatic transmission of sub-multiframe status is enabled by setting bit XSP.AXS and the receiver has been lost multiframe synchronization, the E bit with the programmed polarity will be inserted automatically in S_i-bit position of every outgoing CRC multiframe (under the condition that time-slot 0 transparent mode and transparent Si bit in Service word are both disabled).

AXS… **Automatic Transmission of Submultiframe Status**

Only applicable to CRC multiframe.

0… Normal operation.

1… Information of submultiframe status bits RSP.SI1 and RSP.SI2 will be automatically inserted in S_i -bit positions of the outgoing CRC multiframe (RSP.SI1 $\rightarrow$ S_i -bit of frame 13; RSP.SI2 $\rightarrow$ S_i-bit of frame 15). Contents of XSP.XS13 and XSP.XS15 will be ignored. If one of the time-slot 0 transparent modes XSP.TT0 or TSWM.TSIS is enabled, bit XSP.AXS has no function.

XSIF… Transmit Spare Bit For International Use (FAS Word)

First bit in the FAS word. Only significant in doubleframe format. If not used, this bit should be fixed to ‘1’. If one of the time-slot 0 transparent modes is enabled (bits XSP.TT0, or TSWM.TSIF), bit XSP.XSIF will be ignored.

XS13… Transmit Spare Bit (Frame 13, CRC-Multiframe)

First bit in the service word of frame 13 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to ‘1’. The information of XSP.XS13 will be shifted into internal transmission buffer with beginning of the next following transmitted CRC multiframe.

If automatic transmission of submultiframe status is enabled via bit XSP.AXS, or, if one of the time-slot 0 transparent modes XSP.TT0 or TSWM.TSIS is enabled, bit XSP.XS13 will be ignored.

XS15… Transmit Spare Bit (Frame 15, CRC-Multiframe)

First bit in the service word of frame 15 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to ‘1’. The information of XSP.XS15 will be shifted into internal transmission buffer with beginning of the next following transmitted CRC multiframe.

If automatic transmission of submultiframe status is enabled via bit XSP.AXS, or, if one of the time-slot 0 transparent modes XSP.TT0 or TSWM.TSIF is enabled, bit XSP.XS15 will be ignored.

Transmit Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
XC0	SA8E	SA7E	SA6E	SA5E	SA4E	XCO2	XCO1	XCO0	(20)

SA8E…SA4E SA Bit Signaling Enable

0… Standard operation.

1… Setting this bit it will be possible to send / receive a LAPD protocol in any combination of the SA8- SA4 bit positions in the outgoing / incoming data stream. The on chip signaling controller has to be configured in the HDLC/LAPD mode. In transmit direction together with these bits the TSWM.TSA8-4 bits must be set to enable transmission to the remote end transparently through the FALC.

XCO2…XCO0… Transmit Clock Slot Offset

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse at port $\overline{\text{SYPX}}$ is active (see **figure 26**).

Transmit Control 1 (Read/Write)

Value after RESET: 00_H

	7				0	
XC1	XCOS		XTO5		XTO0	(21)

XCOS… Transmit Clock Offset Shift

0… The delay T between the beginning of time-slot 0 and the initial edge of SCLKX (after $\overline{\text{SYPX}}$ goes active) is an even number in the range from 0 to 1022 SCLKX cycles.

1… The delay T is an odd number in the range from 1 to 1023 SCLKX cycles.

XTO5…XTO0… Transmit Time-Slot Offset

Initial value loaded into the transmit time-slot counter at the trigger edge of SCLKX when the synchronous pulse at port $\overline{\text{SYPX}}$ is active (see **figure 26**).

Receive Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
RC0	RCOS	SICS	CRCI	XCRCI	RDIS	RCO2	RCO1	RCO0	(22)

RCOS… Receive Clock Offset Shift

0… The delay T between the beginning of time-slot 0 and the initial edge of SCLKR (after $\overline{\text{SYPR}}$ goes active) is an even number in the range from 0 to 1022 SCLKR cycles.

1… The delay T is an odd number in the range from 1 to 1023 SCLKR cycles.

SICS… **System Interface Channel Select**

Only applicable if bit FMR1.IMOD (4 MHz system interface) is set.

0… Received data is output on port RDO in the first channel phase. Data in the second channel phase is tri-stated. Data on pin XDI is sampled only in the first channel phase. Data in the second channel phase is ignored.

1… Data on port RDO is output in the second channel phase. The first channel phase is tri-stated. Sampling of data from the system highway is done in the second channel phase.

CRCI… **Automatic CRC4 Bit Inversion**

If set, all CRC bits of one outgoing submultiframe are inverted in case a CRC error is flagged for the previous received submultiframe. This function is logically ORed with RC0.XCRCI.

XCRCI… **Transmit CRC4 Bit Inversion**

If set, the CRC bits in the outgoing data stream are inverted before transmission. This function is logically ORed with RC0.CRCI.

RDIS… **Receive Data Input Sense**

0… Inputs: RDIP, RDIN active low, input ROID is active high

1… Inputs: RDIP, RDIN active high, input ROID is active low

RCO2…RCO0… **Receive Clock-Slot Offset**

Initial value which is loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active (see **figure 25**).

Receive Control 1 (Read/Write)

Value after RESET: 00_H

	7			0	
RC1	SWD	ASY4	RTO5	RTO0	(23)

SWD… **Service Word Condition Disable**

0… Standard operation. Three or four consecutive incorrect service words (depending on bit RC1.ASY4) will cause loss of synchronization.

1… Errors in service words have no influence when in synchronous state. However, they are used for the resynchronization procedure.

ASY4… Select Loss of Sync Condition

0… Standard operation. Three consecutive incorrect FAS words or three consecutive incorrect service words will cause loss of synchronization.

1… Four consecutive incorrect FAS words or four consecutive incorrect service words will cause loss of synchronization. The service word condition may be disabled via bit RC1.SWD.

RTO5…RTO0… Receive Time-Slot Offset

Initial value which is loaded into the receive time-slot counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active (see **figure 25**).

Transmit Pulse-Mask 2...0 (Read/Write)

Value after RESET: $9C_H$, 03_H, 00_H

	7							0	
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00	(24)
XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13	(25)
XPM2	XLHP	XLT	DAXLT		XP34	XP33	XP32	XP31	(26)

The transmit pulse shape which is defined in ITU-T G.703 will be output on pins XL1 and XL2. The level of the pulse shape can be programmed via registers XPM2-0 to create a custom waveform. In order to get an optimized pulse shape for the external transformers each pulse shape will be internally devided into four sub pulse shapes. In each sub pulse shape a programmed 5 bit value will define the level of the analog voltage on pins XL1/2. Together four 5 bit values have to be programmed to form one complete transmit pulse shape. The four 5 bit values will be sent in the following sequence:

XP04-00: First pulse shape level
XP14-10: Second pulse shape level
XP24-20: Third pulse shape level
XP34-30: Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM2-0 will change the amplitude of the differential voltage on XL1/2 by approximately 110 mV.
Example: 120 Ω interface and wired as shown in **figure 15**.

XPM04-00: 1DH
XPM14-10: 1DH
XPM24-20: 00H
XPM34-30: 00H

Programming values for XPM0-2: BD_H, 03_H, 00_H

XLHP … **Transmit Line High Power**

0 ... Normal operation.

1 ... With this bit the output current capability of the transmit line XL1 and XL2 can be influenced. Connecting low impedances to the outputs XL1/XL2 this bit should be set to one to avoid instable pulse shapes. Setting this bit has no influence on the voltage levels of the pulse shape.

XLT… **Transmit Line Tri-state**

0… Normal operation

1… Transmit line XL1/XL2 or XDOP/XDON are switched into high impedance state. If this bit is set the transmit line monitor status information will be frozen.

DAXLT... **Disable Automatic Tristating of XL1/2**

0... Normal operation. If a short is detected on pins XL1/2 the transmit line monitor will set the XL1/2 outputs into a high impedance state.

1... If a short is detected on XL1/2 pins automatic setting these pins into a high impedance (by the XL-monitor) state will be disabled.

Transparent Service Word Mask (Read/Write)

Value after RESET: 00_H

	7							0	
TSWM	TSIS	TSIF	TRA	TSA4	TSA5	TSA6	TSA7	TSA8	(27)

TSWM7…TSWM0…Transparent Service Word Mask

TSIS… Transparent Si Bit in Service Word

0… The SI Bit will be generated internally.

1… The SI Bit in the service word will be taken from port XDI and transparently passed through the FALC54 without any changes. The internal information of the FALC54 (register XSW) will be ignored.

TSIF… Transparent Si Bit in FAS Word

0… The SI Bit will be generated internally.

1… The SI Bit in the FAS word will be taken from port XDI and routed transparently through the FALC54 without any changes. The internal information of the FALC54 (register XSW) will be ignored.

TRA… Transparent Remote Alarm

0… The Remote Alarm Bit will be generated internally.

1… The A Bit will be taken from port XDI and routed transparently through the FALC54 without any changes. The internal information of the FALC54 (register XSW) will be ignored.

TSA4…TSA8... Transparent SA4...8 Bit

0… The SA4-8 bit will be generated internally.

1… The SA4-8 bit will be taken from port XDI or from the internal signaling controller if enabled and transparently passed through the FALC54 without any changes. The internal information of the FALC54 (registers XSW and XSA4-8) will be ignored.

Idle Channel Code Register (Read/Write)

Value after RESET: 00_H

	7							0	
IDLE	IDL7							IDL0	(29)

IDL7…IDL0… Idle Channel Code

If channel loop back is enabled by programming LOOP.ECLB=1, the contents of the assigned outgoing channel at ports XL1/XL2 resp. XDOP/XDON is set equal to the idle channel code selected by this register.

Additionally, the specified pattern overwrites the contents of all channels selected via the idle channel registers ICB1…ICB4. IDL7 will be transmitted first.

Transmit SA4-8 Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H, 00_H

	7							0	
XSA4	XS47	XS46	XS45	XS44	XS43	XS42	XS41	XS40	(2A)
XSA5	XS57	XS56	XS55	XS54	XS53	XS52	XS51	XS50	(2B)
XSA6	XS67	XS66	XS65	XS64	XS63	XS62	XS61	XS60	(2C)
XSA7	XS77	XS76	XS75	XS74	XS73	XS72	XS71	XS70	(2D)
XSA8	XS87	XS86	XS85	XS84	XS83	XS82	XS81	XS80	(2E)

XSA8…XSA4… Transmit S_a-Bit Data

The Sa-bit register access is enabled by setting bits FMR1.XFS = 1 and FMR1.ENSA = 1. With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers XSA4-8 will be copied into a shadow register. The contents will subsequently sent out in the service words of the next outgoing CRC multiframe (or doubleframes) if none of the time-slot 0 transparent modes is enabled. XS40 will be sent out in bit position 4 in frame 1, XS47 in frame 15. The transmit multiframe begin interrupt XMB request that these registers should be serviced. If requests for new information are ignored, current contents will be repeated.

Framer Mode Register 3 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR3					CMI	SA6SY	CFRZ	EXTIW	2F

CMI… **Select CMI Precoding**

Only valid if CMI code (FMR0.XC1/0=01) is selected. This bit defines the CMI precoding and influences only the transmit data and not the receive data.

0… CMI with HDB3 precoding

1… CMI without HDB3 precoding

SA6SY… **Receive SA6 Access Synchron Mode**

Only valid if multiframe format (FMR2.RFS1/0=1x) is selected.

0… The detection of the predefined SA6 bit pattern (refer to chapter SA6 Bit Detection according to ETS 300233) is done independently of the multiframe synchronous state.

1… The detection of the SA6 bit pattern is done synchronously to the multiframe.

CFRZ… **Enable CAS Freeze Output**

This bit selects the function of pin RFSPQ.

0… The receive frame synchron pulse is output on pin RFSPQ.

1… The synchronous status of the integrated CAS controller (FRS1.TS16LFA) is output on pin RFSPQ. If the CAS synchronizer lost its synchronization this pin is set high.

EXTIW… **Extended CRC4 to Non CRC4 Interworking**

Only valid in multiframe format. This bit selects the reaction of the synchronizer after the 400 msec timeout has been elapsed and starts transmitting a remote alarm if FMR2.AXRA is set.

0… The CRC4 to Non CRC4 interworking is done as described in ITU-T G. 706 Annex B.

1… The interworking is done according to ITU-T G. 706 with the exception that the synchronizer will still search the multiframing even if the 400 msec timer is expired. Switching into doubleframe format is disabled. If FMR2.AXRA is set the remote alarm bit will be active in the outgoing data stream.

Idle Channel Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
ICB1	IC0	IC1	IC2	IC3	IC4	IC5	IC6	IC7	(30)
ICB2	IC8	IC9	IC10	IC11	IC12	IC13	IC14	IC15	(31)
ICB3	IC16	IC17	IC18	IC19	IC20	IC21	IC22	IC23	(32)
ICB4	IC24	IC25	IC26	IC27	IC28	IC29	IC30	IC31	(33)

IC1…IC32… **Idle Channel Selection Bits**

These bits define the channels (time-slots) of the outgoing PCM frame to be altered.
Assignments:
IC0 → time-slot 0
IC1 → time-slot 1

IC31 → time-slot 31

0… Normal operation.

1… Idle channel mode. The contents of the selected time-slot is overwritten by the idle channel code defined via register IDLE.

Note: Although time-slot 0 can be selected via bit IC0, its contents is only altered if the transparent mode is selected (XSP.TT0).

Line Interface Mode 0 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM0	XFB	XDOS	SCL1	SCL0	EQON	ELOS	LL	MAS	(34)

XFB… **Transmit Full Bauded Mode**

0…Output signals XDOP/XDON are half bauded (normal operation).

1…Output signals XDOP/XDON are full bauded.

Note: If CMI coding is selected (FMR0.XC1/0=01) this bit has to be cleared.

XDOS… **Transmit Data Out Sense**

0… Output signals XDOP/XDON are active low. Output XOID is active high (normal operation).

1… Output signals XDOP/XDON are active high. Output XOID is active low.

Note: If CMI coding is selected (FMR0.XC1/0=01) this bit has to be cleared.

SCL1 ... SCL0… **Select Clock Output**

00… Output frequency at pin CLKX: 2048 kHz active high

01… Output frequency at pin CLKX: 2048 kHz active low

10… Output frequency at pin CLKX: 4096 kHz active high

11… Output frequency at pin CLKX: 4096 kHz active low

EQON… **Receive Equalizer On**

0… 6 dB Receiver: Equalizer off

1… 18 dB Equalizer on

ELOS **Enable Loss of Signal**

0... Normal operation. The extracted receive clock is output via pin RCLK.

1... In case of loss of signal (FRS0.LOS=1) the RCLK is set high. If FRS0.LOS=0 the received clock is output via RCLK.

LL… **Local Loop**

0… Normal operation

1… Local loop active. The local loopback mode disconnects the receive lines RL1/RL2 resp. RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. The unipolar bit stream will be undisturbed transmitted on the line. Receiver and transmitter coding must be identical.

MAS… **Master Mode**

0… Slave mode

1… Master mode on. If this bit is set and the SYNC pin is connected to V_{SS} the FALC54 works as a master for the system. The internal DCO's of the jitter attenuator are centered and the system clocks which are output via CLK8M/CLKX are stable (divided from the DCO frequencies). If a clock (2.048 MHz) is detected at the SYNC pin the FALC54 synchronizes automatically to this clock. The production tolerance is approximately ± 30 ppm of the crystal frequency if C_{Load} = 15 pF.

Line Interface Mode 1 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM1	EFSC	RIL2	RIL1	RIL0		JATT	RL	DRS	(35)

EFSC… **Enable Frame Synchronization Pulse**

0 ... The transmit clock is output via pin XCLK.

1 ... Pin XCLK provides a 8 kHz frame synchronization pulse which is active high for one 2 MHz cycle (pulse width = 488 ns).

RIL2…RIL0… **Receive Input Threshold**

Only valid if analog line interface is selected (LIM1.DRS=0).

No signal will be declared if the voltage between pins RL1 and RL2 drops below the limits programmed via bits RIL2-0 and the received data stream has no transition for a period defined in the PCD register.

The threshold where no signal will be declared is programmable via the RIL2-0 bits.

Differential input voltage between pins RL1/2:

000 = 1.36 V
001 = 1.04 V
010 = 0.84 V
011 = 0.62 V
100 = 0.43 V
101 = 0.32 V
110 = 0.22 V
111 = Not assigned

JATT…RL... Transmit Jitter Attenuator / Remote Loop

00 ... Normal operation. The transmit jitter attenuator is disabled. Transmit data will bypass the buffer.

01 ... Remote Loop active without transmit jitter attenuator enabled. Transmit data will bypass the buffer.

10 ... Transmit Slicer active. Transmit data received on port XDI from the system highway will be first written into the transmit jitter attenuator and then sent jitter free on ports XL1/2 or XDOP/N or XOID.

11 ... Remote Loop and jitter attenuator active. Received data from pins RL1/2 or RDIP/N or ROID will be sent jitter free on ports XL1/2 or XDOP/N or XOID.

DRS… Dual Rail Select

0 ... The ternary interface is selected. Multifunction ports RL1/2 and XL1/2 become analog in/outputs.

1 ... The digital dual rail interface is selected. Received data is latched on multifunction ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Pulse Count Detection Register (Read/Write)

Value after RESET: 00_H

	7						0	
PCD	PCD7						PCD0	(36)

PCD7…PCD0… Pulse Count Detection

A LOS alarm will be detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable via the PCD register and can be calculated as follows:
T= 16(N+1) ; with 0 =< N =< 255.

The maximum time is: 256 x 16 x 488 ns = 2 ms. Every detected pulse will reset the internal pulse counter. The counter will be clocked with the receive clock RCLK.

Pulse Count Recovery (Read/Write)

Value after RESET: 00_H

	7							0	
PCR	PCR7							PCR0	(37)

PCR7…PCR0… Pulse Count Recovery

A LOS alarm will be cleared if a pulse density is detected in the received bit stream. The number of pulses M which must occur in the predefined PCD time interval is programmable via the PCR register and can be calculated as follows:

M = N+1 ; with 0 =< N =< 255.

The time interval starts with the first detected pulse transition. With every received pulse a counter will be incremented and the actual counter is compared with the contents of PCR register. If the pulse number >= the PCR value the LOS alarm will be reset otherwise the alarm will still be active. In this case the next detected pulse transition will start a new time interval.

Additional Loss of Signal recovery conditions may be selected by register LIM2.LOS2/1.

Line Interface Mode 2 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM2							LOS2	LOS1	(38)

LOS2/1… Loss of Signal Recovery condition

00… The LOS alarm will be cleared if the predefined pulse density by register PCR is detected during the time interval which is defined by register PCD.

01… Additionally to the recovery condition described above a LOS alarm will only be cleared if the pulse density is fulfilled and no more than 15 contiguous zeros are detected during the recovery interval.

10… Clearing a LOS alarm will be done if the pulse density is fulfilled and no more than 99 contiguous zeros are detected during the recovery interval.

11… Not assigned

Disable Error Counter (Write)

Value after RESET: 00_H

	7							0	
DEC			DCEC3	DCEC2	DCEC1	DEBC	DCVC	DFEC	(60)

DCEC3… **Disable CRC Error Counter 3**

Only valid if FMR1.ECM is reset.

This bit has to be set before reading the CRC error counter 3. It will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of this bit the CRC error counter is latched and then cleared.

DCEC2… **Disable CRC Error Counter 2**

Only valid if FMR1.ECM is reset.

This bit has to be set before reading the CRC error counter 2. It will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of this bit the CRC error counter is latched and then cleared.

DCEC1… **Disable CRC Error Counter 1**

Only valid if FMR1.ECM is reset.

This bit has to be set before reading the CRC error counter 1. It will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of this bit the CRC error counter is latched and then cleared.

DEBC… **Disable E-Bit Error Counter**

Only valid if FMR1.ECM is reset.

This bit has to be set before reading the E-Bit error counter. It will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of this bit the E-Bit error counter is latched and then cleared.

DCVC… **Disable Code Violation Counter**

Only valid if FMR1.ECM is reset.

This bit has to be set before reading the code violation counter. It will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of this bit the code violation counter is latched and then cleared.

DFEC… **Disable Framing Error Counter**

Only valid if FMR1.ECM is reset.

This bit has to be set before reading the framing error counter. It will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of this bit the framing error counter is latched and then cleared.

Transmit CAS Register (Write)

Value after RESET: not defined

	7							0	
XS1	0	0	0	0	X	Y	X	X	(70)
XS2	A1	B1	C1	D1	A16	B16	C16	D16	(71)
XS3	A2	B2	C2	D2	A17	B17	C17	D17	(72)
XS4	A3	B3	C3	D3	A18	B18	C18	D18	(73)
XS5	A4	B4	C4	D4	A19	B19	C19	D19	(74)
XS6	A5	B5	C5	D5	A20	B20	C20	D20	(75)
XS7	A6	B6	C6	D6	A21	B21	C21	D21	(76)
XS8	A7	B7	C7	D7	A22	B22	C22	D22	(77)
XS9	A8	B8	C8	D8	A23	B23	C23	D23	(78)
XS10	A9	B9	C9	D9	A24	B24	C24	D24	(79)
XS11	A10	B10	C10	D10	A25	B25	C25	D25	(7A)
XS12	A11	B11	C11	D11	A26	B26	C26	D26	(7B)
XS13	A12	B12	C12	D12	A27	B27	C27	D27	(7C)
XS14	A13	B13	C13	D13	A28	B28	C28	D28	(7D)
XS15	A14	B14	C14	D14	A29	B29	C29	D29	(7E)
XS16	A15	B15	C15	D15	A30	B30	C30	D30	(7F)

Transmit CAS Register 1-16

The transmit CAS register access is enabled by setting bit XSP.CASEN = 1. Each register except XS1 contains the CAS bits for two timeslots. With the transmit multiframe begin ISR1.XMB the contents of these registers will be copied into a shadow register. The contents will subsequently sent out in the timeslots 16 of the outgoing data stream.

XS1.7 will be sent out first and XS16.0 will be sent last. The transmit multiframe begin interrupt (XMB) requests that these registers should be serviced. If requests for new information are ignored, current contents will be repeated. XS1 has to be programmed with the multiframe pattern. This pattern should always stay low otherwise the remote end will lose its synchronization. With setting the Y-bit a remote alarm will be transmitted to the far end. The Y-bit is logically ored with bit CCR1.XTS16RA.

The X bits (Spare bits) should be set to one if they are not used.

3.1.2 Status Register Address Arrangement

Address	Write	Type	Comment
00/01	RFIFO	R	Receive FIFO
4C	FRS0	R	Framer Receive Status 0
4D	FRS1	R	Framer Receive Status 1
4E	RSW	R	Receive Service Word
4F	RSP	R	Receive Spare Bits
50	FECL	R	Framing Error Counter Low
51	FECH	R	Framing Error Counter High
52	CVCL	R	Code Violation Counter Low
53	CVCH	R	Code Violation Counter High
54	CEC1L	R	CRC Error Counter 1 Low
55	CEC1H	R	CRC Error Counter 1 High
56	EBCL	R	E-Bit Error Counter Low
57	EBCH	R	E-Bit Error Counter High
58	CEC2L	R	CRC Error Counter 2 Low
59	CEC2H	R	CRC Error Counter 2 High
5A	CEC3L	R	CRC Error Counter 3 Low

E1: Status Register Address Arrangement (cont'd)

Address	Write	Type	Comment
5B	CEC3H	R	CRC Error Counter 3 High
5C	RSA4	R	Receive SA4 Bit Register
5D	RSA5	R	Receive SA5 Bit Register
5E	RSA6	R	Receive SA6 Bit Register
5F	RSA7	R	Receive SA7 Bit Register
60	RSA8	R	Receive SA8 Bit Register
61	RSA6S	R	Receive SA6 Bit Status Register
62	TSR0	R	Manufacturer Test Register
63	TSR1	R	Manufacturer Test Register
64	SIS	R	Signaling Status Register
65	RSIS	R	Receive Signaling Status Register

E1: Status Register Address Arrangement (cont'd)

Address	Write	Type	Comment
66	RBCL	R	Receive Byte Control Low
67	RBCH	R	Receive Byte Control High
68	ISR0	R	Interrupt Status Register 0
69	ISR1	R	Interrupt Status Register 1
6A	ISR2	R	Interrupt Status Register 2
6B	ISR3	R	Interrupt Status Register 3
6C			
6D			
6E	GIS	R	Global Interrupt Status
6F	VSTR	R	Version Status
70	RS1	R	Receive CAS Register 1
71	RS2	R	Receive CAS Register 2
72	RS3	R	Receive CAS Register 3
73	RS4	R	Receive CAS Register 4
74	RS5	R	Receive CAS Register 5
75	RS6	R	Receive CAS Register 6
76	RS7	R	Receive CAS Register 7
77	RS8	R	Receive CAS Register 8
78	RS9	R	Receive CAS Register 9
79	RS10	R	Receive CAS Register 10
7A	RS11	R	Receive CAS Register 11
7B	RS12	R	Receive CAS Register 12
7C	RS13	R	Receive CAS Register 13
7D	RS14	R	Receive CAS Register 14
7E	RS15	R	Receive CAS Register 15
7F	RS16	R	Receive CAS Register 16

Receive FIFO (Read) RFIFO

	7							0	
RFIFO	RF7							RF0	(00/01)

Reading data from RFIFO can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface.

The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT 1 … 0 (RFIFO threshold level). It can be reduced from 32 bytes (RESET value) down to 2 bytes (four values: 32, 16, 4, 2 bytes).

Data Transfer

Up to 32 bytes/16 words of received data can be read from the RFIFO following an RPF or an RME interrupt.
RPF Interrupt: A fixed number of bytes/words to be read (32, 16, 4, 2 bytes). The message is not yet complete.

RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers.

RFIFO is released by issuing the “Receive Message Complete” command (RMC).

Framer Receive Status Register 0 (Read)

	7							0	
FRS0	LOS	AIS	LFA	RRA	AUXP	NMF	LMFA		(4C)

LOS… Loss of Signal

Detection:
This bit is set when the incoming signal has “no transitions” (analog interface) or logical zeros (dig. interface) in a time interval of T consecutive pulses, where T is programmable via PCD register.
Total account of consecutive pulses: 16 < T < 4096.

Analog interface: The receive signal level where “no transition” will be declared is defined by the programmed value of LIM1.RIL2-0.

Recovery:
Analog interface: The bit will be reset when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL2-0) for at least M pulse periods defined by register PCR in the PCD time interval.
Digital interface: The bit will be reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval.

With the rising edge of this bit an interrupt status bit (ISR2.LOS) will be set. For additionally recovery conditions refer also to register LIM2.LOS2/1.
The bit will also be set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

AIS… **Alarm Indication Signal**

The function of this bit is determined by FMR0.ALM.

FMR0.ALM = 0: This bit is set when two or less zeros in the received bit stream are detected in a time interval of 250 µs and the FALC54 is in the asynchronous state (FRS0.LFA = 1). The bit will be reset when no alarm condition is detected (ETSI).

FMR0.ALM = 1: This bit is set when the incoming signal has two or less Zeros in each of two consecutive double frame periods(512 bits). This bit will be cleared when each of two consecutive doubleframe periods contain three or more Zeros or when the frame alignment signal FAS has been found. (ITU-T: G.775)

The bit will also be set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

With the rising edge of this bit an interrupt status bit (ISR2.AIS) will be set.

LFA… **Loss of Frame Alignment**

This bit is set after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (can be disabled). With the rising edge of this bit an interrupt status bit (ISR2.LFA) will be set. The specification of the loss of sync conditions is done via bits RC1.SWD and RC1.ASY4. After loss of synchronization, the frame aligner will resynchronize automatically.

The following conditions have to be detected to regain synchronous state:
– The presence of the correct FAS word in frame n.
– The presence of the correct service word (bit 2 = 1) in frame n + 1.
– For a second time the presence of a correct FAS word in frame n + 2.

The bit is cleared when synchronization has been regained (directly after the second correct FAS word of the procedure described above has been received).

If the CRC-multiframe structure is enabled by setting bit FMR2.RFS1, multiframe alignment is assumed to be lost if pulse-frame synchronization has been lost. The resynchronization procedure for multiframe alignment starts after the bit FRS0.LFA has been cleared.

Multiframe alignment has been regained if two consecutive CRC-multiframes have been received without a framing error (refer to FRS0.LMFA).

The bit will be set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

If bit FRS0.LFA is cleared a loss of frame alignment recovery interrupt status ISR2.FAR will be generated.

RRA… Receive Remote Alarm

Set if bit 3 of the received service word is set. An alarm interrupt status ISR2.RA can be generated if the alarm condition is detected.

FRS0.RRA will be cleared when no alarm is detected. At the same time a remote alarm recovery interrupt status ISR2.RAR will be generated.

The bit RSW.RRA has the same function.

Both status and interrupt status bits will be set during alarm simulation.

AUXP… Auxiliary Pattern Indication

This bit is set when 254 or more ‘10’ are received in a time interval of 250 µs and the frame alignment is lost FRS0.LFA = 1. An interrupt status ISR3.API will be generated if this bit is set.

The bit will be reset when no auxiliary pattern condition is detected. The bit will also be set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

NMF… **No Multiframe Alignment Found**

This bit is only valid if the CRC4 interworking is selected (FMR2.RFS1/0 = 11). Set if the multiframe pattern could not be detected in a time interval of 400 msec after the framer has reached the doubleframe synchronous state. The receiver is then automatically switched to doubleframe format.

This bit is reset if the basic framing has been lost.

LMFA… **Loss of Multiframe Alignment**

Not used in doubleframe format (FMR2.RFS1 = 0). In this case, set to logical '1'.

In CRC-multiframe mode (FMR2.RFS1 = 1), this bit is set

– if force resynchronization is initiated by setting bit FMR0.FRS, or

– if multiframe force resynchronization is initiated by setting bit FMR1.MFCS, or

– if pulseframe alignment has been lost (FRS0.LFA).

It is reset if two CRC-multiframes have been received at an interval of $n \times 2$ ms (n = 1, 2, 3…) without a framing error.

If bit FRS0.LMFA is cleared a loss of multiframe alignment recovery interrupt status ISR2.MFAR will be generated.

Framer Receive Status Register 1 (Read)

	7							0	
FRS1		TS16RA	TS16LOS	TS16AIS	TS16LFA		XLS	XLO	(4D)

TS16RA… **Receive Timeslot 16 Remote Alarm**

This bit contains the actual information of the received remote alarm bit RS1.2 in time-slot 16. Setting and resetting of this bit will cause an interrupt status change ISR3.RA16.

TS16LOS… **Receive Timeslot 16 Loss of Signal**

This bit is set if the incoming TS16 data stream contains always zeros for at least 16 contiguously received time-slots. A one in a time-slot 16 will reset this bit.

TS16AIS… Receive Timeslot 16 Alarm Indication Signal

The detection of the alarm indication signal in timeslot 16 is according to ITU-T G.775.

This bit is set if the incoming TS16 contains less than 4 zeros in each of two consecutive TS16 multiframe periods. This bit will be cleared if two consecutive received CAS multiframe periods contains more than 3 zeros or the multiframe pattern was found in each of them. This bit will be cleared if TS0 synchronization is lost.

TS16LFA… Receive Timeslot 16 Loss of Multiframe Alignment

0 ... The CAS controller is in synchronous state after frame alignment is accomplished.

1 ... This bit is set if the framing pattern ‘0000’ in 2 consecutive CAS multiframes were not found or in all TS16 of the preceding multiframe all bits were reset. An interrupt ISR3.LMFA16 will be generated.

XLS… Transmit Line Short

Significant only if the ternary line interface is selected by LIM1.DRS=0.

0… Normal operation. No short is detected.

1… The XL1 and XL2 are shortend for at least 32 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high impedance state if bit XPM2.DAXLT is reset. After 32 consecutive pulse periods the outputs XL1/2 are activated again until the first pulse is transmitted. If a short between XL1/2 is still further active the outputs XL1/2 are in high impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit will be reset. With any change of this bit an interrupt ISR1.XLSC will be generated. In case of XPM2.XLT is set this bit will be frozen.

XLO… Transmit Line Open

0… Normal operation

1… This bit will be set if at least 32 consecutive zeros were sent via pins XL1/XL2 resp. XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC will be set. In case of XPM2.XLT is set this bit will be frozen.

Receive Service Word Pulseframe (Read)

	7							0	
RSW	RSI	1	RRA	RYO	RY1	RY2	RY3	RY4	(4E)

RSI… **Receive Spare Bit for International Use**

First bit of the received service word. It is fixed to one if CRC-multiframe mode is enabled.

RRA… **Receive Remote Alarm**

Equivalent to bit FRS0.RRA.

RY0…RY4… **Receive Spare Bits for National Use (Y-Bits, Sn-Bits, Sa-Bits)**

Receive Spare Bits/Additional Status (Read)

	7							0	
RSP	SI1	SI2				RSIF	RS13	RS15	(4F)

SI1…SI2… **Submultiframe Error Indication 1, 2**

Not valid if doubleframe format is enabled. In this case, both bits are set to logical ‘1’.

When using CRC-multiframe format these bits are set to

0… If multiframe alignment has been lost, or
if the last multiframe has been received with CRC error(s). SI1 flags a CRC error in last sub-multiframe 1, SI2 flags a CRC error in last sub-multiframe 2.

1 ... If at multiframe synchronous state last assigned sub-multiframe has been received without a CRC error.

Both flags will be actualized with beginning of every received CRC multiframe.

If automatic transmission of sub-multiframe status is enabled by setting bit XSP.AXS, above status information will be inserted automatically in S_i -bit position of every outgoing CRC multiframe (under the condition that time-slot 0 transparent modes are both disabled):
SI1 $\rightarrow$ S_i -bit of frame 13, SI2 $\rightarrow$ S_i -bit of frame 15.

RSIF… **Receive Spare Bit for International Use (FAS Word)**

First bit in FAS-word. Used only in doubleframe format, otherwise fixed to ‘1’.

RS13… **Receive Spare Bit (Frame 13, CRC Multiframe)**

First bit in service word of frame 13. Significant only in CRC-multiframe format, otherwise fixed to ‘0’. This bit is updated with beginning of every received CRC multiframe.

RS15… **Receive Spare Bit (Frame 15, CRC Multiframe)**

First bit in service word of frame 15. Significant only in CRC-multiframe format, otherwise fixed to ‘0’. This bit is updated with beginning of every received CRC multiframe.

Framing Error Counter (Read)

	7						0	
FECL	FE7						FE0	(50)

	7						0	
FECH	FE15						FE8	(51)

FE15…FE0… **Framing Errors**

This 16-bit counter will be incremented when a FAS word has been received with an error.

Framing errors will not be counted during asynchronous state. During alarm simulation, the counter is incremented every 250 µs up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DFEC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Code Violation Counter (Read)

	7						0	
CVCL	CV7						CV0	(52)

	7						0	
CVCH	CV15						CV8	(53)

CV15…CV0… **Code Violations**

No function if NRZ code has been enabled.

If the HDB3 or the CMI code is selected, the 16-bit counter will be incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit FMR0.EXTD.

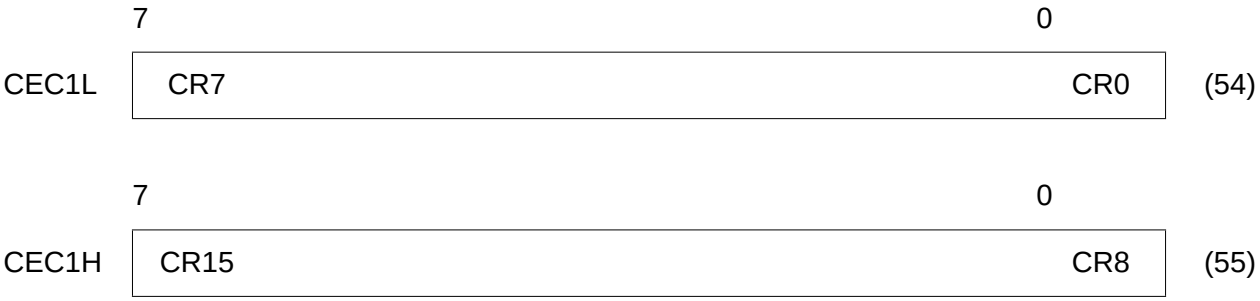
If simple AMI coding is enabled (FMR0.RC0/1 = 10) all bipolar violations are counted.

During alarm simulation, the counter is incremented every four bits received up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCVC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 1 (Read)



CR15…CR0… **CRC Errors**

No function if doubleframe format is selected.

In CRC-multiframe mode, the 16-bit counter will be incremented when a CRC-submultiframe has been received with a CRC error. CRC errors will not be counted during asynchronous state.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC1 has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCEC1 will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

E Bit Error Counter (Read)

	7						0	
EBCL	EB7						EB0	(56)

	7						0	
EBCH	EB15						EB8	(57)

EB15…EB0… E-Bit Errors

If doubleframe format is selected, FEBEH/L has no function. If CRC-multiframe mode is enabled, FEBEH/L works as submultiframe error indication counter (16 bits) which counts zeros in Si-bit position of frame 13 and 15 of every received CRC multiframe.

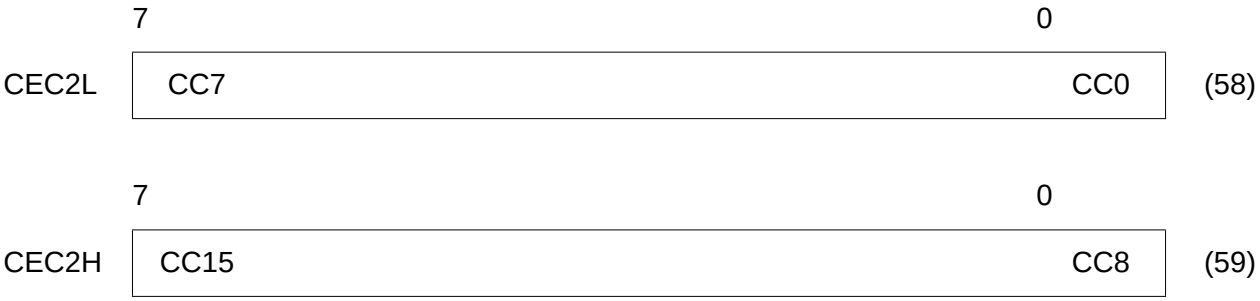
Clearing and updating the counter is done according to bit FMR1.ECM.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DEBC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 2 (Read)



CC15…CC0… CRC Error Counter (Reported from TE via Sa6 -Bit)

If doubleframe format is selected, CEC2H/L has no function. If CRC-multiframe mode is enabled, CEC2H/L works as SA6 Bit error indication counter (16 bits) which counts the SA6 Bit sequence 0001 and 0011in every received CRC submultiframe.
Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = 0.

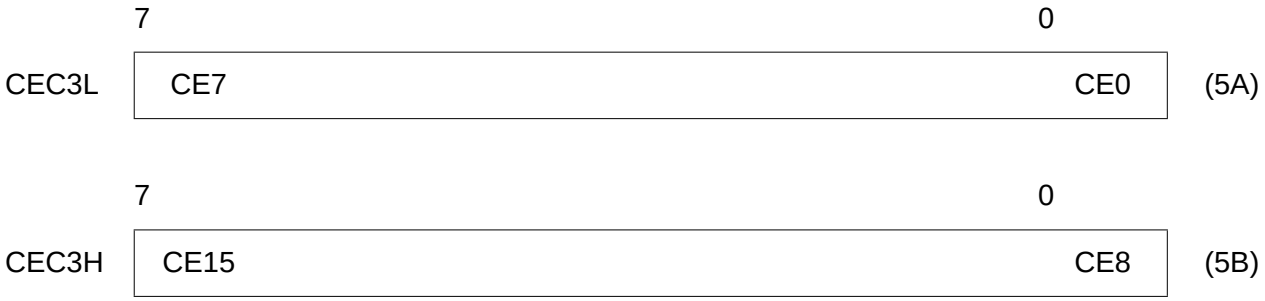
SA6 Bit sequence: SA61, SA62, SA63, SA64 = 0001 or 0011 where SA61 is received in frame 1 or 9 in every multiframe.

Clearing and updating the counter is done according to bit FMR1.ECM.

During alarm simulation, the counter is incremented once per multiframe up to its saturation.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC2 has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCEC2 will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 3 (Read)



CE15…CE0… **CRC Error Counter (detected at T Ref. Point via Sa6 -Bit)**

If doubleframe format is selected, CEC3H/L has no function. If CRC-multiframe mode is enabled, CEC3H/L works as SA6 Bit error indication counter (16 bits) which counts the SA6 Bit sequence 0010 and 0011in every received CRC submultiframe.
Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = 0.

SA6 Bit sequence: SA61, SA62, SA63, SA64 = 0010 or 0011 where SA61 is received in frame 1 or 9 in every multiframe.

Clearing and updating the counter is done according to bit FMR1.ECM.

During alarm simulation, the counter is incremented once per multiframe up to its saturation.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC3 has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCEC3 will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Receive Sa4-Bit Register (Read)

	7						0	
RSA4	RS47						RS40	(5C)

RS47…RS40… Receive Sa4-Bit Data (Y-Bits)

This register contains the information of the eight SA4 bits of the previously received CRC multiframe (bit-slot 4 of every service word). RS40 is received in frame 1, RS47 in frame 15. This register will be updated with every multiframe begin interrupt ISR0.RMB.

Valid if CRC multiframe format is enabled by setting bits FMR2.RFS1 = 1 or FMR2.RFS1/0 = 01 (Doubleframe format).

Receive Sa5-Bit Register (Read)

	7						0	
RSA5	RS57						RS50	(5D)

RS57…RS50… Receive Sa5-Bit Data (Y-Bits)

This register contains the information of the eight SA5 bits of the previously received CRC multiframe (bit-slot 5 of every service word). RS50 is received in frame 1, RS57 in frame 15. This register will be updated with every multiframe begin interrupt ISR0.RMB.

Valid if CRC multiframe format is enabled by setting bits FMR2.RFS1 = 1 or FMR2.RFS1/0 = 01 (Doubleframe format).

Receive Sa6-Bit Register (Read)

	7						0	
RSA6	RS67						RS60	(5E)

RS67…RS60… Receive Sa6-Bit Data (Y-Bits)

This register contains the information of the eight SA6 bits of the previously received CRC multiframe (bit-slot 6 of every service word). RS60 is received in frame 1, RS67 in frame 15. This register will be updated with every multiframe begin interrupt ISR0.RMB.

Valid if CRC multiframe format is enabled by setting bits FMR2.RFS1 = 1 or FMR2.RFS1/0 = 01 (Doubleframe format).

Receive Sa7-Bit Register (Read)

	7							0	
RSA7	RS77							RS70	(5F)

RS77…RS70… Receive Sa7-Bit Data (Y-Bits)

This register contains the information of the eight SA7 bits of the previously received CRC multiframe (bit-slot 7 of every service word). RS70 is received in frame 1, RS77 in frame 15. This register will be updated with every multiframe begin interrupt ISR0.RMB.

Valid if CRC multiframe format is enabled by setting bits FMR2.RFS1 = 1 or FMR2.RFS1/0 = 01 (Doubleframe format).

Receive Sa8-Bit Register (Read)

	7							0	
RSA8	RS87							RS80	(60)

RS87…RS80… Receive Sa8-Bit Data (Y-Bits)

This register contains the information of the eight SA8 bits of the previously received CRC multiframe (bit-slot 8 of every service word). RS80 is received in frame 1, RS87 in frame 15. This register will be updated with every multiframe begin interrupt ISR0.RMB.

Valid if CRC multiframe format is enabled by setting bits FMR2.RFS1 = 1 or FMR2.RFS1/0 = 01 (Doubleframe format).

Receive Sa6-Bit Status (Read)

	7							0	
RSA6S			S_X	S_F	S_E	S_C	S_A	S_8	(61)

Four consecutive received SA6-bits are checked on the by ETS 300233 defined SA6-bit combinations. The FALC54 will detect the following “fixed” SA6-bit combinations:
SA61,SA62,SA63,SA64=1000; 1010; 1100; 1110; 1111. All other possible 4 bit combinations are grouped to status “X”.

A valid SA6-bit combination must occur three times in a row. The corresponding status bit in this register will be set. Even if the detected status will be active for a short time the status bit remains active until this register is read. Reading the register will reset all pending status information.
With any change of state of the SA6-bit combinations an interrupt status ISR0.SA6SC will be generated.
During the basicframe asynchronous state updating of this register and interrupt status ISR0.SA6SC is disabled. In multiframe format the detection of the SA6-bit combinations can be done either synchronous or asynchronous to the submultiframe (FMR3.SA6SY). In synchronous detection mode updating of register RSA6S is done in the multiframe synch. state (FRS0.LMFA=0). In asynchr. detection mode updating is independent to the multiframe synchronous state.

S_X… **Receive Sa6-Bit Status_X**

If none of the fixed SA6-bit combinations are detected this bit will be set.

S_F… **Receive Sa6-Bit Status: “1111”**

Receive SA6-bit status “1111” is detected for three times in a row in the SA6-bit positions.

S_E… **Receive Sa6-Bit Status: “1110”**

Receive SA6-bit status “1110” is detected for three times in a row in the SA6-bit positions.

S_C… **Receive Sa6-Bit Status: “1100”**

Receive SA6-bit status “1100” is detected for three times in a row in the SA6-bit positions.

S_A… **Receive Sa6-Bit Status: “1010”**

Receive SA6-bit status “1010” is detected for three times in a row in the SA6-bit positions.

S_8… **Receive Sa6-Bit Status: “1000”**

Receive SA6-bit status “1000” is detected for three times in a row in the SA6-bit positions.

Signaling Status Register (Read)

	7							0	
SIS	XDOV	XFW	XREP		RLI	CEC			(64)

XDOV… **Transmit Data Overflow**

More than 32 bytes have been written to the XFIFO.
This bit is reset by:

– a transmitter reset command XRES

– or when all bytes in the accessible half of the XFIFO have been moved in the inaccessible half.

XFW… **Transmit FIFO Write Enable**

Data can be written to the XFIFO.

XREP… **Transmission Repeat**

Status indication of CMDR.XREP.

RLI… **Receive Line Inactive**

Neither FLAGs as Interframe Time Fill nor frames are received via the signaling timeslot.

CEC… **Command Executing**

0… No command is currently executed, the CMDR register can be written to.

1… A command (written previously to CMDR) is currently executed, no further command can be temporarily written in CMDR register.

Note: CEC will be active at most 5 SCLKX clock cycles if FMR1.IMOD=0 and 10 SCLKX cycles if FMR1.IMOD is set.

Receive Signaling Status Register (Read)

	7							0	
RSIS	VFR	RDO	CRC16	RAB	HA1	HA0		LA	(65)

RSIS relates to the last received HDLC frame; it is copied into RFIFO when end-of-frame is recognized (last byte of each stored frame).

VFR… **Valid Frame**

Determines whether a valid frame has been received.

1… valid

0… invalid

An invalid frame is either

– a frame which is not an integer number of 8 bits (n × 8 bits) in length (e.g. 25 bits), or

– a frame which is too short taking into account the operation mode selected via MODE (MDS2-0) and the selection of receive CRC ON/OFF (CCR3.RCRC) as follows:

  • MDS2-0 = 011 (16 bit Address),
  RCRC = 0 : 4 bytes; RCRC = 1 : 3-4 bytes

  • MDS2-0 = 010 (8 bit Address),
  RCRC = 0 : 3 bytes; RCRC = 1 : 2-3 bytes

Note: Shorter frames are not reported.

RDO… **Receive Data Overflow**

A RFIFO data overflow has occurred during reception of the frame.

Additionally, an interrupt can be generated (refer to ISR1.RDO/IMR1.RDO).

CRC16… **CRC16 Compare/Check**

0… CRC check failed; received frame contains errors.

1… CRC check o.k.; received frame is error-free.

RAB… **Receive Message Aborted**

The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.

HA1, HA0… **High Byte Address Compare**

Significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the FALC54 compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (broadcast address).

Dependent on the result of this comparison, the following bit combinations are possible:

00… RAH2 has been recognized

01… Broadcast address has been recognized

10… RAH1 has been recognized C/R = 0 (bit 1)

11… RAH1 has been recognized C/R = 1 (bit 1)

Note: If RAH1, RAH2 contain identical values, a match is indicated by '10' or '11'.

LA… **Low Byte Address Compare**

Significant in HDLC modes only.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two registers. (RAL1, RAL2).

0… RAL2 has been recognized

1… RAL1 has been recognized

Receive Byte Count Low (Read)

	7						0	
RBCL	RBC7						RBC0	(66)

Together with RBCH (bits RBC11 - RBC8), indicates the length of a received frame (1…4095 bytes). Bits RBC4-0 indicate the number of valid bytes currently in RFIFO. These registers must be read by the CPU following a RME interrupt.

Received Byte Count High (Read)

Value after RESET: 000_{xxxxx}

	7							0	
RBCH				OV	RBC11			RBC8	(67)

OV… **Counter Overflow**

More than 4095 bytes received.

RBC11 – RBC8… **Receive Byte Count (most significant bits)**

Together with RBCL (bits RBC7…RBC0) indicate the length of the received frame.

Interrupt Status Register 0 (Read)

Value after RESET: 00_H

	7							0	
ISR0	RME	RFS	T8MS	RMB	CASC	CRC4	SA6SC	RPF	(68)

All bits are reset when ISR0 is read.

If bit IPC.VIS is set to ‘1’, interrupt statuses in ISR0 may be flagged although they are masked via register IMR0. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

RME… **Receive Message End**

One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte.

The complete message length can be determined reading the RBCH, RBCL registers, the number of bytes currently stored in RFIFO is given by RBC4–0. Additional information is available in the RSIS register.

RFS… **Receive Frame Start**

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After an RFS interrupt, the contents of

- RAL1
- RSIS - bits 3-1

are valid and can be read by the CPU.

T8MS… **Receive Time Out 8 msec**

Only active if multiframing is enabled.

The framer has found the doubleframing (basic framing) FRS0.LFA = 0 and is searching for the multiframing. This interrupt will be set to indicate that no multiframing could be found within a time window of 8 msec. In multiframe synchronous state this interrupt will be not generated. Refer also to Floating multiframe alignment window.

RMB… **Receive Multiframe Begin**

This bit is set with the beginning of a received CRC multiframe related to the internal receive line timing.

In CRC multiframe format FMR2.RFS1 = 1 or in doubleframe format FMR2.RFS1/0 = 01 this interrupt occurs every 2 msec. If FMR2.RFS1/0 = 00 this interrupt will be generated every doubleframe (512 bits).

CASC… **Received CAS Information Changed**

This bit is set with the updating of a received CAS multiframe information in the registers RS1-16. If the last received CAS information changed from the previous received updating is started. This interrupt will only occur in the TS0 and TS16 synchronous state. The registers RS1-16 should be read within the next 2 ms otherwise the contents may be lost.

CRC4… **Receive CRC4 Error**

0... No CRC4 error occurs.

1... The CRC4 check of the last received submultiframe failed.

SA6S C… **Receive SA6-Bit Status Changed**

With every change of state of the received SA6-bit combinations this interrupt will be set.

RPF… **Receive Pool Full**

32 bytes of a frame have arrived in the receive FIFO. The frame is not yet completely received.

Interrupt Status Register 1 (Read)

	7							0	
ISR1		RDO	ALLS	XDU	XMB		XLSC	XPR	(69)

All bits are reset when ISR1 is read.

If bit IPC.VIS is set to ‘1’, interrupt statuses in ISR1 may be flagged although they are masked via register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

RDO… **Receive Data Overflow**

This interrupt status indicates that the CPU does not respond quickly enough to an RPF or RME interrupt and that data in RFIFO has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO is available again.

Note: Whereas the bit RSIS.RDO in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO, the ISR1.RDO interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.

ALLS… **All Sent**

This bit is set if the last bit of the current frame is completely sent out and XFIFO is empty.

XDU… **Transmit Data Underrun**

Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME was issued.

Note: Transmitter and XFIFO are reset and deactivated if this condition occurs. They are re-activated not before this interrupt status register has been read. Thus, XDU should not be masked via register IMR1.

XMB… **Transmit Multiframe Begin**

This bit is set every 2 ms with the beginning of a transmitted multiframe related to the internal transmitter timing.
Just before setting this bit registers XS1-16 are copied in the transmit shift registers. The registers XS1-16 are empty and has to be updated otherwise the contents will be retransmitted.

XLSC… **Transmit Line Status Change**

XLSC is set to one with the rising edge of the bit FRS1.XLO or with any change of bit FRS1.XLS.

The actual status of the transmit line monitor can be read from the FRS1.XLS and FRS1.XLO.

XPR… **Transmit Pool Ready**

A data block of up to 32 bytes can be written to the transmit FIFO. XPR enables the fastest access to XFIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.

Interrupt Status Register 2 (Read)

	7							0	
ISR2	FAR	LFA	MFAR	T400MS	AIS	LOS	RAR	RA	(6A)

All bits are reset when ISR2 is read.

If bit IPC.VIS is set to ‘1’, interrupt statuses in ISR2 may be flagged although they are masked via register IMR2. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

FAR… **Frame Alignment Recovery**

The framer has reached doubleframe synchronization. Set when bit FSR0.LFA is reset. It is set also after alarm simulation is finished and the receiver is still synchron.

LFA… **Loss of Frame Alignment**

The framer has lost synchronization and bit FRS0.LFA is set. It will be set during alarm simulation.

MFAR… **Multiframe Alignment Recovery**

Set when the framer has found two CRC-multiframes at an interval of n x 2 ms (n = 1, 2, 3, …) without a framing error. At the same time bit FRS0.LMFA is reset.

It is set also after alarm simulation is finished and the receiver is still synchron. Only active if CRC-multiframe format is selected.

T400MS… **Receive Time Out 400 msec**

Only active if multiframing is enabled.

The framer has found the doubleframing (basic framing) FRS0.LFA = 0 and is searching for the multiframing. This interrupt will be set to indicate that no multiframing could be found within a time window of 400 msec after basic framing has been achieved. In multiframe synchronous state this interrupt will not be generated.

AIS… **Alarm Indication Signal**

This bit is set when an alarm indication signal is detected and bit FRS0.AIS is set. It will be set during alarm simulation.
If IPC.SCI is set high this interrupt status bit will be set with every change of state of FRS0.AIS.

LOS… **Loss of Signal**

This bit is set when a loss of signal alarm is detected in the received bitstream and FRS0.LOS is set. It will be set during alarm simulation.
If IPC.SCI is set high this interrupt status bit will be set with every change of state of FRS0.LOS.

RAR… **Remote Alarm Recovery**

Set if a remote alarm in TS0 is cleared and bit FRS0.RA is reset. It is set also after alarm simulation is finished and no remote alarm is detected.

RA… **Remote Alarm**

Set if a remote alarm in TS0 is detected and bit FRS0.RA is set. It will be set during alarm simulation.

Interrupt Status Register 3 (Read)

	7							0	
ISR3	ES	SEC	LMFA16	AIS16	RA16	API	SLN	SLP	(6B)

All bits are reset when ISR3 is read.

If bit IPC.VIS is set to ‘1’, interrupt statuses in ISR3 may be flagged although they are masked via register IMR3. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

ES… **Errored Second**

This bit is set if at least one enabled interrupt source via IMR4 is set during the time interval of one second. Interrupt sources of IMR4 register:
LFA = Loss of frame alignment detected (FRS0.LFA)
FER = Framing error received
CER = CRC error received
AIS = Alarm indication signal (FRS0.AIS)
LOS = Loss of signal (FRS0.LOS)
CVE = Code violation detected
SLIP = Receive Slip positive/negative detected
EBE = E- Bit error detected (RSP.SI1/SI2 =0)

SEC… **Second**

The internal one second timer has expired. The timer is derived from the internal 16 MHz clock.

LMFA16… **Loss of Multiframe Alignment TS 16**

Multiframe alignment of timeslot 16 has been lost if two consecutive multiframe pattern are not detected or if in 16 consecutive timeslot 16 all bits are reset.
If register IPC.SCI is high this interrupt status bit will be set with every change of state of FRS1.TS16LFA.

AIS16… **Alarm Indication Signal TS 16 Status Change**

The alarm indication signal AIS in timeslot 16 for the 64 kbit/s channel associated signaling is detected or cleared. A change in bit FRS1.TS16AIS will set this interrupt. (This bit is set if the incoming TS 16 signal contains less than 4 Zeros in each of two consecutive TS16-multiframe periods.)

RA16… **Remote Alarm TS 16 Status Change**

A change in the remote alarm bit in CAS multiframe alignment word is detected.

API… **Auxiliary Pattern Indication**

This bit is set if the auxiliary pattern is detected in the received bitstream and bit FRS0.AUXP is set.
If register IPC.SCI is high this interrupt status bit will be set with every change of state of FRS0.AUXP.

SLN… **Slip Negative**

The frequency of the receive route clock is greater than the frequency of SCLKR/4. A frame will be skipped. It will be set during alarm simulation.

SLP… **Slip Positive**

The frequency of the receive route clock is less than the frequency of SCLKR/4. A frame will be repeated. It will be set during alarm simulation.

Global Interrupt Status Register (Read)

Value after RESET: 00_H

	7							0	
GIS					ISR3	ISR2	ISR1	ISR0	(6E)

This status register points to pending interrupts (ISR3 ... ISR0).

Version Status Register (Read)

	7					0	
VSTR					VN3	VN0	(6F)

VN3 – VN0… **Version Number of Chip**

0…Version 1.1 - 1.2
1…Version 1.3

Receive CAS Register (Read)

Value after RESET: not defined

	7							0	
RS1	0	0	0	0	X	Y	X	X	(70)
RS2	A1	B1	C1	D1	A16	B16	C16	D16	(71)
RS3	A2	B2	C2	D2	A17	B17	C17	D17	(72)
RS4	A3	B3	C3	D3	A18	B18	C18	D18	(73)
RS5	A4	B4	C4	D4	A19	B19	C19	D19	(74)
RS6	A5	B5	C5	D5	A20	B20	C20	D20	(75)
RS7	A6	B6	C6	D6	A21	B21	C21	D21	(76)
RS8	A7	B7	C7	D7	A22	B22	C22	D22	(77)
RS9	A8	B8	C8	D8	A23	B23	C23	D23	(78)
RS10	A9	B9	C9	D9	A24	B24	C24	D24	(79)
RS11	A10	B10	C10	D10	A25	B25	C25	D25	(7A)
RS12	A11	B11	C11	D11	A26	B26	C26	D26	(7B)
RS13	A12	B12	C12	D12	A27	B27	C27	D27	(7C)
RS14	A13	B13	C13	D13	A28	B28	C28	D28	(7D)
RS15	A14	B14	C14	D14	A29	B29	C29	D29	(7E)
RS16	A15	B15	C15	D15	A30	B30	C30	D30	(7F)

Receive CAS Register 1-16

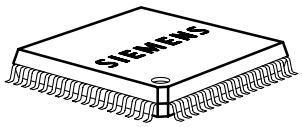
Each register except RS1 contains the received CAS bits for two timeslots. The received CAS multiframe will be compared with the previously received one. If the contents changed a CAS multiframe changed interrupt (ISR0.CASC) is generated and informs the user that a new multiframe has to be read within the next 2 ms. If requests for reading the RS1-16 register are ignored, the received data may be lost. RS1 contains frame 0 of the CAS multiframe. MSB is received first.

SIEMENS

Framing and Line Interface Component FALC54 **PEB 2254**

CMOS

FALC54 in PCM 24 Mode



P-MQPF-80-1

4 General Features T1

Line Interface

- Analog receive and transmit circuitry
- Data and clock recovery using an integrated digital phase locked loop
- Maximum line attenuation up to 18 dB (ITU-T I.431) Adaptively controlled receiver threshold
- Low transmitter output impedance for a high return loss with reasonable protection resistors
- Tri-state function of the analog Transmit Line Outputs
- Programmable transmit pulse shape using a minimum number of external components
- Jitter specifications of ITU-T I.431, G.703 and AT&T TR 62411 met
- Wander and jitter attenuation/compensation clock smoothing
- Dual rail or single rail digital inputs and outputs
- Unipolar NRZ for interfacing fibre optical transmission routes
- Selectable line codes (B8ZS, AMI with ZCS)
- Loss of signal indication with programmable thresholds according to ITU-T G.775 and ANSI T1. 403
- Clock generator for jitter free system clocks and transmit clock using an digital phase locked loop
- Transmit line monitor
- Local loop and remote loop for diagnostic purposes
- Only one type of transformer (ratio 1: $\sqrt{2}$) for CEPT 75/120 Ω and T1 100 Ω

Type	Version	Ordering Code	Package
PEB 2254-H	V1.3	Q67103-H6813	P-MQFP-80 (SMD)

Frame Aligner

- Frame alignment/synthesis for 1544 kbit/s according to ITU-T G.704
- Meets newest ITU-T Rec's, ANSI T1 and AT&T Technical References
- Programmable formats for
  PCM 24: 4-Frame Multiframe (F4), 12-Frame Multiframe (F12, D3/4), Extended Superframe (ESF), Remote Switch Mode (F72, SLC96)
- Selectable conditions for loss of frame alignment
- Error checking via CRC6 procedures according to ITU-T G. 706
- Performance monitoring
  16 bit counter for CRC-, framing errors, code violations, Errored blocks
- Insertion and extraction of alarms (AIS, Remote (Yellow) Alarm, …)
- IDLE code insertion for selectable channels
- 8192 kHz System clock frequency different for receiver and transmitter
- Selectable 2048/4096 kbit/s backplane interface with programmable receive/transmit shifts
  Programmable tri-state function of 4096 kbit/s output via RDO
- Two-frame elastic store for receive route clock wander and jitter compensation; controlled slip capability and slip indication
- One frame elastic store for transmit route clock wander and jitter compensation
- Support for different data link schemes
- Clear channel capabilities
- Flexible transparent modes
- In band Loop Code detection and generation according to TR 62411
- Channel loop back, line loop back or Payload loop back capabilities (AT&T TR 54016)

Signaling Controller

- HDLC controller
  Bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions, programmable preamble
- DL-channel protocol for ESF format according to T1.403-1989 ANSI specification or according to AT&T TR54016.
- Robbed bit signaling with last look capability
- DL-access for F72 (SLC96) format
- Transparent Mode
- FIFO buffers (64 bytes deep) for efficient transfer of data packets.
- Time-slot assignment
  Any combination of time slots selectable for data transfer independent of signaling mode. Useful for Fractional T1 applications.

MP Interface

- 8/16 bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte or word access)
- Extended interrupt capabilities

General

- Boundary Scan Standard IEEE 1149.1
- Advanced CMOS technology
- P-MQFP-80 Package

The FALC’s power consumption is mainly determined by the line length and type of the cable and typical 450 mW.

4.1 Pin Configuration of FALC
(top view)

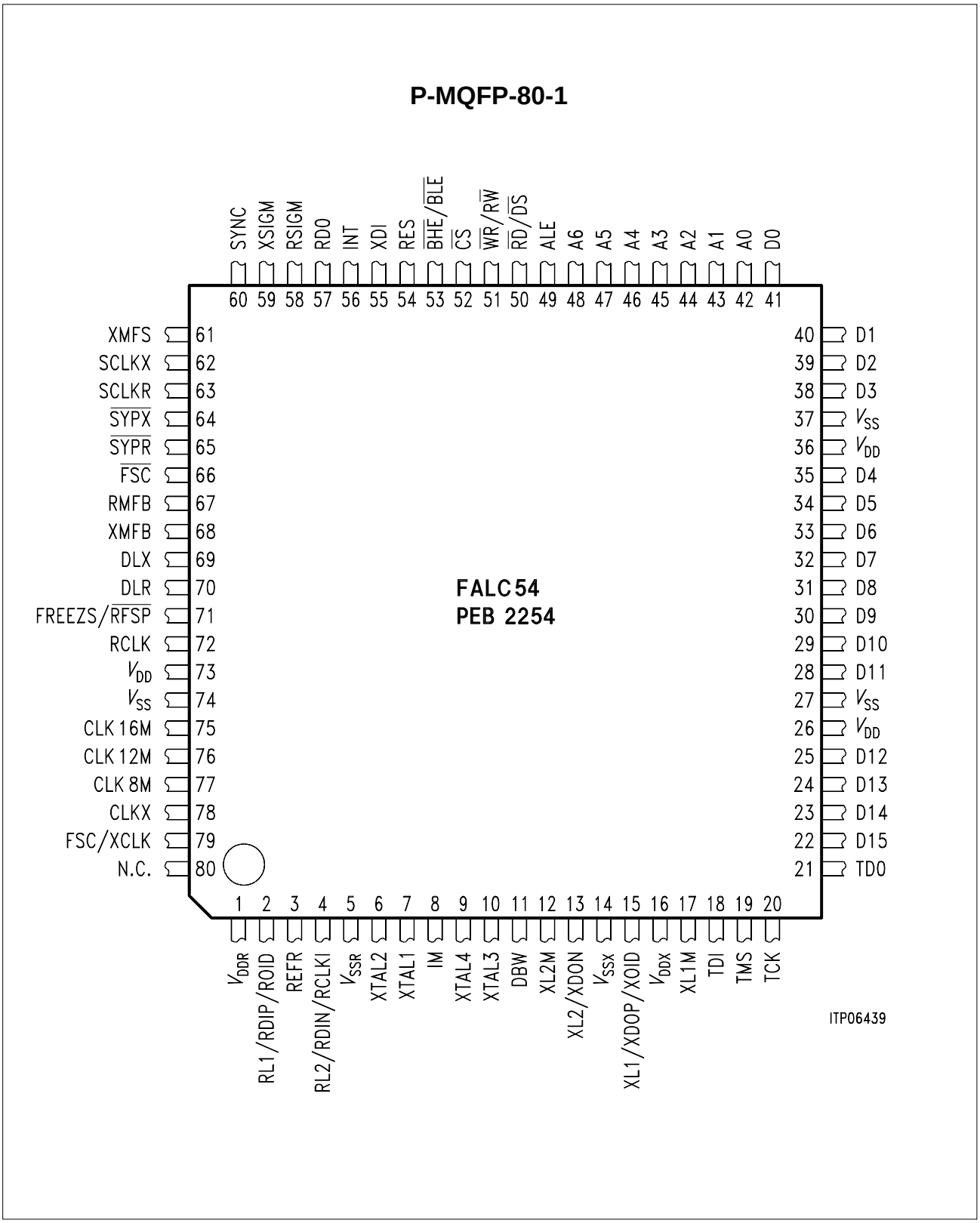


Figure 33

4.2 Pin Definitions and Function

Pin No.	Symbol	Input (I) Output (O)	Function
42 … 48	A0 … A6	I	**Address Bus** These inputs interface with seven bits of the system's address bus to select one of the internal registers for read or write.
41 … 38 35 … 28 25 … 22	D0 … D3 D4 … D11 D12 … D15	I/O	**Data Bus** Bi-directional three-state data lines which interface with the system's data bus. Their configuration is controlled by the level of pin DBW: – 8-bit mode (DBW = 0): D0 … D7 are active. D8 … D15 are in high impedance and have to be connected to V_{DD} or V_{SS}. – 16-bit mode (DBW = 1): D0 … D15 are active. In case of byte transfers, the active half of the bus is determined by A0 and $\overline{BHE}$/$\overline{BLE}$ and the selected bus interface mode (via pin IM). The unused half is in high impedance. For detailed information, refer to **chapter 4.6**.
49	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address/data bus. The address information provided on lines A0 … A6 is internally latched with the falling edge of ALE. This function allows the FALC54 to be directly connected to a multiplexed address/data bus. In this case, pins A0 … A6 must be externally connected to the Data Bus pins.In case of demultiplexed mode this pin has to be connected directly to ground or VDD. For detailed information, refer to **chapter 4.6**.

Note: All unused input pins including pin 80 have to be connected to a defined level

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
50	$\overline{RD}/\overline{DS}$	I	**Read Enable** (Siemens/Intel bus mode) This signal indicates a read operation. When the FALC54 is selected via $\overline{CS}$ the $\overline{RD}$ signal enables the bus drivers to output data from an internal register addressed via A0 … A6 on to Data Bus. For more information about control/status register and FIFO access in the different bus interface modes refer to **chapter 4.6**. **Data Strobe** (Motorola bus mode) This pin serves as input to control read/write operations.
51	$\overline{WR}/R\overline{W}$	I	**Write Enable** (Siemens/Intel bus mode) This signal indicates a write operation. When $\overline{CS}$ is active the FALC54 loads an internal register with data provided via the Data Bus. For more information about control/status register and FIFO access in the different bus interface modes refer to **chapter 4.6**. **Read/Write Enable** (Motorola bus mode) This signal distinguishes between read and write operation.
52	$\overline{CS}$	I	**Chip Select** A low signal selects the FALC54 for read/write operations.
54	RES	I	**Reset** A high signal on this pin forces the FALC54 into reset state. During Reset the FALC54 needs active clocks on pins SCLKR, SCLKX, XTAL1 and XTAL3. During Reset – all uni-directional output stages are in high-impedance state, except pins CLK16M, CLK12M, CLK8M, CLKX, $\overline{FSC}$, XCLK and RCLK – all bi-directional output stages (data bus) are in high-impedance state if signal $\overline{RD}$ is "high", "output" XTAL2/4 is in high-impedance if input XTAL1/3 is "high".

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
53	$\overline{\text{BHE}}$/$\overline{\text{BLE}}$	I	**Bus High Enable** (Siemens/Intel bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus (D8 … D15). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}. Refer to **chapter 4.6** for detailed information. **Bus Low Enable** (Motorola bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus (D0 … D7). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}. Refer to **chapter 4.6** for detailed information.
11	DBW	I	**Data Bus Width** (Bus Interface Mode) A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{\text{BHE}}$/$\overline{\text{BLE}}$.
56	INT	O/oD	**Interrupt Request** INT serves as general interrupt request which may include all interrupt sources. These interrupt sources can be masked via registers IMR0 … 4. Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR0 … 3. Output characteristics (push-pull active low/high, open drain) are determined by programming the IPC register.
8	IM	I	**Interface Mode** The level at this pin defines the bus interface mode: A low signal on this input selects the INTEL interface mode. A high signal on this input selects the Motorola interface mode.
1	V_{DDR}	I	**Positive Power Supply** for the analog receiver

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
2	RL1	I	**Line Receiver 1** Analog Input from the external transformer. Selected if LIM1.DRS = 0.
	RDIP	I	**Receive Data Input Positive** Digital input for received dual rail PCM(+) route signal which will be latched with the internal generated Receive Route Clock. An internal DPLL will extract the Receive Route Clock from the incoming data pulse. The Duty cycle of the receiving signal has to be closely to 50 %. The Dual Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input sense is selected by bit RC0.RDIS (after Reset: active low).
	ROID	I	**Receive Optical Interface Data** Unipolar data received from fibre optical interface with 1544 kbit/s. Latching of data is done with the falling edge of RCLKI. Input sense is selected by bit RC0.RDIS. The Single Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 0.
3	REFR	O	**Reference Resistance** of 12 k$\Omega \pm 1$ % connected to V_{SS}

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
4	RL2	I	**Line Receiver 2** Analog Input from the external transformer. Selected if LIM1.DRS = 0.
	RDIN	I	**Receive Data Input Negative** Input for received dual rail PCM(-) route signal which will be latched with the internal generated Receive Route Clock. An internal DPLL will extract the Receive Route Clock from the incoming data pulse. The Duty cycle of the receiving signal has to be closely to 50 %. The dual rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input sense is selected by bit RC0.RDIS (after Reset: active low).
	RCLKI	I	**Receive Clock Input** Receive clock input for the optical interface if LIM1.DRS = 1 and FMR0.RC1/0 = 00. Clock frequency: 1544 kHz
5	V_{SSR}	I	**Power Ground Supply** for analog receiver
6 7	XTAL2 XTAL1	O I	**Crystal Connection 16.384 MHz** When an external clock is used, normally if the bit LIM0.MAS is set, the FALC54 functions as a master.
9 10	XTAL4 XTAL3	O I	**Crystal Connection 12.352 MHz** A crystal has to be connected to these pins to generate the transmit clock.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
13	XL2	O	**Transmit Line 2** Analog output for the external transformer. Selected if LIM1.DRS = 0. After Reset this pin is in a high impedance state until register FMR0.XC1 is set to one.
	XDON	O	**Transmit Data Output Negative** This digital output for transmitted dual rail PCM(-) route signals can provide – half bauded signals with 50% duty cycle (LIM0.XFB = 0) or – full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output sense is selected by bit LIM0.XDOS (after Reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
14	V_{SSX}	I	**Ground** for analog transmitter

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
15	XL1	O	**Transmit Line 1** Analog output for the external transformer. Selected if LIM1.DRS = 0. After Reset this pin is in a high impedance state until register FMR0.XC1 is set to one.
	XDOP	O	**Transmit Data Output Positive** This digital output for transmitted dual rail PCM(+) route signals can provide – half bauded signals with 50% duty cycle (LIM0.XFB = 0) or – full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output sense is selected by bit LIM0.XDOS (after Reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
	XOID	O	**Transmit Optical Interface Data** Unipolar data sent to fibre optical interface with 1544 kbit/s which will be clocked off on the positive transitions of XCLK. Clocking off data in NRZ code is done with 100 % duty cycle. Output sense is selected by bit LIM0.XDOS (after Reset: data are sent active high). The single rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 0. After Reset this pin is in a high impedance state until register LIM1.DRS is set to one.
17	XL1M	I	**Transmit Line 1 Monitor** Analog input from the external transmit transformer (XL1). This pin must be connected otherwise the XL1 pin could be set in a high impedance state. If digital inputs are selected (LIM1.DRS = 1) this input has to be switched to V_{SSX}.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
12	XL2M	I	**Transmit Line 2 Monitor** Analog input from the external transmit transformer (XL2). This pin must be connected otherwise the XL2 pin could be set in a high impedance state. If digital inputs are selected via LIM1.DRS = 1 this input has to be switched to V_{SSX}.
16	VDDX	I	**Positive Power Supply** for analog transmitter
79	XCLK FSC	O O	**Transmit Clock** Transmit clock frequency: 1544 kHz. Derived from the XTAL3 or RCLK or internally generated. If LIM1.EFSC is set high an **8-kHz Frame Synchronization Pulse** is output via this pin. The synchronization pulse is active high for one 2 MHz cycle (pulse width = 488 ns) and is derived from the clock supplied by pin XTAL1.
80	N.C.		Not connected. For further application this pin should be connected to V_{SS}.
66	$\overline{\text{FSC}}$	O	**8-kHz Frame Synchronization Pulse** is active low for one 2 MHz cycle (pulse width = 488 ns) and is derived from the clock supplied by pin XTAL1.
75	CLK16M	O	**System Clock** 16.384 MHz
76	CLK12M	O	**System Clock** 12.352 MHz only if a crystal or an oscillator is connected to XTAL3/4.
77	CLK8M	O	**System Clock** 8.192 MHz The frequency is derived from the clock supplied by pin XTAL1.
78	CLKX	O	**System Clock Output** Output frequencies are: 2.048 MHz or 4.096 MHz inverted or non-inverted. The frequency and sense on this pin is selectable via LIM0.SCL1/0 and is derived from the clock supplied by pin XTAL1.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
60	SYNC	I	**Clock Synchronization** If a clock is detected at the SYNC pin the FALC54 synchronizes to this clock 1.544 MHz or 2.048 MHz (if LIM1.DCOC = 1). This pin has to be connected to V_{SS} if no clock is supplied.
72	RCLK	O	**Receive Clock** Extracted from the incoming data pulses Clock frequency: 1544 kHz If LIM0.ELOS is set, the RCLK is set high in case of loss of signal (FRS0.LOS=1).
57	RDO	O	**Receive Data Out** Received data which is sent to the system internal highway with 4096 kbit/s or 2048 kbit/s (bit FMR1.IMOD). In 4096 kbit/s mode data is shifted out in that channel phase which is selected by register RC0.SICS.The other channel phase is set in tri-state. Clocking off data is done with the falling edge of SCLKR. The delay between the beginning of time-slot 0 and the initial edge of SCLKR (after $\overline{\text{SYPR}}$ goes active) is determined by the values of Receive Time-slot Offset RC1.RTO5 … 0, Receive Clock-slot Offset RC0.RCO2 … 0 and RC0.RCOS.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
71	$\overline{\text{RFSP}}$/ FREEZS	O	**Receive Frame Synchronous Pulse/ Freeze Signaling** If XC0.SFRZ is set to '0' the Receive Frame Synchronous Pulse (Pulse width = 648 ns) is output on this pin. Pulse frequency: 8 kHz. If XC0.SFRZ is set high the Freeze signaling Status is indicated. Synchronization status signal which informs the signaling processor that current signaling should be frozen. It goes active if – one or more framing bit errors are found in a superframe, – loss of receiver synchronization, or – a receive slip is detected. It is cleared after an error-free superframe. During alarm simulation, this signal goes active during simulation steps 2 and 6.
70	DLR	O	**Data Link Bit Receive** This output provides a 4 kHz signal which marks the DL-bit position within the data stream on RDO. It can be used as receive strobe signal for external data link controllers. In 4096 kbit/s mode DLR is active only during the channel phase which is selected by RC0.SICS.
68	XMFB	O	**Transmit Multiframe Begin** The function depends on programming bit XC0.MFBS: MFBS = 1: XMFB marks the beginning of every transmitted multiframe (XDI). MFBS = 0: Marks the beginning of every transmitted superframe. Additional pulses every 12 frames are provided when using ESF or F72 format. XMFB is always active high for one 2048 kbit/s period. In 4096 kbit/s mode XMFB is active during the first two bits of the multiframe.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
59	XSIGM	O	**Transmit Signaling Marke**r – Marks the transmit time-slots which are defined by register TTR1-4 of every frame transmitted via port XDI. – When using the CAS-BR signaling scheme (bit FMR1.SIGM = 1), the robbed bit of each channel every six frames is marked, if it is enabled via register XC0.BRM = 1. In 4096 kbit/s mode XSIGM is active only during the channel phase which is selected by RC0.SICS.
65	$\overline{\text{SYPR}}$	I	**Synchronous Pulse Receive** Defines the beginning of time-slot 0 at system highway port RDO in conjunction with the values of registers RC0.RCO, RC0.RCOS and RC1.RTO. Sampling is done with the falling edge of the SCLKR clock. Pulse Cycle: Integer multiple of 125 µs.
64	$\overline{\text{SYPX}}$	I	**Synchronous Pulse Transmit** Defines the beginning of time-slot 0 at system highway port XDI in conjunction with the values of registers XC0.XCO, XC1.XTO and XC1.XCOS. Sampling is done with the falling edge of the SCLKX clock. Pulse Cycle: Integer multiple of 125 µs.
63	SCLKR	I	**System Clock Receive** Working clock for the FALC54 with a frequency of 8192 kHz.
62	SCLKX	I	**System Clock Transmit** Working clock for the FALC54 with a frequency of 8192 kHz.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
55	XDI	I	**Transmit Data In** Transmit data received from the system internal highway with 4096 kbit/s or 2048 kbit/s (bit FMR1.IMOD). Latching of data is done with negative transitions of SCLKX. In 4096 kbit/s mode data is sampled in the first channel phase if RC0.SICS is low. If RC0.SICS is high data is sampled in the second channel phase. The delay between the beginning of time-slot 0 and the initial edge of SCLKX (after $\overline{\text{SYPX}}$ goes active) is determined by the values of transmit time-slot offset XC1.XTO5 … 0, transmit clock-slot offset XC0.XCO2 … 0 and XC1.XCOS.
69	DLX	O	**Data Link Bit Transmit** This output provides a 4 kHz signal which marks the DL-bit position within the data stream on XDI. It can be used as transmit strobe signal for external data link controllers. In 4096 kbit/s mode DLX is active only during the channel phase which is selected by RC0.SICS.
58	RSIGM	O	**Receive Signaling Marker** – Marks the time-slots which are defined by register RTR1-4 of every received frame at port RDO. – When using the CAS-BR signaling scheme (bit FMR1.SIGM = 1), the robbed bit of each channel every six frames is marked, if it is enabled via register XC0.BRM = 1. In 4096 kbit/s mode RSIGM is active high only during the channel phase which is selected by RC0.SICS.

Pin Definitions and Function (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
67	RMFB	O	**Receive Multiframe Begin** The function depends on programming bit XC0.MFBS: MFBS = 1: RMFB marks the beginning of every received multiframe (RDO). MFBS = 0: Marks the beginning of every received superframe. Additional pulses every 12 frames are provided when using ESF or F72 format. RMFB is always active high for one 2048 kbit/s period. In 4096 kbit/s mode RMFB is active during the first two bits of the multiframe.
61	XMFS	I	**External Transmit Multiframe Synchronization** This port operates as an input for External Transmit Multiframe Synchronization which defines frame 1 of the Multiframe on XDI. Minimum pulse length is 244 ns. Latching is done equivalent to latching data via XDI. The signal has to be issued during frame 1 and has to be reset at least one bit before begin of frame 2. Recommended: XMFS begins with the first bit of time-slot 0, frame 1 of XDI. *Note: A new multiframe position has been settled at least one multiframe after pulse XMFS has been supplied.*
27, 37, 74	V_{SS}	I	**Power Ground** Supply for digital subcircuits (0 V) For correct operation, all three pins have to be connected to ground.
26, 36, 73	V_{DD}	I	**Positive Power Supply** for the digital subcircuits (5 V) For correct operation, all three pins have to be connected to positive power supply.
18	TDI	I	**Test Data Input** for Boundary Scan acc. to IEEE Std. 1149.1
21	TDO	O	**Test Data Output** for Boundary Scan
19	TMS	I	**Test Mode Select** for Boundary Scan
20	TCK	I	**Test Clock** for Boundary Scan

4.3 Logic Symbol

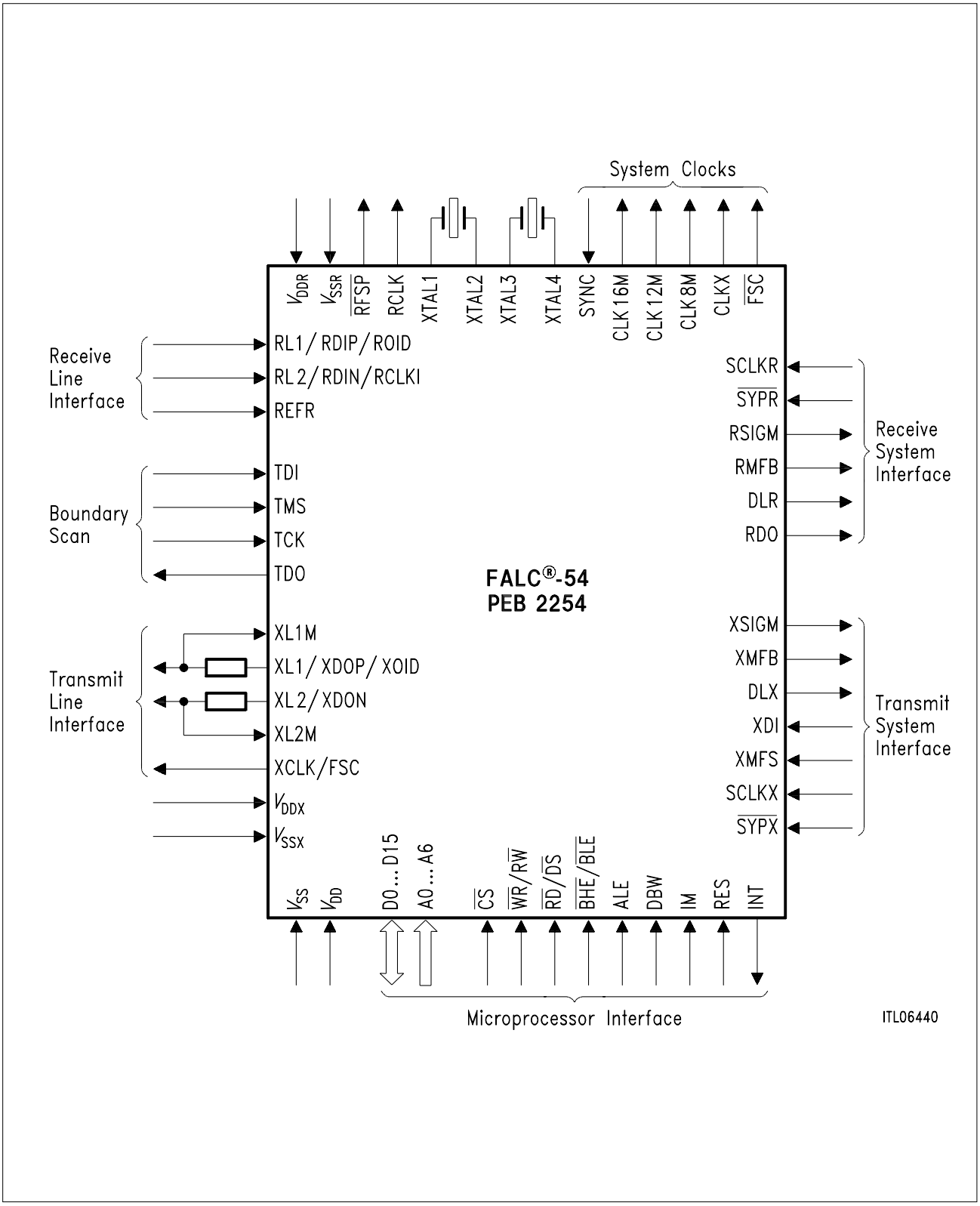


Figure 34
FALC54 Logic Symbol

4.4 Functional Block Diagram

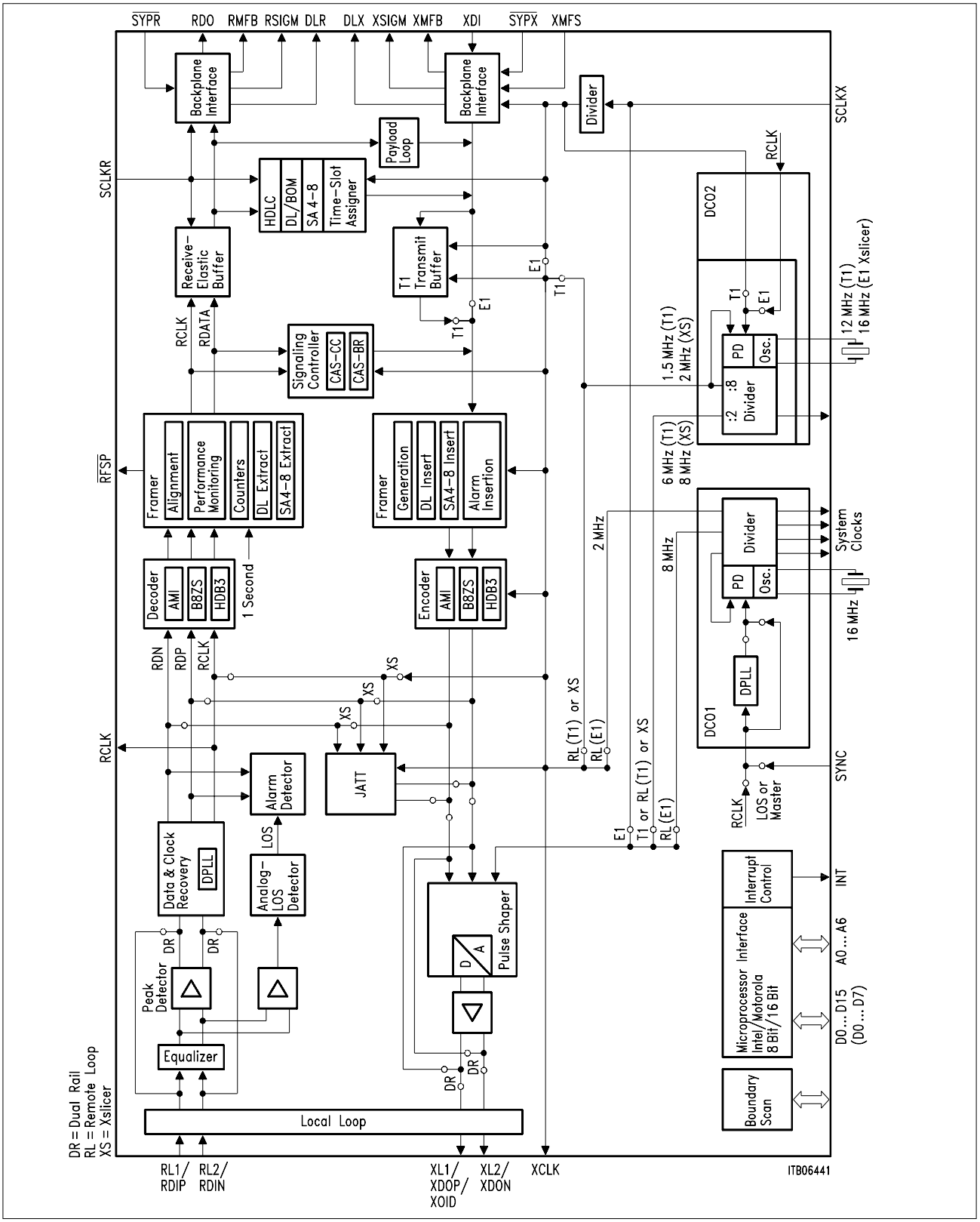


Figure 35
Functional Block Diagram PEB 2254

4.5 System Integration

The figures below show a multiple link application and a NT application.

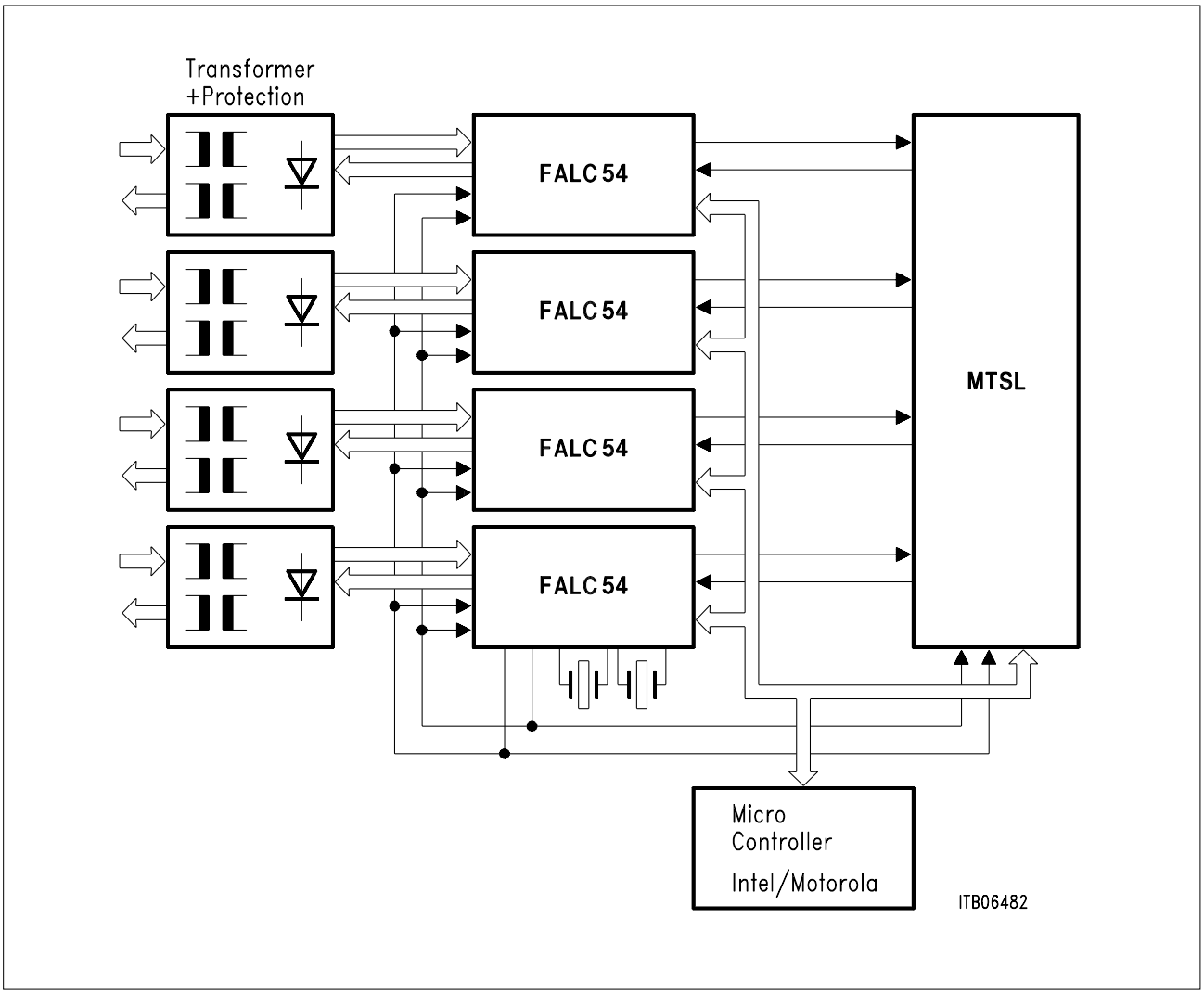


Figure 36
Multiple Link Application

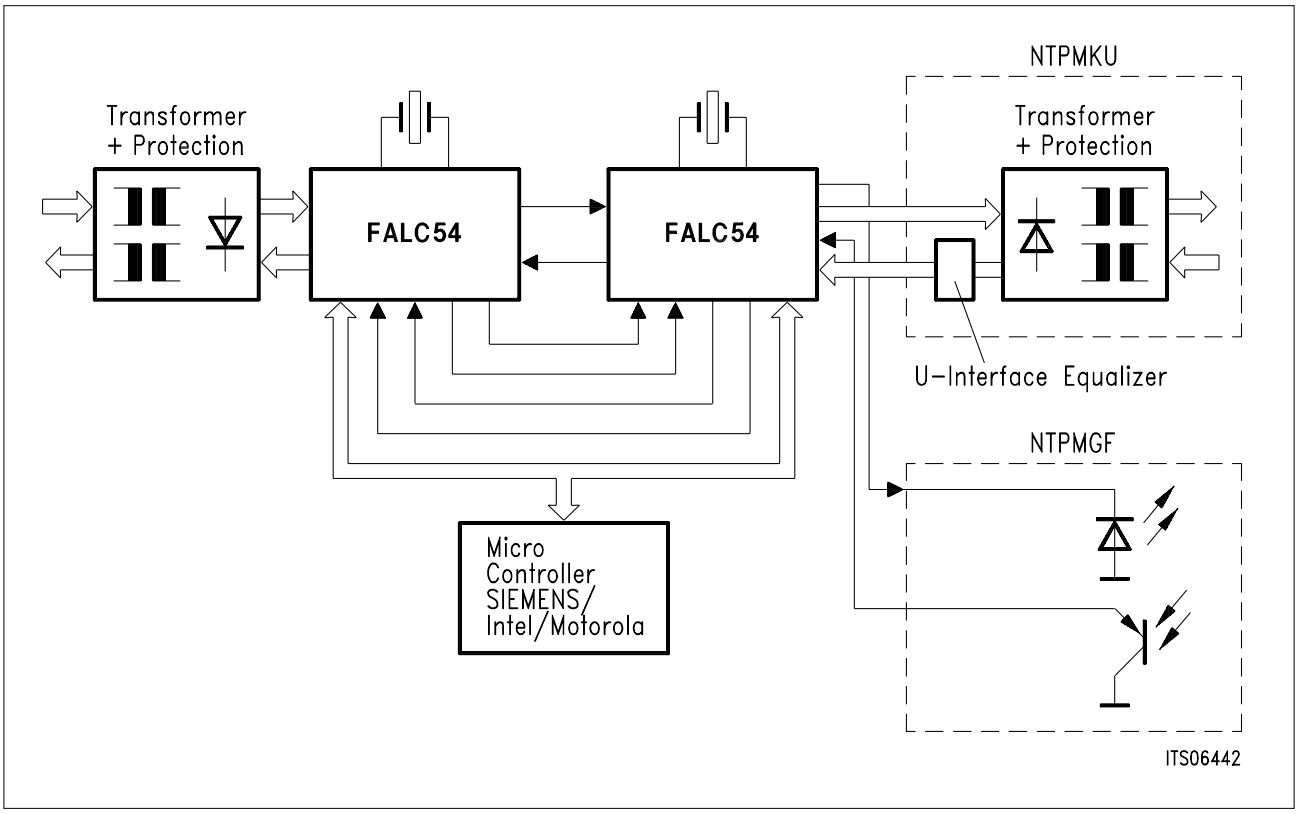


Figure 37
NT - Application

4.6 Microprocessor Interface

The communication between the CPU and the FALC54 is done via a set of directly accessible registers. The interface may be configured as Siemens/Intel or Motorola type with a selectable data bus width of 8 or 16 bits.

The CPU transfers data to/from the FALC54 (via 64 byte deep FIFOs per direction and channel), sets the operating modes, controls function sequences, and gets status information by writing or reading control/status registers. All accesses can be done as byte or word accesses if enabled. If 16-bit bus width is selected, access to lower/upper part of the data bus is determined by address line A0 and signal $\overline{\text{BHE}}$/$\overline{\text{BLE}}$ as shown in **table 11** and **12**.

In **table 13** is shown how the ALE (address latch enable) line is used to control the bus structure and interface type. The switching of ALE allows the FALC54 to be directly connected to a multiplexed address/data bus.

Mixed Byte/Word Access to the FIFOs

Reading from or writing to the internal FIFOs (RFIFO and XFIFO of each channel) can be done using a 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. Randomly mixed byte/word access to the FIFOs is allowed without any restrictions.

Table 11
Data Bus Access (16-Bit Intel Mode)

$\overline{\text{BHE}}$	A0	Register Access	FALC54 Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D0 – D15
0	1	Register byte access (odd addresses)	D8 – D15
1	0	Register byte access (even addresses)	D0 – D7
1	1	No transfer performed	None

Table 12
Data Bus Access (16-Bit Motorola Mode)

BLE	A0	Register Access	FALC54 Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D0 – D15
0	1	Register byte access (odd addresses)	D0 – D7
1	0	Register byte access (even addresses)	D8 – D15
1	1	No transfer performed	None

Table 13
Selectable Bus and Microprocessor Interface Configuration

ALE	IM	Microprocessor Interface	Bus Structure
GND/VDD	1	Motorola	demultiplexed
GND/VDD	0	Intel	demultiplexed
switching	0	Intel	multiplexed

The assignment of registers with even/odd addresses to the data lines in case of 16-bit register access depends on the selected microprocessor interface mode:

Siemens/Intel	(Adr. n + 1)	(Adr. n)
Motorola	(Adr. n)	(Adr. n + 1)

↑↑
↓↓

Data Lines	D15 D8	D7 D0

n: even address

Complete information concerning register functions is provided in – Detailed Register Description.

FIFO Structure

In transmit and receive direction of the signaling controller 64-byte deep FIFOs are provided for the intermediate storage of data between the system internal highway and the CPU interface. The FIFOs are divided into two halves of 32-bytes. Only one half is accessible to the CPU at any time.

In case 16-bit data bus width is selected by fixing pin DBW to logical ‘1’ word access to the FIFOs is enabled. Data output to bus lines D0-D15 as a function of the selected interface mode is shown in **figure 38** and **39**. Of course, byte access is also allowed.The effective length of the accessible part of RFIFO can be changed from 32 bytes (RESET value) down to 2 bytes.

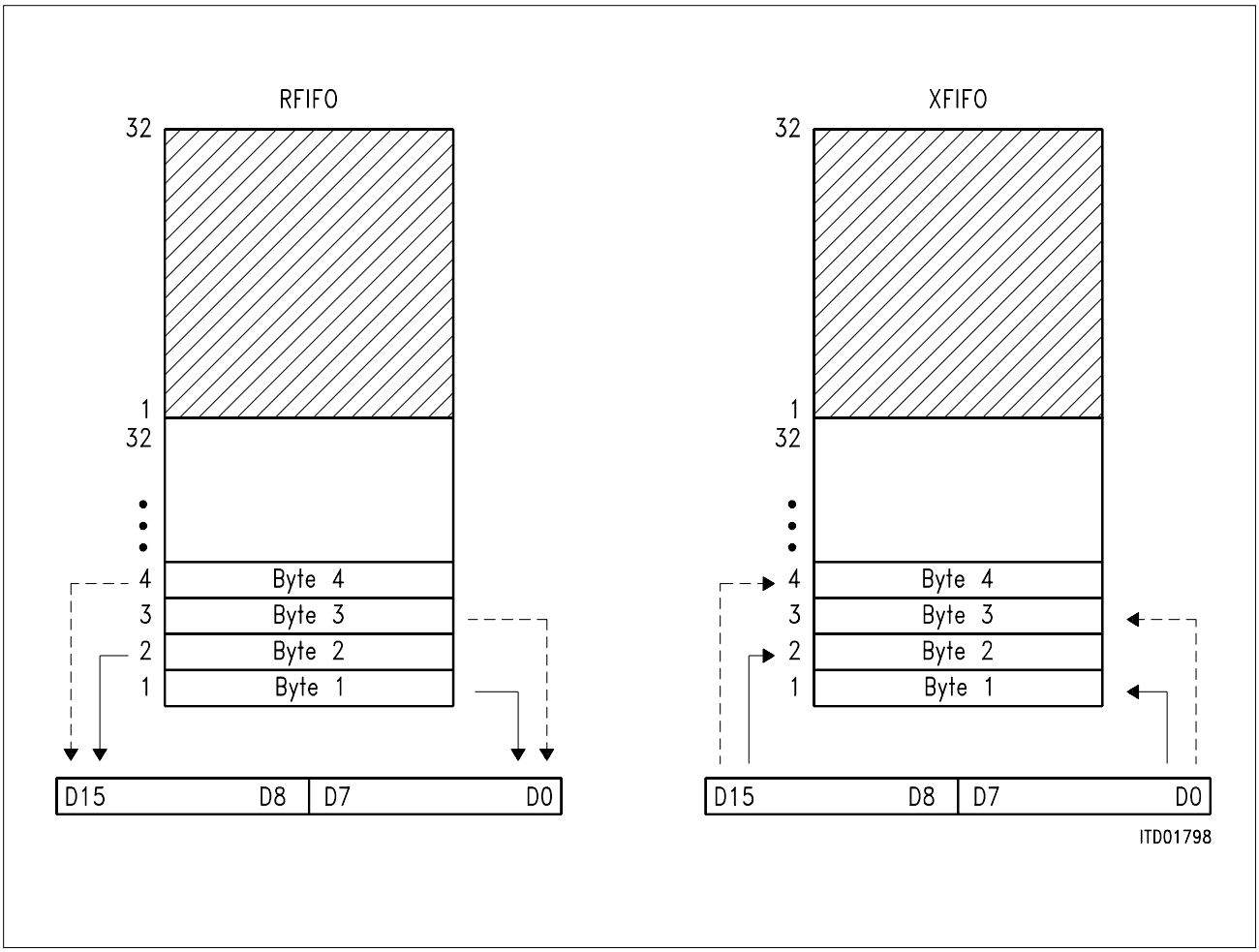


Figure 38
FIFO Word Access (Intel Mode)

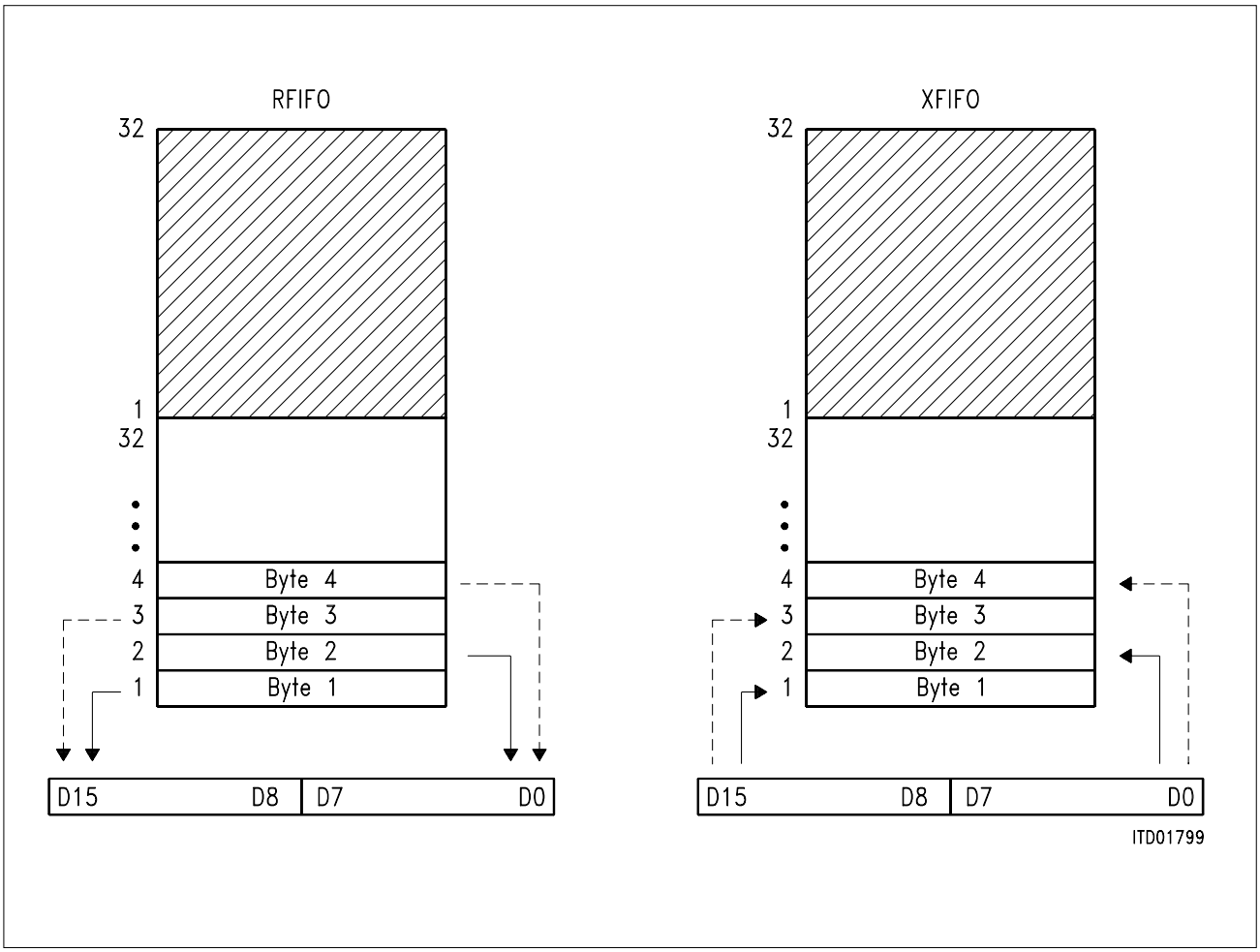


Figure 39
FIFO Word Access (Motorola Mode)

Interrupt Interface

Special events in the FALC54 are indicated by means of a single interrupt output with programmable characteristics (open drain, push-pull; IPC register), which requests the CPU to read status information from the FALC, or to transfer data from/to FALC.

Since only one INT request output is provided, the cause of an interrupt must be determined by the CPU by reading the FALC's interrupt status registers (GIS, ISR0, ISR1, ISR2, ISR3) that means the interrupt at pin INT and the interrupt status bits are reset by reading the interrupt status registers. Register ISR0-3 are from type "Clear on Read".

The structure of the interrupt status registers is shown in **figure 40**.

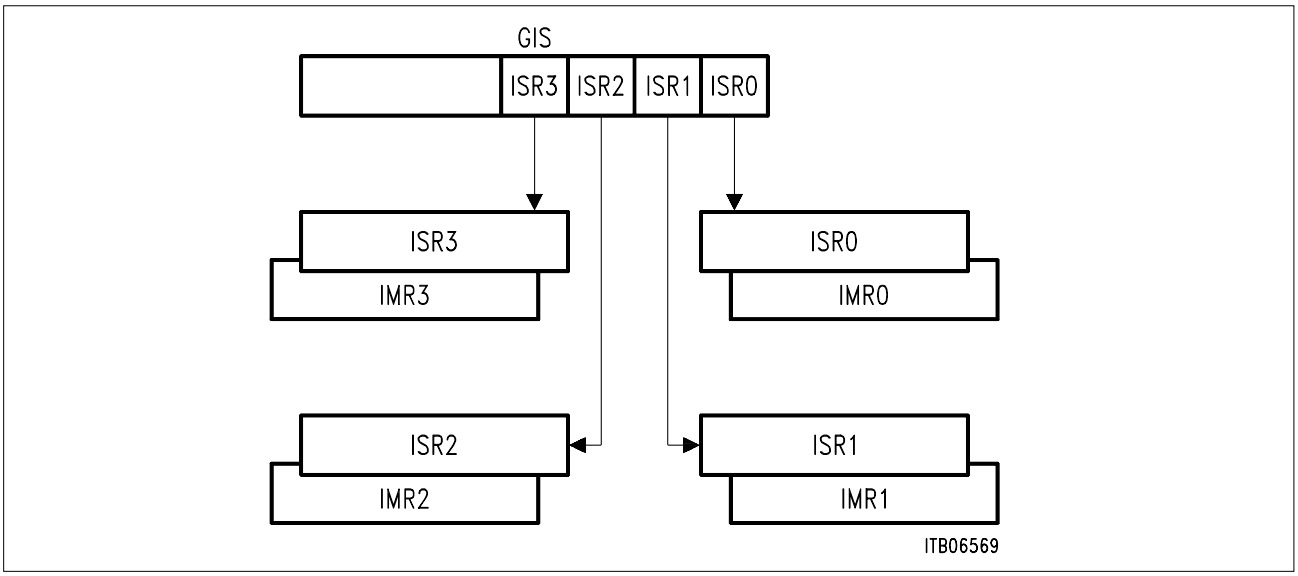


Figure 40
FALC54 Interrupt Status Registers

Each interrupt indication of registers ISR0, ISR1, ISR2 and ISR3 can be selectively masked by setting the corresponding bit in the corresponding mask registers IMR0, IMR1, IMR2, IMR3. If the interrupt status bits are masked they neither generate an interrupt at INT nor are they visible in ISR0-3.

GIS, the non-maskable Global Interrupt Status Register, serves as pointer to pending channel related interrupts. After the FALC54 has requested an interrupt by activating its INT pin, the CPU should first read the Global Interrupt Status register GIS to identify the requesting interrupt source register. After reading the assigned interrupt status registers ISR0- ISR3, the pointer in register GIS is cleared or updated if another interrupt requires service.

If **all** pending interrupts are acknowledged by reading (GIS is reset), pin INT goes inactive.

Updating of interrupt status registers ISR0…3 and GIS is only prohibited during read access.

Masked Interrupts Visible in Status Registers

The Global Interrupt Status register (GIS) indicates those interrupt status registers with active interrupt indications (GIS.ISR0-3).

An additional mode can be selected via bit IPC.VIS.

In this mode, masked interrupt status bits neither generate an interrupt at pin INT nor are they visible in GIS, **but are displayed in the respective interrupt status register(s) ISR0..3**.

This mode is useful when some interrupt status bits are to be polled in the individual interrupt status registers.

Notes:

- *In the visible mode, all active interrupt status bits, whether the corresponding actual interrupt is masked or not, are reset when the interrupt status register is read. Thus, when polling of some interrupt status bits is desired, care must be taken that unmasked interrupts are not lost in the process.*
- *All unmasked interrupt statuses are treated as before.*

Please note that whenever polling is used, all interrupt status registers concerned have to be polled individually (no “hierarchical” polling possible), since GIS only contains information on actually generated - i.e. unmasked-interrupts.

5 General Functions and Device Architecture T1

5.1 Functional Description T1

5.1.1 Receive Path

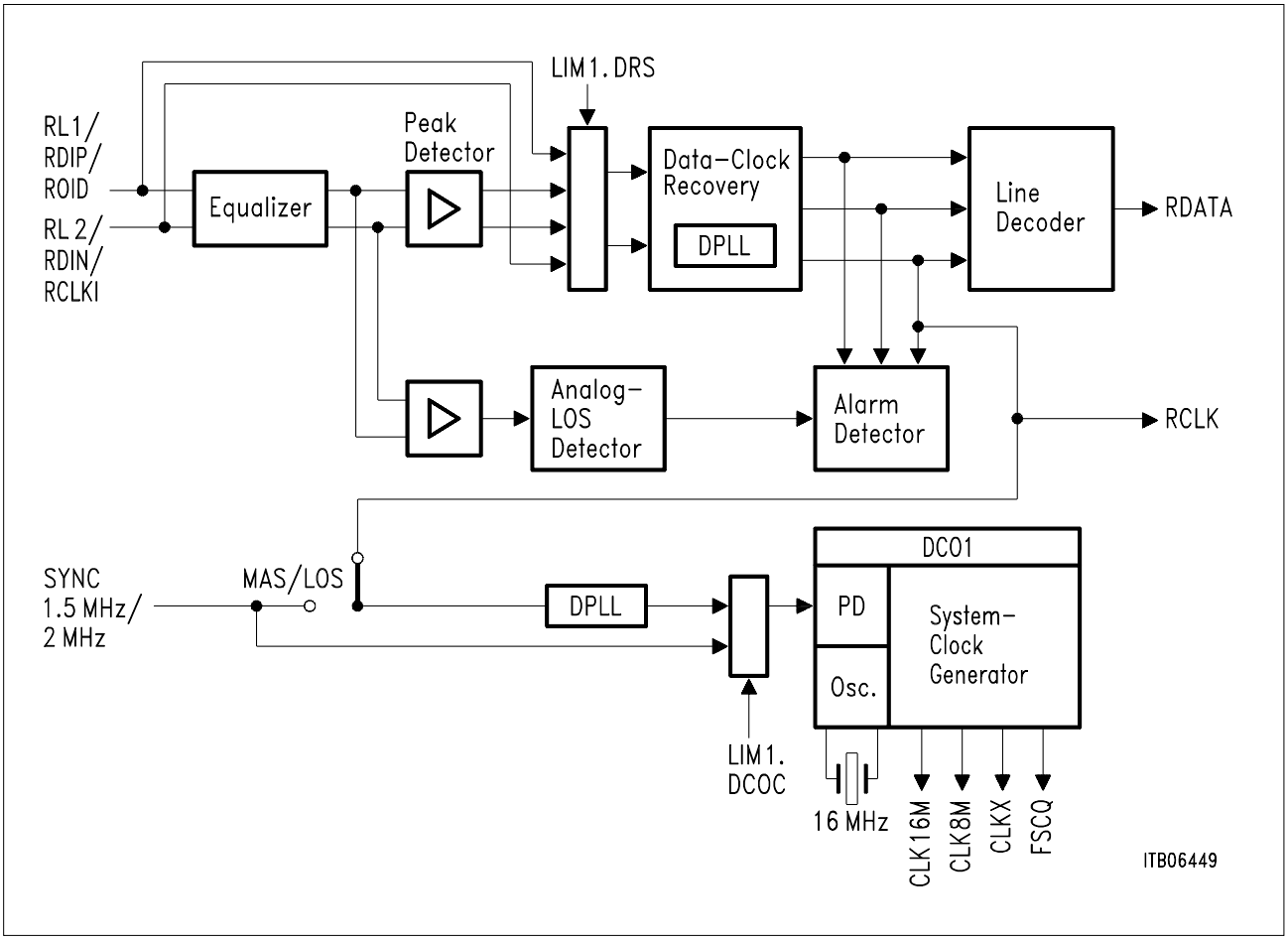


Figure 41
Receive Clock System

Receive Line Interface

For data input, four different data types are supported:

- Ternary coded signals received at multifunction ports RL1 and RL2 from a 6 dB ternary interface. The ternary interface is selected if LIM1.DRS is reset.
- Ternary coded signals received at multifunction ports RL1 and RL2 from a 18 dB ternary interface. The ternary interface is selected if LIM1.DRS is reset.
- Digital dual rail signals received at ports RDIP and RDIN. The dual rail interface is selected if LIM1.DRS and FMR0.RC1 is set.
- Unipolar data at port ROID received from a fibre optical interface. The optical interface is selected if LIM1.DRS is set FMR0.RC1 is reset.

Receive Equalizer

The ITU-T I.431 recommendation requires a minimum loop length of 18 dB for T1 applications. The FALC54 meets this requirement by the integrated receive equalizer. Enabling and disabling the receive equalizer can be performed via a control bit.

Receive Clock and Data Recovery

The analog received signal at port RL1/2 is equalized and then peak-detected to produce a digital signal. The digital received signal at port RDIP/N is directly forwarded to the DPLL. The receive clock and data recovery extracts the route clock RCLK from the received data stream at ports RL1/2, RDIP/RDIN or ROID and converts the data stream into a single rail, unipolar bit stream. The clock and data recovery works with the frequency supplied by XTAL3/4. Normally the clock that is output via pin RCLK is the recovered clock from the signal provided by RL1/2 or RDIP/N and has a duty cycle close to 50 %. The free run frequency is defined by XTAL3/4 devided by 8 in periods with no signal.

Receive Line Coding

A selection between B8ZS or simple AMI (ZCS) coding is employed for the ternary or the dual rail interface. In this case, all code violations that do not correspond to zero substitution rules will be detected. The detected errors increment the code violation counter (16 bits length).

In the optical interface mode the NRZ coding is automatically performed.In this case data will be latched with the falling edge of pin RCLKI.

When using the optical interface with NRZ coding, the decoder is by-passed and no code violations will be detected.

Additionally, the receive line interface comprises the alarm detection for Alarm Indication Signal AIS (Blue Alarm) and the Loss of Signal LOS (Red Alarm).

The signal at the ternary interface is received at both ends of a transformer.

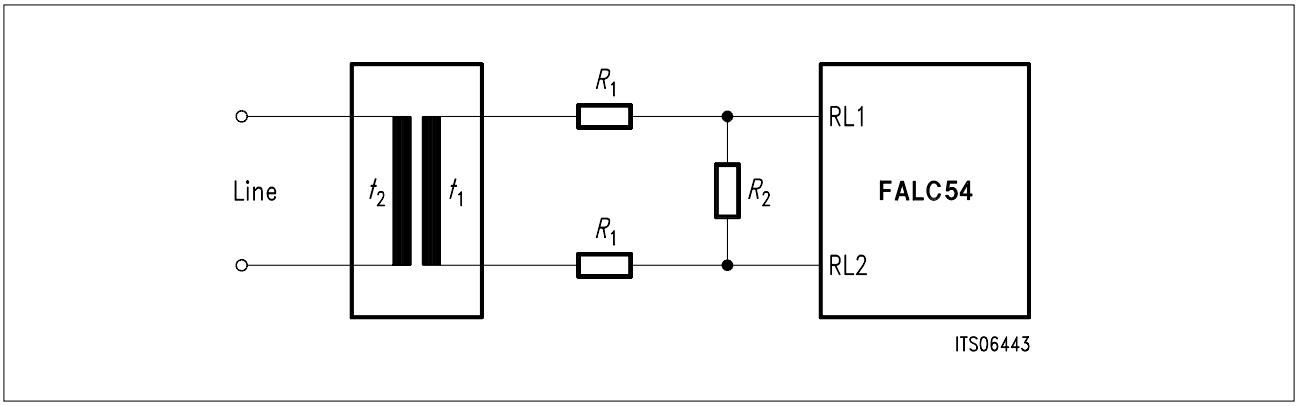


Figure 42
Receiver Configuration

Table 14
Recommended Receiver Configuration Values

Parameter	Characteristic Impedance 100 Ω	
	DS1 (6 dB)	T1 (18 dB)
R_1 (± 2.5 %) [Ω]	0	0
$t_2 : t_1$	1 : $\sqrt{2}$	1 : $\sqrt{2}$
R_2 (± 2.5 %) [Ω]	200	200

Jitter free system clocks (16 MHz / 8 MHz / 4 MHz / 2 MHz and 8 kHz) are generated by the internal PLL circuit DCO1. The DCO1 can work in two different modes:

- Slave mode
  In Slave mode (LIM0.MAS = 0), the DCO1 will be synchronized on the recovered route clock. In case of LOS the DCO1 switches automatically to Master mode.
- Master mode
  In Master mode (LIM0.MAS = 1), the oscillator is in free running mode if pin SYNC is connected to VSS. If there is a frequency of 1.544 MHz (LIM1.DCOC = 0) or 2.048 MHz (LIM1.DCOC = 1) at the SYNC input the DCO1 is then synchronized to this input.

Loss of Signal Detection

There are different definitions for detecting Loss of Signal alarms (LOS) in the ITU-T G.775 and AT&T TR 54016. The FALC54 covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable via register IPC.SCI.

- Detection:
  An alarm will be generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” in the digital receive interface means a logical zero on pins RDIP/RDIN/ROID. A pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS=0). The receive signal level Q is programmable via three control bits LIM1.RIL2-0 in a range of about 1400 to 200 mV differential voltage between pins RL1/2. The number N can be set via a 8 bit register PCD. The contents of the PCD register will be multiplied by 16, which results in the number of pulse periods, or better, the time which has to suspend until the alarm has to be detected. The range results therefore from 16 to 4096 pulse periods.
- Recovery:
  In general the recovery procedure starts after detecting a logical ‘one’ (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM1.RIL2-0) of the nominal pulse. The value in the 8 bit register PCR defines the number of pulses (1 to 255) to clear the LOS alarm. Additional recovery conditions may be programmed by register LIM2.

Jitter Attenuator

Together with a PLL and a tunable crystal attenuation of received input jitter is done in the clock- and data-recovery and either in the received elastic buffer (2 frames) or in the jitter attenuator “JATT“ block of figure 3. The attenuator consists of a 288 Bit FIFO. The FIFO is placed in the transmitter and will be active if bit LIM1.JATT=1 , Remote Loop active.

The jitter attenuator meets the jitter transfer requirements of the PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and Rec. I.431 and G.703 (refer to **figure 43**).

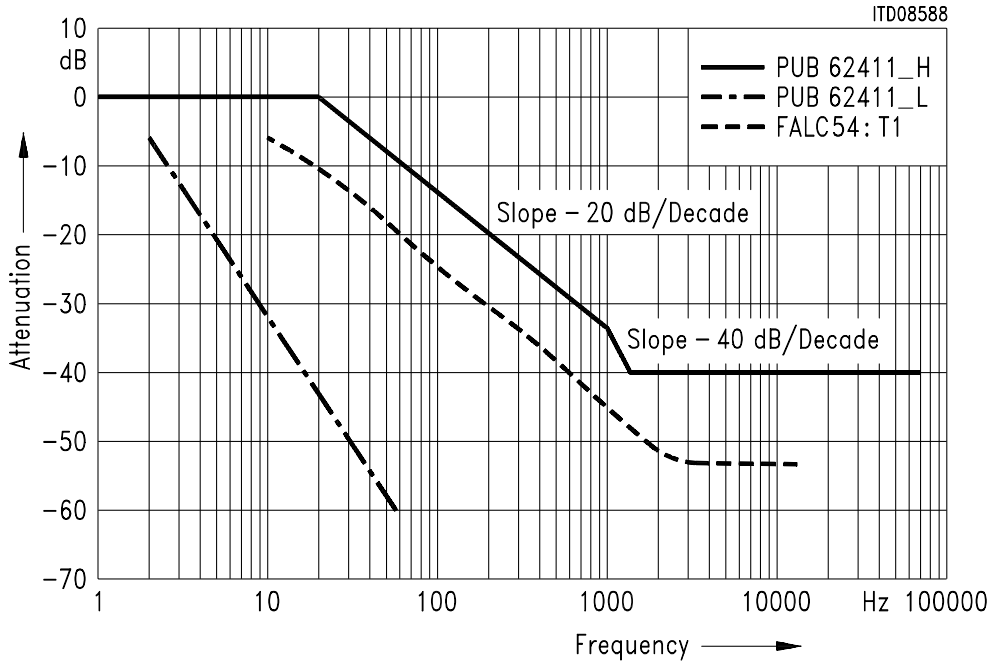


Figure 43
Jitter Attenuation Performance

Jitter Tolerance

The FALC54 receiver's tolerance to input jitter complies to ITU and Bellcore requirements and T1 application.

Figure 44 shows the curves of different input jitter specifications stated above as well as the FALC54 performance.

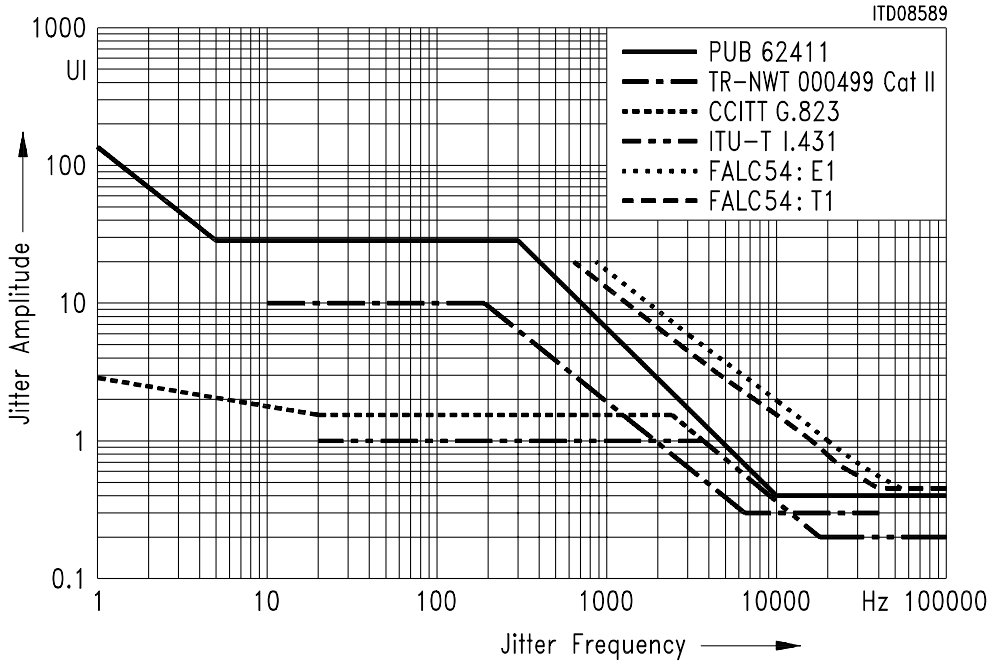


Figure 44
Jitter Tolerance

Output Jitter

In the absence of any input jitter the FALC54 generates the output jitter, which is specified in table below.

Specification	Measurement Filter Bandwidth		Output Jitter (UI peak to peak)
	Lower Cutoff	Upper Cutoff	
PUB 62411	10 Hz	8 kHz	< 0.02
	8 kHz	40 kHz	< 0.025
	10 Hz	40 kHz	< 0.025
	Broadband		< 0.05

Clock Generation and Clock Modes

The high performance integrated Clock Generator meets the recommendations of ITU-T G.735 and I.431 in case of input jitter tolerance, jitter transfer characteristic and output jitter. The following table shows the clock modes with the corresponding synchronization sources.

Mode	Internal LOS Active	SYNC Input	System Clocks
Master	no	GND	Free Running (oscillator centered)
Master	no	1.544 MHz	Synchronized on SYNC input (external 1.544 MHz)
Slave	no	GND	Synchronized on Line (RCLK)
Slave	no	1.544 MHz	Synchronized on Line (RCLK)
Slave	yes	GND	Free Running (oscillator centered)
Slave	yes	1.544 MHz	Synchronized on SYNC input (external 1.544 MHz)

The clock generator unit fulfills three main tasks. One is, to provide jitter free system clocks either derived from the line or from an external input. The other task is to produce a transmission clock for T1 applications (according to the recommendations). The third is to ensure output jitter characteristics in case jittered SCLKX clock.

The system clocks are provided by the DCO1 (16 M, 8 M, 4/2 M, 8 k). The recovered route clock is first transformed to 2.048 MHz by a digital PLL (in Slave Mode). The jitter transfer characteristic is given by a corner frequency of 6 Hz and 20 dB per decade fall off.

The main task of DCO2 is to generate the transmit clock. A 12.352 MHz crystal has to be connected to the DCO2. The Xslicer function is automatically enabled in the T1 mode. This results from the different frequencies of the line and system interface. The jitter transfer characteristics is given by a corner frequency of 6 Hz and 20 dB per decade fall off.

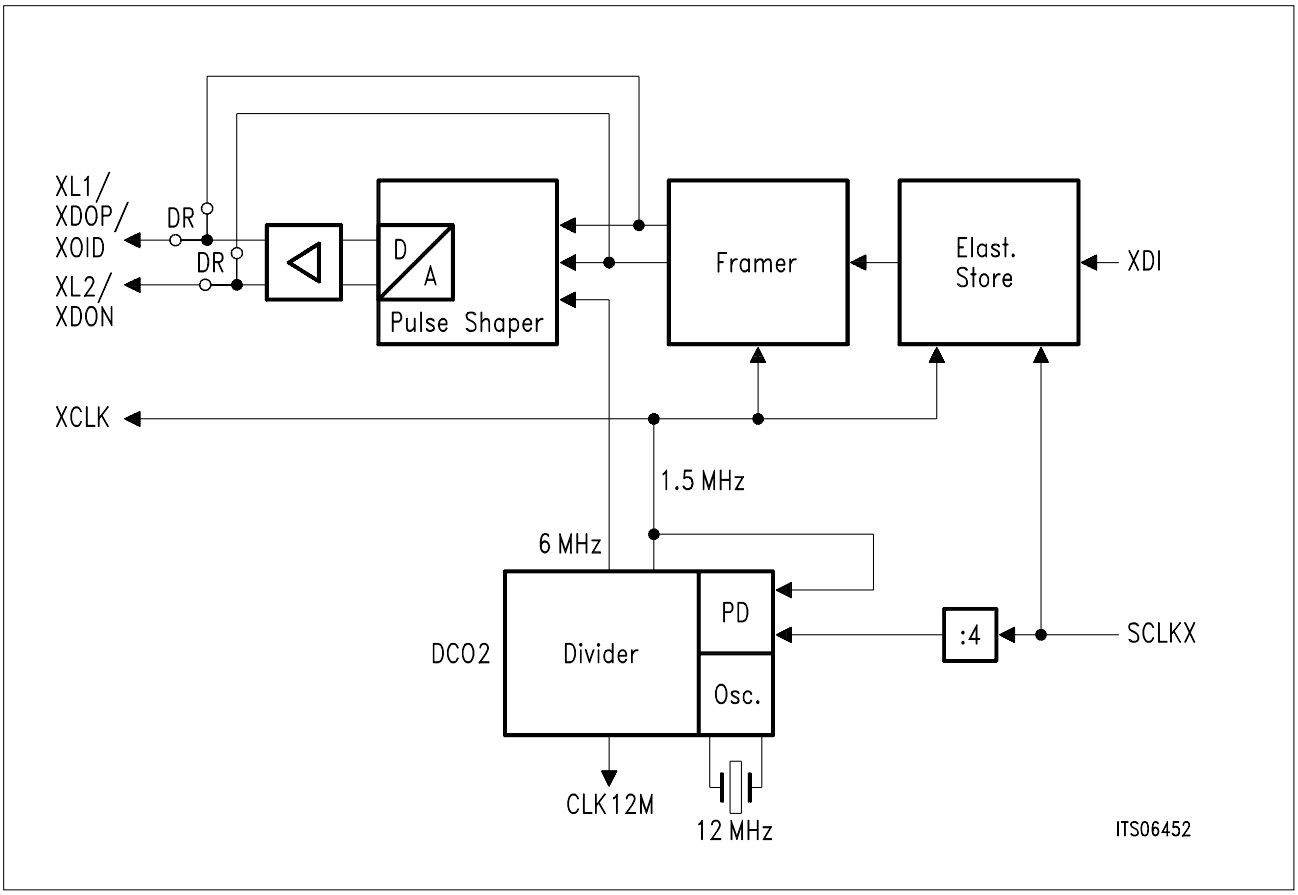


Figure 45
Transmit Clock System

Framer/Synchronizer

The following functions are performed:

- Synchronization on pulse frame
- Synchronization on multiframe
- Error indication when synchronization is lost. In this case, AIS is automatically sent to the system side and Remote Alarm to the remote end if en/disabled.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This may be automatically done by the FALC54 or user controlled via the microprocessor interface.
- Detection of remote alarm (yellow alarm) indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in special status registers.
- Detection of framed or unframed in band Loop Up/Down Code
- Generation of various interrupt statuses of the receiver functions. These interrupts can be masked.
- Generation of control signals to synchronize the CRC checker, and the receive elastic store write control unit.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC multiframe according to the CRC 6 procedure (refer to **ITU-T Rec. G.704**). These bits are compared with those check bits that are received during the next CRC multiframe. If there is at least one mismatch, the CRC error counter (16 bit) will be incremented.

Receive Elastic Store

The received bit stream is stored in the receive elastic store. The memory is organized as a two-frame elastic buffer with a size of 48 $\times$ 8 bit.

The functions are:

- Clock adaption between system clock (SCLKR) and internally generated route clock (RCLK)
- Compensation of input wander and jitter. Maximum of wander amplitude (peak-to-peak):
  142 UI in channel translation mode 0
  78 UI in channel translation mode 1
  (1 UI = 644 ns)
- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel, channel-serial data which is circularly written to the elastic store using internally generated Receive Route Clock (RCLK).

Reading of stored data is controlled by the System Clock (SCLKR) and the Synchronous Pulse ($\overline{\text{SYPR}}$) in conjunction with the programmed offset values for the receive time-slot/clock-slot counters. After conversion into a serial data stream, the data is given out via port RDO.

The 24 received channels are translated into the 32 system channels by a fixed organization. Unequipped time-slots will be set to 'FF_H'.

Two bit rates (2048/4096 kbit/s) are selectable via the microprocessor interface.

In 4096 kbit/s interface mode each channel will be sent out on two different channel-phases. Each channel-phase which should be tri-stated is programmable.

Figure 46 gives an idea of operation of the receive elastic store:
A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the write pointer is within the slip limits (S +, S –). The values of S + and S – depend on the selected channel translation mode. If a slip condition is detected, a negative slip (the next received frame is skipped) or a positive slip (the previous received frame is read out twice) is performed at the system interface, depending on the difference between RCLK and SCLKR/4, i.e. on the position of pointer R and W within the memory.

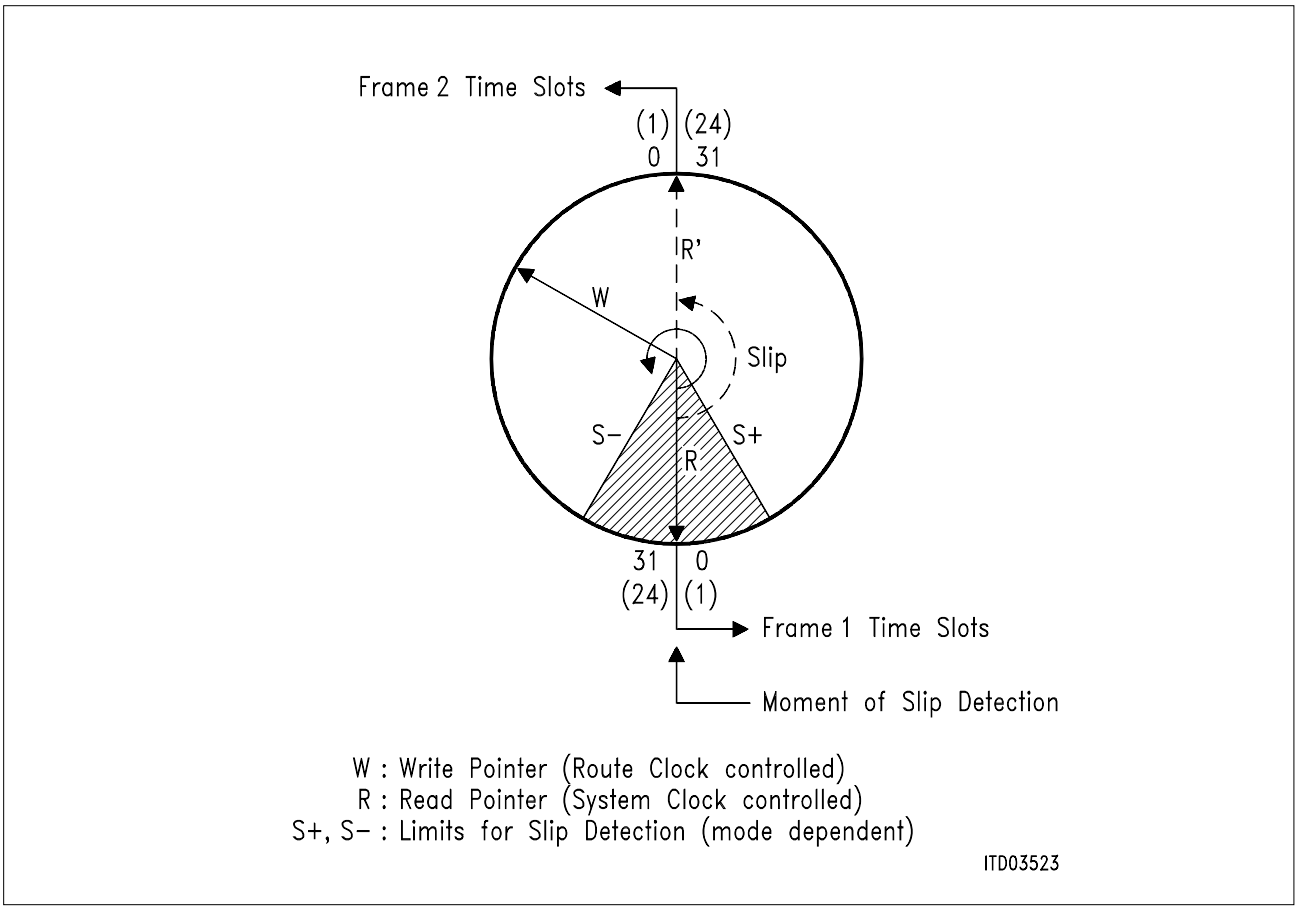


Figure 46
The Receive Elastic Store as Circularly Organized Memory

Receive Signaling and Maintenance Controller

The receive signaling controller can be programmed to operate in various signaling modes. The FALC54 will perform the following signaling and data link methods:

- Message Oriented Signaling also called Common Channel Signaling CCS
- CAS-Bit Robbing CAS-BR
- Bit Oriented Messages in ESF-DL
- 4 kbit/s Data Link Access in F72 Format

The signaling information is carried in TS24 (CCS) or in one bit of every sixth frame for each channel which contains signaling information (Bit Robbing Signaling).

The signaling controller samples the bit stream which is output on pin RDO.

In case of robbed bit signaling data is sampled on the receive line side clocked with the extracted receive route clock and stored in registers RS1-12.

In case of common channel signaling the signaling procedure HDLC/SDLC will be supported. The received data flow and the address recognition features can be performed in very flexible way, to satisfy almost any practical requirements. Depending

on the selected address mode, the FALC54 can perform a 1 or 2 byte address recognition. All frames with valid addresses are forwarded directly via the Receive FIFO (RFIFO) to the system memory. The HDLC control-field, data in the I-field and an additional status byte are temporarily stored in the RFIFO.

In transparent mode, fully transparent data reception without HDLC framing is performed, i.e. without FLAG recognition, CRC checking or bit-stuffing. This allows the user specific protocol variations. The received data are stored in the RFIFO.

The FALC54 offers the flexibility to extract data during certain time-slots which are defined via registers RTR1-4 and TTR1-4. Any combination of time-slots can be programmed independent for the receive and transmit direction.

If the FALC54 is optioned for no signaling, the channels in the data stream from the system interface will pass the FALC54 undisturbed.

Bit Oriented Messages

The FALC54 supports signaling and maintenance functions for T1 - Primary Rate Interfaces using the Extended Super Frame format. The device supports the DL-channel protocol for ESF format according to T1.403 ANSI specification or according to AT&T TR54016. The HDLC- and Bit Oriented Message (BOM) -Receiver can be switched ON/OFF independently. To support the ESF-DL protocol according AT&T TR54016 or if the FALC54 is used for HDLC formats only, the BOM receiver has to be switched off (MODE.BRAC=0). If HDLC- and BOM-receiver has been switched on (MODE:BRAC/HRAC=1), an automatic switching between HDLC and BOM mode is enabled. Two different BOM reception modes may be programmed (CCR1.BRM).

4 Kbit/s Data Link Access in F72 Format

The FALC54 supports the DL-channel protocol using the F72 (SLC96) format in two ways.

First: Sampling of DL bits is done on a multiframe basis and stored in the registers RDL1-3. A receive multiframe begin interrupt is provided to read the received data DL bits. The contents of registers XDL1-3 is subsequently sent out on the transmit multiframe basis if it is enabled via FMR1.EDL. A transmit multiframe begin interrupt requests for writing new information to the DL-bit registers.

Second: The DL bit information from frame 26 to 72 is stored in the Receive FIFO of the signaling controller.The DL bits stored in the XFIFO are inserted in the outgoing datastream, if it is enabled via CCR1.EDLX. If CCR1.EDLX is cleared a HDLC or No-HDLC frame could be sent or received via the RFIFO / XFIFO.

5.1.2 Transmit Path

The inverse functions are performed for the transmit direction.

The PCM data is received from the system internal highway at port XDI with 2048 kbit/s or 4096 kbit/s. The channel assignment is equivalent to the receive direction. All unequipped (idle) time-slots will be ignored.

The contents of selectable channels (time-slots) can be overwritten by the pattern defined via register IDLE. The selection of “idle channels” is done by programming the three-byte registers ICB1 … ICB3.

Internal multiplexing of (speech) data and signaling data can be disabled on a per channel basis (Clear Channel Capability). This is also valid when using the internal signaling controller.

Latching of data is controlled by the System Clock (SCLKX) and the Synchronous Pulse (SYPXQ) in conjunction with the programmed offset values for the Transmit Time-slot/Clock-slot Counters.

Transmit Signaling Controller

Similar to the receive signaling controller the same signaling methods and the same time-slot assignment are provided. The signaling information has to be written in the Transmit FIFO (XFIFO). With a Transmit Frame command the signaling information will be sent in the corresponding signaling bit positions. The signaling will be internally multiplexed with the data at port XDI.

If the transparent mode is selected, the FALC54 supports the continuous transmission of the contents of the transmit FIFO. The cyclic transmission continuous until the Transmitter Reset command (CMDR.SRES) is issued or CMDR.XREP is reset.

In case of CCS the signaling procedure HDLC/SDLC is supported with generation of Preambles and FLAGs, CRC generation and bit-stuffing. For HDLC frames, the address and the control fields have to be entered in the XFIFO as well.

Operating in HDLC or BOM mode “flags” or “idle” may be transmitted as interframe timefill.

Transmit Elastic Store

The transmit elastic store with a size of 24 × 8 bit (one-frame) serves as a temporary store for the PCM data to adapt the system clock (SCLKX) to the internally generated clock for the transmit data, and to re-translate channel structure used in the system to that of the line side. Its optimal start position is initiated when programming the above offset values. A difference in the effective data rates of system side and transmit side may lead to an overflow/underflow of the transmit memory: thus, errors in data transmission to the remote end may occur. This error condition (transmit slip) is reported to the microprocessor via an interrupt status register.

Maximum wander amplitude (peak-to-peak):
58 UI in channel translation mode 0
46 UI in channel translation mode 1
(1 UI = 644 ns)

Because this is, under normal circumstances, a rare error condition no automatic action is taken by the transmit elastic store as opposed to the receive elastic store in the case of a positive or negative slip. In this case the FALC54 requires a re-initialization of the transmit memory by re-programming the transmit time-slot counter. After that, this memory has its optimal start position.

Transmitter

The serial bit stream is then processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the four selectable framing formats
- Insertion of service and data link information
- AIS generation (Blue Alarm)
- Remote alarm (yellow alarm) generation
- CRC generation and insertion of CRC bits
  CRC bits inversion in case of a previously received CRC error or in case of activating per control bit
- Generation of Loop Up/Down code

The multiframe boundries of the transmitter may be externally synchronized by using the XMFS pin. This feature is required if signaling-, service- and data link bits are routed through the switching network and are inserted in transmit direction via the system interface.

Transmit Line Interface

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided by pin XDI and the digital transmitter.

Similar to the receive line interface three different data types are supported:

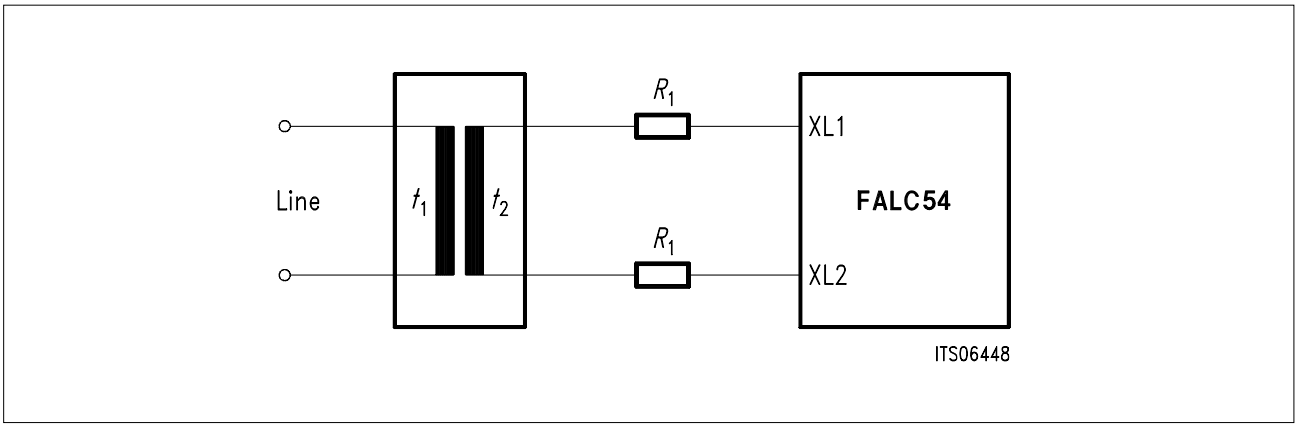


Figure 47
Transmitter Configuration

Table 15
Recommended Transmitter Configuration Values

Parameter	Characteristic Impedance 100 Ω	
	DS1 (6 dB)	T1 (18 dB)
R_1 (± 2.5 %) [Ω]	5	5
$t_2 : t_1$	1 : $\sqrt{2}$	1 : $\sqrt{2}$

- Ternary Signal
  Single rail data is converted into a ternary signal which is output on pins XL1 and XL2. Selection between B8ZS or simple AMI coding with zero code suppression (B7 stuffing) is provided. B7 stuffing can be disabled on a per channel basis (clear channel capability). Selected by FMR0.XC1/0 and LIM1.DRS = 0.
- Dual rail data PCM(+), PCM(-) at multifunction ports XDOP and XDON with 50 % or 100 % duty cycle and with programmable polarity. Line coding is done in the same way as in the ternary interface. Selected by FMR0.XC1=1 and LIM1.DRS = 1.

Unipolar data at port XOID will be transmitted in NRZ (Non Return to Zero) with 100 % duty cycle to a fibre optical interface. Clocking off data is done with the rising edge of the transmit clock XCLK (1544 kHz) and with a programmable polarity. Selection is done by FMR0.XC1 = 0 and LIM1.DRS = 1.

The FALC54 includes a programmable pulse shaper to satisfy the requirements of the AT&T Technical Advisory # 34 at the cross connect point for T1 applications. The amplitude of pulse shaper is individually programmable via the microprocessor interface to allow a maximum of different pulse templates. The line length is selected by programming the registers XPM2-0 as shown for typical values in table below. The values based on simulations with transformer ratio: 1:sqrt(2); cable: PULB 22AWG (100 Ω); serial resistors: 5 Ω. The XPM register values are in decimal.

Range in m	XP04-XP00	XP14-XP10	XP24-XP20	XP34-XP30
0 - 35	29	27	10	3
25 - 65	29	28	10	3
55 - 95	31	28	10	2
85 - 125	31	27	13	2
115 - 155	31	26	13	2
145 - 185	31	26	13	3
175 - 210	31	25	14	3

The transmitter requires an external step up transformer to drive the line.

Transmit Line Monitor

The transmit line monitor compares the transmit line pulses on XL1 and XL2 with the transmit input signals received on pins XL1M and XL2M. The monitor detects faults on the primary side of the transformer and protects the device from damage by setting the transmit line driver XL1/2 automatically in a high impedance state. Faults on the secondary side may not be detected. To detect a short the configuration in **figure 47** and the reset values of register XPM0-2 has to be fulfilled. Otherwise the short detection could not be guaranteed. Two conditions will be detected by the monitor: Transmit Line ones density (more than 31 consecutive zeros) and Transmit Line Shorted. In both cases a transmit line monitor status change interrupt will be provided.

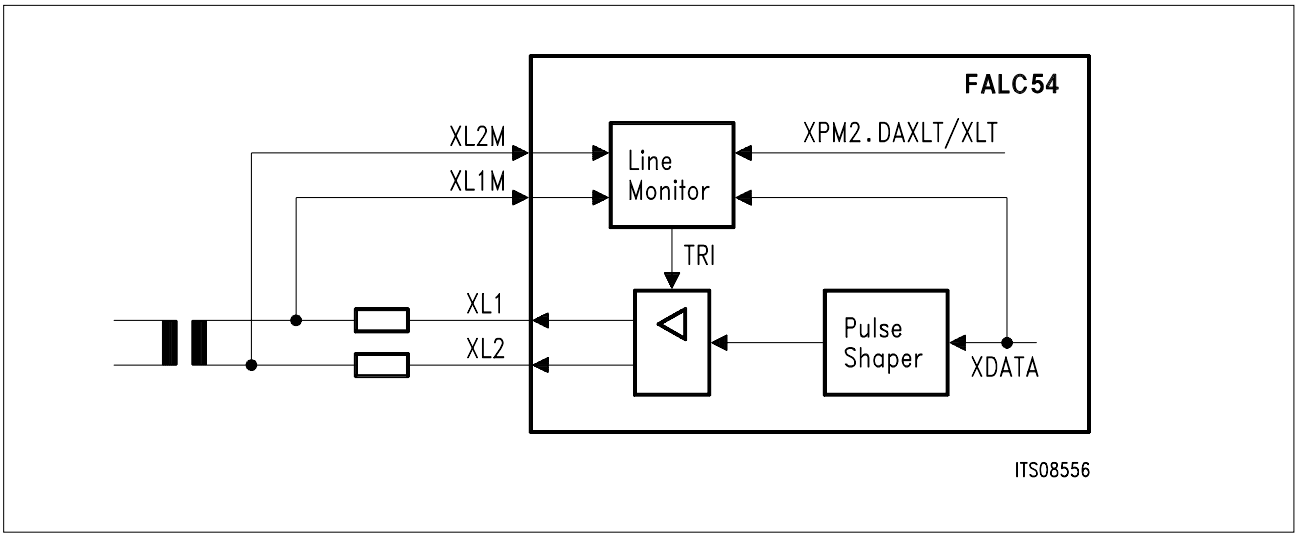


Figure 48
Transmit Line Monitor Configuration

5.1.3 Additional Functions

Clear Channel Capability

For support of common T1 applications, clear channels can be specified via the 3-byte register bank CCB1 … CCB3. In this mode the contents of selected channels will not be overwritten by bit robbing and Zero Code Suppression (B7 stuffing) information.

Idle Code Insertion

In transmit direction, the contents of selectable channels can be overwritten by the pattern defined via register IDLE. The selection of “idle channels” is done by programming the three-byte registers ICB1 … ICB3.

Loop Up/Down Code Detection and Generation

The FALC54 detects a framed or unframed Loop Up/actuate (00001)- and Down/deactuate (001) pattern with bit error rates as high as 1/100. Framing bits are excluded from loop code detection. Status and interrupt-status bits will inform the user whether Loop Up - or Loop Down code was detected.

In transmit direction replacing normal transmit data with Loop Up- or Loop Down code is done via control bits. However framing pattern will overwrite the Loop code.

Transparent Mode

The described transparent modes are useful for loopbacks or for routing signaling information through the system interface.

Setting bit FMR4.TM switches the FALC54 in transparent mode:

In receive direction all bits in F-bit position of the incoming multiframe are forwarded to RDO and inserted in the FS/DL time-slot. In asynchronous state the received data can be transparently switched through if bit FMR2.DAIS is set. Bit RDCF (bit 1 of FS/DL time-slot) indicates a DL bit.

In transmit direction bit 8 of the FS/DL time-slot from the system internal highway (XDI) is inserted in the F-bit position of the outgoing frame. For complete transparency the internal signaling controller and Line Loop Back has to be disabled and “Clear Channels” have to be defined via registers CCB1…3.

Pulse Density Detection

The FALC54 examines the receive data stream on the pulse density requirement which is defined by ANSI T1. 403. More than 15 consecutive zeros or less than N ones in each and every time window of 8(N+1) data bits where N=23 will be detected. Violations of these rules are indicated by setting the status bit FRS1.PDEN and the interrupt status bit

ISR0.PDEN. Generation of the interrupt status can be programmed either with the detection or with any change of state of the pulse density alarm (IPC.SCI).

System Clocks and System Pulses for Transmitter and Receiver

The FALC54 offers a flexible feature for system designers where different system clocks and system pulses are necessary. The interface to the receive system highway will be clocked via pin SCLKR, while the interface to the transmit system highway is clocked via pin SCLKX. The frequency on pin SCLKR/X must fixed 8.192 MHz.

The signals on pin $\overline{\text{SYPR}}$ in conjunction with the assigned timeslot offset in register RC0 and RC1 will define the beginning of a frame on the receive system highway. The signal on pin $\overline{\text{SYPX}}$ in conjunction with the assigned timeslot offset in register XC0 and XC1 will define the beginning of a frame on the transmit system highway.

Error Performance Monitoring

The FALC54 supports the error performance monitoring by detecting following alarms in the received data.

- Framing errors
- CRC errors
- Code violations
- Loss of frame alignment
- Loss of signal
- Alarm indication signal
- Slip

With a programmable interrupt mask (register IMR4) all these error events could generate an Errored Second interrupt (ES) if enabled. Additionally a one Second interrupt could be generated to indicate that the ES interrupt has to be read. If the ES interrupt is set the enabled alarm status bits or the error counters have to be examined.

Additionally an 16 bit wide Errored Block Counter is realized. In ESF format this counter will be incremented once per multiframe if a multiframe has been received with a CRC error or an errored frame alignment has been detected.

Automatic Remote Alarm (Yellow Alarm) Access

If the receiver has lost its synchronization a remote alarm (yellow alarm) could be sent if enabled via bit FMR2.AXRA to the distant end. The remote alarm will be automatically generated in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit will be removed.

5.1.4 Operating Modes T1

General

Activated with bit FMR1.PMOD = 1.

PCM line bit rate : 1544 kbit/s
Single frame length : 193 bit, No. 1 … 193
Framing frequency : 8 kHz
Organization : 24 time-slots, No. 1 … 24
with 8 bits each, No. 1 … 8 and one preceding F bit

Selection of one of the four permissible framing formats is performed by bits FMR4.FM0 and FMR4.FM1. These formats are:

F4 : 4-frame multiframe
F12 : 12-frame multiframe (D4)
ESF : Extended Superframe
F72 : 72-frame multiframe (SLC96)

The operating mode of the FALC54 is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme.

The FALC54 implements all of the standard and/or common framing structures PCM 24 (T1, 1544 kbit/s) carriers. These are summarized in table 6, along with the signaling types applicable in each of the multiframe formats. “General signaling” refers to the support the FALC54 provides for handling the data link or service bits, as the case may be, in the multiframe.

Table 16
Summary of FALC54 Framing and Supported Signaling Modes

	4-Frame Multiframe	**12-Frame Multiframe**	**Extended Multiframe**	**Remote Switch M.**
CRC	–	–	CRC6	–
Signaling				
CCS	e.g. Ch 24	e.g. Ch 24	e.g. Ch 24	e.g. Ch 24
CAS-CC	e.g. Ch 24	e.g. Ch 24	e.g. Ch 24	e.g. Ch 24
CAS-BR	–			
General Signaling	FS bits	–	DL bits	FS bits

CCS = Common Channel Signaling
CAS-CC = Channel Associated Signaling (Common Channel)
CAS-BR = Channel Associated Signaling (Bit Robbing)

For CCS, CAS-CC, and CAS-BR, different types of support are provided.

Note: The internal HDLC- or CAS Controller supports all signaling procedures like signaling frame synchronization / synthesis and signaling alarm detection.

The next pages give a general description of the framing formats. After RESET, the FALC54 must be programmed with FMR1.PMOD = 1.

Line Interfacing

- Ternary data with B8ZS or AMI (ZCS) coding (selection via bit FMR0.XC1/0+ RC1/0). All code violations which do not correspond to zero code substitution rules are registrated by the Code Violation Counter (CVC) with 16 bit length.
  If AMI coding with zero code suppression (B7-stuffing) is selected, "**clear channels**" without B7-stuffing can be defined by programming registers CCB1 … CCB3.
- Single rail unipolar data with no zero suppression algorithm (FMR0.XC1or RC1 = 0).

General Aspects of Synchronization

Synchronization status is reported via bit FRS0.LFA (Loss Of Frame Alignment). Framing errors (pulse frame and multiframe) are counted by the Framing Error Counter FEC.

Asynchronous state is reached if
2 out of 4 (bit FMR4.SSC1/0 = 00), or
2 out of 5 (bit FMR4.SSC1/0 = 01), or
2 out of 6 (bit FMR4.SSC1/0 = 10)
framing bits (terminal framing or multiframing) are incorrect. If auto-mode is enabled, counting of framing errors is interrupted.

The resynchronization procedure can be controlled by either one of the following procedure:

- Automatically (FMR4.AUTO = 1). Additionally, it may be triggered by the user by setting/resetting one of the bits FMR0.FRS (Force Resynchronization) or FMR0.EXLS (External Loss of Frame).
- User controlled, exclusively, via above control bits in the non-auto-mode (FMR4.AUTO = 0).

Addition for F12 and F72 Format

FT and FS bit conditions, i.e. pulse frame alignment and multiframe alignment can be handled separately if programmed via bit FMR2.SSP. Thus, a multiframe re-synchronization can be automatically initiated after detecting 2 errors out of 4/5/6 consecutive multiframing bits without influencing the state of the terminal framing.

In the synchronous state, the setting of FMR0.FRS or FMR0.EXLS resets the synchronizer and initiates a new frame search. The synchronous state is reached if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state.

In asynchronous state, the function of FMR0.EXLS is the same as above. Setting bit FMR0.FRS induces the synchronizer to lock onto the next available framing candidate if there is one. Otherwise, a new frame search is started. This is useful in case the framing pattern that defines the pulseframe position is imitated periodically by a pattern in one of the speech/data channels.The F-bit Error History (FRS3.FEH5 … 0) may be used in the decision whether to initiate resynchronization.

The updating of these bits depends on the resynchronization mode:

- Auto-mode: updating only during the synchronous state.
- Non-auto mode: updating during the synchronous state and until one of the above control bits are set during the asynchronous state.

The control bit FMR0.EXLS should be used first because it starts the synchronizer to search for a definite framing candidate.

To observe actions of the synchronizer, the Frame Search Restart Flag FRS0.FSRF is implemented. It toggles at the start of a new frame search if no candidate has been found at previous attempt.

When resynchronization is initiated, the following values apply for the time required to achieve the synchronous state in case there is one definite framing candidate within the data stream:

Table 17
Resynchronization Timing

Frame Mode	Avg.	Max.	Units
F4	1.0	1.5	ms
F12	3.5	4.5	
ESF	3.4	6.125	
F72	13.0	17.75	

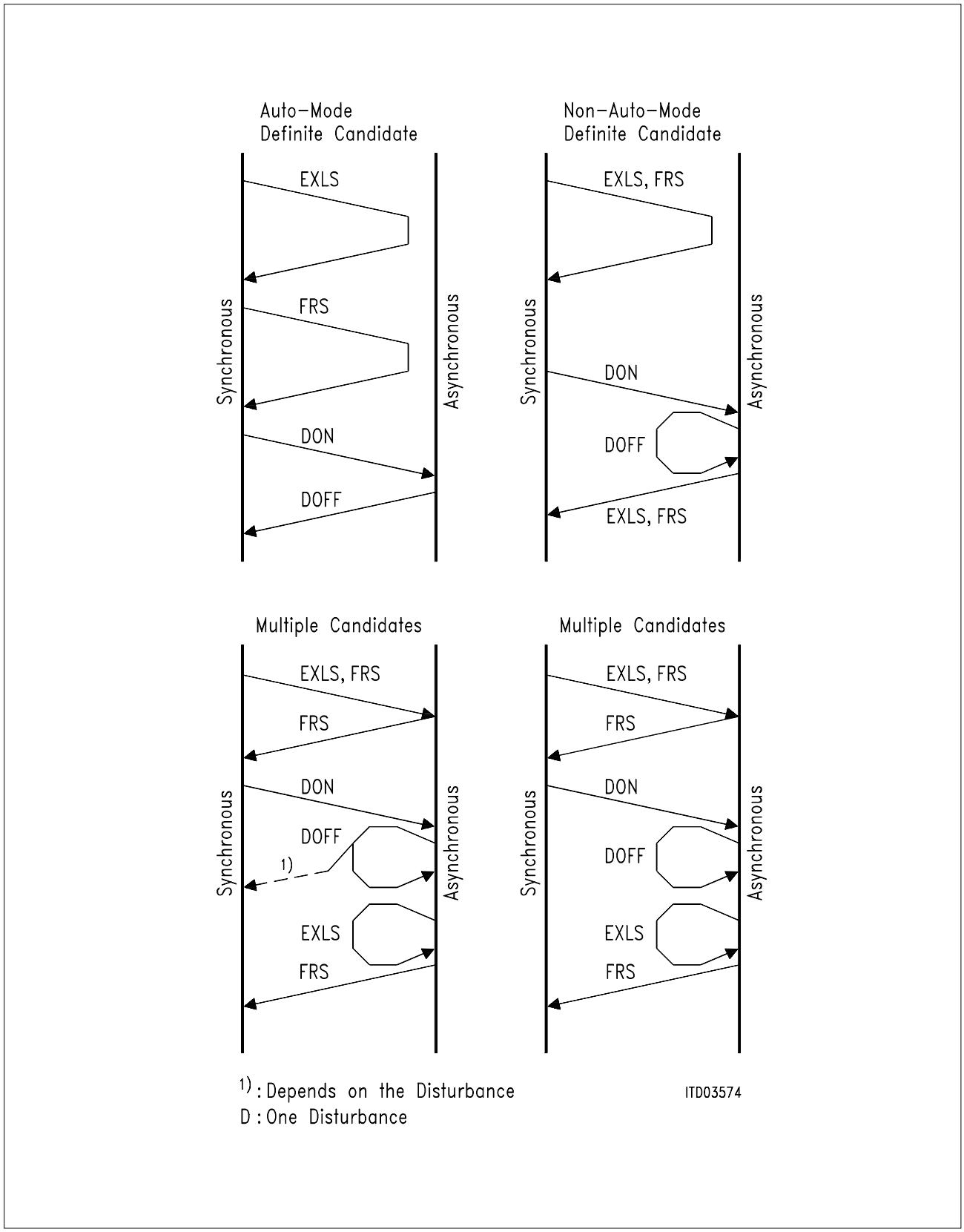


Figure 49
Influences on Synchronization Status

Figure 49 gives an overview of influences on synchronization status for the case of different external actions. Activation of auto-mode and non-auto mode is performed via bit FMR4.AUTO. Generally, for initiating resynchronization it is recommended to use bit: FMR0.EXLS first. In case where the synchronizer remains in the asynchronous state, bit FMR0.FRS may be used to enforce it to lock onto the next framing candidate, although it might be a simulated one.

General Alarms

- AIS (Blue Alarm): Detection is flagged by bit FRS0.AIS. Transmission is enabled via bit FMR1.XAIS.
- LOS (Red Alarm): Detection is flagged at bit FRS0.LOS.
- RAI: Remote Alarm (Yellow Alarm) Indication is flagged at bit FRS0.RRA. Transmission is enabled via bit FMR4.XRA. The type of remote alarm indication depends on the selected multiframe format.

Channel Assignment

There is one possibility provided for converting the 24 channels to the 32 time-slots on the system internal highway (refer to section Interface to System Internal Highway).

Transparent mode setting bit FMR4.TM switches the FALC54 in transparent mode:

– In transmit direction bit 8 of the FS/DL time-slot from the system internal highway (XDI) is inserted
– In the F-bit position of the outgoing frame.
– In receive direction the framing bit is also forwarded to RDO and inserted in the FS/DL time-slot.

Bit RDCF (bit 1 of FS/DL time-slot) indicates a DL bit.

General Signaling

A 4 kHz DL clock which is output on port DLR and DLX marks the DL bit positions within the data stream at RDO and XDI.

Signaling

The selection of the signaling scheme is done via bit FMR1.SIGM.

- **CCS**
  FMR1.SIGM = 0
  For Common Channel Signaling, the use of time-slot 24 is recommended. The use of CCS is permitted for all multiframe formats.
- **CAS-CC**
  FMR1.SIGM = 0
  Instead of CCS the above channels may be used for carrying CAS information. For positioning of the CAS multiframe with respect to the selected multiframe structure, refer to DMI, part III, § 12.1.
  Note: Synchronization to and synthesis of the CAS multiframe is not performed by the FALC54. The use of CAS-CC is permitted for all multiframe formats.
- **CAS-BR**
  FMR1.SIGM = 1
  The use of CAS robbed bit signaling is applicable to F12, ESF, and F72 multiframe format.

Especially when using the CAS-BR signaling schemes it could be necessary to define "**clear channels**" for data transmission. By programming registers CCB1 … CCB3 they can be selected on a per channel basis.

5.1.4.1 4-Frame Multiframe

The allocation of the FT bits (bit 1 of frames 1 and 3) for frame alignment signal is shown in **table 18**.

The FS bit may be used for signaling.
Remote alarm (yellow alarm) is indicated by setting bit 2 to '0' in each channel.

Table 18
4-Frame Multiframe Structure

Frame Number	F_T	F_S
1	1	
2	–	Service bit
3	0	
4	–	Service bit

Synchronization Procedure

For multiframe synchronization, the terminal framing bits (FT bits) are observed. The synchronous state is reached if at least one terminal framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (FMR0.FRS).

5.1.4.2 12-Frame Multiframe

Normally, this kind of multiframe structure only makes sense when using the CAS Robbed Bit Signaling. In addition, CCS and CAS-CC are also allowed. The multiframe alignment signal is located at the FS-bit position of every other frame (refer to **table 19**).

There are two possibilities of remote alarm (yellow alarm) indication:

- Bit 2 = 0 in each channel of a frame, selected with bit FMR0.SRAF = 0
- The last bit of the multiframe alignment signal (bit 1 of frame 12) changes from ‘0’ to ‘1’, selected with bit FMR0.SRAF = 1.

Synchronization Procedure

In the synchronous state terminal framing (FT bits) and multiframing (FS bits) are observed, independently. Further reaction on framing errors depends on the selected sync/resync procedure (via bit FMR2.SSP):

- FMR2.SSP = ‘0’: terminal frame and multiframe synchronization are combined.
  Two errors within 4/5/6 framing bits (via bits FMR4.SSC1/0) of one of the above will lead to the asynchronous state for terminal framing **and** multiframing. Additionally to the bit FRS0.LFA, loss of multiframe alignment is reported via bit FRS0.LMFA.
  The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulseframing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.
- FMR2.SSP = ‘1’: terminal frame and multiframe synchronization are separated
  Two errors within 4/5/6 terminal framing bits will lead to the same reaction as described above for the “combined” mode.
  Two errors within 4/5/6 multiframing bits will lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported via bit FRS0.LMFA. The state of terminal framing is not influenced.
  Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

Table 19
12-Frame Multiframe Structure

Frame Number	F_T	F_S	Signaling Channel Designation
1	1	–	
2	–	0	
3	0	–	
4	–	0	
5	1	–	
6	–	1	A
7	0	–	
8	–	1	
9	1	–	
10	–	1	
11	0	–	
12	–	0	B

5.1.4.3 Extended Superframe

The use of the first bit of each frame for the multiframe alignment word, the data link bits, and the CRC bits is shown in **table 20**.

Table 20
Extended Superframe Structure

Multiframe Frame Number	F Bits				Signaling Channel Designation
	Multiframe Bit Number	Assignments			
		FAS	DL	CRC	
1	0	–	m	–	
2	193	–	–	e_1	
3	386	–	m	–	
4	579	0	–	–	
5	772	–	m	–	
6	965	–	–	e_2	A
7	1158	–	m	–	
8	1351	0	–	–	
9	1544	–	m	–	
10	1737	–	–	e_3	
11	1930	–	m	–	
12	2123	1	–	–	B
13	2316	–	m	–	
14	2509	–	–	e_4	
15	2702	–	m	–	
16	2895	0	–	–	
17	3088	–	m	–	
18	3231	–	–	e_5	C
19	3474	–	m	–	
20	3667	1	–	–	
21	3860	–	m	–	
22	4053	–	–	e_6	
23	4246	–	m	–	
24	4439	1	–	–	D

Additions

CRC6 Inversion

If enabled via bit RC0.CRCI, all CRC bits of one outgoing extended multiframe are automatically inverted in case a CRC error is flagged for the previous received multiframe. Setting the bit RC0.XCRCI will invert the CRC bits before transmitted to the distant end. This function is logically ored with RC0.CRCI.

CRC6 Alarm Interrupt

As an extension of the CRC6 checking algorithm the occurrence of a received CRC6 error may set an interrupt status.

The CRC6 checking algorithm is enabled via bit FMR1.CRC. If not enabled, all check bits in the transmit direction are set to '1'.

Remote alarm (yellow alarm) is indicated by the periodical pattern '1111 1111 0000 0000 …' in the DL bits.

All signaling schemes are applicable for this multiframing structure. For external access to the DL bits, refer to section General.

Synchronization Procedure

For multiframe synchronization the FAS bits are observed. Synchronous state is reached if at least one framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (FMR0.FRS).

In the synchronous state the framing bits (FAS bits) are observed. Two errors within 4/5/6 framing bits or two or more erroneous framing bits within one ESF multiframe will lead to the asynchronous state.

There are two multiframe synchronization modes selectable via FMR2.MCSP

- FMR2.MCSP = 0 : In the synchronous state, the setting of FMR0.FRS or FMR0.EXLS resets the synchronizer and initiates a new frame search. The synchronous state will be reached again, if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state.
  In asynchronous state, setting bit FMR0.FRS induces the synchronizer to lock onto the next available framing candidate if there is one. At the same time the internal framing pattern memory will be cleared and other possible framing candidates are lost. (identical to the synchronization procedure implemented in FALC54 V1.1)

- FMR2.MCSP = 1 : This mode has been added in order to be able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the synchronization might have been based on an alias framing pattern, setting of FMR0.FRS will lead to synchronization on the next candidate available. However, only the previously assumed candidate will discarded in the internal framing pattern memory. The latter procedure can be repeated until the framer has locked on the right pattern (no extensive CRC errors).
  The synchronizer will be completely reset and initiates a new frame search, if there is no multiframing found. In this case bit FSR0.FSRF toggles.

- 72-Frame Multiframe

The 72-multiframe is an alternate use of the FS-bit pattern and is used for carrying data link information. This is done by stealing some of redundant multiframing bits after the transmission of the 12-bit framing header (refer to **table 21**). The position of A and B signaling channels (robbed bit signaling) is defined by zero-to-one and one-to-zero transitions of the FS bits and is continued when the FS bits are replaced by the data link bits. The use of this 24-bit data link channel, however, is not specified by the FALC54. For access to these bits refer to section General.

Remote Alarm (Yellow Alarm) is indicated by setting bit 2 to zero in each channel. An additional use of the D bits for alarm indication is user defined and must be done externally.

In addition to CAS-BR, CCS and CAS-CC are also applicable to this multiframe structure.

Synchronization Procedure

In the synchronous state terminal framing (FT bits) and multiframing (FS bits of the framing header) are observed independently. Further reaction on framing errors depends on the selected sync/resync procedure (via bit FMR2.SSP):

- FMR2.SSP = ‘0’: terminal frame and multiframe synchronization are combined
  Two errors within 4/5/6 framing bits (via bits FMR4.SSC1/0) of one of the above will lead to the asynchronous state for terminal framing **and** multiframing. Additionally to the bit FRS0.LFA, loss of multiframe alignment is reported via bit FRS0.LMFA.
  The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulseframing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.
- FMR2.SSP = ‘1’: terminal frame and multiframe synchronization are separated
  Two errors within 4/5/6 terminal framing bits will lead to the same reaction as described above for the “combined” mode.
  Two errors within 4/5/6 multiframing bits will lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported via bit FRS0.LMFA. The state of terminal framing is not influenced.
  Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

Table 21
72-Frame Multiframe Structure

Frame Number	F_T	F_{feS}	Signaling Channel Designation
1	0	–	
2	–	0	B
3	1	–	
4	–	0	
5	0	–	
6	–	0	
7	1	–	
8	–	1	A
9	0	–	
10	–	1	
11	1	–	
12	–	1	
13	0	–	
14	–	0	B
15	1	–	
16	–	0	
17	0	–	
18	–	0	
19	1	–	
20	–	1	A
21	0	–	
22	–	1	
23	1	–	
24	–	1	
25	0	–	
26	–	D	B
27	1	–	
28	–	D	
.	.	.	
.	.	.	
67	1	–	
68	–	D	A
69	0	–	
70	–	D	
71	1	–	
72	–	D	

5.1.4.4 Test Functions

There are two types of monitoring/testing functions:

- Active tests which partly degrade the functionality (e.g. Payload Loop, Remote Loop, Local Loop, test loop for a single channel).
- Diagnostics, during which the device is not operational (e.g. diagnostic loop of an entire trunk).

Payload Loopback

To perform an effective circuit test a line loop is implemented.

When the payload loopback (FMR2.PLB) is activated the received 192 bits of payload data will be looped back to the transmit direction. The framing bits, CRC6 and DL bits are not looped. They are originated by the FALC54 transmitter. When the PLB is enabled the transmitter and the data on pins XL1/XDOP and XL2/XDON are clocked with SCLKR instead of SCLKX. Data on pin XDI are ignored. All the received data are processed normally. With bit FMR2.SAIS an AIS could be sent to the system interface via pin RDO.

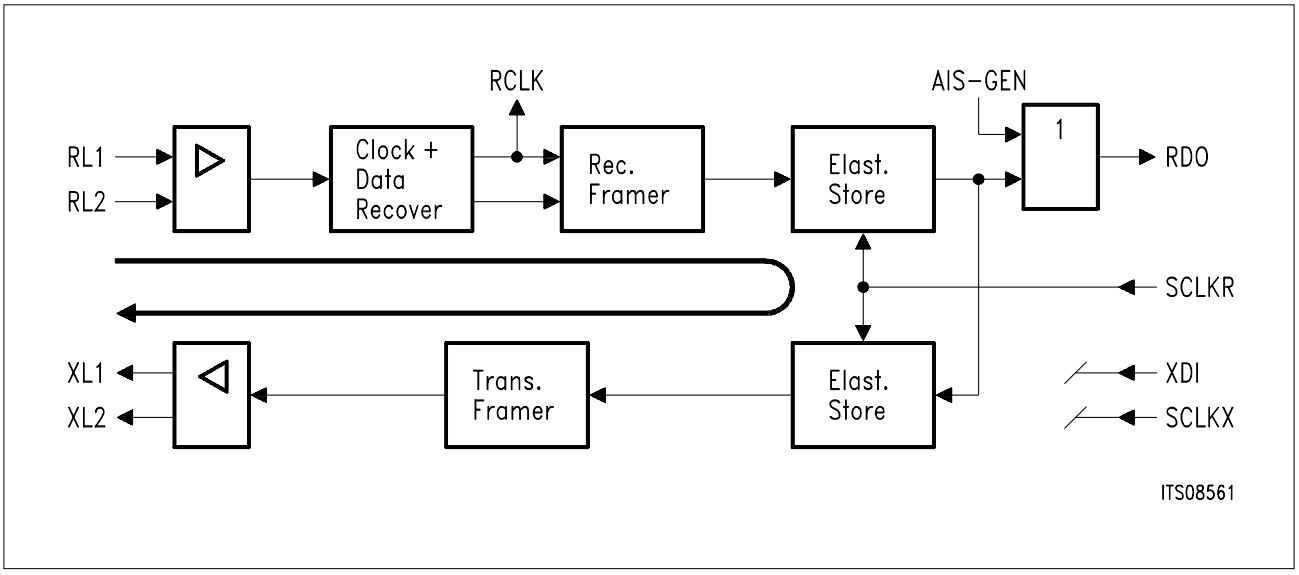


Figure 50
Payload Loop

Remote Loop

In the remote loopback mode the clock and data recovered from the line inputs RL1/2 or RDIP/RDIN are routed back to the line outputs XL1/2 or XDOP/XDON via the analog or digital transmitter. As in normal mode they are also processed by the synchronizer and then sent to the system interface.The remote loopback mode is selected by setting the respective control bits LIM1.RL+JATT. Received data may be looped with or without the transmit jitter attenuator (FIFO).

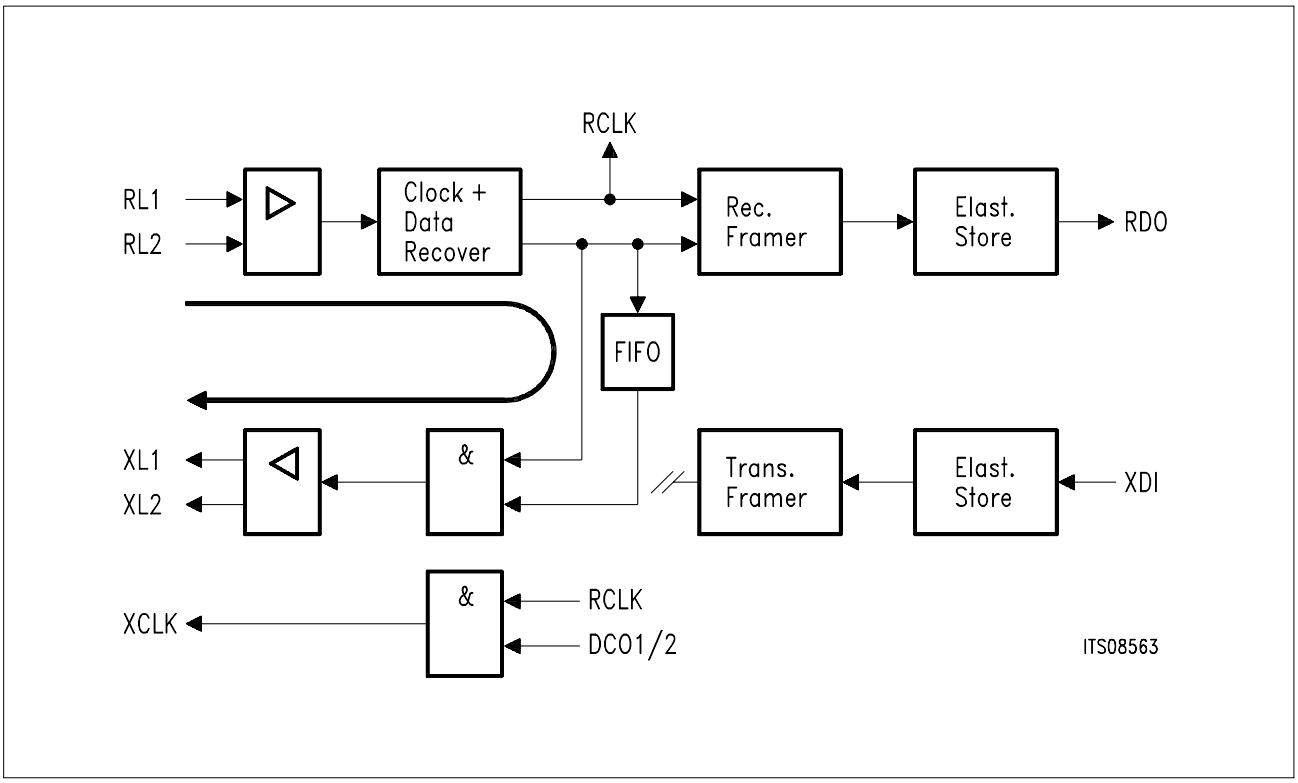


Figure 51
Remote Loop

Local Loop

The local loopback mode, selected by LIM0.LL = 1, disconnects the receive lines RL1/2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. However, the bit stream will be undisturbed transmitted on the line. However an AIS to the distant end could be enabled by setting FMR1.XAIS without influencing the data looped back to the system interface.

Note that enabling the local loop will usually invoke an out of frame error until the receiver can resync to the new framing. The serial code from the transmitter and receiver has to be programmed identically.

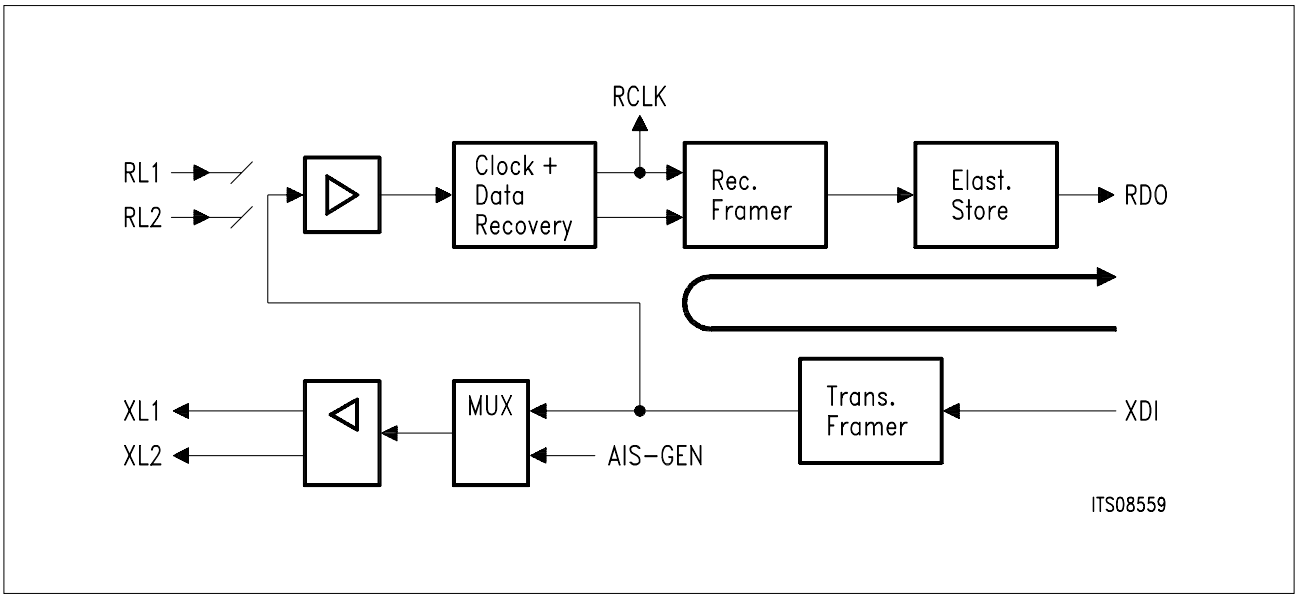


Figure 52
Local Loop

Channel Loop (loopback of time-slots)

The channel loopback is selected via LOOP.ECBL= 1.

Each of the 24 channels may be selected for loopback from the system PCM input (XDI) to the system PCM output (RDO). This loopback is programmed for one channel at a time selected by register LOOP. During loopback, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route channel.

For the channel test, sending sequences of test patterns like a 1 kHz check signal should be avoided. Otherwise, an increased occurrence of slips in the tested channel will disturb testing. These slips do not influence the other channels and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

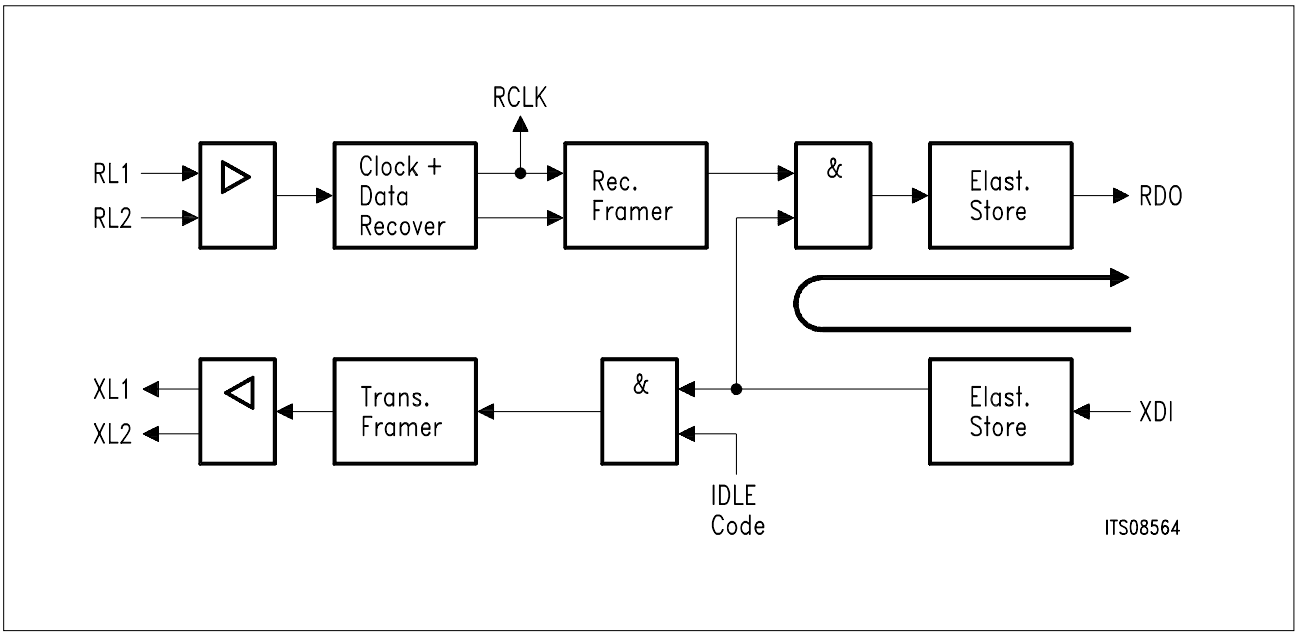


Figure 53
Channel Loopback

Alarm Simulation

Alarm simulation does not affect the normal operation of the device, i.e. all channels remain available for transmission. However, possible ‘real’ alarm conditions are not reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit FMR0.SIM. The following alarms are simulated:

- Loss of Signal (red alarm)
- Alarm Indication Signal AIS (blue alarm)
- Loss of pulse frame
- Remote alarm (yellow alarm) indication
- Receive slip indication
- Transmit slip indication
- Framing error counter
- Code violation counter (B8ZS Code)
- CRC6 error counter

Some of the above indications are only simulated if the FALC54 is configured in a mode where the alarm is applicable.

The alarm simulation is controlled by the value of the Alarm Simulation Counter: FRS2.ESC which is incremented by setting bit: FMR0.SIM.

Clearing of alarm indications:

– Automatically for LOS, remote (yellow) alarm, AIS, and loss of synchronization and

– User controlled for slips by reading the corresponding interrupt status register ISR3.

– Error counter have to be cleared by reading the corresponding counter registers.

is only possible at defined counter steps of FRS2.ESC. For complete simulation (FRS2.ESC = 0), eight simulation steps are necessary.

5.2 Signaling Controller

Operating Modes

The HDLC controller can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be performed in a very flexible way, to satisfy almost any practical requirements.

There are 4 different operating modes which can be set via the MODE register.

5.2.1 HDLC Mode

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Depending on the selected address mode, the FALC54 can perform a 1 or 2 byte address recognition (MODE.MDS0).

If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R) and will be excluded from the address comparison.

Similarly, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the FALC54 can be called (addressed) with 6 different address combinations. HDLC frames with address fields that do not match any of the address combinations, are ignored by the FALC.

In case of a 1-byte address, RAL1 and RAL2 will be used as compare registers. The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. Additional information can also be read from a special register (RSIS).

As defined by the HDLC protocol, the FALC54 perform the zero bit insertion/deletion (bit-stuffing) in the transmit/receive data stream automatically. That means, it is guaranteed that at least after 5 consecutive “1”-s a “0” will appear.

Non-Auto-Mode (MODE.MDS2-1=01)

Characteristics: address recognition, FLAG - and CRC generation/check, bit-stuffing

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Transparent Mode 1 (MODE.MDS2-0=101)

Characteristics: address recognition, FLAG - and CRC generation/check, bit-stuffing

Only the high byte of a 2-byte address field will be compared with registers RAH1/2. The whole frame excluding the first address byte will be stored in RFIFO.

Transparent Mode 0 (MODE.MDS2-0=100)

Characteristics: FLAG - and CRC generation/check, bit-stuffing

No address recognition is performed and each frame will be stored in the RFIFO.

5.2.2 Extended Transparent Mode

Characteristics: fully transparent

In no HDLC mode, fully transparent data transmission/reception without HDLC framing is performed, i.e. without FLAG generation/recognition, CRC generation/check, or bit-stuffing. This feature can be profitably used e.g for:

- Specific protocol variations
- Transmission of a BOM frame
- Test purposes

Data transmission is always performed out of the XFIFO. In transparent mode, the receive data are shifted into the RFIFO.

Receive Data Flow

The following figure gives an overview of the management of the received HDLC frames in the different operating modes.

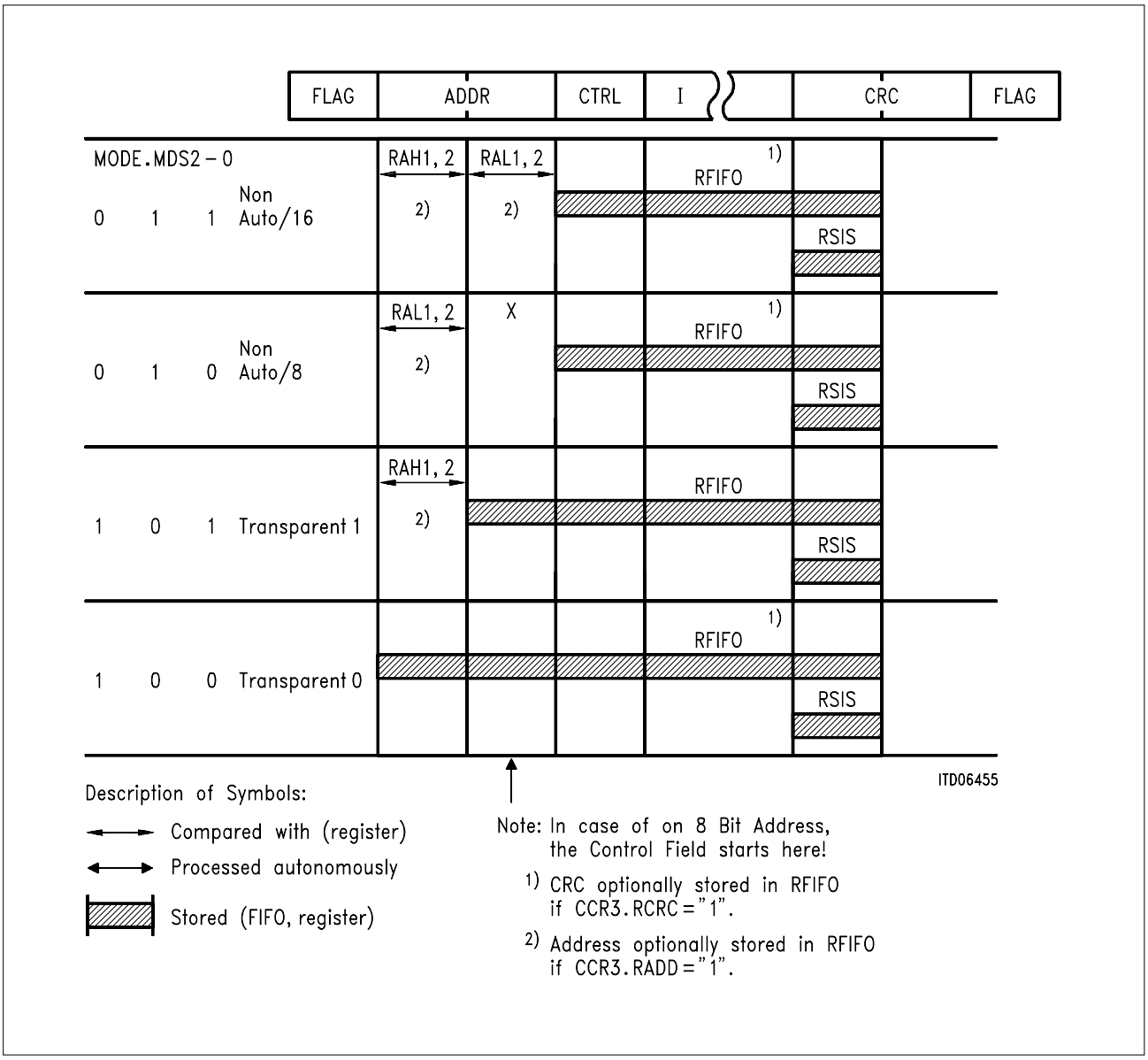


Figure 54
Receive Data Flow of FALC

Transmit Data Flow

The frames can be transmitted as shown below.

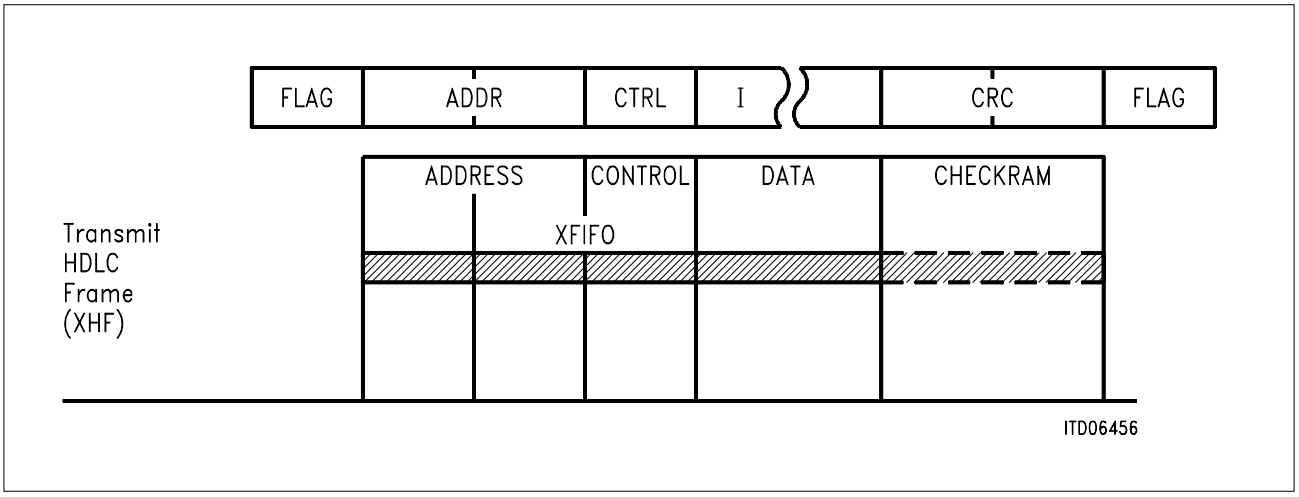


Figure 55
Transmit Data Flow of FALC54

Transmitting a HDLC frame via register CMDR.XTF, the address, the control fields and the data field have to be entered in the XFIFO.

If CCR3.XCRC is set, the CRC checksum will not be generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame will be closed automatically only with a (closing) flag.

The FALC54 does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

5.2.3 Special Functions

Shared Flags

The closing Flag of a previously transmitted frame simultaneously becomes the opening Flag of the following frame if there is one to be transmitted. The Shared Flag feature is enabled by setting bit SFLG in control register CCR1.

Preamble Transmission

If enabled via register CCR3, a programmable 8-bit pattern (register PRE) is transmitted with a selectable number of repetitions after Interframe Timefill transmission is stopped and a new frame is ready to be sent out.

Zero Bit Insertion is disabled during preamble transmission. To guarantee correct function the programmed preamble value should be different from Receive Address Byte values.

In BOM-mode the MSB of the preamble should be reset in order to achieve a quicker synchronization at the BOM-receiver. After the preamble has been sent out the transmitter automatically inserts one synch-byte FF_H before sending the contents of the transmit FIFO.

Transparent Transmission and Reception

When programmed in the extended transparent mode via the MODE register (MDS2-0 = 111), the FALC54 performs fully transparent data transmission and reception without HDLC framing, i.e. without

- FLAG insertion and deletion
- CRC generation and checking
- Bit-stuffing

In order to enable fully transparent data transfer, bit MODE.HRAC has to be set and FF_H has to be written to RAH2.

Data transmission is always performed out of XFIFO by directly shifting the contents of XFIFO in the outgoing datastream. Transmission is initiated by setting CMDR.XTF (04_H). A synch-byte FF_H is automatically sent before the first byte of the XFIFO will be transmitted.

Received data is always shifted into RFIFO.

Cyclic Transmission (fully transparent)

If the extended transparent mode is selected, the FALC54 supports the continuous transmission of the contents of the transmit FIFO.

After having written 1 to 32 bytes to XFIFO, the command XREP.XTF via the CMDR register (bit 7 … 0 = '00100100' = 24_H) forces the FALC54 to repeatedly transmit the data stored in XFIFO to the remote end.

Note: The cyclic transmission continues until a reset command (CMDR: SRES) is issued or with resetting CMDR.XREP, after which continuous '1'-s are transmitted.

Note: During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

CRC ON/OFF Features

As an option in HDLC mode the internal handling of received and transmitted CRC checksum can be influenced via control bits CCR3.RCRC and CCR3.XCRC.

Receive Direction

The received CRC checksum is always assumed to be in the 2 (CRC-ITU) last bytes of a frame, immediately preceding a closing flag. If CCR3.RCRC is set, the received CRC checksum will be written to RFIFO where it precedes the frame status byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If HDLC mode is selected, the limits for 'Valid Frame' check are modified (refer to description of bit RSIS.VFR).

Transmit Direction

If CCR3.XCRC is set, the CRC checksum is not generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame will only be closed automatically with a (closing) flag.

The FALC54 does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

Receive Address Pushed to RFIFO

The address field of received frames can be pushed to RFIFO (first one/two bytes of the frame). This function is especially useful in conjunction with the extended address recognition. It is enabled by setting control bit CCR3.RADD.

5.2.4 Time-Slot Assigner

The FALC54 offers the flexibility to extract or insert data during certain time-slots which are defined via registers RTR1-4 and TTR1-4. Any combination of time-slots can be programmed independent for the receive and transmit direction.

Table 22
Time-Slot Assigner

		Time-Slots
Receive Time-Slot Register	**Transmit Time-Slot Register**	
RTR1.7	TTR1.7	0
RTR1.6	TTR1.6	1
RTR1.5	TTR1.5	2
RTR1.4	TTR1.4	3
RTR1.3	TTR1.3	4
RTR1.2	TTR1.2	5
RTR1.1	TTR1.1	6
RTR1.0	TTR1.0	7
RTR2.7	TTR2.7	8
RTR2.6	TTR2.6	9
RTR2.5	TTR2.5	10
RTR2.4	TTR2.4	11
RTR2.3	TTR2.3	12
RTR2.2	TTR2.2	13
RTR2.1	TTR2.1	14
RTR2.0	TTR2.0	15
RTR3.7	TTR3.7	16
RTR3.6	TTR3.6	17
RTR3.5	TTR3.5	18
RTR3.4	TTR3.4	19
RTR3.3	TTR3.3	20
RTR3.2	TTR3.2	21
RTR3.1	TTR3.1	22
RTR3.0	TTR3.0	23

Table 22
Time-Slot Assigner (cont'd)

		Time-Slots
Receive Time-Slot Register	**Transmit Time-Slot Register**	
RTR4.7	TTR4.7	24
RTR4.6	TTR4.6	25
RTR4.5	TTR4.5	26
RTR4.4	TTR4.4	27
RTR4.3	TTR4.3	28
RTR4.2	TTR4.2	29
RTR4.1	TTR4.1	30
RTR4.0	TTR4.0	31

5.2.5 Bit Oriented Message Mode

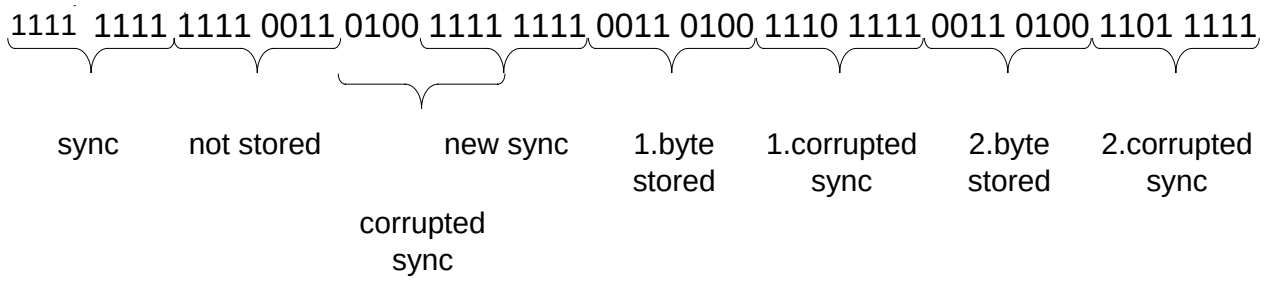
The FALC54 supports signaling and maintenance functions for T1 - Primary Rate Interfaces using the Extended Super Frame format. The device supports the DL-channel protocol for ESF format according to T1.403-1989 ANSI specification or according to AT&T TR54016, 1989. The HDLC- and Bit Oriented Message (BOM) -Receiver can be switched ON/OFF independently. To support the ESF-DL protocol according AT&T TR54016 or if the FALC54 is used for HDLC formats only, the BOM receiver has to be switched off. If HDLC- and BOM-receiver has been switched on (MODE.HRAC/BRAC), an automatic switching between HDLC and BOM mode is enabled. After Reset or software-reset (CMDR.RRES) the FALC54 operates in HDLC mode. If eight or more consecutive ones are detected, the BOM mode is entered. Upon detection of a flag in the data stream, the FALC54 switches back to HDLC-mode. Operating in BOM-mode, the FALC54 may receive an HDLC frame immediately, i.e. without any preceding flags.

In BOM-mode, the following byte format is assumed (the left most bit is received first).
111111110xxxxxx0

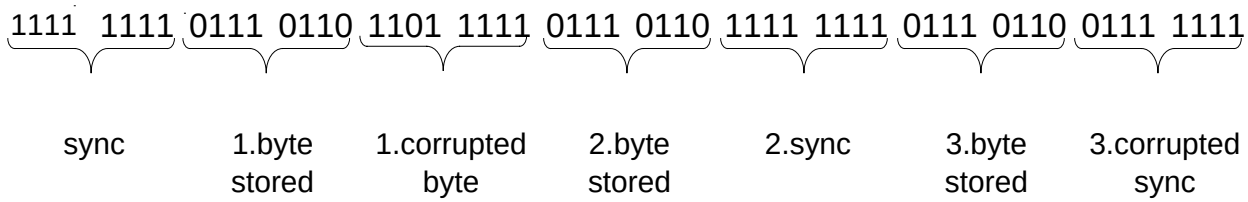
The FALC54 uses the FF_H byte for synchronization, the next byte is stored in RFIFO (first bit received: LSB) if it starts and ends with a '0'. Bytes starting and ending with a '1' are not stored. If there are no 8 consecutive one's detected within 32 bits, an interrupt is generated. However, byte sampling is not stopped.

Byte sampling in BOM Mode

a)



b)



Two different BOM reception modes may be programmed (CCR1.BRM).

10 byte packets: After storing 10 bytes in RFIFO the receive status byte marking a BOM frame (RSIS.HFR) is added as the eleventh byte and an interrupt (ISR0.RME) is generated. The sampling of data bytes continues and interrupts are generated every 10 bytes until an HDLC flag is detected.

Continuous reception: Interrupts are generated every 32 (16, 4, 2) bytes. After detecting an HDLC flag, byte sampling is stopped, the receive status byte is stored in RFIFO and an RME interrupt is generated.

The user may switch between these modes at any time. Byte sampling may be stopped by deactivating the BOM receiver (MODE.BRAC). In this case the receive status byte is added, an interrupt is generated and HDLC-mode is entered. Whether the FALC54 operates in HDLC or BOM mode may be checked by reading the Signaling Status Register (SIS.BOM).

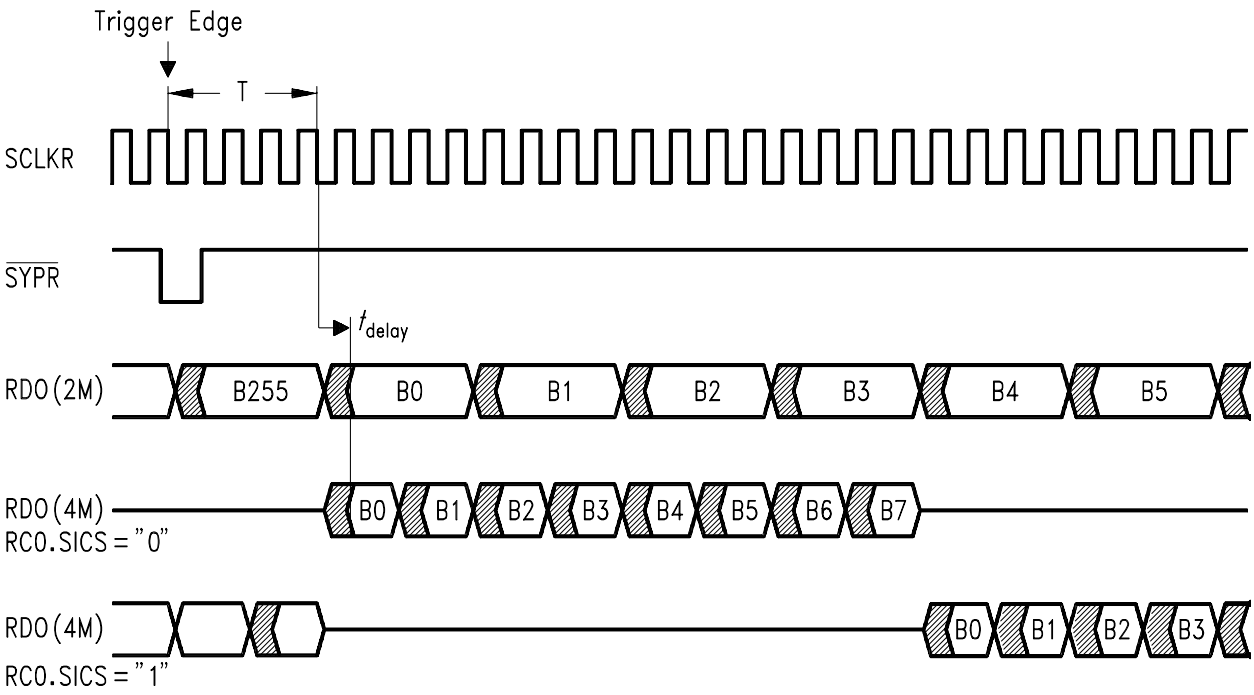
5.2.6 4 Kbit/s Data Link Access in F72 Format

The FALC54 supports the DL-channel protocol using the F72 (SLC96) format in two ways.

First: Sampling of DL bits is done on a multiframe basis and stored in the registers RDL1-3. A receive multiframe begin interrupt is provided to read the received data DL bits. The contents of registers XDL1-3 is subsequently sent out on the transmit multiframe basis if it is enabled via FMR1.EDL. A transmit multiframe begin interrupt requests for writing new information to the DL-bit registers.

Second: The DL bit information from frame 26 to 72 is stored in the Receive FIFO of the signaling controller.The DL bits stored in the XFIFO are inserted in the outgoing datastream, if it is enabled via CCR1.EDLX. If CCR1.EDLX is cleared a HDLC- or a transparent- frame could be sent or received via the RFIFO / XFIFO.

5.2.7 Interface to System Internal Highway



Calculation of value X for Receive Time-Slot Offset:

Delay time T [SCLKR cycles] depends on the value X of the "RECEIVE COUNTER OFFSET"-register.

Delay time T is an even number in the range from 0 to 1022:

RC0.RCOS = "0": $X = 5 - T/2$ if $0 \le T \le 10$

$X = 517 - T/2$ if $12 \le T \le 1022$

Delay time T is an odd number in the range from 1 to 1023:

RC0.RCOS = "1": $X = 5 - (T-1)/2$ if $1 \le T \le 11$

$X = 517 - (T-1)/2$ if $13 \le T \le 1023$

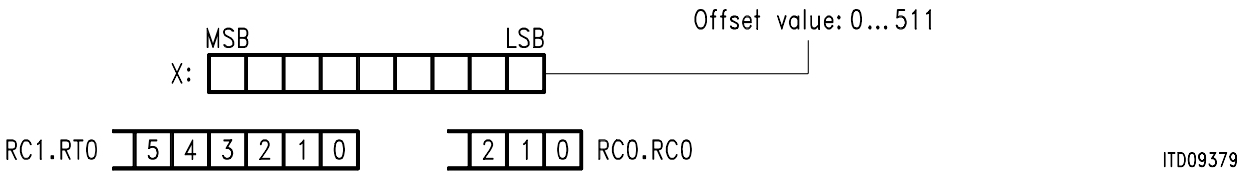
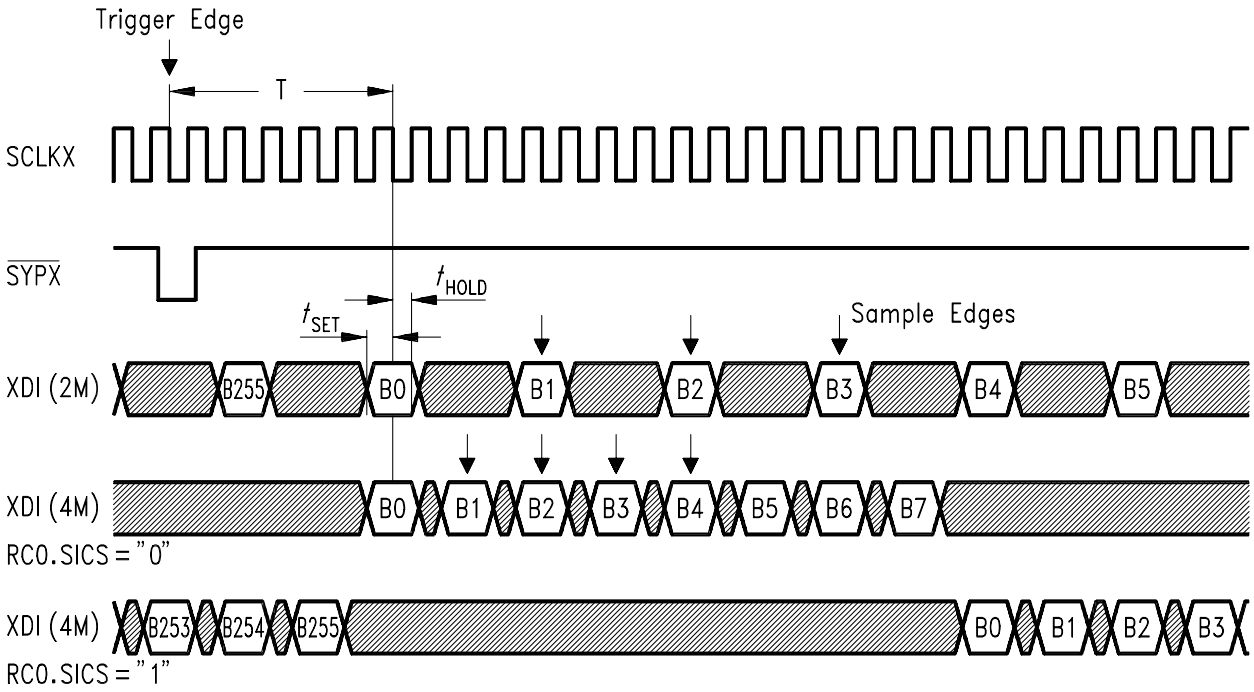


Figure 56
Data on RDO



Calculation of value X for Transmit Time-Slot Offset:

Delay time T [SCLKX cycles] depends on the value X of the "TRANSMIT COUNTER OFFSET"-register.

Delay time T is an even number in the range from 0 to 1022:

XC1.XCOS = "0": $X = 498 - T/2$ if $0 \le T \le 996$

$X = 1010 - T/2$ if $998 \le T \le 1022$

Delay time T is an odd number in the range from 1 to 1023:

XC1.XCOS = "1": $X = 498 - (T-1)/2$ if $1 \le T \le 997$

$X = 1010 - (T-1)/2$ if $999 \le T \le 1023$

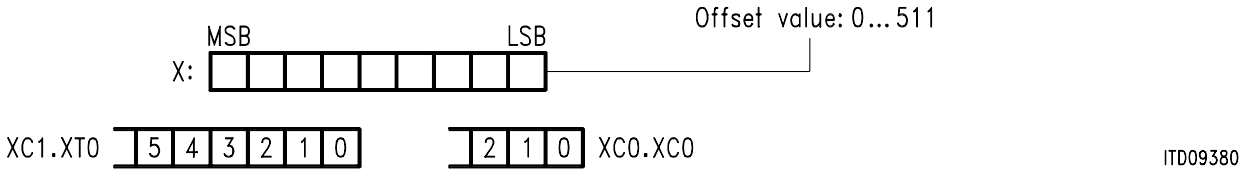


Figure 57
Data on XDI

Table 23
Channel Translation Modes for PCM 24

Speech Channels		Time-Slots
C. Translation Mode 0	C. Translation Mode 1	
FS/DL	FS/DL	0
1	1	1
2	2	2
3	3	3
–	4	4
4	5	5
5	6	6
6	7	7
–	8	8
7	9	9
8	10	10
9	11	11
–	12	12
10	13	13
11	14	14
12	15	15
–	16	16
13	17	17
14	18	18
15	19	19
–	20	20
16	21	21
17	22	22
18	23	23
–	24 --- S	24
19	–	25
20	–	26
21	–	27
–	–	28
22	–	29
23	–	30
S --- 24	–	31

S: CCS/CAS-CC signaling channel.

The formats for FS/DL data transmission via the system interface are as follows:

Receive Direction

FS/DL bits on system internal receive highway (RDO), time-slot 0.

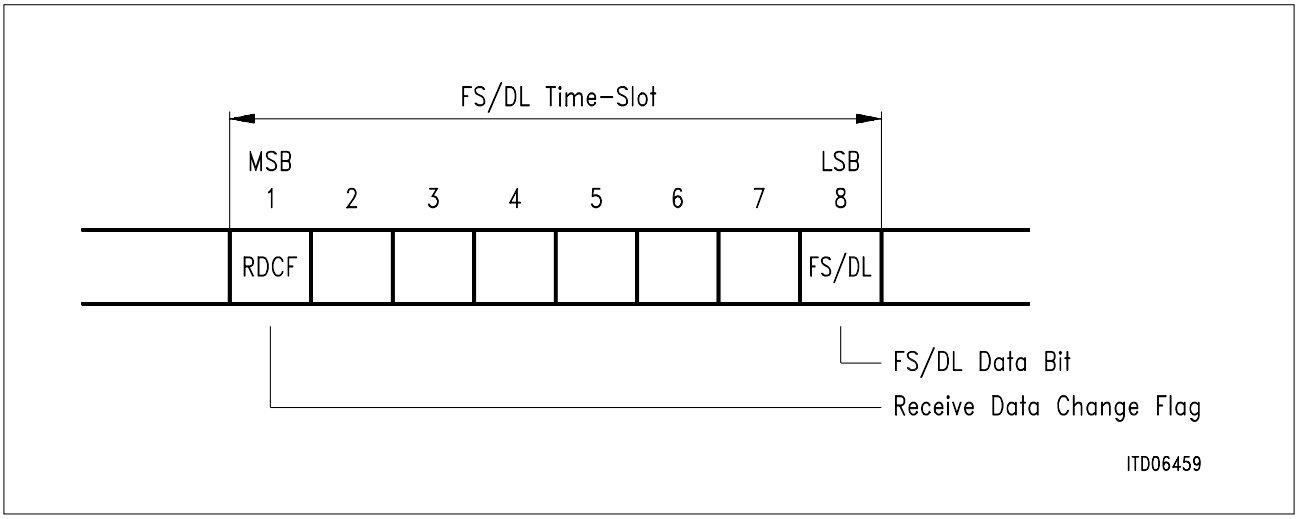


Figure 58
Receive FS/DL Bits on RDO

Each data bit is repeated for two frames. The reception of a new FS/DL bit is indicated by the **R**eceive **D**ata **C**hange **F**lag (normal operation: RDCF toggles; transparent mode enabled via bit FMR4.TM: RDCF is set, if the FS/DL bit-slot contains valid DL information). For further support in locating optionally defined subchannels the signals RMFB and XMFB may be used.
In transparent mode FMR4.TM=1 every received FS/DL bit is transferred unchanged to the system interface. In order to get an undisturbed receiption even in the asynchronous state bit FMR2.DAIS has to be set.

Transmit Direction

FS/DL data on system internal transmit highway (XDI), time-slot 0.

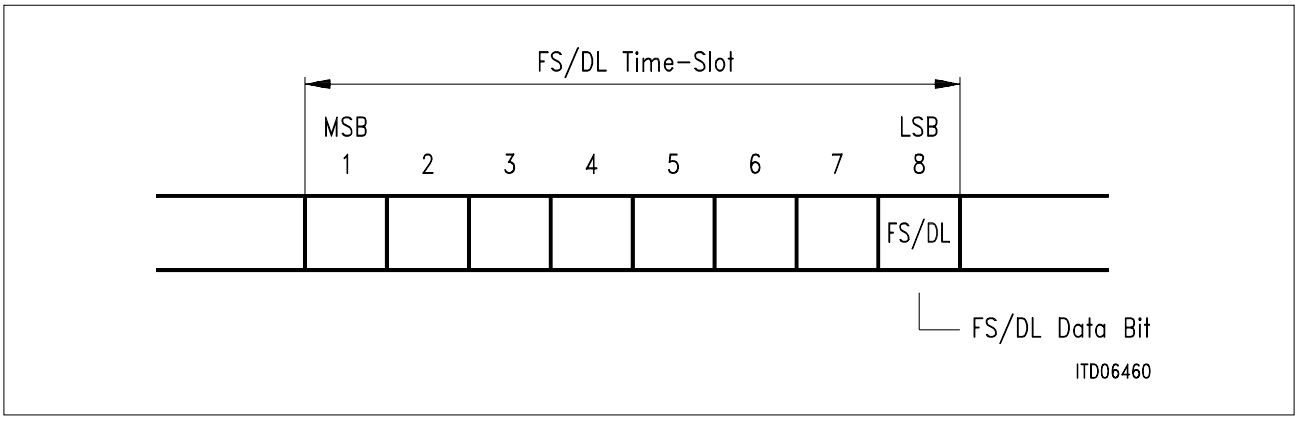


Figure 59
Transmit FS/DL Bits on XDI

The FS/DL bit of every second frame is inserted into the transmit FS/DL-bit location of the assigned outgoing 193-bit frame.

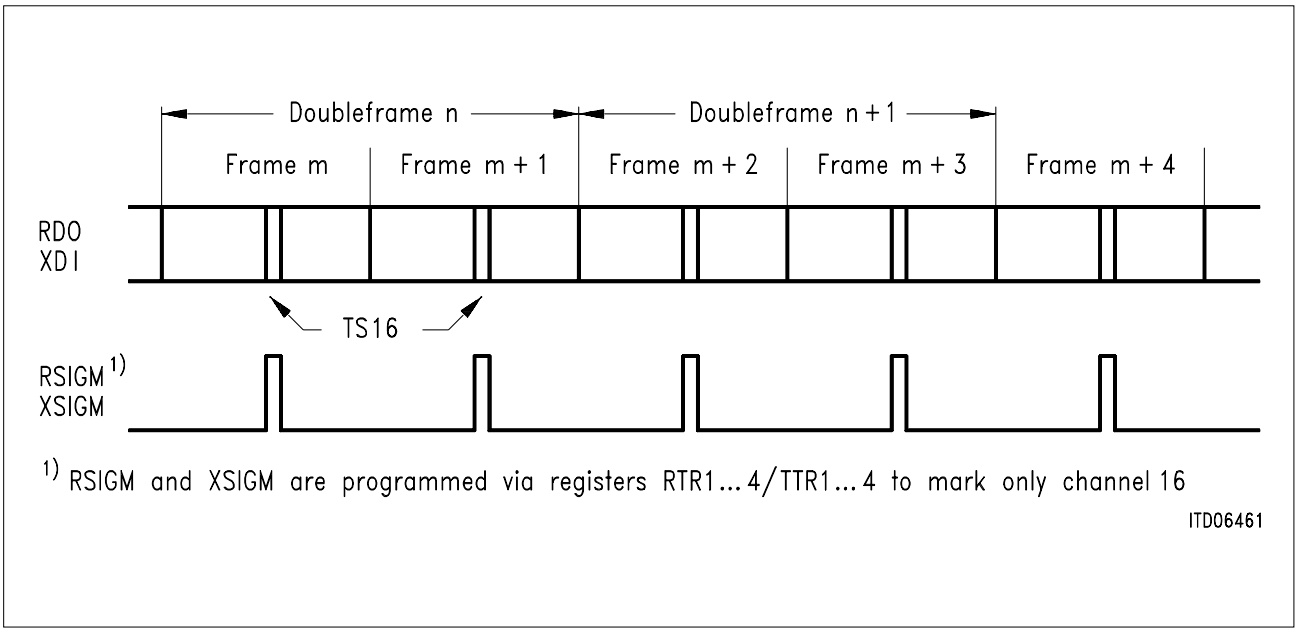


Figure 60
Supporting Signals for CCS/CAS-CC Applications

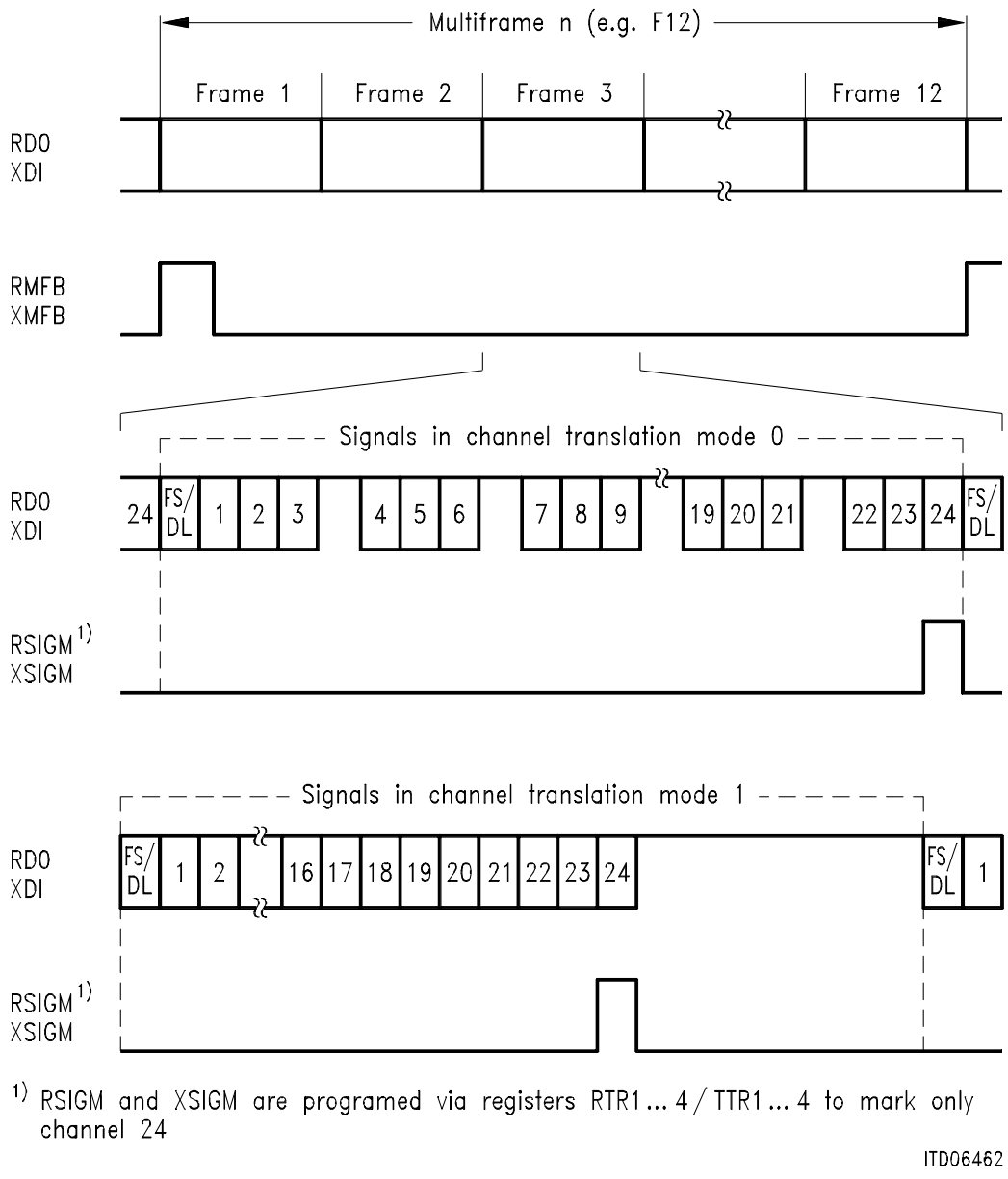
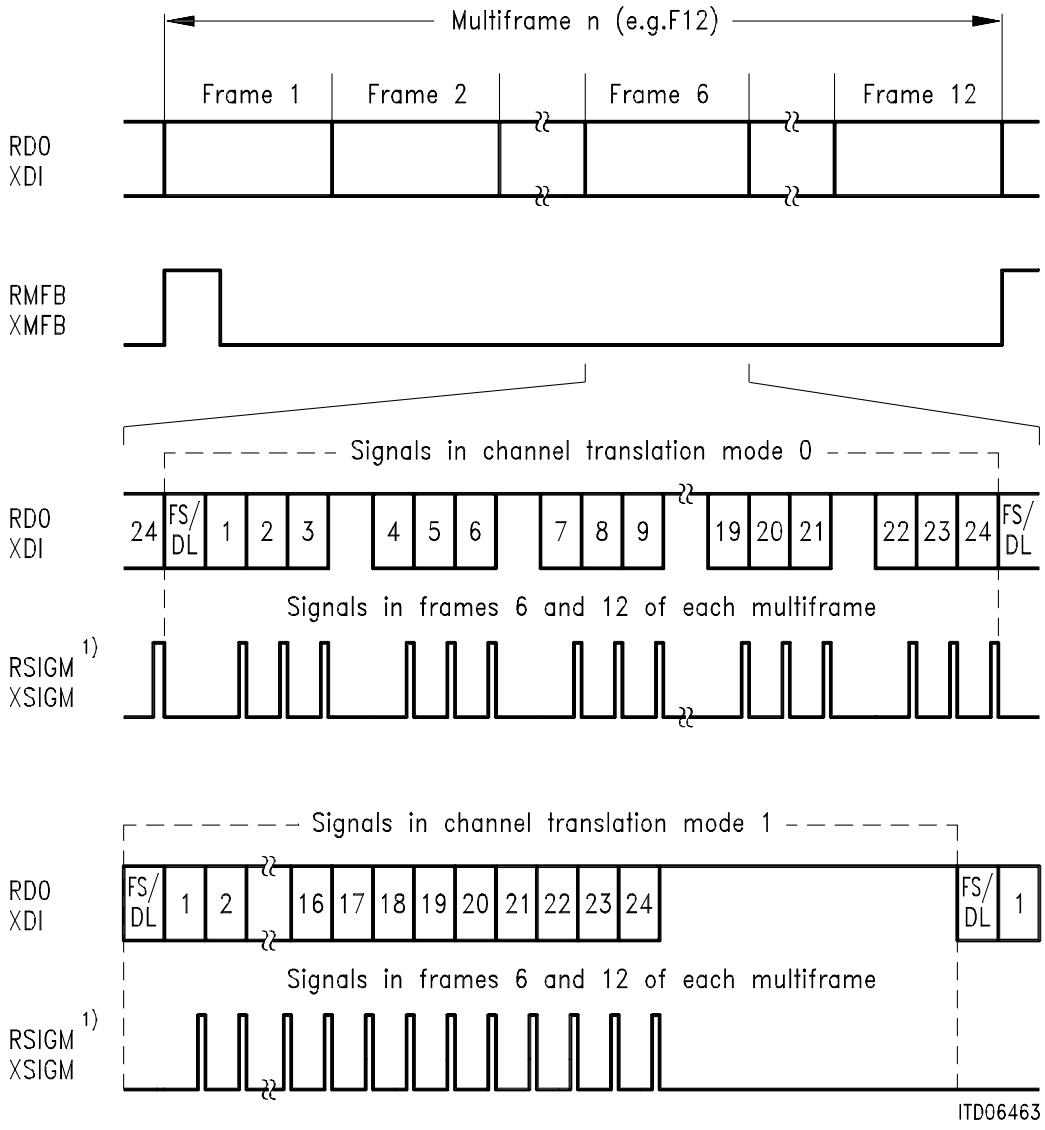


Figure 61
Supporting Signals for CCS/CAS-CC Applications



1) RSIGM and XSIGM will mark the robbed bit positions if XCO.BRM is set high

Figure 62
Supporting Signals for CAS-BR Applications

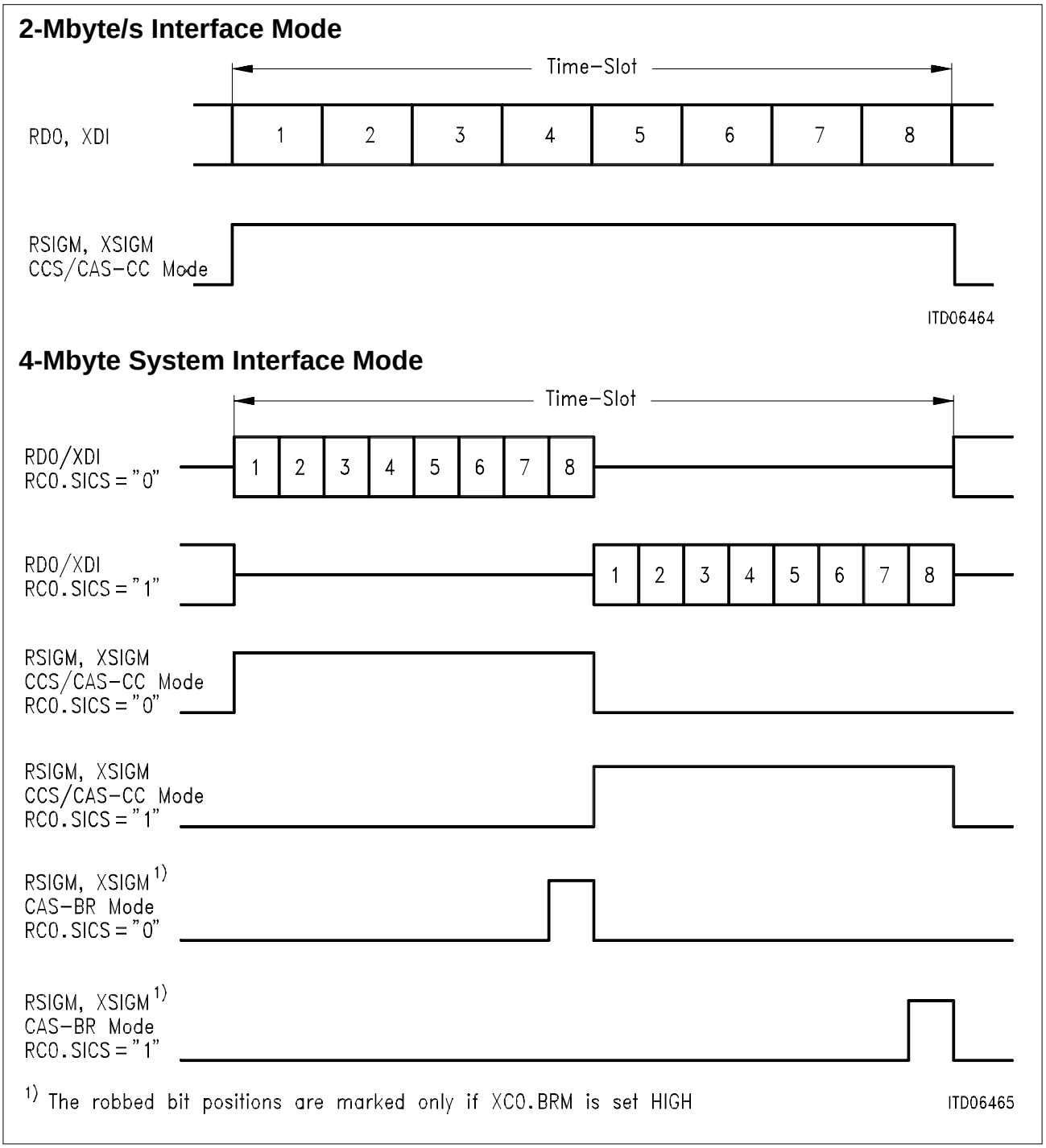


Figure 63
Signaling Markers in 2/4-Mbyte/s System Interface Mode

An additional possibility exists for using the FS/DL bits for signaling, e.g. for CCS (see **figure 63**). For synchronizing this controller to the multiframe structure

– the signals RMFB and XMFB, and
– the signals DLR and DLX (4 kHz DL clock)

may be used.

6 Operational Description T1

Reset

The FALC54 is forced to the reset state if a high signal is input at port RES for a minimum period of 20 µs. During RESET, all output stages except CLK16M, CLK12M, CLK8M, CLKX, $\overline{FSC}$, XCLK and RCLK are tri-stated, all internal flip-flops are reset and most of the control registers are initialized with default values.

After Reset bit FMR1.PMOD has to be set high and the device needs up to 20 µsec to settle up to the internal clocking. After FMR1.PMOD has been set the configuration shown in **table 24** is initialized.

Table 24
Configuration if Initialized after RESET

Register	Initiated Value	Meaning
FMR0	00_H	NRZ Coding, No alarm simulation.
FMR1 FMR2	00_H 00_H	PCM 24 mode, 4 Mbit/s system interface mode, no AIS transmission to remote end or system interface, Payload Loop off
LOOP	00_H	Channel loop back are disabled.
FMR4 FMR5	00_H 00_H	Remote alarm indication towards remote end disabled. LFA condition: 2 out of 4 framing bits, Non-auto-synchronization mode, F12 multiframing, internal Bit Robbing Access disabled
XC0 XC1	00_H 00_H	The transmit clock-slot offset is cleared. The transmit time-slot Offset is cleared.
RC0 RC1	00_H 00_H	The receive clock slot offset is cleared. The receive time-slot offset is cleared.
IDLE ICB 1 … 3	00_H 00_H	Idle channel code is cleared. Normal operation (no “Idle Channels” selected).
CCB 1 … 3	00_H	Normal operation (no clear channel operation).
LIM0 LIM1 PCD PCR	00_H 00_H 00_H 00_H	Slave Mode, Local Loop off, frequency on pin CLKX: 2.048 MHz, no LOS indication on pin RCLK Analog interface selected, Remote Loop off Pulse Count for LOS Detection cleared Pulse Count for LOS Recovery cleared
XPM2-0	$9c_H$,03_H,00_H	Transmit Pulse Mask
IMR1-4	FF_H	All interrupts are disabled

Table 24
Configuration if Initialized after RESET (cont'd)

Register	Initiated Value	Meaning
RTR1-4 TTR1-4	00_H	No time-slots selected
MODE	00_H	Signaling controller disabled
PRE	00_H	Preamble cleared
RAH1/2	FD_H,FF_H	Compare register for receive address cleared
RAL1/2	FF_H,FF_H	

Operational Phase

The FALC54 is programmable via a microprocessor interface which enables access to 61 control and 35 status registers.

After RESET the FALC54 has to be first initialized. General guidelines for initialization are described in section Initialization.

The status registers are read-only and are continuously updated. Normally, the processor periodically reads the status registers to analyze the alarm status and signaling data.

Initialization

For a correct start up of the Primary Access Interface a set of parameters specific to the system and hardware environment must be programmed after RESET goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T and DMI recommendations (e.g. Fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 25** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, may be programmed simultaneously. The bit FMR1.PMOD should always be kept high.

Table 25
Initialization Parameters

Basic Set Up	**PCM 24**
Mode Select	FMR1.PMOD = 1
Specification of Line interface and clock generation	LIM0, LIM1, XPM2-0
Line interface coding	FMR0.XC1/0, FMR0.RC1/0
Loss of Signal detection / recovery conditions	PCD, PCR,LIM1
System interface mode	FMR1.IMOD
channel translation mode	FMR1.CTM
Transmit offset counters	XC0.XCO, XC1.XTO
Receive offset counters	RC0.RCO, RC1.RTO
AIS to system interface	FMR2.DAIS/SAIS
Operational Set Up	**PCM 24**
Select framing	FMR4.FM1/0
Framing additions	FMR1.CRC, FMR0.SRAF
Synchronization mode	FMR4.AUTO, FMR4.SSC1/0, FMR2.MCSP,FMR2.SSP
Signaling mode	FMR1.SIGM, FMR5.EIBR, XC0.BRM, MODE, CCR1, CCR3, PRE, RAH1/2, RAL1/2

Features like channel loop back, idle channel activation, clear channel activation, extensions for signaling support, alarm simulation, … may be activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Note: Read access to unused register addresses: value should be ignored.
Write access to unused register addresses: should be avoided, or set to ‘00’hex.
All control registers (except XFIFO, XS1-12, CMDR, DEC) are of type: Read/Write

HDLC Data Transmission

In transmit direction 2x32 byte FIFO buffers are provided. After checking the XFIFO status by polling the bit SIS.XFW or after an interrupt ISR1.XPR (Transmit Pool Ready), up to 32 bytes may be entered by the CPU to the XFIFO.

The transmission of a frame can be started by issuing a XTF or XHF command via the command register. If enabled, a specified number of preambles (register PRE) are optionally sent out before transmission of the current frame starts. If the transmit command does not include an end of message indication (CMDR.XME), the FALC54 will repeatedly request for the next data block by means of a XPR interrupt as soon as no more than 32 bytes are stored in the XFIFO, i.e. a 32-byte pool is accessible to the CPU.

This process will be repeated until the CPU indicates the end of message per XME command, after which frame transmission is finished correctly by appending the CRC and closing flag sequence. Consecutive frames may be share a flag (enabled via CCR1.SFLG), or may be transmitted as back-to-back frames, if service of XFIFO is quick enough.

In case no more data is available in the XFIFO prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence and the CPU is notified per interrupt ISR1.XDU. The frame may be aborted per software CMDR.SRES.

The data transmission sequence, from the CPU’s point of view, is outlined in **figure 64**.

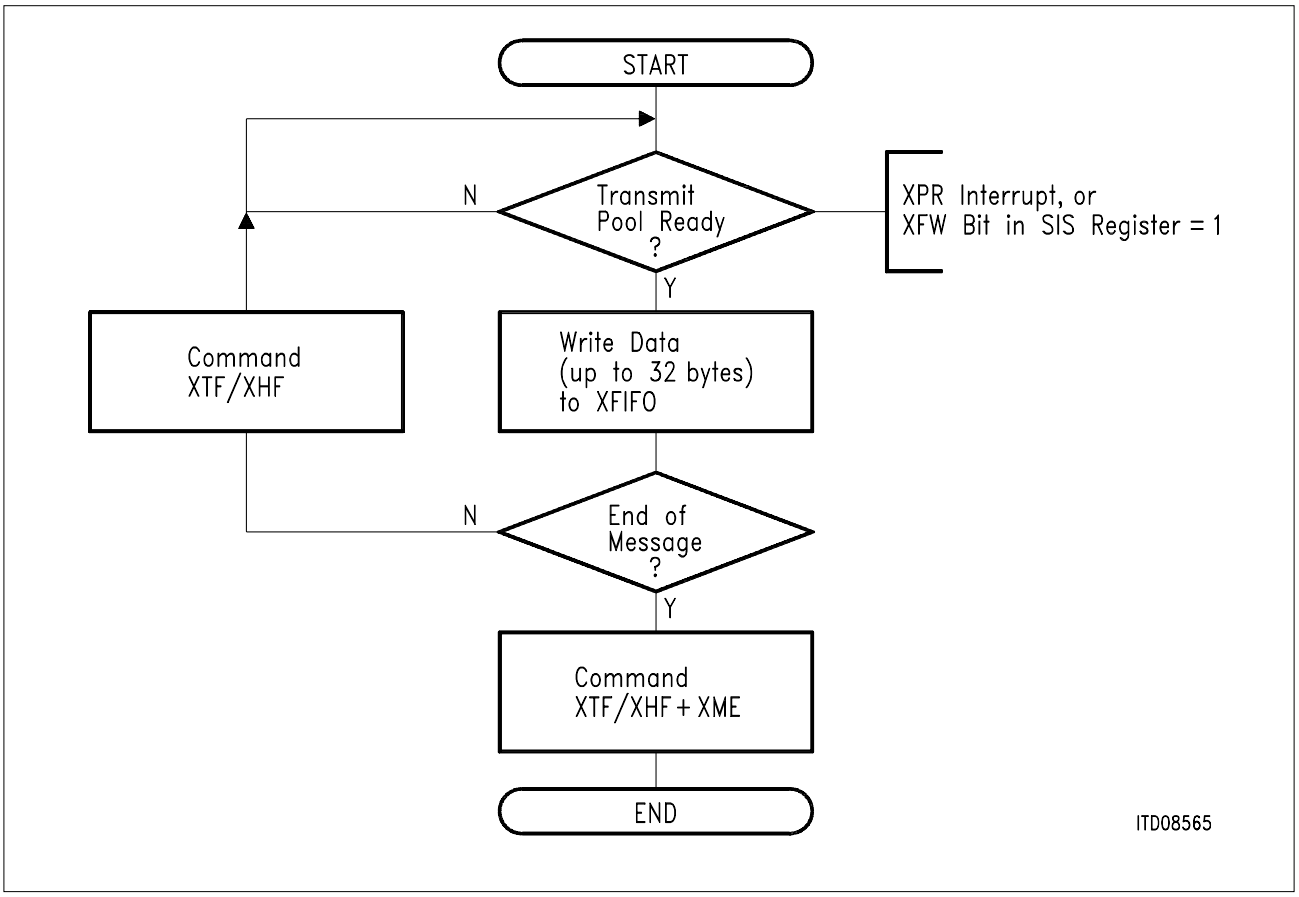


Figure 64
Interrupt Driven Data Transmission (flow diagram)

The activities at both serial and CPU interface during frame transmission (supposed frame length = 70 bytes) is shown in **figure 65**.

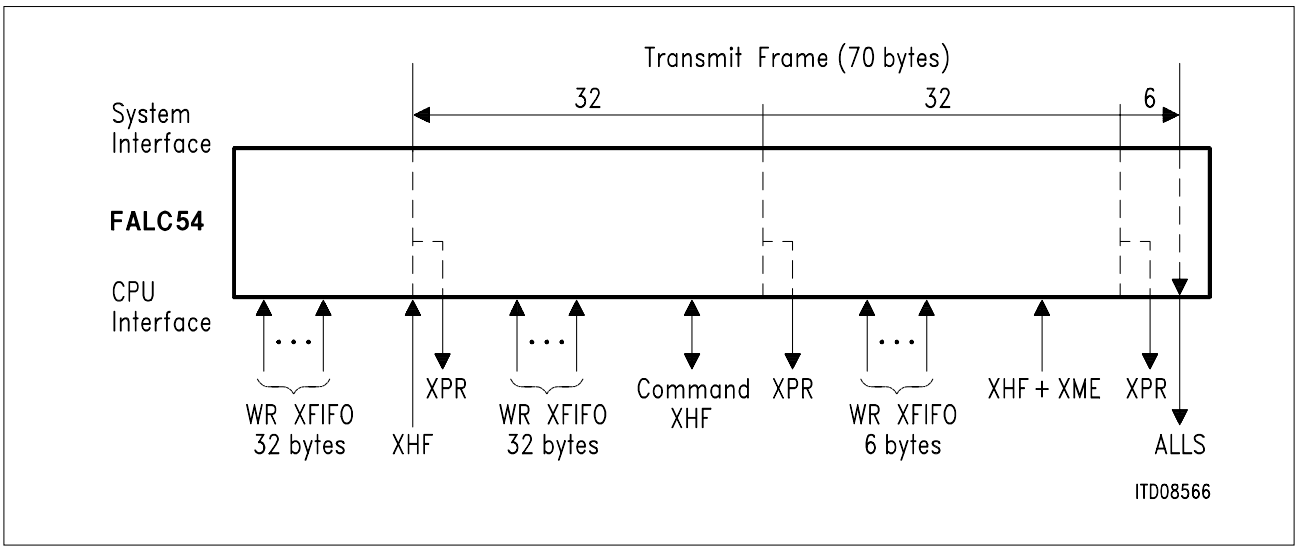


Figure 65
Interrupt Driven Transmission Example

Data Reception

Also 2×32 byte FIFO buffers are provided in receive direction. There are different interrupt indications concerned with the reception of data:

HDLC

RPF (Receive Pool Full) interrupt, indicating that a 32-byte-block of data can be read from RFIFO and the received message is not yet complete.

RME (Receive Message End) interrupt, indicating that the reception of one message is completed.

The following **figure 66** gives an example of a reception sequence, assuming that a “long” frame (66 bytes) followed by two short frames (6 bytes each) are received.

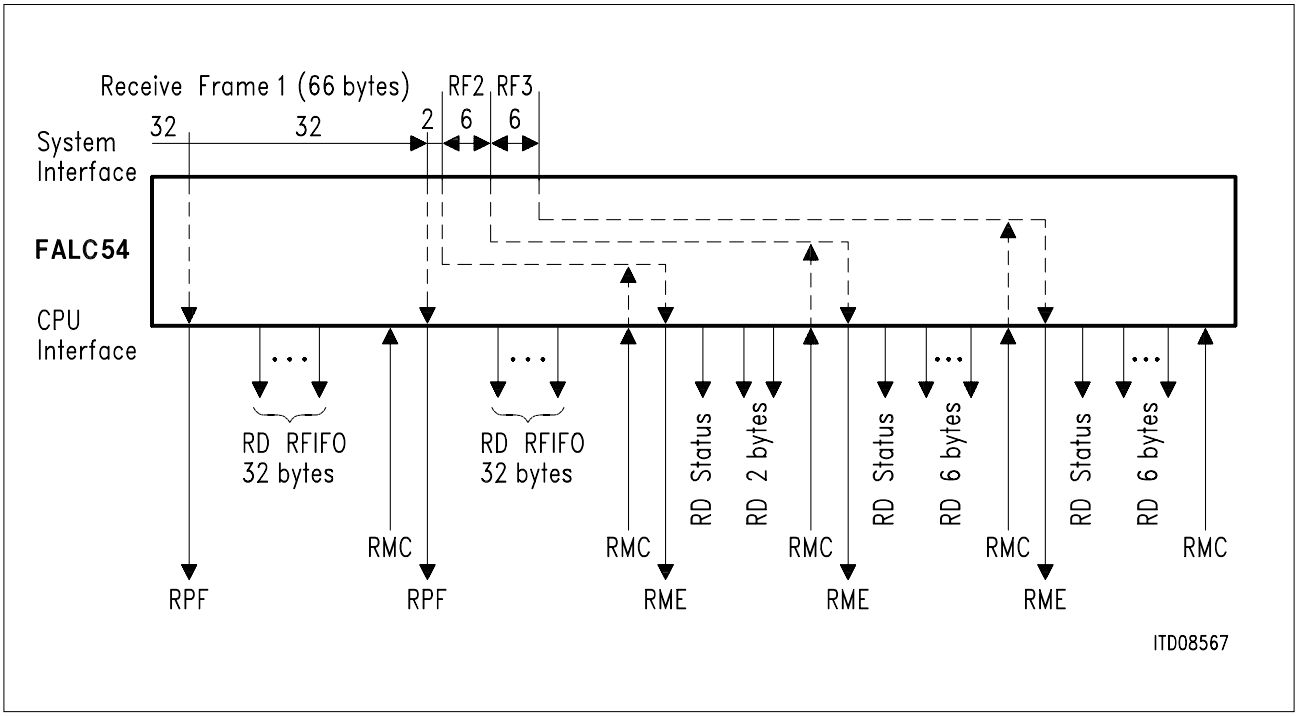


Figure 66
Interrupt Driven Reception Sequence Example

6.1 Detailed Register Description T1

6.1.1 Control Register Definition

Address	Register	Type	Comment
00	XFIFO	W	Transmit FIFO
01	XFIFO	W	Transmit FIFO
02	CMDR	W	Command Register
03	MODE	R/W	Mode Register
04	RAH1	R/W	Receive Address High 1
05	RAH2	R/W	Receive Address High 2
06	RAL1	R/W	Receive Address Low 1
07	RAL2	R/W	Receive Address Low 2
08	IPC	R/W	Interrupt Port Configuration
09	CCR1	R/W	Common Configuration Register 1
0A	CCR3	R/W	Common Configuration Register 3
0B	PRE	R/W	Preamble Register
0C	RTR1	R/W	Receive Timeslot Register 1
0D	RTR2	R/W	Receive Timeslot Register 2
0E	RTR3	R/W	Receive Timeslot Register 3
0F	RTR4	R/W	Receive Timeslot Register 4
10	TTR1	R/W	Transmit Timeslot Register 1
11	TTR2	R/W	Transmit Timeslot Register 2
12	TTR3	R/W	Transmit Timeslot Register 3
13	TTR4	R/W	Transmit Timeslot Register 4
14	IMR0	R/W	Interrupt Mask Register 0
15	IMR1	R/W	Interrupt Mask Register 1
16	IMR2	R/W	Interrupt Mask Register 2
17	IMR3	R/W	Interrupt Mask Register 3
18	IMR4	R/W	Interrupt Mask Register 4
19			
1A	FMR0	R/W	Framer Mode Register 0
1B	FMR1	R/W	Framer Mode Register 1
1C	FMR2	R/W	Framer Mode Register 2

6.1.1 Control Register Definition (cont'd)

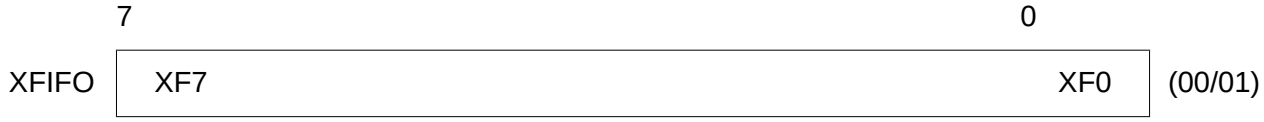
Address	Register	Type	Comment
1D	LOOP	R/W	Channel Loop Back
1E	FMR4	R/W	Framer Mode Register 4
1F	FMR5	R/W	Framer Mode Register 5
20	XC0	R/W	Transmit Control 0
21	XC1	R/W	Transmit Control 1
22	RC0	R/W	Receive Control 0
23	RC1	R/W	Receive Control 1
24	XPM0	R/W	Transmit Pulse Mask 0
25	XPM1	R/W	Transmit Pulse Mask 1
26	XPM2	R/W	Transmit Pulse Mask 2
27			
28	TEST	W	Manufacturer Test Register
29	IDLE	R/W	Idle Channel Code
2A	XDL1	R/W	Transmit DL-Bit Register 1
2B	XDL2	R/W	Transmit DL-Bit Register 2
2C	XDL3	R/W	Transmit DL-Bit Register 3
2D	CCB1	R/W	Clear Channel Register 1
2E	CCB2	R/W	Clear Channel Register 2
2F	CCB3	R/W	Clear Channel Register 3
30	ICB1	R/W	Idle Channel Register 1
31	ICB2	R/W	Idle Channel Register 2
32	ICB3	R/W	Idle Channel Register 3
33	ICB4	R/W	Idle Channel Register 4
34	LIM0	R/W	Line Interface Mode 0
35	LIM1	R/W	Line Interface Mode 1
36	PCD	R/W	Pulse Count Detection
37	PCR	R/W	Pulse Count Recovery
38	LIM2	R/W	Line Interface Register 2
60	DEC	W	Disable Error Counter
62	TEST	W	Manufacturer Test Register

6.1.1 Control Register Definition (cont'd)

Address	Register	Type	Comment
70	XS1	W	Transmit Signaling Register 1
71	XS2	W	Transmit Signaling Register 2
72	XS3	W	Transmit Signaling Register 3
73	XS4	W	Transmit Signaling Register 4
74	XS5	W	Transmit Signaling Register 5
75	XS6	W	Transmit Signaling Register 6
76	XS7	W	Transmit Signaling Register 7
77	XS8	W	Transmit Signaling Register 8
78	XS9	W	Transmit Signaling Register 9
79	XS10	W	Transmit Signaling Register 10
7A	XS11	W	Transmit Signaling Register 11
7B	XS12	W	Transmit Signaling Register 12

After 'RESET' all control registers except the XFIFO and XS1-12 are initialized to defined values.

Transmit FIFO (WRITE) XFIFO



Up to 32 bytes/16 words of received data can be read from the RFIFO following an RPF or an RME interrupt.
Writing data to XFIFO can be done in 8-bit (byte) or 16-bit (word) access. The LSB is transmitted first.

Up to 32 bytes/16 words of transmit data can be written to the XFIFO following an XPR (or ALLS) interrupt.

Command Register (Read/Write)

Value after RESET: 00_H

	7							0	
CMDR	RMC	RRES	XREP	XRES	XHF	XTF	XME	SRES	(02)

RMC… **Receive Message Complete**

Confirmation from CPU to FALC54 that the current frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

RRES… **Receiver Reset**

The receive line interface except the clock and data recovery unit (DPLL), the receive framer, the one second timer and the receive signaling controller are reset. However the contents of the control registers will not be deleted.

XREP… **Transmission Repeat**

If XREP is set to one together with XTF (write 24H to CMDR), the FALC54 repeatedly transmits the contents of the XFIFO (1…32 bytes) without HDLC framing fully transparently, i.e. without FLAG,CRC.

The cyclic transmission is stopped with an SRES command or by resetting XREP.

Note: During cyclic transmission the XREP- bit has to be set with every write operation to CMDR.

XRES… **Transmitter Reset**

The transmit framer and transmit line interface excluding the system clock generator and the pulse shaper will be reset. However the contents of the control registers will not be deleted.

XHF… **Transmit HDLC Frame**

After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a HDLC frame.

XTF… **Transmit Transparent Frame**

Initiates the transmission of a transparent frame without HDLC framing.

XME… **Transmit Message End**

Indicates that the data block written last to the transmit FIFO completes the current frame. The FALC54 can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

SRES… **Signaling Transmitter Reset**

The transmitter of the signaling controller will be reset. XFIFO is cleared of any data and an abort sequence (seven 1's) followed by interframe time fill is transmitted. In response to XRES an XPR interrupt is generated.

This command can be used by the CPU to abort a frame currently in transmission.

Note: The maximum time between writing to the CMDR register and the execution of the command depends on FMR1.IMOD. If FMR1.IMOD is set it takes 10 SCLKX cycles and 5 SCLKX cycles if FMR1.IMOD is cleared. Therefore, if the CPU operates with a very high clock rate in comparison with the FALC's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.

Mode Register (Read/Write)

Value after RESET: 00_H

	7							0	
MODE	MDS2	MDS1	MDS0	BRAC	HRAC				(03)

MDS2-0… **Mode Select**

The operating mode of the HDLC controller is selected.

000… Reserved
001… Reserved
010… 1 byte address comparison mode (RAL1, 2)
011… 2 byte address comparison mode (RAH1, 2 and RAL1, 2)
100… No address comparison
101… 1 byte address comparison mode (RAH1, 2)
110… Reserved
111… No HDLC framing mode 1

BRAC… **BOM Receiver Active**

Switches the BOM receiver to operational or inoperational state.

0… Receiver inactive

1… Receiver active

HRAC… **HDLC Receiver Active**

Switches the HDLC receiver to operational or inoperational state.

0… Receiver inactive
1… Receiver active

Receive Address Byte High Register 1 (Read/Write)
Value after RESET: FD_H

	7			0	
RAH1			0		(04)

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individually programmable values in RAH1 and RAH2.

RAH1… **Value of the First Individual High Address Byte**

Bit 1 (C/R-bit) is excluded from address comparison.

Receive Address Byte High Register 2 (Read/Write)
Value after RESET: FF_H

	7		0	
RAH2				(05)

RAH2… **Value of Second Individual High Address Byte**

Receive Address Byte Low Register 1 (Read/Write)
Value after RESET: FF_H

	7							0	
RAL1									(06)

RAL1… **Value of First Individual Low Address Byte**

Receive Address Byte Low Register 2 (Read/Write)
Value after RESET: FF_H

	7							0	
RAL2									(07)

RAL2... **Value of the second individually programmable low address byte.**

Interrupt Port Configuration (READ/WRITE)

Value after RESET: 00_H

	7							0	
IPC	VIS					SCI	IC1	IC0	(08)

Unused bits have to be set to logical ‘0’.

VIS… **Masked Interrupts Visible**

0… Masked interrupt status bits are not visible.

1… Masked interrupt status bits are visible.

SCI… **Status Change Interrupt**

0… Interrupts will be generated either on coming or going of the internal interrupt source.

1… The following interrupts will be activated if enabled with detecting and recovering of the internal interrupt source:
ISR2.LOS
ISR2.AIS
ISR0.PDEN

IC0, IC1… **Interrupt Port Configuration**

These bits define the function of the interrupt output stage (pin INT):

IOC1	IOC0	Function
X	0	Open drain output
0	1	Push/pull output, active low
1	1	Push/pull output, active high

Common Configuration Register 1 (READ/WRITE)

Value after RESET: 00_H

	7							0	
CCR1	SFLG	BRM	EDLX	EITS	ITF		RFT1	RFT0	(09)

SFLG… **Enable Shared Flags**

If this bit is set, the closing FLAG of a preceding frame simultaneously becomes the opening FLAG of the following frame.

BRM… **BOM Receive Mode (significant in BOM mode only)**

0… 10 byte packets

1… Continuous reception

EDLX… **Enable DL Bit Access via the Transmit FIFO**

A one in this bit position enables the internal DL- bit access via the transmit FIFO of the signaling controller. FMR1.EDL has to be cleared to enable the sending of the contents of the XFIFO on the ports XL1/2 or XDOP/N.

EITS… **Enable Internal Time-Slot 0-31 Signaling**

0… Internal signaling in time-slots 0-31 defined via registers RTR1-4 or TTR1-4 is disabled.

1… Internal signaling in time-slots 0-31 defined via registers RTR1-4 or TTR1-4 is enabled.

ITF… **Interframe Time Fill**

Determines the idle (= no data to send) state of the transmit data coming from the signaling controller.

0… Continuous logical ‘1’ is output

1… Continuous FLAG sequences are output (‘01111110’ bit patterns)

RFT1, RFT0… **RFIFO Threshold Level**

The size of the accessible part of RFIFO can be determined by programming these bits. The number of valid bytes after an RPF interrupt is given in the following table:

RFT1	RFT0	Size of Accessible Part of RFIFO
0	0	32 bytes (RESET value)
0	1	16 bytes
1	0	4 bytes
1	1	2 bytes

The value of RFT 1,0 can be changed dynamically

– If reception is not running or

– after the current data block has been read, but before the command CMDR.RMC is issued (interrupt controlled data transfer). See **Note**.

*Note: It is seen that changing the value of RFT1,0 is possible even during the reception of one frame. The total length of the received frame can be always read directly in RBCL, RBCH after an RPF interrupt, except when the threshold is increased during reception of that frame. The real length can then be inferred by noting which bit positions in RBCL are reset by an RMC command (see **table below**):*

RFT1	RFT0	Bit Positions in RBCL Reset by a CMDR.RMC Command
0	0	RBC4 …. 0
0	1	RBC3 … 0
1	0	RBC1,0
1	1	RBC0

Common Configuration Register 3 (READ/WRITE)

Value after RESET: 00_H

	7							0	
CCR3	PRE1	PRE0	EPT	RADD		RCRC	XCRC		(0A)

Unused bits have to be set to logical ‘0’.

PRE1, PRE0… Number of Preamble Repetition

If Preamble transmission is initiated, the Preamble defined via register PRE is transmitted

00… 1 times
01… 2 times
10… 4 times
11… 8 times.

EPT… Enable Preamble Transmission

This bit enables transmission of a preamble. The preamble is started after Interframe Timefill transmission has been stopped and a new frame is to be transmitted. The preamble consists of an 8-bit pattern repeated a number of times. The pattern is defined via register PRE, the number of repetitions is selected by bits PRE0 and PRE1.

Note: The "Shared Flag" feature is not influenced by preamble transmission.
Zero Bit Insertion is disabled during preamble transmission.

RADD… Receive Address Pushed to RFIFO

If this bit is set to '1', the received HDLC address information (1 or 2 bytes, depending on the address mode selected via MODE.MDS0) is pushed to RFIFO. This function is applicable in non-auto mode.

RCRC… Receive CRC ON/OFF

Only applicable in non-auto mode.

If this bit is set to '1', the received CRC checksum will be written to RFIFO (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO by the status information byte (contents of register RSIS). The received CRC checksum will additionally be checked for correctness. If non-auto mode is selected, the limits for "Valid Frame" check are modified (refer to **RSIS.VFR**).

XCRC… Transmit CRC ON/OFF

If this bit is set to '1', the CRC checksum will not be generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO). The transmitted frame will be closed automatically with a closing flag.

Note: The FALC54 does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

Preamble Register (Read/Write)

Value after RESET: 00_H

	7							0	
PRE	PRE7							PRE0	(0B)

PRE0...PRE7... Preamble Register

This register defines the pattern which is sent out during preamble transmission (refer to **register CCR3**). LSB is sent first.

It should be taken into consideration that Zero Bit Insertion is disabled during preamble transmission.

Receive Timeslot Register 1-4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
RTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(0C)
RTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(0D)
RTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(0E)
RTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(0F)

TS0…TS31… Timeslot Register

These bits define the received channels (time-slots) on the system highway to be extracted. Additionally this registers will control the RSIGM marker which can be forced high during the respective time-slots independent of bit CCR1.EITS.
A one in the RTR1-4 bits will sample the corresponding time-slot from the system highway if bit CCR1.EITS is set.

Assignments:
TS0 $\rightarrow$ time-slot 0

.

.

.
TS31 $\rightarrow$ time-slot 31

0 … Normal operation.

1… The contents of the selected time-slot will be stored in the RFIFO. Although the idle time-slots can be selected. This function will only become active if bits CCR1.EITS is set.
The corresponding time-slot will be forced high on pin RSIGM.

Transmit Timeslot Register 1-4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
TTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(10)
TTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(11)
TTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(12)
TTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(13)

TS0…TS31… Transmit Timeslot Register

These bits define the transmit channels (time-slots) on the system highway to be inserted. Additionally this registers will control the XSIGM marker which can be forced high during the respective time-slots independent of bit CCR1.EITS.
A one in the TTR1-4 bits will insert the corresponding time-slot on the system highway if bit CCR1.EITS is set.

Assignments:
TS0 → time-slot 0

.

.

.
TS31 → time-slot 31

0 … Normal operation.

1… The contents of the selected time-slot will be inserted in the outgoing data stream. Although the idle time-slots can be selected. This function will only become active if bits CCR1.EITS is set.
The corresponding time-slot will be forced high on pin XSIGM.

Interrupt Mask Register 0…4

Value after RESET: FF_H, FF_H, FF_H, FF_H,FF_H

	7							0	
IMR0	RME	RFS	ISF	RMB	RSC	CRC6	PDEN	RPF	(14)
IMR1	CASE	RDO	ALLS	XDU	XMB		XLSC	XPR	(15)
IMR2	FAR	LFA	MFAR	LMFA	AIS	LOS	RAR	RA	(16)
IMR3	ES	SEC	XSLP		LLBSC		SLN	SLP	(17)
IMR4	LFA	FER	CER	AIS	LOS	CVE	SLIP		(18)

IMR0...IMR4... Interrupt Mask Register

Each interrupt source can generate an interrupt signal at port INT (characteristics of the output stage are defined via register IPC). A ‘1’ in a bit position of IMR0…4 sets the mask active for the interrupt status in ISR0…3. Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they will

– not be displayed in the Interrupt Status Register if bit IPC.VIS is set to ‘0’

– be displayed in the Interrupt Status Register if bit IPC.VIS is set to ‘1’.

After RESET, all interrupts are **dis**abled.

Framer Mode Register 0 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR0	XC1	XC0	RC1	RC0	FRS	SRAF	EXLS	SIM	(1A)

XC1…XC0… Transmit Code

Serial code transmitter is different programmable from the receiver.

00… NRZ (optical interface)
01… Not assigned
10… AMI coding with Zero Code Suppression (ZCS, B7 - Stuffing). Disabling of the ZCS is done by activating the clear channel mode via register CCB1-3. (ternary or digital interface)
11… B8ZS Code (ternary or digital dual rail interface)

RC1…RC0… **Receive Code**

Serial code receiver is different programmable from the transmitter.

00… NRZ (optical interface)
01… Not assigned
10… AMI coding with Zero Code Suppression (ZCS, B7 - Stuffing), (ternary or digital dual rail interface)
11… B8ZS Code (ternary or digital dual rail interface)

FRS… **Force Resynchronization**

A transition from low to high will force the frame aligner to execute a resynchronization of the pulse frame. In the asynchronous state, a new frame position is assumed at the next candidate if there is one. Otherwise, a new frame search with the meaning of a general reset is started. In the synchronous state this bit will have the same meaning as bit FMR0.EXLS except if FMR2.MCSP=1.

SRAF… **Select Remote (Yellow) Alarm Format for F12 and ESF Format**

0… F12: bit2 = 0 in every channel. ESF: pattern '1111 1111 0000 0000…' in data link channel.
1… F12: FS bit of frame 12. ESF: bit2 = 0 in every channel

EXLS… **External Loss Of Frame**

With a low to high transition a new frame search will be started. This has the meaning of a general reset of the internal frame alignment unit. Synchronous state is reached only if there is one definite framing candidate. In the case of multiple candidates, the setting of the bit FMR0.FRS forces the receiver to lock onto the next available framing position.

SIM… **Alarm Simulation**

Setting/resetting this bit initiates internal error simulation of: AIS (blue alarm), loss of signal (red alarm), loss of frame alignment, slip, framing errors, CRC errors, code violations. The error counters FEC, CVC, CEC, EBC will be incremented.

The selection of simulated alarms is done via the error simulation counter: FRS2.ESC2-0 which will be incremented with each setting of bit FMR0.SIM. For complete checking of the alarm indications eight simulation steps are necessary (FRS2.ESC2-0 = 0 after a complete simulation).

Framer Mode Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR1	CTM	SIGM	EDL	PMOD	CRC	ECM	IMOD	XAIS	(1B)

CTM… **Channel Translation Mode**

0… Channel translation mode 0

1… Channel translation mode 1

SIGM… **Select Signaling Mode**

0… CCS/CAS-CC mode

1… CAS-BR mode

For selection of clear channels refer Clear Channel Register CCB1…CCB3.

EDL… **Enable DL-Bit Access via Register XDL1-3**

Only applicable in F4, F24 or F72 frame format.

0… Normal operation. The DL-bits will be taken from system highway or if enabled via CCR1.EDLX from the XFIFO of the signaling controller.

1… DL-bit register access. The DL-bit information will be taken from the registers XDL1-3 and will overwrite the DL-bits received at the system highway (pin XDI) or the internal XFIFO of the signaling controller. However, transmitting contents of registers XDL1-3 will be disabled if transparent mode is enabled (FMR4.TM).

PMOD… **PCM Mode**

For T1 application this bit must be set high. Switching into T1 mode the device needs up to 20 µsec to settle up to the internal clocking.

1… PCM 24 mode.

CRC… **Enable CRC6**

This bit is only significant when using the ESF format.

0… CRC6 check/generation disabled. For transmit direction, all CRC bit positions are set to ‘1’.

1… CRC6 check/generation enabled.

ECM… **Error Counter Mode**

The function of the error counters (FEC,CEC,CVC,EBC) will be determined by this bit.

0… Before reading an error counter the corresponding bit in the Disable Error Counter register (DEC) has to be set. In 8 bit access the low byte of the error counter should always be read before the high byte. The error counters will be reset with the rising edge of the corresponding bits in the DEC register.

1… Every second the error counter will be latched and then automatically be reset. The latched error counter state should be read within the next second. Reading the error counter during updating should be avoided.

IMOD… **System Interface Mode**

0… 4 Mbit/s mode

1… 2 Mbit/s mode

XAIS… **Transmit AIS Towards Remote End**

Sends AIS (blue alarm) via ports: XL1, XL2 towards the remote end.

If Local Loop Mode is enabled the transmitted data are looped back to the system internal highway without any changes.

Framer Mode Register 2 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR2		MCSP	SSP	DAIS	SAIS	PLB	AXRA	EXZE	(1C)

MCSP... **Multiple Candidates Synchronization Procedure**

Only valid if F24 format is selected:

0... normal operation (identical to the synchronization procedure implemented in FALC54 V1.1).

1... A one will enable a synchronization mode which is able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the synchronization might have been based on an alias framing pattern, setting of FMR0.FRS will lead to synchronization on the next candidate available. However, only the previously assumed

candidate will discarded in the internal framing pattern memory. The latter procedure can be repeated until the framer has locked on the right pattern (no extensive CRC errors).

SSP… Select Sync/Resync Procedure

Only valid if F12 or F72 format is selected:

0… Specified number of errors in both FT framing and FS framing lead to loss of sync (FRS0.LFA is set). In the case of FS bit framing errors, bit FRS0.LMFA is set additionally. A complete new synchronization procedure is initiated to regain pulseframe alignment and then multiframe alignment.

1… Specified number of errors in FT framing has the same effect as above. Specified number of errors in FS framing only initiates a new search for multiframe alignment without influencing pulseframe synchronous state (FRS0.LMFA is set).

DAIS… Disable AIS to System Interface

0… AIS is automatically inserted into the data stream to RDO if FALC54 is in asynchronous state.

1… Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit FMR2.SAIS.

SAIS… Send AIS Towards System Interface

Sends AIS (blue alarm) via output RDO towards system interface. This function is not influenced by bit FMR2.DAIS.

PLB… Payload Loop Back

0 … Normal operation

1… The payload loopback will loop the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received at port XDI, SYPXQ and XMFS will be ignored. With FMR4.TM=1 all 193 bits per frame will be looped back. If FMR4.TM=0 the DL- or FS- or CRC- bits will be generated internally. AIS is sent immediately on port RDO by setting the FMR2.SAIS bit. During payload loop is active the receive time-slot offset (registers RC1/0) should not be changed.

AXRA… **Automatic Transmit Remote Alarm**

0 … Normal operation

1… The Remote Alarm (yellow alarm) bit will be automatically set in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit will be reset.

EXZE… **Excessive Zeros Detection Enable**

Selects error detection mode in the bipolar receive bit stream.

0… Only bipolar violations are detected.

1… Bipolar violations and zero strings of 8 or more contiguous zeros in B8ZS code or more than 15 contiguous zeros in AMI code are detected additionally and counted in the code violation counter CVC.

LOOP (Read/Write)

Value after RESET: 00_H

	7				0	
LOOP		RTM	ECLB	CLA4	CLA0	(1D)

RTM… **Receive Transparent Mode**

Setting this bit disconnects control of the internal elastic store from the receiver. The elastic store is now in a “free running” mode without any possibility to actualize the time slot assignment to a new frame position in case of re-synchronization of the receiver. This function can be used in conjunction with the “disable AIS to system interface” feature (FMR2.DAIS) to realize undisturbed transparent reception.

ECLB… **Enable Channel Loop Back**

0… Disables the channel loop back.

1… Enables the channel loop back selected by this register.

CLA4…CLA0… **Channel Address For Loop Back**

CLA = 1…24 selects the channel.

During loop back, the contents of the associated outgoing channel at ports XL1/XDOP/XOID and XL2/XDON is equal to the idle channel code programmed in register IDLE.

Framer Mode Register 4 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR4	AIS3	TM	XRA	SSC1	SSC0	AUTO	FM1	FM0	(1E)

AIS3… **Select AIS Condition**

0… AIS (blue alarm) is indicated (FRS0.AIS) when two or less zeros in the received bit stream are detected in a time interval of 12 frames (F4, F12, F72) or 24 frames (ESF).

1… AIS (blue alarm) detection is only enabled when FALC54 is in asynchronous state. The alarm is indicated (FRS0.AIS) when

– three or less zeros within a time interval of 12 frames (F4, F12, F72), or

– five or less zeros within a time interval of 24 frames (ESF) are detected in the received bit stream.

TM… **Transparent Mode**

Setting this bit enables the transparent mode:

– In transmit direction bit 8 of every FS/DL time-slot from the system internal highway (XDI) is inserted in the F-bit position of the outgoing frame. Internal framing generation, insertion of CRC and DL data is disabled.

– In receive direction the framing bit is also forwarded to RDO and inserted in the FS/DL timeslot. Bit RDCF (bit 1 of FS/DL time-slot) indicates a DL bit.

XRA… **Transmit Remote Alarm (Yellow Alarm)**

If high, remote alarm is sent via PCM route. Clearing the bit will remove the remote alarm pattern. Remote alarm indication depends on the multiframe structure as follows:

F4: bit2 = 0 in every speech channel
F12: – FMR0.SRAF = 0: bit2 = 0 in every speech channel
– FMR0.SRAF = 1: FS-bit of frame 12 is forced to ‘1’
ESF: – FMR0.SRAF = 0: pattern ‘1111 1111 0000 0000…’ in data link channel
– FMR0.SRAF = 1: bit2 = 0 in every speech channel
F72: bit2 = 0 in every speech channel

SSC1/0… **Select Sync Conditions**

Loss of Frame Alignment (FRS0.LFA or opt. FRS0.LMFA) is declared if
00 = 2 out of 4 framing bits
01 = 2 out of 5 framing bits
10 = 2 out of 6 framing bits in F4/12/72 format
10 = 2 out of 6 framing bits per multiframe period in ESF format
11 = reserved
are incorrect. It depends on the selected multiframe format and optionally on bit FMR2.SSP which framing bits are observed:

F4: FT bits → FRS0.LFA
F12, F72: SSP = 0: FT bits → FRS0.LFA: FS bits → FRS0.LFA
and FRS0.LMFA SSP = 1:FT → FRS0.LFA
FS → FRS0.LMFA
ESF: ESF framing bits → FRS0.LFA

AUTO… **Enable Auto Resynchronization**

0… The receiver will not resynchronize automatically. Starting a new synchronization procedure is possible via the bits: FMR0.EXLS or FMR0.FRS.

1… Auto-resynchronization is enabled.

FM1…FM0… **Select Frame Mode**

FM = 0: 12-frame multiframe format (F12, D3/4)
FM = 1: 4-frame multiframe format (F4)
FM = 2: 24-frame multiframe format (ESF)
FM = 3: 72-frame multiframe format (F72, remote switch mode)

Framer Mode Register 5 (Read/Write)

Value after RESET: 00_H

	7						0	
FMR5		EIBR	XLD	XLU				(1F)

EIBR… **Enable Internal Bit Robbing Access**

0… Normal operation.

1… A one in this bit position will cause the transmitter to send the bit robbing signaling information stored in the XS1-12 (ESF) resp. XS1-6 (F12/72) registers in the corresponding time slots.

XLD… **Transmit LOOP Down Code**

0… Normal operation.

1… A one in this bit position will cause the transmitter to replace normal transmit data with the Loop Down Code: 001 continuously until this bit is reset. The Loop Down Code will be overwritten by the framing/DL/CRC bits.

XLU… **Transmit LOOP UP Code**

0… Normal operation.

1… A one in this bit position will cause the transmitter to replace normal transmit data with the Loop UP Code '00001' continuously until this bit is reset. The Loop UP Code will be overwritten by the framing/DL/CRC bits.

Transmit Control 0 (Read/Write)

Value after RESET: 00_H

	7						0	
XC0	BRM	MFBS		SFRZ		XCO2	XCO0	(20)

BRM… **Enable Bit Robbing Marker**

A one in this bit will mark the robbed bit positions on the system highway. RSIGM marks the receive and XSIGM marks the transmit robbed bits. Only valid if robbed bit signaling is enabled (FMR1.SIGM=1).

MFBS… **Enable pure Multiframe Begin Signals**

Only valid if ESF or F72 format is selected.

If set, signals RMFB and XMFB indicate only the multiframe begin. Additional pulses (every 12 frames) are disabled.

SFRZ… **Select Freeze Output**

0 … Signal $\overline{\text{RFSP}}$ is output on port $\overline{\text{RFSP}}$/FREEZE.

1 … Freeze status signal will be output on port $\overline{\text{RFSP}}$/FREEZE.

XCO2…XCO0… **Transmit Clock-Slot Offset**

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse at port SYPXQ is active (see **figure 57**).

Transmit Control 1 (Read/Write)

Value after RESET: 00_H

	7							0	
XC1	XCOS		XTO5					XTO0	(21)

XCOS… **Transmit Clock Offset Shift**

0… The delay T between the beginning of time-slot 0 and the initial edge of SCLKX (after $\overline{\text{SYPX}}$ goes active) is an even number in the range from 0 to 1022 SCLKX cycles.

1… The delay T is an odd number in the range from 1 to 1023 SCLKX cycles.

XTO5…XTO0… **Transmit Time-slot Offset**

Initial value loaded into the transmit time-slot counter at the trigger edge of SCLKX when the synchronous pulse at port SYPXQ is active (see **figure 57**).

A write access to this address resets the transmit speech memory to its basic starting position. Therefore, updating the value should only be done when the FALC54 is initialized or when a transmit slip indicates a defective clock system.

Receive Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
RCO	RCOS	SICS	CRCI	XCRCI	RDIS	RCO2	RCO1	RCO0	(22)

RCOS… **Receive Clock Offset Shift**

0… The delay T between the beginning of time-slot 0 and the initial edge of SCLKR (after $\overline{\text{SYPR}}$ goes active) is an even number in the range from 0 to 1022 SCLKR cycles.

1… The delay T is an odd number in the range from 1 to 1023 SCLKR cycles.

SICS… **System Interface Channel Select**

Only applicable if bit FMR1.IMOD (4 MHz system interface) is set.

0… Received data is output on port RDO in the first channel phase. Data in the second channel phase is tri-stated.

Data on pin XDI is sampled only in the first channel phase. Data in the second channel phase is ignored.

1… Data on port RDO is output in the second channel phase. The first channel phase is tri-stated. Sampling of data from the system highway is done in the second channel phase.

CRCI… **Automatic CRC6 Bit Inversion**

If set, all CRC bits of one outgoing extended multiframe are inverted in case a CRC error is flagged for the previous received multiframe. This function is logically ORed with RC0.XCRCI.

XCRCI… **Transmit CRC6 Bit Inversion**

If set, the CRC bits in the outgoing data stream are inverted before transmission. This function is logically ORed with RC0.CRCI.

RDIS… **Receive Data Input Sense**

0… Inputs: RDIP, RDIN active low, input ROID is active high

1… Inputs: RDIP, RDIN active high, input ROID is active low

RCO2…RCO0… **Receive Clock-Slot Offset**

Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active (see **figure 56**).

Receive Control 1 (Read/Write)

Value after RESET: 00_H

	7			0	
RC1		RRAM	RTO5	RTO0	(23)

RRAM… **Receive Remote Alarm Mode**

The conditions for remote (yellow) alarm (FRS0.RRA) detection can be selected via this bit to allow detection even in the presence of BER 10**-3:
RRAM = 0
Detection

F4: bit2 = 0 in every speech channel per frame.
F12: – FMR0.SRAF = 0: bit2 = 0 in every speech channel per frame.
– FMR0.SRAF = 1: S-bit of frame 12 is forced to ‘1’
ESF: – FMR0.SRAF = 0: pattern ‘1111 1111 0000 0000…’ in data link channel
– FMR0.SRAF = 1: bit2 = 0 in every speech channel
F72: bit2 = 0 in every speech channel per frame.

Release
The alarm will be reset when above conditions are no longer detected.
RRAM = 1
Detection
F4: bit2 = 0 in 255 consecutive speech channels.
F12: – FMR0.SRAF = 0: bit 2 = 0 in 255 consecutive speech channels.
– FMR0.SRAF = 1: S-bit of frame 12 is forced to ‘1’
ESF: – FMR0.SRAF = 0: pattern ‘1111 1111 0000 0000…’ in data link channel
– FMR0.SRAF = 1: bit 2 = 0 in 255 consecutive speech channels
F72: bit 2 = 0 in 255 consecutive speech channels.

Release
Depending on the selected multiframe format the alarm will be reset when FALC54 does not detect

– the ‘bit 2 = 0’ condition for three consecutive pulseframes (all formats if selected),
– the ‘FS bit’ condition for three consecutive multiframes (F12),
– the ‘DL pattern’ for three times in a row (ESF).

RTO5…RTO0…Receive Time-Slot Offset

Initial value loaded into the receive time-slot counter at the trigger edge of SCLKR when the synchronous pulse at port $\overline{\text{SYPR}}$ is active (see **figure 56**).

Transmit Pulse-Mask 2…0 (Read/Write)

Value after RESET: $9C_H$, 03_H, 00_H

	7							0	
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00	(24)

XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13	(25)
XPM2	XLHP	XLT	DAXLT		XP34	XP33	XP32	XP31	(26)

The transmit pulse shape which is defined in ITU-T G.703 will be output on pins XL1 and XL2. The level of the pulse shape can be programmed via registers XPM2-0 to create a custom waveform. In order to get an optimized pulse shape for the external transformers each pulse shape will be internally devided into four sub pulse shapes. In each sub pulse shape a programmed 5 bit value will define the level of the analog voltage on pins XL1/2. Together four 5 bit values have to be programmed to form one complete transmit pulse shape.The four 5 bit values will be sent in the following sequence:

XP04-00: First pulse shape level
XP14-10: Second pulse shape level
XP24-20: Third pulse shape level
XP34-30: Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM2-0 will change the amplitude of the differential voltage on XL1/2 by approximately 110 mV.
The XPM- values are valid for the following external circuitry: transformer ratio: 1:sqrt(2); cable: PULB 22AWG (100 Ω); serial resistors: 5 Ω.

DS1: The XPMxx register values shown in the table below are in decimal format.

Range in m	**XP04-XP00**	**XP14-XP10**	**XP24-XP20**	**XP34-XP30**
0 - 35	29	27	10	3
25 - 65	29	28	10	3
55 - 95	31	28	10	2
85 - 125	31	27	13	2
115 - 155	31	26	13	2
145 - 185	31	26	13	3
175 - 210	31	25	14	3

T1- 18 dB: The XPMxx register values shown in the table below are in decimal format.

	XP04-XP00	**XP14-XP10**	**XP24-XP20**	**XP34-XP30**
	24	22	7	3

XLHP… Transmit Line High Power

0 ... Normal operation.

1 ... With this bit the output current capability of the transmit line XL1 and XL2 can be influenced. Connecting low impedances to the outputs XL1/XL2 this bit should be set to one to avoid instable pulse shapes. Setting this bit has no influence on the voltage levels of the pulse shape.

XLT… Transmit Line Tri-state

0 … Normal operation

1 … Transmit line XL1/XL2 or XDOP/XDON are switched into high impedance state. If this bit is set the transmit line monitor status information will be frozen.

DAXLT... Disable Automatic Tristating of XL1/2

0... Normal operation. If a short is detected on pins XL1/2 the transmit line monitor will set the XL1/2 outputs into a high impedance state.

1... If a short is detected on pins XL1/2 an automatic setting these pins into a high impedance state (by the XL-monitor) will be disabled.

Idle Channel Code Register (Read/Write)

Value after RESET: 00_H

	7						0	
IDLE	IDL7						IDL0	(29)

IDL7…IDL0… Idle Channel Code

If channel loop back is enabled by programming the register LOOP.ECLB = 1, the contents of the assigned outgoing channel at ports XL1/XL2 resp. XDOP/XDON is set equal to the idle channel code selected by this register.

Additionally, the specified pattern overwrites the contents of all channels of the outgoing PCM frame selected via the idle channel registers ICB1…ICB3. IDL7 will be transmitted first.

Transmit DL-Bit Register 1-3 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H

	7							0	
XDL1	XDL17	XDL16	XDL15	XDL14	XDL13	XDL12	XDL11	XDL10	(2A)
XDL2	XDL27	XDL26	XDL25	XDL24	XDL23	XDL22	XDL21	XDL20	(2B)
XDL3	XDL37	XDL36	XDL35	XDL34	XDL33	XDL32	XDL31	XDL30	(2C)

XDL1…XDL3… Transmit FS/DL-Bit Data

The DL-bit register access is enabled by setting bits FMR1.EDL = 1. With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers XDL1-3 will be copied into a shadow register. The contents will subsequently sent out in the data stream of the next outgoing multiframe if no transparent mode is enabled. XDL10 will be sent out first.
In F4 frame format only XDL10+XDL11 will be transmitted. In F24 frame format XDL10-XDL23 will be shifted out. In F72 frame format XDL10-XDL37 will be transmitted.
The transmit multiframe begin interrupt (XMB) requests that these registers should be serviced. If requests for new information will be ignored, current contents will be repeated.

Clear Channel Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H

	7							0	
CCB1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	(2D)
CCB2	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	(2E)
CCB3	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	(2F)

CH1…CH24… Channel Selection Bits

0… Normal operation. Bit robbing information and Zero Code Suppression (ZCS, B7 stuffing) may change contents of the selected speech/data channel if assigned modes are enabled via bits FMR1.SIGM and FMR0.XC1/0.

1… Clear channel mode. Contents of selected speech/data channel will not be overwritten by bit robbing and ZCS information. Transmission of channel assigned signaling and control of pulse density is applied by the user.

Idle Channel Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
ICB1	IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	(30)
ICB2	IC9	IC10	IC11	IC12	IC13	IC14	IC15	IC16	(31)
ICB3	IC17	IC18	IC19	IC20	IC21	IC22	IC23	IC24	(32)
ICB4				reserved					(33)

IC1…IC24… **Idle Channel Selection Bits**

These bits define the channels (time-slots) of the outgoing PCM frame to be altered.

0… Normal operation.

1… Idle channel mode. The contents of the selected channel is overwritten by the idle channel code defined via register IDLE.

Line Interface Mode 0 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM0	XFB	XDOS	SCL1	SCL0	EQON	ELOS	LL	MAS	(34)

XFB… **Transmit Full Bauded Mode**

0 … Output signals XDOP/XDON are half bauded (normal operation).

1 … Output signals XDOP/XDON are full bauded.

XDOS… **Transmit Data Output Sense**

0 … Output signals XDOP/XDON are active low (normal operation).

1 … Output signals XDOP/XDON are active high.

SCL1…SCL0… **Select Clock Output**

00 … Output frequency at pin CLKX : 2048 kHz active high

01 … Output frequency at pin CLKX : 2048 kHz active low

10 … Output frequency at pin CLKX : 4096 kHz active high

11 … Output frequency at pin CLKX : 4096 kHz active low

EQON… Receive Equalizer On

0 … 6 dB Receiver

1 … 18 dB Equalizer on

ELOS Enable Loss of Signal

0... Normal operation. The extracted receive clock is output via pin RCLK.

1... In case of loss of signal (FRS0.LOS=1) the RCLK is set high. If FRS0.LOS=0 the received clock is output via RCLK.

LL… Local Loop

0 … Normal operation

1 … Local loop active. The local loopback mode disconnects the receive lines RL1/RL2 resp. RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. The unipolar bit stream will be undisturbed transmitted on the line. Receiver and transmitter coding must be identical.

MAS… Master Mode

0 … Slave mode

1 … Master mode on. If this bit is set and the SYNC pin is connected to V_{SS} the FALC54 works as a master for the system. The internal DCO's of the jitter attenuator are centered and the system clocks which are output via CLK8M/CLKX are stable (divided from the DCO frequencies). If a clock (1.544 MHz or 2.048 MHz) is detected at the SYNC pin the FALC54 synchronizes automatically to this clock. The production tolerance is approximately ± 30 ppm of the crystal frequency if C_{Load} = 15 pF.

Line Interface Mode 1 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM1	EFSC	RIL2	RIL1	RIL0	DCOC	JATT	RL	DRS	(35)

EFSC… Enable Frame Synchronization Pulse

0 = The transmit clock is output via pin XCLK.

1 = Pin XCLK provides a 8 KHz frame synchronization pulse which is active high for one 2 MHz cycle (pulse width = 488 ns).

RIL2…RIL0… Receive Input Threshold

Only valid if analog line interface is selected (LIM1.DRS=0).

No signal will be declared if the voltage between pins RL1 and RL2 drops below the limits programmed via bits RIL2-0 and the received data stream has no transition for a period defined in the PCD register.

The threshold where no signal will be declared is programmable via the RIL2-0 bits.

000 = 1.36 V
001 = 1.04 V
010 = 0.84 V
011 = 0.62 V
100 = 0.43 V
101 = 0.32 V
110 = 0.22 V
111 = Not assigned

DCOC … **DCO1 Control**

A one in this bit position will enable to synchronize the internal generated systems clocks from DCO1 to an external 2 MHz clock provided on pin SYNC.

JATT…RL... Transmit Jitter Attenuator / Remote Loop

00 = Normal operation. The transmit jitter attenuator is disabled. Transmit data will bypass the buffer.

01 = Remote Loop active without transmit jitter attenuator enabled. Transmit data will bypass the buffer.

10 = not assigned

11 = Remote Loop and jitter attenuator active. Received data from pins RL1/2 or RDIP/N or ROID will be sent jitter free on ports XL1/2 or XDOP/N or XOID.

DRS… Dual Rail Select

0 = The ternary interface is selected. Multifunction ports RL1/2 and XL1/2 become analog in/outputs.

1 = The digital dual rail interface is selected. Received data is latched on multifunction ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Pulse Count Detection Register (Read/Write)

Value after RESET: 00_H

	7						0	
PCD	PCD7						PCD0	(36)

PCD7…PCD0… Pulse Count Detection

A LOS alarm (red alarm) will be detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable via the PCD register and can be calculated as follows:
T= 16(N+1) ; with 0 =< N =< 255.

The maximum time is: 256 × 16 × 648 ns = 2.65 ms. Every detected pulse will reset the internal pulse counter. The counter will be clocked with the receive clock RCLK.

Pulse Count Recovery (Read/Write)

Value after RESET: 00_H

	7						0	
PCR	PCR7						PCR0	(37)

PCR7…PCR0… Pulse Count Recovery

A LOS alarm (red alarm) will be cleared if a pulse density is detected in the received bit stream.The number of pulses M which must occur in the predefined PCD time interval is programmable via the PCR register and can be calculated as follows:

M = N+1 ; with 0 =< N =< 255.

The time interval starts with the first detected pulse transition. With every received pulse a counter will be incremented and the actual counter is compared with the contents of PCR register. If the pulse number >= the PCR value the LOS alarm will be reset otherwise the alarm will still be active. In this case the next detected pulse transition will start a new time interval.

Additional Loss of Signal recovery conditions may be selected by register LIM2.LOS2/1.

Line Interface Mode 2 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM2							LOS2	LOS1	(38)

LOS2/1… **Loss of Signal Recovery condition**

00… The LOS alarm will be cleared if the predefined pulse density (register PCR) is detected during the time interval which is defined by register PCD.

01… Additionally to the recovery condition described above a LOS alarm will only be cleared if the pulse density is fulfilled and no more than 15 contigious zeros are detected during the recovery interval. (according to TR-NWT 499).

10… Clearing a LOS alarm will be done if the pulse density is fulfilled and no more than 99 contigious zeros are detected during the recovery interval. (according to TR-NWT 820).

11… Not assigned

Disable Error Counter (Write)

Value after RESET: 00_H

	7							0	
DEC					DCEC	DEBC	DCVC	DFEC	(60)

DCEC… **Disable CRC Error Counter**

Only valid if FMR1.ECM is reset.

This bit has to be set before reading the CRC error counter. It will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of this bit the CRC error counter is latched and then cleared.

DEBC… **Disable Errored Block Counter**

Only valid if FMR1.ECM is reset.

This bit has to be set before reading the errored block counter. It will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of this bit the errored block counter is latched and then cleared.

DCVC… **Disable Code Violation Counter**

Only valid if FMR1.ECM is reset.

This bit has to be set before reading the code violation counter. It will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of this bit the code violation counter is latched and then cleared.

DFEC… **Disable Framing Error Counter**

Only valid if FMR1.ECM is reset.

This bit has to be set before reading the framing error counter. It will be automatically reset if the corresponding error counter high byte has been read. With the rising edge of this bit the framing error counter is latched and then cleared.

Transmit Signaling Register (Write)

Value after RESET: not defined

	7							0	
XS1	A8	A7	A6	A5	A4	A3	A2	A1	(70)
XS2	A16	A15	A14	A13	A12	A11	A10	A9	(71)
XS3	A24	A23	A22	A21	A20	A19	A18	A17	(72)
XS4	B8	B7	B6	B5	B4	B3	B2	B1	(73)
XS5	B16	B15	B14	B13	B12	B11	B10	B9	(74)
XS6	B24	B23	B22	B21	B20	B19	B18	B17	(75)
XS7	A/C8	A7	A6	A5	A4	A3	A2	A/C1	(76)
XS8	A/C16	A15	A14	A13	A12	A11	A10	A/C9	(77)
XS9	A/C24	A23	A22	A21	A20	A19	A18	A/C17	(78)
XS10	B/D8	B7	B6	B5	B4	B3	B2	B/D1	(79)
XS11	B/D16	B15	B14	B13	B12	B11	B10	B/D9	(7A)
XS12	B/D24	B23	B22	B21	B20	B19	B18	B/D17	(7B)

Transmit Signaling Register 1-12

The transmit signaling register access is enabled by setting bit FMR5.EIBR = 1. Each register contains the bit robbing information for 8 DS0 channels. With the transmit CAS empty interrupt ISR1.CASE the contents of these registers will be copied into a shadow register. The contents will subsequently sent out in the corresponding bit positions of the next outgoing multiframe. XS1.0 will be sent out first in channel 1 frame 1 and XS12.7 will be sent out last. In the ESF format the transmit CAS empty interrupt ISR1.CASE requests that these registers should be serviced within the next 3 ms. In F12/F72 format only signaling channel stored in XS1-6 registers will be sent out, registers XS6-12 are ignored. In this framing modes the interrupt ISR1.CASE will be active every 1.5 ms. If requests for new information are ignored, current contents will be repeated.

6.1.2 Status Register Address Arrangement

Address	Write	Type	Comment
00	RFIFO	R	Receive FIFO
4C	FRS0	R	Framer Receive Status 0
4D	FRS1	R	Framer Receive Status 1
4E	FRS2	R	Framer Receive Status 2
4F	FRS3	R	Framer Receive Status 3
50	FECL	R	Framing Error Counter Low
51	FECH	R	Framing Error Counter High
52	CVCL	R	Code Violation Counter Low
53	CVCH	R	Code Violation Counter High
54	CECL	R	CRC Error Counter Low
55	CECH	R	CRC Error Counter High
56	EBCL	R	Errored Block Counter Low
57	EBCH	R	Errored Block Counter High
58			
59			
5A			
5B			
5C	RDL1	R	Receive DL-Bit Register 1
5D	RDL2	R	Receive DL-Bit Register 2
5E	RDL3	R	Receive DL-Bit Register 3
5F			
60			
61			
62	TEST	R	Manufacturer Test Register
63	TEST	R	Manufacturer Test Register
64	SIS	R	Signaling Status Register
65	RSIS	R	Receive Signaling Status Register
66	RBCL	R	Receive Byte Control Low
67	RBCH	R	Receive Byte Control High
68	ISR0	R	Interrupt Status Register 0

T1: Status Register Address Arrangement (cont'd)

Address	Write	Type	Comment
69	ISR1	R	Interrupt Status Register 1
6A	ISR2	R	Interrupt Status Register 2
6B	ISR3	R	Interrupt Status Register 3
6C			
6D			
6E	GIS	R	Global Interrupt Status
6F	VSTR	R	Version Status
70	RS1	R	Receive Signaling Register 1
71	RS2	R	Receive Signaling Register 2
72	RS3	R	Receive Signaling Register 3
73	RS4	R	Receive Signaling Register 4
74	RS5	R	Receive Signaling Register 5
75	RS6	R	Receive Signaling Register 6
76	RS7	R	Receive Signaling Register 7
77	RS8	R	Receive Signaling Register 8
78	RS9	R	Receive Signaling Register 9
79	RS10	R	Receive Signaling Register 10
7A	RS11	R	Receive Signaling Register 11
7B	RS12	R	Receive Signaling Register 12

Receive FIFO (Read) RFIFO

	7							0	
RFIFO	RF7							RF0	(00/01)

Reading data from RFIFO can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface.

The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT1…0 (RFIFO threshold level). It can be reduced from 32 bytes (RESET value) down to 2 bytes (four values: 32, 16, 4, 2 bytes).

Data Transfer

Up to 32 bytes/16 words of received data can be read from the RFIFO following a RPF or a RME interrupt.

RPF Interrupt: A fixed number of bytes/words to be read (32, 16, 4, 2 bytes). The message is not yet complete.

RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers.

RFIFO is released by issuing the “Receive Message Complete” command (RMC).

Framer Receive Status Register 0 (Read)

	7							0	
FRS0	LOS	AIS	LFA	RRA			LMFA	FSRF	(4C)

LOS… Loss of Signal (Red Alarm)

Detection:
This bit is set when the incoming signal has „no transitions“ (analog interface) or logical zeros (dig. interface) in a time interval of T consecutive pulses, where T is programmable via PCD register:
Total account of consecutive pulses: 16 < T < 4096.

Analog interface: The receive signal level where “no transition” will be declared is defined by the programmed value of LIM1.RIL2-0.

Recovery:
Analog interface: The bit will be reset when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL2-0) for at least M pulse periods defined by

register PCR in the PCD time interval.
Digital interface: The bit will be reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval.

With the rising edge of this bit an interrupt status bit (ISR2.LOS) will be set. For additionally recovery conditions refer also to register LIM2.LOS2/1.
The bit will be set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 7 and no alarm condition exists.

AIS… Alarm Indication Signal (Blue Alarm)

This bit is set when the conditions defined by bit FMR4.AIS3 are detected. The flag stays active for at least one multiframe.

With the rising edge of this bit an interrupt status bit (ISR2.AIS) will be set. It will be reset with the beginning of the next following multiframe if no alarm condition is detected.

The bit will be set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 7 and no alarm condition exists.

LFA… Loss of Frame Alignment

The flag is set if pulseframe synchronization has been lost. The conditions are specified via bit FMR4.SSC1/0. Setting this bit will cause an interrupt status (ISR2.LFA).

The flag is cleared when synchronization has been regained. Additionally interrupt status ISR2.FAR is set with clearing this bit.

RRA… Receive Remote Alarm (Yellow Alarm)

The flag is set after detecting remote alarm (yellow alarm). Conditions for setting/resetting are defined by bit RC1.RRAM.

With the rising edge of this bit an interrupt status bit ISR2.RA will be set.

With the falling edge of this bit an interrupt status bit ISR2.RAR will be set.

The bit will be set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 7 and no alarm condition exists.

LMFA… **Loss Of Multiframe Alignment**

Set in F12 or F72 format when 2 out of 4- (or 5 or 6) multiframe alignment patterns are incorrect.

Additionally the interrupt status bit ISR2.LMFA is set.

Cleared after multiframe synchronization has been regained. With the falling edge of this bit an interrupt status bit ISR2.MFAR is generated.

FSRF… **Frame Search Restart Flag**

Toggles when no framing candidate (pulseframing or multiframing) is found and a new frame search is started.

Framer Receive Status Register 1 (Read)

	7							0	
FRS1	EXZD	PDEN		LLBDD	LLBAD		XLS	XLO	(4D)

EXZD… **Excessive Zeros Detected**

Significant only if excessive zeros detection is enabled (FMR2.EXZE=1).

Set after detecting of more than 7 (B8ZS code) or more than 15 (AMI code) contiguous zeros in the received bit stream. This bit is cleared when read.

PDEN… **Pulse Density Violation Detected**

The pulse density of the received data stream is below the requirement defined by ANSI T1. 403 or more than 15 consecutive zeros are detected. With the violation of the pulse density this bit will be set and will remain active until it is read. Reading the register will clear this bit. (Clear on Read).
Additionally an interrupt status ISR0.PDEN is generated with the rising edge of PDEN.

LLBDD… **Line Loop Back Deactuation Signal Detected**

This bit is set to one in case the LLB deactuate signal 001 is detected and then received over a period of more than 33,16 msec with a bit error rate less than 1/100. The bit remains set as long as the bit error rate does not exceed 1/100.

If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.

Any change of this bit will cause a LLBSC interrupt.

LLBAD… Line Loop Back Actuation Signal Detected

This bit is set to one in case the LLB actuate signal 00001 is detected and then received over a period of more than 33,16 msec with a bit error rate less than 1/100. The bit remains set as long as the bit error rate does not exceed 1/100.

If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.

Any change of this bit will cause a LLBSC interrupt.

XLS… Transmit Line Short

Significant only if the ternary line interface is selected by LIM1.DRS=0.

0… Normal operation. No short is detected.

1… The XL1 and XL2 are shortend for at least 32 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high impedance state if bit XPM2.DAXLT is reset. After 32 consecutive pulse periods the outputs XL1/2 are activated again until the first pulse is transmitted. If a short between XL1/2 is still further active the outputs XL1/2 are in high impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit will be reset. With any change of this bit an interrupt ISR1.XLSC will be generated. In case of XPM2.XLT is set this bit will be frozen.

XLO… Transmit Line Open

0… Normal operation

1… This bit will be set if at least 32 consecutive zeros were sent via pins XL1/XL2 resp. XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC will be set. In case of XPM2.XLT is set this bit will be frozen.

Framer Receive Status Register 2 (Read)

	7						0	
FRS2	ESC2	ESC0						(4E)

ESC2…ESC0… Error Simulation Counter

This three-bit counter is incremented by setting bit FMR0.SIM. The state of the counter determines the function to be tested:

For complete checking of the alarm indications, eight simulation steps are necessary (FRS2.ESC = 0 after a complete simulation).

Tested Alarms ESC2…ESC0 =	0	1	2	3	4	5	6	7
LFA			x				x	
LMFA			x				x	
RRA (bit2 =0)		x						
RRA (S-bit fr. 12)			x					
RRA (DL-pattern)							x	
LOS		x	x			x		
EBC (F12,F72)			x				x	
EBC (only ESF)		x	x			x	x	
AIS		x	x			x	x	
FEC			x				x	
CVC (only B8ZS)		x	x			x		
CEC (only ESF)		x	x			x	x	
SLPP		x						
SLPN						x		
XSLP		x	x			x	x	

Some of these alarm indications are simulated only if the FALC54 is configured in the appropriate mode. At simulation steps 0, 3, 4, and 7 pending status flags are reset automatically and clearing of the error counters and interrupt status registers ISR0-3 should be done. Incrementing the simulation counter should not be done at time intervals shorter than 1.5 ms (F4, F12, F72) or 3 ms (ESF). Otherwise, reactions of initiated simulations may occur at later steps.

Framer Receive Status Register 3 (Read)

	7				0	
FRS3			FEH5		FEH0	(4F)

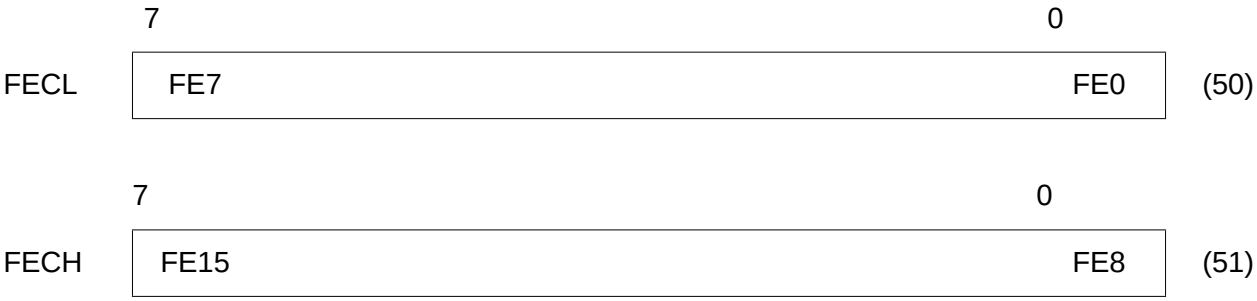
FEH5…FEH0… F-Bit Error History

The bits are set if errors occur in the corresponding framing bit locations. They will be updated once per superframe (ESF format) or every six frames (other framing formats).
Organization:

ESF	Others
FEH5:FAS(24)	FT (6 or 12)
FEH4:FAS(20)	FT (5 or 11)
FEH3:FAS(16)	FT (4 or 10)
FEH2:FAS(12)	FT (3 or 9)
FEH1:FAS(8)	FT (2 or 8)
FEH0:FAS(4)	FT (1 or 7)

Note: All error history bits corresponding to FS bits substituted by data link information are fixed to ‘0’.

Framing Error Counter (READ)



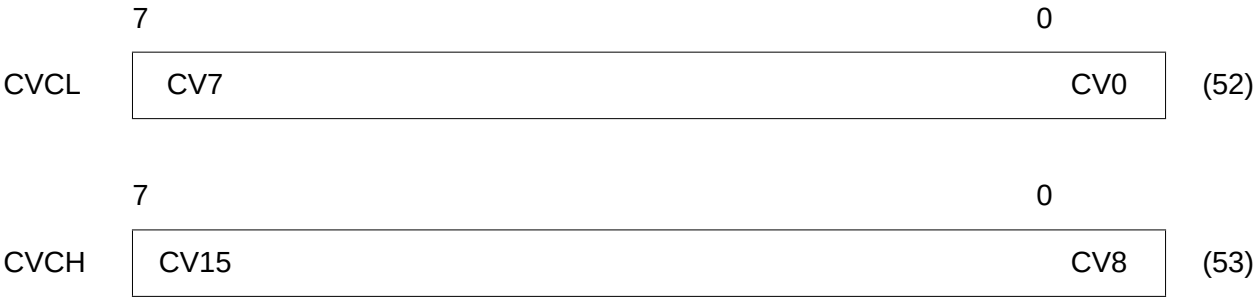
FE15…FE0… **Framing Errors**

This 16-bit counter will be incremented when incorrect FT and FS bits in F4, F12 and F72 format or incorrect FAS bits in ESF format are received.
Framing errors will not be counted during asynchronous state.
Clearing and updating the counter is done according to bit FMR1.ECM.
During alarm simulation, the counter will be incremented twice.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DFEC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Code Violation Counter (READ)



CV15…CV0… **Code Violations**

No function if NRZ Code has been enabled.

If the B8ZS code (bit FMR0.RC1/0 = 11) is selected, the 16-bit counter will be incremented by detecting violations which are not due to zero substitution. If FMR2.EXZE is set, additionally excessive zero strings (more than 7 contiguous zeros) are detected and counted.

If simple AMI coding is enabled (FMR0.RC0/1 = 10) all bipolar violations are counted. If FMR2.EXZE is set, additionally excessive zero strings (more than 15 contiguous zeros) are detected and counted.

During alarm simulation, the counter is incremented continuously with every second received bit.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCVC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter (READ)

	7							0	
CECL	CR7							CR0	(54)

	7							0	
CECH	CR15							CR8	(55)

CR15…CR0… **CRC Errors**

No function if CRC6 procedure or ESF format are disabled.

In ESF mode, the 16-bit counter will be incremented when a multiframe has been received with a CRC error. CRC errors will not be counted during asynchronous state.
Clearing and updating the counter is done according to bit FMR1.ECM.
During alarm simulation, the counter is incremented once per multiframe.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DCEC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Errored Block Counter (READ)

	7							0	
EBCL	EBC7							EBC0	(56)

	7							0	
EBCH	EBC15							EBC8	(57)

EBC15…EBC0… Errored Block Counter

In ESF format this 16-bit counter will be incremented once per multiframe if a multiframe has been received with a CRC error or an errored frame alignment has been detected. CRC and framing errors will not be counted during asynchronous state.

In F4/12/72 format an errored block contain 4/12 or 72 frames. Incrementing is done once per multiframe if framing errors has been detected.
Clearing and updating the counter is done according to bit FMR1.ECM.

During alarm simulation, the counter is incremented in ESF format once per multiframe and in F4/12/72 format only one time.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer will be stopped and the error counter will be reset. Bit DEC.DEBC will automatically be reset with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter will be latched and then automatically reset. The latched error counter state should be read within the next second.

Receive DL-Bit Register 1 (Read)

	7							0	
RDL1	RDL17	RDL16	RDL15	RDL14	RDL13	RDL12	RDL11	RDL10	(5C)

RDL17…RDL10…Receive DL-Bit

Only valid if F12, F24 or F72 format is enabled.
The received FS/DL-Bits are shifted into this register. RDL10 is received in frame 1 and RDL17 in frame 15, if F24 format is enabled. RDL10 is received in frame 26 and RDL17 in frame 40, if F72 format is enabled.
In F12 format the FS-Bits of a complete multiframe is stored in this register. RDL10 is received in frame 2 and RDL15 in frame 12.
This register will be updated with every receive multiframe begin interrupt ISR0.RMB.

Receive DL-Bit Register 2 (Read)

	7							0	
RDL2	RDL27	RDL26	RDL25	RDL24	RDL23	RDL22	RDL21	RDL20	(5D)

RDL27…RDL20…Receive DL-Bit

Only valid if F24 or F72 format is enabled.
The received DL-Bits are shifted into this register. RDL20 is received in frame 17 and RDL23 in frame 23, if F24 format is enabled. RDL20 is received in frame 42 and RDL27 in frame 56, if F72 format is enabled.
This register will be updated with every receive multiframe begin interrupt ISR0.RMB.

Receive DL-Bit Register 3 (Read)

	7							0	
RDL3	RDL37							RDL30	(5E)

RDL37…RDL30…Receive DL-Bit

Only valid if F72 format is enabled.
The received DL-Bits are shifted into this register. RDL30 is received in frame 58 and RDL37 in frame 72, if F72 format is enabled.
This register will be updated with every receive multiframe begin interrupt ISR0.RMB.

Signaling Status Register (Read)

	7							0	
SIS	XDOV	XFW	XREP		RLI	CEC		BOM	(64)

XDOV… **Transmit Data Overflow**

More than 32 bytes have been written to the XFIFO.
This bit is reset by:

– a transmitter reset command XRES or

– when all bytes in the accessible half of the XFIFO have been moved in the inaccessible half.

XFW… **Transmit FIFO Write Enable**

Data can be written to the XFIFO.

XREP… **Transmission Repeat**

Status indication of CMDR.XREP.

RLI… **Receive Line Inactive**

Neither FLAGs as Interframe Time Fill nor frames are received via the signaling timeslot.

CEC… **Command Executing**

0… No command is currently executed, the CMDR register can be written to.

1… A command (written previously to CMDR) is currently executed, no further command can be temporarily written in CMDR register.

Note: CEC will be active at most 5 SCLKX clock cycles if FMR1.IMOD=0 and 10 SCLKX cycles if FMR1.IMOD is set.

BOM… **Bit Oriented Message**

Significant only in ESF frame format and auto switching mode is enabled.

0… HDLC mode

1… BOM mode

Receive Signaling Status Register (Read)

	7							0	
RSIS	VFR	RDO	CRC16	RAB	HA1	HA0	HFR	LA	(65)

RSIS relates to the last received HDLC or BOM frame; it is copied into RFIFO when end-of-frame is recognized (last byte of each stored frame).

VFR… **Valid Frame**

Determines whether a valid frame has been received.

1… valid

0… invalid

An invalid frame is either

– a frame which is not an integer number of 8 bits (n × 8 bits) in length (e.g. 25 bits), or

– a frame which is too short taking into account the operation mode selected via MODE (MDS2-0) and the selection of receive CRC ON/OFF (CCR3.RCRC) as follows:

- MDS2-0 = 011 (16 bit Address),
  RCRC = 0 : 4 bytes; RCRC = 1 : 3-4 bytes
- MDS2-0 = 010 (8 bit Address),
  RCRC = 0 : 3 bytes; RCRC = 1 : 2-3 bytes

Note: Shorter frames are not reported.

RDO… **Receive Data Overflow**

A data overflow has occurred during reception of the frame.

Additionally, an interrupt can be generated
(refer to ISR1.RDO/IMR1.RDO).

CRC16… **CRC16 Compare/Check**

0… CRC check failed; received frame contains errors.

1… CRC check o.k.; received frame is error-free.

RAB… **Receive Message Aborted**

The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.

HA1, HA0… **High Byte Address Compare**

Significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the FALC54 compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (broadcast address).

Dependent on the result of this comparison, the following bit combinations are possible:

00… RAH2 has been recognized

01… Broadcast address has been recognized

10… RAH1 has been recognized C/R = 0(bit 1)

11… RAH1 has been recognized C/R = 1 (bit 1)

Note: If RAH1, RAH2 contain identical values, a match is indicated by '10'or '11'.

HFR … **HDLC Frame Format**

0… A BOM frame was received.

1… A HDLC frame was received.

Note: RSIS 7-2, 0 is not valid with a BOM frame.

LA … **Low Byte Address Compare**

Significant in HDLC modes only.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two registers. (RAL1, RAL2).

0… RAL2 has been recognized
1… RAL1 has been recognized

Receive Byte Count Low (Read)

	7		0	
RBCL	RBC7		RBC0	(66)

Together with RBCH (bits RBC11 - RBC8), indicates the length of a received frame (1…4095 bytes). Bits RBC4-0 indicate the number of valid bytes currently in RFIFO. These registers must be read by the CPU following a RME interrupt.

Received Byte Count High (Read)

Value after RESET: 000_{xxxxx}

	7					0	
RBCH				OV	RBC11	RBC8	(67)

OV… **Counter Overflow**

More than 4095 bytes received.

RBC11 – RBC8… **Receive Byte Count (most significant bits)**

Together with RBCL (bits RBC7… RBC0) indicate the length of the received frame.

Interrupt Status Register 0 (Read)

Value after RESET: 00_H

	7							0	
ISR0	RME	RFS	ISF	RMB	RSC	CRC6	PDEN	RPF	(68)

All bits are reset when ISR0 is read.

If bit IPC.VIS is set to ‘1’, interrupt statuses in ISR0 may be flagged although they are masked via register IMR0. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

RME… **Receive Message End**

One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte.

The complete message length can be determined reading the RBCH, RBCL registers, the number of bytes currently stored in RFIFO is given by RBC4-0. Additional information is available in the RSIS register.

RFS… **Receive Frame Start**

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After a RFS interrupt, the contents of

- RAL1
- RSIS - bits 3-1

are valid and can be read by the CPU.

ISF… **Incorrect Sync Format**

The FALC54 could not detect eight consecutive one's within 32 bits in BOM mode. Only valid if BOM receiver has been activated.

RMB… **Receive Multiframe Begin**

This bit is set with the beginning of a received multiframe of the receive line timing.

RSC… **Received Signaling Information Changed**

This bit is set with the updating of a received signaling information in registers RS1-6 resp. RS1-12. If the last received signaling information changed from the previous received updating is started. This interrupt will only occur in the synchronous state. The registers RS1-6 /12 should be read within the next 1.5 / 3 ms otherwise the contents may be lost.

CRC6… **Receive CRC6 Error**

0… No CRC6 error occurs.

1… The CRC6 check of the last received multiframe failed.

PDEN… **Pulse Density violation**

The pulse density violation of the received data stream defined by ANSI T1. 403 is violated. More than 15 consectuive zeros or less than N ones in each and every time window of 8(N+1) data bits (N=23) are detected. If IPC.SCI is set high this interrupt status bit will be activated with every change of state of FRS1.PDEN.

RPF… **Receive Pool Full**

32 bytes of a frame have arrived in the receive FIFO. The frame is not yet completely received.

Interrupt Status Register 1 (Read)

	7							0	
ISR1	CASE	RDO	ALLS	XDU	XMB		XLSC	XPR	(69)

All bits are reset when ISR1 is read.

If bit IPC.VIS is set to ‘1’, interrupt statuses in ISR1 may be flagged although they are masked via register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

CASE… **Transmit CAS Register Empty**

In ESF and F12 format this bit is set with the beginning of a transmitted multiframe related to the internal transmitter timing. In F72 format this interrupt will occur every 12 frames to inform the user that new bit robbing data has to written to XS1-6 registers. In ESF format this interrupt will occur every 24 frames to write registers XS1-12.

RDO… **Receive Data Overflow**

This interrupt status indicates that the CPU does not respond quickly enough to an RPF or RME interrupt and that data in RFIFO has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO is available again.

Note: Whereas the bit RSIS.RDO in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO, the ISR1.RDO interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.

ALLS… **All Sent**

This bit is set if the last bit of the current frame is completely sent out and XFIFO is empty.

XDU… **Transmit Data Underrun**

Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME was issued.

Note: Transmitter and XFIFO are reset and deactivated if this condition occurs. They are re-activated not before this interrupt status register has been read. Thus, XDU should not be masked via register IMR1.

XMB… **Transmit Multiframe Begin**

This bit is set with the beginning of a transmitted multiframe related to the internal transmitter timing.

XLSC… **Transmit Line Status Change**

XLSC is set to one with the rising edge of the bit FRS1.XLO or with any change of bit FRS1.XLS.

The actual status of the transmit line monitor can be read from the FRS1.XLS and FRS1.XLO.

XPR… **Transmit Pool Ready**

A data block of up to 32 bytes can be written to the transmit FIFO. XPR enables the fastest access to XFIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.

Interrupt Status Register 2 (Read)

	7							0	
ISR2	FAR	LFA	MFAR	LMFA	AIS	LOS	RAR	RA	(6A)

All bits are reset when ISR2 is read.

If bit IPC.VIS is set to ‘1’, interrupt statuses in ISR2 may be flagged although they are masked via register IMR2. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

FAR… **Frame Alignment Recovery**

The framer has reached synchronization. Set with the falling edge of bit FSR0.LFA.

It is set also after alarm simulation is finished and the receiver is still synchron.

LFA… **Loss of Frame Alignment**

The framer has lost synchronization and bit FRS0.LFA is set.
It will be set during alarm simulation.

MFAR… **Multiframe Alignment Recovery**

Set when the framer has reached multiframe alignment in F12 or F72 format. With the negative transition of bit FRS0.LMFA this bit will be set. It will be set during alarm simulation.

LMFA… **Loss of Multiframe Alignment**

Set when the framer has lost the multiframe alignment in F12 or F72 format. With the positive transition of bit FRS0.LMFA this bit will be set. It will be set during alarm simulation.

AIS… **Alarm Indication Signal (Blue Alarm)**

This bit is set when an alarm indication signal is detected and bit FRS0.AIS is set. If IPC.SCI is set high this interrupt status bit will be activated with every change of state of FRS0.AIS.
It will be set during alarm simulation.

LOS… **Loss of Signal (Red Alarm)**

This bit is set when a loss of signal alarm is detected in the received data stream and FRS0.LOS is set. If IPC.SCI is set high this interrupt status bit will be activated with every change of state of FRS0.LOS.
It will be set during alarm simulation.

RAR… **Remote Alarm Recovery**

Set if a remote alarm (yellow alarm) is cleared and bit FRS0.RRA is reset. It is set also after alarm simulation is finished and no remote alarm is detected.

RA… **Remote Alarm**

A remote alarm (yellow alarm) is detected. Set with the rising edge of bit FRS0.RRA. It will be set during alarm simulation.

Interrupt Status Register 3 (Read)

	7							0	
ISR3	ES	SEC	XSLP		LLBSC		SLN	SLP	(6B)

All bits are reset when ISR3 is read.

If bit IPC.VIS is set to ‘1’, interrupt statuses in ISR3 may be flagged although they are masked via register IMR3. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

ES… **Errored Second**

This bit is set if at least one enabled interrupt source via IMR4 is set during the time interval of one second. Interrupt sources of IMR4 register:

LFA = Loss of frame alignment detected
FER = Framing error received
CER = CRC error received
AIS = Alarm indication signal (blue alarm)
LOS = Loss of signal (red alarm)
CVE = Code violation detected
SLIP= Transmit Slip or Receive Slip positive/negative detected

SEC… **Second**

The internal one second timer has expired. The timer is derived from the internal 16 MHz clock.

XSLP… **Transmit Slip Indication**

A one in this bit position indicates that there is an error in the host clock system. If the wander of the transmit route clock, which normally is phase locked to a common submultiple of the system clock (SCLKX), is too great, data transmission errors will occur. In that case, the transmit speech memory has to be reset to its start position by writing the initial value to the transmit time-slot counter XC1.XTO.

LLBSC… **Line Loop Back Status Change**

This bit is set to one, if the LLB actuate signal 00001 or the LLB deactuate signal 001, resp., is detected over a period of 33,16 msec with a bit error rate less than 1/100.

The LLBSC bit is also set to one, if the current detection status is left, i.e., if the bit error rate exceeds 1/100.

The actual detection status can be read from the FRS1.LLBAD and FRS1.LLBDD, resp.

SLN… **Slip Negative**

The frequency of the receive route clock is greater than the frequency of SCLKR. A frame will be skipped. It will be set during alarm simulation.

SLP… **Slip Positive**

The frequency of the receive route clock is less than the frequency of SCLKR. A frame will be repeated. It will be set during alarm simulation.

Global Interrupt Status Register (Read)

Value after RESET: 00_H

	7							0	
GIS					ISR3	ISR2	ISR1	ISR0	(6E)

This status register points to pending interrupts (ISR3…ISR0)

Version Status Register (Read)

	7					0	
VSTR					VN3	VN0	(6F)

VN3 – VN0… Version Number of Chip

0… Version 1.1 - 1.2

1… Version 1.3

Receive Signaling Register (Read)

Value after RESET: not defined

	7							0	
RS1	A8	A7	A6	A5	A4	A3	A2	A1	(70)
RS2	A16	A15	A14	A13	A12	A11	A10	A9	(71)
RS3	A24	A23	A22	A21	A20	A19	A18	A17	(72)
RS4	B8	B7	B6	B5	B4	B3	B2	B1	(73)
RS5	B16	B15	B14	B13	B12	B11	B10	B9	(74)
RS6	B24	B23	B22	B21	B20	B19	B18	B17	(75)
RS7	A/C8	A7	A6	A5	A4	A3	A2	A/C1	(76)
RS8	A/C16	A15	A14	A13	A12	A11	A10	A/C9	(77)
RS9	A/C24	A23	A22	A21	A20	A19	A18	A/C17	(78)
RS10	B/D8	B7	B6	B5	B4	B3	B2	B/D1	(79)
RS11	B/D16	B15	B14	B13	B12	B11	B10	B/D9	(7A)
RS12	B/D24	B23	B22	B21	B20	B19	B18	B/D17	(7B)

Receive Signaling Register 1-12

Each register contains the received bit robbing information for 8 DS0 channels. The received robbed bit signaling information of a complete ESF multiframe will be compared with the previously received one. In F12/72 frame format the received signaling information of every 12 frames will be compared with the previously received 12 frames. If the contents changed a Receive Signaling Changed interrupt ISR0.RSC is generated and informs the user that a new multiframe has to be read within the next 3 ms (ESF) or 1.5 ms (F12/72). Received data will be stored in RS1-12 (ESF) and in RS1-6 (F12/72) registers. RS1.0 is received in channel 1 frame 1 and RS12.7 in channel 24 frame 24 (ESF).

If requests for reading the RS1-12 registers will be ignored the received data may be lost.

7 Electrical Specification

7.1 Absolute Maximum Ratings

Supply voltage	V_{DD}	= – 0.3 to + 7.0 V
Input voltage	V_I	= – 0.3 to V_{DD} + 0.3 V (max. 7 V)
Output voltage	V_0	= – 0.3 to V_{DD} + 0.3 V (max. 7 V)
Storage temperature	T_{stg}	= – 65 to + 150 °C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may affect device reliability.
This is a stress rating only and functional operation of the device under these conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied.

7.2 DC Characteristics

T_A = – 40 to 85 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition	Pins
		min.	max.			
Input low voltage	V_{IL}	– 0.4	0.8	V		All pins except analog pins: RLx, XLx XTALx, XLxM, REFR, TMS, TDI
Input high voltage	V_{IH}	2.0	V_{DD} + 0.4	V		
Output low voltage	V_{OL}		0.45	V	I_{OL} = 2 mA	
Output high voltage Output high voltage	V_{OH} V_{OH}	2.4 V_{DD} – 0.5		V	I_{OH} = – 400 µA I_{OH} = – 100 µA	
Input leakage current Output leakage current	I_{LI} I_{LO}		1	µA µA	$V_{IN} < V_{DD}$ to 0 V 0 V < $V_{OUT} < V_{DD}$ to 0 V	
Input leakage current	I_{TMSLI}		1 250	µA µA	$V_{IN} = V_{DD}$ V_{IN} = 0 V	TMS, TDI
Input low voltage	V_{XTALIL}	– 0.4	1.0	V		XTAL1, XTAL2, XTAL3, XTAL4
Input high voltage	V_{XTALIH}	4.0	V_{DD} + 0.4	V		
Input leakage current	I_{XTALI}		15	µA	0 V ≤ V_{IN} ≤ V_{DD} to 0 V	
Transmitter output impedance	R_X		0.3	Ω	[3] XPM2.XLT=0	XL1, XL2
	R_X	6000		Ω	[3]XPM2.XLT=1	
Transmitter output current	I_{XE1} I_{XT1}		60 75	mA mA	note 1) note 2) depending on line length	

[1] Wiring conditions and external circuit configuration according to figure 15; values of registers XPM2-0 = BD_H, 03_H, 00_H.

[2] Wiring conditions and external circuit configuration according to figure 47; values of registers XPM2-0 = $9F_H$, 27_H, 02_H.

[3] Not tested in production.

7.2 DC Characteristics (cont'd)

T_A = – 40 to 85 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Peak voltage of a mark (CEPT) Peak voltage of a mark (T1)	V_{XCEPT} V_{XT1}	2.9 3.1	3.5 3.7	V V	wired according to figure 15 wired according to figure 47 depending on line length;	XL1, XL2
Receiver input peak voltage of a mark	V_R	0.5	4.4	V		
Receive input impedance		50		kΩ	Note 3)	
Receiver input threshold	V_{RTH}	45		%	Note 3)	
Loss of signal threshold (differential input voltage between pins RL1/RL2)	V_{LOS}	1.36 1.04 0.84 0.62 0.43 0.32 0.22 not assigned		V	RIL2-0 = 000 RIL2-0 = 001 RIL2-0 = 010 RIL2-0 = 011 RIL2-0 = 100 RIL2-0 = 101 RIL2-0 = 110 RIL2-0 = 111 depends on programming of register LIM1.RIL2-0 (typical values)	RL1, RL2
Operational power supply current	I_{CC}		140 140	mA mA	E1 application[1], T1 application[2], max value for all ones	

[1] Wiring conditions and external circuit configuration according to figure 15; values of registers XPM2-0 = BD_H, 03_H, 00_H.

[2] Wiring conditions and external circuit configuration according to figure 47; values of registers XPM2-0 = $9F_H$, 27_H, 02_H.

[3] Not tested in production.

7.3 Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Pins
		typ.	max.		
Input capacitance[1)]	C_{IN}	5	10	pF	all except XLxM, XTALx, REFR
Output capacitance[1)]	C_{OUT}	8	15	pF	all except XLx, XTALx
Output capacitance[1)]	C_{OUT}	8	20	pF	XLx

[1)] Not tested in production.

7.4 Recommended Oscillator Circuits

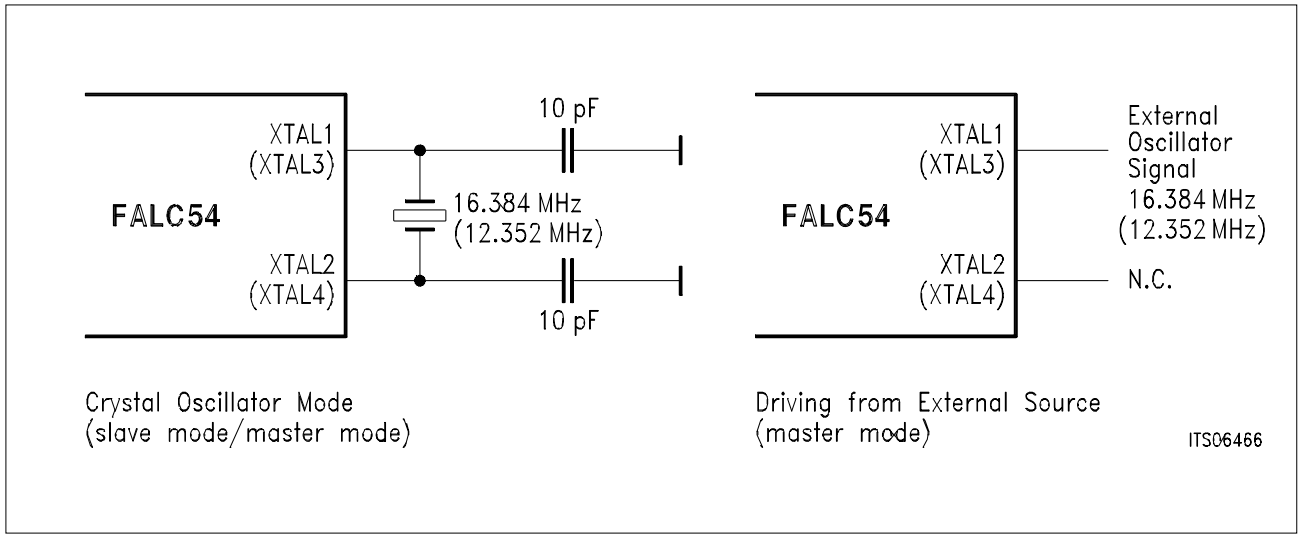


Figure 67
Oscillator Circuits

The jitter attenuator requires unique performance specifications for the crystals.

The following typical crystal parameters will meet this specifications:

– Motional capacitance C_1 = 25 fF min

– Shunt capacitance C_0 = 7 pF max

– Load capacitance C_L = 15 pF typ

– Resonance resistance $R_r \leq 20\ \Omega$

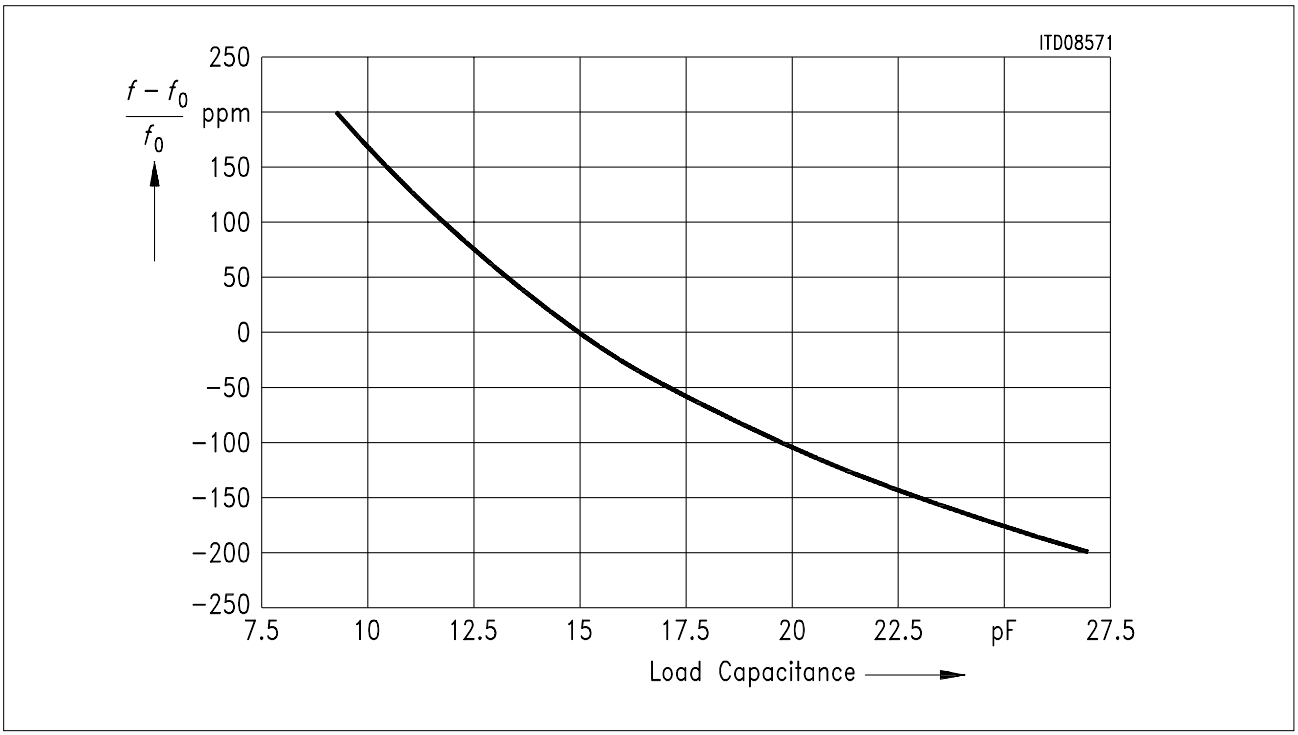


Figure 68
DCO1 Tuning Range (16.384 MHz Crystal)
Crystal specified for C_L = 15 pF)

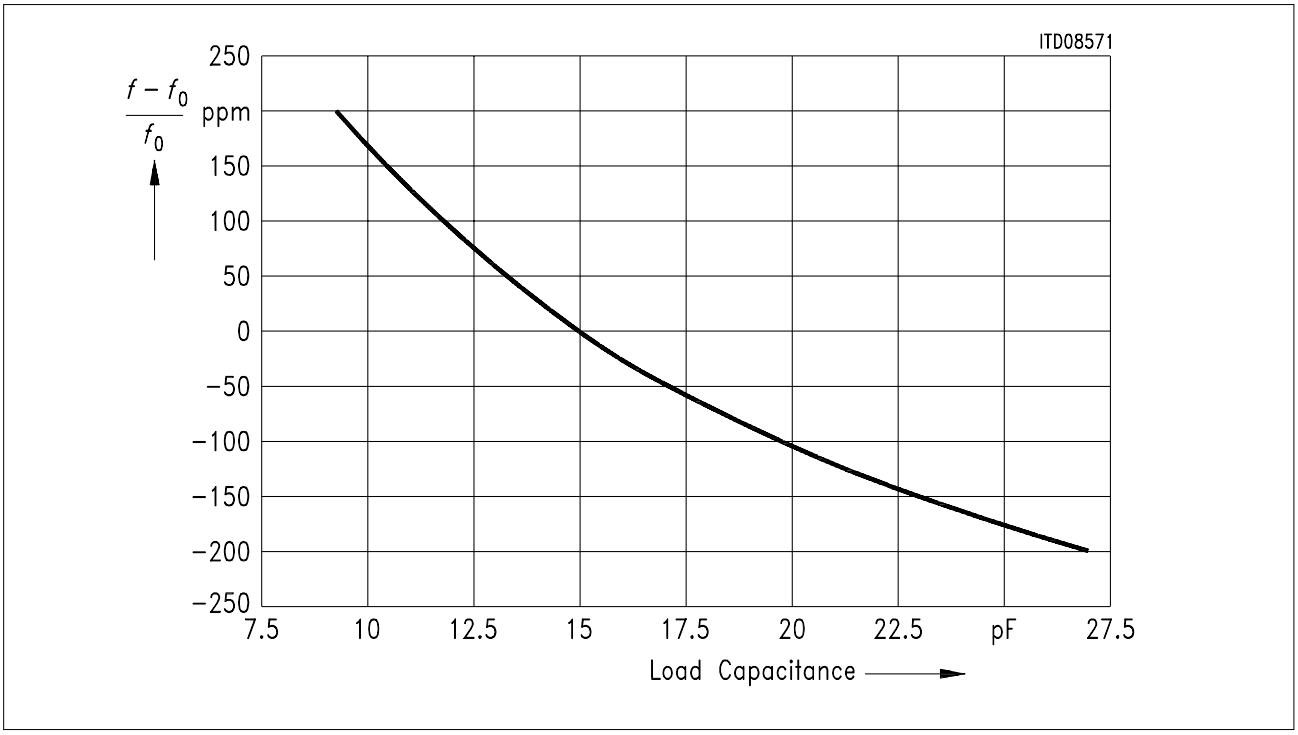


Figure 69
DCO2 Tuning Range (12.352 MHz Crystal)
Crystal specified for C_L = 15 pF

7.5 AC Characteristics

T_A = – 40 to 85 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

All inputs except RLx, XLxM, XTAL1/3 are driven to V_{IH} = 2.4 V for a logical “1”
and to V_{IL} = 0.4 V for a logical “0”

Timing measurements except for XLx are made at V_H = 2.0 V for a logical “1”
and at V_L = 0.8 V for a logical “0”

The AC testing input/output waveforms are shown below.

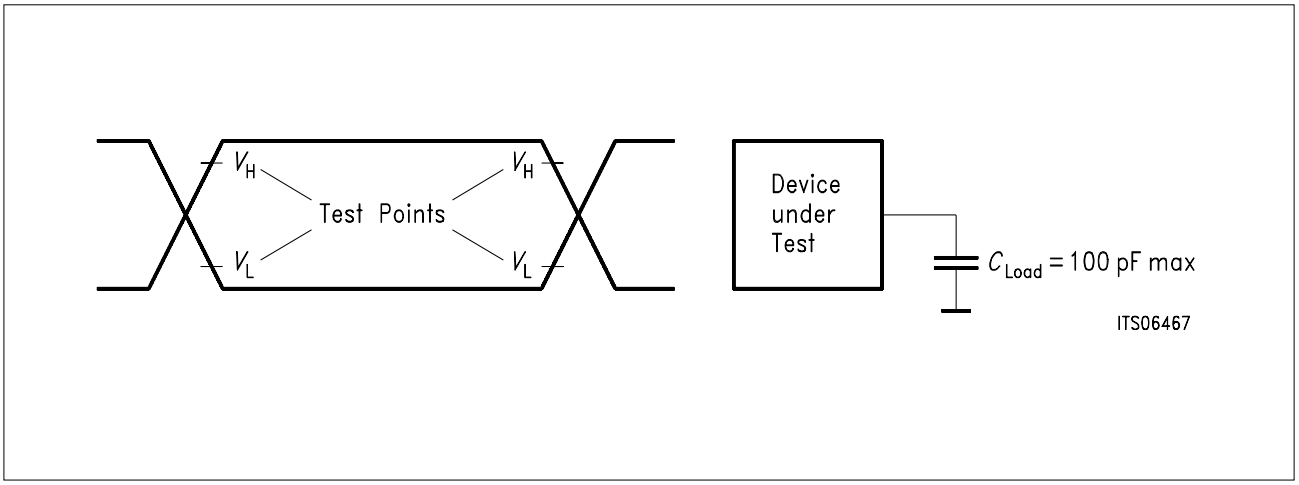


Figure 70
Input/Output Waveform for AC Tests

7.5.1 Microprocessor Interface

7.5.1.1 Siemens/Intel Bus Interface Mode

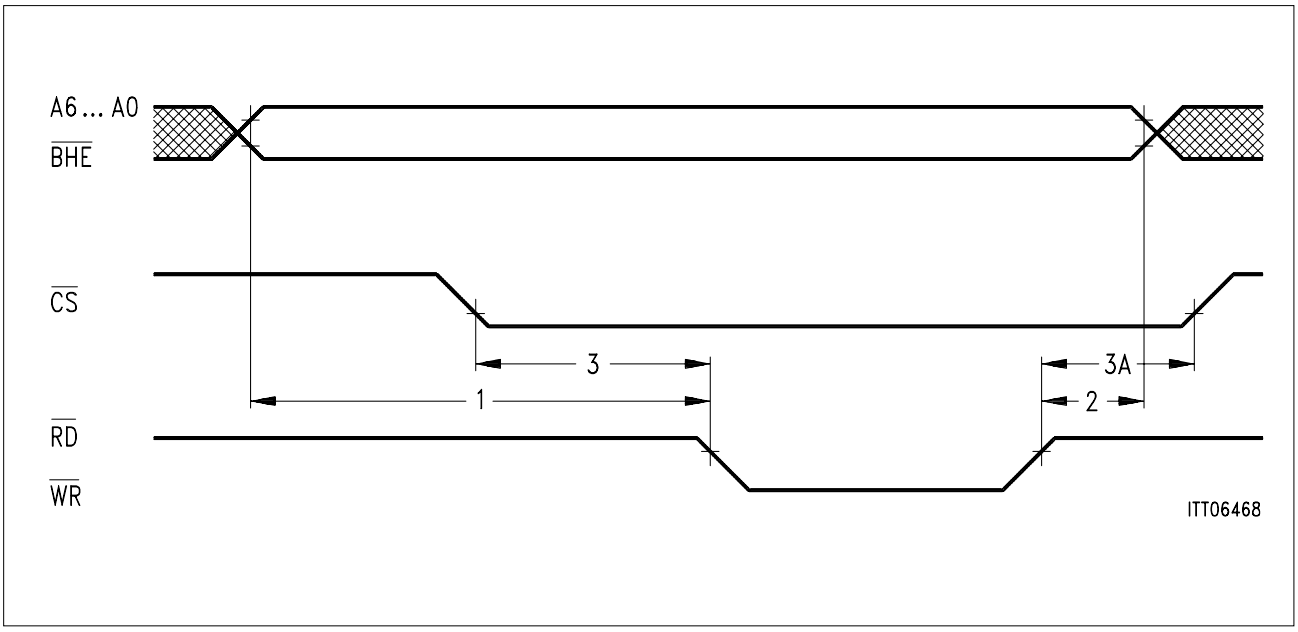


Figure 71
Siemens/Intel Non-Multiplexed Address Timing

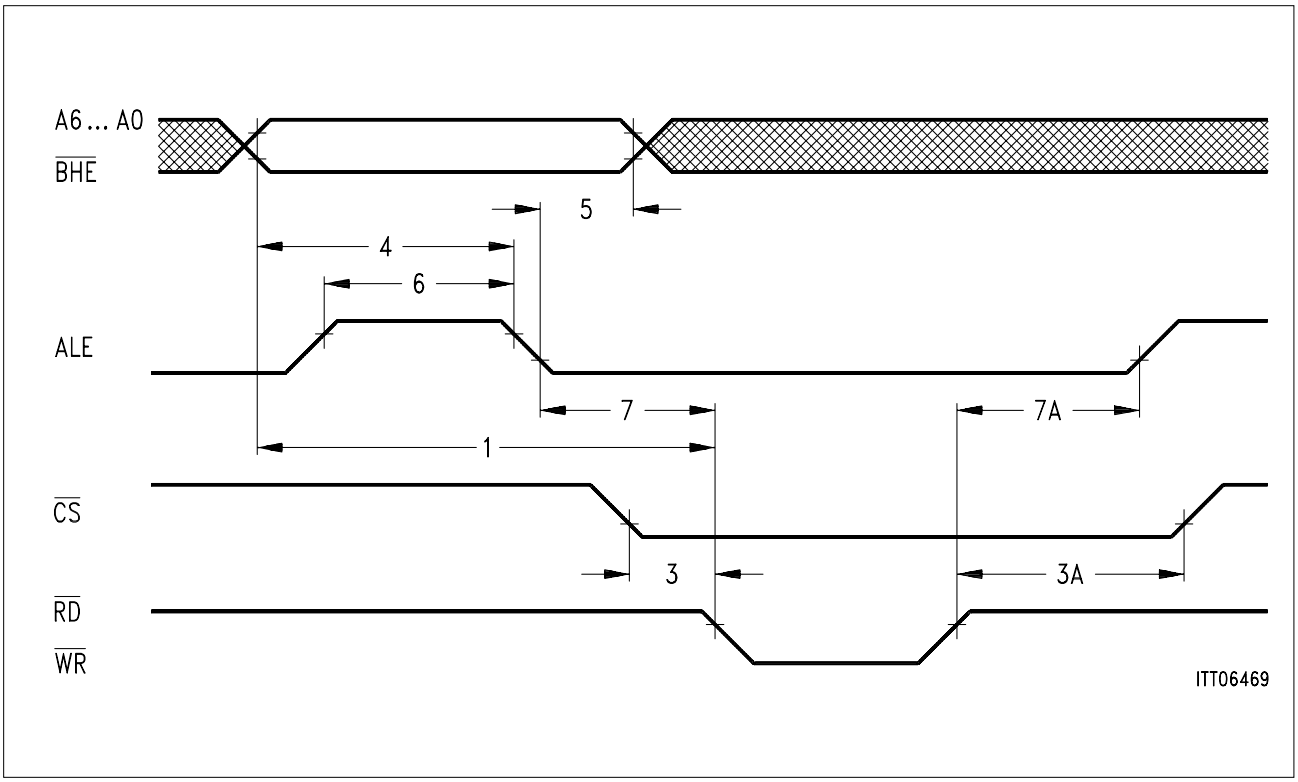


Figure 72
Siemens/Intel Multiplexed Address Timing

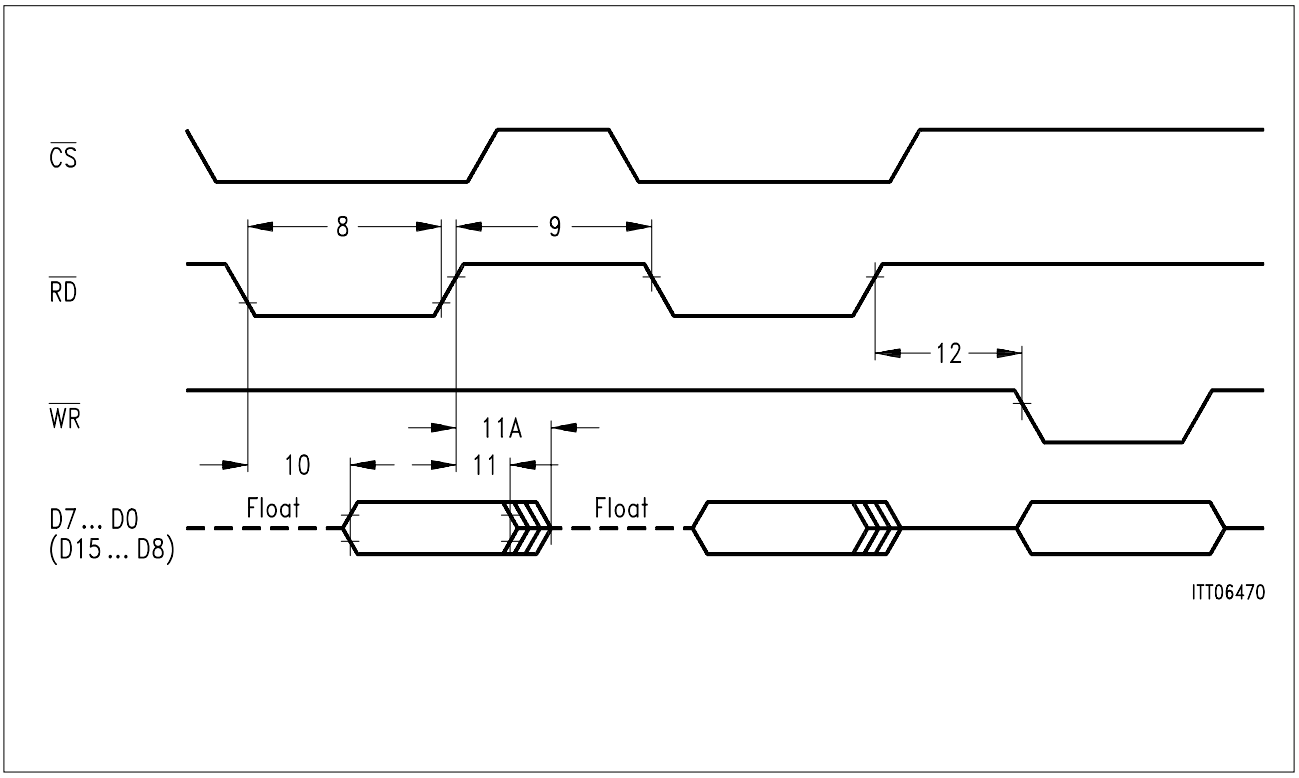


Figure 73
Siemens/Intel Read Cycle Timing

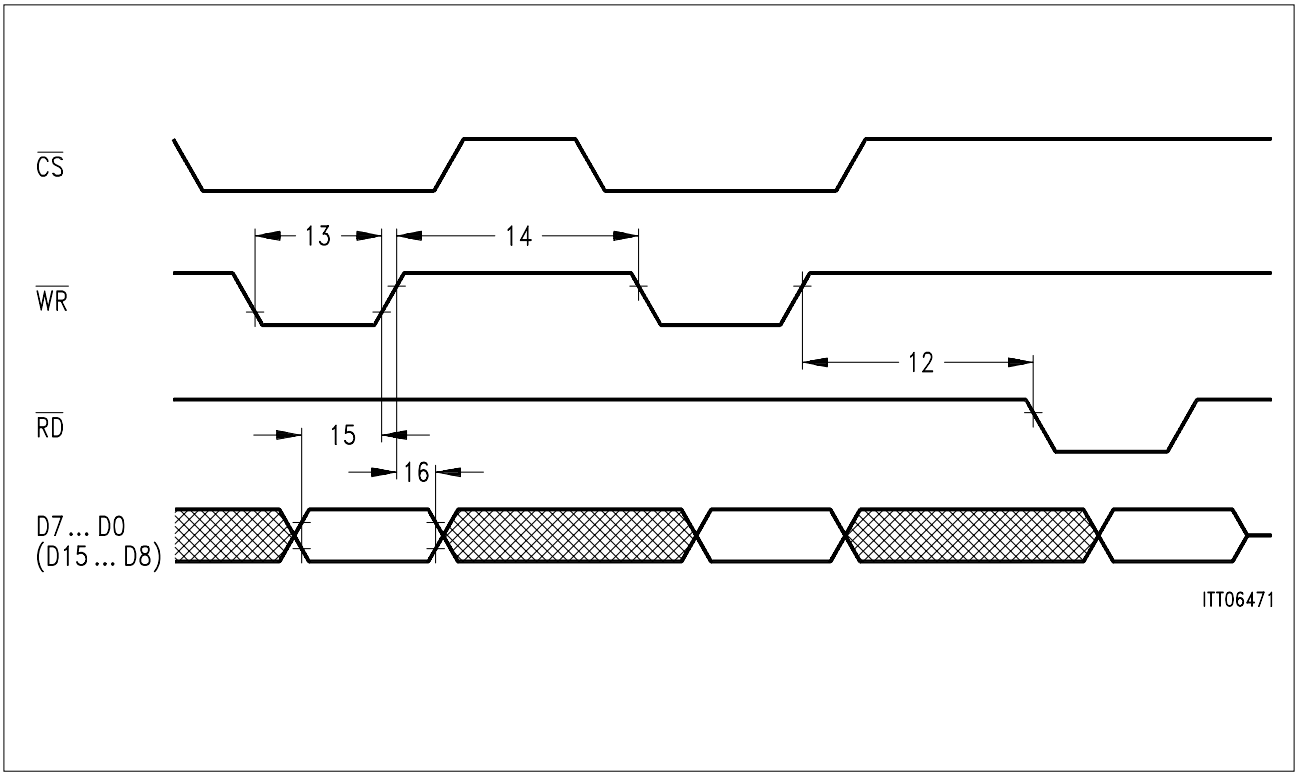


Figure 74
Siemens/Intel Write Cycle Timing

Siemens/Intel Bus Interface and Interrupt Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
1	Address, $\overline{BHE}$ setup time	15		ns
2	Address, $\overline{BHE}$ hold time	0		ns
3	$\overline{CS}$ setup time	0		ns
3A	$\overline{CS}$ hold time	0		ns
4	Address, $\overline{BHE}$ stable before ALE inactive	20		ns
5	Address, $\overline{BHE}$ hold after ALE inactive	10		ns
6	ALE pulse width	30		ns
7	Address latch setup time before cmd active	0		ns
7A	ALE to command inactive delay	30		ns
8	$\overline{RD}$ pulse width	100		ns
9	$\overline{RD}$ control interval	80		ns
10	Data valid after $\overline{RD}$ active		95	ns
11	Data hold after $\overline{RD}$ inactive	10		ns
11A	$\overline{RD}$ inactive to data bus tristate[1)]		50	ns
12	$\overline{WR}$ to $\overline{RD}$ or $\overline{RD}$ to $\overline{WR}$ control interval	80		ns
13	$\overline{WR}$ pulse width	60		ns
14	$\overline{WR}$ control interval	50		ns
15	Data stable before $\overline{WR}$ inactive	30		ns
16	Data hold after $\overline{WR}$ inactive	10		ns

[1)] Not tested in production.

7.5.1.2 Motorola Bus Interface Mode

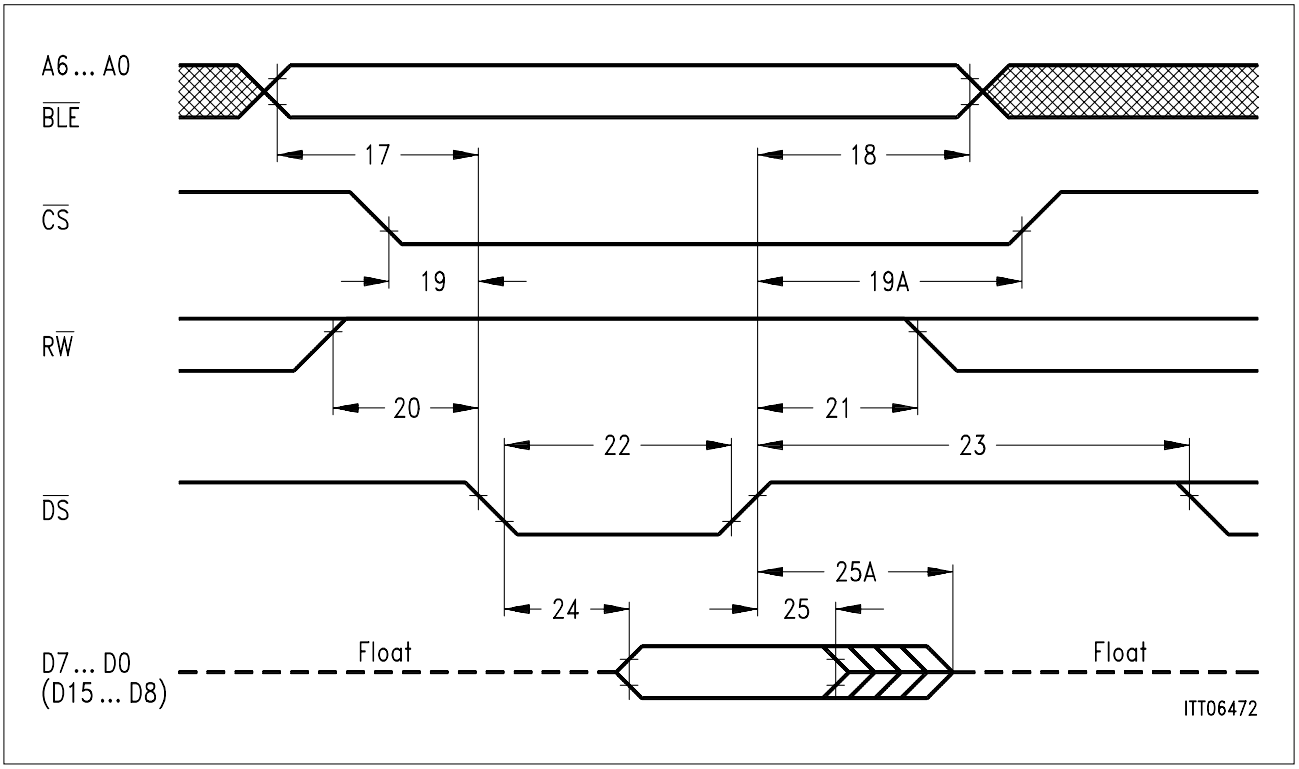


Figure 75
Motorola Read Cycle Timing

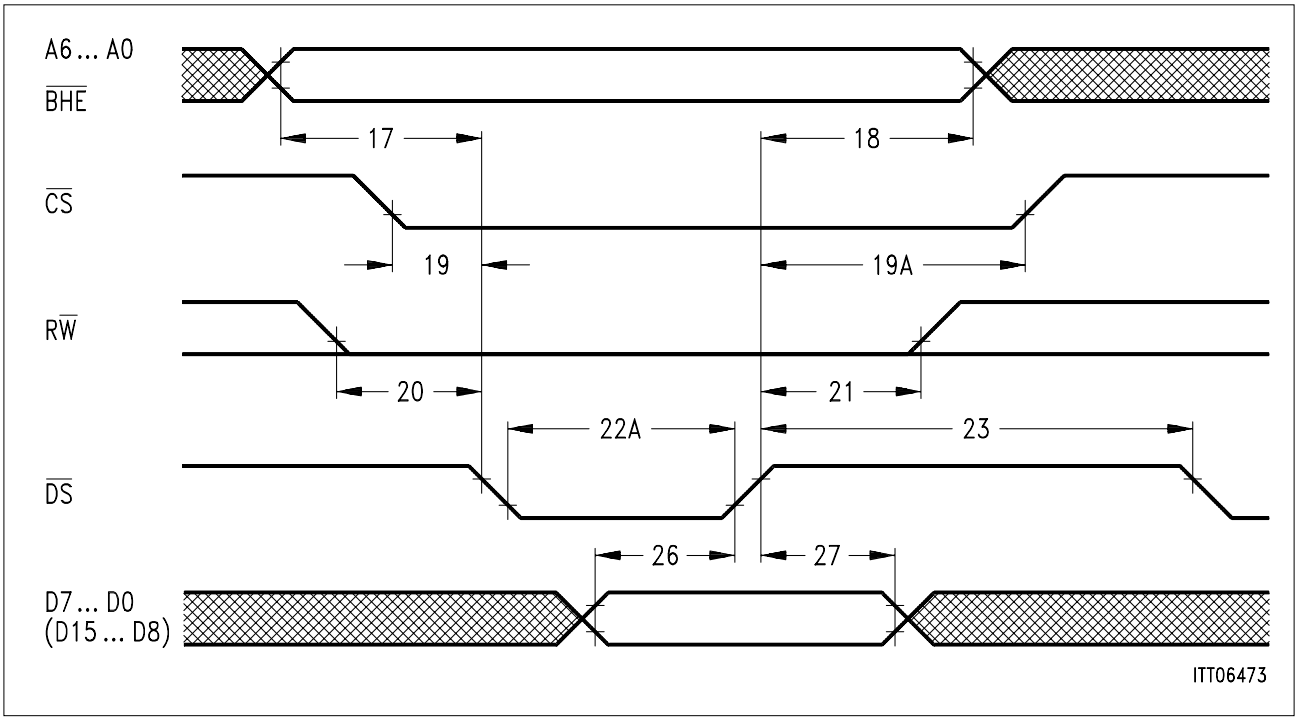


Figure 76
Motorola Write Cycle Timing

Motorola Bus Interface Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
17	Address, $\overline{BLE}$, setup time before $\overline{DS}$ active	15		ns
18	Address, $\overline{BLE}$, hold after $\overline{DS}$ inactive	0		ns
19	$\overline{CS}$ active before $\overline{DS}$ active	0		ns
19A	$\overline{CS}$ hold after $\overline{DS}$ inactive	0		ns
20	R$\overline{W}$ stable before $\overline{DS}$ active	10		ns
21	R$\overline{W}$ hold after $\overline{DS}$ inactive	0		ns
22 22A	$\overline{DS}$ pulse width (read access) (write access)	100 60		ns ns
23	$\overline{DS}$ control interval	80		ns
24	Data valid after $\overline{DS}$ active (read access)		95	ns
25	Data hold after $\overline{DS}$ inactive (read access)	10		ns
25A	$\overline{DS}$ inactive to databus tristate (read access)[1)]		40	ns
26	Data stable before $\overline{DS}$ active (write access)	30		ns
27	Data hold after $\overline{DS}$ inactive (write access)	10		ns

[1)] Not tested in production.

7.6 Line Interface

7.6.1 Timing of Dual Rail and Optical Interface

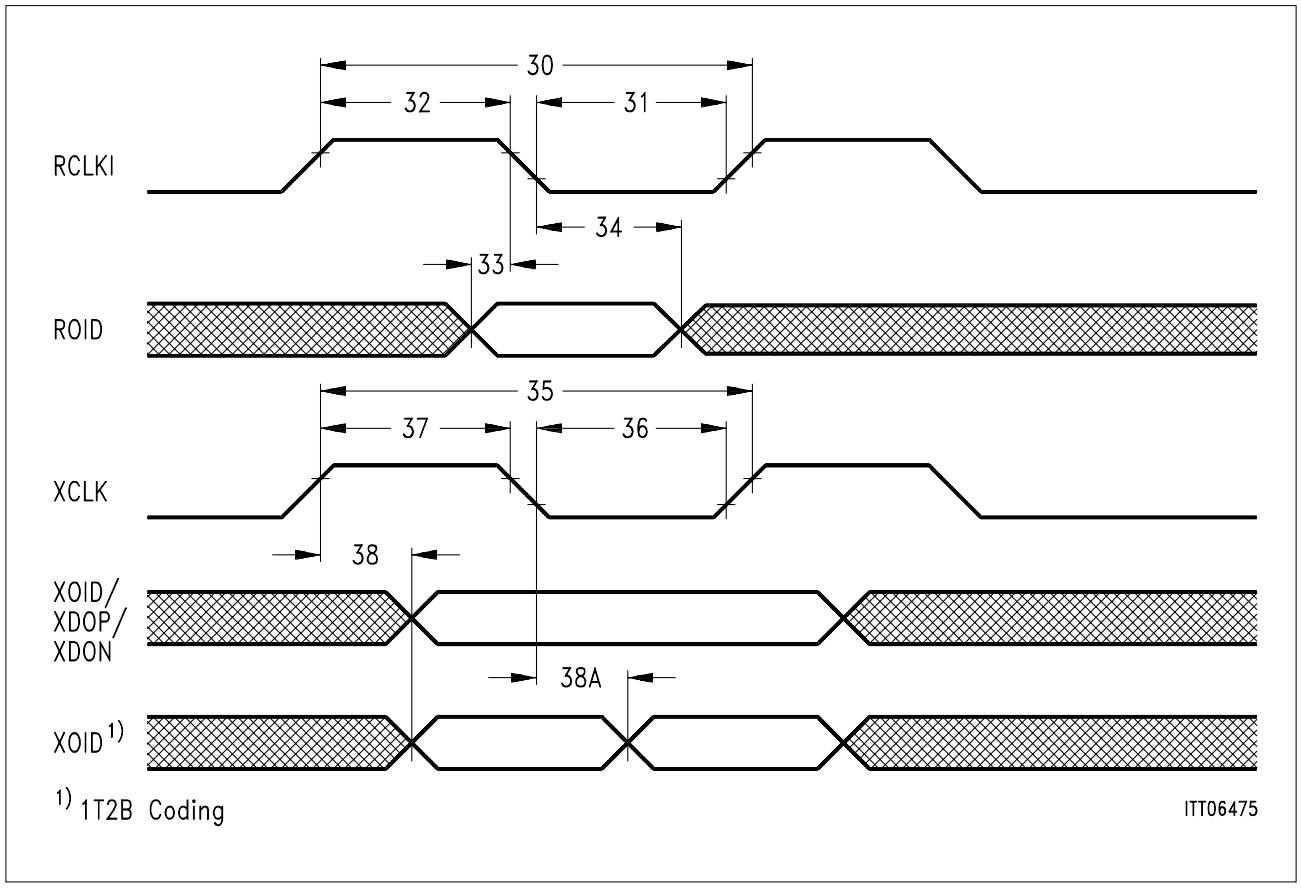


Figure 77
Timing of Dual Rail and Optical Interface

No.	Parameter	Limit Values						Unit
		PCM 30			PCM 24			
		min.	typ.	max.	min.		max.	
30	RCLKI clock period		488			648		ns
31	RCLKI clock period low	180			240			ns
32	RCLKI clock period high	180			240			ns
33	ROID setup	50			50			ns
34	ROID hold	50			50			ns
35	XCLK clock period		488			648		ns
36	XCLK clock period low XCLK clock period low[4)]	190 150			230 200			ns
37	XCLK clock period high XCLK clock period high[4)]	190 150			230 200			ns
38	XOID delay[1)] XDOP/XDON delay[2)]			50			50	ns
38A	XOID delay[3)]			50				ns

[1)] NRZ coding

[2)] HDB3/AMI coding

[3)] 1T2B coding

[4)] depends on input RCLKI in optical interface and remote loop without transmit jitter attenuator enabled (LIM1.JATT/RL=01).

Receive Clock and $\overline{\text{RFSP}}$/FREEZS Timing

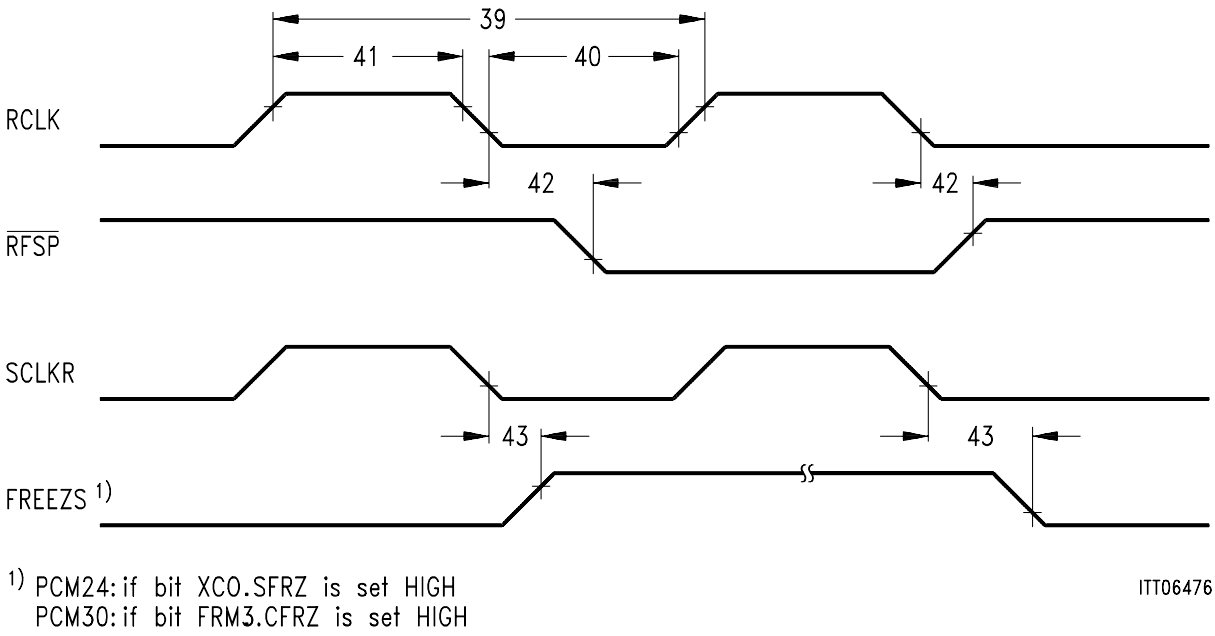


Figure 78
Receive Clock and $\overline{\text{RFSP}}$/FREEZS Timing

No.	Parameter	Limit Values						Unit
		PCM 30			PCM 24			
		min.	typ.	max.	min.	typ.	max.	
39	RCLK clock period		488			648		ns
40	RCLK clock period low	180			240			ns
41	RCLK clock period high	180			240			ns
42	$\overline{\text{RFSP}}$ delay			70			70	ns
43	FREEZS delay[1)]			95			95	ns

[1)] Only in PCM24 mode and if bit XCO.SFRZ is set HIGH.
In PCM30 mode and if bit FMR3.CFRZ is set high.

7.7 System Clocks

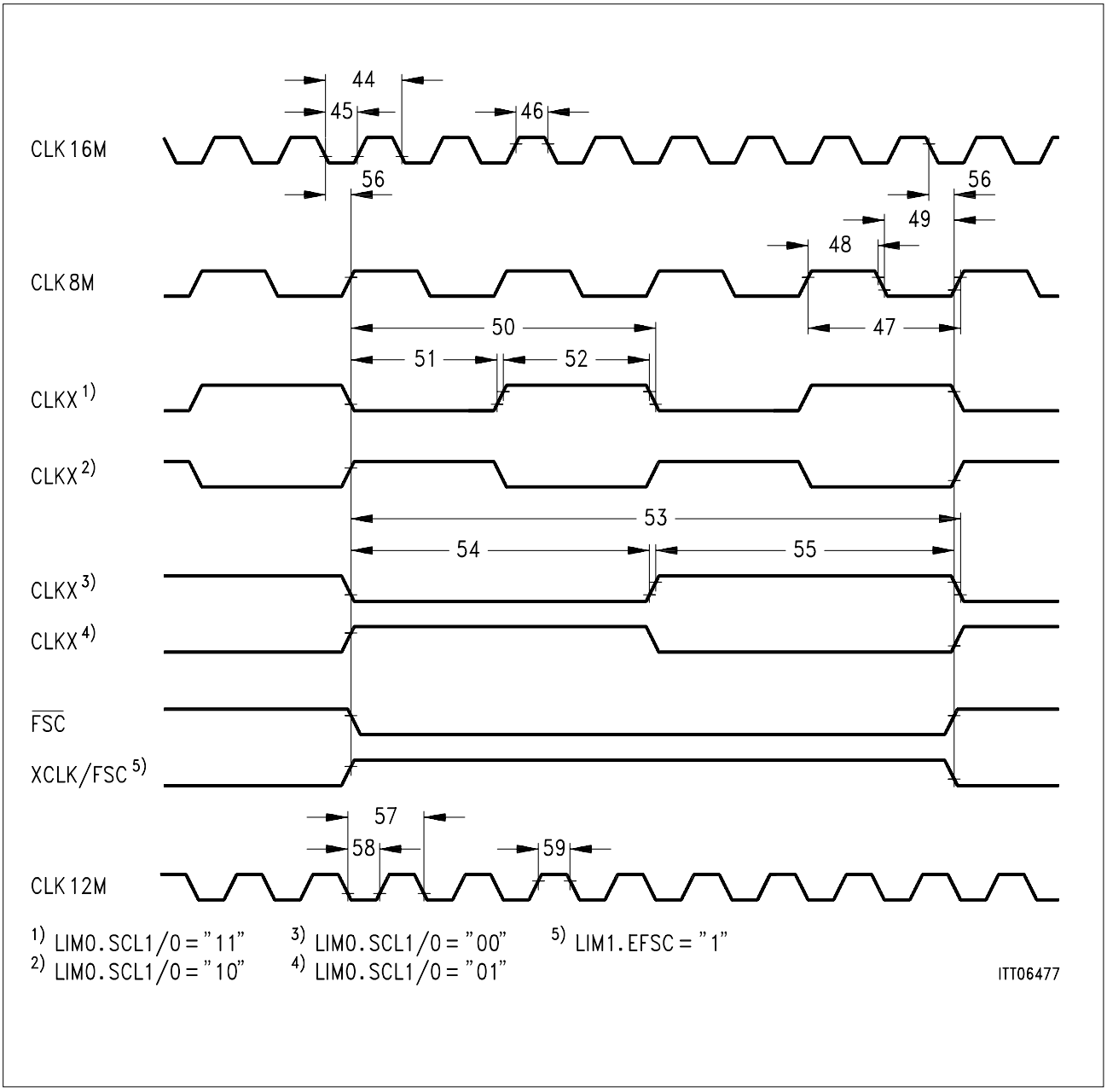


Figure 79
Timing of the System Clock Interface

System Clock Interface Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
44	CLK16M period 16 MHz		61		ns
45	CLK16M period 16 MHz low	20			ns
46	CLK16M period 16 MHz high	20			ns
47	CLK8M period 8 MHz		122		ns
48	CLK8M period 8 MHz low	45			ns
49	CLK8M period 8 MHz high	45			ns
50	CLKX period 4 MHz		244		ns
51	CLKX period 4 MHz low	100			ns
52	CLKX period 4 MHz high	100			ns
53	CLKX period 2MHz		488		ns
54	CLKX period 2 MHz low	220			ns
55	CLKX period 2 MHz high	220			ns
56	$\overline{\text{FSC}}$, FSC, CLK8M, CLKX delay			50	ns
57	CLK12M period 12 MHz		81		
58	CLK12M period 12 MHz low	25			ns
59	CLK12M period 12 MHz high	25			ns

XTAL Timing

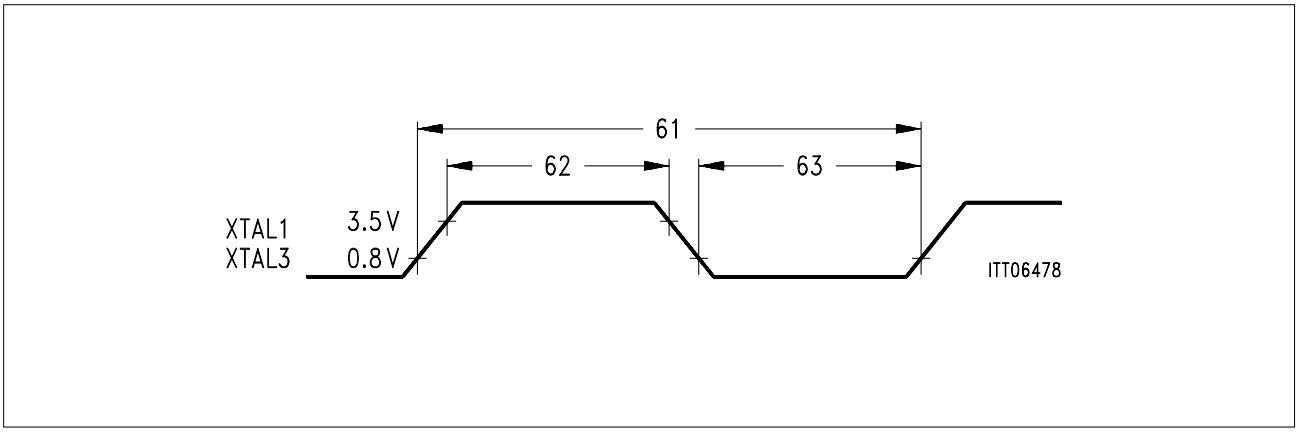


Figure 80
Timing of XTAL1/XTAL3

XTAL1/XTAL3 Timing Parameter Values

No.	Parameter	Limit Values			Unit	Condition
		min.	typ.	max.		
61	Clock period of crystal/clock		61 81		ns	XTAL1/3 XTAL3
62	High phase of crystal/clock	25 33			ns	XTAL1/3 XTAL3
63	Low phase of crystal/clock	25 33			ns	XTAL1/3 XTAL3

7.8 System Interface

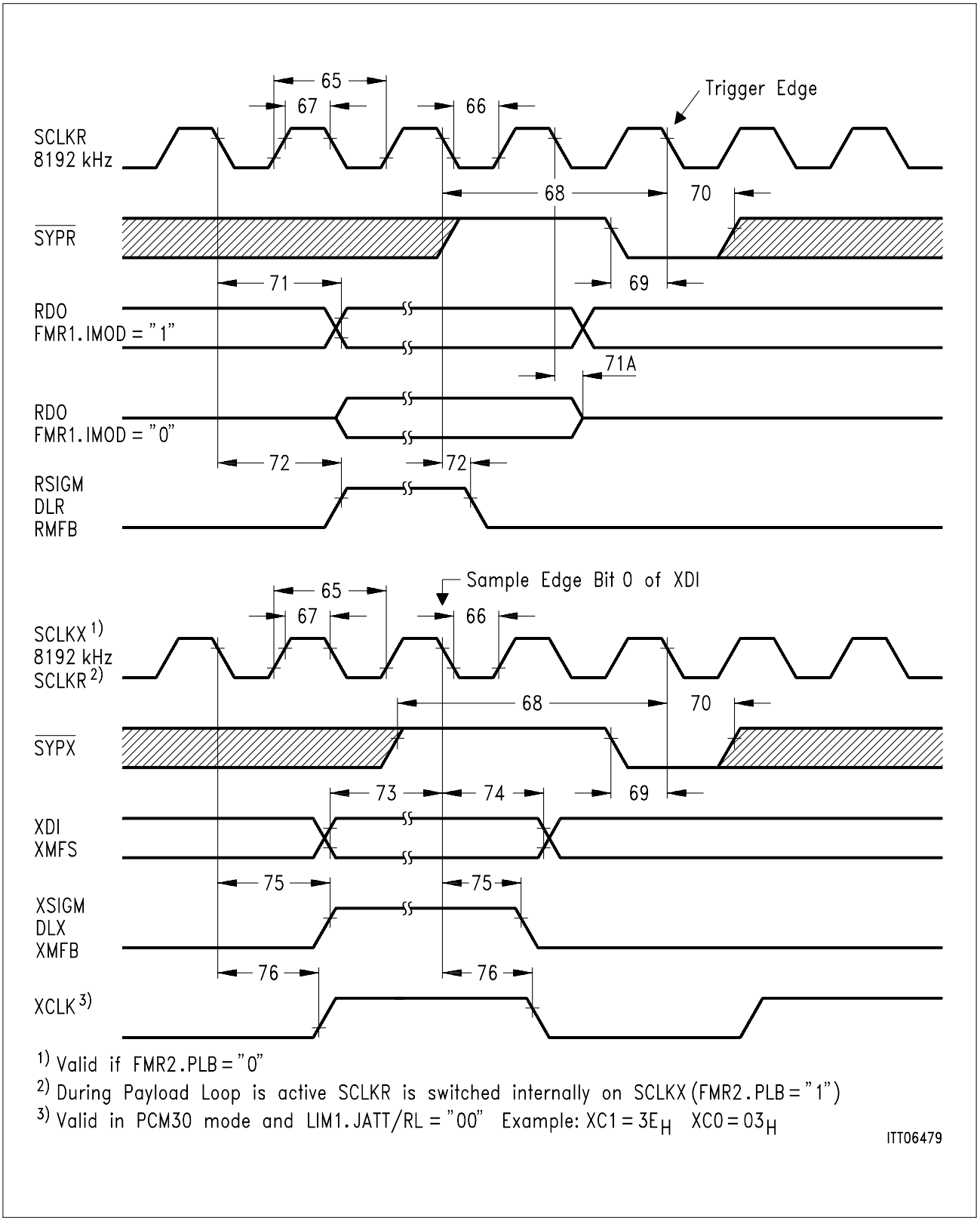


Figure 81
System Interface Timing

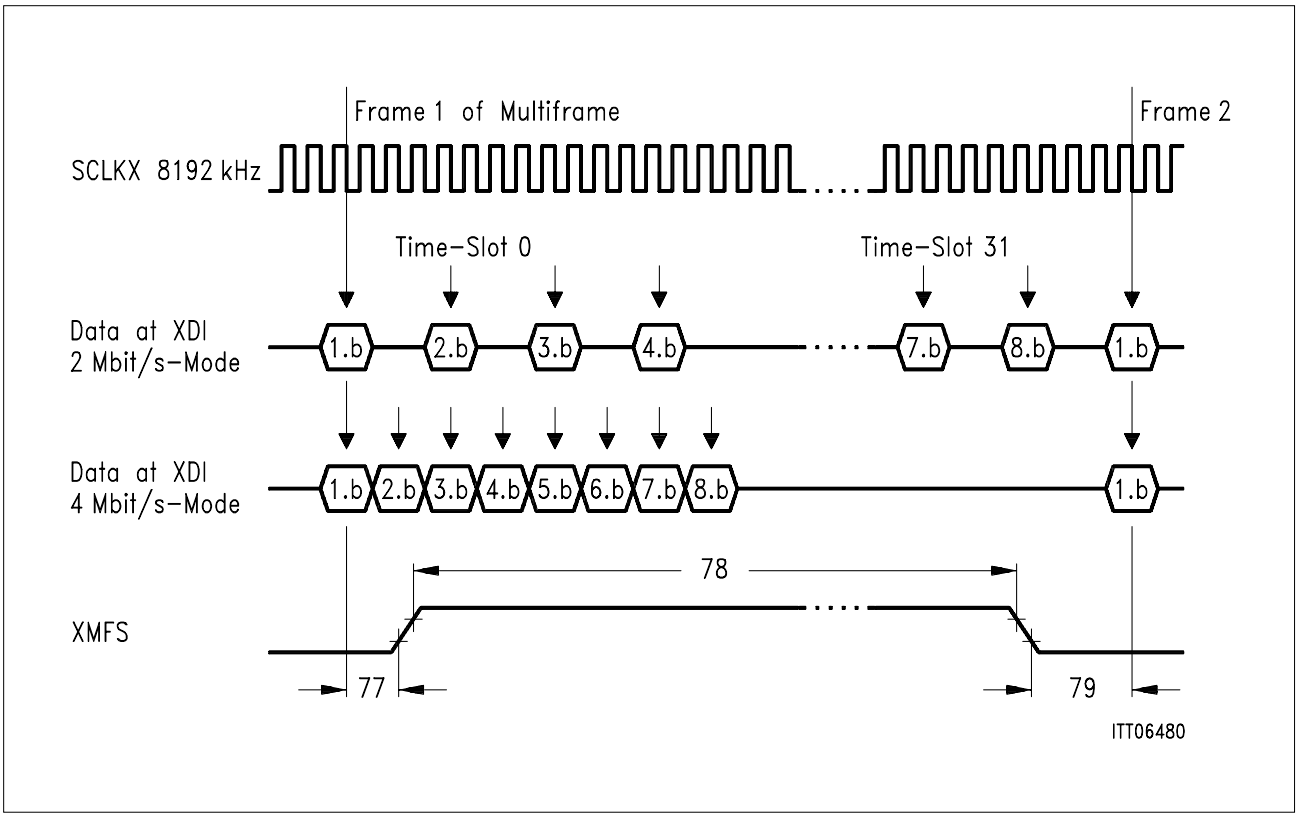


Figure 82
XMFS-Timing

System Interface Timing

No.	Parameter	Limit Values			Unit
		8192 kHz SCLK			
		min.	typ.	max.	
65	SCLKX/SCLKR period 8 MHz		122		ns
66	SCLKX/SCLKR period 8 MHz low	40			ns
67	SCLKX/SCLKR period 8 MHz high	40			ns
68	$\overline{\text{SYPX}}$/$\overline{\text{SYPR}}$ inactive setup time[1)]	$2 \times t_{65}$			ns
69	$\overline{\text{SYPX}}$/$\overline{\text{SYPR}}$ setup time	5			ns
70	$\overline{\text{SYPX}}$/$\overline{\text{SYPR}}$ hold time	55			ns
71	RDO delay	10 [1)]		105	ns
71A	RDO to high impedance[1)] (FMR1.IMOD = '0')	10		105	ns
72	RSIGM, RMFB, DLR marker delay			105	ns
73	XDI setup	5			ns
74	XDI hold	55			ns
75	XSIGM, XMFB, DLX marker delay			105	ns
76	XCLK delay			105	ns
77	XMFS setup time	5			ns
78	XMFS pulse width	$2 \times t_{65}$			ns
79	XMFS inactive setup time[1)]	$4 \times t_{65}$			ns

[1)] Not tested in production.

7.9 JTAG Boundary Scan Timing

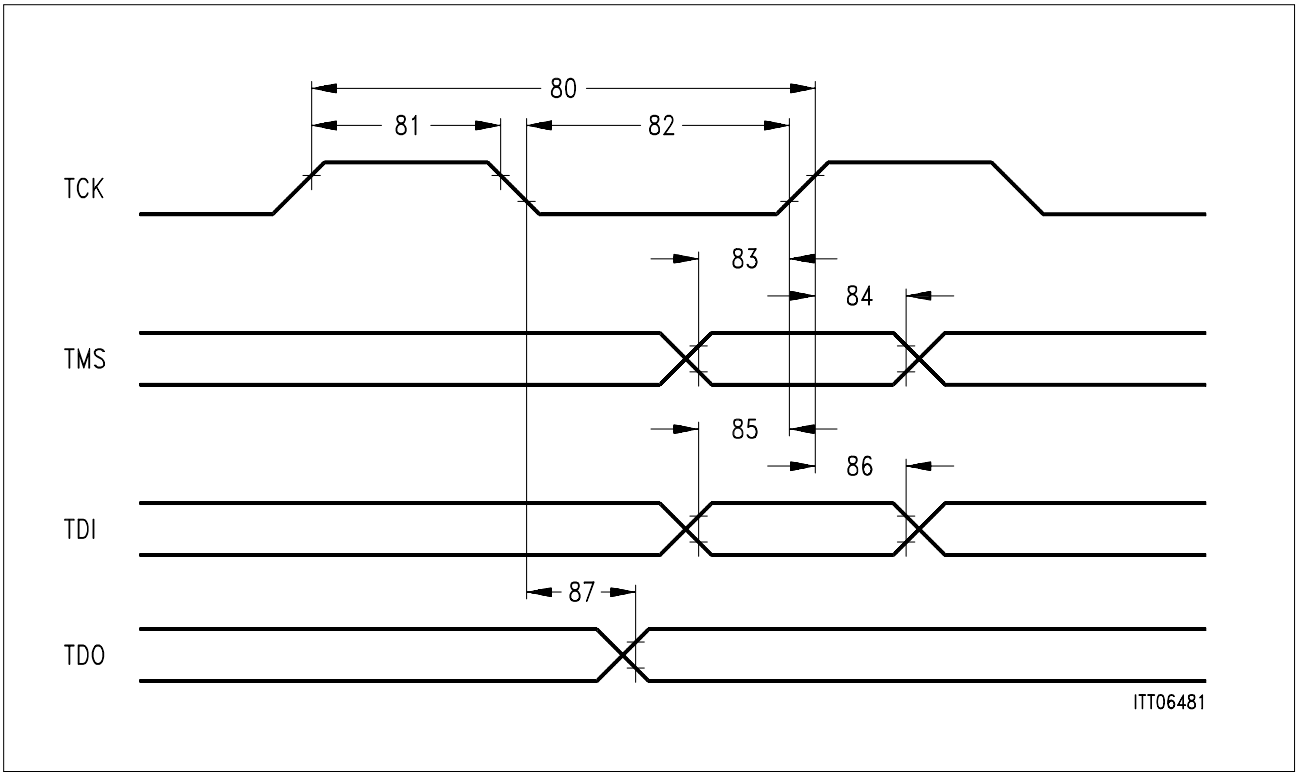


Figure 83
JTAG Boundary Scan Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
80	TCK period	250		ns
81	TCK high time	80		ns
82	TCK low time	80		ns
83	TMS setup time	40		ns
84	TMS hold time	40		ns
85	TDI setup time	40		ns
86	TDI hold time	40		ns
87	TDO valid delay		100	ns

Reset Timing

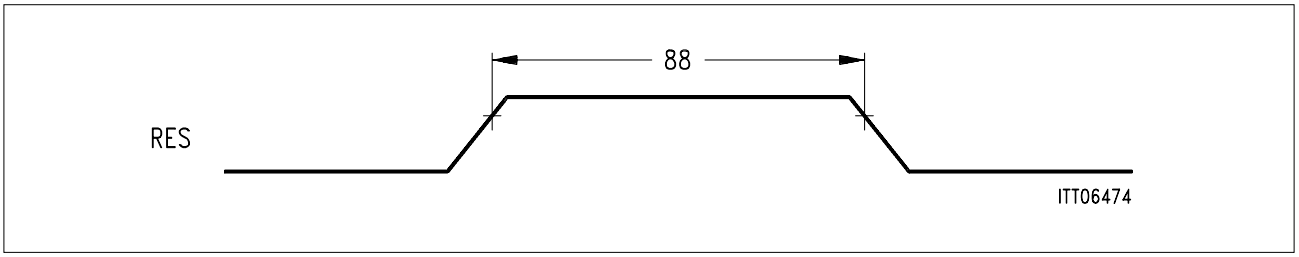


Figure 84
Reset Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
88	RES pulse width	20000		ns

7.10 Pulse Templates - Transmitter

The FALC54 meets both ITU-T and T1 pulse template requirements.

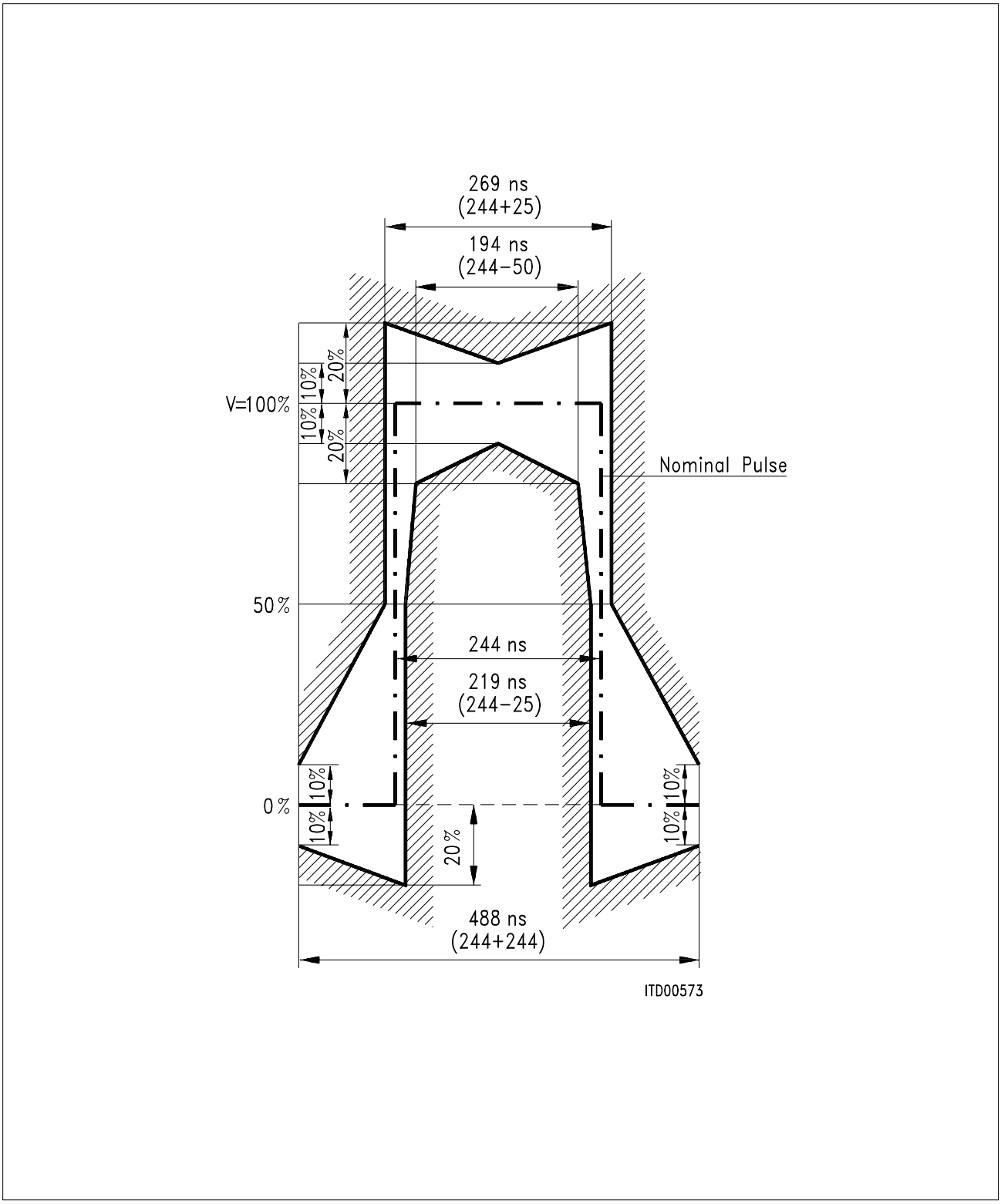


Figure 85
Pulse Template at the Transmitter Ouput for CEPT Applications

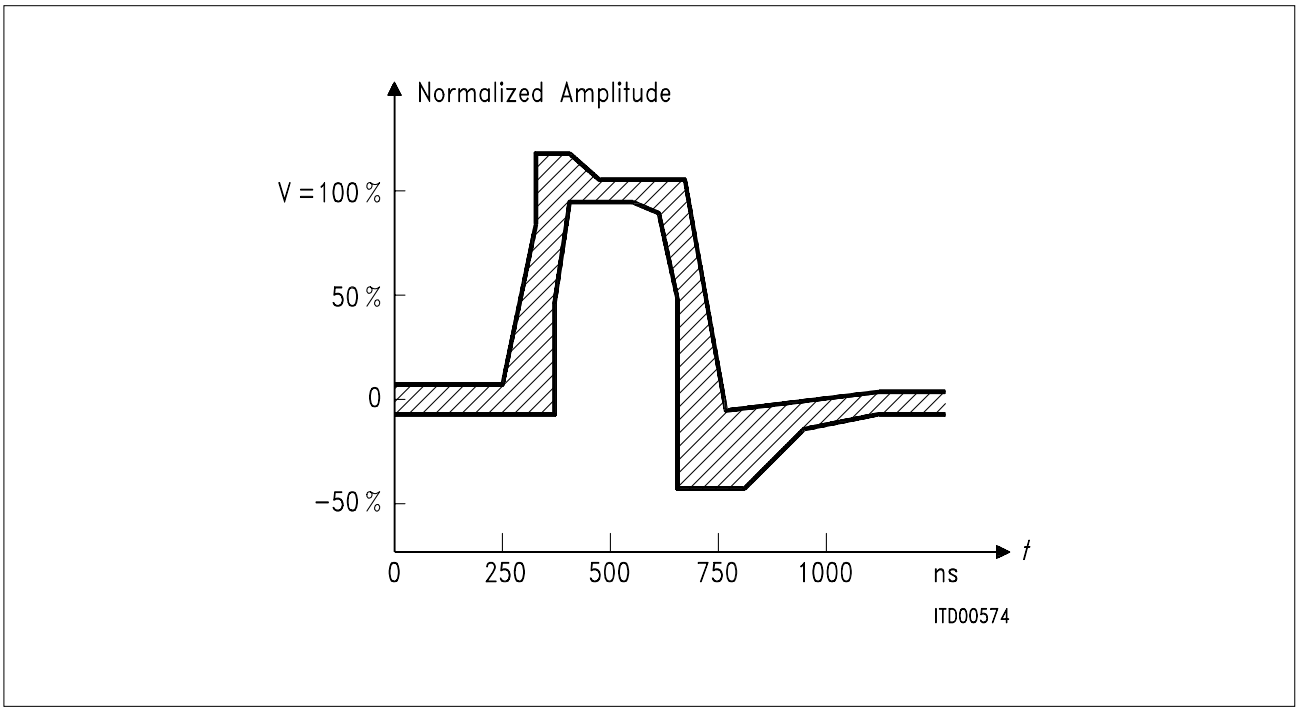


Figure 86
T1 Pulse Shape at the Cross Connect Point

Table 26
T1 Pulse Template Corner Points at the Cross Connect Point (T1.I102)

Maximum Curve		Minimum Curve	
Time [ns]	**V [%]**	**Time [ns]**	**V [%]**
(0,	0.05)	(0,	-0.05)
(250,	0.05)	(350,	-0.05)
(325,	0.80)	(350,	0.5)
(325,	1.15)	(400,	0.95)
(425,	1.15)	(500,	0.95)
(500,	1.05)	(600,	0.90)
(675,	1.05)	(650,	0.50)
(725,	-0.07)	(650,	-0.45)
(1100,	0.05)	(800,	-0.45)
(1250,	0.05)	(925,	-0.2)
		(1100,	-0.05)
		(1250,	-0.05)

100 % Value must be in the range between 2.4 V and 3.6 V.

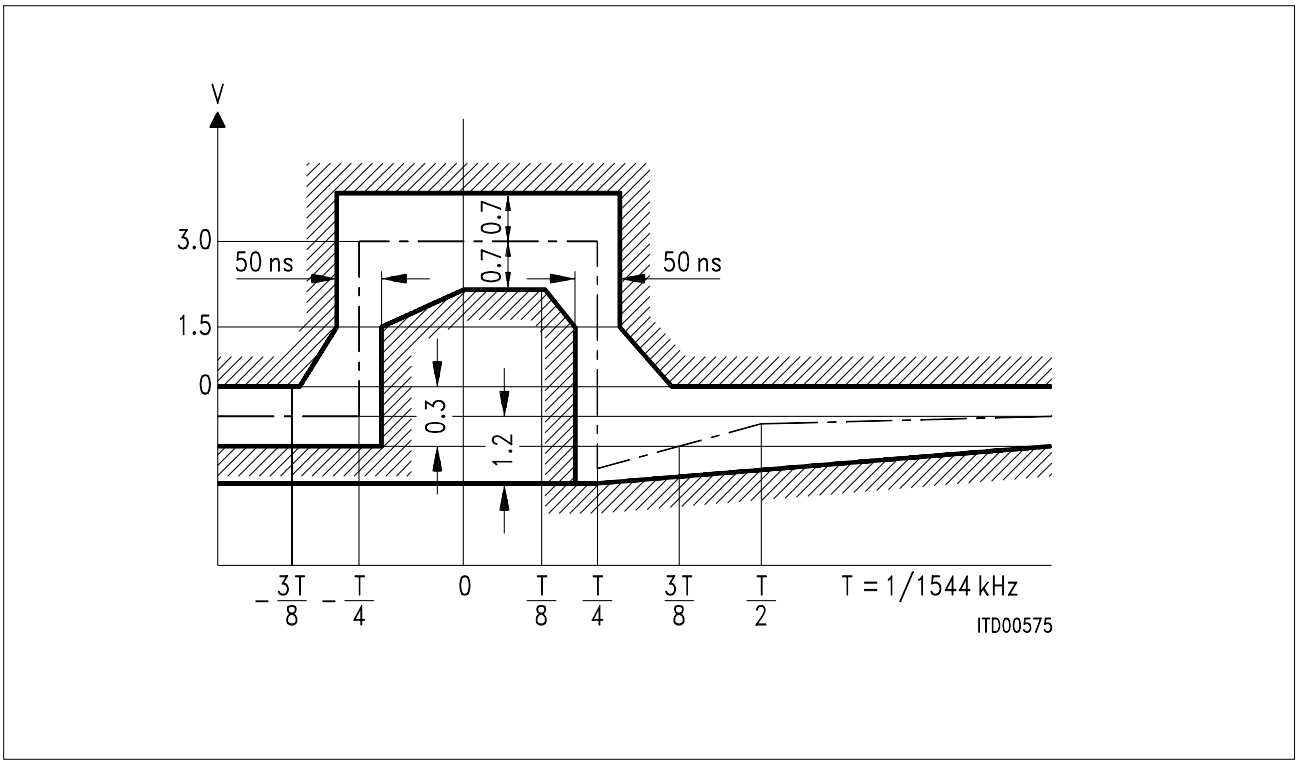
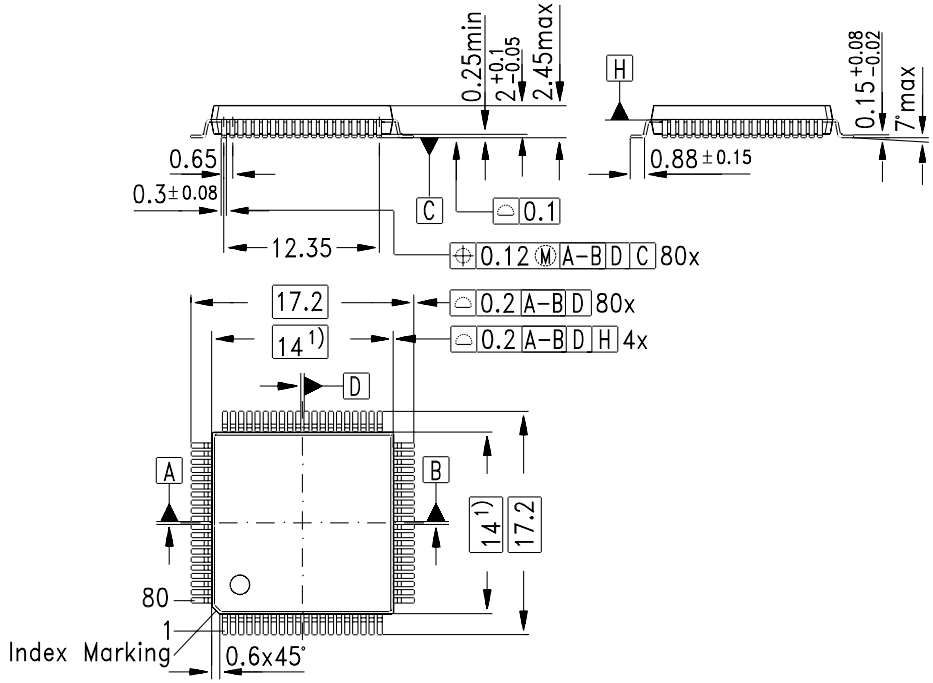


Figure 87
Pulse Shape According to ITU-T G.703

8 Package Outlines

P-MQFP-80-1
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”
SMD = Surface Mounted Device

Dimensions in mm