8255A

Programmable Peripheral Interface
iAPX86 Family
MILITARY INFORMATION

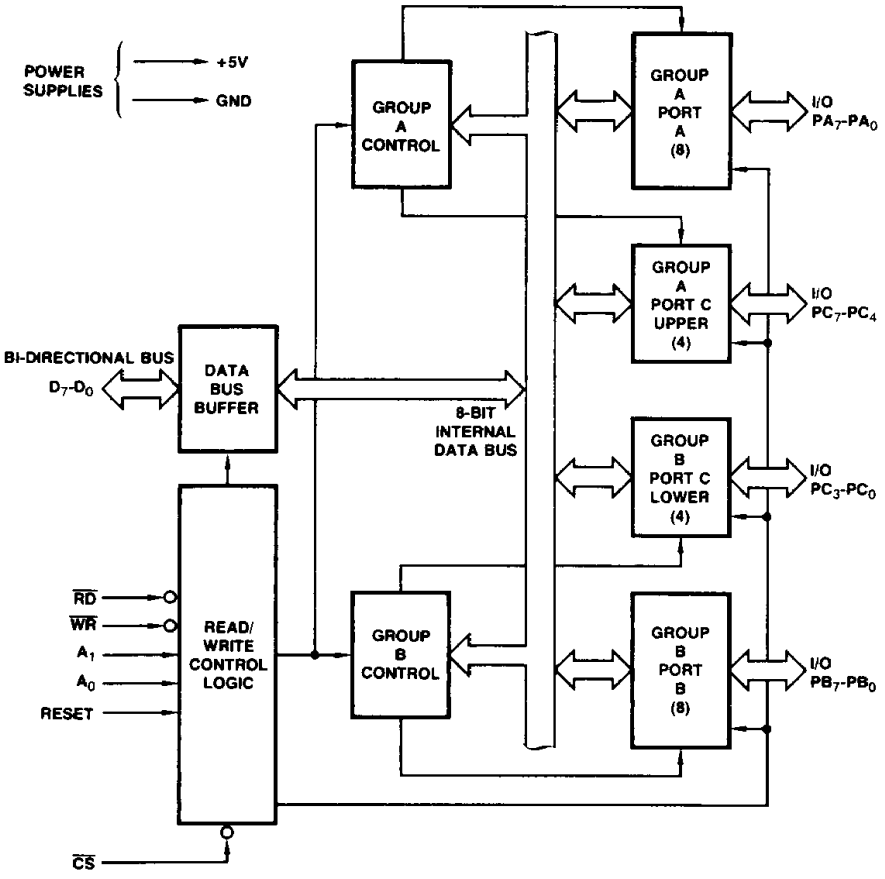
DISTINCTIVE CHARACTERISTICS

- SMD/DESC qualified
- Direct bit set/reset capability easing control application interface
- Reduces system package count
- Improved DC driving capability
- 24 programmable I/O pins
- Completely TTL-compatible
- Fully compatible with the iAPX86 microprocessor family
- Improved timing characteristics

GENERAL DESCRIPTION

The 8255A is a general-purpose, programmable I/O device designed for use with iAPX Family microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve, and used in three major modes of operation. In the first mode, each group of twelve I/O pins may be programmed in sets of four and eight to be input or output. In Mode 1, the second mode, each group may be programmed to have eight lines of input or output. Of the remaining four pins, three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a bidirectional bus mode which uses eight lines for a bidirectional bus, and five lines, borrowing one from the other group, for handshaking.

BLOCK DIAGRAM



BD003600

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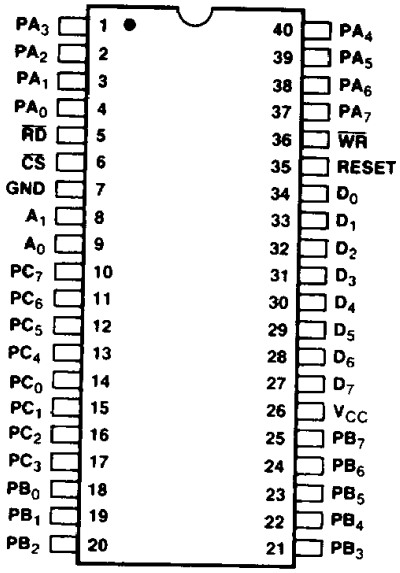
CONNECTION DIAGRAM
Top View



CD005401

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

5962-87570 01 Q X

d. LEAD FINISH
X = Any Lead Finish Acceptable

c. CASE OUTLINE
Q = 40-Pin Ceramic DIP (CD 040)

b. MILITARY DEVICE TYPE
01 = 2.5 MHz (8255A)
02 = 3.3 MHz (8255A-5)

a. MILITARY DRAWING NO./DESCRIPTION
5962-87570
Programmable Peripheral Interface

Valid Combinations	
5962-8757001	QX
5962-8757002	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

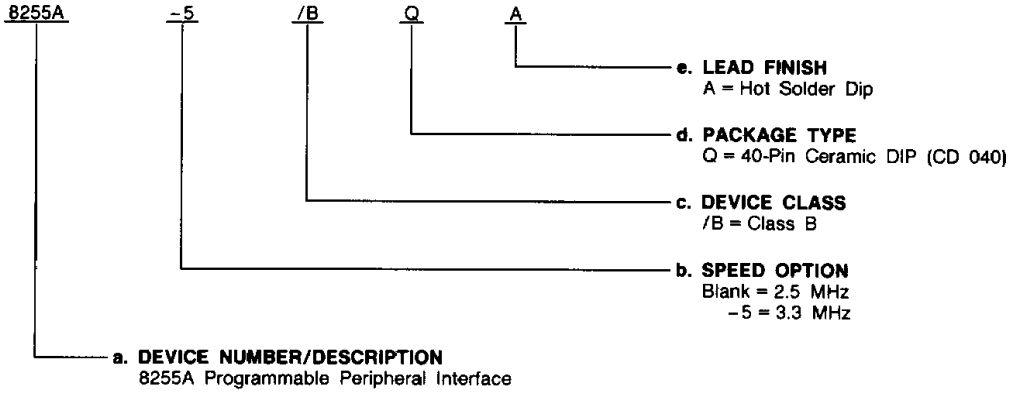
Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8255A	/BQA
8255A-5	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
V_{CC} with Respect to V_{SS} ..... −0.5 to 7.0 V
All Signal Voltages
with Respect to V_{SS} ..... −0.5 to +7.0 V
Power Dissipation ..... 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (TC) ..... −55 to 125°C
Supply Voltage (V_{CC}) ..... 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

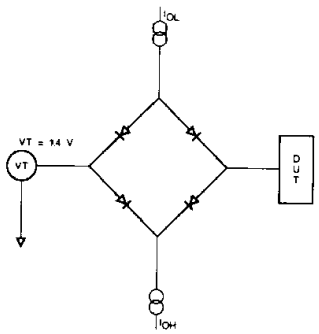
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}†	Input Low Voltage	V_{CC} = 4.5 V	−0.5 *	0.8	V
V_{IH}†	Input High Voltage	V_{CC} = 5.5 V	2.2	5.5*	V
V_{OL}(DB)	Output Low Voltage (Data Bus)	I_{OL} = 2.5 mA, V_{CC} = 5.5 V		0.45	V
V_{OL}(PER)	Output Low Voltage (Peripheral Port)	I_{OL} = 1.7 mA, V_{CC} = 5.5 V		0.45	V
V_{OH}(DB)	Output High Voltage (Data Bus)	I_{OH} = −400 μA, V_{CC} = [illegible]	2.4		V
V_{OH}(PER)	Output High Voltage (Peripheral Port)	I_{OH} = −200 μA, V_{CC} = [illegible]	2.4		V
I_{DAR}	Darlington Drive Current (Note 1)	R_{EXT} = [illegible] V_{EXT} = 1.5 V	−1.0	−4.0	mA
I_{CC}	Power Supply Current (Note 2)	V_{CC} = 5.5 V		120	mA
I_{IL}	Input Load Current	V_{IN} = V_{CC} to 0 V, V_{CC} = 5.5 V		±10	μA
I_{OFL}	Output Float Leakage	V_{OUT} = V_{CC} to 0 V, V_{CC} = 5.5 V		±10	μA

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0 V

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}††	Input Capacitance	fc = 1 MHz			15*	pF
$C_{I/O}$††	I/O Capacitance	Unmeasured pins returned to GND			25*	pF

*Guaranteed by design; not tested.
†Group A, Subgroups 9, 10, 11 only are tested.
††Not included in Group A tests.
Notes: 1. Available on any 8 pins from Port B and C.
2. I_{CC} test conditions: the supply current is measured with loaded outputs while running AC patterns.

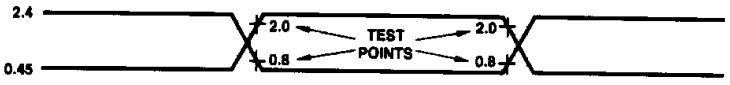
SWITCHING TEST CIRCUIT



TC003850

This test circuit is the dynamic load of a Teradyne J941.

SWITCHING TEST WAVEFORM



WF006351

AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0."
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 1)

BUS PARAMETERS

No.	Parameter Symbol	Parameter Description	8255A		8255A-5		Unit
			Min.	Max.	Min.	Max.	
READ							
1	t_{AR}	Address Stable Before READ	0		0		ns
2	t_{RA}	Address Stable After READ	0		0		ns
3	t_{RR}	READ Pulse Width	300		300		ns
4	t_{RD}	Data Valid From READ (Note 1)		250		200	ns
5	t_{DF}	Data Float After READ (Note 3)	10	150	10	100	ns
6	t_{RV}	Time Between READs and/or WRITEs	850		850		ns
WRITE							
7	t_{AW}	Address Stable Before WRITE	0		0		ns
8	t_{WA}	Address Stable After WRITE	20		20		ns
9	t_{WW}	WRITE Pulse Width	400		300		ns
10	t_{DW}	Data Valid to WRITE (T.E.)	[illegible]		100		ns
11	t_{WD}	Data Valid After WRITE	[illegible]		30		ns
OTHER TIMINGS							
12	t_{WB}	WR = 1 to Output (Note 1)		350		350	ns
13	t_{IR}	Peripheral Data Before RD	0		0		ns
14	t_{HR}	Peripheral Data After RD	0		0		ns
15	t_{AK}	ACK Pulse Width	300		300		ns
16	t_{ST}	STB Pulse Width	500		500		ns
17	t_{PS}	Per. Data Before T.E. of STB	0		0		ns
18	t_{PH}	Per. Data After T.E. of STB	180		180		ns
19	t_{AD}	ACK = 0 to Output (Note 1)		300		300	ns
20	t_{KD}	ACK = 1 to Output Float (Note 3)	20	250	20	250	ns
21	t_{WOB}	WR = 1 to OBF = 0 (Note 1)		650		650	ns
22	t_{AOB}	ACK = 0 to OBF = 1 (Note 1)		350		350	ns
23	t_{SIB}	STB = 0 to IBF = 1 (Note 1)		300		300	ns
24	t_{RIB}	RD = 1 to IBF = 0 (Note 1)		300		300	ns
25	t_{RIT}	RD = 0 to INTR = 0 (Note 1)		400		400	ns
26	t_{SIT}	STB = 1 to INTR = 1 (Note 1)		300		300	ns
27	t_{AIT}	ACK = 1 to INTR = 1 (Note 1)		350		350	ns
28	t_{WIT}	WR = 1 to INTR = 0 (Note 1)		450		450	ns

Notes: 1. Test Conditions: V_{CC} = 5.5 V and 4.5 V, V_{IH} = 2.4 V, V_{IL} = .45 V, V_{OH} = 2.0 V, V_{OL} = .8 V, C_L = 100 pF ± 20 pF.

2. Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

3. AC float timing parameters t_{DF} and t_{KD} are tested Logic 0 to float only.