AT&T

DATA SHEET

229CG Framer

FEATURES

- Multiple line-format capability
  - AMI and HDB3 (CEPT)
  - Bipolar and B8ZS
- Multiple DS1 TDM frame formats
  - Independent formats — D4, *SLC*® Carrier, ESF, and DDS T1DM (DS1)
  - CCITT 30-channel format, with optional TS-16 signaling (CEPT)
- Off-line, defensive, and fast frame synchronization
- *SLC* Carrier, ESF, and DDS T1DM facility data-link insertion and extraction
- Remote frame/multiframe alarm activation and detection
- AIS detection
- Transmission performance monitoring capability:
  - Bipolar, B8ZS, AMI, and HDB3 violations
  - Frame-alignment signal (frame bit) errors
  - Loss-of-frame/loss-of-multiframe alignment
  - CRC-6 errors (ESF mode)
  - Change-of-frame alignment

DESCRIPTION

The 229CG Framer integrated circuit provides the line format and frame format interfaces for DS1 (1.544 Mb/s) and CEPT (2.048 Mb/s) digital carrier systems. It performs in-line and off-line frame-oriented functions in both the receive and transmit directions. The 229CG Framer is TTL-compatible and is packaged in a 40-pin ceramic DIP.

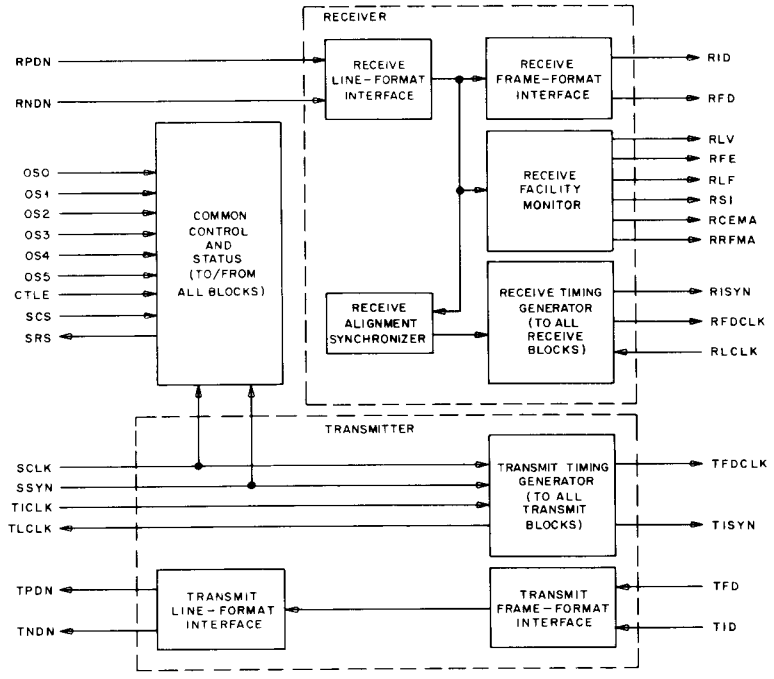

Figure 1. 229CG Framer Block Diagram

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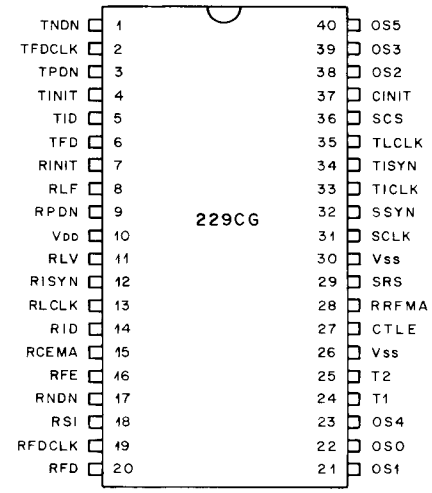
USER INFORMATION

Pin Descriptions



Symbol	Pin	Symbol	Pin	Symbol	Pin
CINIT	37	RISYN	12	TFD	6
CTLE	27	RLCLK	13	TFDCLK	2
OS0	22	RLF	8	TICLK	33
OS1	21	RLV	11	TID	5
OS2	38	RNDN	17	TINIT	4
OS3	39	RPDN	9	TISYN	34
OS4	23	RRFMA	28	TLCLK	35
OS5	40	RSI	18	TNDN	1
RCEMA	15	SCLK	31	TPDN	3
RFD	20	SCS	36	VDD	10
RFDCLK	19	SRS	29	VSS	26
RFE	16	SSYN	32	VSS	30
RID	14	T1	24		
RINIT	7	T2	25		

Figure 2. 229CG Framer Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. 229CG Framer Pin Descriptions

Pin	Symbol	Type	Name/Function
1	TNDN	O	**Transmit Negative-Rail Data Inverted.** 1.544 Mb/s (DS1) or 2.048 Mb/s (CEPT) dual-rail pseudoternary (bipolar, B8ZS, AMI, or HDB3) TDM data.
2	TFDCLK	O	**Transmit Facility Data Link Clock.** Reference clock for transmit facility data-link data on pin 6. In DDS mode, this is an 8 kHz clock signal; in *SLC* Carrier, ESF, and IRSM modes, this is a 4 kHz clock signal.
3	TPDN	O	**Transmit Positive-Rail Data Inverted.** 1.544 Mb/s (DS1) or 2.048 Mb/s (CEPT) dual-rail pseudoternary (bipolar, B8ZS, AMI, or HDB3) TDM data.
4	TINIT	I	**Transmit Initialization.** Manufacturing test pin. Ground this pin for normal operation. Setting (1) pins 4, 7, and 37 puts all transmit output pins in a high-impedance, 3-state mode.
5	TID	I	**Transmit Interdevice Data.** 1.544 Mb/s (DS1) or 2.048 Mb/s (CEPT) unipolar TDM source data.

Table 1. 229CG Framer Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
6	TFD	I	**Transmit Facility Data-Link Data.** 8 kb/s data in the DDS mode. 4 kb/s in the *SLC* Carrier, ESF, and IRSM modes. Data-link source data is strobed in by negative transitions of TFDCLK (pin 2).
7	RINIT	I	**Receive Initialization.** Manufacturing test pin. Ground this pin for normal operation. Setting (1) pins 4, 7, and 37 puts all receive section output pins in a high-impedance, 3-state mode.
8	RLF	O	**Receive Loss-of-Frame Alignment.** This pin is set (1) upon loss-of-frame and/or loss-of-multiframe alignment.
9	RPDN	I	**Receive Positive-Rail Data Inverted.** 1.544 Mb/s (DS1) or 2.048 Mb/s (CEPT) dual-rail pseudoternary (bipolar, B8ZS, AMI, or HDB3) TDM data. Tie RPDN and RNDN (pin 17) together for unipolar TDM received data.
10	V_{DD}	—	**5 V Supply.**
11	RLV	O	**Receive Line-Format Violations.** This pin is set (1) for each received line-format violation.
12	RISYN	O	**Receive Interdevice Synchronization.** A 648 ns (DS1 mode) or 488 ns (CEPT mode) pulse repeated at 3 ms intervals in DS1 mode; 2 ms intervals in CEPT mode. Transitions of RISYN occur on negative transitions of RLCLK (pin 13).
13	RLCLK	I	**Receive Line Clock.** 1.544 MHz (DS1) or 2.048 MHz (CEPT) clock signal.
14	RID	O	**Receive Interdevice Data.** 1.544 Mb/s (DS1) or 2.048 Mb/s (CEPT) unipolar TDM output data. Transitions of RID occur on negative transitions of RLCLK (pin 13).
15	RCEMA	O	**Receive CRC-6 Errors/Loss-of-Multiframe Alignment.** This pin is set (1) upon a received cyclic redundancy check error in DS1 ESF mode, or loss-of-multiframe alignment in CEPT mode.
16	RFE	O	**Receive Frame Alignment Signal Error.** This pin is set (1) upon detection of frame-alignment signal (frame bit) error.
17	RNDN	I	**Receive Negative-Rail Data Inverted.** 1.544 Mb/s (DS1) or 2.048 Mb/s (CEPT) dual-rail pseudoternary (bipolar, B8ZS, AMI, or HDB3) TDM data.
18	RSI	O	**Receive Signaling Inhibit.** This pin is set (1) by a framing error, loss-of-frame and/or loss-of-multiframe alignment.
19	RFDCLK	O	**Receive Facility Data-Link Clock.** Reference clock for receive facility data-link data on pin 20. In DDS mode, this is an 8 kHz clock signal; in *SLC* Carrier, ESF, and IRSM modes, this is a 4 kHz clock signal.
20	RFD	O	**Receive Facility Data-Link Data.** 8 kb/s data in DDS mode; 4 kb/s data in *SLC* Carrier, ESF, and IRSM modes.

Table 1. 229CG Framer Pin Descriptions (Continued)			
Pin	**Symbol**	**Type**	**Name/Function**
21 22 23	OS1 OS0 OS4	I	**Option Selects 1, 0, and 4.** Option selection pins. Options may also be selected by using the serial control stream (pin 36).
24	T1	I	**Test 1.** For manufacturing purposes only. Must be grounded for normal operation.
25	T2	I	**Test 2.** For manufacturing purposes only. Must be grounded for normal operation.
26	VSS	—	**Ground.**
27	CTLE	I	**Control Enable.** Control lead to enable loading of serial control stream (pin 36).
28	RRFMA	O	**Receive Remote Frame and Multiframe Alarm.** This pin is set (1) upon a received remote frame alarm and cleared (0) otherwise.
29	SRS	O	**Serial Report Stream.** The serial report stream is output at a 1 MHz bit rate. SRS contains one byte for facility reports, one byte for device alarms, and four bytes for auditing the option, exercise, action, and action-mask control fields. Each of these six bytes is repeated twice per frame; the remaining four bytes are padded with zeros. Facility and alarm bytes are updated once a frame; the remaining four control bytes are updated twice a frame.
30	VSS	—	**Ground.**
31	SCLK	I	**System Clock.** 4.096 MHz system clock.
32	SSYN	I	**System Synchronization.** 8 kHz system synchronization pulse of 244 ns duration. SSYN is strobed on positive transitions of both SCLK (pin 31) and TICLK (pin 33).
33	TICLK	I	**Transmit Interdevice Clock.** 1.544 MHz (DS1 mode) or 2.048 MHz (CEPT mode).
34	TISYN	O	**Transmit Interdevice Synchronization.** This pin establishes frame alignment. It is a bit interval pulse set (1) every 3 ms in DS1 mode and every 2 ms in the CEPT mode.
35	TLCLK	O	**Transmit Line Clock.** 1.544 MHz (DS1 mode) or 2.048 MHz (CEPT mode).
36	SCS	I	**Serial Control Stream.** SCS accepts 8-bit control bytes at a 1 MHz bit rate. Control bytes determine options, consequent actions (channel squelch, FDL squelch remote-alarm insertion, etc.), action masks, and maintenance exercises. A control byte is shifted in on SCS while CTLE (pin 27) is set (1).
37	CINIT	I	**Control Initialization.** Manufacturing test pin. Ground this pin for normal operation. Setting (1) pins 4, 7, and 37 puts all control and report pins in a high-impedance, 3-state mode.
38 39 40	OS2 OS3 OS5	I	**Option Selects 2, 3, and 5.** Option selection pin. Options may also be selected by using the serial control stream (pin 36).

Overview

The 229CG Framer is part of an LSI DS1 chip set that also includes the 257AU Receive Synchronizer, the 257AL Transmit Formatter, and the 229FB Maintenance Buffer. The framer performs in-line data processing, off-line terminal-frame and signaling-frame synchronization, transmission-facility monitoring, and system-fault monitoring.

The functional operation of the 229CG Framer is discussed in terms of Figure 1. The circuit is divided into three main blocks: transmitter, receiver, and common control and status. The transmitter and receiver process information signals passing through the device in the transmit and receive directions, respectively; the common control and status block is the control and status interface for the device.

Transmitter

The transmit section of the 229CG Framer consists of the transmit timing generator (TTG), transmit frame-format interface (TFFI) and the transmit line-format interface (TLFI). The TFFI accepts a unipolar, time-division multiplex (TDM) signal on TID and a unipolar facility data-link bit stream in TFD. TID is clocked either by a 1.544 MHz (DS1 mode) or 2.048 MHz (CEPT mode) timing signal input on TICLK, and must be synchronized to the 3 ms (DS1 mode) or 2 ms (CEPT mode) interval pulse output on TISYN. The FDL bit stream on TFD must be clocked by the 4 MHz or 8 MHz timing signal output on TFDCLK.

The TDM signal on TID must be formatted with customer data and signaling already in place in channel time slots, but with a pseudorandom maintenance pattern in the framing bit (F-bit) positions in the DS1 mode and in TS0 in the CEPT mode. According to the selected DS1 mode, the TFFI overwrites the F bits with the terminal-framing (Ft or Fe) or signaling-framing (Fs) pattern, the CRC-6 check bits and/or the FDL bit stream. The TFFI also inserts the remote-frame (yellow) alarm (RFA) in the FDL bit positions in the extended superframe (ESF) mode, and generates the CRC-6 check bits. In the CEPT mode, the TFFI overwrites TS0 with the FAS pattern and the RFA bit and, when requested, sets the I and N bits to 1. It can also set the TS16 RMA bit and x bits.

In general, the TFFI is transparent to channel time slots. When requested, however, it can overwrite the words as follows:

- D4 RFA, zero-code suppression (ZCS) and maintenance squelch patterns in all words.
- DDS frame-alignment pattern, FDL bits and RFA in word 24.

The TLFI converts the unipolar TDM signal from the TFFI to a dual-rail bipolar signal and, in the B8ZS or HDB3 mode, replaces strings of zeros with the B8ZS or HDB3 violation codes. The resulting dual-rail TDM signal is output on TPDN and TNDN.

The TTG generates TISYN in fixed relation to a 125 μs interval system sync pulse input on SSYN. It also generates TFDCLK, a 1.544 MHz (DS1 mode) or 2.048 MHz (CEPT mode) timing signal output on TLCLK, and all internal synchronization signals. Finally, in the *SLC* Carrier mode (SL mode), it synchronizes to the Fs pattern that must be embedded in the FDL bit stream on TFD.

Receiver

The receive section of the 229CG Framer comprises the receive timing generator (RTG), the receive frame-format interface (RFFI), the receive line-format interface (RLFI), the receive alignment synchronizer (RAS), and the receive facility monitor (RFM). The RFFI accepts a dual-rail TDM signal on RPDN and RNDN. These inputs are clocked by a 1.544 MHz (DS1 mode) or 2.048 MHz (CEPT

mode) timing signal input on RLCLK. The TDM signal is converted to unipolar and, in the B8ZS or HDB3 mode, instances of the B8ZS or HDB3 violation code are replaced by strings of zeros. The RLFI detects violations of the bipolar, B8ZS, or HDB3 codes and reports them to the RFM. The TDM output signal is distributed to the RFFI, the RAS, and the RFM sections.

The RFFI first extracts the FDL bit stream from the F-bits in the TDM signal and then overwrites the DS1 F-bits or TS0 bit 3 with the pseudorandom pattern (PRP). In general, the RFFI is transparent to channel time slots. When requested or authorized, however, it can overwrite all words with a maintenance squelch pattern. In the DDS mode, facility-error information from the RFM section is autonomously inserted in the RFA bit position of word 24. The RFFI outputs the processed unipolar TDM signal on RID and the extracted FDL bit stream on RFD. RID is clocked by the 1.544 MHz (DS1 mode) or 2.048 MHz (CEPT mode) timing signal RLCLK and is synchronized to the 3 ms (DS1 mode) or 2 ms (CEPT mode) interval pulse output on RISYN. The FDL bit stream on RFD is clocked by the 4 MHz or 8 MHz timing signal output on RFDCLK.

The RFM section monitors the TDM signal for facility trouble conditions and alarms. Detected trouble conditions and alarms are forwarded to the common control and status block, and also to dedicated status output leads RLV, RFE, RLF, RCEMA, RRFMA, and RSI. Detected loss-of-alignment conditions are reported to the RAS section.

The RAS section establishes terminal-frame alignment in all modes, superframe alignment in the D4, SL, and ESF modes, and multiframe alignment in the CEPT mode. It operates in a fast, off-line, defensive mode for terminal-frame synchronization; the search for the frame-alignment pattern and/or sequence (FAS) covers all possible alignment phases simultaneously. When a single candidate FAS is found, alignment is adjusted to the phase of that FAS. To avoid synchronization to a random data pattern, the search cannot be satisfied until at least 24 bits of the candidate FAS have been examined. The search does not affect operation of the other sections of the receiver until the decision is made that a new frame alignment is required. Consequently, an error burst does not force a loss of alignment.

To avoid alignment to a fixed data or signaling pattern that emulates the FAS, the RAS does not adjust alignment to a new phase if there is more than one candidate FAS present. When static emulators last for more than 100 ms in the ESF mode, the synchronizer aligns successively to each candidate FAS (at 200 ms per candidate) until an alignment with the correct CRC-6 pattern is found. This on-line trial-and-error mode is not possible in the D4, DDS, SL, and CEPT modes.

The RTG generates RISYN in fixed relation to the TDM signal output on RID, RFDCLK in fixed relation to the FDL bit stream output on RFD, and all internal synchronization signals.

Common Control and Status

The principle control access to the 229CG Framer is the 1.024 Mb/s serial control stream input on SCS. The SCS is used for provisioning, maintenance exercises, and requests for the application of squelch patterns and remote alarms. The SCS is enabled by the control stream enable input on CTLE. The mode of the device may also be controlled via external option input leads OS0—OS5.

The 1.024 Mb/s serial report stream, output on SRS, carries reports from the RFM section, reports from fault-monitoring circuits distributed throughout the device, and audits of the current control state.

The SCS and SRS are clocked at the 1.024 Mb/s rate by a submultiple of the 4.096 MHz timing signal input on SCLK. The bit boundaries in both the SCS and the SRS and the byte and block boundaries in the SRS are synchronized to the system sync pulse input on SSYN.

Functional Description

Line Format Processing

The transmitter line-format interface processing converts the frame-formatted TDM bit stream into a dual-rail bipolar signal or a modified bipolar output signal (B8ZS or HDB3). In the bipolar and AMI modes, binary ones (1s) in the TDM bit stream become pulses of alternating polarity transmitted between the two output rails, TPDN and TNDN; binary zeros are transmitted as null pulses. Note that the outputs are active low, so that a pulse corresponds to a binary zero (0) and no pulse corresponds to a binary one (1). In the B8ZS and HDB3 modes, the bipolar algorithm is modified to guarantee at least one pulse for every 8 transmitted bits by substituting a bipolar violation code (BPV) for blocks of 8 or 4 successive 0's, as illustrated in Tables 2 and 3. The transmitter generates BPVs by sending the BPV pulse to the same output rail as the last preceding bipolar pulse.

Table 2. B8ZS Substitution Code

Before B8ZS	0	0	0	0	0	0	0	0
After B8ZS	0	0	0	V	B	0	V	B

Table 3. HDB3 Substitution Code

Before HDB3	0	0	0	0
After HDB3	X	0	0	V

The receiver line-format interface processing is complementary to the transmitter processing. Input pulses on RPDN and RNDN, also active low, become binary ones (1s) on the TDM output bit stream; missing pulses become binary zeros. In the B8ZS and HDB3 modes, the processing circuit recognizes valid violation codes and replaces them with the correct number of binary zeros.

Frame Format Processing

Frame format refers to the organization of information as it is time-division multiplexed within the transmitted signal. The common elements in DS1 and CEPT frame-format structures are the 8-bit word or time slot and the 125 μs frame.

In the DS1 structure, a frame contains 24 words (192 bits) preceded by one framing bit. A superframe contains 12 frames and an extended superframe 24, as illustrated in Figure 3. When robbed-bit signaling is used, the superframes identify frames 6, 12, 18 and 24, which contain signaling information. The 229CG Framer supports four DS1 TDM frame formats: D4 channel bank (D4), *SLC* 96 Carrier System (SL), extended superframe (ESF), and digital data system (DDS) T1 digital multiplexer (T1DM).

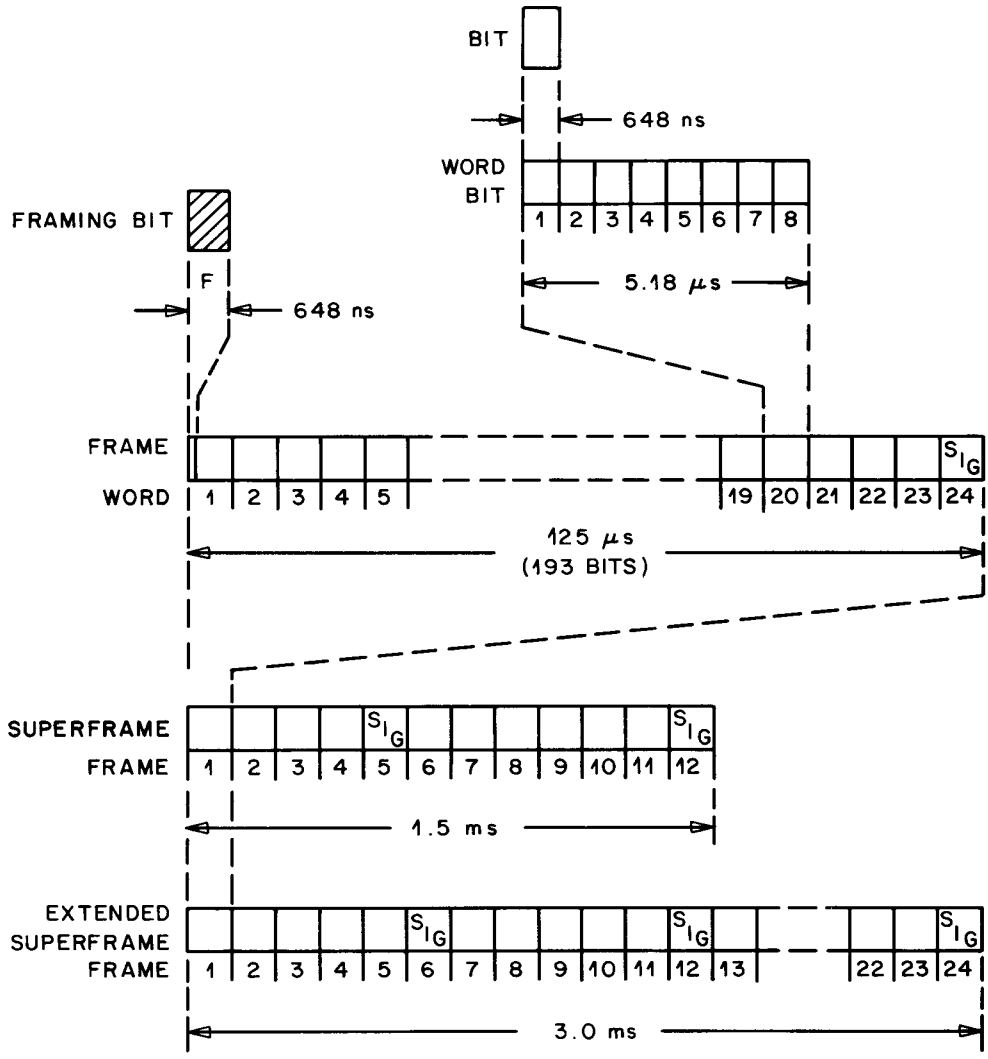


Figure 3. DS1 Frame-Format Structure

In the CEPT structure, a frame consists of 32 time slots (256 bits). In each frame, time slot 0 (TS0) is reserved for frame-alignment and control information, while time slot 16 (TS16) may be used for per-channel signaling (PCS) information. In the latter case, TS16 is formatted in a 16-frame multiframe. Figure 4 illustrates the basic CEPT frame-format structure. The 229CG Framer supports the common-channel signaling (CCS) mode, the per-channel signaling phase 0 (PCS0) and phase 1 (PCS1) modes, and the CEPT remote-switching module (IRSM) mode. The CCS mode is used when TS16 does not contain a PCS channel; otherwise, the PCS0 and PCS1 modes are used. Phase 0 means that the transmitter will align the TS16 Multiframe-Alignment Signal (MAS) word with the TS0 frame alignment signal (FAS) word. In the PCS1 mode, the transmitter aligns the MAS word with the TS0 Not word.

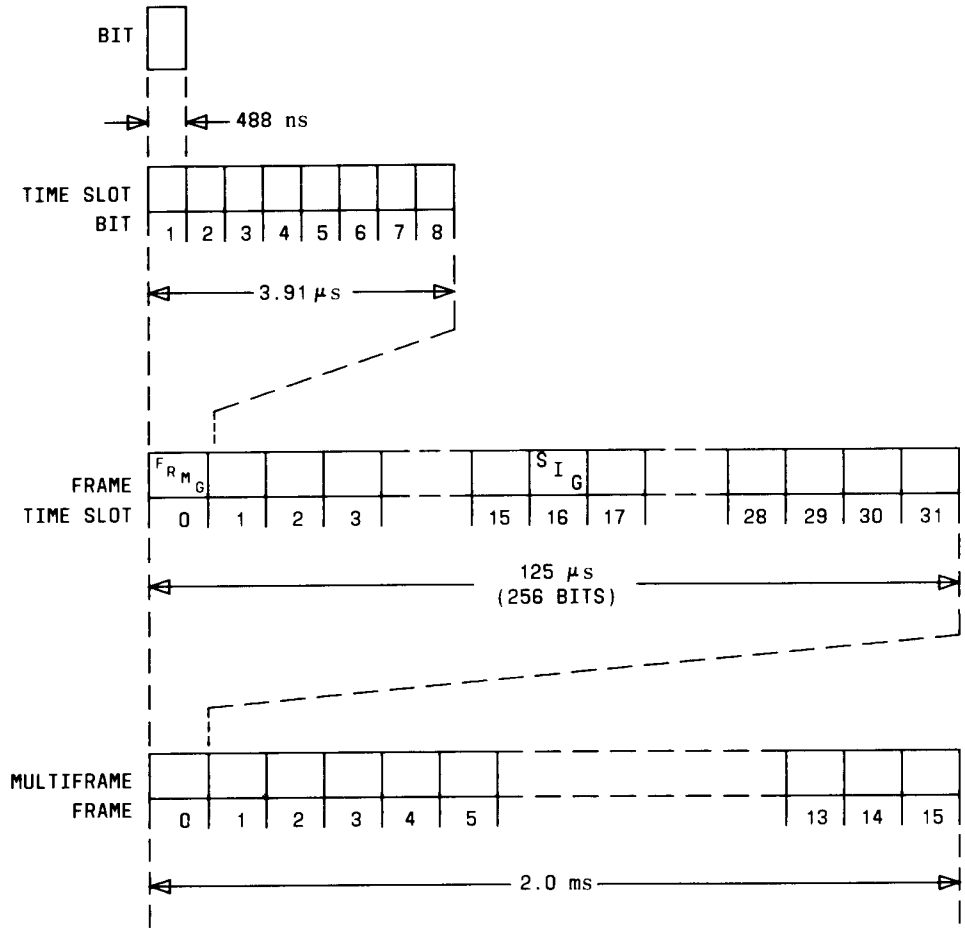


Figure 4. CEPT Frame-Format Structure

Table 4 lists the DS1 TDM Formats and Table 5 lists the CEPT TDM formats supported by the 229CG Framer. The designated symbols defined in Tables 4 and 5 represent the format in this document.

There are two levels of frame format interface processing: data-level and frame-level. Data-level processing overwrites bits in specified data words, time slots, or the facility data link (FDL) with new information. Frame-level processing affects the framing bits, word 24 in the DDS mode, and TS0 in the CEPT modes.

Table 4. DS1 TDM Frame Formats

DS1 TDM Format	Designated Symbol	Signaling-Bit Identification
D4 Channel Bank	D4	12-Frame Superframe
SLC 96 Carrier	SL	12-Frame Superframe
Extended Superframe	ESF	24-Frame Superframe
DDS T1DM	DDS	No Signaling

Table 5. CEPT Frame Formats		
CEPT TDM Format	**Designated Symbol**	**Signaling-Bit Identification**
Common Channel Signaling	CCS	No Signaling
Per-Channel Signaling	PCS0, PCS1	16-Frame Multiframe
CEPT RSM	IRSM	16-Frame Multiframe

Data-Level Processing. The 229CG Framer operation is transparent to message channels and to embedded or formatted signaling bits. However, it has the capability to overwrite certain bits in channel words. The majority of this type of processing is for consequent actions, i.e., inserting remote alarms or squelching the data with specific bit patterns in response to detected trouble conditions. Consequent action capabilities are discussed in **Responses to Facility Trouble and Alarms.**

An additional data-level processing capability is DS1 zero-code suppression (ZCS). ZCS may be implemented when the ls density requirements are not met transparently (e.g., with B8ZS). It consists of setting bit 7 to 1 in any word to be transmitted that contains all 0s. The 229CG Framer must apply ZCS or squelch patterns to all words simultaneously. Table 6 defines the specific ZCS and maintenance patterns.

Table 6. DS1 ZCS and Maintenance (Squelch) Patterns										
Words 1—24	**Format**	**Location**	**B1**	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**
ZCS	DS1 Non-DDS	XMTR	0	0	0	0	0	0	1	0
Idle Code	DS1 Non-DDS	XMTR	0	1	1	1	1	1	1	1
UC Code	DDS	XMTR	0	0	0	1	1	0	0	0
MOS Code	DDS	RCVR	0	0	0	1	1	0	1	0
AIS Code	Non-DDS	RCVR	1	1	1	1	1	1	1	1

The transmitter also generates two types of remote alarms: remote frame alarm (RFA), i.e., yellow alarm, and remote multiframe alarm (RMA). Table 7 defines the remote alarms.

Table 7. Remote Alarms		
Alarm Format	**Definition**	
RFA	D4	Bit 2 of all words in each frame cleared (0).
	DDS	Bit 6 of word 24 in each frame cleared (0).
	SL	Not processed by the 229CG
	ESF	An alternating pattern of eight 1s and eights 0s on the FDL.
RMA	CEPT	Bit 6 of TS16 MAS word = 1.

Squelch patterns and remote alarms may be turned on by explicit external order or may be enabled for automatic activation; ZCS is activated only by external order. In cases where simultaneous squelch and remote alarm patterns affect the same bit, the remote alarm takes precedence. The B8ZS option overrides the ZCS option.

Patterns inserted by the transmitter appear in the dual-rail bipolar output signal; patterns inserted by the receiver appear on the RID and RFD leads.

Frame-Level Processing. Frame-level processing affects the framing bits, the DDS word-24 pattern and the CEPT FAS word, MAS word, and Not word. A pseudorandom pattern (PRP) is embedded for maintenance purposes in the input data on TID and the output data on RID in all modes. In the DS1 mode, the pattern repeats in the framing bit positions at 24-frame intervals; in the CEPT mode, it repeats in bit 3 of TS0 at 16-frame intervals. The CEPT pattern is a truncated version of the DS1 pattern.

At the dual-rail bipolar inputs and outputs, the DS1 framing bit positions contain the standard framing, data-link, and CRC bits as defined in Table 8. Additional DS1 framing information is contained in word 24 in the DDS mode (Table 11). TS0 in the CEPT mode contains FAS, RFA, and control bits as shown in Table 9.

The transmitter has several functions in frame-level processing. In the DS1 mode, it checks the PRP in the TDM input and checks the superframe F-bit (Fs) sequence in the *SLC* Carrier FDL input for errors. It generates the Ft and Fs or Fe bits in the D4, DDS, and ESF modes, and both generates the Ft pattern and synchronizes to the Fs pattern on the FDL input in the SL mode. The transmitter generates and inserts the ESF CRC-6 check bits as required and copies the *SLC* Carrier and ESF FDL input data (D) to the FDL bits.

The receiver synchronizes to the Ft and Fs or Fe bits. It then checks the Ft, Fs or Fe, and CRC-6 check bits for errors. The *SLC* Carrier and ESF FDL bits are copied to the FDL output. The receiver inserts the PRP in the TDM output. Table 5 summarizes the assignment of DS1 framing bits.

In CEPT modes, the transmitter inserts the FAS pattern in the TS0 FAS word, inserts the spoiler bit (bit 2 = 1) in the TS0 Not word, manages the I and N control bits in TS0, and manages the X control bits in TS16 (when used). The receiver overwrites bit 3 of TS0 with the PRP and manages the X control bits in TS16 (when used).

Table 8. DS1 Framing Bit Assignments

DDS, D4, SL			ESF			
FRs	Ft	Fs or FDL	FRe	FDL	CRC	Fe
1	1		1	D		
2		0 or D	2		C1	
3	0		3	D		
4		0 or D	4			0
5	1		5	D		
6		1 or D	6		C2	
7	0		7	D		
8		1 or D	8			0
9	1		9	D		
10		1 or D	10		C3	
11	0		11	D		
12		0 or D	12			1
1	1		13	D		
2		0 or D	14		C4	
3	0		15	D		
4		0 or D	16			0
5	1		17	D		
6		1 or D	18		C5	
7	0		19	D		
8		1 or D	20			1
9	1		21	D		
10		1 or D	22		C6	
11	0		23	D		
12		0 or D	24			1

Table 9. CEPT TS0 Bit Assignments

FAS Word	I	0	0	1	1	0	1	1
Not Word	I	RFA	1	N0	N1	N2	N3	N4

The 229CG Framer provides two options for handling the I, N, and X control bits: transparent and nontransparent. In the nontransparent mode, the transmitter sets all control bits to binary ones (1s) and the receiver ignores all control bits. In the transparent mode, the transmitter expects to receive all control bits in TS0 on TID and the receiver returns all control bits in TS0 on RID. In the PCS mode, the transmitter transfers the X control bits from TS0 to TS16 and the receiver does the reverse transfer. To distinguish the FAS word from the Not word, the transmitter synchronizes to the alternating 0 and 1 pattern in bit 2 of TS0.

Table 10 shows the combined format of TS0 as seen on TID and RID. The dashes indicate bits that are irrelevant to the transmitter and receiver. Note that the X bits are updated at 2 ms intervals (every multiframe).

Table 10. Internal Time Slot 0 Format (Control-Bit Transparency)								
FAS Word	I	0	—	—	—	X0	X1	X2
Not Word	I	1	—	N0	N1	N2	N3	N4

The IRSM mode is a hybrid: the nontransparent mode is used for the I and X control bits, control bits N1 through N4 are treated transparently, and control bit N0 is used for the FDL.

Table 11 summarizes word-24 processing in the DDS mode. The transmitter sets the frame-alignment signal (FAS) to the correct pattern. It sets the remote frame alarm (RFA) bit to 1 for no alarm or clears (0) the RFA bit for the alarm. The transmitter copies the FDL input data, D, to the FDL bits in the DDS FDL mode and the receiver routes the FDL bit to the FDL output. The receiver synchronizes to the FAS pattern, while checking the FAS bits for errors. It checks the RFA bit for an alarm condition. The receiver overwrites the RFA bit with the logical OR of the current framing error and loss-of-frame alignment status.

Alignment and Synchronization

The 229CG Framer is responsible for determining alignment in the received and transmitted signals. The two types of signals used to establish alignment are bit sequences and bit patterns. Bit sequences are composed of individual bits spaced at frame or multiple-frame intervals. Bit patterns are multiple bits in one frame. Table 12 contains the bit sequences and patterns used to establish alignment.

The terminal-frame (Ft) and superframe (Fs) sequences alternate in the F-bit positions. The SL Fs bits occur only in 2 out of every 6 superframes. Frame and superframe alignment is established simultaneously by the ESF Fe bits. The DDS and CEPT frame-alignment signals (FAS) provide fast frame synchronization.

Table 11. Word 24 Bits Processed in the DDS Mode								
Word 24	**B1**	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**
FAS	1	0	1	1	1	—	—	0
RFA	—	—	—	—	—	0/1	—	—
FDL	—	—	—	—	—	—	D	—

Table 12. Bit Sequences and Patterns Used to Establish Alignment				
Name	**Format**	**Location**	**Pattern**	**Alignment**
Ft Bits	Non-ESF	Every 2nd F bit	01	Frame
Fs Bits	D4 & SL	Every 2nd F bit	001110	Superframe
Fe Bits	ESF	Every 4th F bit	001011	Frame, Superframe
FAS	DDS	Every word 24 bits 1—5, 8	101110	Frame
PRP	All DS1	Every F bit (bits 2 to 8)	0xF8DD42	Interdevice
FAS	CEPT	Every FAS word	0011011	Frame
FAS	CEPT	Every Not word (bit 2)	1	Frame
PRP	CEPT	Every TS0 (bit 3)	0xF8DD	Interdevice

Interdevice Synchronization

The 229CG Framer internal timing generators provide external 24-frame syncs (TISYN and RISYN) for interdevice synchronization. These syncs define the phase of the TDM signals on TID and RID, respectively. Normally, the transmitter is locked in frame synchronization to the input system sync pulse (SSYN), but has arbitrary superframe or multiframe phase. In the SL mode, however, the transmitter is forced to synchronize to the transmit FDL input on TFD because this data stream has the Fs-alignment sequence embedded in it. The receive interdevice sync is locked to the frame and superframe/multiframe phase determined by the receive alignment synchronizer.

Interdevice syncs identify frame and superframe alignment; they also define the phase of the interdevice PRP embedded in the framing bit positions. The relation of the PRP to the DS1 frame and superframe patterns is shown in Table 13.

Link Synchronization

When a loss-of-frame alignment (LFA) condition is detected in the receiver, the alignment synchronizer activates, but the normal receiver functions continue to operate at the previously determined frame alignment. After the synchronization circuit determines that a new alignment is required, the receiver circuits are forced to that new alignment. The defensive mode of the synchronization circuit inhibits realignment when repetitive data patterns emulate the frame-alignment signal (FAS) pattern. Synchronization cannot occur until all emulators disappear and only

In the ESF mode only, an on-line search procedure starts when an emulator has inhibited synchronization for 100 ms. The synchronization circuit selects one of the multiple candidate positions and checks for a correct CRC-6 pattern at this time. If the CRC-6 pattern does not match, the next candidate position is tried. The procedure repeats until the correct position is found. Each CRC-6 check takes 100 ms and each synchronization attempt takes an additional 100 ms.

When there are no emulators, the internal memory needed to implement the defensive algorithm leads to very fast synchronization; however, to avoid false reframes, the search does not end until at least 24 FAS-bit positions have been examined.

In the DS1 D4, SL modes and in the CEPT PCS modes, signaling-frame synchronization is performed off line, but no special defensive or fast algorithms are used. The D4/SL synchronization uses the standard D4 algorithm, while the PCS synchronization conforms to CCITT standards. Signaling-frame synchronization is not required in the DDS mode and is accomplished concurrently with terminal-frame synchronization in ESF mode. It is accomplished by a separate Fs resynchronizer in the D4 and SL modes and a separate multiframe resynchronizer in the CEPT modes.

Table 13. DS1 Interdevice Alignment

Bits	Bit Sequence*
Ft	1x0x1x0x1x0x1x0x1x0x1x0x
Fs	x0x0x1x1x1x0x0x0x1x1x1x0
Fe	xxx0xxx0xxx1xxx0xxx1xxx1
Fm	xxxxxxxxxxxxxxxxxxxxxxxx
PRP	111110001101110101000010

*x = don't care.

Tables 14—17 summarize the mean times and criteria for loss and recovery of alignment.

Table 14. Mean Recovery-of-Alignment Time

Alignment	Format	Mean Time*
Frame	DDS	0.75 ms
	D4 & SL	6 ms
	CEPT	1 ms
Superframe	D4-Ft/Fs	4.5 ms
	SL	21 ms
Frame/Superframe	ESF	12 ms
Multiframe	CEPT	2 ms

*Assumes no line errors and no emulators.

Table 15. Recovery-of-Alignment Criteria

Alignment	Format	Recovery Indication	Recovery Criterion
Frame	DDS	LFA off	The first unique correct combination of an Ft/Fs sequence and FAS pattern that exists for at least six consecutive frames.
	D4-Ft	LFA off	The first unique correct Ft sequence that exists for at least 24 consecutive Ft intervals (48 frames).
	D4-Ft/Fs & SL	None	The first unique correct Ft sequence that exists for at least 24 consecutive Ft intervals (48 frames).
	ESF	LFA off	The first unique correct Fe sequence that exists for at least 24 consecutive Fe intervals (96 frames).
Superframe	D4 & SL	LFA off	The first correct Fs sequence that exists for 2 consecutive superframes.
Extended Superframe	ESF	LFA off	Recovery-of-frame alignment.
Multiframe	CEPT	LMA off	The first correct instance of an MAS pattern that exists for 2 consecutive multiframes.

Table 16. Mean Loss-of-Alignment Time			
Alignment	Format	Mean Time*	
		True (max)	False (min)
Frame	DDS	–	–
Frame/Superframe	D4 & SL	1.1 ms	1.4 min
	ESF (LFA)	2.1 ms	2.8 min
	ESF (LCC)	96 ms	132 ms
Multiframe	CEPT	4 ms	2.1 min

*Max times are for a 0.5 error rate. Min times are for a 0.001 error rate.

Table 17. Loss-of-Alignment Criteria			
Alignment	Format	Loss Indication	Loss Criterion
Frame	DDS	LFA on	4 FERs in 12 consecutive frames
	D4 & SL	LFA on	2 FERs in 4 consecutive Ft bits
	ESF	LFA on	2 FERs in 4 consecutive Fe bits
Superframe	D4 & SL	LFA on	Loss-of-frame alignment
Frame/Superframe	ESF	LFA on	32 consecutive CERs (LCC)
Multiframe	CEPT	LMA on	2 consecutive MAS errors or TS16 = 0 in 2 consecutive multiframes

Recovery time calculations assume no line error. True loss-of-alignment time calculations assume a 0.5 error rate; false loss-of-alignment time conditions assume a 10^{-3} error rate. See Table 19 for definitions of FER, CER, LFA, LMA, and LCA.

Facility Trouble and Alarm Processing

Fault and Alarm Detection

The criteria used to detect transmission-facility faults and alarms fall into two categories: events and conditions. Event criteria activate the fault or alarm indication for each separate occurrence of the event. Condition criteria require algorithmic processing of a number of events to activate the fault or alarm indication. The indication persists until deactivated by a different event. Table 18 lists the event-activated faults and alarms detected by the 229CG Framer.

With the exception of LFVs and RFAs, all event indications remain activated for one frame (125 μs). LFV indications remain activated for one TDM bit interval (648 ns DS1 and 488 ns CEPT), while RFA indications remain activated until the following RFA event slot (125 μs DDS/D4 and 250 μs CEPT). The 229CG Framer does not recognize RFA for *SLC* 96 Carrier.

Table 19 lists the fault and alarm conditions detected by the 229CG Framer. Condition indications remain activated for the duration of the condition. The receive signaling inhibit (RSI) fault indication on report lead RSI is a special case. It is the logical OR of FER, LFA, and LMA (in the PCS and IRSM modes) and is used by the 257AU receive synchronizer to prevent false signaling interpretations.

Table 18. Transmission-Facility Fault and Alarm Events			
Name	**Symbol**	**Format**	**Activation Criterion**
Line-format Violations	LFV	Bipolar/AMI	Any BPV.
		B8ZS/HDB3	Any BPV not in a valid violation code.
Frame-Alignment Error	FER	D4 & SL	An error in an Ft bit.
		ESF	An error in an Fe bit.
		DDS	An error in an Ft, Fs or word-24 FAS bit.
		CEPT	An error in a TS0 FAS bit.
Change-of-Frame Alignment	CFA	All	Synchronization at a new frame alignment.
CRC-6 errors	CER	ESF	One or more CRC-6 check bits in error in any extended superframe.
Remote Multiframe Alarm	RMA	PCS/IRSM	Bit 6 of TS16 MAS word = 1.
Remote Frame Alarm	RFA	DDS	A word 24 bit 6 RFA bit = 0.
		D4	Bit 2 of all words in one frame = 0.
		CEPT	Bit 3 of TS0 Not word = 1.
Alarm Indication Signal	AIS	All	Less than 3 zeros in a two-frame interval.

Table 19. Transmission-Facility Fault and Alarm Conditions			
Name	**Symbol**	**Format**	**Activation Criterion**
Loss-of-Frame Alignment	LFA	DDS	4 FERs in 12 consecutive frames.
		D4 & SL	2 FERs in 4 consecutive Ft bits.
		ESF	2 FERs in 4 consecutive Fe bits.
		CEPT	3 or 4 consecutive FERs (optional)
Loss-of-Multiframe Alignment	LMA	PCS/IRSM	2 consecutive MAS errors or TS16 = 0 in 2 consecutive multiframes.
Remote Frame Alarm	RFA	ESF	A repeating 0x00FF pattern in the FDL after an initial 0x00 or 0xFF start-up sequence.

Responses to Facility Trouble and Alarms

Consequent action is a CCITT term that covers responses to the detection of trouble or alarm conditions. The 229CG Framer provides two types of consequent actions: demand and automatic. Demand consequent actions are invoked by external command only; automatic consequent actions are hardware-implemented responses triggered by the detection of specific events or conditions. There are two categories of automatic consequent actions: standard and optional. Standard actions are mandatory; optional actions may be enabled or disabled by external command. Table 20 summarizes the consequent action capabilities of the 229CG Framer.

Table 20. Demand Consequent Actions Capabilities			
Name	**Symbol**	**Format**	**Action**
Receive Signaling Inhibit	RSINH	All	RSI output lead set to 1
Transmit TDM Squelch	XCHSQ	DDS	T1DM UC Code to words 1—23
		Other DS1	Idle Code to all words
		CEPT	AIS to TS1 through TS31
Transmit RFA	XRFAL	DDS	All word 24 bit 6 RFA bits = 0
		D4	Bit 2 of all words = 0
		ESF	Repeating 0x00ff pattern to FDL
		CEPT	Bit 3 of not word = 1
Transmit RMA	XRMAL	CEPT	Bit 6 of MAS word = 1
Receive TDM Squelch	RCHSQ	DDS	T1DM MOS Code to words 1—23
Receive TS16 Squelch	RSGSQ	CEPT	AIS to TS16

In DS1 modes, consequent actions are activated via a control byte input on SCS. In CEPT modes, however, the CCITT (Consultative Committee for International Telephone and Telegraph) recommends a fast response to certain facility fault conditions. Accordingly, automatic fast responses may be enabled on an optional basis by an SCS consequent-action enable byte. Table 21 summarizes the automatic consequent actions.

Table 21. Automatic Consequent Actions			
Action	**Format**	**Trigger**	**Type**
RSINH	All	FER, LFA	Standard
	PCS, IRSM	LMA	
RCHSQ	CEPT	LFA	Optional
RSGSQ	PCS/IRSM	LMA	Optional
XRFAL	CEPT	LFA	Optional
XRMAL	PCS/IRSM	LMA	Optional

The receiver side of the 229CG Framer activates receive signaling inhibit (RSIGN) for a one-frame interval after each detected FER and/or MER and for the duration of each LFA and/or LMA condition.

Each time a signaling bit is received, the receive synchronizer transfers that bit's previous value to backup storage. When the RSI lead is set (1) (RSINH activated), the receive synchronizer freezes the signaling states at the backup values and maintains this state for 32 frames after the RSI lead returns to 0 (RSINH deactivated).

The RSGSQ capability is a means of passing on the RSINH function in applications that do not use the signaling extraction capabilities of the receive synchronizer.

System Status Monitoring

Device Duplication and Match Alarms

The principal technique used for internal device-fault monitoring is duplication and match circuitry. This technique checks output signals for internally generated errors and checks synchronizers and facility-monitor detectors for algorithm failures. Table 22 lists the 229CG Framer duplication and match operations. Table 23 lists the interface signal checks performed by the framer.

Table 22. Device Duplication and Match Alarms

Symbol	Format	Activation Criterion
TDNMM	All	Transmit TDM output data mismatch.
TFDCMM	SLC/DDS/ESF/IRSM	Transmit FDL output clock mismatch.
RIDMM	All	Receive TDM output data mismatch.
RFDMM	SLC/DDS/ESF/IRSM	Receive FDL output data mismatch.
RFDCMM	SLC/DDS/ESF/IRSM	Receive FDL output clock mismatch.
RSSPMM	D4 & SL	Receive superframe synchronizer pulse mismatch.
LFVDMM	All	LFV detector output mismatch.
FERDMM	All	FER detector output mismatch.
LMADMM	All	LMA detector output mismatch.
RMADMM	All	RMA detector output mismatch.
RFADMM	All	RFA detector output mismatch.
AISDMM	All	AIS detector output mismatch.

Table 23. Device Interface Fault-Condition Alarms

Symbol	Format	Activation Criterion
TPRPER	All	Transmit pseudorandom pattern error on TID.
TLOSA	SL	Transmit loss-of-superframe alignment on TFD.
TLOCLK	All	Transmit loss of-clock on TICLK.
RLOCLK	All	Receive loss of clock on RLCLK.
SCSPER	All	Control stream parity error on SCS.
TLOBA	CEPT	Transmit loss of TS0 biframe alignment on TID.

Diagnostic Exercises

The 229CG Framer provides a number of diagnostic exercises to ensure that the device can detect and/or report faults and alarms. These exercises fall into five categories. Exercises that do not affect service, 1—6, check the system-fault detection circuits without affecting normal operation. Facility-monitor-affecting exercises, 8, 9, and 13—15, check the facility-monitor circuits but do not affect normal data processing. The one data-processing-affecting exercise, 11, effectively forces the receiver input data stream to all zeros. The null exercise, 0, clears any other exercise and its responses. Exercises 7, 10, and 12 have no function. The response time for any exercise depends on the fault or alarm condition that it forces.

Table 24 lists the system-status exercises and their expected responses. Table 25 lists the facility status exercises and their expected responses. Two exercises are required to fully check most duplicate and match circuits. The response to an exercise that does not affect service and that checks a facility-monitor circuit may be inhibited when the corresponding facility fault or alarm indication is activated.

Table 24. System-Status Exercise Responses

Exercise	Format	Activated Response	
		Report Bits	Reported Condition
0	All	None	None (clears all fault and alarm indications)
1	All	SR1, SR2	TLOCLK, LFVDMM
	All	SR3, SR4[1]	FERDMM, RFADMM
	Non-D4 DS1/IRSM	SR5, SR7[2]	TFDCMM, TDNMM
2	All	SR1, SR2	TLOCLK, LFVDMM
	All	SR3, SR4[1]	FERDMM, RFADMM
	Non-D4 DS1/IRSM	SR7[2]	TDNMM
3, 4	CEPT Transparent	SR0	TLOBA
	All	SR1	TLOPRP
	All	SR3[3], SR4	LMADMM, RMADMM
	All	SR7	TDMNN
5	All	SR1	RLOCLK
	All	SR3	RSSPMM
	All	SR4	AISDMM
	All	SR5	RFDCMM
	Non-D4 DS1/IRSM	SR6[2]	RFDMM
	All	SR7	RIDMM
6	All	SR1	RLOCLK
	All	SR3	RSSPMM
	All	SR4	AISDMM
External	SL	SR0[4]	TLOSA
	All	SR2[5]	SCSPER

[1]May not respond if exercised during an RFA condition.
[2]May not respond if exercised while the FDL is inactive.
[3]May not respond if exercised during an LMA condition.
[4]TLOSA may be exercised by sending an incorrect Fs pattern to the FDL.
[5]SCSPER may be exercised by sending bad parity on the SCS.

Table 25. Facility-Status Exercise Responses Non-BOS Modes				
		Activated Response		
Exercise	Format	Report Bit	Report Lead	Reported Condition
0	All	None	None	None
8	All	FR0	RLV	LFV
	ESF	FR4	RCEMA	CER
	ESF	FR5	None	LCC*
	D4 & DDS	FR6	RRFMA	RFA
	ESF	FR6	RRFMA	CRFA
9	PCS/IRSM	FR5	RRFMA	AIS
	CEPT	FR6	RRFMA	RFA
	All	FR7	None	AIS
11	All	FR1	RFE	FER
	All	FR2	RLF	LFA
	ESF	FR4	RCEMA	CER
	PCS/IRSM	FR4	RCEMA	LMA
	D4 & DDS	FR6	RRFMA	RFA
	All	None	RSI	FER, LFA, LMA
13	All	FR1	RFE	FER
	All	FR2	RLF	LFA
	PCS/IRSM	FR4	RCEMA	LMA
14	All	FR1	RFE	FER
	All	FR2	RLF	LFA
	DDS, ESF, & CEPT	FR3	None	CFA
	PCS/IRSM	FR4	RCEMA	LMA
15	ESF	FR3*,**	None	CFA
	ESF	FR5	None	LCC

*Response may require more than 150 ms to activate.
**Response activates only if an FAS emulator is present.

Control and Status

Serial Control Stream

Control and maintenance commands to the 229CG Framer are input on SCS at a 1.024 Mb/s rate. The commands are organized into groups of 8-bit bytes and are accepted on SCS when CTLE is held high. The last eight bits entered are stored as a command byte; preceding bits are ignored. Once a command has been entered, it remains in effect until explicitly changed. Command bytes may have arbitrary phase in relation to system sync (SSYN). Control bytes consist of four types: option, exercise, consequent action, and action control bytes. Figure 5 illustrates the bit assignments for each control type.

As illustrated on Figure 5, each control byte consists of eight bits, labeled CB0 (LSB) to CB7 (MSB). CB7 is a parity bit that forces odd parity across the entire byte. Control bits 4, 5, and 6 (CB4—CB6) determine the control byte type.

An option byte is selected when CB6 = 0. For this byte, bit positions CB0—CB5 are relabeled OP0—OP5, respectively, and are used to select individual 229CG Framer options. DS1 mode is selected when OP0 is low and the remaining option bits, OP1—OP5, are used to select line-format and frame-format structures as listed in Table 26. CEPT mode is selected when either OP0 = 1 and/or OS0 is set (1). CEPT mode options are listed in Table 27. In CEPT mode, the OS0—OS5 option select leads control the same options listed in Tables 26 and 27 for the respective bit positions OP0—OP5. Although the selected option is determined by the logical OR of the two possible sources of option selections, only one source for option selection should be used.

In CEPT mode, OP2 determines the loss-of-frame alignment error condition. When OP2 = 1, three consecutive frame-alignment signal errors activate a loss-of-frame alignment signal (LFA) error. When OP2 = 0, four consecutive frame-alignment signal errors are required before an LFA error is reported.

In the DDS-TDM mode, FDL processing is inactive; in the DDS-FDL mode, FDL data is copied to and from word 24/bit 7.

Tables 28, 29, and 30 list the exercise, consequent action, and action control bit assignments.

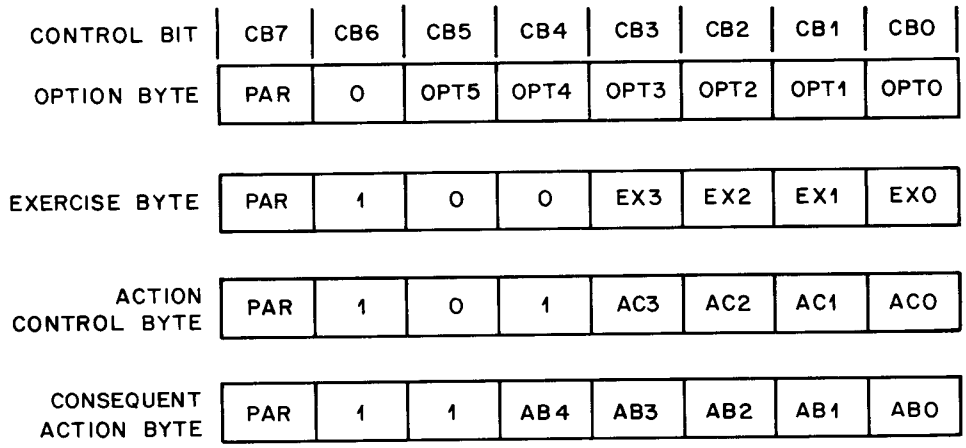


Figure 5. Control Byte Formats

Table 26. DS1 Option-Byte Bit Assignments (OP0=0)

OP5*	OP4*	OP3*	OP2*	OP1*	OP0*	Word 24	ZCS	Line Format	Frame Format
x	x	0	x	x	0	Transparent	—	—	—
x	x	1	x	x	x	DDS FAS Word	—	—	—
x	x	x	0	0	x	—	Off	—	—
x	x	x	1	0	x	—	On	—	—
x	x	x	x	0	x	—	—	Bipolar	—
x	x	x	x	1	x	—	—	B8ZS	—
0	0	0	x	x	x	—	—	—	D4
1	0	0	x	x	x	—	—	—	SL
x	1	0	x	x	x	—	—	—	ESF
x	0	1	x	x	x	—	—	—	DDS-TDM
x	1	1	x	x	x	—	—	—	DDS-FDL

*x = don't care.

Table 27. CEPT Mode Option Bit Definitions (OP0 = 1)

OP5*	OP4*	OP3*	OP2*	OP1*	Line Format	FAS Errors	Frame Format	Control Bit Mode
x	x	x	x	0	AMI	—	—	—
x	x	x	x	1	HDB3	—	—	—
x	x	x	0	x	—	4	—	—
x	x	x	1	x	—	3	—	—
x	0	0	x	x	—	—	CCS	—
x	1	0	x	x	—	—	IRSM	—
x	0	1	x	x	—	—	PCS0	—
x	1	1	x	x	—	—	PCS1	—
0	x	x	x	x	—	—	—	Transparent
1	x	x	x	x	—	—	—	All 1's

*x = don't care.

Table 28. Exercise-Byte Bit Assignments				
EX3	EX2	EX1	EX0	Exercise Number
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
1	0	0	0	8
1	0	0	1	9
1	0	1	1	11
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 29. Demand Consequent-Action-Byte Bit Assignments										
					DS1			CEPT Mode		
AB4*	AB3*	AB2*	AB1*	AB0*	DDS/ESF	D4	SL	CCS	PCS	IRSM
x	x	x	x	1	RCHSQ	RCHSQ	RCHSQ	RCHSQ	RCHSQ	RCHSQ
x	x	x	1	x	RDLSQ	–	RDLSQ	–	RSGSQ	RSGSQ
x	x	1	x	x	XRFAL	XRFAL	–	XFRAL	XRFAL	XRFAL
x	1	x	x	x	XDLSQ	–	–	–	XRMAL	XRMAL
1	x	x	x	x	XCHSQ	XCHSQ	XCHSQ	XCHSQ	XCHSQ	XCHSQ

*x = don't care.

Table 30. Action-Control-Byte Bit Assignments						
AC3*	AC2*	AC1*	AC0*	Format	Action	Trigger
x	x	x	1	CEPT	RCHSQ	LFA
x	x	1	x	PCS/IRSM	RSGSQ	LMA
x	1	x	x	CEPT	XRFAL	LFA
1	x	x	x	PCS/IRSM	XRMAL	LMA

*x = don't care.

In the 229CG Framer, the action-control byte is used to control the optional automatic consequent actions. Bits AC0, AC1, and/or AC2 must be set (1) to enable the consequent actions. All unused bits should be initialized to 0.

Status Report Mechanisms. Facility fault and alarm reports are available on both the serial report stream bits (FR0—FR7) and on the external report leads. System status alarms are reported only on the report stream. For maintenance purposes, the report stream provides a means of auditing the contents of the device's internal control registers previously set by serial control commands and/or option select pins. The device outputs the serial report stream on SRS at a 1.024 Mb/s rate in fixed relation to system sync (SSYN).

A serial report stream contains the six report byte types illustrated on Figure 6. The six report bytes are organized into a serial report stream frame consisting of sixteen bytes, as illustrated on Figure 7.

A facility report byte is transmitted at the start of each frame. The next five bytes consist of a system status (device alarms) report, exercise audit, option audit, consequent action audit, and action control audit byte, respectively. Two null bytes, all 0s, are then transmitted, followed by the retransmission of the previous eight bytes. The lower-order bit is transmitted first for each byte output on SRS.

Table 31 lists the facility fault alarm bit status. Table 32 lists the system fault alarm bit assignments.

FACILITY ALARMS

BIT	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
BYTE 0	FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0

SYSTEM STATUS REPORT

BIT	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
BYTE 1	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

BYTE 2	EXERCISE AUDIT BYTE
BYTE 3	OPTION AUDIT BYTE
BYTE 4	CONSEQUENT ACTION AUDIT BYTE
BYTE 5	ACTION CONTROL AUDIT BYTE

Figure 6. Report Byte Formats

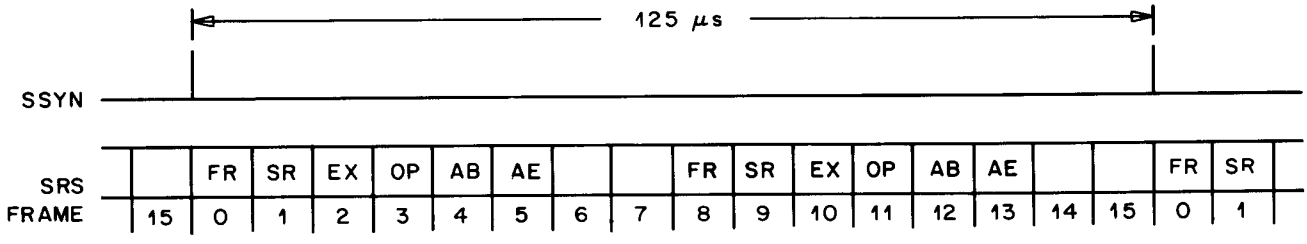


Figure 7. Serial Report Stream Frame-Format

Table 31. Facility-Status Report-Byte Bit Assignments									
FR7*	FR6*	FR5*	FR4*	FR3*	FR2*	FR1*	FR0*	Format	Report
x	x	x	x	x	x	x	1	All	LFV
x	x	x	x	x	x	1	x	All	FER
x	x	x	x	x	1	x	x	All	LFA
x	x	x	x	1	x	x	x	All	CFA
x	x	x	1	x	x	x	x	ESF	CER
								PCS/IRSM	LMA
x	x	1	x	x	x	x	x	ESF	LCC
								PCS/IRSM	RMA
x	1	x	x	x	x	x	x	D4 & DDS	RFA
								ESF	CRFA
1	x	x	x	x	x	x	x	All	AIS

*x = don't care.

Table 32. System-Status Report-Byte Bit Assignments									
SR7*	SR6*	SR5*	SR4*	SR3*	SR2*	SR1*	SR0*	Format	Report
x	x	x	x	x	x	x	1	SL	TLOSA
								CEPT	TLOBA
x	x	x	x	x	x	1	x	All	TPRPER, TLOCLK, RLOCLK
x	x	x	x	x	1	x	x	All	SCSPER, LFVDMM
x	x	x	x	1	x	x	x	All	FERDMM
								D4 & SL	RSSPMM
								PCS/IRSM	LMADMM
x	x	x	1	x	x	x	x	All	AISDMM, RFADMM
								PCS/IRSM	RMADMM
x	x	1	x	x	x	x	x	Non-D4	TFDCMM, RFDCMM
x	1	x	x	x	x	x	x	Non-D4	RFDMM
1	x	x	x	x	x	x	x	All	TDNMM, RIDMM

*x = don't care.

The second report mechanism in the 229CG Framer is the dedicated report lead. Table 33 shows the assignment of facility fault and alarm reports to these leads.

Table 33. Facility-Status Report-Lead Assignments		
Report Lead	**Format**	**Report**
RLV	All	LFV
RFE	All	FER
RLF	All	LFA
RCEMA	ESF	CER
	PCS/IRSM	LMA
RRFMA	D4 &DDS	RFA
	ESF	CRFA
	PCS/IRSM	RFA, RMA
RSI	PCS/IRSM	FER, LFA, LMA
	All other	FER, LFA

CHARACTERISTICS

Clocks

Clock	Period	Tolerance	Unit	Duty Cycle*	Mode
RLCLK	648	100 ± 2%	ns	50 ± 5%	DS1
	488	100 ± 2%	ns	50 ± 5%	CEPT
TICLK	648	100 ± 1%	ns	50 ± 8%	DS1
	488	100 ± 1%	ns	50 ± 5%	CEPT
SCLK	244	100 ± 1%	ns	50 ± 5%	All
RFDCLK	125	—	μs	50 ± 1%	DDS
	250	—	μs	25 ± 1%	SL, ESF, IRSM
TFDCLK	125	—	μs	50 ± 1%	DDS
	250	—	μs	75 ± 1%	SL, ESF, IRSM

*Duty cycle = Zero-Level Duration / (Clock Period)*100.

Electrical Characteristics

T_A = 0 to 70° C, V_{DD} = 5 V ±5%, GRD = 0 V

Parameter		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	140	295	mA
Input Current	Low	I_{IL}	—	—	−20	μA
	High	I_{IH}	20	—	—	μA
Output Current	Low	I_{OL}	—	—	2.2	mA
	High	I_{OH}	—	—	0.2	mA
Input Voltage	Low	V_{IL}	—	—	0.7	V
	High	V_{IH}	2.4	—	—	V
Output Voltage	Low	V_{OL}	—	—	0.4	V
	High	V_{OH}	2.4	—	—	V
Power Dissipation		PD	—	0.7	1.4	W

Maximum Ratings

DC Supply Voltage Range (V_{DD}) ..... −0.5 to +7 V
Power Dissipation (PD) ..... 2 W
Storage Temperature Range (Tstg) ..... −40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit	Mode
tSCHTCH	Skew Time SCLK to TICLK	−122	10	142	ns	All
tSSHSSL	SSYN Pulse Duration	—	244	—	ns	All
tSSHTCH	Pulse Set-Up Time SSYN to TICLK	40	—	—	ns	All
tTCHSSL	Pulse Hold Time TICLK to SSYN	50	—	—	ns	All
tSSHSCH	Pulse Set-Up Time SSYN to SCLK	40	—	—	ns	All
tSCHSSL	Pulse Hold Time SCLK to SSYN	70	—	—	ns	All
tRPVRCH	Data Set-Up Time RPDN to RLCLK	200	—	—	ns	All

Symbol	Description	Min	Typ	Max	Unit	Mode
tRNVRCH	Data Set-Up Time RNDN to RLCLK	200	—	—	ns	All
tRCHRPX	Data Hold Time RLCLK to RPDN	200	—	—	ns	All
tRCHRNX	Data Hold Time RLCLK to RNDN	200	—	—	ns	All
tRCLRDV	Propagation Delay RLCLK to RID	0	—	140	ns	All
tRCLRSH	Propagation Delay RLCLK to RISYN	0	—	140	ns	All
tRCLRSL	Propagation Delay RLCLK to RISYN	0	—	140	ns	All
tTDVTCH	Data Set-Up Time TID to TICLK	124	—	—	ns	All
tTCHTDX	Data Hold Time TICLK to TID	124	—	—	ns	All
tTCLTSV	Propagation Delay TICLK to TISYN	0	—	140	ns	All
tTCHTPV	Propagation Delay TICLK to TPDN	0	—	190	ns	All
tTCHTNV	Propagation Delay TICLK to TNDN	0	—	190	ns	All
tTCHTLL	Propagation Delay TICLK to TLCLK	0	—	150	ns	All
tTCLTLH	Propagation Delay TICLK to TLCLK	0	—	150	ns	All
tRKLRFV	Skew Time RFDCLK to RFD	−4	0	4	µs	All
tTFVTKH	Data Set-Up Time TFD to TFDCLK	2	—	—	µs	All
tTKHTFX	Data Hold Time TFDCLK to TFD	2	—	—	µs	All
tCSVCSV	SCS Time-Slot Period	—	976	—	ns	All
tSRVSRV	SRS Time-Slot Period	—	976	—	ns	All
tCSVSCH	Data Set-Up Time SCS to SCLK	244	—	—	ns	All
tCEVSCH	Data Set-Up Time CTLE to SCLK	244	—	—	ns	All
tSCHCSX	Data Hold Time SCLK to SCS	244	—	—	ns	All
tSCHCEX	Data Hold Time SLCK to CTLE	244	—	—	ns	All
tSCHSRV	Propagation Delay SCLK to SRS	0	—	300	ns	All
tRCLRVV	Propagation Delay RLCLK to RLV	0	—	250	ns	All
tRCLREV	Propagation Delay RLCLK to RFECE	0	—	2	µs	All
tRCLRLV	Propagation Delay RLCLK to RLF	0	—	2	µs	All
tRCLRAV	Propagation Delay RLCLK to RCEMA	0	—	2	µs	All
tRCLRMV	Propagation Delay RLCLK to RRFMA	0	—	2	µs	All
tRCLRIV	Propagation Delay RLCLK to RSI	0	—	2	µs	All

Timing Diagrams

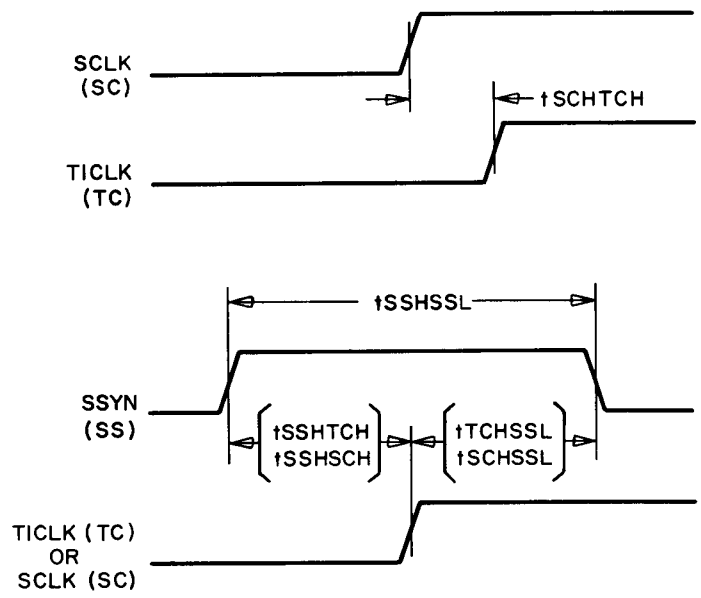


Figure 8. Clock Signals

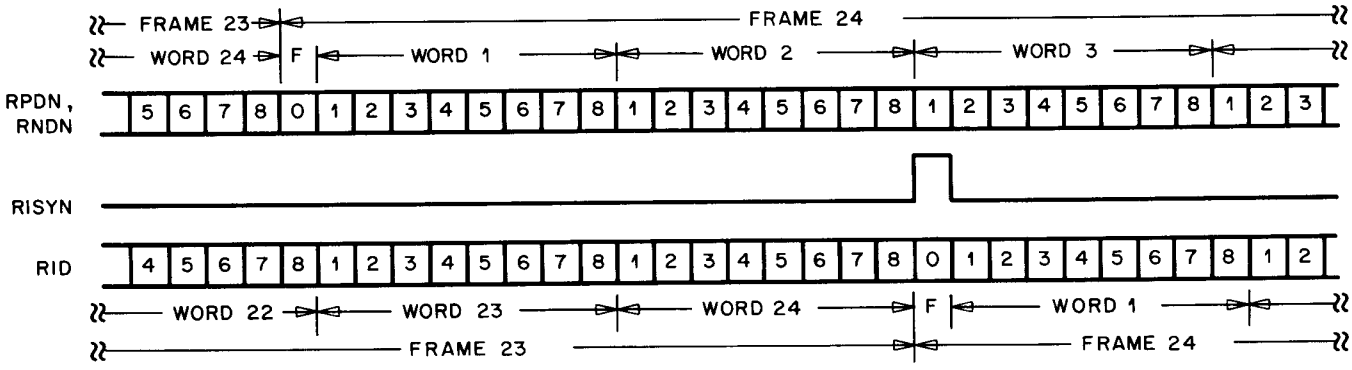


Figure 9. Receiver TDM Timing (DS1 Mode)

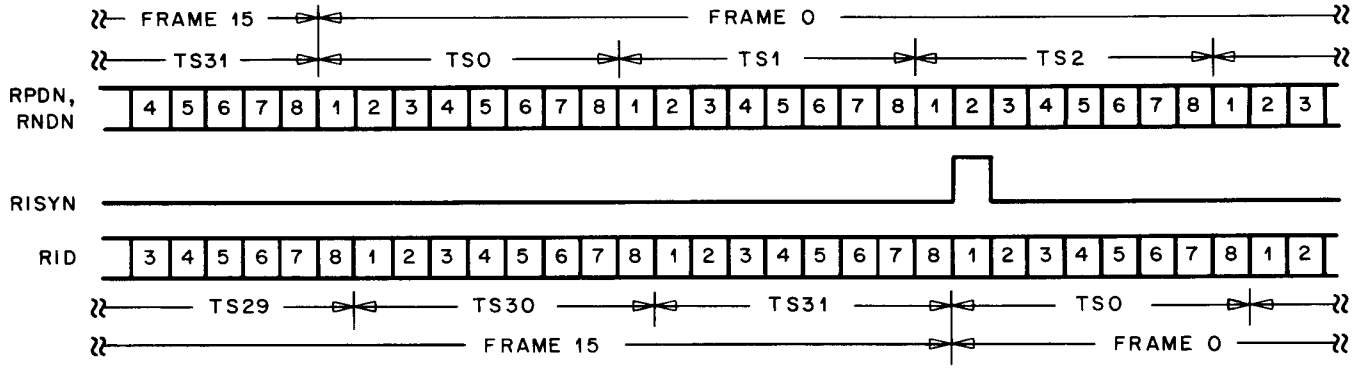


Figure 10. Receiver TDM Timing (CEPT Mode)

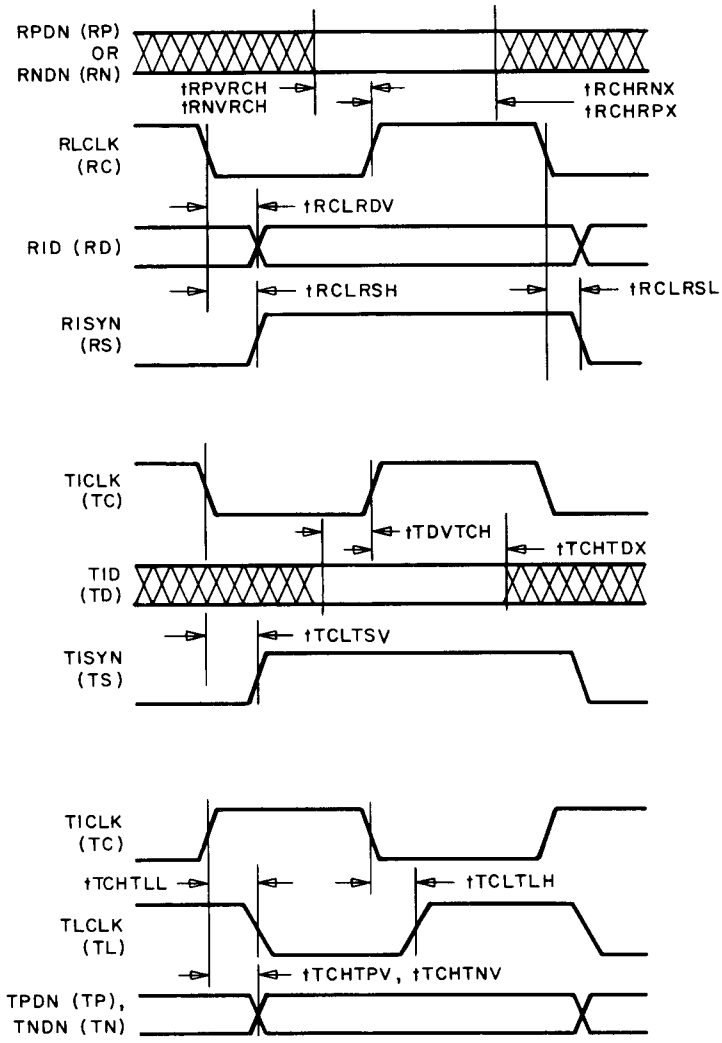


Figure 11. Line-Rate I/O Signals

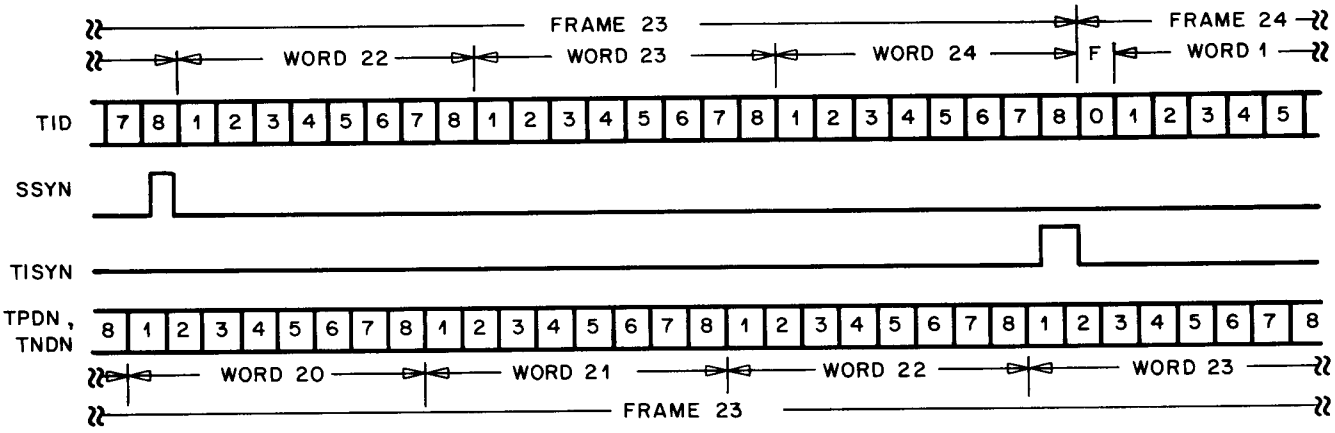


Figure 12. Transmitter TDM Timing (DS1 Mode)

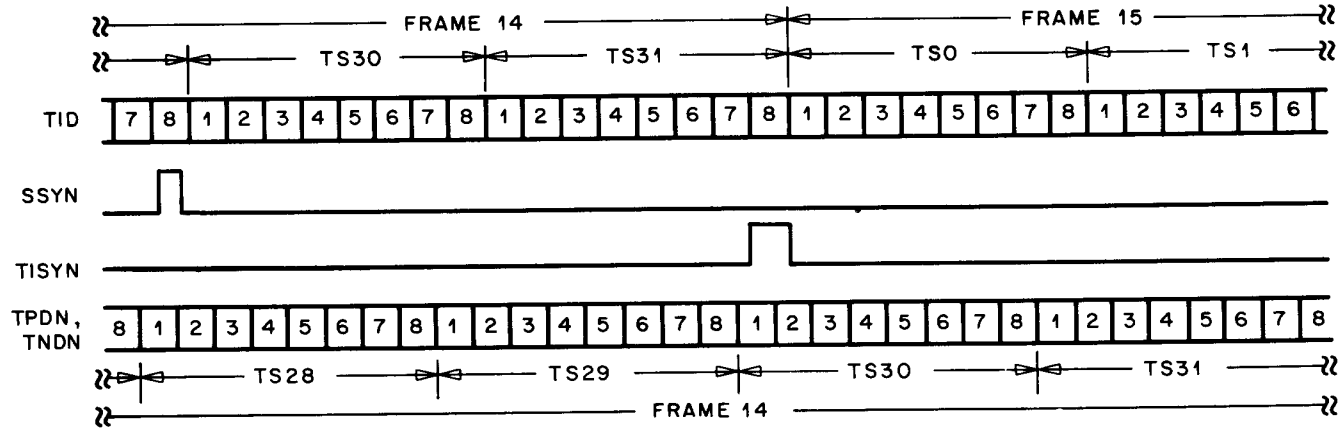


Figure 13. Transmitter TDM Timing (CEPT Mode)

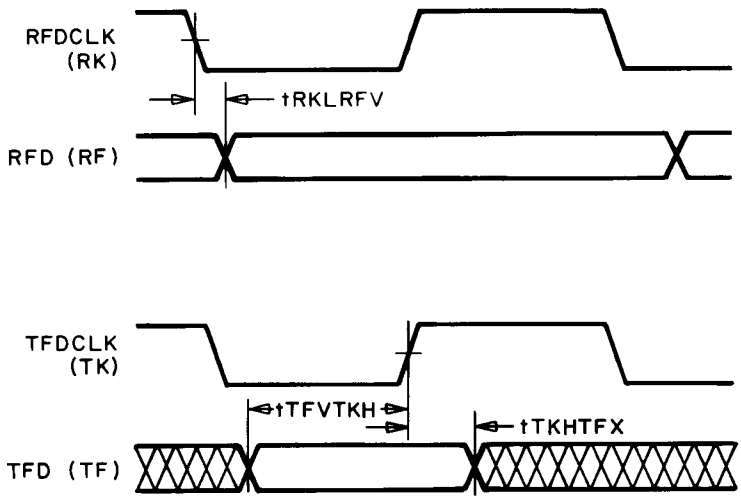


Figure 14. Facility Data Link Clocks and Data

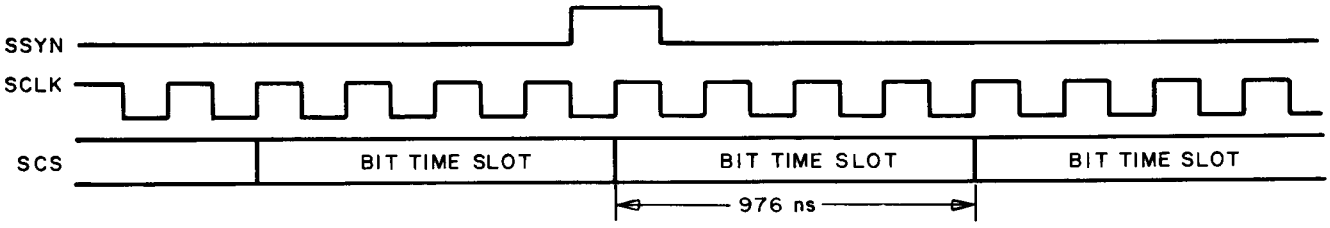


Figure 15. Serial Control Stream Bit Timing

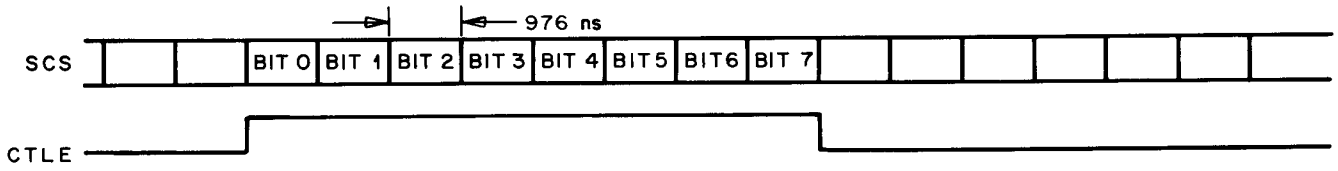


Figure 16. Serial Control Stream Byte Timing

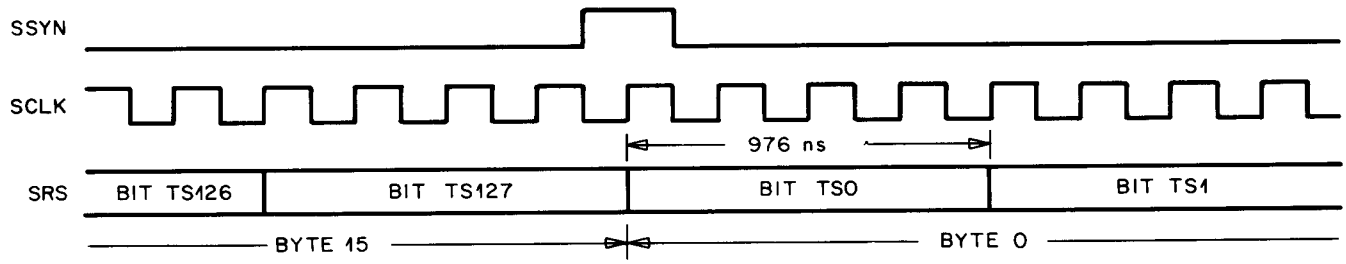


Figure 17. Serial Report Stream Bit Timing

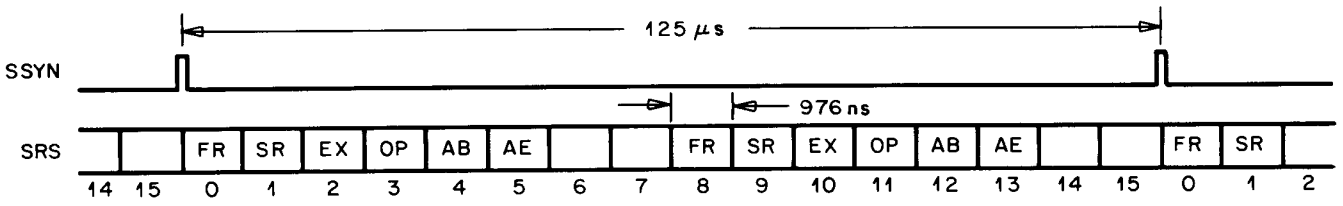


Figure 18. Serial Report Stream Frame Timing

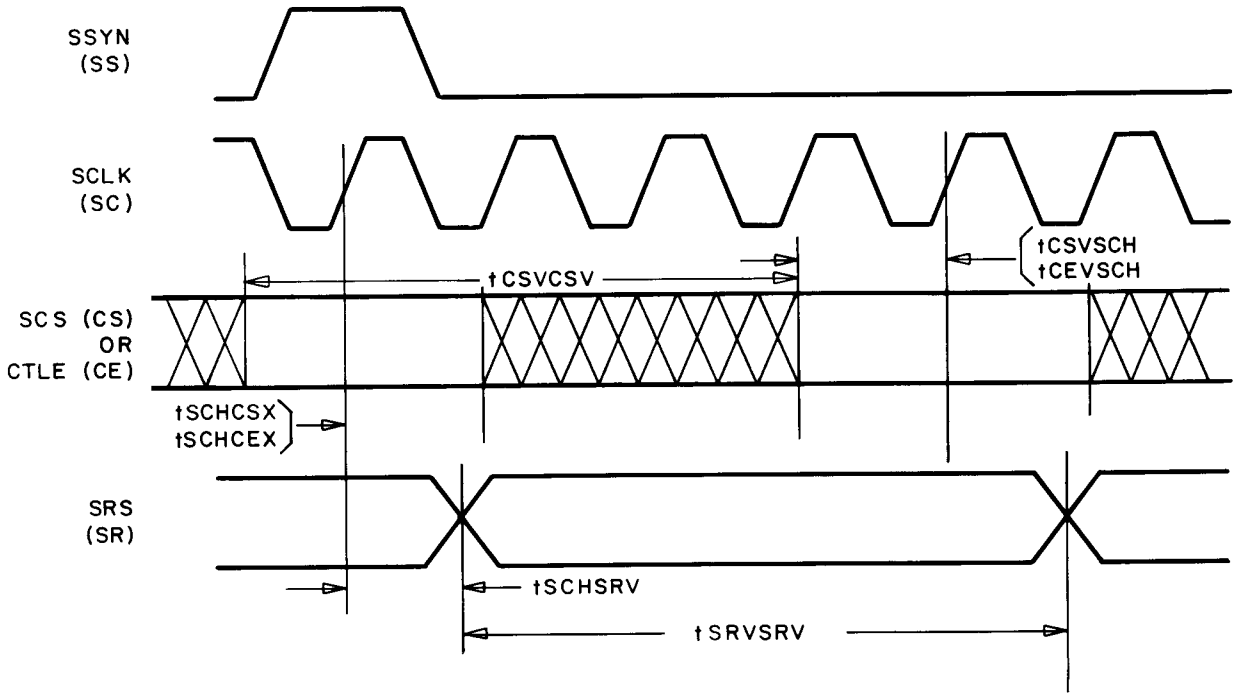


Figure 19. Serial Stream I/O

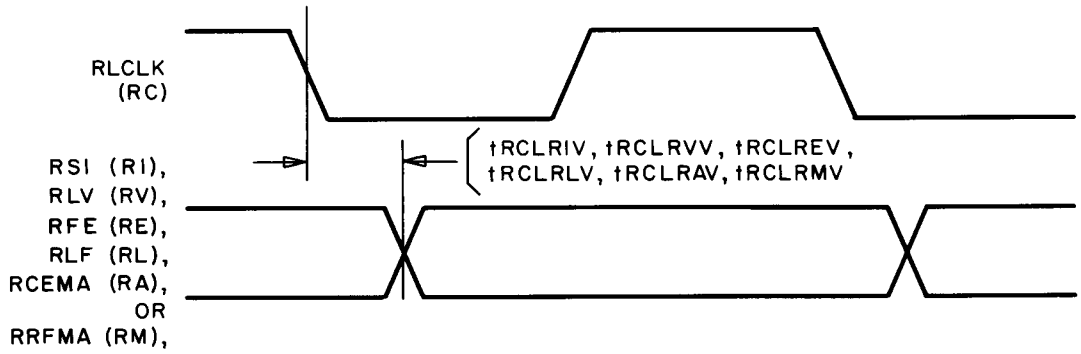
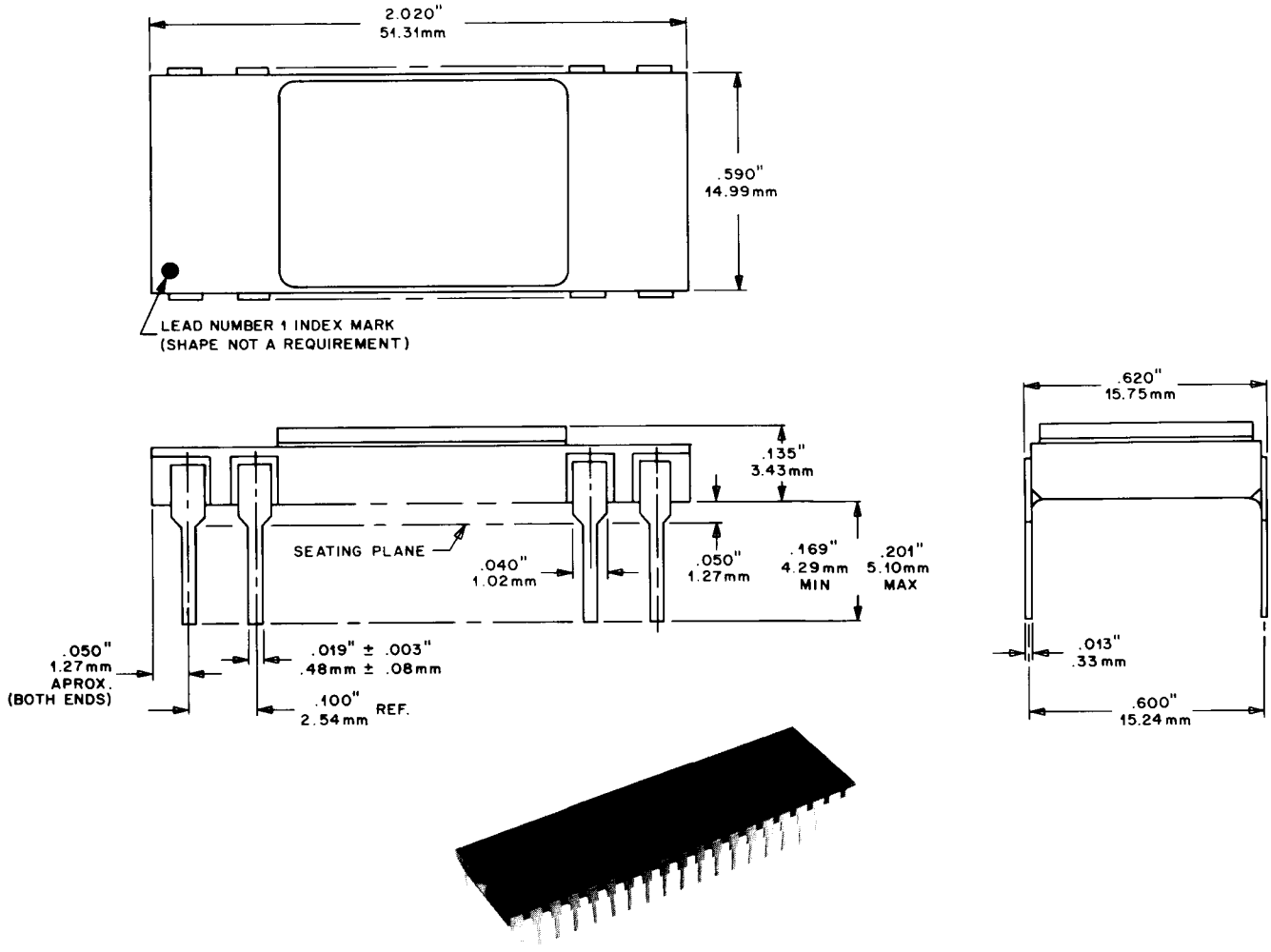


Figure 20. Status Outputs

Outline Diagram



ORDERING INFORMATION

Device Code	Package	Temperature	COMCODE
229CG	40-Pin Ceramic DIP	0 to 70 °C	103757084

For additional information contact your AT&T Account Manager, or call:

- AT&T Technologies, 555 Union Boulevard, Dept. 50AL203140, Allentown, PA 18103
  1-800-372-2447

In Europe, contact:

- AT&T Microelectronics, Freischützstrasse 92, 8000 München 81, West Germany
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