MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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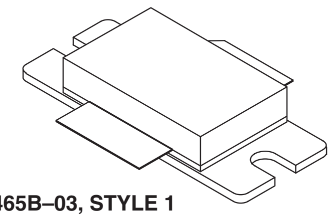
The RF Sub–Micron MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21090
MRF21090S

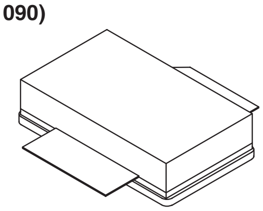
2170 MHz, 90 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

- Typical W–CDMA Performance for 2140 MHz, 28 Volts
  4.096 MHz BW @ 5 MHz offset, 1 PERCH 15 DTCH:
  Output Power — 11.5 Watts
  Efficiency — 16%
  Gain — 12.2 dB
  ACPR — –45 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2110 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 465B–03, STYLE 1
(NI–880)
(MRF21090)



CASE 465C–02, STYLE 1
(NI–880S)
(MRF21090S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions		Class
Human Body Model	MRF21090 MRF21090S	2 (Minimum) 1 (Minimum)
Machine Model	MRF21090 MRF21090S	M3 (Minimum) M4 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

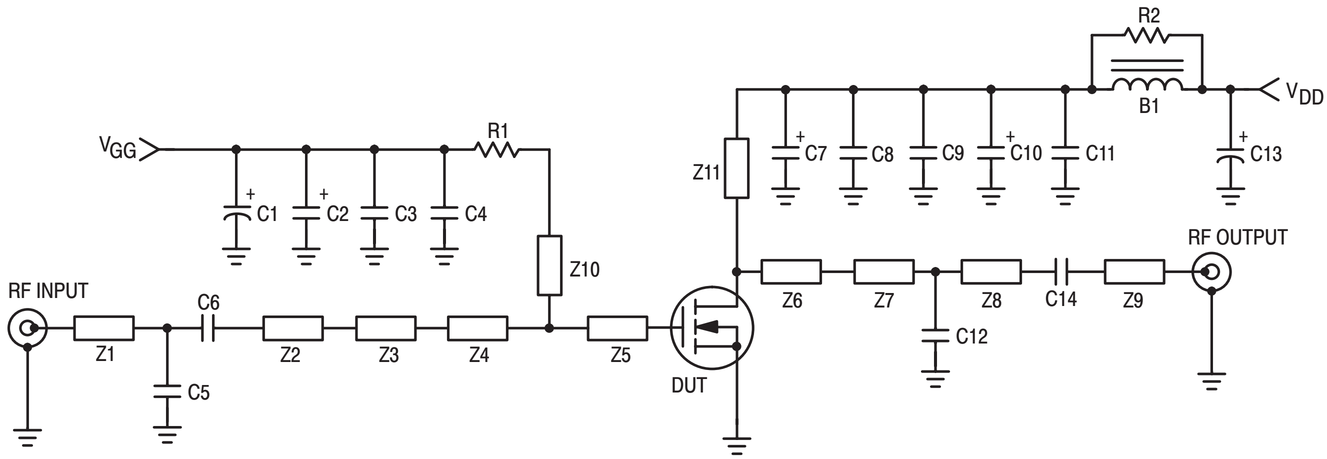
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 5

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 300 μA)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 750 mA)	$V_{GS(Q)}$	3	3.8	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(on)}$	—	0.1	0.6	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	G_{ps}	10	11.7	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	η	30	33	—	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IMD	—	–30	–27.5	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IRL	—	–12	–9.0	dB
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 75 W CW, I_{DQ} = 750 mA, f = 2170 MHz)	G_{ps}	—	11.7	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 75 W CW, I_{DQ} = 750 mA, f = 2170 MHz)	η	—	41	—	%
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1	Ferrite Bead, Fair Rite #2743019447
C1, C13	470 μF, 50 V Electrolytic Capacitors
C2, C10	22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet
C3, C9	20 nF Chip Capacitors, ATC #100B203MCA500X
C4, C8	5.1 pF Chip Capacitors, ATC #100B5R1CCA500X
C5, C12	0.4 – 2.5 pF Variable Capacitors, Johanson Gigatrim
C6	10 pF Chip Capacitor, ATC #100B100JCA500X
C7	1 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet
C11	1 nF Chip Capacitor, ATC #100B102JCA500X
C14	8.2 pF Chip Capacitor, ATC #100B8R2CCA500X
R1	13 Ω, 1/4 W Chip Resistor, Garret Instrument #RM73B2B130JT,
R2	12 Ω, 1/4 W Chip Resistor, Garret Instrument #RM73B2B120JT
Z1	30.7 x 2.09 mm Microstrip
Z2	5.99 x 2.09 mm Microstrip
Z3	7.55 x 9.89 mm Microstrip
Z4	3.77 x 15.71 mm Microstrip
Z5	6.89 x 26.17 mm Microstrip
Z6	14.93 x 32.05 mm Microstrip
Z7	10.23 x 2.09 mm Microstrip
Z8	6.03 x 2.09 mm Microstrip
Z9	23.98 x 2.09 mm Microstrip
Z10	29.82 x 1.15 mm Microstrip
Z11	17.08 x 1.15 mm Microstrip
WS1, WS2	Beryllium Copper Wear Blocks 5 mils Thick
	Brass Banana Jack and Nut
	Red Banana Jack and Nut
	Green Banana Jack and Nut
	Type N Jack Connectors, 3052–1648–10, Omni Specra
	4–40 Head Screws 0.125″ Long
	4–40 Head Screws 0.188″ Long
	4–40 Head Screws 0.312″ Long
	4–40 Head Screws 0.438″ Long
Endplates Brass	Endplates for Copper Bedstead
Bedstead	Copper Bedstead/Heatsink
Insert	Copper Bedstead Insert
Raw PCB	0.030″ Glass Teflon®, 2 oz Copper Clad 3″ x 5″ Arion
RF Circuit	3″ x 5″ Copper Clad PCB Teflon®, MRF21090, CMR

Figure 1. MRF21090 Test Circuit Schematic

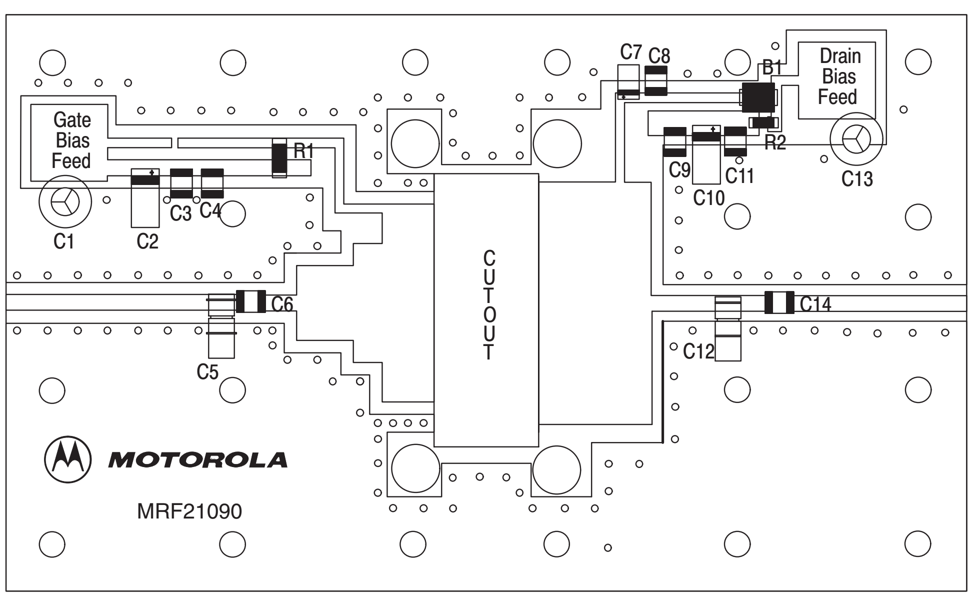


Figure 2. MRF21090 Test Circuit Component Layout

TYPICAL PERFORMANCE (IN MOTOROLA TEST FIXTURE)

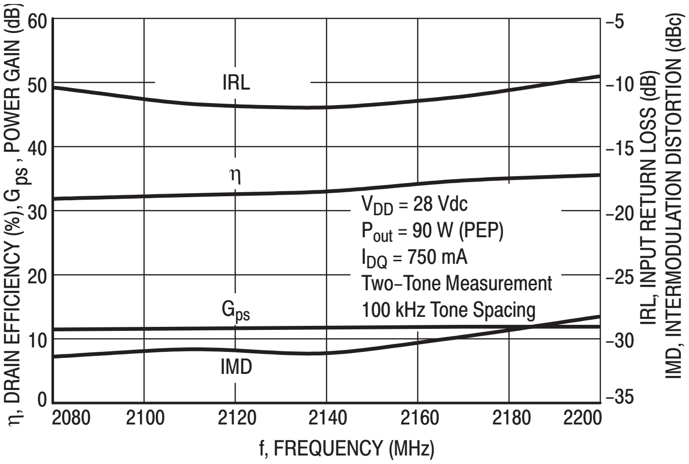


Figure 3. Class AB Broadband Circuit Performance

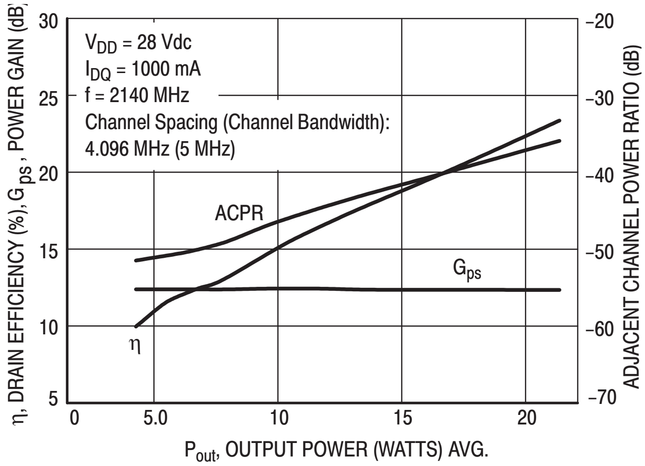


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

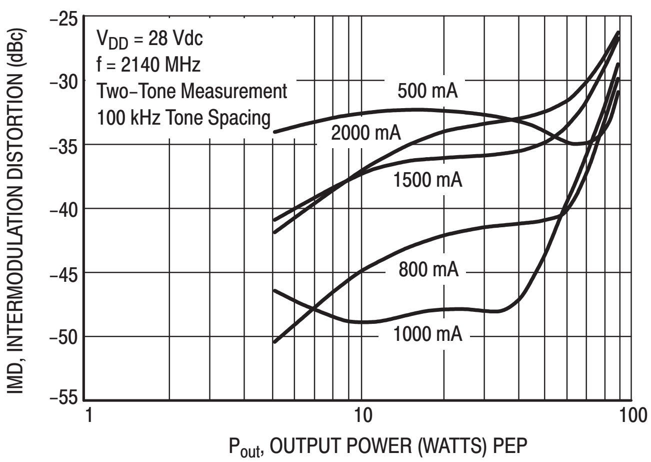


Figure 5. Intermodulation Distortion versus Output Power

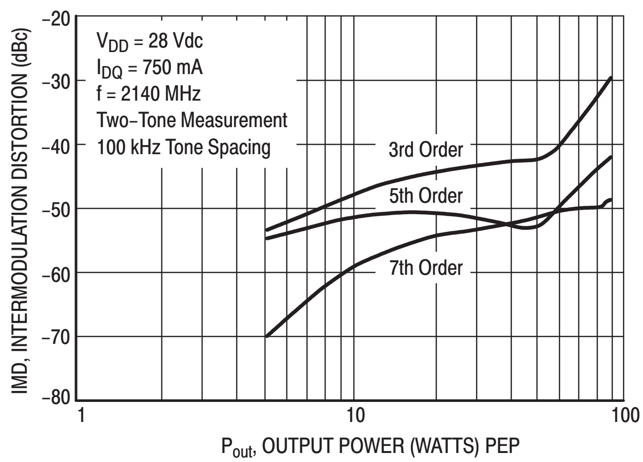


Figure 6. Intermodulation Distortion Products versus Output Power

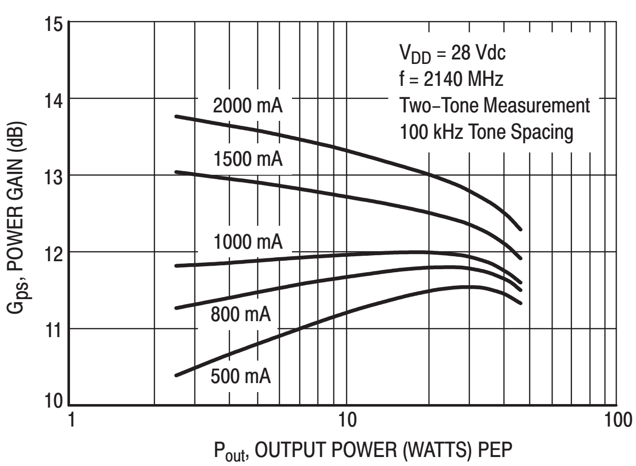


Figure 7. Power Gain versus Output Power

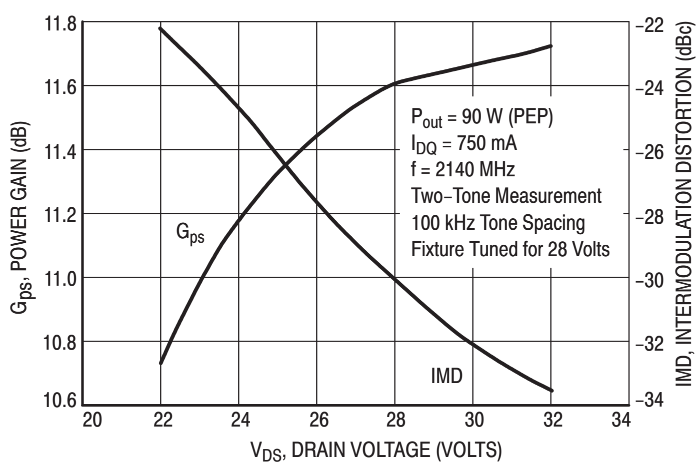
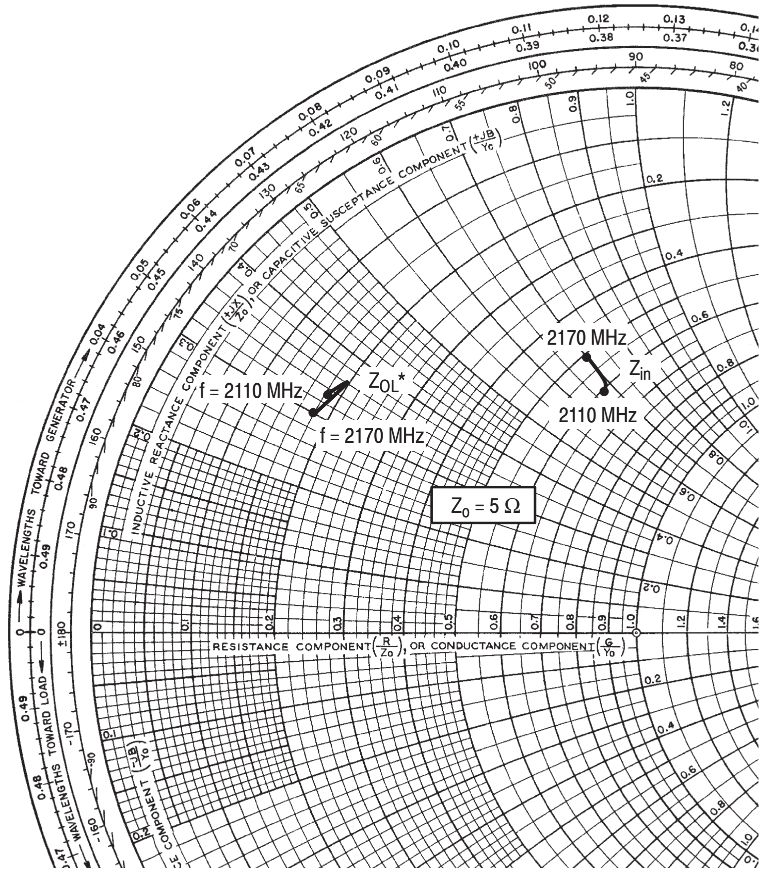


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 28 V, I_{DQ} = 750 mA, P_{out} = 90 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	3.03 + j3.40	0.92 + j1.67
2140	3.02 + j3.46	0.97 + j1.80
2170	2.60 + j3.50	0.90 + j1.52

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given power, voltage, IMD, bias current and frequency.

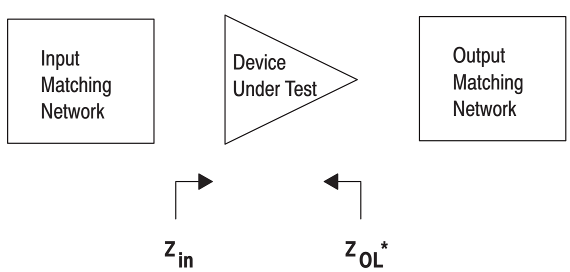
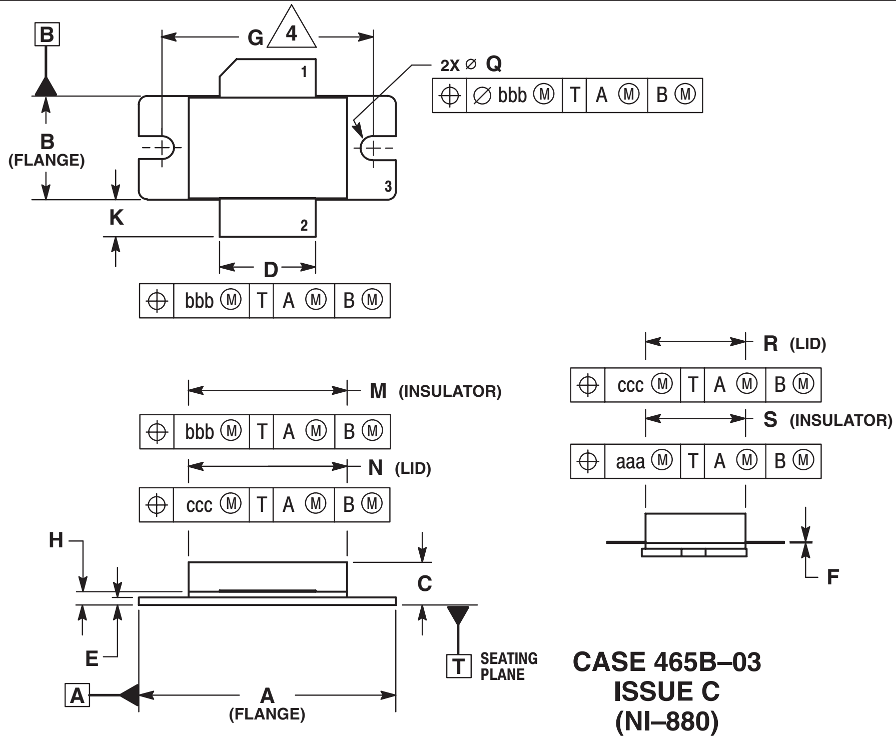


Figure 9. Series Equivalent Input and Output Impedance

NOTES

PACKAGE DIMENSIONS

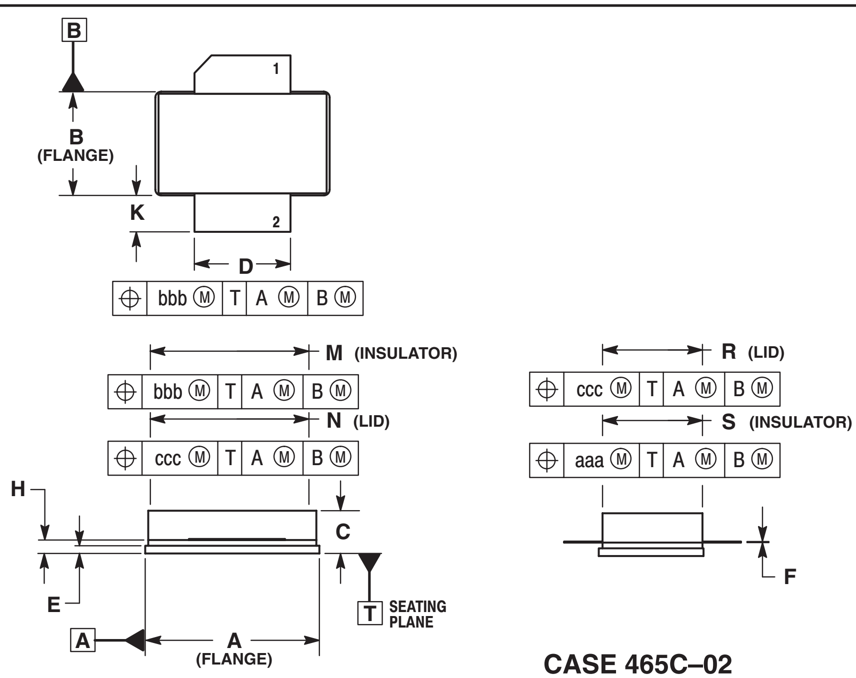


CASE 465B–03
ISSUE C
(NI–880)
(MRF21090)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.16 (29.57) BASED ON M3 SCREW.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.175	0.205	4.44	5.21
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE



CASE 465C–02
ISSUE A
(NI–880S)
(MRF21090S)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

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