The Wideband IC Line

RF LDMOS Wideband Integrated Power Amplifiers

MW5IC2030MBR1
MW5IC2030GMBR1

1930 - 1990 MHz, 30 W, 26 V
GSM/GSM EDGE, W - CDMA, PHS
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

The MW5IC2030 wideband integrated circuit is designed for base station applications. It uses Motorola's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi - stage structure. Its wideband On - Chip design makes it usable from 1930 to 1990 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, PHS, CDMA and W - CDMA.

Final Application

Typical CDMA Performance: V_{DD} = 27 Volts, I_{DQ1} = 160 mA, I_{DQ2} = 230 mA, P_{out} = 5 Watts Avg., Full Frequency Band, IS - 95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13)

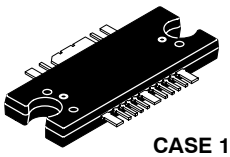
Power Gain — 23 dB
Drain Efficiency — 20%
ACPR @ 885 kHz Offset — - 49 dBc @ 30 kHz Channel Bandwidth

Driver Application

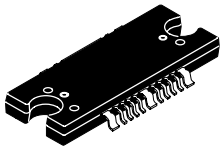
Typical CDMA Performance: V_{DD} = 27 Volts, I_{DQ1} = 200 mA, I_{DQ2} = 550 mA, P_{out} = 1 Watt Avg., Full Frequency Band, IS - 95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13)

Power Gain — 24 dB
ACPR @ 885 kHz Offset — - 64 dBc @ 30 kHz Channel Bandwidth

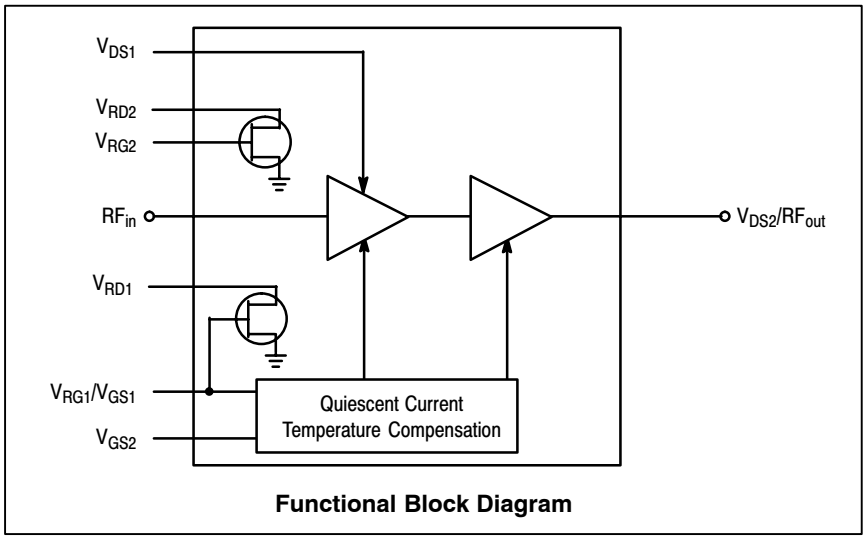
- On - Chip Matching (50 Ohm Input, >4 Ohm Output)
- Integrated Temperature Compensation Capability with Enable/Disable Function
- On - Chip Current Mirror g_m Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- Designed for Lower Memory Effects and Wide Instantaneous Bandwidth Applications
- Also Available in Gull Wing for Surface Mount
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel



CASE 1329 - 09
TO - 272 WB - 16
PLASTIC
MW5IC2030MBR1

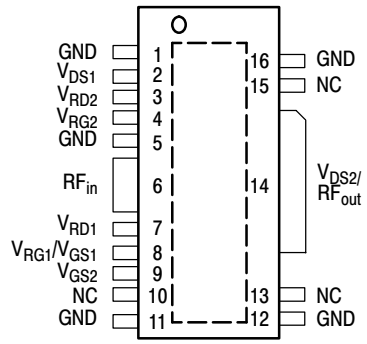


CASE 1329A - 03
TO - 272 WB - 16 GULL
PLASTIC
MW5IC2030GMBR1



Functional Block Diagram

PIN CONNECTIONS



(Top View)

NOTE: Exposed backside flag is source terminal for transistors.

(1) Refer to AN1987/D, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.motorola.com/semiconductors/rf. Select Documentation/Application Notes - AN1987.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	-65 to +175	°C
Operating Junction Temperature	T_J	200	°C
Input Power	P_{in}	20	dBm

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
CDMA Application	Stage 1, 27 Vdc, I_{DQ} = 160 mA		4.89	
(P_{out} = 5 W CW)	Stage 2, 27 Vdc, I_{DQ} = 230 mA		1.75	
PHS Application	Stage 1, 26 Vdc, I_{DQ} = 300 mA		4.85	
(P_{out} = 12.6 W CW)	Stage 2, 26 Vdc, I_{DQ} = 1300 mA		1.61	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1B (Minimum)
Machine Model	A (Minimum)
Charge Device Model	3 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

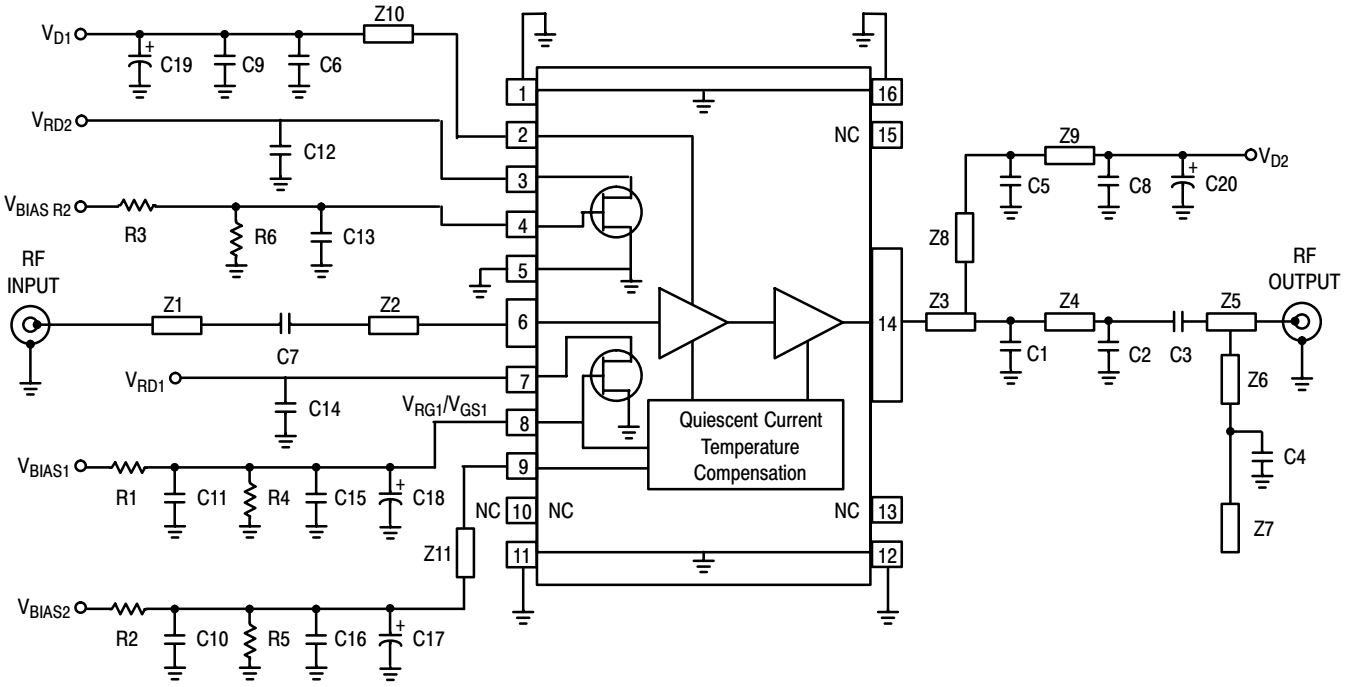
Characteristic	Symbol	Min	Typ	Max	Unit
CDMA FUNCTIONAL TESTS (In Motorola 1.9 GHz Test Fixture, 50 ohm system) V_{DD} = 27 Vdc, I_{DQ1} = 160 mA, I_{DQ2} = 230 mA, P_{out} = 5 W Avg., 1960 MHz, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Channel Bandwidth @ ± 885 kHz Offset. Peak/Avg. = 9.8 dB @ 0.01 Probability on CCDF.					
Power Gain	G_{ps}	21.5	23	—	dB
Drain Efficiency	η_D	18	20	—	%
Input Return Loss	IRL	—	-18	-10	dB
Adjacent Channel Power Ratio	ACPR	—	—	-47	dBc
Stability (0 dBm<P_{out}<43 dBm CW; 3:1 VSWR)		No Spurious > -60 dBc			
Gain Flatness in 30 MHz BW, 1930-1990 MHz	G_F	—	0.2	0.3	dB

(1) Refer to AN1955/D, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.motorola.com/semiconductors/rf. Select Documentation/Application Notes - AN1955.

(continued)

ELECTRICAL CHARACTERISTICS - (continued) (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
TYPICAL PERFORMANCES (In Motorola Test Fixture) V_{DD} = 26 Vdc, I_{DQ1} = 160 mA, I_{DQ2} = 230 mA, P_{out} = 5 W, f = 1960 MHz					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	30	—	W
Deviation from Linear Phase in 30 MHz BW (Characterized from 1930 - 1990 MHz)	Φ	—	±1	—	°
Delay	Delay	—	2.25	—	ns
Part to Part Phase Variation	ΔΦ	—	±10	—	°
Part to Part Gain Variation (Per Lot or Reel)	ΔG	—	±1.5	—	dB
Reference FET to RF FET Scaling Ratio Delta (Stages 1 and 2)		—	10	—	%
TYPICAL PHS PERFORMANCES (In Motorola Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1} = 260 mA, I_{DQ2} = 1100 mA, P_{out} = 12.6 W, 1.9 GHz, PHS Signal Mask					
Power Gain	G_{ps}	—	24	—	dB
Power Added Efficiency	PAE	—	25	—	%
Input Return Loss	IRL	—	-15	—	dB
Adjacent Channel Power Ratio (600 kHz Offset in 192 kHz BW)	ACPR	—	-72	—	dBc



Z1	0.465″ x 0.041″ Microstrip	Z7	0.200″ x 0.025″ Microstrip
Z2	0.518″ x 0.041″ Microstrip	Z8	0.274″ x 0.050″ Microstrip
Z3	0.282″ x 0.235″ Microstrip	Z9	0.615″ x 0.050″ Microstrip
Z4	0.221″ x 0.081″ Microstrip	Z10	0.450″ x 0.025″ Microstrip
Z5	0.489″ x 0.041″ Microstrip	Z11	0.340″ x 0.014″ Microstrip
Z6	0.471″ x 0.025″ Microstrip	PCB	Rogers 4350, 0.020″, ε_r = 3.5

Figure 1. MW5IC2030MBR1(GMBR1) Test Circuit Schematic

Table 1. MW5IC2030MBR1(GMBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	1.8 pF High Q Chip Capacitor (0603)	600S1R8AT-250-T	ATC
C2	1.5 pF High Q Chip Capacitor (0603)	600S1R5AT-250-T	ATC
C3	3.9 pF High Q Chip Capacitor (0603)	600S3R9AT-250-T	ATC
C4	6.8 pF High Q Chip Capacitor (0805)	600S6R8AT-250-T	ATC
C5, C6	100 pF Class 1 NPO Chip Capacitors (0805)	GRM215CB1H101CZ01D	Murata
C7	4.7 pF Class 1 NPO Chip Capacitor (0805)	GRM215CB1H4R7CZ01D	Murata
C8, C9, C10, C11	0.1 μF X7R Chip Capacitors (1206)	C1206C104K5RACT	Kemet
C12, C13, C14, C15, C16	0.01 μF Class 2 X7R Chip Capacitors (0805)	C0805C103K5RACT	Kemet
C17, C18	22 μF, 35 V Electrolytic Capacitors	ECE-1AVKS220	Panasonic
C19, C20	330 μF, 50 V Electrolytic Capacitors	ECA-1HM331	Panasonic
R1, R3	1 kΩ, 5% Chip Resistors (0805)	RK73B2ALTD102J	KOA Speer
R2	499 Ω, 1% Chip Resistor (0805)	RK73H2ATD4990F	KOA Speer
R4, R5, R6	100 kΩ, 5% Chip Resistors (0805)	RK73B2ALTD104J	KOA Speer

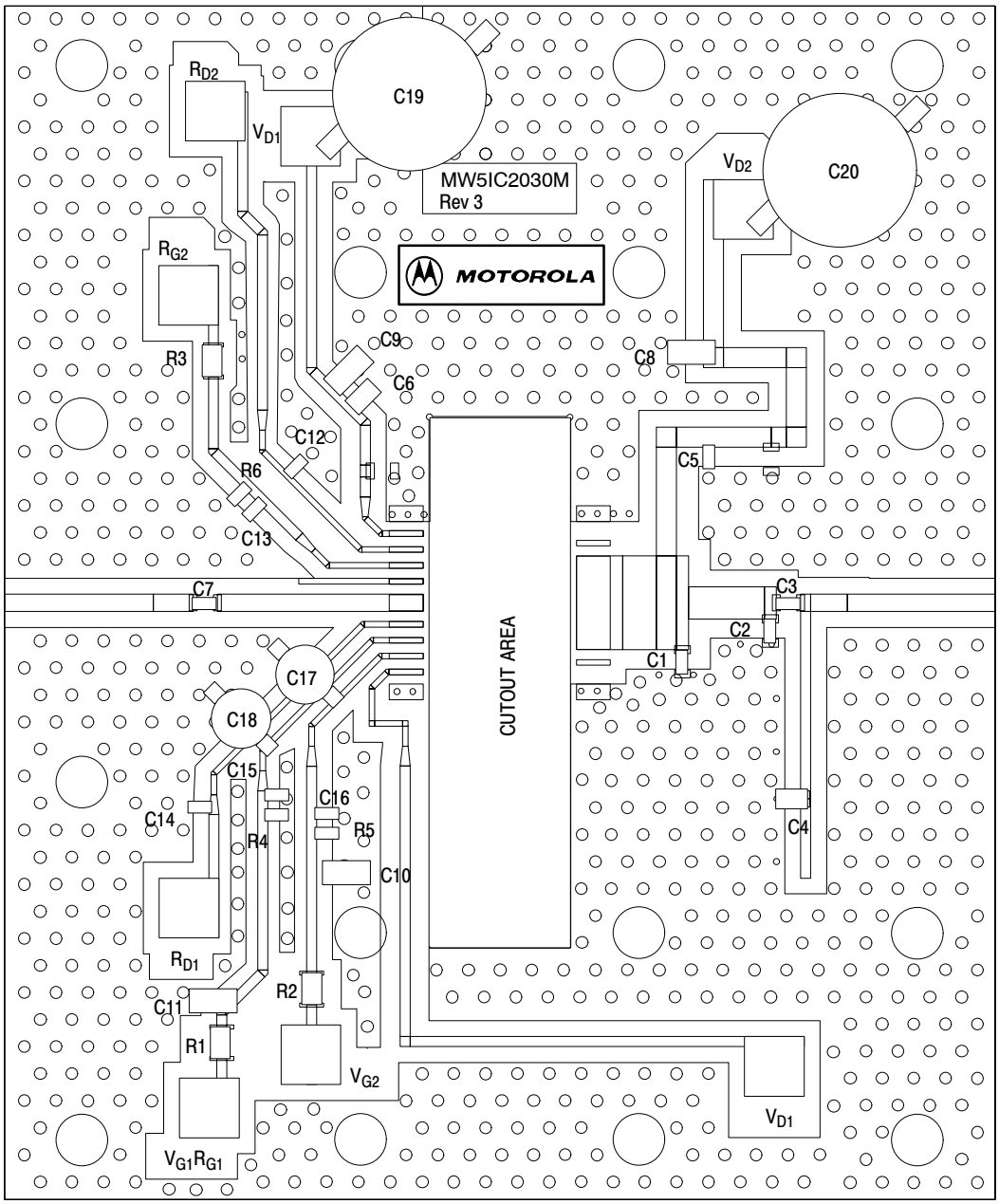


Figure 2. MW5IC2030MBR1(GMBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

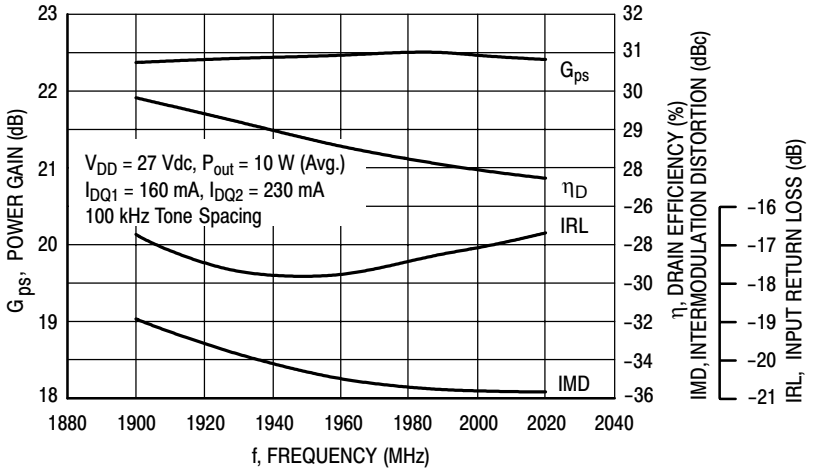


Figure 3. Two-Tone Broadband Performance

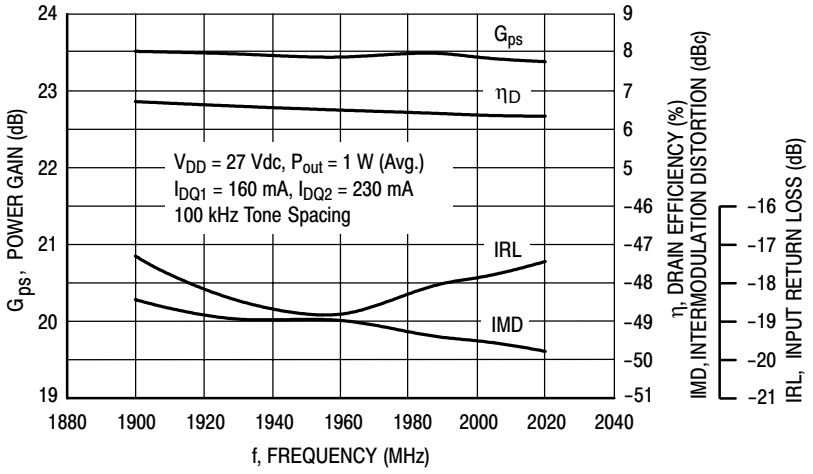


Figure 4. Two-Tone Broadband Performance

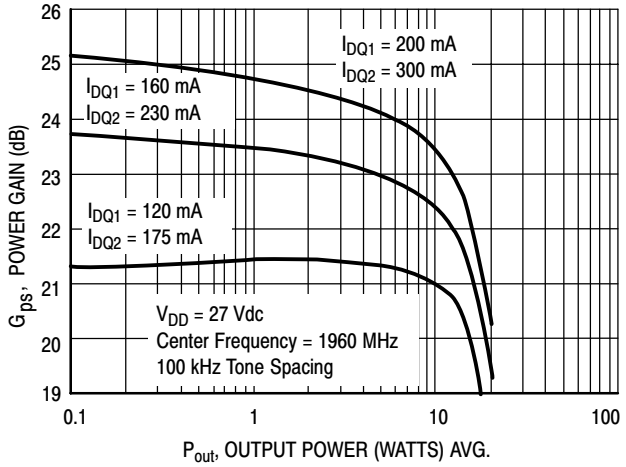


Figure 5. Two-Tone Power Gain versus Output Power

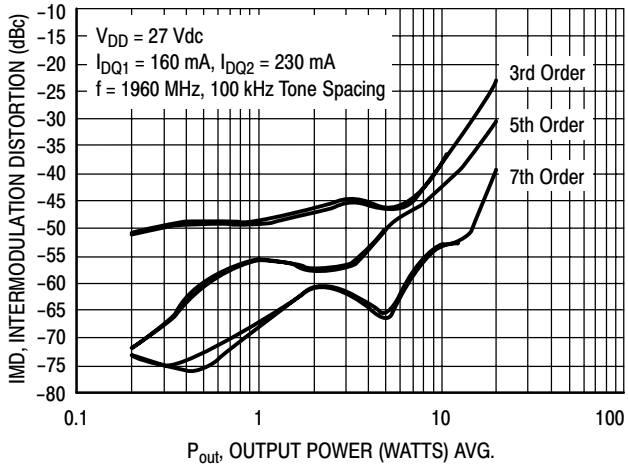


Figure 6. Intermodulation Distortion Products versus Output Power

TYPICAL CHARACTERISTICS

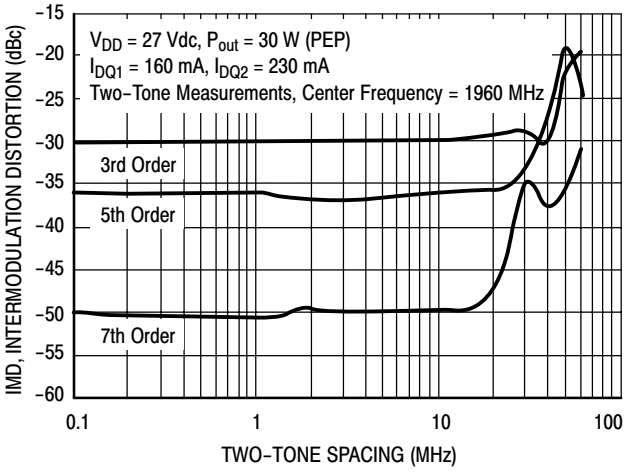


Figure 7. Intermodulation Distortion Products versus Tone Spacing

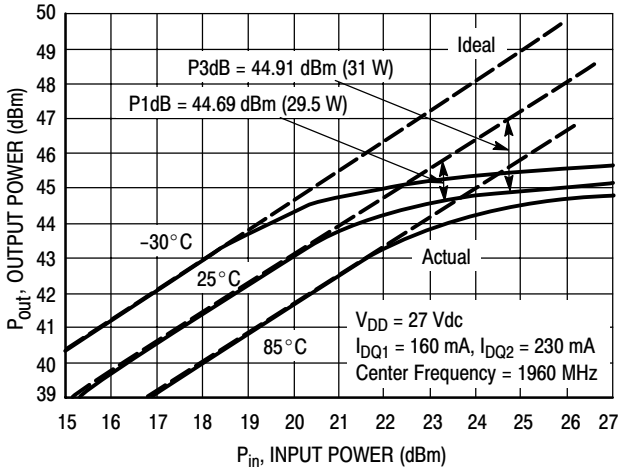


Figure 8. Pulse CW Output Power versus Input Power

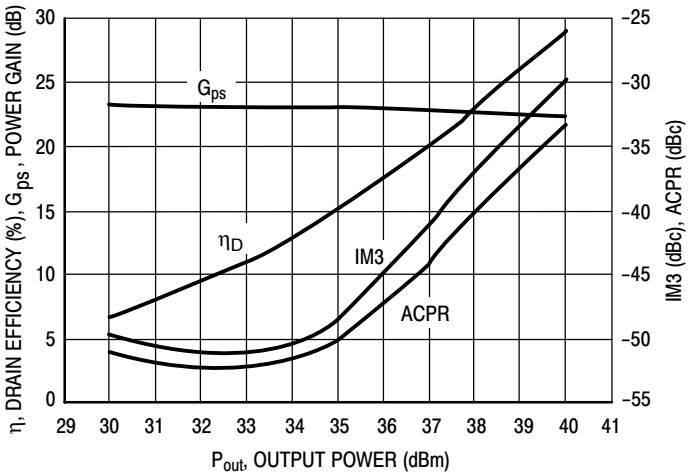


Figure 9. 2-Carrier W-CDMA IM3, Power Gain, and Efficiency versus Output Power

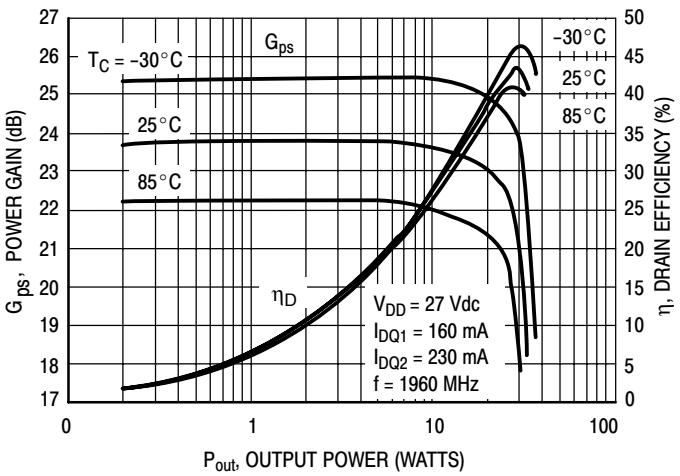


Figure 10. Power Gain and Power Added Efficiency versus Output Power

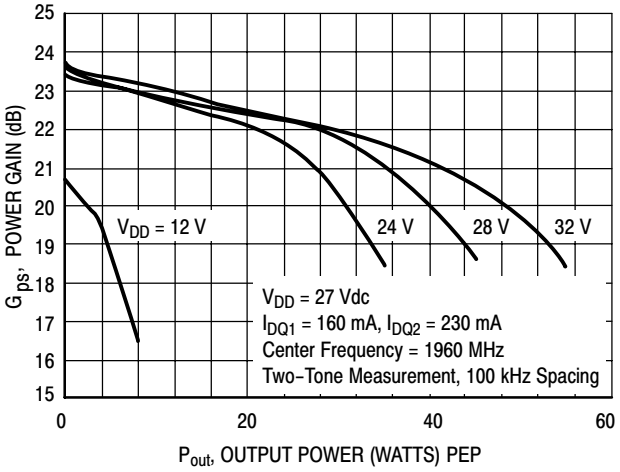


Figure 11. Power Gain versus Output Power

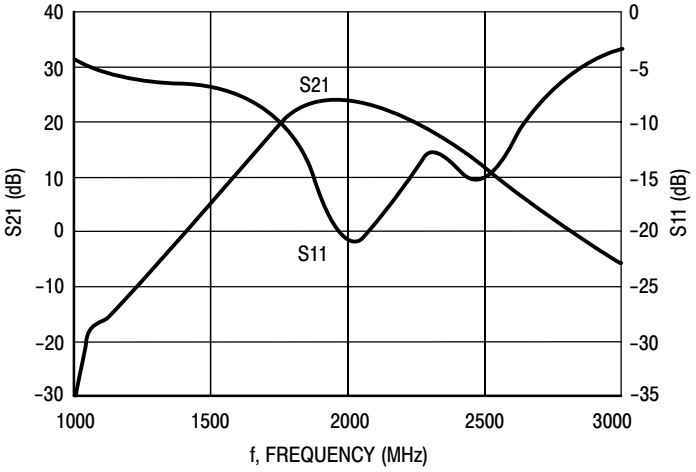


Figure 12. Broadband Frequency Response

TYPICAL CHARACTERISTICS

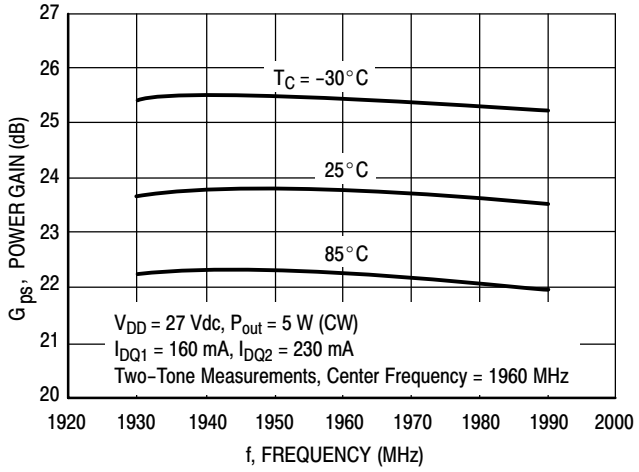


Figure 13. Power Gain versus Frequency

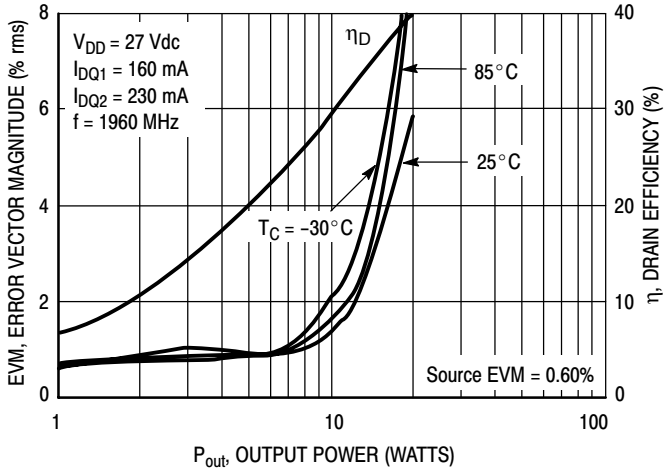


Figure 14. EVM and Drain Efficiency versus Output Power

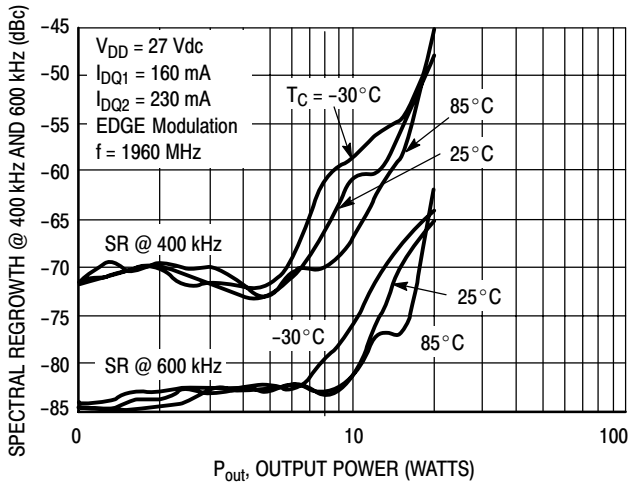


Figure 15. Spectral Regrowth at 400 kHz and 600 kHz versus Output Power

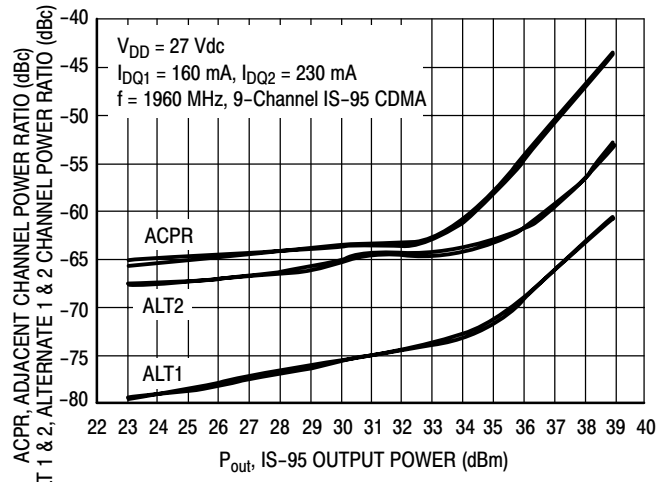


Figure 16. IS-95 Spectral Regrowth versus Output Power

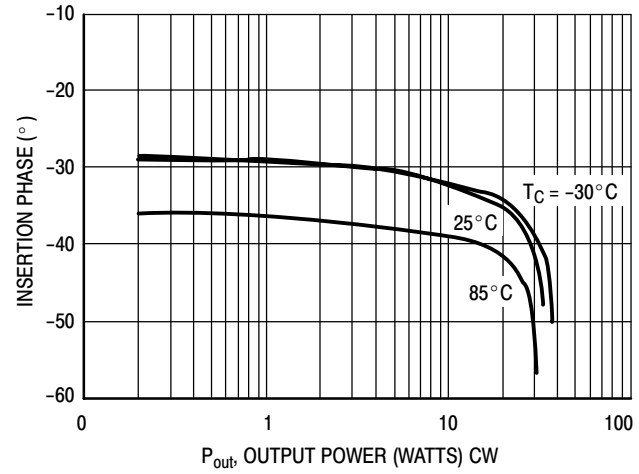
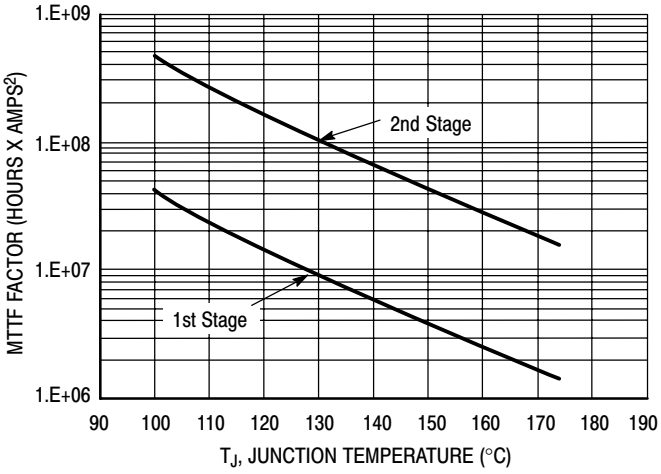
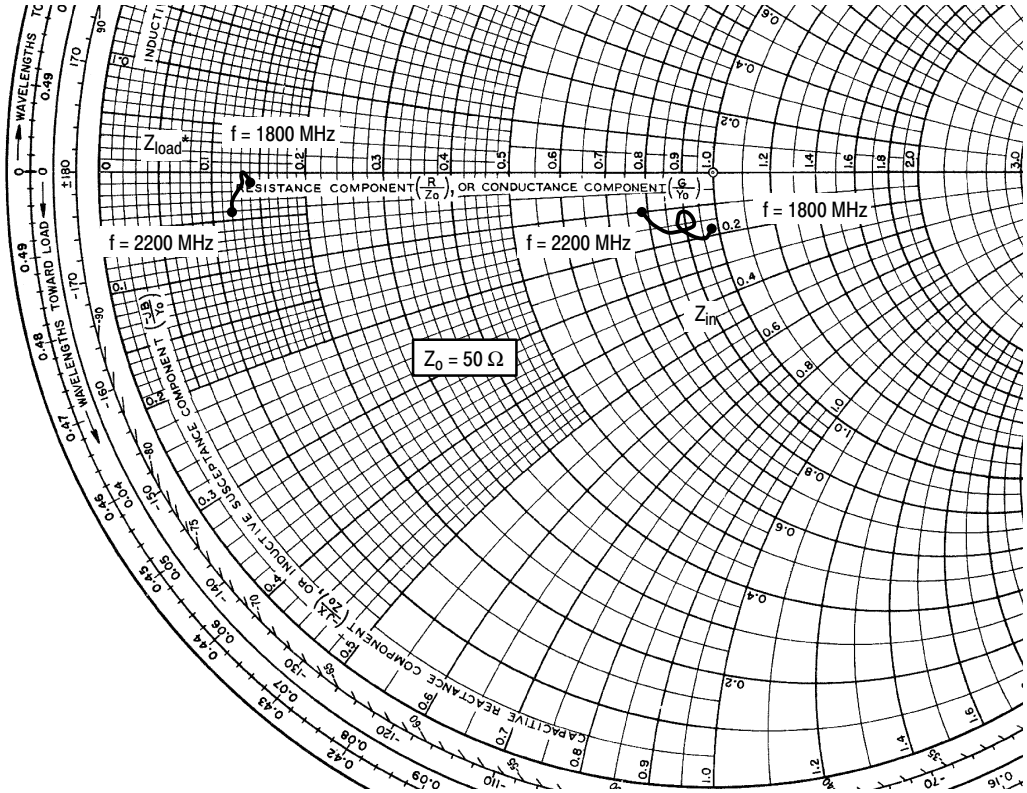


Figure 17. Insertion Phase versus Output Power



This above graph displays calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 18. MTTF Factor versus Junction Temperature



V_{DD} = 27 V, I_{DQ1} = 160 mA, I_{DQ2} = 230 mA

f MHz	Z_{in} Ω	Z_{load} Ω
1800	49.7 - j9.3	6.9 - j0.3
1850	47.7 - j9.8	6.9 - j0.3
1930	44.8 - j8.5	6.7 - j0.1
1960	44.0 - j7.3	6.6 - j0.0
1990	44.6 - j5.6	6.6 + j0.1
2050	45.7 - j8.6	6.4 + j0.4
2100	42.5 - j8.3	6.2 + j0.8
2150	40.6 - j6.8	6.1 + j1.1
2200	39.3 - j5.0	6.0 + j1.6

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

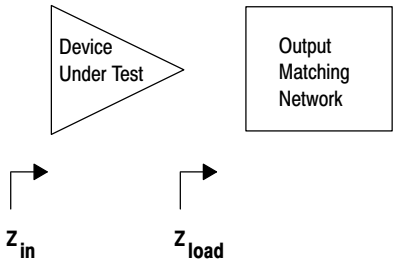
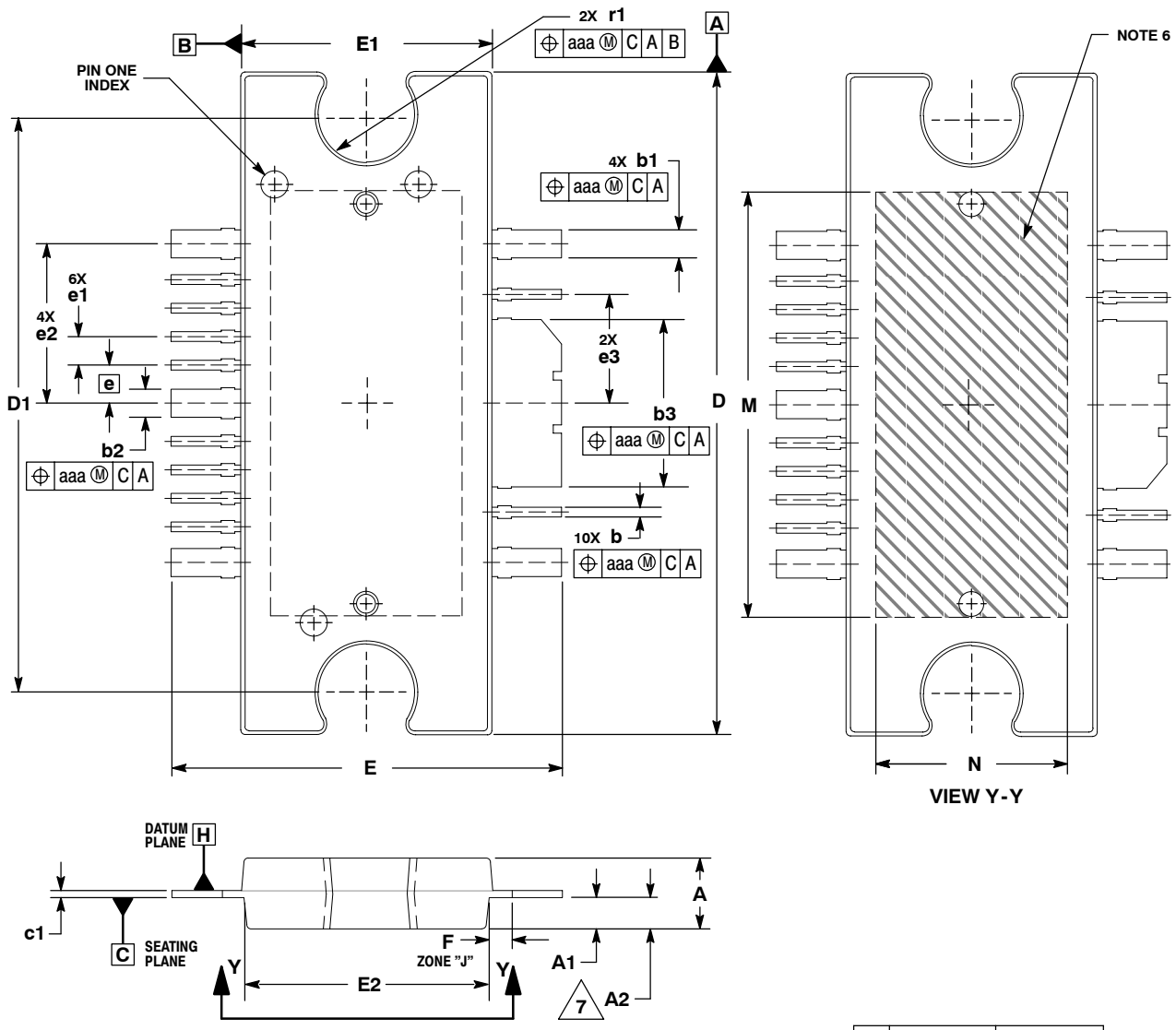


Figure 19. Series Equivalent Input and Load Impedance

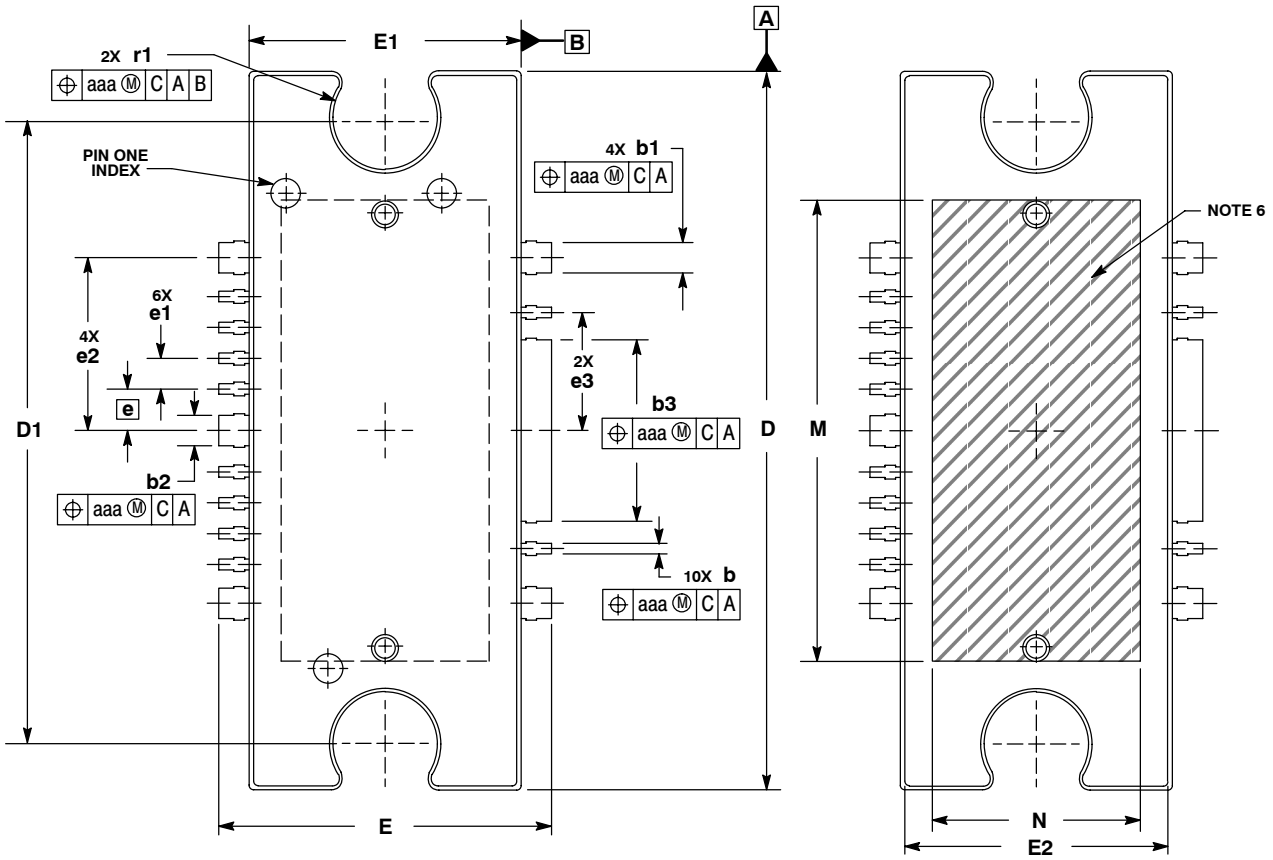
PACKAGE DIMENSIONS

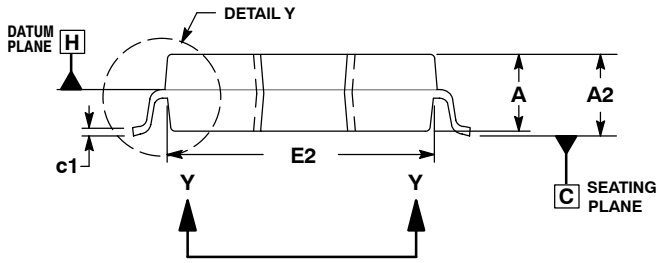


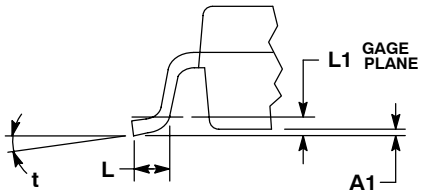
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.038	.044	0.96	1.12
A2	.040	.042	1.02	1.07
D	.928	.932	23.57	23.67
D1	.810 BSC		20.57 BSC	
E	.551	.559	14.00	14.20
E1	.353	.357	8.97	9.07
E2	.346	.350	8.79	8.89
F	.025 BSC		0.64 BSC	
M	.600	---	15.24	---
N	.270	---	6.86	---
b	.011	.017	0.28	0.43
b1	.037	.043	0.94	1.09
b2	.037	.043	0.94	1.09
b3	.225	.231	5.72	5.87
c1	.007	.011	.18	.28
e	.054 BSC		1.37 BSC	
e1	.040 BSC		1.02 BSC	
e2	.224 BSC		5.69 BSC	
e3	.150 BSC		3.81 BSC	
r1	.063	.068	1.6	1.73
aaa	.004		.10	

NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

CASE 1329-09
ISSUE J
TO-272 WB-16
PLASTIC
MW5IC2030MBR1







DETAIL Y

NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SINK.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.001	.004	0.02	0.10
A2	.099	.110	2.51	2.79
D	.928	.932	23.57	23.67
D1	.810 BSC		20.57 BSC	
E	.429	.437	10.90	11.10
E1	.353	.357	8.97	9.07
E2	.346	.350	8.79	8.89
L	.018	.024	4.90	5.06
L1	.01 BSC		0.25 BSC	
M	.600	---	15.24	---
N	.270	---	6.86	---
b	.011	.017	0.28	0.43
b1	.037	.043	0.94	1.09
b2	.037	.043	0.94	1.09
b3	.225	.231	5.72	5.87
c1	.007	.011	.18	.28
e	.054 BSC		1.37 BSC	
e1	.040 BSC		1.02 BSC	
e2	.224 BSC		5.69 BSC	
e3	.150 BSC		3.81 BSC	
r1	.063	.068	1.6	1.73
t	2°	8°	2°	8°
aaa	.004		.10	

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