LH28F032SUTD

32M (2M × 16, 4M × 8) Flash Memory

FEATURES

- User-Configurable x8 or x16 Operation
- User-Selectable 3.3 V or 5 V V_{CC}
- Maximum Access Time:
  - 70/100 ns (V_{CC} = 5.0 V ± 0.25 V)
  - 80/110 ns (V_{CC} = 5.0 V ± 0.5 V)
- 0.64 MB/sec Write Transfer Rate
- 1,000,000 Erase Cycles per Block
- 64 Independently Lockable Blocks
- 5 V Write/Erase Operation (5 V V_{PP})
  - No Requirement for DC/DC Converter to Write/Erase
  - Capable to Perform Erase, Write, Read for each Chip independently
- Dual LH28F016SU (5 V Single Voltage 16M Flash Memory) Chips Encapsulated in a Single Package
- Revolutionary Architecture
  - Pipelined Command Execution
  - Write During Erase
  - Command Superset of Sharp LH28F016SU
- 20 µA (MAX.) I_{CC} Both Chips in Standby
- 10 µA (MAX.) Deep Power-Down
- State-of-the Art 0.6 µm ETOX™ Flash Technology
- 56-Pin, 1.2 mm x 14 mm x 20 mm TSOP (Type I) Package

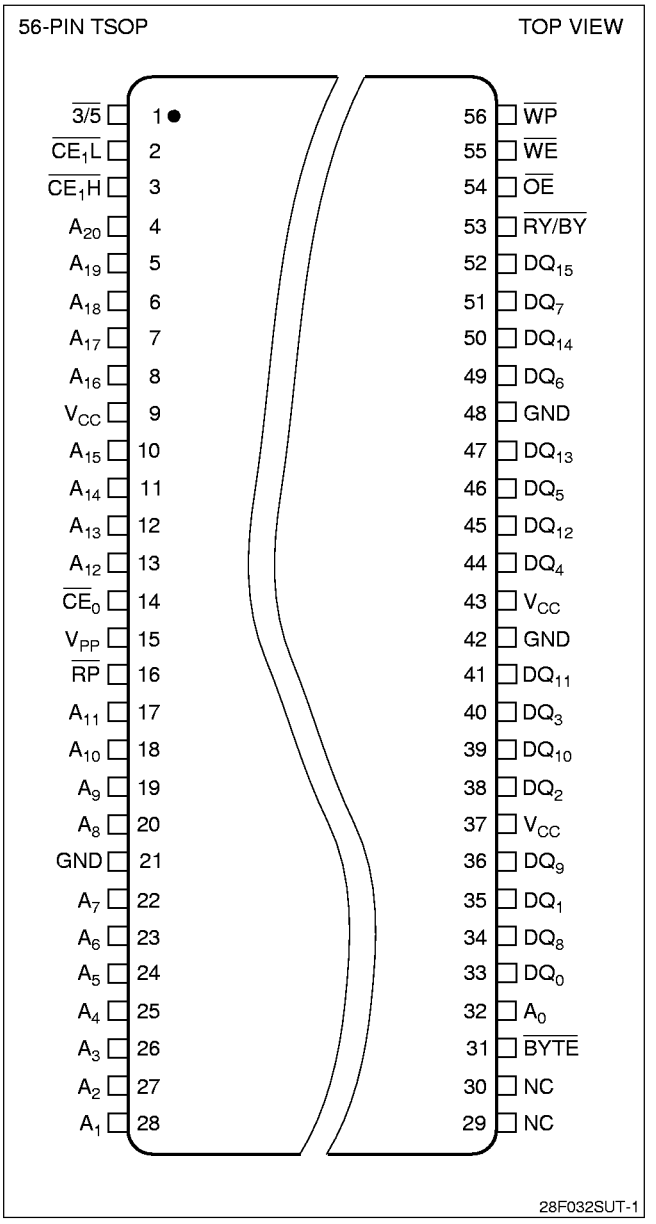


Figure 1. TSOP Configuration

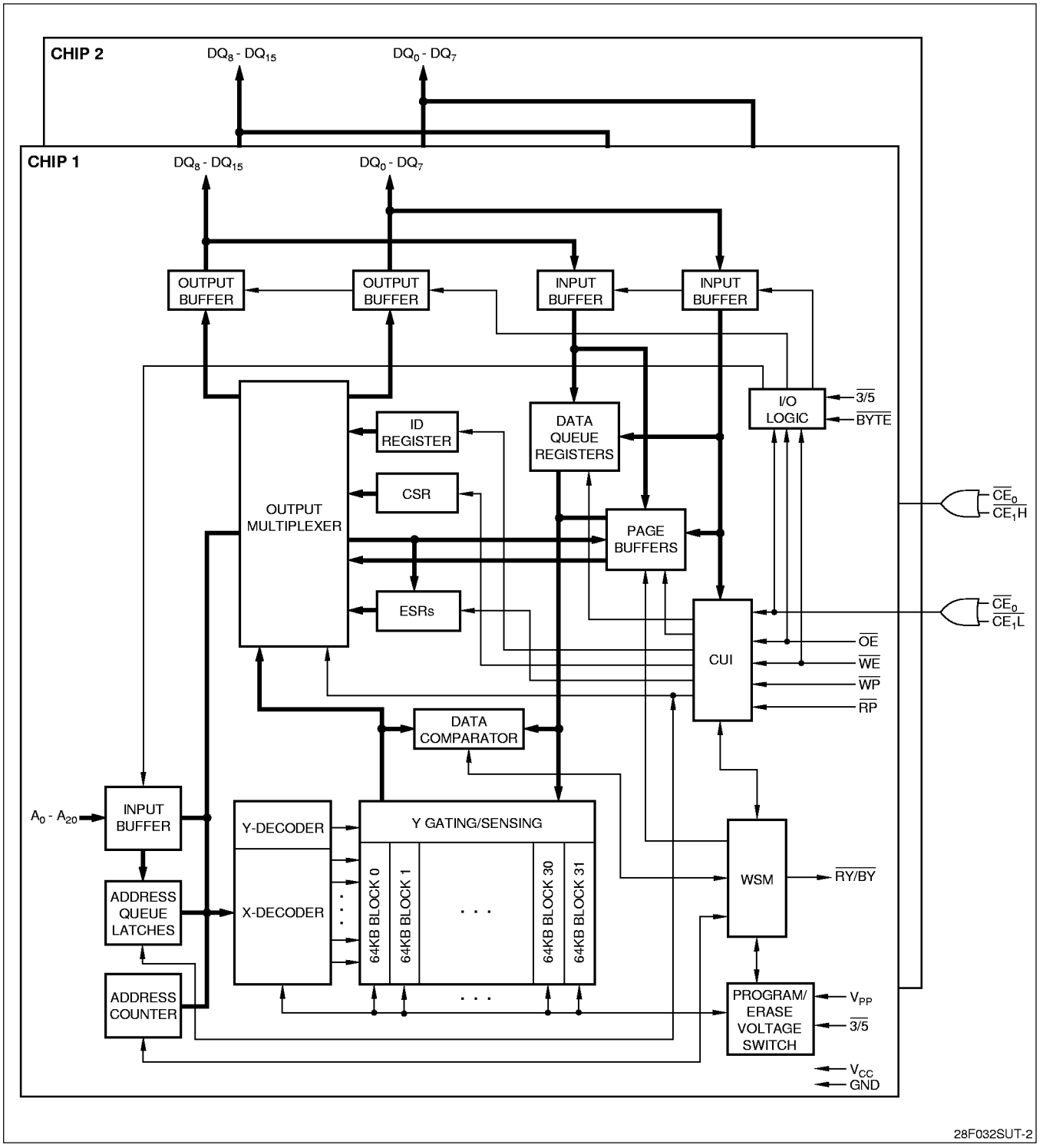


Figure 2. LH28F032SU Block Diagram (Architectural Evolution Includes Page Buffers, Queue Registers and Extended Status Registers)

PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
A_0	INPUT	**BYTE-SELECFT ADDRESS:** Selects between high and low byte when device is in x8 mode. This address is latched in x8 Data Writes. Not used in x16 mode (it must be fixed to 'L' or 'H') (i.e., the A_0 input buffer is turned off when $\overline{BYTE}$ is high).
A_1 - A_{15}	INPUT	**WORD-SELECT ADDRESSES:** Select a word within one 64K block. A_6 - A_{15} selects 1 of 1024 rows, and A_1 - A_5 selects 16 of 512 columns. These addresses are latched during Data Writes.
A_{16} - A_{19}	INPUT	**BLOCK-SELECT ADDRESSES:** Select 1 of 32 Erase blocks. These addresses are latched during Data Writes, Erase and Lock-Block operations.
DQ_0 - DQ_7	INPUT/OUTPUT	**LOW-BYTE DATA BUS:** Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate Read mode. Floated when the chip is de-selected or the outputs are disabled.
DQ_8 - DQ_{15}	INPUT/OUTPUT	**HIGH-BYTE DATA BUS**: Inputs data during x16 Data-Write operations. Outputs array, buffer or identifier data in the appropriate Read mode; not used for Status register reads. Floated when the chip is de-selected or the outputs are disabled.
$\overline{CE}_0$, $\overline{CE}_1$	INPUT	**CHIP ENABLE INPUTS**: Activate the device's control logic, input buffers, decoders and sense amplifiers. When $\overline{CE}_0$ or $\overline{CE}_{1L}$ are 'low', chip1 is in active. When $\overline{CE}_0$, $\overline{CE}_{1H}$ are 'low', chip2 is active.
$\overline{RP}$	INPUT	**RESET/POWER-DOWN:** With $\overline{RP}$ low, the device is reset, any current operation is aborted and device is put into the deep power down mode.All circuits that burn static power, even those cirucits enabled instandby mode, are turned off. When returning from Deep Power-Down, a recovery time of 400 ns is required to allow these circuits to power-up. When $\overline{RP}$ goes low, any current or pending WSM operation(s) are terminated, and the device is reset. All Status registers return to ready (with all status flags cleared).
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates device data through the output buffers when low. The outputs float to tri-state off when $\overline{OE}$ is high. **NOTE:** $\overline{CE}_X$ overrides $\overline{OE}$, and $\overline{OE}$ overrides $\overline{WE}$.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. $\overline{WE}$ is active low, and latches both address and data (command or array) on its rising edge.
$\overline{RY}/\overline{BY}$	OPEN DRAIN OUTPUT	**READY/BUSY:** Indicates status of the internal WSM. When low, it indicates that the chip1 WSM or chip2 WSM is busy performing an operation. $\overline{RY}/\overline{BY}$ high indicates that the WSM is ready for new operations (or WSM has completed all pending operations), or Erase is Suspended, or the device is in deep power-down mode. This output is always active (i.e., not floated to tri-state off when $\overline{OE}$ or $\overline{CE}_0$, $\overline{CE}_1$ are high), except if a $\overline{RY}/\overline{BY}$ Pin Disable command is issued.

PIN DESCRIPTION (Continued)

SYMBOL	TYPE	NAME AND FUNCTION
$\overline{WP}$	INPUT	**WRITE PROTECT:** Erase blocks can be locked by writing a non-volatile lock-bit for each block. When $\overline{WP}$ is low, those locked blocks as reflected by the Block-Lock Status bits (BSR.6), are protected from inadvertent Data Writes or Erases. When $\overline{WP}$ is high, all blocks can be Written or Erased regardless of the state of the lock-bits. The $\overline{WP}$ input buffer is disabled when $\overline{RP}$ transitions low (deep power-down mode).
$\overline{BYTE}$	INPUT	**BYTE ENABLE:** BYTE low places device x8 mode. All data is then input or output on DQ_0 - DQ_7, and DQ_8 - DQ_{15} float. Address A_0 selects between the high and low byte. $\overline{BYTE}$ high places the device in x16 mode, and turns off the A0 input buffer. Address A_1, then becomes the lowest order address.
$\overline{3/5}$	INPUT	**3.3/5.0 VOLT SELECT:** $\overline{3/5}$ high configures internal circuits for 3.3 V operation. $\overline{3/5}$ low configures internal circuits for 5.0 V operation. **NOTES:** Reading the array with $\overline{3/5}$ high in a 5.0 V system could damage the device. There is a significant delay from $\overline{3/5}$ switching to valid data.
V_{PP}	SUPPLY	**ERASE/WRITE POWER SUPPLY (5.0 V ±0.5 V):** For erasing memory array blocks or writing words/bytes/pages into the flash array.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.3 V ±0.3 V, 5.0 V ±0.5 V):** Do not leave any power pins floating.
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.
NC		**NO CONNECT:** No internal connection to die, lead may be driven or left floating.

INTRODUCTION

Sharp's LH28F032SU 32M Flash Memory is a revolutionary architecture which enables the design of truly mobile, high performance, personal computing and communication products. With innovative capabilities, 5 V single voltage operation and very high read/write performance, the LH28F032SU is also the ideal choice for desinging embedded mass storage flash memory systems.

The LH28F032SU is the result of highly advanced packaging innovation which encapsulates two LH28F016SU die in a single 56-pin TSOP (Type I) package.

The LH28F032SU is the highest density, highest performance non-volatile read/write solution for solid-state storage applications. Its symmetrically blocked architecture (100% compatible with the LH28F008SA 8M Flash memory), extended cycling, low power 3.3 V operation, very fast write and read performance and selective block locking provide a highly flexible memory component suitable for high density memory cards, Resident Flash Arrays and PCMCIA-ATA Flash Drives. The LH28F032SU's dual read voltage enables the design of memory cards which can interchangeably be read/written in 3.3 V and 5.0 V systems. Its x8/x16 architecture allows the optimization of memroy to processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. Manufactured on Sharp's 0.6 µm ETOX™ process technology, the LH28F032SU is the most cost-effective, high-density 3.3 V memory.

DESCRIPTION

The LH28F032SU is a high performance 5 V single voltage 32M (33,554,432 bit) block erasable non-volatile random access memory organized as either 2M × 16 or 4M × 8. The LH28F032SU is built using the LH28F016SU chips encapsulated in a single 56-pin TSOP (Type I) package. Pin assignment and memory map are shown in Figure 1 and Figure 3. All pin except of $\overline{CE}_1$ are shared by both LH28F016SU, and $\overline{CE}_1$ is divided to $\overline{CE}_{1L}$ and $\overline{CE}_{1H}$ in order to select one of LH28F016SU. $\overline{CE}_{1L}$ is assigned to Number 2 pin which is $\overline{CE}_1$ in LH28F016SU, $\overline{CE}_{1H}$ is assigned to Number 3 pin which is NC in LH28F016SU (chip1), both $\overline{CE}_0$ and $\overline{CE}_{1H}$ must be 'L', and to select another LH28F016SU (chip2), both $\overline{CE}_0$ and $\overline{CE}_{1H}$ must be 'L'. If you make both $\overline{CE}_{1L}$, and $\overline{CE}_{1H}$ 'L', you can select

both chip (chip1 and chip2) at a time, except of Read operation (Array Read, Status Register Read).

Operation mode of chip1 and chip2 are as follows:

- Both chip1 and chip2 are in Deep Power-Down ($\overline{RP}$ = 'L').
- Both chip1 and chip2 are in Standby ($\overline{CE}_0$ = 'H' or $\overline{CE}_{1L}$ = $\overline{CE}_{1H}$ = 'H')
- Chip1 is a Standby and Chip2 is in active state of programming or erase, or chip1 is in active state of programming or erase and chip2 is in standby.
- Both chip1 and chip2 are in active state (impossible to perform simultaneous read from both chip). In this case chip1 and chip2 perform independent operation, for example, after input Erase command to chip1 erase or program command to chip2 is succeeded, chip1 and chip2 perform each operation concurrently. If you turns both $\overline{CE}_{1L}$ and $\overline{CE}_{1H}$ 'L' and performs full-chip erase to both chip, it takes same time of convential 16M device's that to perform chip1 and chip2 erase.

LH28F032SU is succeeded enhanced featues of LH28F016SU. Following includes principal features:

- 5 V Write/Erase Operation (5 V V_{PP})
- 3.3 V Low Power Capability
- Dedicated Block Write/Erase Protection

A $\overline{3/5}$ input pin reconfigures the device internally for optimized 3.3 V or 5.0 V read/write operation.

The LH28F032SU will be available in a 56-pin, 1.2 mm thick × 14 mm × 20 mm TSOP (Type I) package. This form factor and pinout allow for very high board layout densities.

A Command User Interface (CUI) serves as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal Algorithm Automation allows Byte/Word Writes and Block Erase operations to be executed using a Two-Write command sequence to the CUI.

The following LH28F016SU commands are also available in LH28F032SU.

- Page Buffer Writes to Flash
- Command Queuing Capability
- Automatic Data Writes During Erase
- Software Locking of Memory Blocks
- Two-Byte Successive Writes in 8-bit Systems
- Erase All Unlocked Blocks

Writing of memory data is performed in either byte or word increments typically within 8 µs, a 25% improvement over the LH28F008SA. A Block Erase operation erases each one block of 32 blocks in chip1 and chip2 in typically 0.7 seconds, independent of the other blocks, which is about 55% improvement over the LH28F008SA.

The LH28F032SU incorporates two Page Buffers of 256 Bytes (128 Words) each chip1 and chip2 to allow page data writes.

All operations are started by a sequence of Write commands to the device. Three Status Registers (described in detail later) and a $\overline{RY}/\overline{BY}$ output pin provide information on the progress of the requestd operation. Because of the chip1, 2 share $\overline{RY}/\overline{BY}$ output, they are treated as a wired-OR. When either of the chip1,2 is in active (except of read), $\overline{RY}/\overline{BY}$ outputs 'L', therefore in order to know which chip is in active, it requires to read Status Register.

Command queuing is accepted up to two commands in each chip1, 2 independently.

The LH28F032SU provides user-selectable block locking to protect code or data such as Device Drivers, PCMCIA card information, ROM-Executable O/S or Application Code. Each block has a associated nonvolatile lock-bit which determines the lock status of the block. In addition, the LH28F032SU has a masterWrite Protect pin ($\overline{WP}$) which prevents any modifications to memory blocks whose lock-bits are set.

In LH28F032SU, each chip1, 2 contains three types of Status Registers to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the LH28F008SA flash memory's Status Register. This register, when used alone, provides a straightforward upgrade capability to the LH28F032SU from a LH28F008SA-based design.
- A Global Status Register (GSR) which informs the system of command Queue status. Page Buffer status, and overallWrite Status Machine (WSM) status.
- 32 Block Status Registers (BSRs) which provide block-specific status information such as the block lock-bit status.

The GSR and BSR memory maps for Byte-Wide and Word-Wide modes are shown in Figures 4 and 5.

The LH28F032SU incorporates an open drain $\overline{RY}/\overline{BY}$ output pin. This feature allows the user to OR-tie many $\overline{RY}/\overline{BY}$ pins together in a multiple memory configuration such as a Resident Flash Array. Other configurations of the $\overline{RY}/\overline{BY}$ pin are enabled via special CUI commands and are described in detail in the LH28F016SU User's Manual.

The LH28F032SU also incorporates a dual chip-enable function with two input pins, $\overline{CE}_0$ and $\overline{CE}_{1L}$, $\overline{CE}_{1H}$. These pins have exactly the same functionality as the regular chip-enable pin $\overline{CE}$ on the LH28F008SA. For minimum chip designs, $\overline{CE}_0$ may be tied to ground and use $\overline{CE}_{1L}$ or $\overline{CE}_{1H}$ as the chip enable input. The LH28F032SU uses the logical combination of these two signals to enable or disable the entire chip. Both $\overline{CE}_0$ and $\overline{CE}_1$ must be active low to enable the device and if either one becomes inactive, the chip will be disabled.

MEMORY MAP

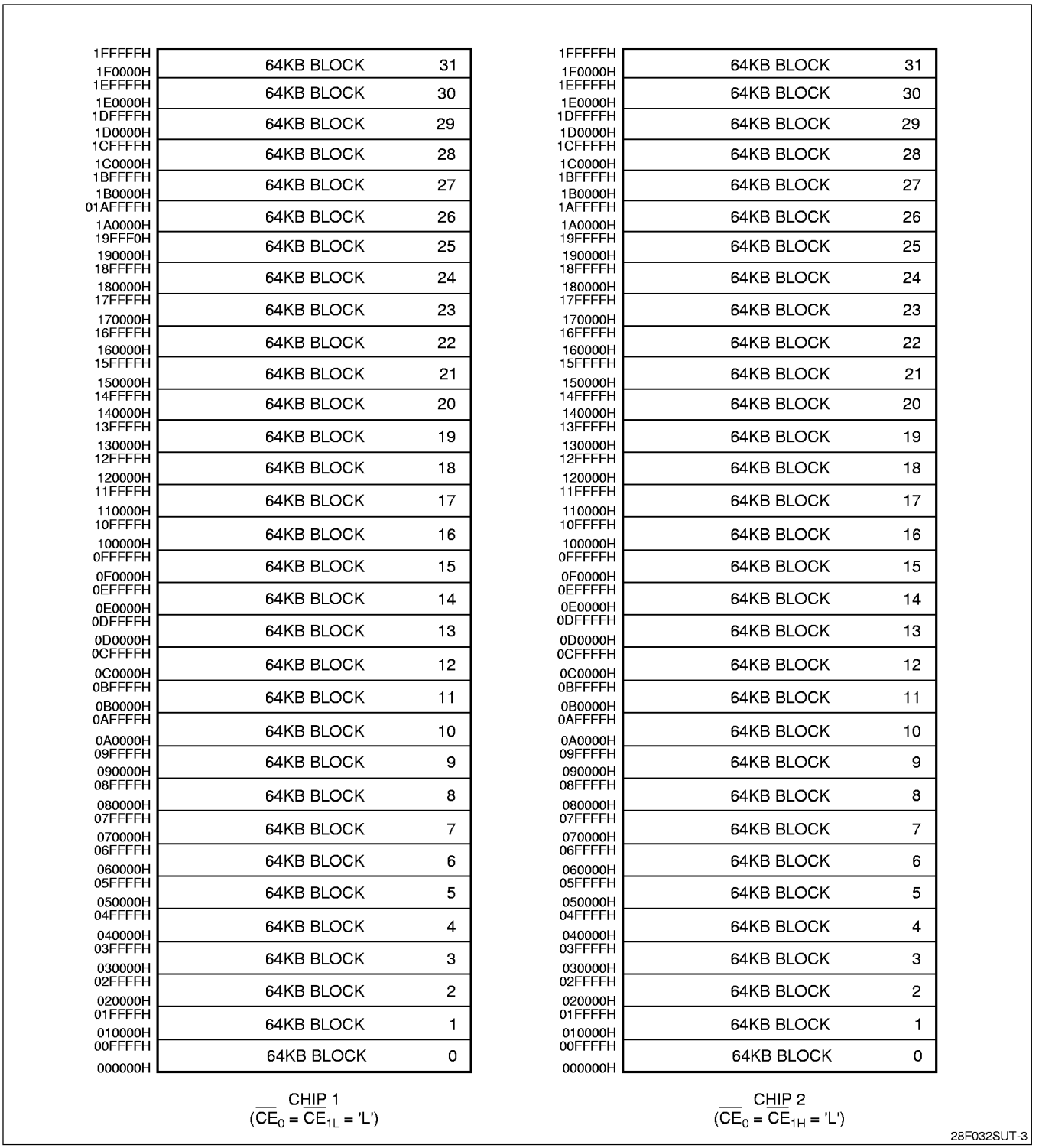


Figure 3. LH28F032SU Memory Map (Byte-Wide Mode)

This feature, along with the open drain $\overline{RY}/\overline{BY}$ pin, allows the system designer to reduce the number of control pins used in a large array of 32M devices.

The $\overline{BYTE}$ pin allows either x8 or x16 read/writes to the LH28F032SU. $\overline{BYTE}$ at logic low selects 8-bit mode with address A0 selecting between low byte and high byte. On the other hand, $\overline{BYTE}$ at logic high enables 16-bit operation with address A_1 becoming the lowest order address and address A_0 is not used (don't care). A device diagram is shown in Figure 1.

OPERATING TEMPERATURE	V_{CC} SUPPLY	MAX. ACCESS (T_{ACC})
0 - 70°C	4.75 - 5.25 V	70 ns
0 - 70°C	4.5 - 5.5 V	80 ns
0 - 70°C	3.0 - 3.6 V	120 ns

Extended Status Registers Memory Map

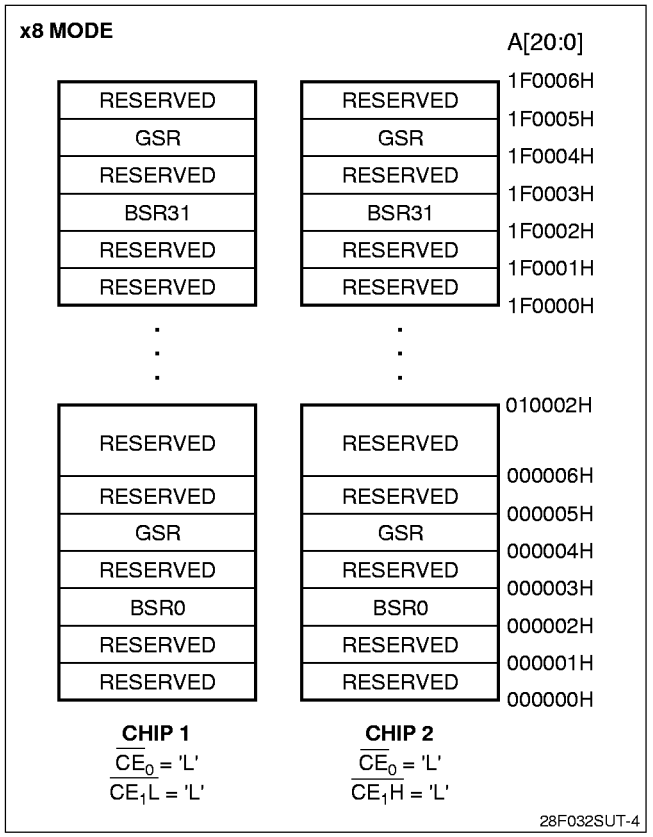


Figure 4. Extended Status Register Memory Map (Byte-Wide Mode)

The LH28F032SU is specified for a maximum access time of each version, as follows:

TheLH28F032SU incorporates an Automatic Power Saving (APS) feature which substantially reduces the active current when the device is in static mode of operation (addresses not switching).

In APS mode, the typical I_{CC} current is 4 mA at 5.0 V (2 mA at 3.3 V), both chip1, 2 are in active state.

A Deep Power-Down mode of operation is invoked when the $\overline{RP}$ (called PWD on the LH28F008SA) pin transitions low. This mode brings the device power consumption to less than 10 uA, typically, and provides additional write protection by acting as a device reset pin during power transitions. A 400 ns longer reset time than access time is required from $\overline{RP}$ switching high until outputs are again valid. In the Deep Power-Down state, the WSM is reset (any current operation will abort) and the CSR, GSR and BSR registers are cleared.

A CMOS Standby mode of operation is enabled when either $\overline{CE}_0$, or both $\overline{CE}_{1L}$ and $\overline{CE}_{1H}$, transition high and $\overline{RP}$ stays high with all input control pins at CMOS levels. In this mode, the device typically draws an I_{CC} standby current of 20 µA.

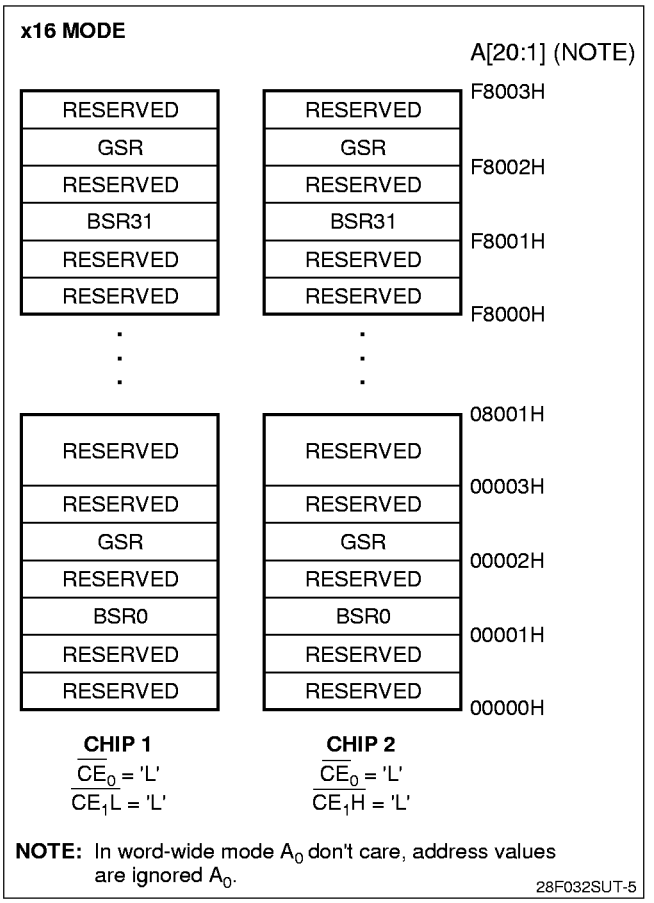


Figure 5. Extended Status Register Memory Map (Word-Wide Mode)

BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

Bus Operations for Word-Wide Mode ($\overline{BYTE}$ = V_{IH})

MODE		$\overline{RP}$	$\overline{CE}_{1L}$	$\overline{CE}_{1H}$	$\overline{CE}_0$	$\overline{OE}$	$\overline{WE}$	A_1	DQ_0 - DQ_{15}	$\overline{RY}/\overline{BY}$	NOTE
Read	Chip1 Chip2 Inhibit	V_{IH}	V_{IL} V_{IH} V_{IL}	V_{IH} V_{IL} V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X	1, 2, 7
Output Disable		V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	High-Z	X	1, 6, 7
Standby	Chip1 Chip2 Chip1, 2 Chip1, 2	V_{IH}	V_{IL} V_{IH} V_{IH} X	V_{IH} V_{IL} V_{IH} X	V_{IL} V_{IL} X V_{IH}	X	X	X	High-Z	X	1, 6, 7
Deep Power-Down		V_{IL}	X	X	X	X	X	X	High-Z	V_{OH}	1, 3
Manufacturer ID	Chip1 Chip2 Inhibit	V_{IH}	V_{IL} V_{IH} V_{IL}	V_{IH} V_{IL} V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	00B0H	V_{OH}	4
Device ID	Chip1 Chip2 Inhibit	V_{IH}	V_{IL} V_{IH} V_{IL}	V_{IH} V_{IL} V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	6688H	V_{OH}	4, 8
Write	Chip1 Chip2 Chip1, 2	V_{IH}	V_{IL} V_{IH} V_{IL}	V_{IH} V_{IL} V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X	1, 5, 6

BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS (Continued)

Bus Operations For Byte-Wide Mode ($\overline{BYTE}$ = V_{IL})

MODE		$\overline{RP}$	$\overline{CE}_{1L}$	$\overline{CE}_{1H}$	$\overline{CE}_0$	$\overline{OE}$	$\overline{WE}$	A_1	DQ_0 - DQ_{15}	$\overline{RY}/\overline{BY}$	NOTE
Read	Chip1 Chip2 Inhibit	V_{IH}	V_{IL} V_{IH} V_{IL}	V_{IH} V_{IL} V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X	1, 2, 7
Output Disable		V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	High-Z	X	1, 6, 7
Standby	Chip1 Chip2 Chip1, 2 Chip1, 2	V_{IH}	V_{IL} V_{IH} V_{IH} X	V_{IH} V_{IL} V_{IH} X	V_{IL} V_{IL} X V_{IH}	X	X	X	High-Z	X	1, 6, 7
Deep Power-Down		V_{IL}	X	X	X	X	X	X	High-Z	V_{OH}	1, 3
Manufacturer ID	Chip1 Chip2 Inhibit	V_{IH}	V_{IL} V_{IH} V_{IL}	V_{IH} V_{IL} V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	B0H	V_{OH}	4
Device ID	Chip1 Chip2 Inhibit	V_{IH}	V_{IL} V_{IH} V_{IL}	V_{IH} V_{IL} V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	88H	V_{OH}	4, 8
Write	Chip1 Chip2 Chip1, 2	V_{IH}	V_{IL} V_{IH} V_{IL}	V_{IH} V_{IL} V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X	1, 5, 6

NOTES:

1. X can be V_{IH} or V_{IL} for address or control pins except for $\overline{RY}/\overline{BY}$, which is either V_{OL} or V_{OH}.
2. $\overline{RY}/\overline{BY}$ output is open drain. When the WSM is ready, Erase is suspended or the device is in deep power-down mode, $\overline{RY}/\overline{BY}$ will be at V_{OH} if it is tied to V_{CC} through a resistor. When the $\overline{RY}/\overline{BY}$ at V_{OH} is independent of $\overline{OE}$ while a WSM operation is in progress.
3. $\overline{RP}$ at GND ± 0.2 V ensures the lowest deep power-down current.
4. A_0 and A_1 at V_{IL} provide manufacturer ID codes in x8 and x16 modes respectively. A_0 and A_1, at V_{IH} provide device ID codes in x8 and x16 modes respectively. All other addresses are set to zero.
5. Commands for different Erase operations, Data Write operations of Lock-Block operations can only be successfully completed when V_{PP} = V_{PPH}.
6. While the WSM is running, $\overline{RY}/\overline{BY}$ in Level-Mode (default) stays at V_{OL} until all operations are complete. $\overline{RY}/\overline{BY}$ goes to V_{OH} when the WSM is not busy or in erase suspend mode.
7. $\overline{RY}/\overline{BY}$ may be at V_{OL} while the WSM is busy performing various operations. For example, a status register read during a write operations.
8. Same device code of LH28F016SU.

LH28F008SA, LH28F016SU Compatible Mode Command Bus Definitions

(The following is for wach 16M chip operation.)

COMMAND	FIRST BUS CYCLE			SECOND BUS CYCLE			NOTE
	OPER.	ADDRESS	DATA	OPER.	ADDRESS	DATA	
Read Array	Write	X	FFH	Read	AA	AD	
Intelligent Identifier	Write	X	90H	Read	IA	ID	1
Read Compatible Status Register	Write	X	70H	Read	X	CSRD	2
Clear Status Register	Write	X	50H				3
Word/Byte Write	Write	X	40H	Write	WA	WD	
Alternate Word/Byte Write	Write	X	10H	Write	WA	WD	
Block Erase/Confirm	Write	X	20H	Write	BA	D0H	4
Erase Suspend/Resume	Write	X	B0H	Write	X	D0H	4

ADDRESS
AA = Array Address
BA = Block Address
IA = Identifier Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
CSRD = CSR Data
ID = Identifier Data
WD = Write Data

NOTES:
1. Following the intelligent identifier command, two Read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters Data Write, Erase or Suspend operations.
3. Clears CSR.3, CSR.4, and CSR.5. Also clears GSR.5 and all BSR.5 and BSR.2 bits. See Status register definitions.
4. While device performs Block Erase, if you issue Erase Suspend command (B0H), be sure to confirm ESS (Erase-Suspend-Status) is set to 1 on compatible status register. In the case, ESS bit was not set to 1, also completed the Erase (ESS = 0, WASM = 1), be sure to issue Resume command (D0H) after completed next Erase command. Beside, when the Erase Suspend command is issued, while the device is not in Erase, be sure to issue Resume command (D0H) after the next erase completed. When you use Erase Suspend/ Resume command, we recommend to issue serial Block Erase command (20H, D0H) and Resume command (D0H). (Refer to Performance Enhancement Command Bus Definitions.)

LH28F016SU Performance Enhancement Command Bus Definitions

Following is for each 16M bit chip operation.

COMMAND	MODE	FIRST BUS CYCLE			SECOND BUS CYCLE			THIRD BUS CYCLE			NOTE
		OPER.	ADDR.	DATA	OPER.	ADDR.	DATA	OPER.	ADDR.	DATA	
Read Extended Status Register		Write	X	71H	Read	RA	GSRD BSRD				1
Page Buffer Swap		Write	X	72H							7
Read Page Buffer		Write	X	75H	Read	PA	PD				
Single Load to Page Buffer		Write	X	74H	Write	PA	PD				
Sequential Load to Page Buffer	x8	Write	X	E0H	Write	X	BCL	Write	X	BCH	4, 6, 10
	x16	Write	X	E0H	Write	X	WCL	Write	X	WCH	4, 5, 6, 10
Page Buffer Write to Flash	x8	Write	X	0CH	Write	A0	BC (L,H)	Write	WA	BC (H, L)	3, 4, 9, 10
	x16	Write	X	0CH	Write	X	WCL	Write	WA	WCH	4, 5, 10
Two-Byte Write	x8	Write	X	FBH	Write	A0	WD (L,H)	Write	WA	WD (H, L)	3
Block Erase/Confirm		Write	X	20H	Write	BA	D0H	Write	X	D0H	11
Lock Block/Confirm		Write	X	77H	Write	BA	D0H				
Upload Status Bits/Confirm		Write	X	97H	Write	X	D0H				2
Upload Device Information		Write	X	99H	Write	X	D0H	Read	PA	PD	
Erase All Unlocked Blocks/Confirm		Write	X	A7H	Write	X	D0H	Write	X	D0H	11
$\overline{RY}/\overline{BY}$ Enable to Level-Mode		Write	X	96H	Write	X	01H				8, 11, 12
$\overline{RY}/\overline{BY}$ Pulse-On-Write		Write	X	96H	Write	X	02H				8
$\overline{RY}/\overline{BY}$ Pulse-On-Erase		Write	X	96H	Write	X	03H				8
$\overline{RY}/\overline{BY}$ Disable		Write	X	96H	Write	X	04H				8
Sleep		Write	X	F0H							
Abort		Write	X	80H							

ADDRESS
BA = Block Address
PA = Page Buffer Address
RA = Extended Register Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
PD = Page Buffer Data
BSRD = BSR Data
GSRD = GSR Data
WC (L, H) = Word Count (Low, High)
BC (L, H) = Byte Count (Low, High)
WD (L, H) = Write Data (Low, High)

NOTES:
1. RA can be the GSR address or any BSR address. See Figure 4 and 5 for Extended Status Register Memory Maps.
2. Upon device power-up, all BSR lock-bits come up locked. The Uploaded Status Bits command must be written to reflect the actual lock-bit status.
3. A_0 is automatically complemented to load second byte of data. $\overline{BYTE}$ must be at V_{IL}. A_0 value determines which WD/BC is supplied first: A_0 = 0 looks at the WDL/BCL, A_0 = 1 looks at the WDH/BCH.
4. BCH/WCH must be at 00H for this product because of the 256-Byte (128 Word) Page Buffer size and to avoid writing the Page Buffer contents into more than one 256-Byte segment within an array block. They are simply shown for future Page Buffer expandability.
5. In x16 mode, only the lower byte DQ_0 - DQ_7 is used for WCL and WCH. The upper byte DQ_8 - DQ_{15} is a don't care.
6. PA and PD (Whose count is given in cycles 2 and 3) are supplied starting in the 4th cycle which is not shown.
7. This command allows the user to swap between available Page Buffers (0 or 1).
8. These commands reconfigure $\overline{RY}/\overline{BY}$ output to one of two pulse-modes or enable and disable the $\overline{RY}/\overline{BY}$ function.
9. Write address, WA, is the Destination address in the flash array which must match the Source address in the Page Buffer. Refer to the LH28F800SU User's Manual.
10. BCL = 00H corresponds to a Byte count of 1. Similarly, WCL = 00H corresponds to a Word count of 1.
11. Unless you issue erase suspend command, it is not necessary to input D0H on third bus cycle.
12. Both chip1, 2 erase needs to input this command for both chips.

Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

CSR.6 = ERASE-SUSPEND STATUS (ESS)
1 = Erase Suspended
0 = Erase in Progress/Completed

CSR.5 = ERASE STATUS (ES)
1 = Error in Block Erasure
0 = Successful Block Erase

CSR.4 = DATA-WRITE STATUS (DWS)
1 = Error in Data Write
0 = Data Write Successful

CSR.3 = V_{PP} STATUS (VPPS)
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

NOTES:
1. $\overline{RY}/\overline{BY}$ output or WSMS bit must be checked to determine completion of an operation (Erase Suspend, Erase or Data Write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.
2. If DWS and ES are set to '1' during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.
3. The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}'s level only after the Data-Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.
4. CSR.2 - CSR.0 = Reserved for future enhancements. These bits are reserved for future use and should be masked out when polling the CSR.

GLOBAL STATUS REGISTER

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

GSR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

GSR.6 = OPERATION SUSPEND STATUS (OSS)
1 = Operation Suspended
0 = Operation in Progress/Completed

GSR.5 = DEVICE OPERATION STATUS (DOS)
1 = Operation Unsuccessful
0 = Operation Successful or Currently Running

GSR.4 = DEVICE SLEEP STATUS(DSS)
1 = Device in Sleep
0 = Device Not in Sleep
MATRIX 5/4
00 = Operation Successful or currently Running
01 = Device in Sleep Mode or Pending Sleep
10 = Operation Unsuccesful
11 = Operation Unsuccessful or Aborted

GSR.3 = QUEUE STATUS (QS)
1 = Queue Full
0 = Queue Available

GSR.2 = PAGE BUFFER AVAILABLE STATUS (PBAS)
1 = One or Two Page Buffers Available
0 = No Page Buffer Available

GSR.1 = PAGE BUFFER STATUS (PBS)
1 = Selected Page Buffer Ready
0 = Selected Page Buffer Busy

GSR.0 = PAGE BUFFER SELECT STATUS (PBSS)
1 = Page Buffer 1 Selected
0 = Page buffer 0 Selected

NOTES:
1. $\overline{RY}/\overline{BY}$ output or WSMS bit must be checked to determine completion of an operation (Block Lock, Suspend, any $\overline{RY}/\overline{BY}$ reconfiguration, Upload Status Bits, Erase or Data Write) before the appropriate Status bit (OSS or DOS) is checked for success.
2. If operation currently running, then GSR.7 = 0.
3. If device pending sleep, then GSR.7 = 0.
4. Operation aborted: Unsucccessful due to Abort command.
5. The device contains two Page Buffers.
6. Selected Page Buffer is currently busy with WSM operation.
7. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queuedf operations are completed.

BLOCK STATUS REGISTER

BS	BLS	BOS	BOAS	QS	VPPS	R	R
7	6	5	4	3	2	1	0

BSR.7 = BLOCK STATUS (BS)
1 = Ready
0 = Busy

BSR.6 = BLOCK-LOCK STATUS (BLS)
1 = Block Unlocked for Write/Erase
0 = Block Locked for Write/Erase

BSR.5 = BLOCK OPERATION STATUS (BOS)
1 = Operation Unsuccessful
0 = Operation Successful or Currently Running

BSR.4 = BLOCK OPERATION ABORT STATUS (BOAS)
1 = Operation Aborted
0 = Operation Not Aborted

MATRIX 5/4
00 = Operation Successful or Currently Running
01 = Not a valid Combination
10 = Operation Unsuccessful
11 = Operation Aborted

BSR.3 = QUEUE STATUS (QS)
1 = Queue Full
0 = Queue Available

BSR.2 = V_{PP} STATUS (V_{PPS})
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

NOTES:
1. $\overline{RY}/\overline{BY}$ output or BS bit must be checked to determine completion of an operation (Block Lock, Suspend, Erase or Data Write) before the appropriate Status bits (BOS, BLS) is checked for success.
2. The BOAS bit will not be set until BSR.7 = 1.
3. Operation halted via Abort command.
4. BSR.1-0 = RESERVED FOR FUTURE ENHANCEMENTS These bits are reserved for future use; mask them out when polling the BSRs.
5. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Temperature under bias ..... 0°C to +80°C

Storage temperature ..... -65°C to +125°C

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

V_{CC} = 3.3 V ±0.3 V Systems[4]

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
T_A	Operating Temperature, Commercial	0	70.0	°C	Ambient Temperature	1
V_{CC}	V_{CC} with Respect to GND	-0.2	7.0	V		2
V_{PP}	V_{PP} Supply Voltage with Respect to GND	-0.2	7.0	V		2
V	Voltage on any Pin (Except V_{CC}, V_{PP}) with Respect to GND	-0.5	V_{CC} + 0.5	V		2
I	Current into any Non-Supply Pin		±30	mA		
I_{OUT}	Output Short Circuit Current		100.0	mA		3

V_{CC} = 5.0 V ±0.5 V Systems[4]

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
T_A	Operating Temperature, Commercial	0	70.0	°C	Ambient Temperature	1
V_{CC}	V_{CC} with Respect to GND	-0.2	7.0	V		2
V_{PP}	V_{PP} Supply Voltage with Respect to GND	-0.2	7.0	V		2
V	Voltage on any Pin (Except V_{CC}, V_{PP}) with Respect to GND	-0.5	7.0	V		2
I	Current into any Non-Supply Pin		±30	mA		
I_{OUT}	Output Short Circuit Current		100.0	mA		3

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is -0.5 V on input/output pins. During transitions, this level may undershoot to -2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. AC specifications are valid at both voltage ranges. See DC Characteristics tables for voltage range-specific specifications.

Capacitance

For 3.3 V Systems

SYMBOL	PARAMETER	TYP.	MAX.	UNITS	TEST CONDITIONS	NOTE
C_{IN}	Capacitance Looking into an Address/Control Pin	12	16	pF	T_A = 25°C, f = 1.0 MHz	1, 2
C_{OUT}	Capacitance Looking into an Output Pin	16	24	pF	T_A = 25°C, f = 1.0 MHz	1
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications		50	pF	For V_{CC} = 3.3 V ±0.3 V	1
	Equivalent Testing Load Circuit		2.5	ns	50 Ω transmission line delay	

Capacitance

For 5.0 V Systems

SYMBOL	PARAMETER	TYP.	MAX.	UNITS	TEST CONDITIONS	NOTE
C_{IN}	Capacitance Looking into an Address/Control Pin	12	16	pF	T_A = 25°C, f = 1.0 MHz	1, 2
C_{OUT}	Capacitance Looking into an Output Pin	16	24	pF	T_A = 25°C, f = 1.0 MHz	1
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications		100	pF	For V_{CC} = 5.0 V ±0.5 V	1
			30	pF	For V_{CC} = 5.0 V ±0.25 V	
	Equivalent Testing Load Circuit		2.5	ns	25 Ω transmission line delay	
			2.5	ns	83 Ω transmission line delay	

NOTE:
1. Sampled, not 100% tested.
2. $\overline{CE}_{1L}$, $\overline{CE}_{1H}$ capacitance is half of above.

Timing Nomenclature

For 3.3 V systems use 1.5 V cross point definitions. For 5.0 V systems use the standard JEDEC crosspoint definitions. Each timing parameter consists of 5 characters. Some common examples are defined below:

t_{CE} t_{ELQV} time (t) from $\overline{CE}$ (E) going low (L) to the outputs (Q) becoming valid (V)

t_{OE} t_{GLQV} time (t) from $\overline{OE}$ (G) going low (L) to the outputs (Q) becoming valid (V)

t_{ACC} t_{AVQV} time (t) from address (A) valid (V) to the outputs (Q) becoming valid (V)

t_{AS} t_{AVWH} time (t) from address (A) valid (V) to $\overline{WE}$ (W) going high (H)

t_{DH} t_{WHDX} time (t) from $\overline{WE}$ (W) going high (H) to when the data (D) can become undefined (X)

	PIN CHARACTERS		PIN STATES
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	$\overline{CE}$ (Chip Enable)	X	Driven, but not necessarily valid
G	$\overline{OE}$ (Output Enable)	Z	High Impedance
W	$\overline{WE}$ (Write Enable)		
P	$\overline{RP}$ (Deep Power-Down Pin)		
R	$\overline{RY}/\overline{BY}$ (Ready/Busy)		
V	Any Voltage Level		
Y	$\overline{3/5}$ Pin		
5 V	V_{CC} at 4.5 V MIN.		
3 V	V_{CC} at 3.0 V MIN.		

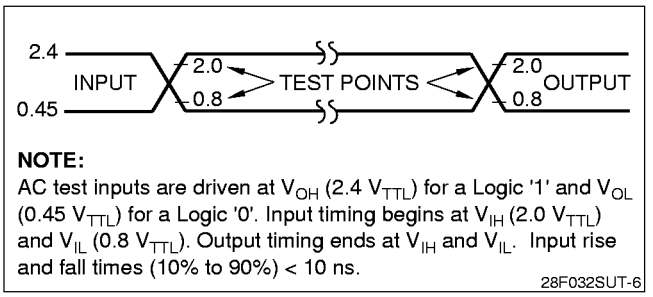


Figure 6. Transient Input/Output Reference Waveform (V_{CC} = 5.0 V)

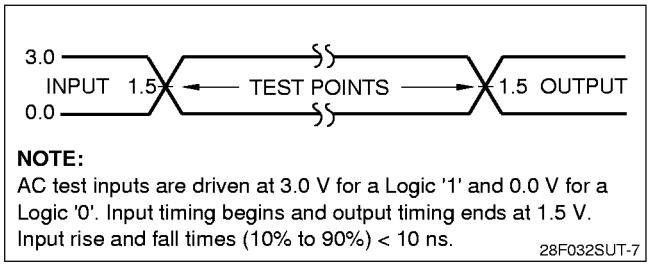


Figure 7. Transient Input/Output Reference Waveform (V_{CC} = 3.3 V)

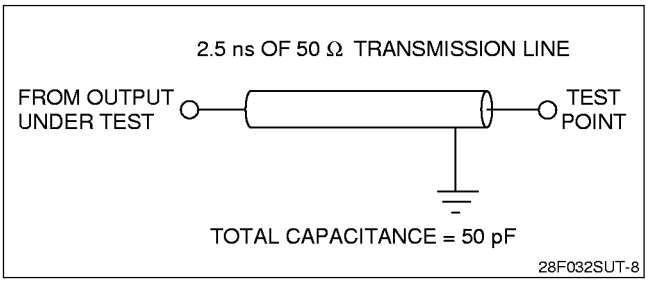


Figure 8. Transient Equivalent Testing Load Circuit (V_{CC} = 3.3 V)

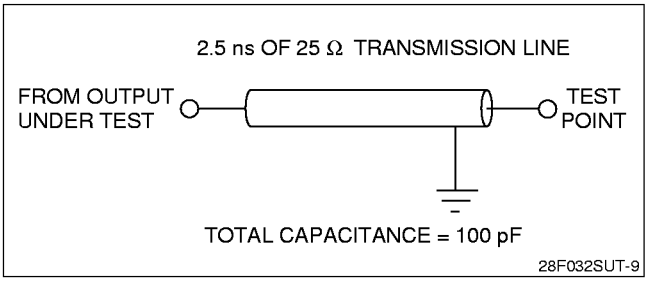


Figure 9. Transient Equivalent Testing Load Circuit (V_{CC} = 5.0 V)

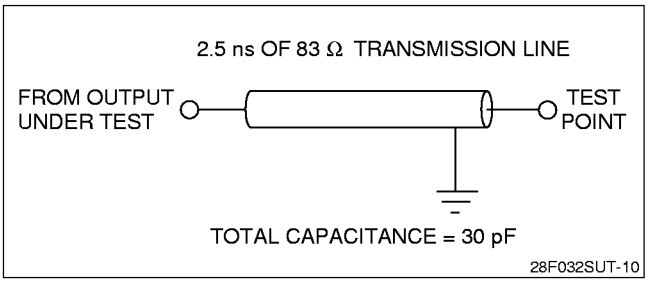


Figure 10. High Speed Transient Equivalent Testing Load Circuit (V_{CC} = 5.0 V ±5%)

DC Characteristics

V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to +70°C

$\overline{3/5}$ = Pin Set High for 3.3 V Operations

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
I_{IL}	Input Load Current			±2	µA	V_{CC} = V_{CC} MAX., V_{IN} = V_{CC} or GND	1
I_{LO}	Output Leakage Current			±20	µA	V_{CC} = V_{CC} MAX., V_{IN} = V_{CC} or GND	1
I_{CCS}	V_{CC} Standby Current	4		8	µA	V_{CC} = V_{CC} MAX., $\overline{CE}_0$, $\overline{CE}_{1\ (L\ or\ H)}$, $\overline{RP}$ = V_{CC} ±0.2 V $\overline{BYTE}$, $\overline{WP}$, $\overline{3/5}$ = V_{CC} ±0.2 V or GND ±0.2 V	1, 4, 5
		1		4	mA	V_{CC} = V_{CC} MAX., $\overline{CE}_0$, $\overline{CE}_{1\ (L\ or\ H)}$, $\overline{RP}$ = V_{IH} $\overline{BYTE}$, $\overline{WP}$, $\overline{3/5}$ = V_{IH} or V_{IL}	
I_{CCD}	V_{CC} Deep Power-Down Current	2		10	µA	$\overline{RP}$ = GND ±0.2 V	1
I_{CCR}[1]	V_{CC} Read Current	30		35	mA	V_{CC} = V_{CC} MAX., CMOS: $\overline{CE}_0$, $\overline{CE}_{1(L\ or\ H)}$ = GND ±0.2 V $\overline{BYTE}$ = GND ±0.2 V or V_{CC} ±0.2 V Inputs = GND ±0.2 V or V_{CC} ±0.2 V TTL: $\overline{CE}_0$, $\overline{CE}_{1(L\ or\ H)}$ = V_{IL}, $\overline{BYTE}$ = V_{IH} or V_{IL} Inputs = V_{IL} or V_{IH} f = 8 MHz, I_{OUT} = 0 mA	1, 3, 4, 5
I_{CCR}[2]	V_{CC} Read Current	15		20	mA	V_{CC} = V_{CC} MAX., CMOS: $\overline{CE}_0$, $\overline{CE}_{1(L\ or\ H)}$ = GND ±0.2 V $\overline{BYTE}$ = V_{CC} ±0.2 V or GND ±0.2 V Inputs = GND ±0.2 V or V_{CC} ±0.2 V TTL: $\overline{CE}_0$, $CE_{1(L\ or\ H)}$ = V_{IL}, $\overline{BYTE}$ = V_{IH} or V_{IL} Inputs = V_{IL} or V_{IH} f = 4 MHz, I_{OUT} = 0 mA	1, 3, 4, 5
I_{CCW}	V_{CC} Write Current	8		12	mA	Word/Byte Write in Progress	1, 5
I_{CCE}	V_{CC} Block Erase Current	6		12	mA	Block Erase in Progress	1, 5
I_{CCES}	V_{CC} Erase Suspend Current	3		6	mA	$\overline{CE}_0$, $\overline{CE}_{1(L\ or\ H)}$ = V_{IH} Block Erase Suspended	1, 2, 5
I_{PPS}	V_{PP} Standby Current	±1		±10	µA	$V_{PP} \leq V_{CC}$	1, 5
I_{PPD}	V_{PP} Deep Power-Down Current	0.4		10	µA	$\overline{RP}$ = GND ±0.2 V	1

DC Characteristics (Continued)

V_{CC} = 3.3 V ± 0.3 V, T_A = 0 °C to +70 °C

$\overline{3/5}$ = Pin Set High for 3.3 V Operations

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
I_{PPR}	V_{PP} Read Current			200	µA	$V_{PP} > V_{CC}$	1
I_{PPW}	V_{PP} Write Current	40		60	mA	$V_{PP} = V_{PPH}$, Word/Byte Write in Progress	1
I_{PPE}	V_{PP} Erase Current	20		40	mA	$V_{PP} = V_{PPH}$, Block Erase in Progress	1
I_{PPES}	V_{PP} Erase Suspend Current			200	µA	$V_{PP} = V_{PPH}$, Block Erase Suspended	1
V_{IL}	Input Low Voltage		-0.3	0.8	V		
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.3	V		
V_{OL}	Output Low Voltage			0.4	V	$V_{CC} = V_{CC}$ MIN. and I_{OL} = 4 mA	
V_{OH}^1	Output High Voltage		2.4		V	I_{OH} = 2.0 mA $V_{CC} = V_{CC}$ MIN.	
V_{OH}^2			V_{CC} - 0.2		V	I_{OH} = -100 µA $V_{CC} = V_{CC}$ MIN.	
V_{PPL}	V_{PP} during Normal Operations		0.0	5.5	V		
V_{PPH}	V_{PP} during Write/Erase Operations	5.0	4.5	5.5	V		
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.0		V		

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 3.3 V, V_{PP} = 5.0 V, T = 25 °C. These currents are valid for all product versions (package and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Automatic Power Saving (APS) reduces I_{CCR} to less than 1 mA in Static operation.
4. CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL Inputs are either V_{IL} or V_{IH}.
5. These are for each chip current in this mode, total device current is chip1 current and chip2 current. For example when the chip1 is in erase and chip1 is in program, total $I_{PP} = I_{PPE} + I_{PPW}$ = 40 mA + 60 mA = 100 mA.

DC Characteristics

V_{CC} = 5.0 V ± 0.5 V, T_A = 0°C to +70°C

$\overline{3.5}$ Pin Set Low for 5 V Operations

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
I_{IL}	Input Load Current			±2	µA	V_{CC} = V_{CC} MAX., V_{IN} = V_{CC} or GND	1
I_{LO}	Output Leakage Current			±20	µA	V_{CC} = V_{CC} MAX., V_{IN} = V_{CC} or GND	1
I_{CCS}	V_{CC} Standby Current	5		10	µA	V_{CC} = V_{CC} MAX., $\overline{CE}_0$, $\overline{CE}_{1(L\text{ or }H)}$, $\overline{RP}$ = V_{CC} ±0.2 V $\overline{BYTE}$, $\overline{WP}$, $\overline{3/5}$ = V_{CC} ±0.2 V or GND ±0.2 V	1, 4, 5
		2		4	mA	V_{CC} = V_{CC} MAX., $\overline{CE}_0$, $\overline{CE}_{1(L\text{ or }H)}$, $\overline{RP}$ = V_{IH} $\overline{BYTE}$, $\overline{WP}$, $\overline{3/5}$ = V_{IH} or V_{IL}	
I_{CCD}	V_{CC} Deep Power-Down Current	2		10	µA	$\overline{RP}$ = GND ±0.2 V	1
I_{CCR}[1]	V_{CC} Read Current	50		60	mA	V_{CC} = V_{CC} MAX., CMOS: $\overline{CE}_0$, $\overline{CE}_{1(L\text{ or }H)}$ = GND ±0.2 V $\overline{BYTE}$ = GND ±0.2 V or V_{CC} ±0.2 V Inputs = GND ±0.2 V or V_{CC} ±0.2 V TTL: $\overline{CE}_0$, $\overline{CE}_{1\ (L\text{ or }H)}$ = V_{IL}, $\overline{BYTE}$ = V_{IH} or V_{IL} Inputs = V_{IL} or V_{IH} f = 10 MHz, I_{OUT} = 0 mA	1, 3, 4, 5
I_{CCR}[2]	V_{CC} Read Current	30		35	mA	V_{CC} = V_{CC} MAX., CMOS: $\overline{CE}_0$, $\overline{CE}_{1(L\text{ or }H)}$ = GND ±0.2 V $\overline{BYTE}$ = V_{CC} ±0.2 V or GND ±0.2 Inputs = GND ±0.2 V or V_{CC} ±0.2 V TTL: $\overline{CE}_0$, $\overline{CE}_{1(L\text{ or }H)}$ = V_{IL}, $\overline{BYTE}$ = V_{IH} or V_{IL} Inputs = V_{IL} or V_{IH} f = 5 MHz, I_{OUT} = 0 mA	1, 3, 4, 5
I_{CCW}	V_{CC} Write Current	25		35	mA	Word/Byte Write in Progress	1, 5
I_{CCE}	V_{CC} Block Erase Current	18		25	mA	Block Erase in Progress	1, 5
I_{CCES}	V_{CC} Erase Suspend Current	5		10	mA	$\overline{CE}_0$, $\overline{CE}_{1(L\text{ or }H)}$ = V_{IH} Block Erase Suspended	1, 2, 5
I_{PPS}	V_{PP} Standby Current	±1		±10	µA	$V_{PP} \leq V_{CC}$	1, 5
I_{PPD}	V_{PP} Deep Power-Down Current	0.4		10	µA	$\overline{RP}$ = GND ±0.2 V	1

DC Characteristics (Continued)

V_{CC} = 5.0 V ± 0.5 V, T_A = 0 °C to +70 °C

$\overline{3.5}$ Pin Set Low for 5 V Operations

SYMBOL	PARAMETER	TYPE	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
I_{PPR}	V_{PP} Read Current	65		200	µA	$V_{PP} > V_{CC}$	1
I_{PPW}	V_{PP} Write Current	40		60	mA	$V_{PP} = V_{PPH}$, Word/Byte Write in Progress	1
I_{PPE}	V_{PP} Erase Current	20		40	mA	$V_{PP} = V_{PPH}$, Block Erase in Progress	1
I_{PPES}	V_{PP} Erase Suspend Current	65		200	µA	$V_{PP} = V_{PPH}$, Block Erase Suspended	1
V_{IL}	Input Low Voltage		-0.5	0.8	V		
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V		
V_{OL}	Output Low Voltage			0.45	V	$V_{CC} = V_{CC}$ MIN. and I_{OL} = 5.8 mA	
V_{OH}^1	Output High Voltage		0.85 V_{CC}		V	I_{OH} = -2.5 mA $V_{CC} = V_{CC}$ MIN.	
V_{OH}^2			V_{CC} - 0.4		V	I_{OH} = -100 µA $V_{CC} = V_{CC}$ MIN.	
V_{PPL}	V_{PP} during Normal Operations		0.0	5.5	V		
V_{PPH}	V_{PP} during Write/Erase Operations	5.0	4.5	5.6	V		
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.0		V		

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0 V, V_{PP} = 5.0 V, T = 25 °C. These currents are valid for all product versions (package and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Automatic Power Saving (APS) reduces I_{CCR} to less than 1 mA in Static operation.
4. CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL Inputs are either V_{IL} or V_{IH}.
5. These are for each chip current in this mode, total device current is chip1 current and chip2 current. For example when the chip1 is in erase and chip1 is in program, total $I_{PP} = I_{PPE} + I_{PPW}$ = 40 mA + 60 mA = 100 mA.

AC Characteristics - Read Only Operations[1]

V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
t_{AVAV}	Read Cycle Time	120		ns	
t_{AVEL}	Address Setup to $\overline{CE}$ Going Low	10		ns	3, 4
t_{AVGL}	Address Setup to $\overline{OE}$ Going Low	0		ns	3, 4
t_{AVQV}	Address to Output Delay		120	ns	
t_{ELQV}	$\overline{CE}$ to Output Delay		120	ns	2
t_{PHQV}	$\overline{RP}$ High to Output Delay		620	ns	
t_{GLQV}	$\overline{OE}$ to Output Delay		45	ns	2
t_{ELQX}	$\overline{CE}$ to Output in Low Z	0		ns	3
t_{EHQZ}	$\overline{CE}$ to Output in High Z		50	ns	3
t_{GLQX}	$\overline{OE}$ to Output in Low Z	0		ns	3
t_{GHQZ}	$\overline{OE}$ to Output in High Z		30	ns	3
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ change, whichever occurs first	0		ns	3
t_{FLQV} t_{FHQV}	$\overline{BYTE}$ to Output Delay		120	ns	3
t_{FLQZ}	$\overline{BYTE}$ Low to Output in High Z		30	ns	3
t_{ELFL} t_{ELFH}	$\overline{CE}$ Low to $\overline{BYTE}$ High of Low		5	ns	3

AC Characteristics - Read Only Operations[1] (Continued)

T_A = 0°C to +70°C

SYMBOL	PARAMETER	V_{CC} = 5.0 V ± 0.25V		V_{CC} = 5.0 V ± 0.5V		UNITS	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Read Cycle Time	70		80		ns	
t_{AVEL}	Address Setup to $\overline{CE}$ Going Low	10		10		ns	3, 4
t_{AVGL}	Address Setup to $\overline{OE}$ Going Low	0		0		ns	3, 4
t_{AVQV}	Address to Output Delay		70		80	ns	
t_{ELQV}	$\overline{CE}$ to Output Delay		70		80	ns	2
t_{PHQV}	$\overline{RP}$ High to Output Delay		400		480	ns	
t_{GLQV}	$\overline{OE}$ to Output Delay		30		35	ns	2
t_{ELQX}	$\overline{CE}$ to Output in Low Z	0		0		ns	3
t_{EHQZ}	$\overline{CE}$ to Output in High Z		25		30	ns	3
t_{GLQX}	$\overline{OE}$ to Output in Low Z	0		0		ns	3
t_{GHQZ}	$\overline{OE}$ to Output in High Z		25		30	ns	3
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ change, whichever occurs first	0		0		ns	3
t_{FLQV} t_{FHQV}	BYTE to Output $\overline{Delay}$		70		80	ns	3
t_{FLQZ}	BYTE Low to $\overline{Output}$ in High Z		25		30	ns	3
t_{ELFL} t_{ELFH}	$\overline{CE}$ Low to BYTE High or $\overline{Low}$		5		5	ns	3

NOTES:
1. See AC Input/Output Reference Waveforms for timing measurements, Figures 5 and 6.
2. $\overline{OE}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{CE}$ without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. This timing parameter is used to latch the correct BSR data onto the outputs.

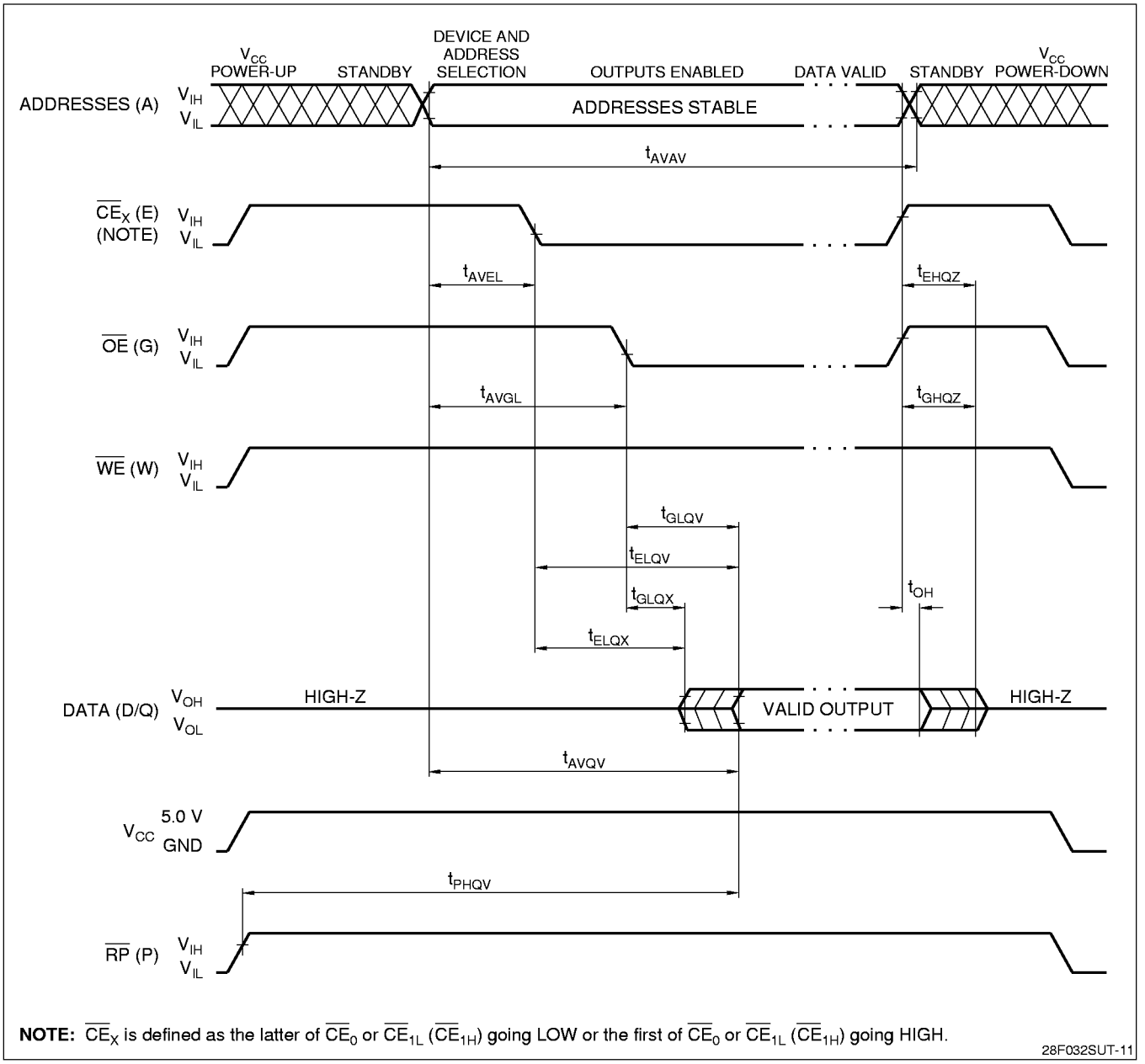


Figure 11. Read Timing Waveforms

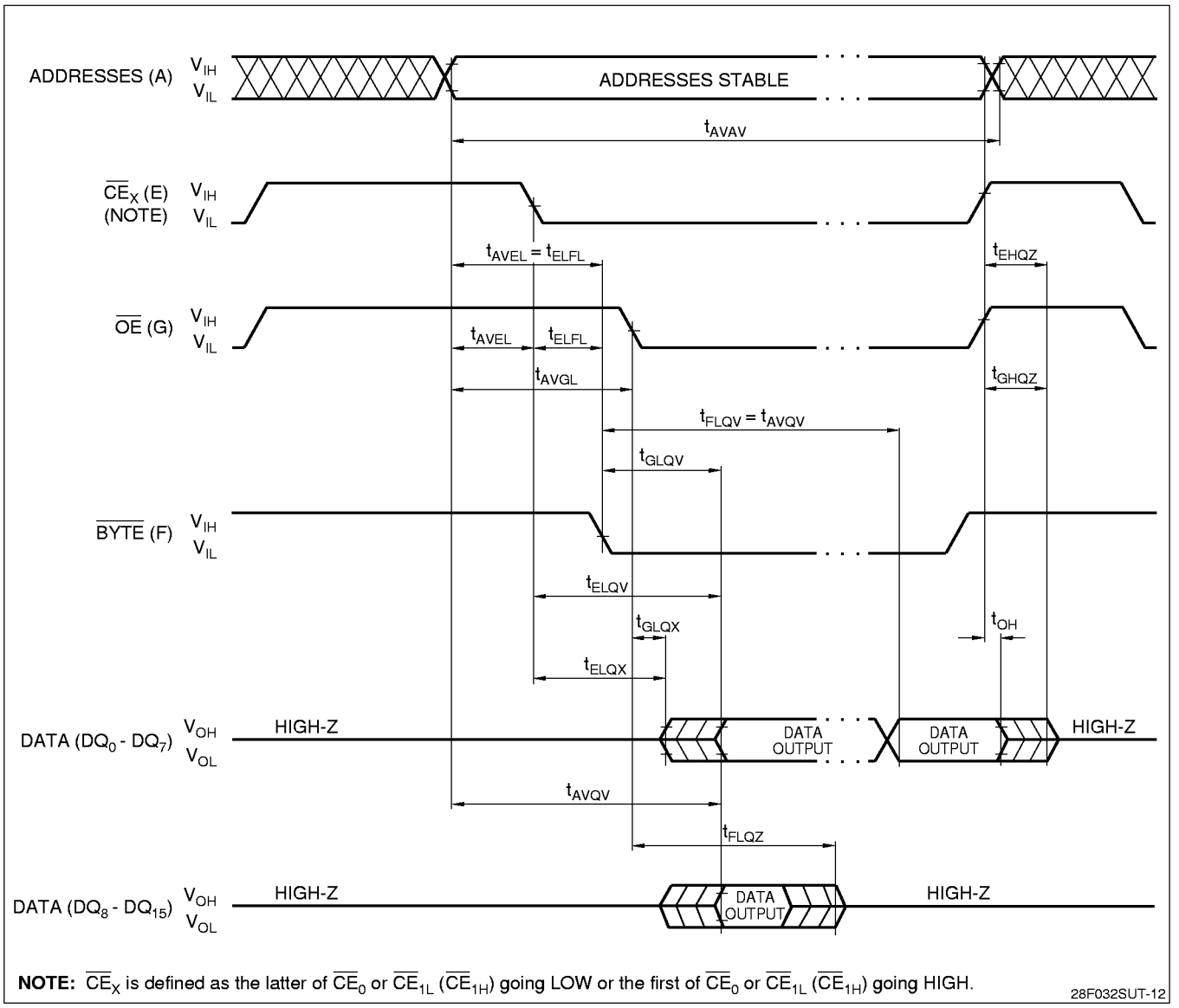


Figure 12. BYTE Timing Waveforms

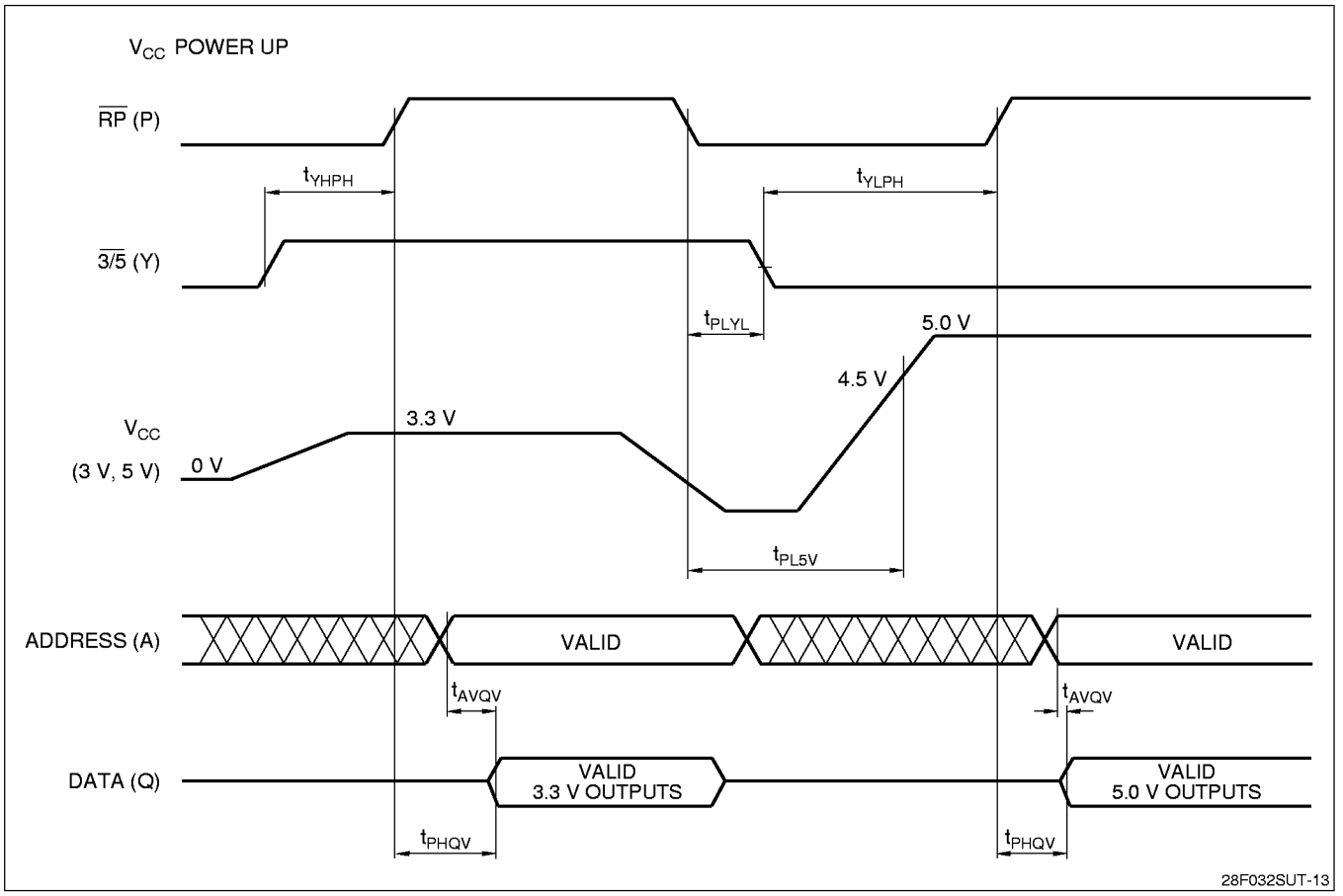


Figure 13. V_{CC} Power-UP and $\overline{RP}$ Reset Waveforms

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
t_{PLYL} t_{PLYH}	$\overline{RP}$ Low to $\overline{3/5}$ Low (High)	0		µs	
t_{YLPH} t_{YHPH}	$\overline{3/5}$ Low (High) to RP# High	2		µs	1
t_{PL5V} t_{PL3V}	$\overline{RP}$ Low to V_{CC} at 4.5 V MIN. (to V_{CC} at 3.0 V MIN. or 3.6 V MAX.)	0		µs	2
t_{AVQV}	Address Valid to Data Valid for V_{CC} = 5 V ± 10%		80	ns	3
t_{PHQV}	$\overline{RP}$ High to Data Valid for V_{CC} = 5 V ± 10%		480	ns	3

NOTES:
$\overline{CE}_0$, $\overline{CE}_1$ and $\overline{OE}$ are switched low after Power-Up.
1. Minimum of 2 µs is required to meet the specified t_{PHQV} times.
2. The power supply may start to switch concurrently with $\overline{RP}$ going Low. $\overline{RP}$ is required to stay low, until V_{CC} stays at recommended operating voltage.
3. The address access time and $\overline{RP}$ high to data valid time are shown for 5 V V_{CC} operation. Refer to the AC Characteristics Read Only Operations 3.3 V V_{CC} operation and all other speed options.

AC Characteristics for $\overline{WE}$ - Controlled Command Write Operations[1]

V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	NOTE
t_{AVAV}	Write Cycle Time		120		ns	
t_{VPWH}	V_{PP} Setup to $\overline{WE}$ Going High		100		ns	3
t_{PHEL}	$\overline{RP}$ Setup to $\overline{CE}$ Going Low		480		ns	
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		10		ns	
t_{AVWH}	Address Setup to $\overline{WE}$ Going High		75		ns	2, 6
t_{DVWH}	Data Setup to $\overline{WE}$ Going High		75		ns	2, 6
t_{WLWH}	$\overline{WE}$ Pulse Width		75		ns	
t_{WHDX}	Data Hold from $\overline{WE}$ High		10		ns	2
t_{WHAX}	Address Hold from $\overline{WE}$ High		10		ns	2
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ High		10		ns	
t_{WHWL}	$\overline{WE}$ Pulse Width High		45		ns	
t_{GHWL}	Read Recovery before Write		0		ns	
t_{WHRL}	$\overline{WE}$ High to $\overline{RY}/\overline{BY}$ Going Low			100	ns	
t_{RHPL}	$\overline{RP}$ Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0		ns	3
t_{PHWL}	$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low		1		µs	
t_{WHGL}	Write Recovery before Read		95		ns	
t_{QVVL}	V_{PP} Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0		µs	
t_{WHQV}^{1}	Duration of Byte Write Operation	12	5		µs	4, 5
t_{WHQV}^{2}	Duration of Block Erase Operation		0.3		s	4

AC Characteristics for $\overline{WE}$ - Controlled Command Write Operations[1] (Continued)

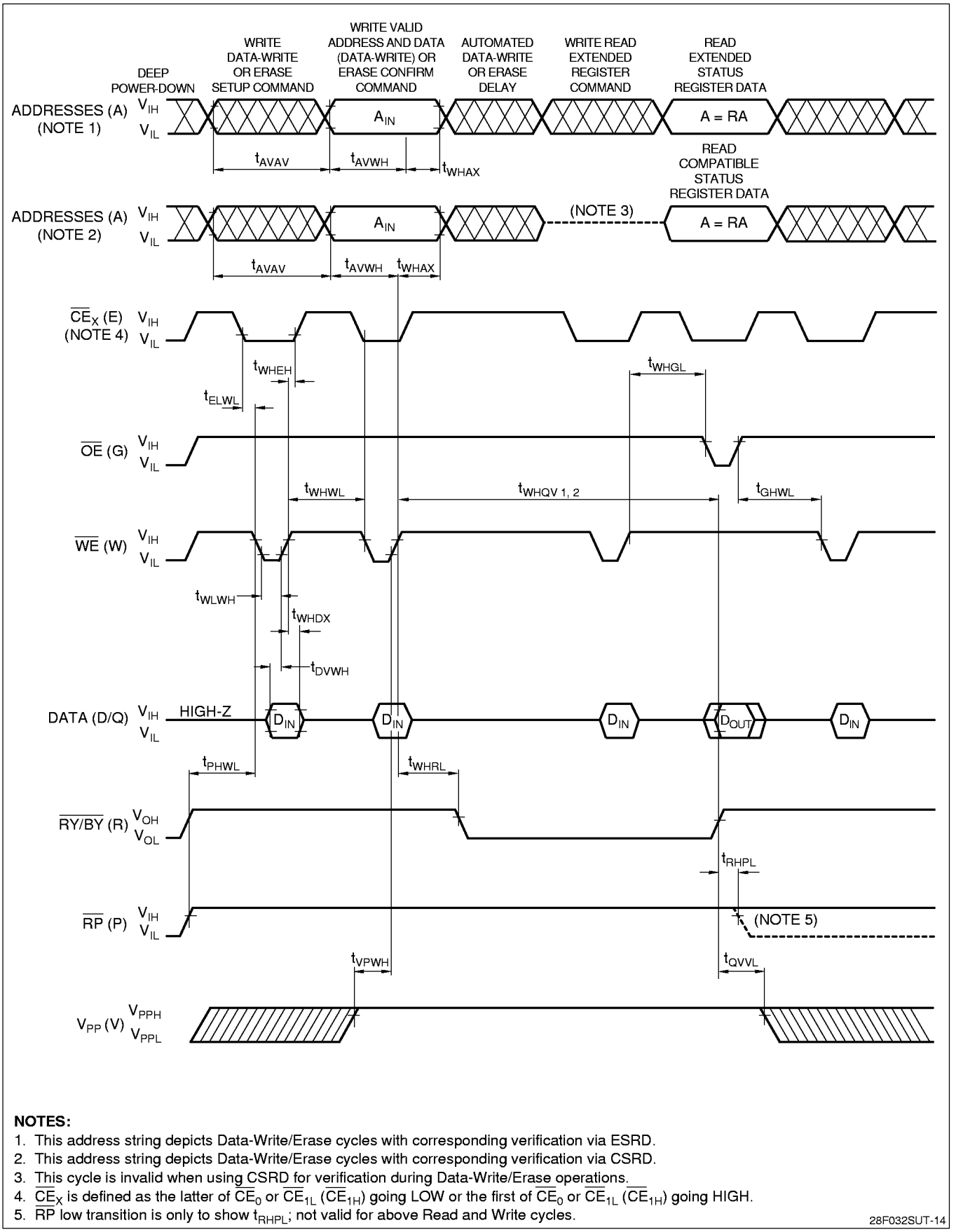
V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	V_{CC} = 5.0 V ± 0.25 V			V_{CC} = 5.0 V± 0.5 V			UNITS	NOTE
		TYP.	MIN.	MAX.	TYP.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time		70			80		ns	
t_{VPWH}	V_{PP} Setup to $\overline{WE}$ Going High		100			100		ns	3
t_{PHEL}	$\overline{RP}$ Setup to $\overline{CE}$ Going Low		480			480		ns	
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		0			0		ns	
t_{AVWH}	Address Setup to $\overline{WE}$ Going High		50			50		ns	2, 6
t_{DVWH}	Data Setup to $\overline{WE}$ Going High		50			50		ns	2, 6
t_{WLWH}	$\overline{WE}$ Pulse Width		40			40		ns	
t_{WHDX}	Data Hold from $\overline{WE}$ High		0			0		ns	2
t_{WHAX}	Address Hold from $\overline{WE}$ High		10			10		ns	2
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ High		10			10		ns	
t_{WHWL}	$\overline{WE}$ Pulse Width High		30			30		ns	
t_{GHWL}	Read Recovery before Write		0			0		ns	
t_{WHRL}	$\overline{WE}$ High to $\overline{RY}/\overline{BY}$ Going Low			100			100	ns	
t_{RHPL}	$\overline{RP}$ Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0			0		ns	3
t_{PHWL}	$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low		1			1		µs	
t_{WHGL}	Write Recovery before Read		60			65		ns	
t_{QVVL}	V_{PP} Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0			0		µs	
$t_{WHQV}{}^{1}$	Duration of Byte Write Operation	6	4.5		6	4.5		µs	4, 5
$t_{WHQV}{}^{2}$	Duration of Block Erase Operation		0.3			0.3		s	4

NOTES:

$\overline{CE}$ is defined as the latter of $\overline{CE}_0$ or $\overline{CE}_{1L}$ ($\overline{CE}_{1H}$) going Low or the first of $\overline{CE}_0$ or $\overline{CE}_{1L}$ ($\overline{CE}_{1H}$) going High.

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Word/Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of $\overline{CE}$ for all Command Write Operations.



NOTES:
1. This address string depicts Data-Write/Erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations.
4. $\overline{CE}_X$ is defined as the latter of $\overline{CE}_0$ or $\overline{CE}_{1L}$ ($\overline{CE}_{1H}$) going LOW or the first of $\overline{CE}_0$ or $\overline{CE}_{1L}$ ($\overline{CE}_{1H}$) going HIGH.
5. $\overline{RP}$ low transition is only to show t_{RHPL}; not valid for above Read and Write cycles.

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Figure 14. AC Waveforms for Command Write Operations

AC Characteristics for $\overline{CE}$ - Controlled Command Write Operations[1]

V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	NOTE
t_{AVAV}	Write Cycle Time		120		ns	
t_{PHWL}	$\overline{RP}$ Setup to $\overline{WE}$ Going Low		480		ns	3
t_{VPEH}	V_{PP} Set up to $\overline{CE}$ Going High		100		ns	3
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low		0		ns	
t_{AVEH}	Address Setup to $\overline{CE}$ Going High		75		ns	2, 6
t_{DVEH}	Data Setup to $\overline{CE}$ Going High		75		ns	2, 6
t_{ELEH}	$\overline{CE}$ Pulse Width		75		ns	
t_{EHDX}	Data Hold from $\overline{CE}$ High		10		ns	2
t_{EHAX}	Address Hold from $\overline{CE}$ High		10		ns	2
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ High		10		ns	
t_{EHEL}	$\overline{CE}$ Pulse Width High		45		ns	
t_{GHEL}	Read Recovery before Write		0		ns	
t_{EHRL}	$\overline{CE}$ High to $\overline{RY}/\overline{BY}$ Going Low			100	ns	
t_{RHPL}	$\overline{RP}$ Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0		ns	3
t_{PHEL}	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low		1		µs	
t_{EHGL}	Write Recovery before Read		95		ns	
t_{QVVL}	V_{PP} Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0		µs	
t_{EHQV}^{1}	Duration of Byte Write Operation	12	5		µs	4, 5
t_{EHQV}^{2}	Duration of Block Erase Operation		0.3		s	4

AC Characteristics for $\overline{CE}$ - Controlled Command Write Operations[1] (Continued)

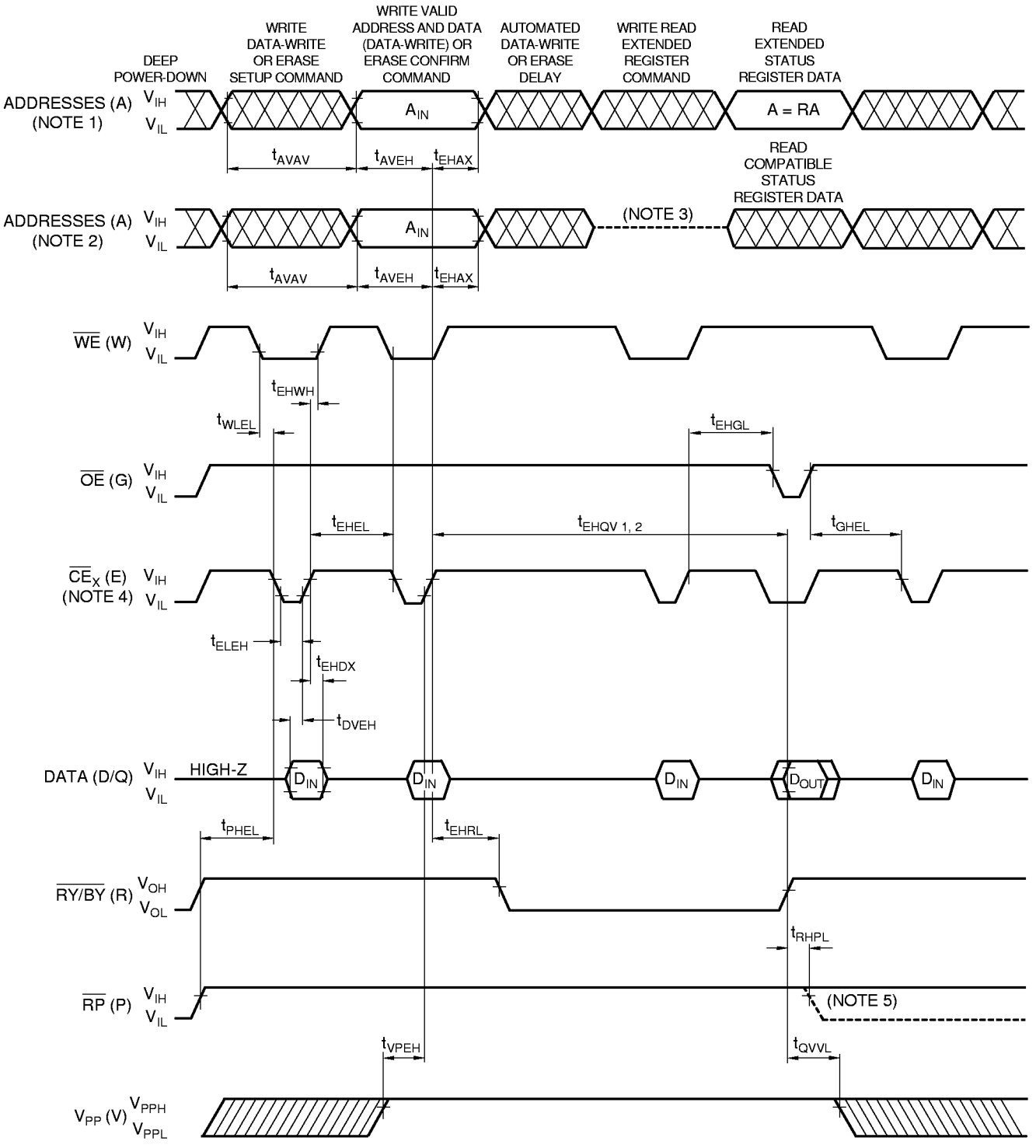
T_A = 0°C to +70°C

SYMBOL	PARAMETER	V_{CC} = 5.0 V ± 0.25 V			V_{CC} = 5.0 V ± 0.5 V			UNITS	NOTE
		TYP.	MIN.	MAX.	TYP.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time		70			80		ns	
t_{PHWL}	$\overline{RP}$ Setup to $\overline{WE}$ Going Low		480			480		ns	
t_{VPEH}	V_{PP} Set up to $\overline{CE}$ Going High		100			100		ns	
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low		0			0		ns	
t_{AVEH}	Address Setup to $\overline{CE}$ Going High		50			50		ns	2, 6
t_{DVEH}	Data Setup to $\overline{CE}$ Going High		50			50		ns	2, 6
t_{ELEH}	$\overline{CE}$ Pulse Width		40			50		ns	
t_{EHDX}	Data Hold from $\overline{CE}$ High		0			0		ns	2
t_{EHAX}	Address Hold from $\overline{CE}$ High		10			10		ns	2
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ High		10			10		ns	
t_{EHEL}	$\overline{CE}$ Pulse Width High		30			50		ns	
t_{GHEL}	Read Recovery before Write		0			0		ns	
t_{EHRL}	$\overline{CE}$ High to $\overline{RY}/\overline{BY}$ Going Low			100				ns	
t_{RHPL}	$\overline{RP}$ Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0			0		ns	3
t_{PHEL}	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low		1			1		µs	
t_{EHGL}	Write Recovery before Read		60			80		ns	
t_{QVVL}	V_{PP} Hold from Valid Status Register Data and $\overline{RY}/\overline{BY}$ High		0			0		µs	
t_{EHQV}^{1}	Duration of Byte Write Operation	8	4.5		8	4.5		µs	4, 5
t_{EHQV}^{2}	Duration of Block Erase Operation		0.3			0.3		s	4

NOTES:

$\overline{CE}$ is defined as the latter of $\overline{CE}_0$ or $\overline{CE}_{1L}$ ($\overline{CE}_{1H}$) going Low or the first of $\overline{CE}_0$ or $\overline{CE}_{1L}$ ($\overline{CE}_{1H}$) going High.

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Word/Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of $\overline{CE}$ for all Command Write Operations.



NOTES:

1. This address string depicts Data-Write/Erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations.
4. $\overline{CE}_X$ is defined as the latter of $\overline{CE}_0$ or $\overline{CE}_{1L}$ ($\overline{CE}_{1H}$) going LOW or the first of $\overline{CE}_0$ or $\overline{CE}_{1L}$ ($\overline{CE}_{1H}$) going HIGH.
5. $\overline{RP}$ low transition is only to show t_{RHPL}; not valid for above Read and Write cycles.

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Figure 15. Alternate AC Waveforms for Command Write Operations

AC Characteristics for Page Buffer Write Operations[1]

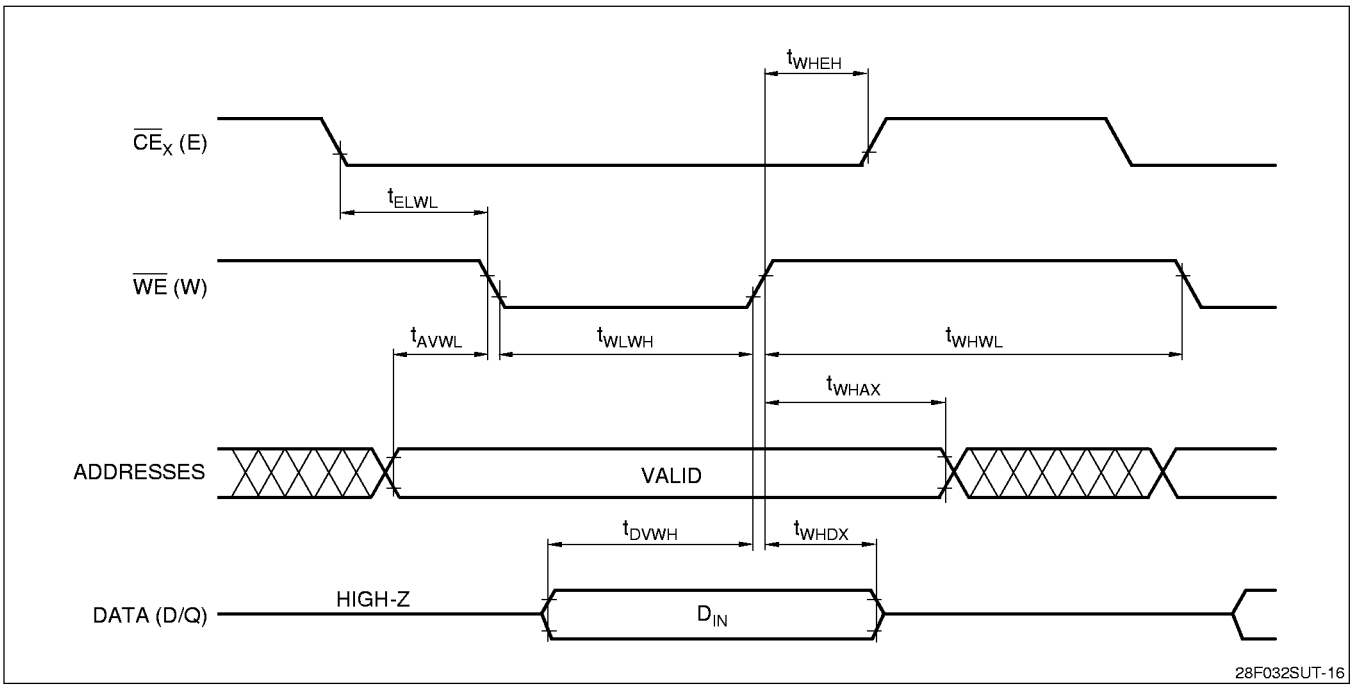
V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	TYP.	MIN.	MAX.	UNITS	NOTE
t_{AVAV}	Write Cycle Time		120		ns	
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		10		ns	
t_{AVWL}	Address Setup to $\overline{WE}$ Going Low		0		ns	3
t_{DVWH}	Data Setup to $\overline{WE}$ Going High		75		ns	2
t_{WLWH}	$\overline{WE}$ Pulse Width		75		ns	
t_{WHDX}	Data Hold from $\overline{WE}$ High		10		ns	2
t_{WHAX}	Address Hold from $\overline{WE}$ High		10		ns	2
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ High		10		ns	
t_{WHWL}	$\overline{WE}$ Pulse Width High		45		ns	
t_{GHWL}	Read Recovery before Write		0		ns	
t_{WHGL}	Write Recovery before Read		95		ns	

T_A = 0°C to +70°C

SYMBOL	PARAMETER	V_{CC} = 5.0 V ± 0.25 V			V_{CC} = 5.0 V ± 0.5 V			UNITS	NOTE
		TYP.	MIN.	MAX.	TYP.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time		70			80		ns	
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		0			0		ns	
t_{AVWL}	Address Setup to $\overline{WE}$ Going Low		0			0		ns	3
t_{DVWH}	Data Setup to $\overline{WE}$ Going High		50			50		ns	2
t_{WLWH}	$\overline{WE}$ Pulse Width		40			50		ns	
t_{WHDX}	Data Hold from $\overline{WE}$ High		0			0		ns	2
t_{WHAX}	Address Hold from $\overline{WE}$ High		10			10		ns	2
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ High		10			10		ns	
t_{WHWL}	$\overline{WE}$ Pulse Width High		30			30		ns	
t_{GHWL}	Read Recovery before Write		0			0		ns	
t_{WHGL}	Write Recovery before Read		60			65		ns	

NOTES:
$\overline{CE}$ is defined as the latter of $\overline{CE}_0$ or $\overline{CE}_{1L}$ ($\overline{CE}_{1H}$) going Low or the first of $\overline{CE}_0$ or $\overline{CE}_{1L}$ ($\overline{CE}_{1H}$) going High.
1. These are $\overline{WE}$ controlled write timings, equivalent $\overline{CE}$ controlled write timings apply.
2. Sampled, but not 100% tested.
3. Address must be valid during the entire $\overline{WE}$ Low pulse.



Figuer 16. Page Buffer Write Timing Waveforms

Erase and Word/Byte Write Performance

V_{CC} = 3.3 V ±0.3 V, T_A = 0°C to +70°C

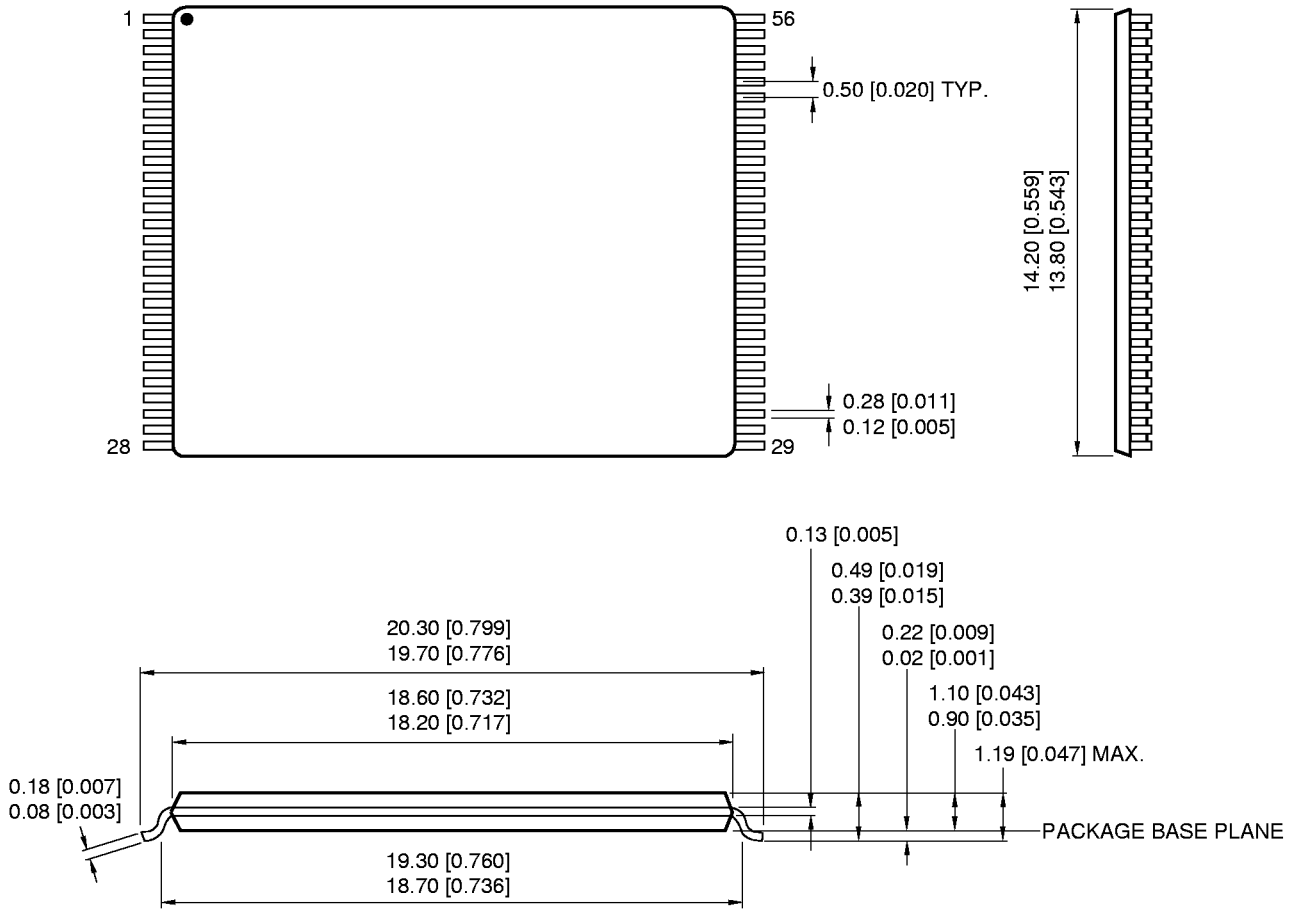
SYMBOL	PARAMETER	TYP.(1)	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
t_{WHRH}^1	Word/Byte Write Time	12			µs		2
t_{WHRH}^2	Block Write Time	0.8		2.1	s	Byte Write Mode	2
t_{WHRH}^3	Block Write Time	0.4		1.0	s	Word Write Mode	2
	Block Erase Time	0.9		10	s		2
	Full Chip Erase Time	28.8			s		2

V_{CC} = 5.0 V ±0.5 V, T_A = 0°C to +70°C

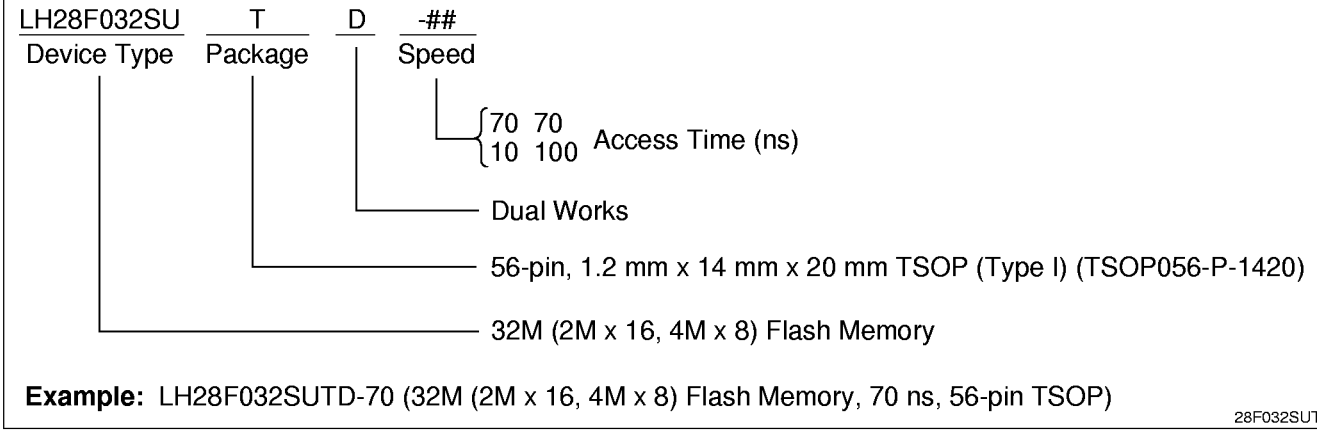
SYMBOL	PARAMETER	TYP.(1)	MIN.	MAX.	UNITS	TEST CONDITIONS	NOTE
t_{WHRH}^1	Word/Byte Write Time	8			µs		2
t_{WHRH}^2	Block Write Time	0.54		2.1	s	Byte Write Mode	2
t_{WHRH}^3	Block Write Time	0.27		1.0	s	Word Write Mode	2
	Block Erase Time	0.7		10	s		2
	Full Chip Erase Time	22.4			s		2

NOTES:
1. 25°C, V_{PP} = 5.0 V Sampled.
2. Excludes System-Level Overhead.

56TSOP (TSOP056-P-1420)



ORDERING INFORMATION



Example: LH28F032SUTD-70 (32M (2M x 16, 4M x 8) Flash Memory, 70 ns, 56-pin TSOP)

28F032SUT-17