PRELIMINARY PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LH28F160SPN-50

16M Flash Memory

(Model No.: LHF16P03)

Spec No.: FM983017

Issue Date: March 13, 1998

SHARP

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CONTENTS

1 INTRODUCTION

This datasheet contains LH28F160SPXX specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

1.1 FEATURES

- High Speed Page Mode Read Performance
  - Normal access time : 100ns
  - Page mode access time : 50ns
- Page Depth
  - 16 Bytes / 8 Words
- High Speed Write Performance
  - 32 Bytes x 2 plane Page Buffer
- High - Density Symmetrically - Blocked Architecture
  - Thirty - two 64K-byte Erasable Blocks
- Enhanced Data Protection Features
  - Flexible Block Locking
  - Erase/Write Lockout during Power Transitions
- Low Power Management
  - Deep Power - Down Mode : 15 μA (Max)
- User - Configurable x8 or x16 Operation
- Extended Cycling Capability
  - 100,000 Block Erase Cycles
  - 3.2 Million Block Erase Cycles/Chip
- Enhanced Automated Suspend Options
  - Write Suspend to Read
  - Block Erase Suspend to Write
  - Block Erase Suspend to Read
- Power Supply
  - 3.3V $\pm$ 0.3V
- Package
  - 44SOP
- Not designed or rated as radiation hardened

1.2 Product Overview

The LH28F160SPXX is a high-performance 16Mbit Page Mode Flash memory organized as 2Mbitx8/1Mbitx16. The 2MB of data is arranged in thirty-two 64K-byte blocks which are individually erasable, lockable, and unlockable in-system. The memory map is shown in Figure 3.

A Command User Interface (CUI) serve as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations.

Each block can be independently erased 100,000 times (3.2 million block erases per device). Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

(Multi) Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of thirty-two block lock-bits and RP# to lock and unlock blocks. Block lock-bits gate block erase, full chip erase and (multi) word/byte write operations. Block lock-bit configuration operations (Set Block Lock-Bit and Clear Block Lock-Bits commands) set and cleared block lock-bits.

The status register indicates when the WSM's block erase, full chip erase, (multi) word/byte write or block lock-bit configuration operation is finished.

The normal access time and page mode access time are 100ns(t AVQV) and 50ns(t PAVQV) over the commercial temperature range (0°C to +70°C) and Vcc supply voltage range of 3.0V - 3.6V. When CE# and RP# pins are at Vcc, the Icc CMOS standby mode is enabled. When the RP# pin is at GND, deep power - down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time(tPHQV) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time(tPHEL) from RP# - high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared. The device is available in 44 - SOP. Pinout is shown in Figure 2.

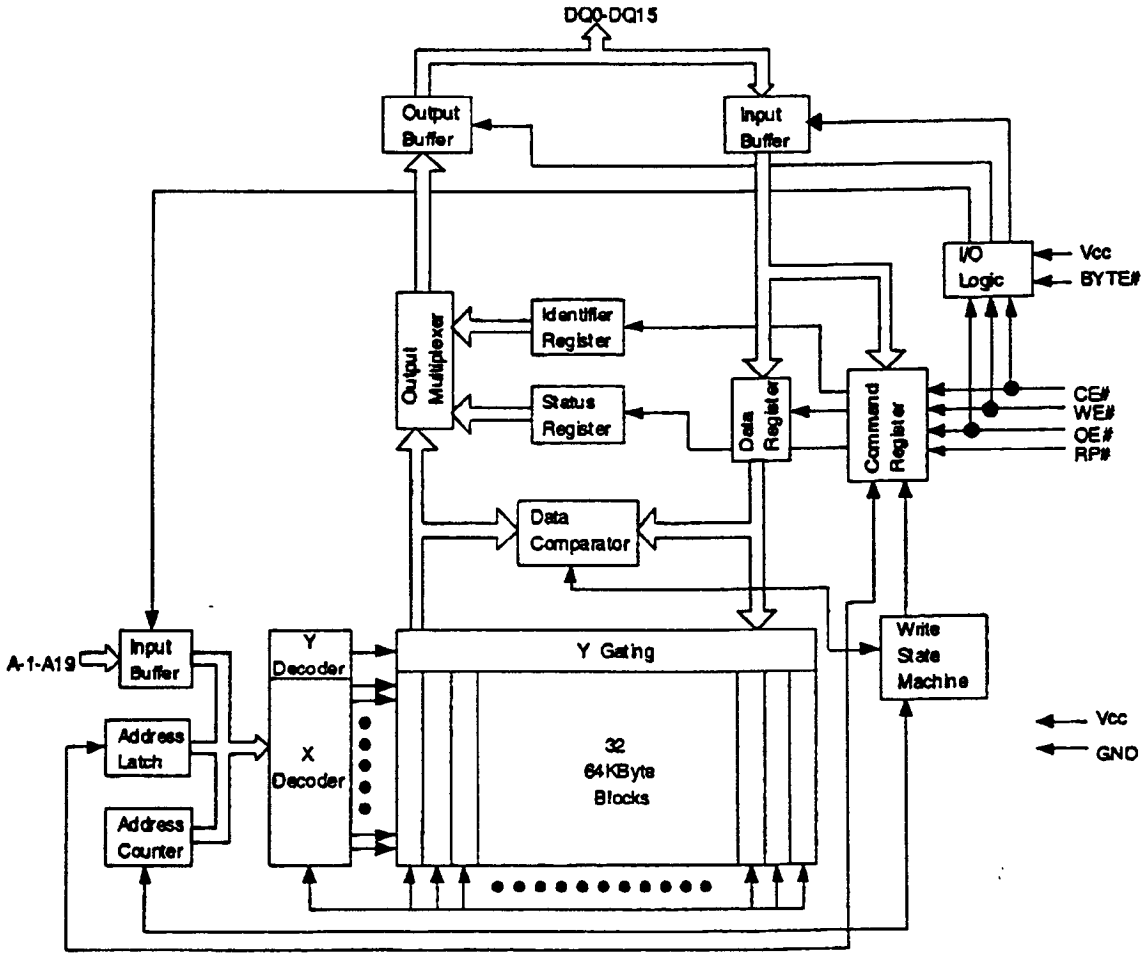


Figure 1. Block Diagram

Table 1. Pin Description

Symbol	Type	Pin name and function
A_{-1}-A_{19}	INPUT	**ADDRESS INPUTS** : Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle. A_{-1}-A_2 are address inputs for page mode read operation.
DQ_0-DQ_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS** : DQ_0~DQ_7 : Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. DQ_8~DQ_{15} : Inputs data during CUI write cycles in x16 mode; outputs data during memory array read cycles in x16 mode; not used for status register and identifier code read mode. Data pins float to high-impedance when the chip is deselected, outputs are disabled, or in x8 mode(BYTE#=VIL). Data is internally latched during a write cycle.
CE#	INPUT	**CHIP ENABLE** : Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RP#	INPUT	**RESET/DEEP POWER-DOWN** : Puts the device in deep power-down mode and resets internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. Block erase, word write, or lock-bit configuration with VIH < RP# <VHH produce spurious results and should not be attempted.
OE#	INPUT	**OUTPUT ENABLE** : Controls the device's outputs during a read cycle.
WE#	INPUT	**WRITE ENABLE** : Controls writes to the CPU and array block. Addresses and data are lached on the rising edge of the WE# pulse.
Vcc	SUPPLY	**DEVICE POWER SUPPLY** : With Vcc ≦ VLKO, all write attempts to the flash memory are inhibited. Device operations at invalid Vcc voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	**GROUND** : Do not float any ground pins.

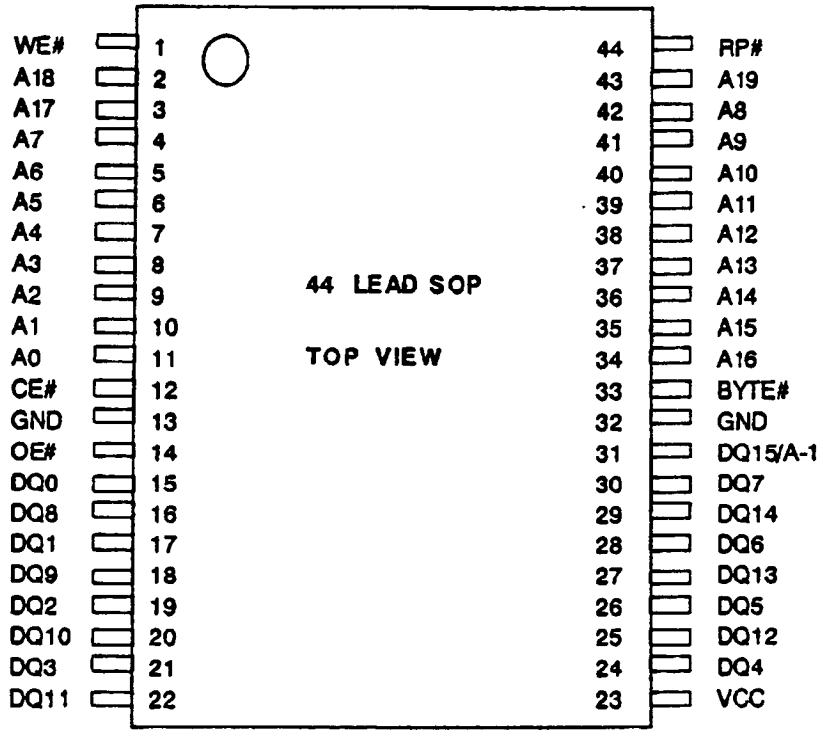


Figure 2. SOP 44-Lead Pinout

2 PRINCIPLES OF OPERATION

The LH28F160SPXX Flash memory includes an on-chip WSM to manage block erase, full chip erase, (multi) word/byte write and block lock-bit configuration functions. It allows for 100% TTL-Level control inputs, fixed power supplies during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, and minimal processor overhead with RAM-LIKE interface timing.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register and identifier codes can be accesssed through the CUI. All functions associated with altering memory contents – block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, status and identifier codes – are accessed via the CUI and verified through the status register.

The CUI contents serve as input to the WSM, which controls the block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, or outputs status register data.

Interface software that initiates and polls progress of block erase, full chip erase, (multi) word/byte write and block lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the READ Array command. Block erase suspend allows system software to suspend a block erase to read or write data from any other block. Write suspend allows system software to suspend a (multi) word/byte write to read data from any other flash memory array locations.

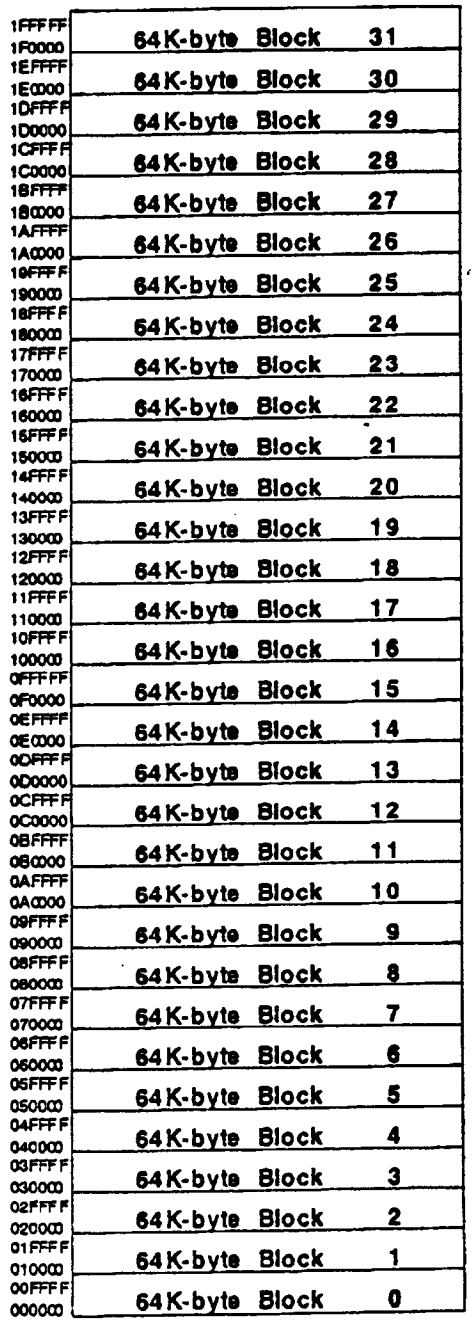


Figure 3. Memory Map

2.1 Data Protection

All write functions are disabled when Vcc is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, full chip erase and (multi) word/byte write operations.

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Four control pins dictate the data flow in and out of the component: CE#, OE#, WE# and RP#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output(DQ0 - DQ15) control and when active drives the selected memory data onto the I/O bus. WE# must be at V_{IH} and RP# must be at V_{IH} or V_{HH}. Figure 15 illustrates read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins DQ0 - DQ15 are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ0-DQ15 outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, word write, or lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at V_{IL} initiates the deep power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, word write, or lock-bit configuration modes, RP#-low will abort the operation. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high(V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes

The read identifier codes operation outputs the manufacture code, device code, block status codes for each block(see Figure 4). Using the manufacture and device codes, the system CPU can automatically match the device with its proper algorithms. The block status codes identify locked or unlocked block setting and erase completed or erase uncompleted condition.

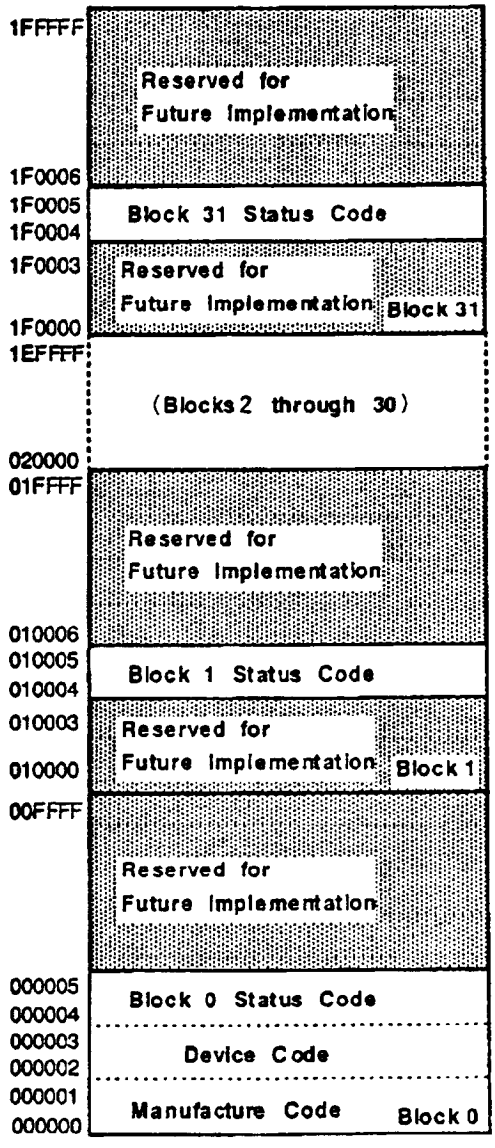


Figure 4. Device Identifier Code Memory Map

3.6 Write

Writing commands to the CPU enable reading of device data and identifier codes. They also control inspection and clearing of the status register.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word/byte Write command requires the command and address of the location to be written. Set Block Lock-Bit command requires the command and block address within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE#(whichever goes high first). Standard microprocessor write timings are used. Figures 16 and 17 illustrate WE# and CE# controlled write operations.

4 COMMAND DEFINITIONS

Device operations are selected by writing specific commands into CUI. Table 3 defines these commands.

Table 2. Bus Operations(BYTE# = VIH)

Mode	Notes	RP#	CE#	OE#	WE#	Address	DQ0-15
Read	1,6	VIH or VHH	VIL	VIL	VIH	X	DOUT
Output Disable		VIH or VHH	VIL	VIH	VIH	X	High Z
Standby		VIH or VHH	VIH	X	X	X	High Z
Deep Power-Down	2	VIL	X	X	X	X	High Z
Read Identifier Codes	6	VIH or VHH	VIL	VIL	VIH	See Figure 4	Note 3
Write	4,5,6	VIH or VHH	VIL	VIH	VIL	X	DIN

Table 2.1 Bus Operations(BYTE# = VIL)

Mode	Notes	RP#	CE#	OE#	WE#	Address	DQ0-7
Read	1,6	VIH or VHH	VIL	VIL	VIH	X	DOUT
Output Disable		VIH or VHH	VIL	VIH	VIH	X	High Z
Standby		VIH or VHH	VIH	X	X	X	High Z
Deep Power-Down	2	VIL	X	X	X	X	High Z
Read Identifier Codes	6	VIH or VHH	VIL	VIL	VIH	See Figure 4	Note 3
Write	4,5,6	VIH or VHH	VIL	VIH	VIL	X	DIN

NOTES :

1. X can be VIL or VIH for control pins and addresses.
2. RP# at GND $\pm$ 0.2V ensures the lowest deep power-down current.
3. See Section 4.2 for read identifier code data.
4. VIH<RP#<VHH produce spurious results and should not be attempted.
5. Refer to Table 3 for valid DIN during a write operation.
6. Don't use the timing both OE# and WE# are VIL.

Table 3. Command Definitions[10]

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper[1]	Addr[2]	Data[3]	Oper[1]	Addr[2]	Data[3]
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase Setup/Confirm	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase Setup/Confirm	2		Write	X	30H	Write	X	D0H
Word/Byte Write Setup/Write	2	5,6	Write	WA	40H	Write	WA	WD
Alternate Word/Byte Write Setup/Write	2	5,6	Write	WA	10H	Write	WA	WD
Multi Word/Byte Write Setup/Confirm	≥4	9	Write	WA	E8H	Write	WA	N
Block Erase and (Multi) Word/byte Write Suspend	1	5	Write	X	B0H			
Confirm and Block Erase and (Multi) Word/byte Write Resume	1	5	Write	X	D0H			
Block Lock-Bit Set Setup/Confirm	2	7	Write	BA	60H	Write	BA	01H
Block Lock-Bit Reset Setup/Confirm	2	8	Write	X	60H	Write	X	D0H

NOTES :

1. BUS operations are defined in Table 2 and Table 2.1.
2. X=Any valid address within the device.
   IA=Identifier Code Address: see Figure 4.
   BA=Address within the block being erased or locked.
   WA=Address of memory location to be written.
3. SRD=Data read from status register. See Table 6 for a description of the status register bits.
   WD=Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high).
   ID=Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacture, device and block status codes. See Section 4.2 for read identifier code data.
5. If the block is locked, RP# must be at VHH to enable block erase or (multi) word/byte write operations. Attempts to issue a block erase or (multi) word/byte write to a locked block while RP# is VIH.
6. Either 40H or 10H are recognized by the WSM as the word write setup.
7. RP# must be at VHH to set a block lock-bit.
8. RP# must be at VHH to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits.
9. Following the Third Bus cycle, input the write address and write data of 'N'+1 times. Finally, input the confirm command 'D0H'.
10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend and (Multi) Word/byte Write Suspend command. RP# can be V_{IH} or V_{HH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer, device, block lock configuration and block erase status (see Table 4 for identifier code values). To terminate the operation, write another valid command. RP# can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the following information can be read:

Table 4. Identifier Codes

Code	Address	Data
Manufacture Code	00000 00001	B0
Device Code	00002 00003	70
Block Status Code	x0004(1) x0005(1)	
·Block is Unlocked		DQ_0=0
·Block is Locked		DQ_0=1
·Last erase operation completed successfully		DQ_1=0
·Last erase operation did not completed successfully		DQ_1=1
·Reserved for Future Use		DQ_{2-7}

NOTE:
1. X selects the specific block status code to be read. See Figure 8 for the device identifier code memory map.

4.3 Read Status Register Command

The status register may be read to determine when a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration is complete and whether the operation completed successfully (see Table 6). It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE# whichever occurs. OE# or CE# must toggle to V_{IH} before further reads to update the status register latch. RP# can be V_{IH} or V_{HH}. The extended status register may be read to determine multi byte write availability (see Table 6.1). The extended status register may be read at any time by writing the Multi Byte Write command. After writing this command, all subsequent read operations output data from the extended status register, until another valid command is written. The contents of the extended status register are latched on the falling edge of OE# or CE#, whichever occurs last in the read cycle. Multi Byte Write command must be re-issued to update the extended status register latch.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 6). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurs during the sequence. To clear the status register, the Clear Status Register command (50H) is written. RP# can be V_{IH} or V_{HH}. This command is not functional during block erase, full chip erase, (multi) word/byte write block lock-bit configuration, block erase suspend or (multi) word/byte write suspend modes.

4.5 Block Erase Command

Block erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect block erase completion by analyzing status register bit SR.7. When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Successful block erase requires that the corresponding block lock-bit be cleared or if set, that RP#=V_{HH}, If block erase is attempted when the corresponding block lock-bit is set and RP#=V_{IH}, SR.1 and SR.5 will be set to "1".

4.6 Full Chip Erase Command

This command followed by a confirm command (DOH) erases all of the unlocked blocks. A full chip erase setup is first written, followed by a full chip erase confirm. After a confirm command is written, device erases the all unlocked blocks from block 0 to Block 31 block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle full chip erase sequence is written , the device automatically outputs status register data when read (see Figure 6). The CPU can detect full chip erase completion by analyzing status register bit SR.7. When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. If error is detected on a block during full chip erase operation, WSM stops erasing. Reading the block valid status by issuing Read ID Codes command or informs which blocks failed to its erase. This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". When RP#=V_{HH}, all blocks are erased independent of block lock-bits status. When RP#=V_{IH}, only unlocked blocks are erased. In this case, SR.1 and SR.4 will not be set to "1". Full chip erase can not be suspended.

4.7 Word/Byte Write Command

Word/byte write is executed by a two-cycle command sequence. Word/Byte Write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect the completion of the word/byte write event by analyzing status register bit SR.7. When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command. Successful word/byte write requires that the corresponding block lock-bit be cleared or, if set, that RP#=V_{HH}. If word/byte write is attempted when the corresponding block lock-bit is set and RP#=V_{IH}, SR.1 and SR.4 will be set to "1". Word/byte write operations with V_{IH}<RP#<V_{HH} produce spurious results and should not be attempted.

4.8 Multi Word/Byte Write Command

Multi word/byte write is executed by at least four-cycle or up to 35-cycle command sequence. Up to 32 bytes in x8 mode (16 words in x16 mode) can be loaded into the buffer and written to the Flash Array. First, multi word/byte write setup (E8H) is written with the write address. At this point, the device automatically outputs extended status register data (XSR) when read (see Figure 8,9). If extended status register bit XSR.7 is 0, no Multi Word/Byte Write command is available and multi word/byte write setup which just has been written is ignored. To retry, continue monitoring XSR.7 by writing multi word/byte write setup with write address until XSR.7 transitions to 1. When XSR.7 transitions to 1, the device is ready for loading the data to the buffer. A word/byte count (N) is written with write address. After writing a word/byte count(N), the device automatically turns back to output status register data. The word/byte count (N) must be less than or equal to 1FH in x8 mode (0FH in x16 mode). On the next write, device start address is written with buffer data. Subsequent writes provide additional device address and data, depending on the count. All subsequent address must lie within the start address plus the count. After the final buffer data is written, write confirm (D0H) must be written. This initiates WSM to begin copying the buffer data to the Flash Array. An invalid Multi Wore/Byte Write command sequence will result in both status register bits SR.4 and SR.5 being set to "1". For additional multi word/byte write, write another multi word/byte write setup and check XSR.7. The Multi Word/Byte Write command can be queued while WSM is busy as long as XSR.7 indicates "1", because LHE16PXX has two buffers. If an error occurs while writing, the device will stop writing and flush next multi word/byte write command loaded in multi word/byte write command. Status register bit SR.4 will be set to "1". No multi word/byte write command is available if either SR.4 or SR.5 are set to "1". SR.4 and SR.5 should be cleared before issuing multi word/byte write command. If a multi word/byte write command is attempted past an erase block boundary, the device will write the data to Flash Array up to an erase block boundary and then stop writing. Status register bits SR.4 and SR.5 will be set to "1".

Successful multi word/byte write requires that the corresponding block lock-bit be cleared or, if set, that RP#=V_{HH}. If multi byte write is attempted when the corresponding block lock-bit is set and RP#=V_{IH}, SR.1 and SR.4 will be set to "1".

4.9 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or (multi) word/byte-write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1").

At this point, a Read Array command can be written to read data from blocks others than that which is suspended. A (Multi) Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the (Multi) Word/Byte Write Suspend command (see Section 4.10), a (multi) word/byte write operation can also be suspended. During a (multi) word/byte write operation with block erase suspended, status register bit SR.7 will return to "0". However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 10). RP# must also remain at V_{IH}. Block erase cannot resume until (multi) word/byte write operations initiated during block erase suspend have completed.

4.10 (Multi) Word/Byte Write Suspend Command

The (Multi) Word/Byte Write Suspend command allows (multi) word/byte write interruption to read data in other flash memory locations. Once the (multi) word/byte write process starts, writing the (Multi) Word/Byte Write Suspend command requests that the WSM suspend the (multi) word/byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the (Multi) Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the (multi) word/byte write operation has been suspended (both will be set to "1"). Specification t_{WHRH1} defines the (multi) word/byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid comands while (multi) word/byte write is suspended are Read Status Register and (Multi) Word/Byte Write Resume. After (Multi) Word/Byte Write Resume command is written to the flash memory, the WSM will continue the (multi) word/byte write process. Status register bits SR.2 and SR.7 will automatically clear. After the (Multi) Word/Byte Write command is written, the device automatically outputs status register data when read (see Figure11).

4.11 Set Block Lock-Bit Command

A flexible block locking and unlocking scheme is enabled via block lock-bits. The block lock-bits gate program and erase operation. With RP#=VHH, individual block lock-bits can be set using the Set Block Lock-Bit command. See Table 5 for a summary of hardware and software write protection options.

Set block lock-bit is executed by a two-cycle command sequence. The set block lock-bit setup along with appropriate block or device address is written followed by the set block lock-bit confirm (and an address within the block to be locked). The WSM then controls the set block lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 12). The CPU can detect the completion of the set block lock-bit event by analyzing status register bit SR.7.

When the set block lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally set. An invalid Set Block Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1".

A successful set block lock-bit operation requires RP#=V_{HH}. If it is attempted with RP#=V_{IH}, SR.1 and SR.4 will be set to "1" and the operation will fail. Set block lock-bit operations with V_{IH}<RP#< V_{HH}, produce spurious results and should not be attempted.

4.12 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With RP#=V_{HH}, block lock-bits can be cleared using only the Clear Block Lock-Bits command. See Table 5 for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 13). The CPU can detect completion of the clear block lock-bits event by analyzing status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". A successful clear block lock-bits operation requires RP#=V_{HH}. If it is attempted with RP#=V_{IH}, SR.1 and SR.5 will be set to "1" and the operation will fail. Clear block lock-bits operations with V_{IH}<RP#<V_{HH} produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to VCC transitioning out of valid range or RP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values.

Table 12. Write Protection Alternatives

Operation	Block Lock-Bit	RP#	Effect
Block Erase, (Multi) Word/Byte Write	0	V_{IH} or V_{HH}	Block Erase and (Multi) Word/Byte Write Enabled
	1	V_{IH}	Block is Locked. Block Erase and (Multi) Word/Byte Write Disabled
		V_{HH}	Block Lock-Bit Override. Block Erase and (Multi) Word/Byte Write Enabled
Full Chip Erase	0,1	V_{IH}	All unlocked blocks are erased, locked blocks are not erased
	X	V_{HH}	All blocks are erased
Set Block Lock-Bit	X	V_{IH}	Set Block Lock-Bit Disabled
		V_{HH}	Set Block Lock-Bit Enabled
Clear Block Lock-Bits	X	V_{IH}	Clear Block Lock-Bits Disabled
		V_{HH}	Clear Block Lock-Bits Enabled

Table 14. Status Register Definition

WSMS	BESS	ECBLBS	WSBLBS	R	WSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS
1 = Error in Erase or Clear Block Lock-Bits
0 = Successful Erase or Clear Block Lock-Bits

SR.4 = WRITE AND SET BLOCK LOCK-BIT STATUS
1 =Error in Write or Set Block Lock-Bit
0 = Successful Write or Set Block Lock-Bit

SR.3 = RESERVED FOR FUTURE ENHANCEMENTS

SR.2 = WRITE SUSPEND STATUS
1 = Write Suspended
0 = Write in Progress/Completed

SR.1 = DEVICE PROTECT STATUS
1 = Block Lock-Bit and/or WP# Lock Detected, Operation Abort
0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

Check SR.7 to determine block erase, full chip erase, (multi) word/byte write or block lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (multi) word/byte write, block lock-bit configuration attempt, an .Inproper command sequence was entered.

SR.3 is reserved for future use and should be masked out when polling the status register.

SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates block lobk-bit, and WP# only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set and/or RP# is not V_{HH}. Reading the block lock configuration codes after writing the Read Identifier Codes command indecates block lock-bit status.

SR.0 is reserved for future use and should be masked out when polling the status register.

Table 14.1. Extended Status Register Definition

SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

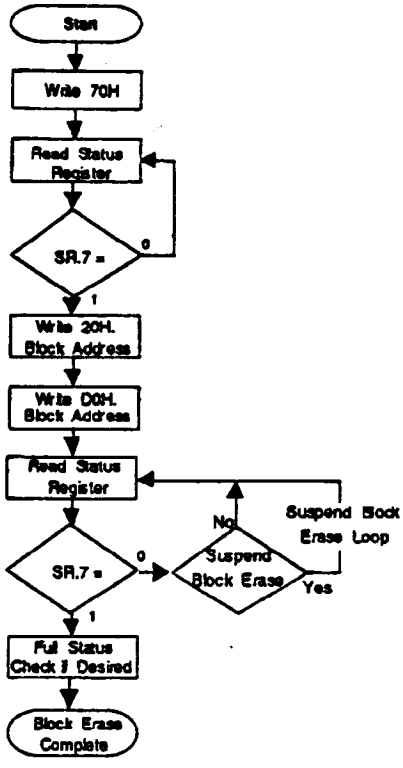
XSR.7 = STATE MACHINE STATUS
1 = Multi Word/Byte Write available
0 = Multi Word/Byte Write not available

XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

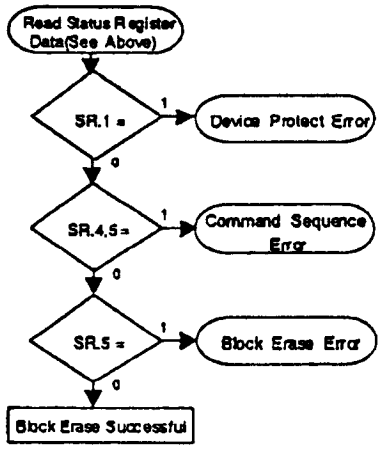
After issue a Multi Word/Byte Write command: XSR.7 indicates that a next Multi Word/Byte Write command is available.

XSR.6-0 is reserved for future use and should be masked out when polling the extended status register.



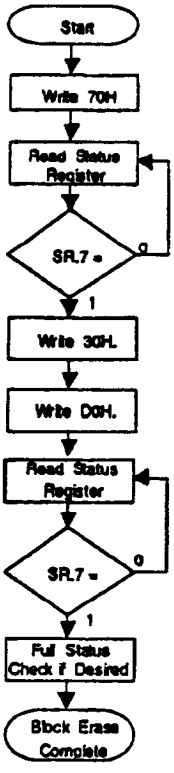
Bus Operation	Command	Comments
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent block erasures. Full status check can be done after each block erase or after sequence of block erasures. Write FFH after the last operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



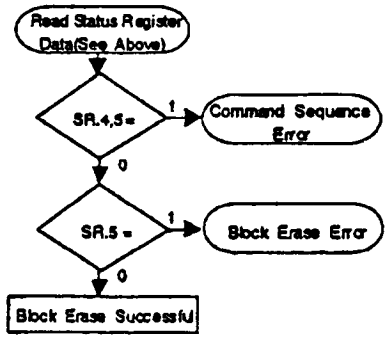
Bus Operation	Command	Comments
Standby		Check SR.1 1 = Device Protect Detect WP# = VIL, Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Write		Check SR.4, 5 Both 1 = Command Sequence Error
Write		Check SR.5 1 = Block Erase Error
SR.5, SR.4 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 5. Automated Block Erase Flowchart



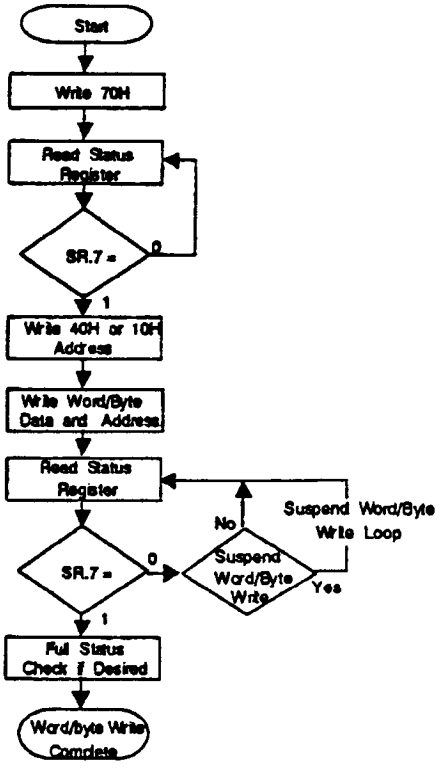
Bus Operation	Command	Comments
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Full Chip Erase Setup	Data = 30H Addr = X
Write	Full Chip Erase Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Full status check can be done after each full chip erase. Write FFH after the last operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



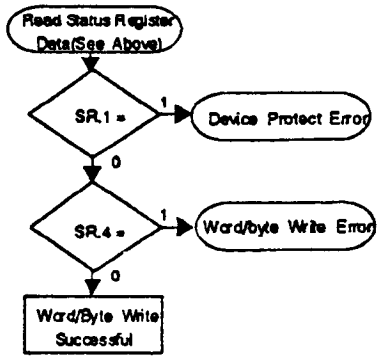
Bus Operation	Command	Comments
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
SR.5, SR.4 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 6. Automated Full Chip Erase Flowchart



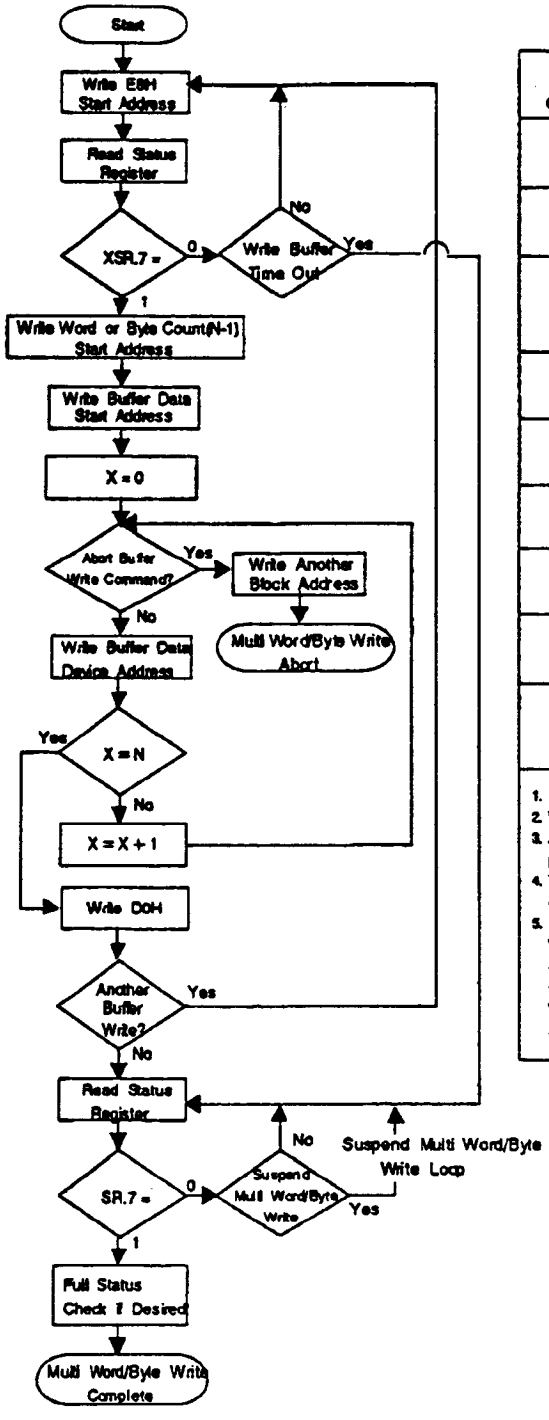
Bus Operation	Command	Comments
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Setup Word/Byte Write	Data = 40H or 10H Addr = Location to be Written
Write	Word/Byte Write	Data = Data to be Written Addr = Location to be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent word/byte writes. SR full status check can be done after each word/byte write, or after a sequence of word/byte writes. Write FFH after the last word/byte write operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.1 1 = Device Protect Detect WP# = VIL, Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Write		Check SR.4 1 = Data Write Error
SR.4 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple locations are written before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 7. Automated Word/byte Write Flowchart

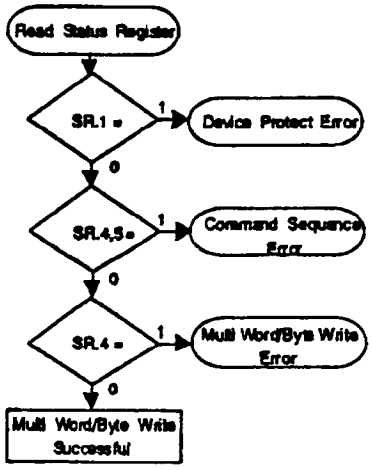


Bus Operation	Command	Comments
Write	Setup Multi Word/Byte Write	Data = E8H Addr = Start Address
Read		Extended Status Register Data
Standby		Check SR.7 1 = Multi Word/Byte Write Ready 0 = MULTI Word/Byte Write Busy
Write (Note2)		Data = Word or Byte Count (N-1) Addr = Start Address
Write (Note2,3)		Data = Buffer Data Addr = Start Address
Write (Note4,5)		Data = Buffer Data Addr = Device Address
Write		Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

1. Byte or word count value on DQ0-7 are loaded into the count register.
2. Write Buffer contents will be programmed at the start address.
3. Align the start address on a Write Buffer boundary for maximum programming performance.
4. The device aborts the Multi Word/Byte Write command if the current address is outside of the original block address.
5. The Status Register indicates an "Improper command sequence" if the Multi Word/Byte command is aborted. Follow this with a Clear Status Register command. SR full status check can be done after each multi word/byte write, or after a sequence of multi word/byte writes.
   Write FFH after the last multi word/byte write operation to place device in read array mode.

Figure 8. Automated Multi Word/Byte Write Flowchart

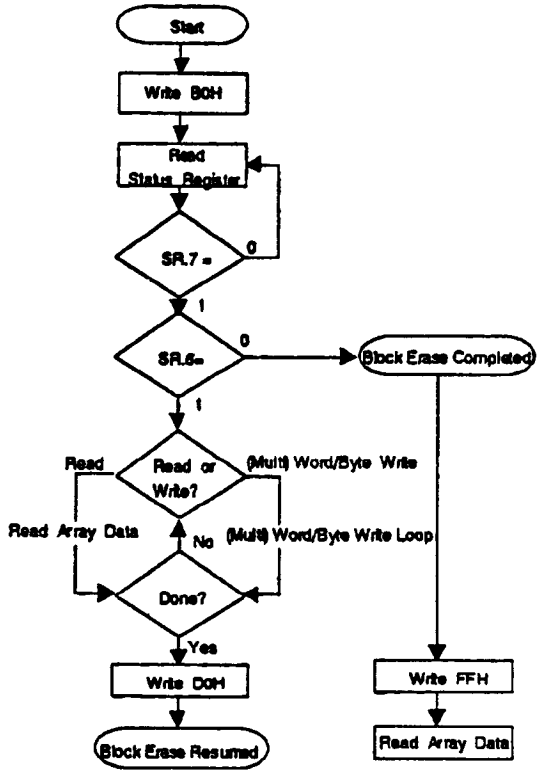
FULL STATUS CHECK PROCEDURE FOR MULTI WORD/BYTE WRITE OPERATION



Bus Operation	Command	Comments
Standby		Check SR.1 1 = Device Protect Detect WP# = VIL, Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Write		Check SR.4, 5 Both 1 = Command Sequence Error
Write		Check SR.4 1 = Data Write Error

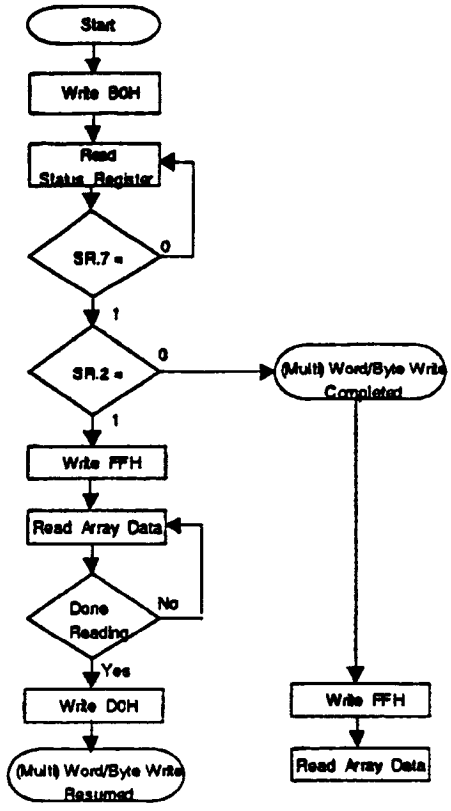
SR.5, SR.4 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 9. Full Status Check Procedure for Automated Multi Word/Byte Write



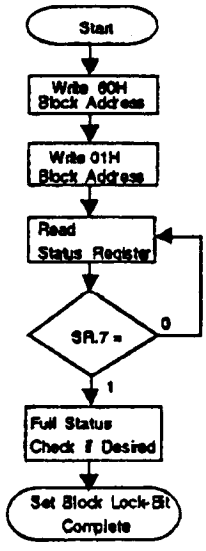
Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X

Figure 10. Block Erase Suspend/Resume Flowchart



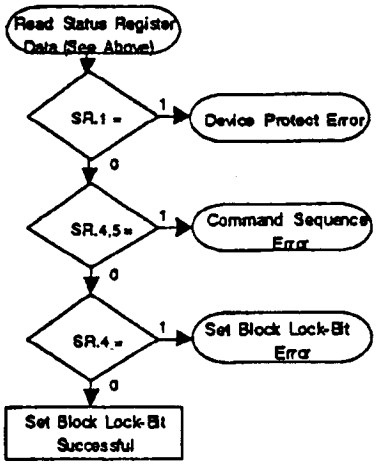
Bus Operation	Command	Comments
Write	(Multi) Word/Byte Write Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = (Multi) Word/Byte Write Suspended 0 = (Multi) Word/Byte Write Completed
Write	Read Array	Data = FFH Addr = X
Read		Read Array Locations other than that being written.
Write	(Multi) Word/Byte Write Resume	Data = D0H Addr = X

Figure 11. (Multi) Word/Byte Write Suspend/Resume Flowchart



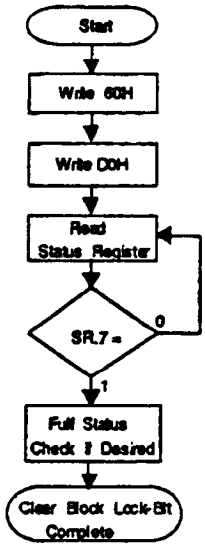
Bus Operation	Command	Comments
Write	Set Block Lock-Bit Setup	Data = 60H Addr = Block Address
Write	Set Block Lock-Bit Confirm	Data = 01H Addr = Block Address
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent block lock-bit set operations. Full status check can be done after each block lock-bit set operation or after a sequence of block lock-bit set operations. Write FFH after the last block lock-bit set operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



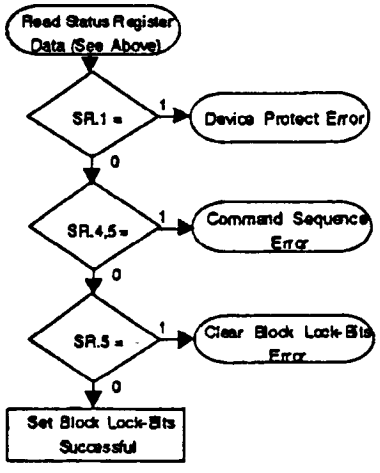
Bus Operation	Command	Comments
Standby		Check SR.1 1 = Device Protect Detect WP# = VIL
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Block Lock-Bit Error
SR.5, SR.4 and SR.1 are only cleared by the Clear Status Register command in cases where multiple block lock-bits are set before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 12. Set Block Lock-Bit Flowchart



Bus Operation	Command	Comments
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write FFH after the Clear Block Lock-Bits operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.1 1 = Device Protect Detect WP# = VIL
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Set Block Lock-Bits Error
SR.5, SR.4 and SR.1 are only cleared by the Clear Status Register command. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 13. Clear Block Lock-Bits Flowchart

5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-Line control provides for:

a. Lowest possible memory power dissipation.
b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 Plower Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a ceramic capacitor connected between its V_{CC} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads.

5.3 V_{CC}, RP# Transitions

Block erase, full chip erase, (multi) word/byte write and block lock-bit configuration are not guaranteed if V_{CC} falls outside of a V_{CC} range, or RP#=V_{IL}. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP# transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

5.4 Power-Up/Down Protection

The device is designed to offer protection against accidental block and full chip erasure, (multi) word/byte writing or block lock-bit configuration during power transitions.
Internal circuitry resets the CUI to read array mode at power-up.
Since both WE# and CE# must be low for a command write, driving either to VIH will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.
In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while RP#=V_{IL} regardless of its control inputs state.

5.5 Power Dissipation

Deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering RP# to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after RP# is first raised to V_{IH}. See AC Characteristics--Read Only and Write Operations and Figures 16, 17, 18, 19 for more information.

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Commercial Operating Temperature
During Read, Erase, Write and
Block Lock-Bit Configuration.....0°C to + 70°C(1)
Temperature under Bias.....-10°C to + 80°C

Storage Temperature.....-65°C to + 125°C

Voltage On Any Pin
(except V_{CC}) .....-0.5V to V_{CC} + 0.5V(2)

V_{CC} Supply Voltage.....-0.2V to 4.6V(2)

Output Short Circuit Current.....100mA(3)

NOTICE: This datasheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local SHARP Sales office that you have the latest datasheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC} +0.5V which, during transitions, may overshoot to V_{CC} +2.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Test Condition
T_A	Operating Temperature	0	+70	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage (3.3V ± 0.3V)	3.0	3.6	V	

6.2.1 CAPACITANCE(1)

T_A = +25°C, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Condition
C_{IN}	Input Capacitance	7	10	pF	V_{IN} = 0.0V
C_{OUT}	Output Capacitance	9	12	pF	V_{OUT} = 0.0V

NOTE:
1. Sampled, not 100% tested.

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS

AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for LOGIC "0". Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10ns.

Figure 14. Transient Input/Output Reference Waveform

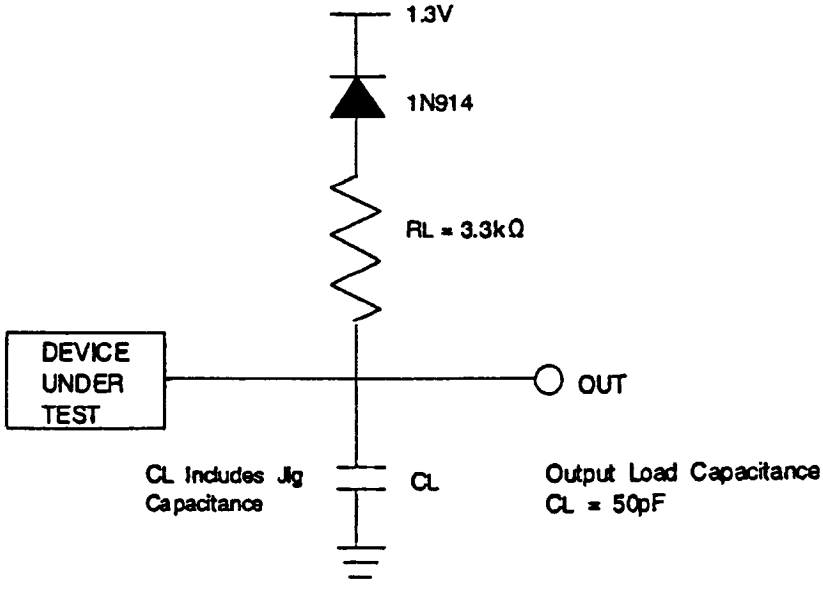


Figure 15. Transient Equivalent Testing Load Circuit

6.2.3 DC CHARACTERISTICS

Sym.	Parameter	Notes	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current	1		±0.5	μA	V_{CC}=VccMax V_{IN}=Vcc or GND
I_{LO}	Output Leakage Current	1		±0.5	μA	V_{CC}=VccMax V_{OUT}=Vcc or GND
I_{CCS}	Vcc Standby Current	1, 3	20	100	μA	CMOS Input V_{CC}=VccMax CE#=RP#=Vcc±0.2V
			1	4	mA	TTL Input V_{CC}=VccMax CE#=RP#=V_{IH}
I_{CCD}	Vcc Deep Power-Down Current	1		15	μA	RP#=GND±0.2V I_{OUT}=0mA
I_{CCR}	Vcc Read Current	1, 3		95	mA	CMOS Input V_{CC}=VccMax, CE#=GND f=5MHz I_{OUT}=0mA
				100	mA	TTL Input V_{CC}=VccMax, CE#=V_{IL} f=5MHz I_{OUT}=0mA
I_{CCW}	Write Current ((Multi)W/B Write or Set Block Lock Bit)	1, 4		90	mA	
I_{CCE}	Erase Current (Block Erase, Full Chip Erase, Clear Block Lock Bits)	1, 4		60	mA	
I_{CCWS} I_{CCES}	Write or Block Erase Suspend Current	1, 2	1	7	mA	CE#=V_{IH}

DC Characteristics (Continued)

Sym.	Parameter	Notes	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	4	-0.5	0.8	V	
V_{IH}	Input High Voltage	4	2.0	Vcc +0.5	V	
V_{OL}	Output Low Voltage	4		0.4	V	Vcc=VccMin I_{OL}=1.6mA
V_{OH}	Output High Voltage	4	2.4		V	Vcc=VccMin I_{OH}=-1mA
V_{LKO}	Vcc Lockout Voltage		2.0		V	
V_{HH}	RP# Unlock Voltage	5	11.4	12.6	V	Override Block Lock-Bit

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal Vcc voltage and TA = +25°C.
2. ICCWS and ICCES are specified with the device de-selected. If read or byte written while in erase suspend mode, the device's current draw is the sum of ICCW or ICCES, respectively.
3. CMOS inputs are either VCC±0.2V or GND±0.2V. TTL inputs are either VIL or VIH.
4. Sampled, not 100% tested.
5. Block erases and (multi)word/byte writes are inhibited when the corresponding block-lock bit is set and RP# = VIH. Block erase, (multi)word/byte write, and lock-bit configuration operations are not guaranteed with Vcc < 2.7V or VIH < RP# < VHH and should not be attempted.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATION (1)

V_{CC}=3.3V±0.3V, T_A=0°C to +70°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		100		ns
t_{AVQV}	Address to Output Delay			100	ns
t_{ELQV}	CE# to Output Delay	2		100	ns
t_{PAVQV}	Pagemode Address to Output Delay			50	ns
t_{PHQV}	RP# High to Output Delay			600	ns
t_{GLQV}	OE# to Output Delay	2		45	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# High to Output in High Z	3		50	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# High to Output in High Z	3		25	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		100	ns
t_{FLQZ}	BYTE# to Output in High Z	3		30	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		5	ns

NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.

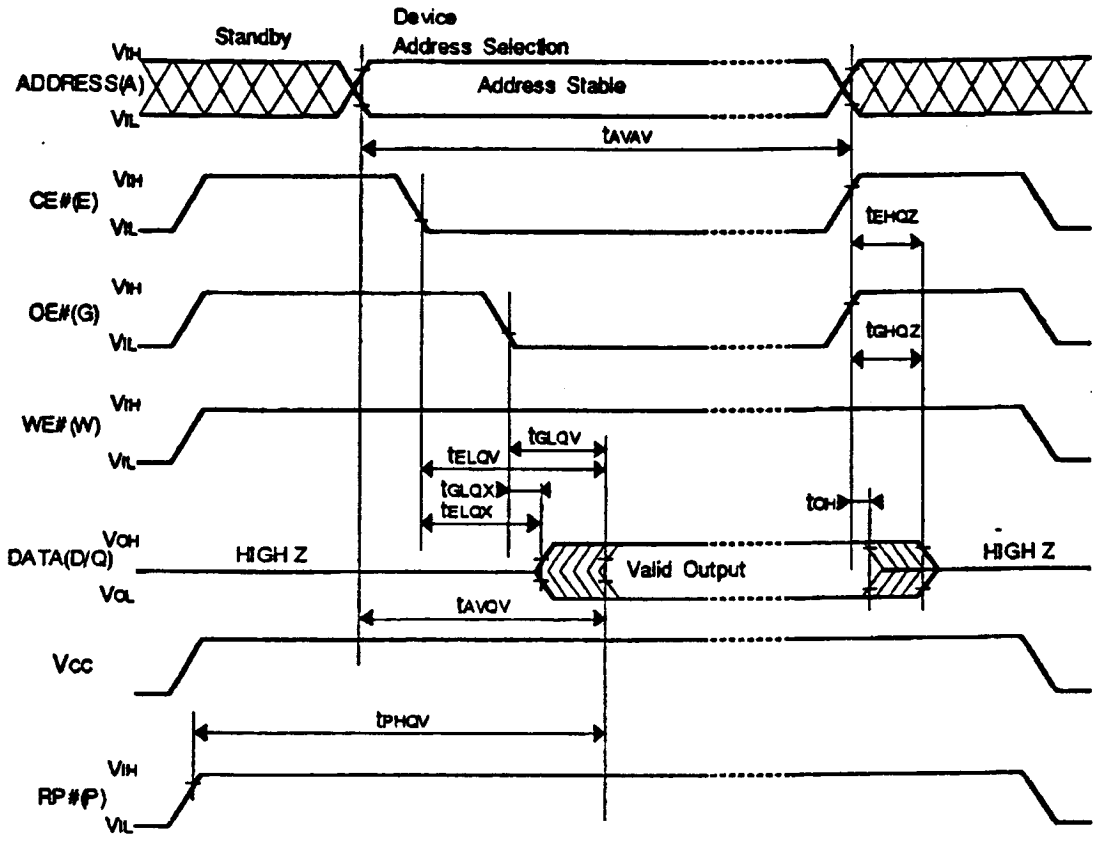


Figure 16. AC Waveform for Normal Read Cycle Operations

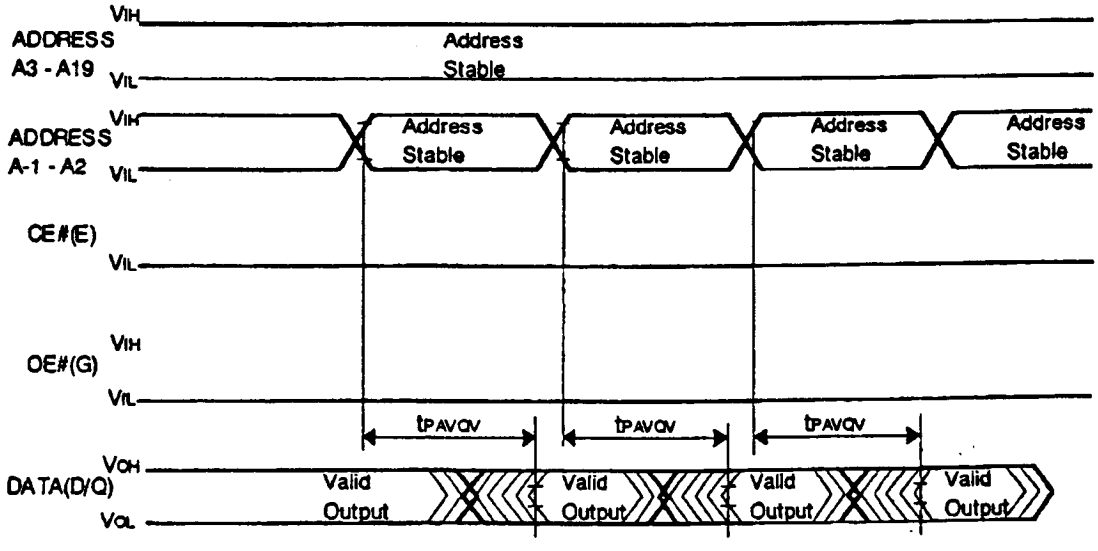


Figure 16.1. AC Waveform for Pagemode Read Cycle Operations

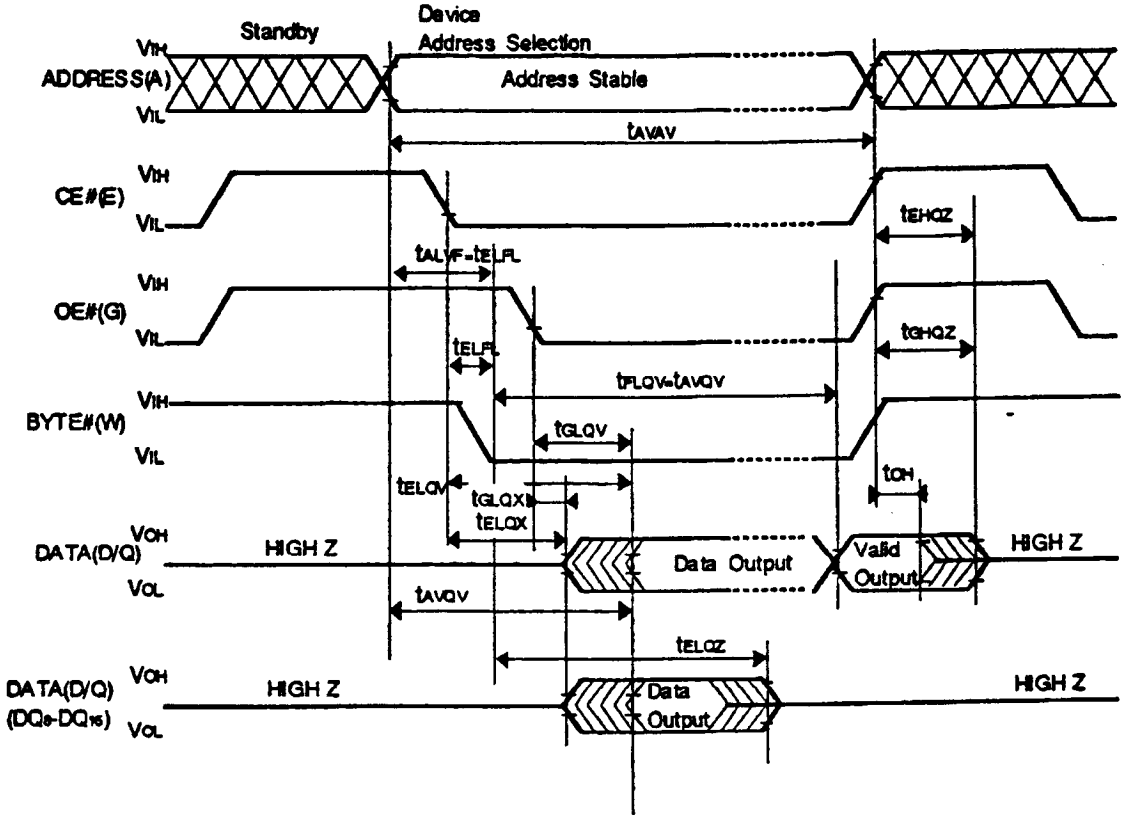


Figure 17. BYTE# Timing Waveforms

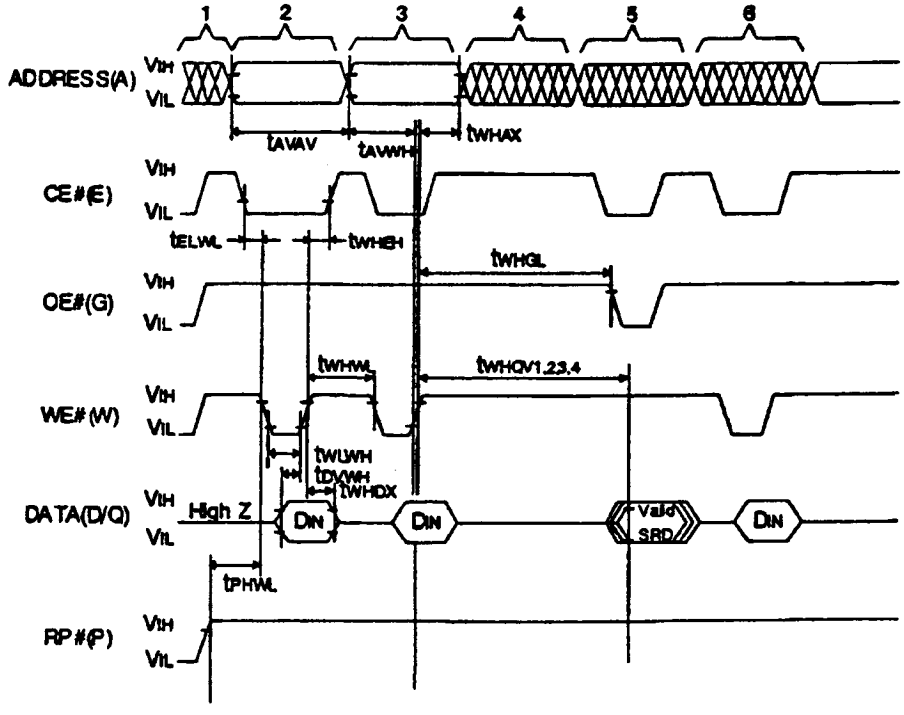
6.2.5 AC CHARACTERISTICS – WRITE OPERATIONS [1]

V_{CC}=3.3V±0.3V, T_A=0°C to +70°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		100		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		μs
t_{ELWL}	CE# Setup to WE# Going Low		10		ns
t_{WLWH}	WE# Pulse Width		50		ns
t_{PHHWH}	RP# V_{HH} Setup to WE# Going High	2	100		ns
t_{AVWH}	Address Setup to WE# Going High	2	100		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		ns
t_{WHDX}	Data Hold from WE# High	3	50		ns
t_{WHAX}	Address Hold from WE# High		5		ns
t_{WHEH}	CE# Hold from WE# High		10		ns
t_{WHWL}	WE# Pulse Width High		30		ns
t_{WHGL}	Write Recovery before Read		0		ns

NOTES :

1. Read timing characteristics during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid AIN and DIN for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.



NOTES:

1. Vcc power-up and standby.
2. Write erase or write setup.
3. Write erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write read array command.

Figure 18. AC Waveform for WE#-Controlled Write Operations

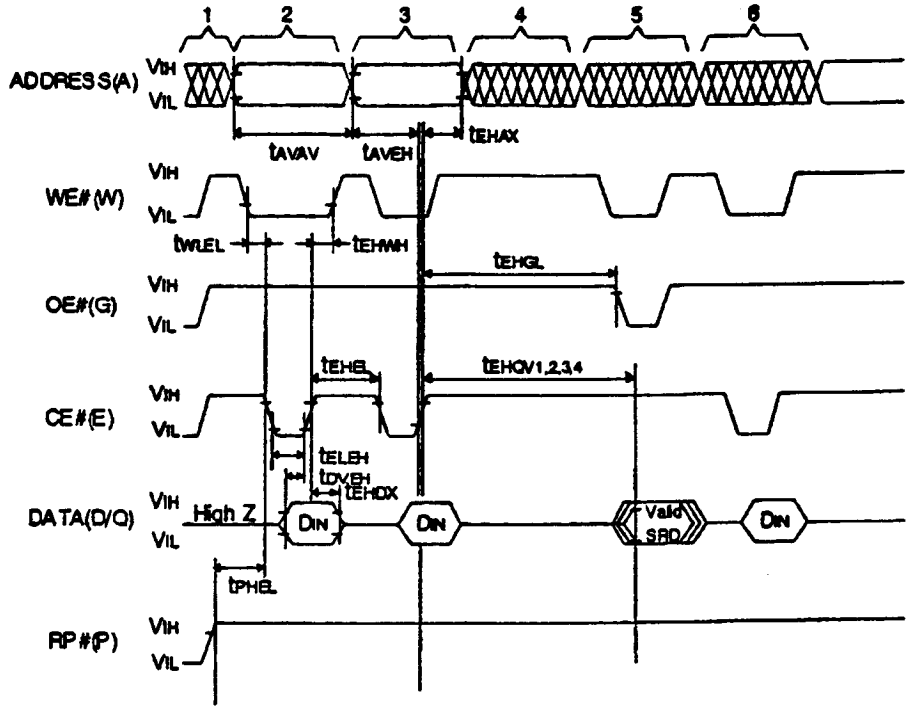
6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES[1]

V_{CC}=3.3V±0.3V, T_A=0°C to +70°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		100		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		μs
t_{WLEL}	WE# Setup to CE# Going Low		0		ns
t_{ELEH}	CE# Pulse Width		70		ns
t_{PHHEH}	RP# V_{HH} Setup to CE# Going High	2	100	-	ns
t_{AVEH}	Address Setup to CE# Going High	2	50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		ns
t_{EHDX}	Data Hold from CE# High	3	5		ns
t_{EHAX}	Address Hold from CE# High		5		ns
t_{EHWH}	WE# Hold from CE# High		0		ns
t_{EHEL}	CE# Pulse Width High		25		ns
t_{EHGL}	Write Recovery before Read		0		ns

NOTES :

1. In system where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold and inactive WE# times should be measured relative to CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid AIN and DIN for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.

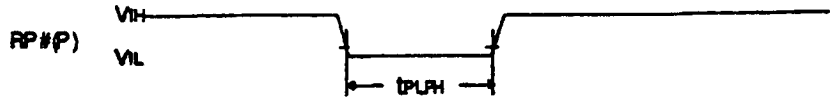


NOTES:

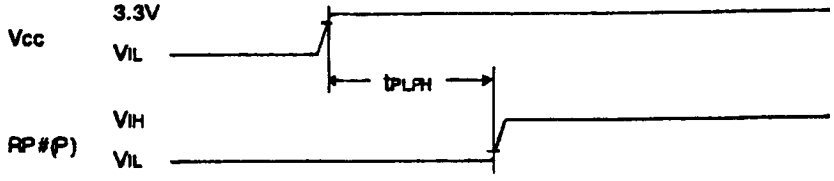
1. Vcc power-up and standby.
2. Write erase or write setup.
3. Write erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write read array command.

Figure 19. Alternate AC Waveform for CE#-Controlled Write Operations

6.2.7 RESET OPERATIONS



(A) Reset During Read Array Mode,Block Erase, Full Chip Erase, (Multi) Word/Byte Write or Block Lock-Bit Configuration



(B) Vcc Power Up Timing

Figure 20. AC Waveform for Reset Operation

Reset AC Specifications

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	RP# Pulse Low Time (If RP# is tied to Vcc, this specification is not applicable.)		100		ns
t_{5VPH}	Vcc at 3.0V to RP# High	1		50	μs

NOTES:

1. When the device power-up, holding RP# low minimum 100ns is required after Vcc has been in predifined range and also has been in stable there.

6.2.8 BLOCK ERASE, FULL CHIP ERASE, (MULTI) WORD/BYTE WRITE AND BLOCK LOCK-BIT CONFIGURATION PERFORMANCE (3)

V_{CC}=3.3V±0.3V, T_A=0°C to +70°C

Sym.	Parameter	Notes	Min.	Typ.(1)	Max.	Unit
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time (using W/B write, in word mode)	2		21.75	TBD	µs
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time (using W/B write, in byte mode)	2		19.51	TBD	µs
	Word/Byte Write Time (using multi word/byte write)	2		5.66	TBD	µs
	Block Write Time (using W/B write, in word mode)	2		0.89	TBD	sec
	Block Write Time (using W/B write, in byte mode)	2		1.6	TBD	sec
	Block Write Time (using multi word/byte write)	2		0.36	TBD	sec
t_{WHQV2} t_{EHQV2}	Block Erase Time	2		0.55	TBD	sec
	Full Chip Erase Time	2		17.6	TBD	sec
t_{WHQV3} t_{EHQV3}	Set Block Lock-Bits Time	2		21.75	TBD	µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	2		0.55	TBD	sec
t_{WHRH1} t_{EHRH1}	Write Suspend Latency Time to Read			7.1	10	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read			15.2	21.1	µs

NOTES :

1. Typical values measured at TA = +25°C and nominal voltage. Assumes corresponding block lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.

16 Mbit, Page Mode, 100/50 ns, 3V, (2M x 8/1M x 16), LH28F160SPN-50