PM7349

S/UNI™-4xD3F

S/UNI-4xD3F

Quad J2, E3 and DS-3 Framer

Data Sheet

Released

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5	June 2001	Included Application Examples, Description, complete Normal Mode Register Description, Operation, Functional Timing, Absolute Maximum Rating, A.C. Timing Characteristics, and Microprocessor Interface Timing sections. Changed references to the FDL to PMDL (path maintenance data link). Modified block diagram to include ROHM[4:1]. Corrected references to pin TDAT to TDATI.
4	July 2000	Name on datasheet was corrected to reflect the device name change. New name is S/UNI-4xD3F.
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2	June 2000	Corrected pin U13 listing in NC pin description section. Corrected pin T3 in pin diagram to REF8KI.
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1 Features

The S/UNI®–4xD3F is a quad DS3, E3 (G.751 and G.832), and J2 framer device. Each channel can be independently configured as a DS3, E3, or J2 Framer. Furthermore, it:

- Optionally generates gapped transmit and receive clocks for interfacing with devices that only need access to payload data bits.
- Provides programmable pseudo-random test pattern generation, detection, and analysis features.
- Provides integral transmit and receive HDLC controllers with 128-byte FIFO depths.
- Provides performance monitoring counters suitable for accumulation periods of up to 1 second.
- Provides an 8-bit microprocessor interface for configuration, control and status monitoring.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Has low power 3.3 V CMOS technology with 5 V tolerant inputs.
- Is available in a high density 256-pin SBGA package (27 mm x 27 mm).

The receiver section:

- Provides frame synchronization for the M23 or C-bit parity DS3 applications, alarm detection, and accumulates line code violations (LCVs), framing errors, parity errors, path parity errors, and far-end block error (FEBE) events. Also detects far end alarm channel (FEAC) codes and provides an integral HDLC receiver to terminate the path maintenance data link (PMDL).
- Provides frame synchronization for the G.751 or G.832 E3 applications, alarm detection, and accumulates LCVs, framing errors, parity errors, and FEBE events. Also, in G.832, detects the Trail Trace and provides an integral HDLC receiver to terminate either the Network Requirement or the General Purpose data link.
- Provides frame synchronization for G.704 and NTT 6.312 Mbit/s J2 applications, alarm detection, and accumulates LCVs, framing errors, and CRC parity errors. Also provides an integral HDLC receiver to terminate the data link.
- Provides a receive HDLC controller with a 128-byte FIFO to accumulate data link information.
- Provides detection of yellow alarm and loss of frame (LOF), and accumulates BIP-8 errors, framing errors and FEBE events.
- Provides programmable pseudo-random test-sequence detection (up to 2^{32}-1 bit length patterns conforming to ITU-T O.151 standards) and analysis features.

The transmitter section:

- Provides frame insertion for the M23 or C-bit parity DS3 applications, alarm insertion, and diagnostic features. Also inserts, FEAC codes and provides an integral HDLC transmitter to insert the PMDL.
- Provides frame insertion for the G.751 or G.832 E3 applications, alarm insertion, and diagnostic features. Also, for G.832, inserts the Trail Trace and provides an integral HDLC transmitter to insert either the Network Requirement or the General Purpose data link.
- Provides frame insertion for G.704 6.312 Mbit/s J2 applications, alarm insertion, and diagnostic features. Also provides an integral HDLC transmitter to insert the PMDL.
- Provides a transmit HDLC controller with a 128-byte FIFO.
- Provides programmable pseudo-random test sequence generation (up to 2^{32}-1 bit length sequences conforming to ITU-T O.151 standards). Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from 10^{-1} to 10^{-7}.

The S/UNI-4xD3F also provides for diagnostic loopbacks, line loopbacks, and payload loopbacks.

2 Applications

- SONET/SDH Mux E3/DS3 Tributary Interfaces
- PDH Mux J2/E3/DS3 Line Interfaces
- DS3/E3/J2 Digital Cross Connect Interfaces
- DS3/E3/J2 PPP Internet Access Interfaces
- DS3/E3/J2 Frame Relay Interfaces

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- NTT Technical Reference, “NTT Technical Reference for High-Speed Digital Leased Circuit Services”, 1991.
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- ETS 300 687, “Business TeleCommunications (BTC); 34 Mbit/s digital leased lines (D34U and D34S); Connection characteristics”, January 1996.
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4 Definitions

The following table defines the abbreviations used in this document.

AIC	Application Identification Channel
AIS	Alarm Indication Signal
ATM	Asynchronous Transfer Mode
BIP	Bit Interleaved Parity
CMOS	Complementary Metal Oxide Semiconductor
COFA	Change of Frame Alignment
CPERR	Path Parity Error
CRC	Cyclic Redundancy Check
DSLAM	DSL Access Multiplexer
DS1	Digital Signal Level 1
DS3	Digital Signal Level 3
EXZS	Excess Zeros
F-bit	Framing Bit
FAS	Frame Alignment Signal
FEAC	Far-End Alarm Control
FEBE	Far-End Block Error
FERF	Far End Receive Failure
FERR	Framing Bit Error
FIFO	First-In First-Out
HCS	Header Check Sequence
HDLC	High-level Data Link Controller
ISDN	Integrated Services Digital network
ITU	International Telecommunications Union
JTAG	Joint Test Action Group
LCD	Loss of Cell Delineation
LCV	Line Code Violation
LOF	Loss of Frame
LOS	Loss of Signal
NRZ	Non Return to Zero
OOF	Out of Frame
PERR	Parity Error
PHY	Physical Layer
PMDL	Path Maintenance Data Link
PMON	Performance Monitor
POS	Packet Over SONET
PPP	Point-to-Point Protocol
RAI	Receive Alarm Indication

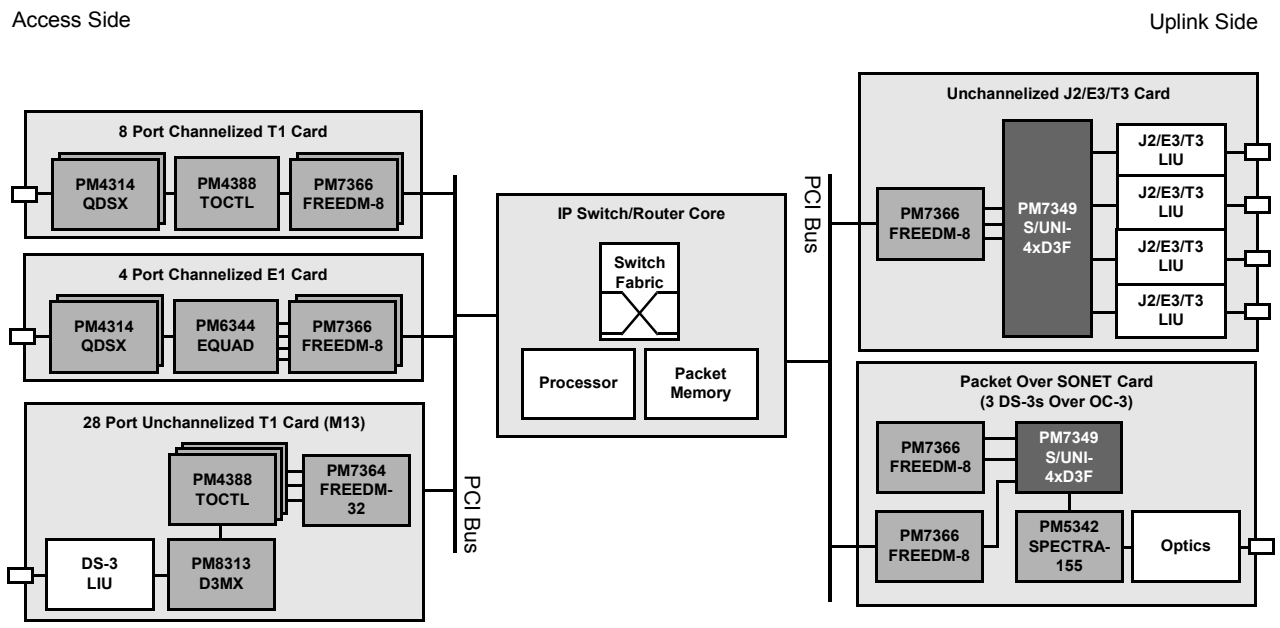
RBOC	Bit Oriented Code Detector
RDLC	Data Link Receiver
RED	Receive Error Detection
SBGA	Super Ball Grid Array
SCI-PHY™	SATURN® Compatible Interface Specification for PHY and ATM layer devices
SMDS	Switched Multi-Megabit Data Service
SONET	Synchronous Optical Network
TAP	Test Access Port
TSB	Telecom System Block
TTB	Trail Trace Buffer

5 Application Example

The PM7349 S/UNI-4xD3F is functionally equivalent to a PM7349 S/UNI-QJET placed in DS3/E3/J2 Transceiver mode.

As a J2/E3/T3 framer, the S/UNI-4xD3F can be used in router, frame relay switch, and multiplexer applications. Refer to Figure 1.

Figure 1 S/UNI-4xD3F Operating as a Quad Framer Device in Frame Relay Equipment

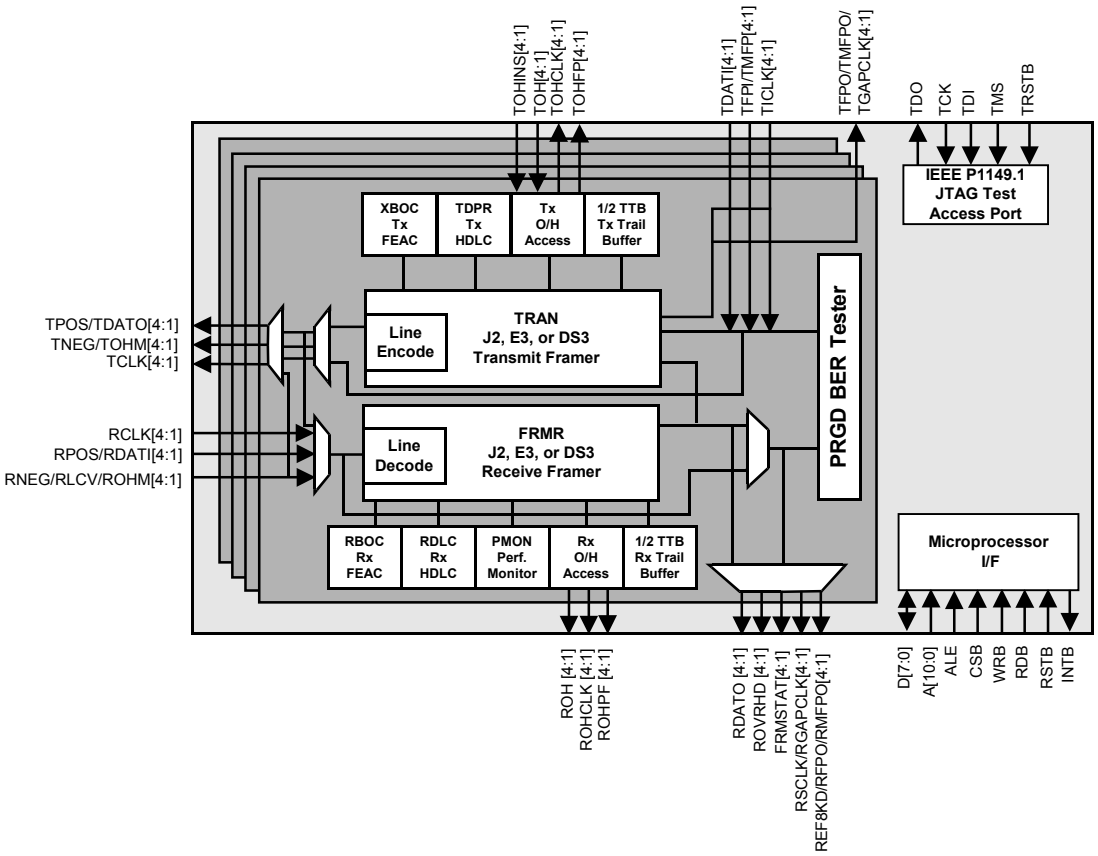


In an unchannelized J2/E3/T3 line card, the S/UNI-4xD3F directly connects to one or more PM7366 FREEDM-8 HDLC controllers. Each FREEDM-8 can process two high-speed links such as T3 and E3, or can process up to eight lower speed links such as J2. The S/UNI-4xD3F gaps all the overhead bits so that only the payload data is passed to and from FREEDM-8. On the line side, the S/UNI-4xD3F is connected to one or more J2/E3/T3 line interface units. On the system side, the S/UNI-4xD3F interfaces with a data link device over a serial bit interface.

In a PPP-Over-SONET (POS) application, the S/UNI-4xD3F connects to a PM5342 SPECTRA-155 to map three T3 data streams onto three corresponding STS-1 services that are collectively carried over an OC-3 link.

6 Block Diagram

Figure 2 Block Diagram



7 Description

The PM7349 S/UNI-4xD3F is comprised of integrated quad DS3, E3, and J2 framers. It is functionally equivalent to a PM7346 S/UNI-QJET placed in DS3/E3/J2 Transceiver mode.

The S/UNI-4xD3F contains:

- Integral DS3 framers that provide DS3 framing and error accumulation in accordance with ANSI T1.107, and T1.107a.
- Integral E3 framers that provide E3 framing in accordance with ITU-T Recommendations G.832 and G.751.
- Integral J2 framers that provide J2 framing in accordance with ITU-T Recommendation G.704 and I.432.

The S/UNI-4xD3F accepts and outputs the appropriate type of bipolar and unipolar signals as described in Table 1:

Table 1 Transmission System Sublayer Processing Acceptance and Output

Transmission System Sublayer Processing	Acceptance and Output
DS3	Accepts and outputs both digital B3ZS-encoded bipolar and unipolar signals compatible with M23 and C-bit parity applications.
E3	Accepts and outputs both HDB3-encoded bipolar and unipolar signals compatible with G.751 and G.832 applications.
J2	Accepts and outputs both B8ZS-encoded bipolar and unipolar signals compliant with G.704 and NTT 6.312 Mbit/s applications.

In the DS3 receive direction, the S/UNI-4xD3F frames to DS3 signals with a maximum average reframe time of 1.5 ms. It detects LCVs, LOS, framing bit errors, parity errors, path parity errors, AIS, FERF, and idle code. The DS3 overhead bits are extracted and presented on serial outputs. When in C-bit parity mode, the PMDL and the FEAC channels are extracted. (HDLC receivers are provided for PMDL support.) Valid bit-oriented codes in the FEAC channels are also detected and are available through the microprocessor port.

Table 2 Summary of Receive and Detection Features

Transmission System Sublayer Processing	Transmit or Receive	Detected Features
DS3	Receive	LCVs, LOS, framing bit errors, parity errors, path parity errors, AIS, FERF, and idle code
E3	Receive	LCVs, LOS, framing bit errors, AIS, and RAI
J2	Receive	LCVs, LOS, LOF, framing bit errors, physical layer AIS, payload AIS, CRC-5 errors, Remote End Alarm, and RAI

In the E3 receive direction, the S/UNI-4xD3F frames to G.751 and G.832 E3 signals with a maximum average reframe times of 135 µs for G.751 frames and 250 µs for G.832 frames. LCVs, LOS, framing bit errors, alarm indication signals (AIS), and receive alarm indications (RAI) are detected. Also detected when processing G.832 formatted data are parity errors, FERF, and FEBEs. As well, a trace message can be extracted and made available through the microprocessor port. HDLC receivers are provided for either the G.832 Network Requirement or the G.832 General Purpose Data Link support.

In the J2 receive direction, the S/UNI-4xD3F frames to G.704 6.312 MHz signals with a maximum average reframe time of 5.07 ms. An alternate framing algorithm that uses the CRC-5 bits to rule out 99.9% of all static mimic framing patterns is available with a maximum average reframe time of 10.22 ms when operating with a 10^{-4} bit error rate. This algorithm can be selected by the CRC_REFR bit in the J2-FRMR Configuration register. LCVs, LOS, loss of frame (LOF), framing bit errors, physical layer AIS, payload AIS, CRC-5 errors, Remote End Alarm, and RAI are detected. HDLC receivers are provided for Data Link support.

The S/UNI-4xD3F also provides error event accumulation. Framing bit errors, LCVs, parity errors, path parity errors, and FEBEs are accumulated, when appropriate, in saturating counters for DS3, E3, and J2 frames. LOF detection for DS3, E3, and J2 is provided as recommended by ITU-T G.783 with integration times of 1 ms, 2 ms, and 3 ms.

In the DS3 transmit direction, the S/UNI-4xD3F inserts DS3 framing, X and P bits. When enabled for C-bit parity operation, bit-oriented code transmitters and HDLC transmitters are provided for the insertion of FEAC channels and the PMDL in the appropriate overhead bits. AIS can be inserted by using internal register bits and other status signals such as the idle signal can be inserted when they are enabled by internal register bits. When M23 operation is selected, the C-bit Parity ID bit (the first C-bit of the first M sub-frame) is forced to toggle so that downstream equipment will not confuse an M23-formatted stream with “stuck-at 1” C-bits for C-bit parity application.

In the E3 transmit direction, the S/UNI-4xD3F inserts E3 framing in either G.832 or G.751 format. When the device is enabled for G.832 operation, it provides an HDLC transmitter that the Network Requirement or General Purpose Data Link is inserted into the appropriate overhead bits. The AIS and other status signals can be inserted by internal register bits.

In the J2 transmit direction, the S/UNI-4xD3F inserts J2 6.312 Mbit/s G.704 framing. HDLC transmitters are provided the Data Links are inserted. CRC-5 check bits are calculated and inserted into the J2 multiframe. External pins are provided so that any of the overhead bits within the J2 frame can be overwritten.

The S/UNI-4xD3F also supports diagnostic options that allow it to insert, when appropriate, the transmit framing format, parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, LCVs, all-zeros, AIS, RAIs, and Remote End Alarms.

The S/UNI-4xD3F is configured, controlled, and monitored by a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be identified, acknowledged, or masked with this interface.

The S/UNI-4xD3F requires a software. initialization sequence in order to guarantee proper device operation and long term reliability. Please refer to Section 13.1 of this document for the details on how to program this sequence.

8 Pin Diagram

The S/UNI-4xD3F is packaged in a 256-pin SBGA package having a body size of 27 mm by 27 mm and a pin pitch of 1.27 mm.

Quadrant A11/A20 to K11/K20

	20	19	18	17	16	15	14	13	12	11	
A	VSS	VSS	VSS	VSS	VSS	D[1]	D[5]	VSS	A[3]	A[7]	A
B	VSS	VDD	VDD	VSS	VSS	D[0]	D[4]	A[0]	A[2]	A[6]	B
C	VSS	VDD	VDD	VSS	VSS	VSS	D[2]	D[6]	A[1]	A[5]	C
D	VSS	VSS	VSS	NC	VSS	VSS	VDD	D[3]	D[7]	A[4]	D
E	VSS	VSS	VSS	VSS							E
F	VSS	VSS	VSS	VSS							F
G	VSS	VSS	VSS	VDD	**Bottom View**						G
H	BIAS	NC	VSS	VSS	**(Top Left)**						H
J	VSS	NC	NC	NC							J
K	VSS	NC	VSS	VDD							K
	20	19	18	17	16	15	14	13	12	11	

Quadrant A1/A10 to K1/K10

	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	ALE	INTB	TRSTB	TNEG/ TOHM[4]	RCLK[4]	VSS	VSS	VSS	A
B	A[9]	A[10]	WRB	TDO	TCK	TCLK[4]	TPOS[3]/ TDATO[3]	VDD	VDD	VSS	B
C	A[8]	CSB	RSTB	TMS	TPOS[4]/ TDATO[4]	RNEG[4]/ RDATI[4]	TCLK[3]	VDD	VDD	VSS	C
D	VDD	RDB	TDI	VDD	RPOS[4]	TNEG/ TOHM[3]	BIAS	TPOS[2]/ TDATO [2]	TCLK[2]	RPOS[3]	D
E							TNEG/ TOHM[2]	RNEG[3]/ RDATI[3]	RPOS[2]	RNEG[2]/ RDATI[2]	E
F							RCLK[3]	RCLK[2]	TPOS[1]/ TDATO[1]	TNEG/ TOHM[1]	F
G	**Bottom View**						VDD	TCLK[1]	RNEG[1]/ RDATI[1]	RCLK[1]	G
H	**(Top Right)**						RPOS[1]	TOH[4]	TOHCLK[4]	VSS	H
J							TOHINS[4]	TOHFP[4]	ROH[4]	ROHFP[4]	J
K							ROHCLK[4]	TOH[3]	TOHINS[3]	TOHCLK[3]	K
	10	9	8	7	6	5	4	3	2	1	

Quadrant L11/L20 to Y11/Y20

	20	19	18	17	16	15	14	13	12	11	
L	VSS	VSS	VSS	NC	**Bottom View (Bottom Left)**						L
M	NC	NC	NC	NC							M
N	VSS	NC	VSS	VSS							N
P	VSS	VSS	VSS	VDD							P
R	VSS	VSS	NC	NC							R
T	NC	NC	NC	NC							T
U	NC	NC	NC	BIAS	NC	NC	VDD	NC	REF8KO/ RFPO/ RMFPO[4]	VDD	U
V	VSS	VDD	VDD	NC	NC	TICLK[4]	VSS	ROVRHD[4]	TFPI/ TMFPI[3]	NC	V
W	VSS	VDD	VDD	NC	NC	TFPI/ TMFPI[4]	TFPO/ TMFPO/ TGAPCLK[4]	RSCLK/ RGAPCLK[4]	TDATI[3]	VSS	W
Y	VSS	VSS	VSS	NC	NC	TDATI[4]	RDATO[4]	TICLK[3]	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	

Quadrant L1/L10 to Y1/Y10

	10	9	8	7	6	5	4	3	2	1	
L	**Bottom View (Bottom Right)**						VDD	TOHFP[3]	ROH[3]	VSS	L
M							TOHINS[2]	ROHCLK[3]	ROHFP[3]	VSS	M
N							ROHCLK[2]	TOHFP[2]	TOHCLK[2]	TOH[2]	N
P							VDD	TOH[1]	ROHFP[2]	ROH[2]	P
R							ROHCLK[1]	TOHFP[1]	TOHCLK[1]	TOHINS[1]	R
T							FRMSTAT[2]	REF8KI	ROHFP[1]	ROH[1]	T
U	RSCLK/ RGAPCLK[3]	VSS	ROVRHD[2]	VDD	NC	RSCLK/ RGAPCLK[1]	BIAS	FRMSTAT[1]	FRMSTAT[3]	FRMSTAT[4]	U
V	ROVRHD[3]	TFPI/ TMFPI[2]	NC	RSCLK/ RGAPCLK[2]	TFPI/ TMFPI[1]	TFPO/ TMFPO/ TGAPCLK[1]	REF8KO/ RFPO/ RMFPO[1]	VDD	VDD	VSS	V
W	RDATO[3]	TICLK[2]	TDATI[2]	RDATO[2]	TICLK[1]	VSS	ROVRHD[1]	VDD	VDD	VSS	W
Y	TFPO/ TMFPO/ TGAPCLK[3]	REF8KO/ RFPO/ RMFPO[3]	VSS	TFPO/ TMFPO/ TGAPCLK[2]	REF8KO/ RFPO/ RMFPO[2]	TDATI[1]	RDATO[1]	VSS	VSS	VSS	Y
	10	9	8	7	6	5	4	3	2	1	

9 Pin Descriptions

Pin Name	Type	Pin No.	Function
TPOS[4] TPOS[3] TPOS[2] TPOS[1] TDATO[4] TDATO[3] TDATO[2] TDATO[1]	Output	C6 B4 D3 F2	The Transmit Digital Positive Pulse (TPOS[4:1]) contains the positive pulses transmitted on the B3ZS-encoded DS3, HDB3-encoded E3, or B8ZS-encoded J2 transmission system when the dual-rail output format is selected. Transmit Data (TDATO[4:1]) contains the transmit data stream when the single-rail (unipolar) output format is enabled or when a non-DS3/E3/J2-based transmission system is selected. The TPOS/TDATO[4:1] pin function selection is controlled by the TFRM[1:0] and the TUNI bits in the S/UNI-4xD3F Transmit Configuration Registers. Output signal polarity control is provided by the TPOSINV bit in the S/UNI-4xD3F Transmit Configuration Registers. Both TPOS[4:1] and TDATO[4:1] are updated on the falling edge of TCLK[4:1] by default, and may be configured for update on the rising edge of TCLK[4:1] through the TCLKINV bit in the S/UNI-4xD3F Transmit Configuration Registers. Both TPOS[4:1] and TDATO[4:1] can be updated on the rising edge of TICLK[4:1], enabled by the TICLK bit in the S/UNI-4xD3F Transmit Configuration Registers.
TNEG[4] TNEG[3] TNEG[2] TNEG[1] TOHM[4] TOHM[3] TOHM[2] TOHM[1]	Output	A5 D5 E4 F1	The Transmit Digital Negative Pulse (TNEG[4:1]) contains the negative pulses transmitted on the B3ZS-encoded DS3, HDB3-encoded E3, or B8ZS-encoded J2 transmission system when the dual-rail NRZ output format is selected. The Transmit Overhead Mask (TOHM[4:1]) indicates the position of overhead bits (non-payload bits) in the transmission system stream aligned with TDATO[4:1]. TOHM[4:1] indicates the location of the M-frame boundary for DS3, the position of the frame boundary for E3, and the position of the multiframe boundary for J2 when the single-rail (unipolar) NRZ input format is enabled. The TNEG/TOHM[4:1] pin function selection is controlled by the TFRM[1:0] and the TUNI bits in the S/UNI-4xD3F Transmit Configuration registers. Output signal polarity is controlled by the TNEGINV bit in the S/UNI-4xD3F Transmit Configuration registers. Both TNEG[4:1] and TOHM[4:1] are updated on the falling edge of TCLK[4:1] by default, and can be enabled for update on the rising edge of TCLK[4:1]. This sampling is controlled by the TCLKINV bit in the S/UNI-4xD3F Transmit Configuration registers. Note: Both TNEG[4:1] and TOHM[4:1] can be updated on the rising edge of TICLK[4:1] by enabling the TICLK bit in the S/UNI-4xD3F Transmit Configuration registers.

Pin Name	Type	Pin No.	Function
TCLK[4] TCLK[3] TCLK[2] TCLK[1]	Output	B5 C4 D2 G3	The Transmit Output Clock (TCLK[4:1]) provides the transmit direction timing. TCLK[4:1] is a buffered version of TICLK[4:1. TCLK[4:1} can be enabled to update the TPOS/TDATO[4:1] and TNEG/TOHM[4:1] outputs on its rising or falling edge.
RPOS[4] RPOS[3] RPOS[2] RPOS[1] RDATI[4] RDATI[3] RDATI[2] RDATI[1]	Input	D6 D1 E2 H4	The Receive Digital Positive Pulse (RPOS[4:1]) contains the positive pulses received on the B3ZS-encoded DS3, the HDB3-encoded E3, or the B8ZS-encoded J2 transmission system when the dual-rail NRZ input format is selected. Receive Data (RDATI[4:1]) contains the data stream when the single-rail (unipolar) NRZ input format is enabled or when a non-DS3/E3/J2 based transmission system is being processed (for example RDATI may contain a DS1 or E1 stream). The RPOS/RDATI[4:1] pin function selection is controlled by the RFRM[1:0] bits in the S/UNI-4xD3F Configuration Registers and by the UNI bits in the DS3 FRMR, the E3 FRMR, or the J2 FRMR Configuration Registers. Both RPOS[4:1] and RDATI[4:1] are sampled on the rising edge of RCLK[4:1] by default, and may be enabled for sampling on the falling edge of RCLK[4:1]. This sampling is controlled by the RCLKINV bit in the S/UNI-4xD3F Receive Configuration Registers. Note: Signal polarity control is provided by the RPOSINV bit in the same registers.
RNEG[4] RNEG[3] RNEG[2] RNEG[1] RLCV[4] RLCV[3] RLCV[2] RLCV[1] ROHM[4] ROHM[3] ROHM[2] ROHM[1]	Input	C5 E3 E1 G2	The Receive Digital Negative Pulse (RNEG[4:1]) contains the negative pulses received on the B3ZS encoded DS3, the HDB3-encoded E3, or the B8ZS-encoded J2 transmission system when the dual-rail NRZ input format is selected. The Receive LCV (RLCV[4:1]) contains LCV indications of when the single-rail (unipolar) NRZ input format is enabled for DS3, E3, or J2 applications. Each LCV is represented by an RCLK[4:1] period-wide pulse. When an alternate frame-based signal is received, the Receive Overhead Mask (ROHM[4:1]) indicates the position of each overhead bit in the transmission frame. The RNEG/RLCV/ROHM[4:1] pin function selection is controlled by the RFRM[1:0] bits in the S/UNI-4xD3F Receive Configuration registers, the UNI bits in the DS3 FRMR, E3 FRMR, or J2 FRMR Configuration registers, and the PLCPEN and EXT bits in the SPLR Configuration register. RNEG[4:1], RLCV[4:1], and ROHM[4:1] are sampled on the rising edge of RCLK[4:1] by default, and may be enabled for sampling on the falling edge of RCLK[4:1]. This sampling is controlled by the RCLKINV bit in the S/UNI-4xD3F Receive Configuration registers. Note: Signal polarity control is provided by the RNEGINV bit in the S/UNI-4xD3F Receive Configuration registers.

Pin Name	Type	Pin No.	Function
RCLK[4] RCLK[3] RCLK[2] RCLK[1]	Input	A4 F4 F3 G1	The Receive Clock (RCLK[4:1]) provides the receive direction timing. RCLK[4:1] is the externally recovered transmission system baud rate clock that samples the RPOS/RDATI[4:1] and RNEG/RLCV/ROHM[4:1] inputs on its rising or falling edge.
TOHINS[4] TOHINS[3] TOHINS[2] TOHINS[1]	Input	J4 K2 M4 R1	The Transmit DS3/E3/J2 Overhead Insertion (TOHINS[4:1]) controls the insertion of the DS3, E3, or J2 overhead bits from the TOH[4:1] input. When TOHINS[4:1] is high, the associated overhead bit in the TOH[4:1] stream is inserted in the transmitted DS3, E3, or J2 frame. When TOHINS[4:1] is low, the DS3, E3, or J2 overhead bit is generated and inserted internally. TOHINS[4:1] is sampled on the rising edge of TOHCLK[4:1]. Note: If TOHINS[4:1] is a logic one, the TOH[4:1] input has precedence over the internal datalink transmitter, or any internal register bit setting.
TOH[4] TOH[3] TOH[2] TOH[1]	Input	H3 K3 N1 P3	When configured for DS3 operation, the Transmit DS3/E3/J2 Overhead Data (TOH[4:1]) contains the overhead bits (C, F, X, P, and M) that may be inserted in the transmit DS3 stream. When configured for G.832 E3 operation, TOH[4:1] contains the overhead bytes (FA1, FA2, EM mask, TR, MA, NR, and GC) that may be inserted in the transmit G.832 E3 stream. When configured for G.751 E3 operation, TOH[4:1] contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) that may be inserted in the transmit G.751 E3 stream. When configured for J2 operation, TOH[4:1] contains the overhead bits (TS97, TS98, Framing, X_{1-3}, A, M, E_{1-5}) that may be inserted in the transmit J2 stream. If TOHINS[4:1] is a logic one, the TOH[4:1] input has precedence over the internal datalink transmitter, or any other internal register bit setting. TOH[4:1] is sampled on the rising edge of TOHCLK[4:1].
TOHFP[4] TOHFP[3] TOHFP[2] TOHFP[1]	Output	J3 L3 N3 R3	The Transmit DS3/E3/J2 Overhead Frame Position (TOHFP[4:1]) is used to align the individual overhead bits in the transmit overhead data stream, TOH[4:1], to the DS3 M-frame or the E3 frame. TOHFP[4:1] is high for DS3, during the X1 overhead bit position in the TOH[4:1] stream, for G832 E3, during the first bit of the FA1 byte, for G.751 E3, during the RAI overhead bit position in the TOH[4:1] stream, and for J2, during the first bit of timeslot 97 in the first frame of a 4-frame multiframe. TOHFP[4:1] is updated on the falling edge of TOHCLK[4:1].

Pin Name	Type	Pin No.	Function
TOHCLK[4] TOHCLK[3] TOHCLK[2] TOHCLK[1]	Output	H2 K1 N2 R2	The Transmit DS3/E3/J2 Overhead Clock (TOHCLK[4:1]) is active when a DS3, E3, or J2 stream is being processed. TOHCLK[4:1] is nominally a 526 kHz clock for DS3, a 1.072 MHz clock for G.832 E3, a 1.074 MHz clock for G.751 E3, and a gapped 6.312 MHz clock with an average frequency of 168 kHz for J2. TOHFP[4:1] is updated on the falling edge of TOHCLK[4:1]. TOH[4:1], and TOHINS[4:1] are sampled on the rising edge of TOHCLK[4:1].
REF8KI	Input	T3	REF8KI is required for the power up sequence described in Section 13.1.
TDATI[4] TDATI[3] TDATI[2] TDATI[1]		Y15 W12 W8 Y5	The Framer Transmit Data (TDATI[4:1]) contains the serial data to be transmitted. TDATI[4:1] is sampled on the rising edge of TICLK[4:1] if the TXGAPEN register bit in the S/UNI-4xD3F Configuration 2 register is logic zero. If TXGAPEN is logic one, then TDATI[4:1] is sampled on the falling edge of TGAPCLK[4:1].
TFPO[4] TFPO[3] TFPO[2] TFPO[1] TMFPO[4] TMFPO[3] TMFPO[2] TMFPO[1]	Output	W14 Y10 Y7 V5	The Transmit Path Overhead Frame Position (TFPO[4:1]) is logic one, while bit 1 (the most significant bit) of the path user channel octet (F1) is present in the TDAT[4:1] stream. TFPO[4:1] is updated on the falling edge of TPOHCLK[4:1]. The Framer Transmit Frame Pulse/Multi-frame Pulse Reference (TFPO/TMFPO[4:1]) is valid by setting the TXGAPEN-bit in the S/UNI-4xD3F Configuration registers to logic zero. When configured for DS3, the TFPO[4:1] pulses high for 1 out of every 85 clock cycles, giving a free-running mark for all overhead bits in the frame. When configured for G.751 E3, it pulses high for 1 out of every 1536 clock cycles, giving a free-running reference G.751 indication, and for G.832 E3, it pulses high for 1 out of every 4296 clock cycles, giving a free-running reference G.832 frame indication. For J2, it pulses high for 1 out of every 789 clock cycles, giving a free-running reference frame indication. The TMFPO[4:1] pulses high for 1 out of every 4760 clock cycles when configured for DS3, giving a free-running reference M-frame indication. TMFPO[4:1] pulses high for 1 out of every 3156 clock cycles when configured for J2, giving a free-running reference multiframe indication. TMFPO[4:1] behaves the same as TFPO[4:1] for E3 applications. TFPO/TMFPO[4:1] is updated on the rising edge of TICLK[4:1] or RCLK[4:1] if loop-timed.

Pin Name	Type	Pin No.	Function
TGAPCLK[4] TGAPCLK[3] TGAPCLK[2] TGAPCLK[1]	Output		The Framer Gapped Transmit Clock (TGAPCLK[4:1]) is valid by setting the TXGAPEN-bit in the S/UNI-4xD3F Configuration 2 registers to logic one. TGAPCLK[4:1] is derived from the transmit reference clock TICLK[4:1] or from the receive clock if loop-timed. The overhead bit (gapped) positions are generated internal to the device. TGAPCLK[4:1] is held high during the overhead bit positions. This clock is useful for interfacing to devices which source payload data only. TGAPCLK[4:1] is used to sample TDATI[4:1].
TFPI[4] TFPI[3] TFPI[2] TFPI[1] TMFPI[4] TMFPI[3] TMFPI[2] TMFPI[1]	Input	W15 V12 V9 V6	The Framer Transmit Frame Pulse/Multiframe Pulse (TFPI/TMFPI[4:1]) indicates the position of all overhead bits in each DS3 M-subframe, the first bit in each G.751 E3 or G.832 E3 frame, or the first framing bit in each J2 frame. TFPI[4:1] is not required to pulse at every frame boundary in E3 or J2 modes. TMFPI[4:1] indicates the position of the first bit in each DS3 M-frame, the first bit in each E3 frame, or the first framing bit in each J2 multiframe. TMFPI[4:1] is not required to pulse at every multiframe boundary. TFPI/TMFPI[4:1] is sampled on the rising edge of TICLK[4:1].
TICLK[4] TICLK[3] TICLK[2] TICLK[1]	Input	V15 Y13 W9 W6	The Transmit Input Clock (TICLK[4:1]) provides the transmit direction timing. TICLK[4:1] is the externally generated transmission system baud rate clock. It is internally buffered to produce the transmit clock output, TCLK[4:1]. It can be enabled to update the TPOS/TDATO[4:1] and TNEG/TOHM[4:1] outputs on the TICLK[4:1] rising edge. The TICLK[4:1] maximum frequency is 52 MHz.
ROHFP[4] ROHFP[3] ROHFP[2] ROHFP[1]	Output	J1 M2 P2 T2	The Receive DS3/E3/J2 Overhead Frame Position (ROHFP[4:1]) locates the individual overhead bits in the received overhead data stream, ROH[4:1]. ROHFP[4:1] is high during the X1 overhead bit position in the ROH[4:1] stream when processing a DS3 stream. ROHFP[4:1] is high during the first bit of the FA1 byte when processing a G.832 E3 stream. ROHFP[4:1] is high during the RAI overhead bit position when processing a G.751 E3 stream. ROHFP[4:1] is high during the first bit in “Timeslot 97” of the first frame of the 4-frame multiframe when processing a J2 stream. ROHFP[4:1] is updated on the falling edge of ROHCLK[4:1].

Pin Name	Type	Pin No.	Function
ROH[4] ROH[3] ROH[2] ROH[1]	Output	J2 L2 P1 T1	The Receive DS3/E3/J2 Overhead Data (ROH[4:1]) contains the overhead bits (C, F, X, P, and M) extracted from the received DS3 stream. ROH[4:1] contains the overhead bytes (FA1, FA2, EM, TR, MA, NR, and GC) extracted from the received G.832 E3 stream; ROH[4:1] contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) extracted from the received G.751 E3 stream; ROH[4:1] contains the overhead bits (Framing, X_{1-3}, A, M, E_{1-5}) extracted from the received J2 stream. ROH[4:1] is updated on the falling edge of ROHCLK[4:1].
ROHCLK[4] ROHCLK[3] ROHCLK[2] ROHCLK[1]	Output	K4 M3 N4 R4	The Receive DS3/E3/J2 Overhead Clock (ROHCLK[4:1]) is active when a DS3, E3, or J2 stream is being processed. ROHCLK[4:1] is nominally a 526 kHz clock when processing DS3, a 1.072 MHz clock when processing G.832 E3, a 1.074 MHz clock when processing G.751 E3, and a gapped 6.312 MHz clock with an average frequency of 168 kHz for J2. ROH[4:1], and ROHFP[4:1] are updated on the falling edge of ROHCLK[4:1].
REF8KO[4] REF8KO[3] REF8KO[2] REF8KO[1]	Output	U12 Y9 Y6 V4	The Reference 8kHz Output (REF8KO[4:1]) is an 8kHz reference derived from the receive clocks on RCLK[4:1]. A free-running divide-down counter is used to generate REF8KO[4:1] so it will not glitch on reframe actions. REF8KO[4:1] will pulse high for approximately 1 RCLK[4:1] cycle every 125 µs. REF8KO[4:1] should be treated as a glitch-free asynchronous signal.
RFPO[4] RFPO[3] RFPO[2] RFPO[1]			The Framer Receive Frame Pulse/Multi-frame Pulse (RFPO/RMFPO[4:1]) is valid when the 8KREFO bit is set to logic zero in the S/UNI-4xD3F Configuration register. RFPO[4:1] is aligned to RDATO[4:1] and indicates the position of the first bit in each DS3 M-subframe, the first bit in each G.751 E3 or G.832 E3 frame, or the first framing bit in each J2 frame.
RMFPO[4] RMFPO[3] RMFPO[2] RMFPO[1]			RMFPO[4:1] is aligned to RDATO[4:1] and indicates the position of the first bit in each DS3 M-frame, the first bit in each G.751 or G.832 E3 multiframe, or the first framing bit in each J2 multiframe. RFPO/RMFPO[4:1] is updated on either the falling or rising edge of RSCLK[4:1] depending on the setting of the RSCLKR bit in the S/UNI-4xD3F Receive Configuration register.
ROVRHD[4] ROVRHD[3] ROVRHD[2] ROVRHD[1]	Output	V13 V10 U8 W4	The Framer Receive Overhead Indication (ROVRHD[4:1]) will be high whenever the data on RDATO[4:1] corresponds to an overhead bit position. ROVRHD[4:1] is updated on the either the falling or rising edge of RSCLK[4:1] depending on the setting of the RSCLKR bit in the S/UNI-4xD3F Receive Configuration register.

Pin Name	Type	Pin No.	Function
RSCLK[4] RSCLK[3] RSCLK[2] RSCLK[1] RGAPCLK[4] RGAPCLK[3] RGAPCLK[2] RGAPCLK[1]	Output	W13 U10 V7 U5	The Framer Recovered Clock (RSCLK[4:1]) is the recovered clock and timing reference for RDATO[4:1], RFPO/RMFPO[4:1], and ROVRHD[4:1]. The Framer Recovered Gapped Clock (RGAPCLK[4:1]) is valid by setting the RXGAPEN-bit in the S/UNI-4xD3F Configuration 2 register. RGAPCLK[4:1] is the recovered clock and timing reference for RDATO[4:1]. RGAPCLK[4:1] is held high for bit positions which correspond to overhead.
RDATO[4] RDATO[3] RDATO[2] RDATO[1]		Y14 W10 W7 Y4	The Framer Receive Data (RDATO[4:1]) is the received data aligned to RFPO/RMFPO[4:1] and ROVRHD[4:1]. RDATO[4:1] is updated on the active edge (as set by the RSCLKR register bit) of RSCLK[4:1] or RGAPCLK[4:1].
FRMSTAT[4] FRMSTAT[3] FRMSTAT[2] FRMSTAT[1]	Output	U1 U2 T4 U3	The Framer Status (FRMSTAT[4:1]) is an active high signal which can be configured to show when one of the J2, E3 or DS3 framers have detected certain conditions. The FRMSTAT[4:1] outputs can be programmed via the STATSEL[2:0] bits in the S/UNI-4xD3F Configuration 2 register to indicate: E3/DS3 LOF or J2 extended LOF, E3/DS3 OOF or J2 LOF, AIS, LOS, and DS3 Idle. FRMSTAT[4:1] should be treated as a glitch-free asynchronous signal.
CSB	Input	C9	The active low Chip Select (CSB) signal must be low to enable S/UNI-4xD3F register accesses. If CSB is not used, (RDB and WRB determine register reads and writes) then it should be tied to an inverted version of RSTB.
WRB	Input	B8	The active low Write Strobe (WRB) signal is pulsed low to enable a S/UNI-4xD3F register write access. The D[7:0] bus is clocked into the addressed register on the rising edge of WRB while CSB is low.
RDB	Input	D9	The active low Read Enable (RDB). This signal is pulsed low to enable a S/UNI-4xD3F register read access. The S/UNI-4xD3F drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	D12 C13 A14 B14 D13 C14 A15 B15	The Bi-directional Data Bus (D[7:0]) is used during S/UNI-4xD3F register read and write accesses.

Pin Name	Type	Pin No.	Function
A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	B9 B10 C10 A11 B11 C11 D11 A12 B12 C12 B13	The Address Bus (A[10:0]) selects specific registers during S/UNI-4xD3F register accesses.
RSTB	Input	C8	The Active low Reset (RSTB) signal is set low to asynchronously reset the S/UNI-4xD3F. RSTB is a Schmitt-trigger input with an integral pull-up resistor.
ALE	Input	A8	The Address Latch Enable (ALE) is active-high and latches the address bus A[10:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-4xD3F to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	Output	A7	The Active low Open-Drain Interrupt (INTB) signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.
TCK	Input	B6	The Test Clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	C7	The Test Mode Select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	D8	The Test Data Input (TDI) signal carries test data into the S/UNI-4xD3F via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Output	B7	The Test Data Output (TDO) signal carries test data out of the S/UNI-4xD3F via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	A6	The active low Test Reset (TRSTB) signal provides an asynchronous S/UNI-4xD3F test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence. Note: If not used, TRSTB must be connected to the RSTB input.
BIAS	Input	H20 U17 D4 U4	When tied to +5V, the +5V Bias (BIAS) input is used to bias the wells in the input and I/O pads so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. When tied to VDD, the inputs and bi-directional inputs will only tolerate input levels up to VDD.

Pin Name	Type	Pin No.	Function
VDD[1] VDD[2] VDD[3] VDD[4] VDD[5] VDD[6] VDD[7] VDD[8] VDD[9] VDD[10] VDD[11] VDD[12] VDD[13] VDD[14] VDD[15] VDD[16] VDD[17] VDD[18] VDD[19] VDD[20] VDD[21] VDD[22] VDD[23] VDD[24] VDD[25] VDD[26] VDD[27] VDD[28]	Power	B2 B3 B18 B19 C2 C3 C18 C19 D7 D10 D14 G4 G17 K17 L4 P4 P17 U7 U11 U14 V2 V3 V18 V19 W2 W3 W18 W19	The DC Power pins should be connected to a well-decoupled +3.3V DC supply.

Pin Name	Type	Pin No.	Function
VSS[1] VSS[2] VSS[3] VSS[4] VSS[5] VSS[6] VSS[7] VSS[8] VSS[9] VSS[10] VSS[11] VSS[12] VSS[13] VSS[14] VSS[15] VSS[16] VSS[17] VSS[18] VSS[19] VSS[20] VSS[21] VSS[22] VSS[23] VSS[24] VSS[25] VSS[26] VSS[27] VSS[28] VSS[29] VSS[30] VSS[31] VSS[32] VSS[33] VSS[34] VSS[35] VSS[35] VSS[36] VSS[37] VSS[38] VSS[39] VSS[40] VSS[41] VSS[42] VSS[43] VSS[44] VSS[45] VSS[46] VSS[47] VSS[48] VSS[49] VSS[50] VSS[51] VSS[52] VSS[53] VSS[54] VSS[55]	Ground	A1 A2 A3 A9 A10 A13 A16 A17 A18 A19 A20 B1 B16 B17 B20 C1 C15 C16 C17 C20 D15 D16 D18 D19 D20 E17 E18 E19 E20 F17 F18 F19 F20 G18 G19 G20 H1 H17 H18 J20 K18 K20 L1 L18 L19 L20 M1 N17 N18 N20 P18 P19 P20 R19 R20 U9	The DC Ground pins should be connected to GND.

Pin Name	Type	Pin No.	Function
VSS[56] VSS[57] VSS[58] VSS[59] VSS[60] VSS[61] VSS[62] VSS[63] VSS[64] VSS[65] VSS[66] VSS[67] VSS[68] VSS[69] VSS[70] VSS[71]	Ground	V1 V14 V20 W1 W5 W11 W20 Y1 Y2 Y3 Y8 Y11 Y12 Y18 Y19 Y20	The DC Ground pins should be connected to GND.
NC	No connect	D17 H19 J17 J18 J19 K19 L17 M17 M18 M19 M20 N19 R17 R18 T17 T18 T19 T20 U6 U13 U15 U16 U18 U19 U20 V8 V11 V16 V17 W16 W17 Y16 Y17	No connect.

Notes

1. All S/UNI-4xD3F inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels.

2. All S/UNI-4xD3F outputs and bi-directionals have at least 3 mA drive capability. The data bus outputs, D[7:0], have 3 mA drive capability. The outputs TCLK[4:1], TPOS [4:1], TNEG [4:1], TFPO/TMFPO/TGAPCLK[4:1], RDATO[4:1], ROVRHD[4:1], RSCLK/RGAPCLK[4:1], and REF8KO/ RFPO/RMFPO[4:1] have 6 mA drive capability. All other outputs have 3 mA drive capability.
3. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.
4. RSTB, TRSTB, TMS, TDI, TCK, REF8KI, TICLK[4:1], and RCLK[4:1] are Schmitt trigger input pads.
5. The VSS [72:1] ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-4xD3F.
6. The VDD[28:1] power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the device. These power supply connections must all be utilized and must all connect to a common +3.3 V or ground rail, as appropriate.
7. During power-up and power-down, the voltage on the BIAS pin must be kept equal to or greater than the voltage on the VDD [28:1] pins, to avoid damage to the device.

10 Functional Description

The S/UNI 4xD3F devices contains the following blocks:

- Framers for DS3, E3, and J2
- RBOC Bit-oriented code detector
- RDLC PMDL receiver
- PMON Performance monitor accumulator
- PRGD Pseudo-random sequence generator/detector
- Transmitters for DS3, E3, J2
- XBOC Bit-oriented code generator
- TDPR PMDL transmitter
- JTAG Test access port

10.1 DS3 Framer

The DS3 Framer (T3-FRMR) Block integrates the circuitry required for decoding a B3ZS-encoded signal and framing to the resulting DS3 bit stream. The T3-FRMR is directly compatible with the M23 and C-bit parity DS3 applications.

The T3-FRMR decodes a B3ZS-encoded signal and provides indications of LCVs. The B3ZS decoding algorithm and the LCV definition can be independently chosen through software. A LOS defect is also detected for B3ZS encoded streams. LOS is declared when inputs RPOS and RNEG contain zeros for 175 consecutive RCLK cycles. LOS is removed when the ones' density on RPOS and/or RNEG is greater than 33% for 175 ±1 RCLK cycles.

The framing algorithm examines five F-bit candidates simultaneously. When at least one discrepancy has occurred in each candidate, the algorithm examines the next set of five candidates. When a single F-bit candidate remains in a set, the first bit in the supposed M-subframe is examined for the M-frame alignment signal (that is, the M-bits, M1, M2, and M3 are following the 010 pattern). Framing is declared, and OOF is removed, if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. During the examination of the M-bits, the X-bits and P-bits are ignored. The algorithm gives a maximum average reframe time of 1.5 ms.

While the T3-FRMR is synchronized to the DS3 M-frame, the F-bit and M-bit positions in the DS3 stream are examined. An out-of-frame (OOF) defect is detected when 3 F-bit errors out of 8 or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration register), or when one or more M-bit errors are detected in three out of four consecutive M-frames. The M-bit error criteria for OOF can be disabled by the MBDIS bit in the DS3 Framer Configuration register. The "three out of eight consecutive F-bits OOF ratio" provides more robust operation, in the presence of a high bit error rate, than the 3 out of 16 consecutive F-bits ratio. Either OOF criteria allows an OOF defect to be detected quickly when the M-subframe alignment patterns or, optionally, when the M-frame alignment pattern is lost.

Also while in-frame, LCVs, M-bit or F-bit framing bit errors, and P-bit parity errors are indicated. When C-bit parity mode is enabled, both C-bit parity errors and FEBEs are indicated. These error indications, as well as the LCV and excessive zeros indication, are accumulated over 1-second intervals with the PMON. Note that the framer is an off-line framer, indicating both OOF and COFA events. Even if an OOF is indicated, the framer will continue indicating performance monitoring information based on the previous frame alignment.

Three DS3 maintenance signals (a RED alarm condition, the AIS, and the idle signal) are detected by the T3-FRMR. The maintenance detection algorithm uses a simple integrator with a 1:1 slope based on the occurrence of "valid" M-frame intervals. For the RED alarm, an M-frame is said to be a "valid" interval if it contains a RED defect, which is defined as an occurrence of an OOF or LOS event during that M-frame. For AIS and IDLE, an M-frame interval is "valid" if it contains AIS or IDLE, defined as the occurrence of less than 15 discrepancies in the expected signal pattern (1010... for AIS, 1100... for IDLE) while valid frame alignment is maintained. This discrepancy threshold ensures the detection algorithms operate in the presence of a 10^{-3} bit error rate. For AIS, the expected pattern may be selected to be:

- The framed "1010" signal.
- The framed arbitrary DS3 signal and the C-bits all zero.
- The framed "1010" signal and the C-bits all zero.
- The framed all-ones signal (with overhead bits ignored).
- The unframed all-ones signal (with overhead bits equal to ones).

Each "valid" M-frame causes an associated integration counter to increment; "invalid" M-frames cause a decrement. With the "slow" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 127, which results in a detection time of 13.5 ms. With the "fast" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 21, which results in a detection time of 2.23 ms (i.e., 1.5 times the maximum average reframe time). RED, AIS, or IDLE are removed when the respective counter decrements to 0. DS3 LOF detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an OOF condition and integrates down when the framer de-asserts the OOF condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

Valid X-bits are extracted by the T3-FRMR to provide indication of FERF (FERF). A FERF defect is detected if the extracted X-bits are equal and are logic zero (X1=X2=0); the defect is removed if the extracted X-bits are equal and are logic one (X1=X2=1). If the X-bits are not equal, the FERF status remains in its previous state. The extracted FERF status is buffered for 2 M-frames before being reported within the DS3 FRMR Status register. This buffer ensures a better than 99.99% chance of freezing the FERF status on a correct value during the occurrence of an OOF.

When the C-bit parity application is enabled, both the FEAC channel and the PMDL are extracted. Codes in the FEAC channel are detected by the Bit Oriented Code Detector (RBOC). HDLC messages in the PMDL are received by the Data Link Receiver (RDLC).

The T3-FRMR can be enabled to automatically assert the RAI, the outgoing transmit stream upon detection of any combination of LOS, OOF or RED, or AIS. The T3-FRMR can also be enabled to automatically insert C-bit Parity FEBE upon detection of receive C-bit parity error.

The T3-FRMR extracts the entire DS3 overhead (56 bits per M-frame) using the ROH output, along with the ROHCLK, and ROHFP outputs.

The T3-FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the T3-FRMR. Access to these registers is via a generic microprocessor bus.

10.2 E3 Framer

The E3 Framer (E3-FRMR) Block integrates circuitry required for decoding an HDB3-encoded signal and framing to the resulting E3 bit stream. The E3-FRMR is directly compatible with the G.751 and G.832 E3 applications.

The E3-FRMR searches for frame alignment in the incoming serial stream based on either the G.751 or G.832 formats. For the G.751 format, the E3-FRMR expects to see the selected framing pattern error-free for three consecutive frames before declaring INFRAME. For the G.832 format, the E3-FRMR expects to see the selected framing pattern error-free for two consecutive frames before declaring INFRAME. Once the frame alignment is established, the incoming data is continuously monitored for framing bit errors and byte interleaved parity (BIP) errors (in G.832 format).

While in-frame, the E3-FRMR also extracts various overhead bytes and processes them according to the framing format selected:

In G.832 E3 format, the E3-FRMR extracts:

- The Trail Trace bytes and outputs them as a serial stream for further processing by the Trail Trace Buffer (TTB) block.
- The FERF-bit and indicates an alarm when the FERF-bit is a logic one for three or five consecutive frames. The FERF indication is removed when the FERF-bit is a logic zero for three or five consecutive frames.
- The FEBE bit and outputs it for accumulation in PMON.
- The Payload Type bits and buffers them so that they can be read by the microprocessor.
- The Timing Marker bit and asserts the Timing Marker indication when the value of the extracted bit has been in the same state for three or five consecutive frames.
- The Network Operator byte and presents it as a serial stream for further processing by the RDLC block when the RNETOP bit in the S/UNI-4xD3F Data Link and FERF Control register is logic one. The byte is also brought out on the ROH[x] output with an associated clock on ROHCLK[x]. All eight bits of the Network Operator byte are extracted and presented on the overhead output and, optionally, presented to the RDLC.

- The General Purpose Communication Channel byte and presents it to the RDLC when the RNETOP bit in the S/UNI-4xD3F Data Link and FERF Control register is logic zero. The byte is also brought out on the ROH[x] output with an associated clock on ROHCLK[x].

In G.751 E3 mode, the E3-FRMR extracts:

- The RAI bit (bit 11 of the frame) and indicates a Remote Alarm when the RAI bit is a logic one for three or five consecutive frames. Similarly, the Remote Alarm is removed when the RAI bit is logic zero for three or five consecutive frames.
- The National Use reserved bit (bit 12 of the frame) and presents it as a serial stream for further processing in the RDLC when the RNETOP bit in the S/UNI-4xD3F Data Link and FERF Control register is logic zero. The bit is also brought out on the ROH[x] output with an associated clock on ROHCLK[x]. Optionally, an interrupt can be generated when the National Use bit changes state.

Further, while in-frame, the E3-FRMR indicates the position of all the overhead bits in the incoming digital stream. For G.751 mode, the tributary justification bits can optionally be identified as either overhead or payload for payload mappings that take advantage of the full bandwidth.

The E3-FRMR declares OOF alignment if the framing pattern is in error for four consecutive frames. The E3-FRMR is an “off-line” framer, where all frame alignment indications, all overhead bit indications, and all overhead bit processing continue based on the previous alignment. Once the framer has determined the new frame alignment, the OOF indication is removed and a COFA indication is declared if the new alignment differs from the previous alignment.

The E3-FRMR detects the presence of AIS in the incoming data stream when less than 8 zeros in a frame are detected while the framer is OOF in G.832 mode, or when less than five zeros in a frame are detected while OOF in G.751 mode. This algorithm provides a probability of detecting AIS in the presence of a 10^{-3} BER as 92.9% in G.832 and 98.0% in G.751.

LOS is declared when no marks have been received for 32 consecutive bit-periods. LOS is de-asserted after 32 bit-periods during which there is no sequence of four consecutive zeros.

E3 LOF detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1 ms, 2 ms, or 3 ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an OOF condition and integrates down when the framer de-asserts the OOF condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

The E3-FRMR can also be enabled to automatically assert the RAI/FERF indication in the outgoing transmit stream upon detection of any combination of LOS, OOF, or AIS. The E3-FRMR can also be enabled to automatically insert G.832 FEBE upon detection of receive BIP-8 errors.

10.3 J2 Framer

The J2-FRMR integrates circuitry to decode a unipolar or B8ZS encoded signal and frame to the resulting 6312 kbps J2 bit stream. Having found frame, the J2-FRMR extracts a variety of overhead and datalink information from the J2 bit stream.

The J2 format consists of 789-bit frames, each 125 µs long, consisting of 96 bytes of payload, 2 reserved bytes, and 5 F-bits. The frames are grouped into 4-frame multiframes. The multiframe format is as follows:

Table 3 J2 Framer Multiframe Format

Bit	1-8	...	761–768	769–776	777–784	785	786	787	788	789
1	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	1	1	0	0	m
2	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	1	0	1	0	0
3	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	x1	x2	x3	a	m
4	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	e1	e2	e3	e4	e5

Notes

1. *TS1* .. *TS96* is the byte interleaved payload.
2. *TS97* and *TS98* are reserved channels for signaling.
3. The Frame Alignment Signal is represented as binary ones and zeroes.
4. *m* is a 4 kHz datalink.
5. *x1*, *x2*, *x3* are spare bits, usually logic one.
6. *a* is the Remote LOF alarm bit, active high.
7. *e1*, *e2*, *e3*, *e4*, and *e5* are the CRC-5 check sequence. The entire 3156-bit multiframe, including the CRC-5 check sequence, should have a remainder of 0 when divided by $x^5 + x^4 + x^2 + 1$.

The J2-FRMR frames to a J2 signal with an average reframe time of 5.07 ms. An alternate framing algorithm that uses the CRC-5 check to detect static mimic patterns is available. Once in frame, the J2-FRMR provides indications of frame and multiframe boundaries, and marks overhead bits, x-bits, m-bits, and reserved channels (TS97 and TS98). LOS, bipolar violations, excessive zeroes, change of frame alignment, framing errors, and CRC errors are indicated and can be accumulated by the PMON (with the exception of change of frame alignment). Maskable interrupts are available to alert the microprocessor to the occurrence of any of these events. In addition to marking x-bit values, J2-FRMR provides microprocessor access to the x-bits, and will optionally generate an interrupt when any of the x-bits changes state. The m-bits and the associated clock are can either be extracted through the RDLC or through the ROH[x] and ROHCLK[x] output pins of the S/UNI-4xD3F. The m-bits are also presented to the RBOC for detection of any generic bit-oriented codes.

Status signals such as Physical AIS, Payload AIS, RAI in m-bits, and Remote LOF (a-bit) are detected by the J2-FRMR. In addition to providing indication signals of these states, the J2-FRMR will optionally generate an interrupt when any of these status signals changes.

J2 LOS is declared when no marks have been received for one of 15, 31, 63, or 255 consecutive bit periods. J2 LOS is cleared when either 15, 31, 63, or 255 consecutive bit periods have passed without an excessive zeros (8 or more consecutive zeros) detection as required by ITU-T G.775.

J2 LOF is declared when seven or more consecutive multiframes with errored framing patterns are received. The J2 LOF is cleared when three or more consecutive multiframes with correct framing patterns are received. A framing algorithm which takes into account the CRC calculation is also available. The framing algorithms are described in Section 10.3.1.

J2 Physical Layer AIS is declared when two or less zeros are detected in a sequence of 3156 bits. It is cleared when three or more zeros are detected in a sequence of 3156 bits as required by ITU-T G.775.

J2 Payload AIS is detected when the incoming J2 payload has two or less zeros in a sequence of 3072 bits. It is cleared when three or more zeros are detected in a sequence of 3072 bits.

The J2-FRMR may be forced to re-frame by microprocessor control. Similarly, the microprocessor may disable the J2-FRMR from reframing due to framing bit errors.

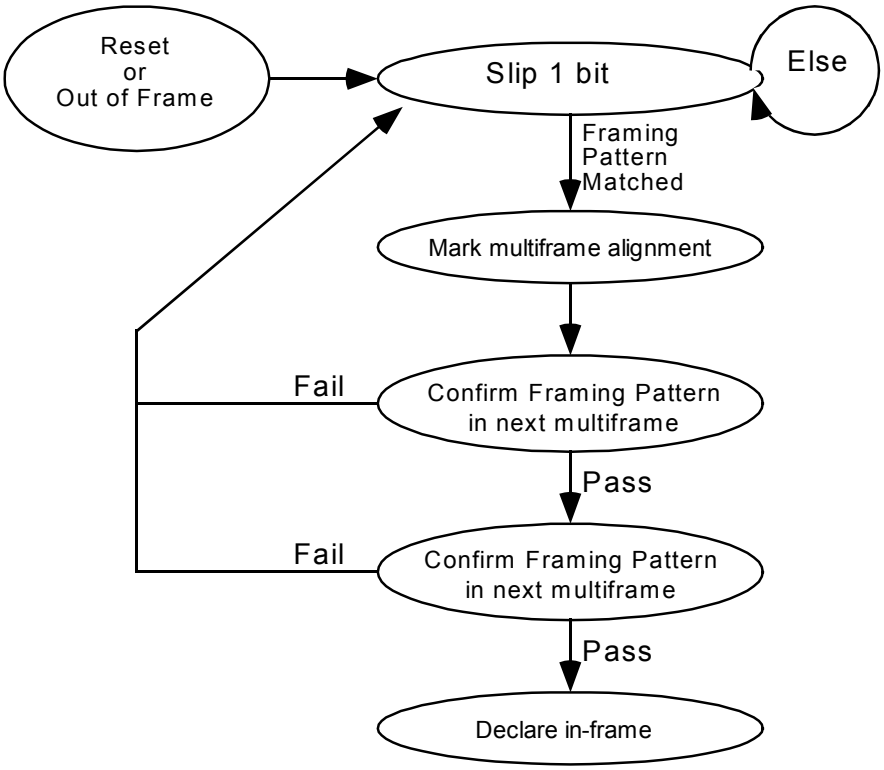
The J2-FRMR may be configured, and all sources of interrupts may be masked or acknowledged, via internal registers. These internal registers are accessed through a generic microprocessor bus.

10.3.1 J2 Frame Find Algorithms

The J2-FRMR searches for frame alignment using one of two algorithms, as selected by the CRC_REFR bit in the J2-FRMR Configuration register.

When the CRC_REFR bit is set to logic zero, the J2-FRMR uses only the frame alignment sequence to find frame, searching for three consecutive correct frame alignment sequences. The frame find block searches for the entire 9-bit sequence (spread over two multiframes) at the same time, greatly reducing the time required to find frame alignment. The framing process with CRC-REFR cleared is illustrated in Figure 3.

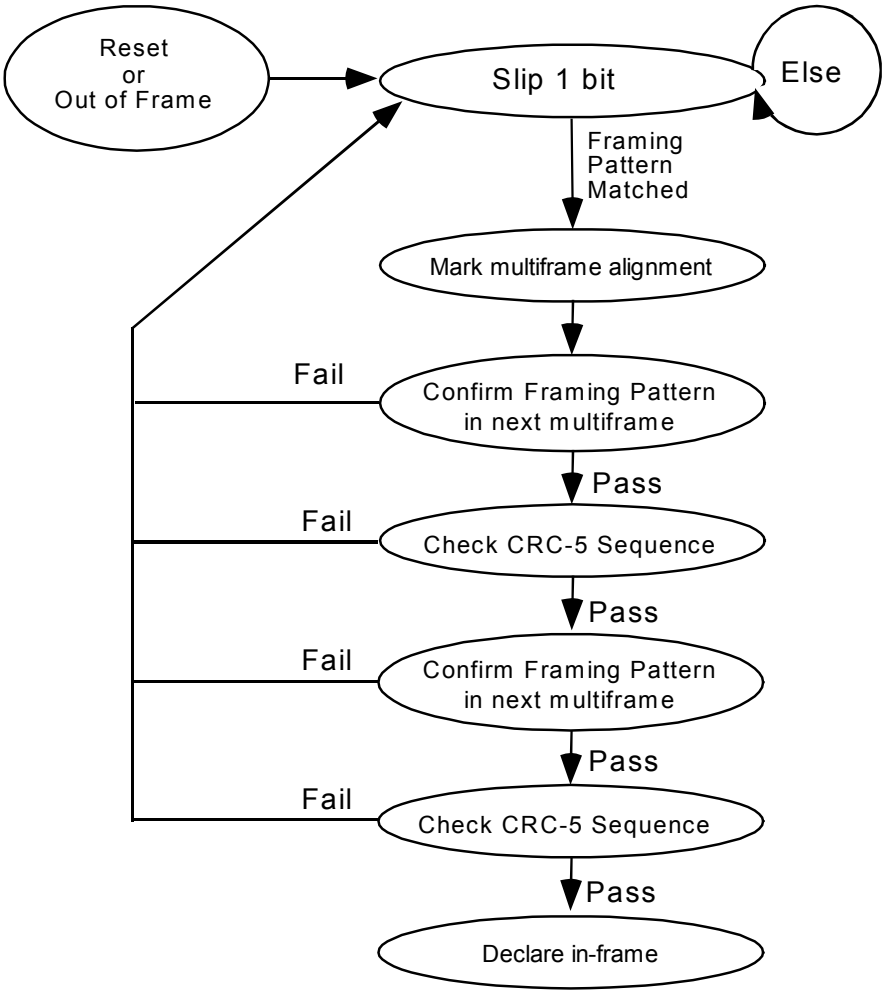
Figure 3 Framing Algorithm (CRC_REFR = 0)



Using this algorithm, the J2-FRMR will on average find frame in 5.07 ms when starting the search in the worst possible position, given a 10^{-4} error rate and no static mimic patterns.

When the CRC_REFR bit is set to logic one, in addition to requiring three consecutive correct framing patterns, the J2-FRMR requires that the first two CRC-5 checks be correct, or a reframe is initiated. To speed the process, the CRC-5 and frame alignment checks are run concurrently, as illustrated in Figure 4.

Figure 4 Framing Algorithm (CRC_REFR = 1)



Using this algorithm, the J2-FRMR will find frame in 10.22 ms, on average when starting the search in the worst possible position, given a 10^{-4} error rate and no static mimic patterns. The algorithm will reject 99.90% of mimic patterns. Further protection against mimic patterns is available by monitoring the rate of CRC-5 errors.

Once frame alignment is found, the block sets the LOF indication low, indicates a change of frame alignment (if it occurred). The block declares LOF alignment if seven consecutive framing algorithm signals (FAS) have been received in error. In the presence of a random 10^{-3} bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of 1.65 years. The Frame Find Block can be forced to initiate a frame search at any time when the REFRAME bit in the J2-FRMR Configuration. Conversely, when the FLOCK bit is set to logic one, the J2-FRMR will never declare LOF or search for a new frame alignment due to excess framing bit errors.

J2 extended LOF detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1 ms, 2 ms, or 3 ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an OOF condition and integrates down when the framer de-asserts the OOF condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

10.4 RBOC Bit-Oriented Code Detector

The Bit-Oriented Code Detector (RBOC) is only used in DS3 C-bit Parity or J2 mode.

The RBOC Block detects the presence of 63 of the 64 possible bit-oriented codes (BOCs) contained in the DS3 C-bit parity FEAC channel or in the J2 datalink signal stream. The 64th code (“111111”) is similar to the HDLC flag sequence and is ignored.

Bit-oriented codes (BOCs) are received on the FEAC channel as 16-bit sequences each consisting of 8 ones, a zero, 6 code bits, and a trailing zero (“111111110xxxxxx0”). BOCs are validated when repeated at least 10 times. The RBOC can be enabled to declare a code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable register. The RBOC declares that the code is removed if two code sequences containing code values different from the detected code are received in a moving window of ten code periods.

Valid BOCs are indicated through the RBOC Interrupt Status register. The BOC bits are set to all-ones (“111111”) when no valid code is detected. The RBOC can be programmed to generate an interrupt when a detected code has been validated and when the code is removed.

10.5 RDLC PMDL Receiver

The RDLC is a microprocessor peripheral used to receive LAPD/HDLC frames on any serial HDLC bit stream that provides data and clock information such as the DS3 C-bit parity path maintenance data link (PMDL), the E3 G.832 Network Requirement byte or the General Purpose data link (selectable using the RNETOP bit in the S/UNI-4xD3F Data Link and FERF/RAI Control register), the E3 G.751 Network Use bit, or the J2 m-bit Data Link.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all-ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status register contains bits which indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the Status register indicates the FCS status and if the packet contained a non-integer number of bytes.

10.6 PMON Performance Monitor Accumulator

The PMON Block interfaces directly with either the DS3 Framer (T3-FRMR) to accumulate LCV events, parity error (PERR) events, path parity error (CPERR) events, FEBE events, excess zeros (EXZS), and Framing bit errors (FERR) events using saturating counters; the E3 Framer (E3-FRMR) to accumulate LCV, PERR (in G.832 mode), FEBE and FERR events; or the J2 Framer (J2-FRMR) to accumulate LCVs, CRC errors (in the PERR counter), FERR, and EXZS. The PMON stops accumulating error signal from the E3, DS3, or J2 Framers once frame synchronization is lost.

When an accumulation interval is signaled by a write to the PMON register address space or a write to the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update register, the PMON transfers the current counter values into microprocessor accessible holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

When counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled. If the holding registers have not been read since the last interrupt, an overrun status bit is set. In addition, a register is provided to indicate changes in the PMON counters since the last accumulation interval.

10.7 PRGD Pseudo-Random Sequence Generator/Detector

The Pseudo-Random Sequence Generator/Detector (PRGD) block is a software programmable test pattern generator, receiver, and analyzer. Two types of test patterns (pseudo-random and repetitive) conform to ITU-T O.151.

The PRGD can be programmed to generate any pseudo-random pattern with length up to 2^{32}-1 bits or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rate between 10^{-1} to 10^{-7}.

The PRGD can be programmed to check for the presence of the generated pseudo-random pattern. The PRGD can perform an auto-synchronization to the expected pattern, and generate interrupts on detection and loss of the specified pattern. The PRGD can accumulate the total number of bits received and the total number of bit errors in two saturating 32-bit counters. The counters accumulate over an interval defined by writes to the S/UNI-4xD3F Identification/Master Reset, and Global Monitor Update register (006H) or by writes to any PRGD accumulation register. When an accumulation is forced by either method, then the holding registers are updated, and the counters reset to begin accumulating for the next interval. The counters are reset in such a way that no events are missed. The data is then available in the holding registers until the next accumulation. In addition to the two counters, a record of the 32 bits received immediately prior to the accumulation is available.

The PRGD may also be programmed to check for repetitive sequences. When configured to detect a pattern of length N-bits, the PRGD will load N-bits from the detected stream, and determine whether the received pattern repeats itself every N subsequent bits. Should it fail to find such a pattern, it will continue loading and checking until it finds a repetitive pattern. All the features (error counting, auto-synchronization, etc.) available for pseudo-random sequences are also available for repetitive sequences. Whenever a PRGD accumulation is forced, the PRGD stores a snapshot of the 32 bits received immediately prior to the accumulation. This snapshot may be examined in order to determine the exact nature of the repetitive pattern received by PRGD.

The pseudo-random or repetitive pattern can be inserted/extracted in the DS3, E3, or J2.

10.8 DS3 Transmitter

The DS3 Transmitter (T3-TRAN) Block integrates circuitry required to insert the overhead bits into a DS3 bit stream and produce a B3ZS-encoded signal. The T3-TRAN is directly compatible with the M23 and C-bit parity DS3 formats.

Status signals such as FERF, AIS, and the idle signal can be inserted when their transmission is enabled by internal register bits. FERF can also be automatically inserted on detection of any combination of LOS, OOF or RED, or AIS by the T3-FRMR.

A valid pair of P-bits is automatically calculated and inserted by the T3-TRAN. When C-bit parity mode is selected, the path parity bits, and FEBE indications are automatically inserted.

When enabled for C-bit parity operation, the FEAC channel is sourced by the XBOC bit-oriented code transmitter. The PMDL messages are sourced by the TDPR data link transmitter. These overhead signals can also be overwritten by using the TOH[x] and TOHINS[x] inputs.

When enabled for M23 operation, the C-bits are forced to logic one with the exception of the C-bit Parity ID bit (first C-bit of the first M-subframe), which is forced to toggle every M-frame.

The T3-TRAN supports diagnostic modes in which it inserts parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, LCVs, or all-zeros.

User control of each of the overhead bits in the DS3 frame is provided. Overhead bits may be inserted on a bit-by-bit basis from a user supplied data stream. An overhead clock (at 526 kHz) and a DS3 overhead alignment output are provided to allow for control of the user provided stream.

10.9 E3 Transmitter

The E3 Transmitter (E3-TRAN) Block integrates circuitry required to insert the overhead bits into an E3 bit stream and produce an HDB3-encoded signal. The E3-TRAN is directly compatible with the G.751 and G.832 framing formats.

The E3-TRAN generates the frame alignment signal and inserts it into the incoming serial stream based on either the G.751 or G.832 formats. All overhead and status bits in each frame format can be individually controlled by register bits or by the transmit overhead stream. While in certain framing format modes, the E3-TRAN generates various overhead bytes according to the following:

In G.832 E3 format, the E3-TRAN:

- Inserts the BIP-8 byte calculated over the preceding frame.
- Inserts the Trail Trace bytes through the TTB block.
- Inserts the FERF-bit via a register bit or, optionally, when the E3-FRMR declares OOF, or when the LCD defect is declared.
- Inserts the FEBE bit, which is set to logic one when one or more BIP-8 errors are detected by the receive framer. If there are no BIP-8 errors indicated by the E3-FRMR, the E3-TRAN sets the FEBE bit to logic zero.
- Inserts the Payload Type bits based on the register value set by the microprocessor.
- Inserts the Tributary Unit multiframe indicator bits either via the TOH overhead stream or by register bit values set by the microprocessor.
- Inserts the Timing Marker bit via a register bit.
- Inserts the Network Operator (NR) byte from the TDPR block when the TNETOP bit in the S/UNI-4xD3F Data Link and FERF Control register is logic one; otherwise, the NR byte is set to all-ones. The NR byte can be overwritten by using the TOH[x] and TOHINS[x] input pins. All eight bits of the Network Operator byte are available for use as a datalink.
- Inserts the General Purpose Communication Channel (GC) byte from the TDPR block when the TNETOP bit in the S/UNI-4xD3F Data Link and FERF Control register is logic zero; otherwise, the byte is set to all-ones. The GC byte can be overwritten by using the TOH[x] and TOHINS[x] input pins.

In G.751 E3 mode, the E3-TRAN :

- Inserts the RAI bit (bit 11 of the frame) either via a register bit or, optionally, when the E3-FRMR declares OOF;
- Inserts the National Use reserved bit (bit 12 of the frame) either as a fixed value through a register bit or from the TDPR block as configured by the TNETOP bit in the S/UNI-4xD3F Data Link and FERF Control register and the NATUSE bit in the E3 TRAN Configuration register.
- Optionally identifies the tributary justification bits and stuff opportunity bits as either overhead or payload to SPLT for payload mappings that take advantage of the full bandwidth.

Further, the E3-TRAN can provide insertion of bit errors in the framing pattern or in the parity bits, and insertion of single LCVs for diagnostic purposes. Most of the overhead bits can be overwritten by using the TOH[x] and TOHINS[x] input pins.

10.10 J2 Transmitter

The J2 Transmitter (J2-TRAN) Block integrates circuitry required to insert the overhead bits into an J2 bit stream and produce a B8ZS-encoded signal. The J2-TRAN is directly compatible with the framing format specified in G.704 and NTT Technical Reference for High-Speed Digital Leased Circuit Services.

The J2-TRAN generates the frame alignment signal and inserts it into the incoming serial stream. All overhead and status bits in each frame format can be individually controlled by either register bits or by the transmit overhead stream.

The J2-TRAN:

- Inserts the CRC-5 bits calculated over the preceding multiframe.
- Inserts the x-bits through microprocessor programmable register bits.
- Inserts the a-bit through a microprocessor programmable register bit.
- Inserts the m-bit data link through the TDPR block.
- Inserts payload AIS or physical layer AIS through microprocessor programmable register bits.
- Inserts RAI over the m-bits, overwriting HDLC frames, by using the XBOC block or through automatic activation upon detection of certain remote alarm conditions.

The J2-TRAN allows overwriting of any of the overhead bits by using the TOH[x], TOHINS[x], TOHFP[x], and TOHCLK[x] overhead signals. Further, the J2-TRAN can provide insertion of single bit errors in the framing pattern or in the CRC-5 bits, and insertion of single LCVs for diagnostic purposes.

10.11 XBOC Bit Oriented Code Generator

The Bit Oriented Code Generator (XBOC) Block transmits 63 of the possible 64 BOCs in the C-bit parity FEAC channel. A BOC is a 16-bit sequence consisting of eight ones, a zero, six code bits, and a trailing zero (111111110xxxxxx0) that is repeated as long as the code is not 111111. The code to be transmitted is programmed by writing the XBOC Code register. The 64th code (111111) is similar to the HDLC idle sequence and is used to disable the transmission of any bit oriented codes. When transmission is disabled, the FEAC channel is set to all-ones.

10.12 TDPR PMDL Transmitter

The Path Maintenance Data Link Transmitter (TDPR) provides a serial data link for the C-bit parity PMDL in DS3, the serial Network Operator byte or the General Purpose datalink in G.832 E3, the National Use bit datalink in G.751 E3, or the m-bit datalink in J2. The TDPR is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT FCS can be appended, followed by flags. If the TDPR transmit data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits flags (01111110) until data is ready to be transmitted. Data bytes to be transmitted are written into the TDPR Transmit Data register. The TDPR automatically begins transmission of data once at least one complete packet is written into its FIFO. All complete packets of data will be transmitted if no error condition occurs. After the last data byte of a packet, the CRC FCS (if CRC insertion has been enabled) and a flag, or just a flag (if CRC insertion has not been enabled) is transmitted. The TDPR then returns to the transmission of flag characters until the next packet is available for transmission. The TDPR will also force transmission of the FIFO data once the FIFO depth has surpassed the programmable upper limit threshold. Transmission commences regardless of whether or not a packet has been completely written into the FIFO. The user must be careful to avoid overfilling the FIFO. Underruns can only occur if the packet length is greater than the programmed upper limit threshold because, in such a case, transmission will begin before a complete packet is stored in the FIFO.

An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data. Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort sequences (01111111 sequence where the 0 is transmitted first) can be continuously transmitted at any time by setting a control bit. During packet transmission, an underrun situation can occur if data is not written to the TDPR Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDR register bit. An abort sequence will also be transmitted if the user overflows the FIFO with a packet of length greater than 128 bytes. Overflows where other complete packets are still stored in the FIFO will not generate an abort. Only the packet which caused the overflow is corrupted and an interrupt is generated to the user via the OVR register bit. The other packets remain unaffected.

When the TDPR is disabled, a logic one (Idle) is inserted in the PMDL.

10.13 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-4xD3F identification code is 073460CD hexadecimal.

10.14 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. Normal mode registers are required for normal operation. Test mode registers are used to enhance the testability of the S/UNI-4xD3F.

The register set is accessed as described in Table 4.

Table 4 Register Memory Map

Address				Register
000H	100H	200H	300H	S/UNI-4xD3F Configuration 1
001H	101H	201H	301H	S/UNI-4xD3F Configuration 2
002H	102H	202H	302H	S/UNI-4xD3F Transmit Configuration
003H	103H	203H	303H	S/UNI-4xD3F Receive Configuration
004H	104H	204H	304H	S/UNI-4xD3F Data Link and FERF/RAI Control
005H	105H	205H	305H	S/UNI-4xD3F Interrupt Status
006H				S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update
	106H	206H	306H	S/UNI-4xD3F Reserved
007H	107H	207H	307H	S/UNI-4xD3F Clock Activity Monitor and Interrupt Identification
010H	110H	210H	310H	PMON Change of PMON Performance Meters
011H	111H	211H	311H	PMON Interrupt Enable/Status
012H-013H	112H-113H	212H-213H	312H-313H	PMON Reserved
014H	114H	214H	314H	PMON LCV Event Count LSB
015H	115H	215H	315H	PMON LCV Event Count MSB
016H	116H	216H	316H	PMON Framing Bit Error Event Count LSB
017H	117H	217H	317H	PMON Framing Bit Error Event Count MSB
018H	118H	218H	318H	PMON Excessive Zeros Count LSB
019H	119H	219H	319H	PMON Excessive Zeros Count MSB
01AH	11AH	21AH	31AH	PMON Parity Error Event Count LSB
01BH	11BH	21BH	31BH	PMON Parity Error Event Count MSB
01CH	11CH	21CH	31CH	PMON Path Parity Error Event Count LSB
01DH	11DH	21DH	31DH	PMON Path Parity Error Event Count MSB
01EH	11EH	21EH	31EH	PMON FEBE/J2-EXZS Event Count LSB
01FH	11FH	21FH	31FH	PMON FEBE/J2-EXZS Event Count MSB
030H	130H	230H	330H	DS3 FRMR Configuration
031H	131H	231H	331H	DS3 FRMR Interrupt Enable
032H	132H	232H	332H	DS3 FRMR Interrupt Status
033H	133H	233H	333H	DS3 FRMR Status
034H	134H	234H	334H	DS3 TRAN Configuration

Address				Register
035H	135H	235H	335H	DS3 TRAN Diagnostics
036H-037H	136H-137H	236H-237H	336H-337H	DS3 TRAN Reserved
038H	138H	238H	338H	E3 FRMR Framing Options
039H	139H	239H	339H	E3 FRMR Maintenance Options
03AH	13AH	23AH	33AH	E3 FRMR Framing Interrupt Enable
03BH	13BH	23BH	33BH	E3 FRMR Framing Interrupt Indication and Status
03CH	13CH	23CH	33CH	E3 FRMR Maintenance Event Interrupt Enable
03DH	13DH	23DH	33DH	E3 FRMR Maintenance Event Interrupt Indication
03EH	13EH	23EH	33EH	E3 FRMR Maintenance Event Status
03FH	13FH	23FH	33FH	E3 FRMR Reserved
040H	140H	240H	340H	E3 TRAN Framing Options
041H	141H	241H	341H	E3 TRAN Status and Diagnostic Options
042H	142H	242H	342H	E3 TRAN BIP-8 Error Mask
043H	143H	243H	343H	E3 TRAN Maintenance and Adaptation Options
044H	144H	244H	344H	J2 FRMR Configuration
045H	145H	245H	345H	J2 FRMR Status
046H	146H	246H	346H	J2 FRMR Alarm Interrupt Enable
047H	147H	247H	347H	J2 FRMR Alarm Interrupt Status
048H	148H	248H	348H	J2 FRMR Error/X-bit Interrupt Enable
049H	149H	249H	349H	J2 FRMR Error/X-bit Interrupt Status
04AH-04BH	14AH-14BH	24AH-24BH	34AH-34BH	J2 FRMR Reserved
04CH	14CH	24CH	34CH	J2 TRAN Configuration
04DH	14DH	24DH	34DH	J2 TRAN Diagnostics
04EH	14EH	24EH	34EH	J2 TRAN TS97 Signaling
04FH	14FH	24FH	34FH	J2 TRAN TS98 Signaling
050H	150H	250H	350H	RDLC Configuration
051H	151H	251H	351H	RDLC Interrupt Control
052H	152H	252H	352H	RDLC Status
053H	153H	253H	353H	RDLC Data
054H	154H	254H	354H	RDLC Primary Address Match
055H	155H	255H	355H	RDLC Secondary Address Match
056H	156H	256H	356H	RDLC Reserved
057H	157H	257H	357H	RDLC Reserved
058H	158H	258H	358H	TDPR Configuration
059H	159H	259H	359H	TDPR Upper Transmit Threshold
05AH	15AH	25AH	35AH	TDPR Lower Interrupt Threshold
05BH	15BH	25BH	35BH	TDPR Interrupt Enable
05CH	15CH	25CH	35CH	TDPR Interrupt Status/UDR Clear

Address				Register
05DH	15DH	25DH	35DH	TDPR Transmit Data
05EH-05FH	15EH-15FH	25EH-25FH	35EH-35FH	TDPR Reserved
090H	180H	290H	390H	TTB Control Register
091H	181H	291H	391H	TTB Trail Trace Identifier Status
092H	182H	292H	392H	TTB Indirect Address Register
093H	183H	293H	393H	TTB Indirect Data Register
094H	184H	294H	394H	TTB Expected Payload Type Label Register
095H	195H	295H	395H	TTB Payload Type Label Control/Status
096H-097H	196H-197H	296H-297H	396H-397H	TTB Reserved
098H	198H	298H	398H	RBOC Configuration/Interrupt Enable
099H	199H	299H	399H	RBOC Status
09AH	19AH	29AH	39AH	XBOC Code
09BH	19BH	29BH	39BH	S/UNI-4xD3F Misc.
09CH	19CH	29CH	39CH	S/UNI-4xD3F FRMR LOF Status.
0A0H	1A0H	2A0H	3A0H	PRGD Control
0A1H	1A1H	2A1H	3A1H	PRGD Interrupt Enable/Status
0A2H	1A2H	2A2H	3A2H	PRGD Length
0A3H	1A3H	2A3H	3A3H	PRGD Tap
0A4H	1A4H	2A4H	3A4H	PRGD Error Insertion
0A5H-0A7H	1A5H-1A7H	2A5H-2A7H	3A5H-3A7H	PRGD Reserved
0A8H	1A8H	2A8H	3A8H	PRGD Pattern Insertion Register #1
0A9H	1A9H	2A9H	3A9H	PRGD Pattern Insertion Register #2
0AAH	1AAH	2AAH	3AAH	PRGD Pattern Insertion Register #3
0ABH	1ABH	2ABH	3ABH	PRGD Pattern Insertion Register #4
0ACH	1ACH	2ACH	3ACH	PRGD Pattern Detector Register #1
0ADH	1ADH	2ADH	3ADH	PRGD Pattern Detector Register #2
0AEH	1AEH	2AEH	3AEH	PRGD Pattern Detector Register #3
0AFH	1AFH	2AFH	3AFH	PRGD Pattern Detector Register #4
0B0H-0FFH	1B0H-1FFH	2B0H-2FFH	3B0H-3FFH	S/UNI-4xD3F Reserved
400H				S/UNI-4xD3F Master Test Register
401H - 7FFH				Reserved for S/UNI-4xD3F Test

Note

1. CSB must be low for all register accesses.

11 Normal Mode Register Descriptions

Normal mode registers are used to configure and monitor the operation of the S/UNI-4xD3F. Normal mode registers (as opposed to test mode registers) are selected when A[10] is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-4xD3F to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-4xD3F operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-4xD3F operates as intended, reserved register bits must only be written with the suggested logic levels. Similarly, writing to reserved registers should be avoided.

6. The S/UNI-4xD3F requires a software initialization sequence in order to guarantee proper device operation and long term reliability. Please refer to Section 10.1 of this document for the details on how to program this sequence.

7. All reserved bits *must be* programmed in order for device to function properly.

Register 000H, 100H, 200H, 300H: S/UNI-4xD3F Configuration

Bit	Type	Function	Default
Bit 7	R/W	8KREFO	1
Bit 6	R/W	Reserved6	1
Bit 5	R/W	Reserved5	0
Bit 4	R/W	FRAMER	0
Bit 3	R/W	LOOPT	0
Bit 2	R/W	LLOOP	0
Bit 1	R/W	DLOOP	0
Bit 0	R/W	PLOOP	0

PLOOP

The PLOOP bit controls the DS3, E3, or J2 payload loopback. When a logic zero is written to PLOOP, DS3, E3, or J2 payload loopback is disabled. When a logic one is written to PLOOP, the DS3, E3, or J2 overhead bits are regenerated and inserted into the received DS3, E3, or J2 stream and the resulting stream is transmitted. Setting the PLOOP bit disables the effect of the TICLK bit in the S/UNI-4xD3F Transmit Configuration register, thereby forcing flow-through timing. The TFRM[1:0] and RFRM[1:0] bits in the S/UNI-4xD3F Transmit Configuration and Receive Configuration registers respectively, must be set to the same value for PLOOP to work properly.

DLOOP

The DLOOP bit controls the diagnostic loopback. When a logic zero is written to DLOOP, diagnostic loopback is disabled. When a logic one is written to DLOOP, the transmit data stream is looped in the receive direction. The TFRM[1:0] and RFRM[1:0] bits in the S/UNI-4xD3F Transmit Configuration and Receive Configuration registers respectively, must be set to the same value for DLOOP to work properly. The DLOOP should not be set to a logic one when either the PLOOP, LLOOP, or LOOPT bit is a logic one. The TUNI register bit in the S/UNI-4xD3F Transmit Configuration register should be set to the same value as the UNI bit in the DS3, E3, or J2 FRMR registers.

LLOOP

The LLOOP bit controls the line loopback. When a logic zero is written to LLOOP, line loopback is disabled. When a logic one is written to LLOOP, the stream received on RPOS/RDATI and RNEG/RLCV/ROHM is looped to the TPOS/TDATO and TNEG/TOHM outputs. Note that the TPOS, TNEG, and TCLK outputs are referenced to RCLK when LLOOP is logic one.

LOOPT

The LOOPT bit selects the transmit timing source. When a logic one is written to LOOPT, the transmitter is loop-timed to the receiver. When loop timing is enabled, the receive clock (RCLK) is used as the transmit timing source. Setting the LOOPT bit disables the effect of the TICLK and TXREF-bits in the S/UNI-4xD3F Transmit Configuration and S/UNI-4xD3F Configuration 2 registers, respectively, thereby forcing flow-through timing.

FRAMER

This bit must be programmed to logic one for proper operation.

Reserved5

This reserved bit must be programmed to logic zero for proper operation..

Reserved6

This reserved bit must be programmed to logic one for proper operation.

8KREFO

If 8KREFO is logic one1, then an 8kHz reference will be derived from the RCLK[x] signal and output on REF8KO. If 8KREFO is logic zero, then the RXMFPO register bit in the S/UNI-4xD3F Configuration 2 registers will select either the RFPO or RMFPO function.

Register 001H, 101H, 201H, 301H: S/UNI-4xD3F Configuration 2

Bit	Type	Function	Default
Bit 7	R/W	STATSEL[2]	0
Bit 6	R/W	STATSEL[1]	0
Bit 5	R/W	STATSEL[0]	0
Bit 4	R/W	TXMFPI	0
Bit 3	R/W	TXGAPEN	0
Bit 2	R/W	RXGAPEN	0
Bit 1	R/W	TXMFPO	0
Bit 0	R/W	RXMFPO	0

RXMFPO

The RXMFPO bit controls which of the outputs RMFPO[4:1] or RFPO[4:1] is valid. If RXMFPO is a logic one, then RMFPO[4:1] will be available. If RXMFPO is a logic zero, then RFPO[4:1] will be available. This bit is effective only if the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is a logic one.

TXMFPO

The TXMFPO bit controls which of the outputs TMFPO[4:1] or TFPO[4:1] is valid. If TXMFPO is a logic one, then TMFPO[4:1] will be available. If TXMFPO is a logic zero, then TFPO[4:1] will be available. This bit is effective only if the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is a logic one. The TXGAPEN-bit takes precedence over the TXMFPO bit.

RXGAPEN

The RXGAPEN-bit configures the S/UNI-4xD3F to enable the RGAPCLK[x] outputs. When RXGAPEN is a logic one, then the RGAPCLK[x] output is enabled. When RXGAPEN is a logic zero, then the RSCLK[x] output is enabled. The FRMRONLY register bit must be a logic one for RXGAPEN to have effect.

TXGAPEN

The TXGAPEN-bit configures the S/UNI-4xD3F to enable the TGAPCLK[x] outputs. When TXGAPEN is a logic one, the TGAPCLK[x] output is enabled. When TXGAPEN is a logic zero, then either the TFPO[x] or TMFPO[x] output is enabled, depending on the setting of the TXMFPO register bit. The FRMRONLY register bit must be a logic one for TXGAPEN to have effect.

TXMFPI

The TXMFPI bit controls which of the inputs TMFPI[4:1] or TFPI[4:1] is valid. If TXMFPI is a logic one, then TMFPI[4:1] will be expected. If TXMFPI is a logic zero, then TFPI[4:1] will be expected. This bit is effective only if the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is a logic one.

STATSEL[2:0]

The STATSEL[2:0] bits are used to select the function of the FRMSTAT[4:1] output. The selection is shown in Table 5:

Table 5 STATSEL[2:0] Options

STATSEL[2:0]	FRMSTAT output pin indication function
000	E3/DS3 LOF or J2 extended LOF (integration periods are selected by the LOFINT[1:0] register bits in the S/UNI-4xD3FReceive Configuration register)
010	E3/DS3 OOF or J2 LOF
100	AIS
101	LOS
110	DS3 Idle
111	Reserved

Register 002H, 102H, 202H, 302H: S/UNI-4xD3F Transmit Configuration

Bit	Type	Function	Default
Bit 7	R/W	TFRM[1]	0
Bit 6	R/W	TFRM[0]	0
Bit 5	R/W	TXREF	0
Bit 4	R/W	TICLK	0
Bit 3	R/W	TUNI	0
Bit 2	R/W	TCLKINV	0
Bit 1	R/W	TPOSINV	0
Bit 0	R/W	TNEGINV	0

TNEGINV

The TNEGINV bit provides polarity control for outputs TNEG/TOHM. When a logic zero is written to TNEGINV, the TNEG/TOHM output is not inverted. When a logic one is written to TNEGINV, the TNEG/TOHM output is inverted. The TNEGINV bit setting does not affect the loopback data in diagnostic loopback.

TPOSINV

The TPOSINV bit provides polarity control for outputs TPOS/TDATO. When a logic zero is written to TPOSINV, the TPOS/TDATO output is not inverted. When a logic one is written to TPOSINV, the TPOS/TDATO output is inverted. The TPOSINV bit setting does not affect the loopback data in diagnostic loopback.

TCLKINV

The TCLKINV bit provides polarity control for output TCLK. When a logic zero is written to TCLKINV, TCLK is not inverted and outputs TPOS/TDATO and TNEG/TOHM are updated on the falling edge of TCLK. When a logic one is written to TCLKINV, TCLK is inverted and outputs TPOS/TDATO and TNEG/TOHM are updated on the rising edge of TCLK.

TUNI

The TUNI bit enables the S/UNI-4xD3F to transmit unipolar or bipolar DS3, E3, or J2 data streams. When a logic one is written to TUNI, the S/UNI-4xD3Ftransmits unipolar DS3, E3, or J2 data on TDATO. When TUNI is logic one, the TOHM output indicates the start of the DS3 M-Frame (the X1 bit), the start of the E3 frame (bit 1 of the frame), or the first framing bit of the J2 multiframe. When a logic zero is written to TUNI, the S/UNI-4xD3Ftransmits B3ZS-encoded DS3 data, HDB3-encoded E3 data, or B8ZS-encoded J2 data on TPOS and TNEG. The TUNI bit has no effect if TFRM[1:0] is set to 11 binary as the output data is automatically configured for unipolar format.

TICLK

The TICLK bit selects the transmit clock used to update the TPOS/TDATO and TNEG/TOHM outputs. When a logic zero is written to TICLK, the buffered version of the input transmit clock, TCLK, is used to update TPOS/TDATO and TNEG/TOHM on the edge selected by the TCLKINV bit. When a logic one is written to TICLK, TPOS/TDATO and TNEG/TOHM are updated on the rising edge of TICLK, eliminating the flow-through TCLK signal. The TICLK bit has no effect if the LOOPT, LLOOP, or PLOOP bit is a logic one.

TXREF

The TXREF register bit determines if TICLK[1] and TIOHM/TFPI/TMFPI[1] should be used as the reference transmit clock and overhead/frame pulse, respectively, instead of TICLK[X] and TIOHM/TFPI/TMFPI[X]. If TXREF is set to a logic one, then TICLK[1] and TIOHM/TFPI/TMFPI[1] will be used as the reference transmit clock and overhead/frame pulse, respectively. If TXREF is set to a logic zero, then TICLK[X] and TIOHM/TFPI/TMFPI[X] will be used as the reference transmit clock and overhead/frame pulse, respectively, for quadrant X. If loop-timing is enabled (LOOPT = 1), the TXREF-bit has no effect on the corresponding quadrant. Note: When TXREF is set to logic one, the unused TICLK[x] and TIOHM/TFPI/TMFPI[x] should be tied to power or ground, not left floating.

TFRM[1:0]

The TFRM[1:0] bits determine the frame structure of the transmitted signal. Refer to Table 6:

Table 6 TFRM[1:0] Transmit Frame Structure Configurations

TFRM[1:0]	Transmit Frame Structure
00	DS3 (C-bit parity or M23 depending on the setting of the CBIT bit in the DS3 TRAN Configuration register)
01	E3 (G.751 or G.832 depending on the setting of the FORMAT[1:0] bits in the E3 TRAN Framing Options register)
10	J2 (G.704 and NTT compliant framing format)
11	DS1/E1/Arbitrary framing format - If the EXT bit in the SPLT Configuration register is a logic zero, then DS1 or E1 direct-mapped. If EXT is a logic one, then the arbitrary framing format is selected and overhead positions are indicated by the TIOHM[x] input pin.

Register 003H, 103H, 203H, 303H: S/UNI-4xD3F Receive Configuration

Bit	Type	Function	Default
Bit 7	R/W	RFRM[1]	0
Bit 6	R/W	RFRM[0]	0
Bit 5	R/W	LOFINT[1]	0
Bit 4	R/W	LOFINT[0]	0
Bit 3	R/W	RSCLKR	0
Bit 2	R/W	RCLKINV	0
Bit 1	R/W	RPOSINV	0
Bit 0	R/W	RNEGINV	0

RNEGINV

The RNEGINV bit provides polarity control for input RNEG/RLCV/ROHM. When a logic zero is written to RNEGINV, the input RNEG/RLCV/ROHM is not inverted. When a logic one is written to RNEGINV, the input RNEG/RLCV/ROHM is inverted. The RNEGINV bit setting does not affect the loopback data in diagnostic loopback.

RPOSINV

The RPOSINV bit provides polarity control for input RPOS/RDATI. When a logic zero is written to RPOSINV , the input RPOS/RDATI is not inverted. When a logic one is written to RPOSINV , the input RPOS/RDATI is inverted. The RPOSINV bit setting does not affect the loopback data in diagnostic loopback.

RCLKINV

The RCLKINV bit provides polarity control for input RCLK. When a logic zero is written to RCLKINV, RCLK is not inverted and inputs RPOS/RDATI and RNEG/RLCV/ROHM are sampled on the rising edge of RCLK. When a logic one is written to RCLKINV, RCLK is inverted and inputs RPOS/RDATI and RNEG/RLCV/ROHM are sampled on the falling edge of RCLK.

RSCLKR

The RSCLKR bit is in effect only when the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is set to logic one. When RSCLKR is a logic one, the RDATO, RFPO/RMFPO, and ROVRHD outputs are updated on the rising edge of RSCLK. When RSCLKR is a logic zero, the RDATO, RFPO/RMFPO, and ROVRHD outputs are updated on the falling edge of RSCLK. If the RXGAPEN-bit is a logic one, then RSCLKR affects RGAPCLK in the same manner as it affects RSCLK.

LOFINT[1:0]

The LOFINT[1:0] bits determine the integration period used for asserting and de-asserting E3 and DS3 LOF or J2 extended LOF on the FRMLOF register bit of the S/UNI-4xD3FFRMR LOF Status register (x9CH) and on the FRMSTAT[4:1] output pins (if this function is enabled by the STATSEL[2:0] register bits of the S/UNI-4xD3F Configuration 2 register). The integration times are selected as shown in Table 7:

Table 7 LOF[1:0] Integration Period Configuration

LOFINT[1:0]	Integration Period
00	3 ms
01	2 ms
10	1 ms
11	Reserved

RFRM[1:0]

The RFRM[1:0] bits determine the expected frame structure of the received signal. Refer to Table 8:

Table 8 RFRM[1:0] Receive Frame Structure Configurations

RFRM[1:0]	Expected Receive Frame Structure
00	DS3 (C-bit parity or M23 depending on the setting of the CBE bit in the DS3 FRMR Configuration register)
01	E3 (G.751 or G.832 depending on the setting of the FORMAT[1:0] bits in the E3 FRMR Framing Options register)
10	J2 (G.704 and NTT compliant framing format)
11	DS1/E1/Arbitrary framing format (When EXT in the SPLR Configuration register is a logic zero, then DS1 or E1 direct-mapped. When EXT is a logic one, then the arbitrary framing format is selected and overhead bit positions are indicated by the ROHM[x] input pin.)

Register 004H, 104H, 204H, 304H: Data Link and FERF/RAI Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	AISEN	1
Bit 5	R/W	RBLEN	1
Bit 4	R/W	OOFEN	1
Bit 3	R/W	LOSEN	1
Bit 2	R/W	TNETOP	0
Bit 1	R/W	RNETOP	0
Bit 0	R/W	DLINV	0

DLINV

The DLINV bit provides polarity control for the DS3 C-bit Parity PMDL, which is located in the three C-bits of M-subframe 5. When a logic one is written to DLINV, the PMDL is inverted before being processed. The rationale behind this bit is to safe-guard the S/UNI-4xD3Fin case the inversion is required in the future. Currently, the ANSI standard T1.107 specifies that the C-bits, which carry the PMDL, be set to all-zeros while the AIS maintenance signal is transmitted. The data link is obviously inactive during AIS transmission, and ideally the HDLC idle sequence (all-ones) should be transmitted. By inverting the data link, the all-zeros C-bit pattern becomes an idle sequence and the data link is terminated gracefully.

RNETOP

The RNETOP bit enables the Network Operator Byte (NR) extracted from the G.832 E3 stream to be terminated by the internal HDLC receiver, RDLC. When RNETOP is logic one, the NR byte is extracted from the G.832 stream and terminated by RDLC. When RNETOP is logic zero, the GC byte is extracted from the G.832 stream and terminated by RDLC. Both the NR byte and the GC byte are extracted and output on the ROH pin for external processing.

TNETOP

The TNETOP bit enables the Network Operator Byte (NR) inserted in the G.832 E3 stream to be sourced by the internal HDLC transmitter, TDPR. When TNETOP is logic one, the NR byte is inserted into the G.832 stream through the TDPR block; the GC byte of the G.832 E3 stream is sourced by through the TOH[x] and TOHINS[x] pins. If TOH[x] and TOHINS[x] are not active, then an all-ones signal will be inserted into the GC byte. When TNETOP is logic zero, the GC byte is inserted into the G.832 stream through the TDPR block; the NR byte of the G.832 E3 stream is sourced by the TOH[x] and TOHINS[x] pins. If TOH[x] and TOHINS[x] are not active, then an all-ones signal will be inserted into the NR byte.

For G.751 E3 streams, the National Use bit is sourced by the TDPR block if TNETOP and the NATUSE bit (from the E3 TRAN Configuration register x41H) are both logic zero. If either TNETOP or NATUSE is logic one, the National Use bit will be sourced from the NATUSE register bit in register x41H.

If the S/UNI-4xD3F is configured for DS3 or J2 operation, TNETOP has no effect. The DS3 C-bit Parity and J2 datalink is inserted into the DS3 or J2 stream through the internal HDLC transmitter TDPR.

The TOH[x] and TOHINS[x] input pins can be used to overwrite the values of these overhead bits in the transmit stream.

LOSEN

The LOSEN-bit enables the receive LOS indication to automatically generate a FERF indication in the transmit stream. This bit operates regardless of framer selected (DS3, E3, or J2). When LOSEN is logic one, assertion of the LOS indication by the framer causes a FERF (RAI in G.751 or J2 mode) to be transmitted by TRAN for the duration of the LOS assertion. When LOSEN is logic zero, assertion of the LOS indication does not cause transmission of a FERF/RAI.

Note: For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register must all be set to logic one. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic zero.

OOFEN

The OOFEN-bit enables the receive OOF indication to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the transmit stream. This bit operates when the E3 or J2 framer is selected or when the DS3 framer is selected and the RBLEN-bit is logic zero. When OOFEN is logic one, assertion of the OOF indication by the framer causes a FERF/RAI to be transmitted by TRAN for the duration of the OOF assertion. When OOFEN is logic zero, assertion of the OOF indication does not cause transmission of a FERF/RAI.

Note: For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register must all be set to logic one. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic zero.

RBLEN

The RBLEN-bit enables: the receive RED alarm (persistent OOF) indication to automatically generate a FERF indication in the DS3 transmit stream, or a BIP8 error detection in the E3 G.832 Framer to generate a FEBE indication in the E3 G.832 transmit stream, or an LOF to generate a RLOF indication (A-bit) in the J2 transmit stream. When the E3 G.751 framer is selected, this bit has no effect.

When RBLEN is logic one, TFRM[1:0] is 00 binary, and RFRM[1:0] is 00 binary, assertion of the RED indication by the framer causes a FERF to be transmitted by DS3_TRAN for the duration of the RED assertion. Also, for DS3 frame format, the OOFEN-bit is internally forced to logic zero when RBLEN is logic one. When RBLEN is logic zero, assertion of the RED indication does not cause transmission of a FERF.

When RBLEN is logic one, TFRM[1:0] is 01 binary, and RFRM[1:0] is 01 binary, any BIP8 error indication by the E3 G.832 framer causes a FEBE to be generated by the E3 G.832 TRAN. When RBLEN is logic zero, BIP8 errors detected by the E3 framer do not cause FEBEs to be generated by the E3_TRAN.

When RBLEN is logic one, TFRM[1:0] is 10 binary, and RFRM[1:0] is 10 binary, any LOF error indication by the J2 framer causes the RLOF-bit (also known as the A bit) to be set in the J2 transmit stream. When RBLEN is logic zero, LOF errors detected by the J2 framer do not cause the RLOF-bit to be set in the transmit stream.

AISEN

The AISEN-bit enables the RAI signal to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the transmit stream. This bit operates regardless of framer selected (DS3, E3, or J2). When AISEN is logic one, assertion of the AIS indication (physical AIS for J2) by the framer causes a FERF/RAI to be transmitted by TRAN for the duration of the AIS assertion. When AISEN is logic zero, assertion of the AIS indication does not cause transmission of a FERF/RAI.

Note: For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register must all be set to logic one. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic zero.

Reserved

The Reserved bit **must be programmed to logic zero** for proper operation.

Register 005H, 105H, 205H, 305H: S/UNI-4xD3F Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPLRI/TTBI	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	RBOCI/PRGDI	X
Bit 3	R	FRMRI/LOFI	X
Bit 2	R	PMONI	X
Bit 1	R	TDPRI	X
Bit 0	R	RDLCI	X

SPLRI/TTBI, RBOCI/PRGDI, FRMRI/LOFI, PMONI, TDPRI, RDLCI

These bits are interrupt status indicators that identify the block that is the source of a pending interrupt. The SPLRI/TTBI bit will be logic one if either the SPLR or the TTB block has produced the interrupt. The RBOCI/PRGDI bit will be logic one if either the RBOC or PRGD block has produced the interrupt. The FRMRI/LOFI will be logic one if either the FRMR (J2, E3, or T3 - whichever one is enabled) or the E3, T3, or J2 Extended LOF signal (FRMLOFI from register x9CH) is the source of the interrupt. This register is typically used by interrupt service routines to determine the source of a S/UNI-4xD3F interrupt.

Register 006H: S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[3]	1
Bit 5	R	TYPE[2]	0
Bit 4	R	TYPE[1]	0
Bit 3	R	TYPE[0]	0
Bit 2	R	Reserved	X
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	0

This register is used for global performance monitor updates, global software resets, and for device identification. Writing any value except 80H into this register initiates latching of all performance monitor counts in the PMON block in all four quadrants of the S/UNI-4xD3F. The TIP register bit is used to signal when the latching is complete.

RESET

The RESET bit allows software to asynchronously reset the S/UNI-4xD3F. The software reset is equivalent to setting the RSTB input pin low, except that the S/UNI-4xD3FMaster Test register is not affected. When a logic one is written to RESET, the S/UNI-4xD3F is reset. When a logic zero is written to RESET, the reset is removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

TYPE[3:0]

The TYPE[3:0] bits allow software to identify this device as the S/UNI-4xD3Fmember of the S/UNI family of products.

Reserved

The reserved bit must be a not connect.

ID[1:0]

The ID[1:0] bits allows software to identify the version level of the S/UNI-4xD3F.

Register 007H, 107H, 207H, 307H: S/UNI-4xD3F Clock Activity Monitor and Interrupt Identification

Bit	Type	Function	Default
Bit 7	R	INT[4]	X
Bit 6	R	INT[3]	X
Bit 5	R	INT[2]	X
Bit 4	R	INT[1]	X
Bit 3	R	RCLKA	X
Bit 2	R	TICLKA	X
Bit 1		Unused	X
Bit 0		Unused	X

TICLKA

The TICLKA bit monitors for low-to-high transitions on the TICLK[x] input. TICLKA is set low when this register is read and is set high on a rising edge of TICLK[x].

RCLKA

The RCLKA bit monitors for low-to-high transitions on the RCLK[x] input. RCLKA is set low when this register is read and is set high on a rising edge of RCLK[x].

INT[4:1]

The INT[4:1] bits identify which of the four quadrants of the S/UNI-4xD3Fhave generated the current interrupt. When the INT[x] bit is set to logic one, then the Xth quadrant has generated the interrupt. The particular block(s) within that quadrant that generated the interrupt can be identified by reading the corresponding quadrant's S/UNI-4xD3F Interrupt Status register. When the INT[x] bit is set to logic zero, then the X^{th} quadrant has not generated an interrupt. Note: The INT[4:1] bits are valid only in register address 007H.

Register 010H, 110H, 210H, 310H: Change of PMON Performance Meters

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	LCVCH	X
Bit 4	R	FERRCH	X
Bit 3	R	EXZS	X
Bit 2	R	PERRCH	X
Bit 1	R	CPERRCH	X
Bit 0	R	FEBECH	X

FEBECH

The FEBECH bit is set to logic one if one or more FEBE events (or J2 EXZS events when the J2 framing format is selected) have occurred during the latest PMON accumulation interval.

CPERRCH

The CPERRCH bit is set to logic one if one or more path parity error events have occurred during the latest PMON accumulation interval.

PERRCH

The PERRCH bit is set to logic one if one or more parity error events (or J2 CRC-5 errors) have occurred during the latest PMON accumulation interval.

EXZS

The EXZS bit is set to logic one if one or more summed LCV events in DS3 mode have occurred during the latest PMON accumulation interval.

FERRCH

The FERRCH bit is set to logic one if one or more F-bit or M-bit error events have occurred during the latest PMON accumulation interval.

LCVCH

The LCVCH bit is set to logic one if one or more LCV events have occurred during the latest PMON accumulation interval.

Register 011H, 111H, 211H, 311H: PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	X
Bit 0	R	OVR	X

OVR

The OVR bit indicates the overrun status of the PMON holding registers. A logic one in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic zero indicates that no overrun has occurred. This bit is reset to logic zero when this register is read.

INTR

The INTR bit indicates the current status of the interrupt signal. A logic one in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic zero indicates that no transfer has occurred. The INTR bit is set to logic zero when this register is read.

INTE

The INTE bit enables the generation of an interrupt when the PMON counter values are transferred to the holding registers. When a logic one is written to INTE, the interrupt generation is enabled.

Register 014H, 114H, 214H, 314H: PMON LCV Event Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 015H, 115H, 215H, 315H: PMON LCV Event Count MSB

Bit	Type	Function	Default
Bit 7	R	LCV[15]	X
Bit 6	R	LCV[14]	X
Bit 5	R	LCV[13]	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

LCV[15:0]

LCV[15:0] represents the number of DS3, E3, or J2 LCV errors that have been detected since the last time the LCV counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the LCV Error Count registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes three RCLK[x] cycles to complete.

Register 016H, 116H, 216H, 316H: PMON Framing Bit Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

Register 017H, 117H, 217H, 317H: PMON Framing Bit Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FERR[9]	X
Bit 0	R	FERR[8]	X

FERR[9:0]

FERR[9:0] represents the number of DS3 F-bit and M-bit errors, or E3 or J2 framing pattern errors, that have been detected since the last time the framing error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the FERR Error Event Count registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK[x] cycles to complete in DS3 mode and three RCLK[x] cycles to complete in E3 and J2 mode.

This counter is paused when the corresponding framer has lost frame alignment.

Register 018H, 118H, 218H, 318H: PMON EXZS Count LSB

Bit	Type	Function	Default
Bit 7	R	EXZS[7]	X
Bit 6	R	EXZS[6]	X
Bit 5	R	EXZS[5]	X
Bit 4	R	EXZS[4]	X
Bit 3	R	EXZS[3]	X
Bit 2	R	EXZS[2]	X
Bit 1	R	EXZS[1]	X
Bit 0	R	EXZS[0]	X

Register 019H, 119H, 219H, 319H: PMON EXZS Count MSB

Bit	Type	Function	Default
Bit 7	R	EXZS[15]	X
Bit 6	R	EXZS[14]	X
Bit 5	R	EXZS[13]	X
Bit 4	R	EXZS[12]	X
Bit 3	R	EXZS[11]	X
Bit 2	R	EXZS[10]	X
Bit 1	R	EXZS[9]	X
Bit 0	R	EXZS[8]	X

EXZS[15:0]

In DS3 mode, EXZS[15:0] represents the number of summed Excessive Zeros (EXZS) that occurred during the previous accumulation interval. One or more excessive zeros occurrences within an 85 bit DS3 information block is counted as one summed excessive zero. Excessive zeros are accumulated by this register only when the EXZSO and EXZDET are logic one in the DS3 FRMR Additional Configuration register. This register accumulates summed LCVs when the EXZSO is logic zero. The count of summed LCVs is defined as the number of DS3 information blocks (85 bits) that contain one or more LCVs since the last time the summed LCV counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the EXZS Event Count registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK[x] cycles to complete in DS3 mode and a maximum of 500 RCLK[x] cycles to complete in G.832 E3 mode.

Register 01AH, 11AH, 21AH, 31AH: PMON Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Register 01BH, 11BH, 21BH, 31BH: PMON Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7	R	PERR[15]	X
Bit 6	R	PERR[14]	X
Bit 5	R	PERR[13]	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[15:0]

PERR[15:0] represents the number of DS3 P-bit errors, the number of E3 G.832 BIP-8 errors or the number of J2 CRC-5 errors that have been detected since the last time the parity error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the PERR Error Count registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK[x] cycles to complete in DS3 mode and three RCLK[x] cycles to complete in E3 and J2 mode.

This counter is paused when the corresponding framer has lost frame alignment.

Register 01CH, 11CH, 21CH, 31CH: PMON Path Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	CPERR[7]	X
Bit 6	R	CPERR[6]	X
Bit 5	R	CPERR[5]	X
Bit 4	R	CPERR[4]	X
Bit 3	R	CPERR[3]	X
Bit 2	R	CPERR[2]	X
Bit 1	R	CPERR[1]	X
Bit 0	R	CPERR[0]	X

Register 01DH, 11DH, 21DH, 31DH: PMON Path Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	CPERR[13]	X
Bit 4	R	CPERR[12]	X
Bit 3	R	CPERR[11]	X
Bit 2	R	CPERR[10]	X
Bit 1	R	CPERR[9]	X
Bit 0	R	CPERR[8]	X

CPERR[13:0]

When configured for DS3 applications, CPERR[13:0] represents the number of DS3 path parity errors that have been detected since the last time the DS3 path parity error counter was polled.

This counter is forced to zero when the S/UNI-4xD3F is configured for either J2 and E3 applications.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the CPERR Error Count registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK[x] cycles to complete.

This counter is paused when the corresponding framer has lost frame alignment.

Register 01EH, 11EH, 21EH, 31EH: PMON FEBE/J2-EXZS Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE/J2-EXZS[7]	X
Bit 6	R	FEBE/J2-EXZS[6]	X
Bit 5	R	FEBE/J2-EXZS[5]	X
Bit 4	R	FEBE/J2-EXZS[4]	X
Bit 3	R	FEBE/J2-EXZS[3]	X
Bit 2	R	FEBE/J2-EXZS[2]	X
Bit 1	R	FEBE/J2-EXZS[1]	X
Bit 0	R	FEBE/J2-EXZS[0]	X

Register 01FH, 11FH, 21FH, 31FH: PMON FEBE/J2-EXZS Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	FEBE/J2-EXZS[13]	X
Bit 4	R	FEBE/J2-EXZS[12]	X
Bit 3	R	FEBE/J2-EXZS[11]	X
Bit 2	R	FEBE/J2-EXZS[10]	X
Bit 1	R	FEBE/J2-EXZS[9]	X
Bit 0	R	FEBE/J2-EXZS[8]	X

FEBE/J2-EXZS[13:0]

FEBE/J2-EXZS[13:0] represents the number of DS3 or E3 G.832 FEBEs that have been detected since the last time the FEBE error counter was polled.

In J2 mode, FEBE/J2-EXZS[13:0] represents the number of Excessive Zeros (EXZS is a string of eight or more consecutive zeros) that have occurred during the previous accumulation interval.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (x14H to x1FH) or to the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update register (006H). Such a write transfers the internally accumulated count to the FEBE Event Count registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK[x] cycles to complete in DS3 mode and three RCLK[x] cycles to complete in E3 and J2 mode.

Register 030H, 130H, 230H, 330H: DS3 FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	AISPAT	1
Bit 6	R/W	FDET	0
Bit 5	R/W	MBDIS	0
Bit 4	R/W	M3O8	0
Bit 3	R/W	UNI	0
Bit 2	R/W	REFR	0
Bit 1	R/W	AISC	0
Bit 0	R/W	CBE	0

CBE

The CBE bit enables the DS3 C-bit parity application. When a logic one is written to CBE, C-bit parity mode is enabled. When a logic zero is written to CBE, the DS3 M23 format is selected. While the C-bit parity application is enabled, C-bit parity error events, FEBEs are accumulated.

AISC

The AISC bit controls the algorithm used to detect the AIS. When a logic one is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic zero is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic zero is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits. (Refer to the bit mapping table in the Additional Configuration register description.)

REFR

The REFR bit initiates a DS3 reframe. When a logic one is written to REFR, the S/UNI-4xD3F is forced OOF, and a new search for frame alignment is initiated. Note: Only a low-to-high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

UNI

The UNI bit configures the S/UNI-4xD3F to accept either dual-rail or single-rail receive DS3 streams. When a logic one is written to UNI, the S/UNI-4xD3F accepts a single-rail DS3 stream on RDATI. The S/UNI-4xD3F accumulates LCVs on the RLCV input. When a logic zero is written to UNI, the S/UNI-4xD3F accepts B3ZS-encoded dual-rail data on RPOS and RNEG.

M3O8

The M3O8 bit controls the DS3 OOF decision criteria. When a logic one is written to M3O8, DS3 OOF is declared when three of eight framing bits (F-bits) are in error. When a logic zero is written to M3O8, the three of 16 framing bits in error criteria is used, as recommended in ANSI T1.107

MBDIS

The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic one, M-bit errors are disabled from causing an OOF; the LOF criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is set to logic zero, errors in either M-bits or F-bits are enabled to cause an OOF. When MBDIS is logic zero, an OOF can occur when one or more M-bit errors occur in three out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit is exceeded.

FDET

The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic one, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic zero, the detection time is 13.5 ms.

AISPAT

The AISPAT bit controls the pattern used to detect the AIS. When a logic one is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010.. is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic zero is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration register description).

Register 031H, 131H, 231H, 331H: DS3 FRMR Interrupt Enable (ACE=0)

Bit	Type	Function	Default
Bit 7	R/W	COFAE	0
Bit 6	R/W	REDE	0
Bit 5	R/W	CBITE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	IDLE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	LOSE	0

LOSE

The LOSE bit enables interrupt generation when a DS3 LOS defect is declared or removed. The interrupt is enabled when a logic one is written.

OOFE

The OOFE bit enables interrupt generation when a DS3 OOF defect is declared or removed. The interrupt is enabled when a logic one is written.

AISE

The AISE bit enables interrupt generation when the DS3 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic one is written.

IDLE

The IDLE bit enables interrupt generation when the DS3 IDLE maintenance signal is detected or removed. The interrupt is enabled when a logic one is written.

FERFE

The FERFE bit enables interrupt generation when a DS3 FERF defect is declared or removed. The interrupt is enabled when a logic one is written.

CBITE

The CBITE bit enables interrupt generation when the S/UNI-4xD3F detects a change of state in the DS3 application identification channel. The interrupt is enabled when a logic one is written.

REDE

The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When REDE is set to logic one, the interrupt output, INTB, is set low when the state of the RED indication changes.

COFAE

The COFAE bit enables interrupt generation when the S/UNI-4xD3F detects a DS3 change of frame alignment. The interrupt is enabled when a logic one is written.

Register 031H, 131H, 231H, 331H: DS3 FRMR Additional Configuration Register (ACE=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	AISONES	0
Bit 4	R/W	BPVO	0
Bit 3	R/W	EXZSO	0
Bit 2	R/W	EXZDET	0
Bit 1	R/W	SALGO	0
Bit 0	R/W	DALGO	0

DALGO

The DALGO bit determines the criteria used to decode a valid B3ZS signature. When DALGO is set to logic one, a valid B3ZS signature is declared and three zeros substituted whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen. When the DALGO bit is set to logic zero, a valid B3ZS signature is declared and the three zeros are substituted whenever a zero followed by a bipolar violation is observed.

SALGO

The SALGO bit determines the criteria used to establish a valid B3ZS signature used to map BPVs to LCV indications. Any BPV that is not part of a valid B3ZS signature is indicated as an LCV. When the SALGO bit is set to logic one, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation is observed. When SALGO is set to logic zero, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen.

EXZDET

The EXZDET bit determines the type of zero occurrences to be included in the LCV indication. When EXZDET is set to logic one, the occurrence of an excessive zero generates a single pulse indication that is used to indicate an LCV. When EXZDET is set to logic zero, every occurrence of three consecutive zeros generates a pulse indication that is used to indicate an LCV. For example, if a sequence of 15 consecutive zeros were received, with EXZDET=1 only a single LCV would be indicated for this string of excessive zeros; with EXZDET=0, five LCVs would be indicated for this string (i.e. one LCV for every three consecutive zeros). Refer to Table 9.

EXZSO

The EXZSO bit enables only summed zero occurrences to be accumulated in the PMON EXZS Count registers. When EXZSO is set to logic one, any excessive zeros occurrences over an 85 bit period increments the PMON EXZS counter by one. When EXZSO is set to logic zero, summed LCVs are accumulated in the PMON EXZS Count registers. A summed LCV is defined as the occurrence of either BPVs not part of a valid B3ZS signature or three consecutive zeros (or excessive zeros if EXZDET=1) occurring over an 85 bit period; each summed LCV occurrence increment the PMON EXZS counter by one. Refer to Table 9.

BPVO

The BPVO bit enables only bipolar violations to indicate LCVs and be accumulated in the PMON LCV Count registers. When BPVO is set to logic one, only BPVs not part of a valid B3ZS signature generate an LCV indication and increment the PMON LCV counter. When BPVO is set to logic zero, both BPVs not part of a valid B3ZS signature, and either three consecutive zeros or excessive zeros generate an LCV indication and increment the PMON LCV counter. Refer to Table 9.

Table 9 DS3 FRMR EXZS/LCV Count Configurations

Register Bit			Counter Function	
EXZSO	BPVO	EXZDET	PMON EXZ Count	PMON LCV Count
0	0	0	Summed LCVs	BPVs & every 3 consecutive zeros
0	0	1	Summed LCVs	BPVs & every string of 3+ consecutive zeros
0	1	0	Reserved	Reserved
0	1	1	Reserved	Reserved
1	0	0	Summed excessive zeros	BPVs & every 3 consecutive zeros
1	0	1	Summed excessive zeros	BPVs & every string of 3+ consecutive zeros
1	1	0	Summed excessive zeros	Only BPVs
1	1	1	Summed excessive zeros	Only BPVs

AISONES

The AISONES bit controls the pattern used to detect the AIS when both AISPAT and AISC bits in DS3 FRMR Configuration register are logic zero; if either AISPAT or AISC are logic one, the AISONES bit is ignored. When a logic zero is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111..) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored. When a logic one is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111..) signal is observed for a period of time before declaring AIS. In this case all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized in Table 10:

Table 10 DS3 FRMR AIS Configurations

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010… pattern; overhead bits ignored.
0	1	X	Framed DS3 stream containing C-bits all logic zero; payload bits ignored.
1	1	X	Framed DS3 stream containing repeating 1010… pattern in the payload, C-bits all logic zero, and X-bits=1. This can be detected by setting both AISPAT and AISC high, and declaring AIS only when AISV=1 and FERFV=0 (register x33H).
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

Register 032H, 132H, 232H, 332H: DS3 FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	X
Bit 6	R	REDI	X
Bit 5	R	CBITI	X
Bit 4	R	FERFI	X
Bit 3	R	IDLI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0	R	LOSI	X

LOSI

The LOSI bit is set to logic one when a LOS defect is detected or removed. The LOSI bit position is set to logic zero when this register is read.

OOFI

The OOFI bit is set to logic one when an OOF defect is detected or removed. The OOFI bit position is set to logic zero when this register is read.

AISI

The AISI bit is set to logic one when the DS3 AIS maintenance signal is detected or removed. The AISI bit position is set to logic zero when this register is read.

IDLI

The IDLI bit is set to logic one when the DS3 IDLE maintenance signal is detected or removed. The IDLI bit position is set to logic zero when this register is read.

FERFI

The FERFI bit is set to logic one when a FERF defect is detected or removed. The FERFI bit position is set to logic zero when this register is read.

CBITI

The CBITI bit is set to logic one when a change of state is detected in the DS3 application identification channel. The CBITI bit position is set to logic zero when this register is read.

REDI

The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When the REDI bit is a logic one, a change in the RED state has occurred. When the REDI bit is logic zero, no change in the RED state has occurred.

COFAI

The COFAI bit is set to logic one when a change of frame alignment is detected. A COFA is generated when a new DS3 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic zero when this register is read.

Register 033H, 133H, 233H, 333H: DS3 FRMR Status

Bit	Type	Function	Default
Bit 7	R/W	ACE	0
Bit 6	R	REDV	X
Bit 5	R	CBITV	X
Bit 4	R	FERFV	X
Bit 3	R	IDLV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0	R	LOSV	X

LOSV

The LOSV bit indicates the current LOS defect state. LOSV is a logic one when a sequence of 175 zeros is detected on the B3ZS encoded DS3 receive stream. LOSV is a logic zero when a signal with a ones density greater than 33% for 175 ± 1 bit periods is detected.

OOFV

The OOFV bit indicates the current DS3 OOF defect state. When the S/UNI-4xD3F has lost frame alignment and is searching for the new alignment, OOFV is set to logic one. When the S/UNI-4xD3F has found frame alignment, the OOFV bit is set to logic zero.

AISV

The AISV bit indicates the AIS state. When the S/UNI-4xD3F detects the AIS maintenance signal, AISV is set to logic one.

IDLV

The IDLV bit indicates the IDLE signal state. When the S/UNI-4xD3F detects the IDLE maintenance signal, IDLV is set to logic one.

FERFV

The FERFV bit indicates the current FERF defect state. When the S/UNI-4xD3F detects an M-frame with the X1 and X2 bits both set to zero, FERFV is set to logic one. When the S/UNI-4xD3F detects an M-frame with the X1 and X2 bits both set to one, FERFV is set to logic zero.

CBITV

The CBITV bit indicates the application identification channel (AIC) state. CBITV is set to logic one (indicating the presence of the C-bit parity application) when the AIC bit is set high for 63 consecutive M-frames. CBITV is set to logic zero (indicating the presence of the M23 or SYNTRAN applications) when AIC is set low for 2 or more M-frames in the last 15.

REDV

The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic one, the DS3 FRMR frame alignment acquisition circuitry has been OOF for 2.23 ms (or for 13.5 ms when FDET is logic zero). When the REDV bit is logic zero, the frame alignment circuitry has found frame (i.e. OOFV=0) for 2.23 ms (or 13.5 ms if FDET=0).

ACE

The ACE bit selects the Additional Configuration register. This register is located at address x31H, and is only accessible when the ACE bit is set to logic one. When ACE is set to logic zero, the Interrupt Enable register is accessible at address x31H.

Register 034H, 134H, 234H, 334H: DS3 TRAN Configuration

Bit	Type	Function	Default
Bit 7	R/W	CBTRAN	0
Bit 6	R/W	AIS	0
Bit 5	R/W	IDL	0
Bit 4	R/W	FERF	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	CBIT	0

CBIT

The CBIT bit enables the DS3 C-bit parity application. When CBIT is written with a logic one, C-bit parity is enabled, and the S/UNI-4xD3F modifies the C-bits as required to include the PMDL, the FEAC channel, the FEBE indication, and the path parity. When CBIT is written with a logic zero, the M23 application is selected, and each C-bit is set to logic one by the S/UNI-4xD3F except for the first C-bit of the frame, which is forced to toggle every frame. Note: The C-bits may be modified as required using the DS3 overhead access port (TOH) regardless of the setting of this bit.

FERF

The FERF-bit enables insertion of the FERF maintenance signal in the DS3 stream. When FERF is written with a logic one, the X1 and X2 overhead bit positions are set to logic zero. When FERF is written with a logic zero, the X1 and X2 overhead bit positions in the DS3 stream are set to logic one.

IDL

The IDL bit enables insertion of the idle maintenance signal in the DS3 stream. When IDL is written with a logic one, the DS3 payload is overwritten with the repeating pattern 1100.. The DS3 overhead bit insertion (X, P, M F, and C) continues normally. When IDL is written with a logic zero, the idle signal is not inserted.

AIS

The AIS bit enables insertion of the AIS maintenance signal in the DS3 stream. When AIS is written with a logic one, the DS3 payload is overwritten with the repeating pattern 1010.. The DS3 overhead bit insertion (X, P, M and F) continues normally. The values inserted in the C-bits during AIS transmission are controlled by the CBTRAN-bit in this register. When AIS is written with a logic zero, the AIS signal is not inserted.

CBTRAN

The CBTRAN-bit controls the C-bit values during AIS transmission. When CBTRAN is written with a logic zero, the C-bits are overwritten with zeros during AIS transmission as specified in ANSI T1.107. When CBTRAN is written with a logic one, C-bit insertion continues normally (as controlled by the CBIT bit in this register) during AIS transmission.

Reserved

The reserved bit must be programmed to logic zero for proper operation.

Register 035H, 135H, 235H, 335H: DS3 TRAN Diagnostic

Bit	Type	Function	Default
Bit 7	R/W	DLOS	0
Bit 6	R/W	DLCV	0
Bit 5		Unused	X
Bit 4	R/W	DFERR	0
Bit 3	R/W	DMERR	0
Bit 2	R/W	DCPERR	0
Bit 1	R/W	DPERR	0
Bit 0	R/W	DFEBE	0

DFEBE

The DFEBE bit controls the insertion of FEBEs in the DS3 stream. When DFEBE is written with a logic one, and the C-bit parity application is enabled, the three C-bits in M-subframe four are set to a logic zero. When DFEBE is written with a logic zero, FEBEs are indicated based on receive framing bit errors and path parity errors.

DPERR

The DPERR bit controls the insertion of parity errors (P-bit errors) in the DS3 stream. When DPERR is written with a logic one, the P-bits are inverted before insertion. When DPERR is written with a logic zero, the parity is calculated and inserted normally.

DCPERR

The DCPERR bit controls the insertion of path parity errors in the DS3 stream. When DCPERR is written with a logic one and the C-bit parity application is enabled, the three C-bits in M-subframe 3 are inverted before insertion. When DCPERR is written with a logic zero, the path parity is calculated and inserted normally.

DMERR

The DMERR bit controls the insertion of M-bit framing errors in the DS3 stream. When DMERR is written with a logic one, the M-bits are inverted before insertion. When DMERR is written with a logic zero, the M-bits are inserted normally.

DFERR

The DFERR bit controls the insertion of F-bit framing errors in the DS3 stream. When DFERR is written with a logic one, the F-bits are inverted before insertion. When DFERR is written with a logic zero, the F-bits are inserted normally.

DLCV

The DLCV bit controls the insertion of a single LCV in the DS3 stream. When DLCV is written with a logic one, a LCV is inserted by generating an incorrect polarity of violation in the next B3ZS signature. The data being transmitted must therefore contain periods of three consecutive zeros in order for the LCV to be inserted. For example, LCVs may not be inserted when transmitting AIS, but may be inserted when transmitting the idle signal. DLCV is automatically cleared upon insertion of the LCV.

DLOS

The DLOS bit controls the insertion of LOSin the DS3 stream. When DLOS is written with a logic one, the data on outputs TPOS/TDATO and TNEG/TOHM is forced to continuous zeros.

Register 038H, 138H, 238H, 338H: E3 FRMR Framing Options

Bit	Type	Function	Default
Bit 7	Unused	X	
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	UNI	0
Bit 3	R/W	FORMAT[1]	0
Bit 2	R/W	FORMAT[0]	0
Bit 1	R/W	REFRDIS	0
Bit 0	R/W	REFR	0

REFR

A transition from logic zero to logic one in the REFR bit position forces the E3 Framer to initiate a search for frame alignment. The bit must be cleared to logic zero, then set to logic one again to initiate subsequent searches for frame alignment.

REFRDIS

The REFRDIS bit disables reframing under the consecutive framing bit error condition once frame alignment has been found, leaving reframing to be initiated only by software via the REFR bit. A logic one in the REFRDIS bit position causes the FRMR to remain “locked in frame” once initial frame alignment has been found. A logic zero allows reframing to occur when four consecutive framing patterns are received in error.

FORMAT[1:0]

The FORMAT[1:0] bits determine the framing mode used for pattern matching when finding frame alignment and for generating the output status signals. The FORMAT[1:0] bits select one of two framing formats. Refer to Table 11.

Table 11 E3 FRMR FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

UNI

The UNI bit selects the mode of the receive data interface. When UNI is logic one, the E3-FRMR expects unipolar data on the RDATI input and accepts LCV indications on the RLCV input. When UNI is logic zero, the E3-FRMR expects bipolar data on the RPOS and RNEG inputs and decodes the pulses according to the HDB3 line code.

Reserved

The Reserved bit must be programmed to logic zero for proper operation.

Register 039H, 139H, 239H, 339H: E3 FRMR Maintenance Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	WORDBIP	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	WORDERR	0
Bit 2	R/W	PYLD&JUST	0
Bit 1	R/W	FERFDET	0
Bit 0	R/W	TMARKDET	0

TMARKDET

The TMARKDET bit determines the persistency check performed on the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TMARKDET is logic one, the Timing Marker bit must be in the same state for 5 consecutive frames before the TIMEMK status is changed to that state. When TMARKDET is logic zero, the Timing Marker bit must be in the same state for three consecutive frames. When a framing mode other than G.832 is selected, the setting of the TMARKDET bit is ignored.

FERFDET

The FERFDET bit determines the persistency check performed on the FERF (FERF) bit (bit 1 of the G.832 Maintenance and Adaptation byte) or on the RAI (RAI) bit (bit 11 of the frame in G.751 mode). When FERFDET is logic one, the FERF, or RAI, bit must be in the same state for 5 consecutive frames before the FERF/RAI status is changed to that state. When FERFDET is logic zero, the FERF, or RAI, bit must be in the same state for three consecutive frames.

PYLD&JUST

The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing mode G.751 is indicated as overhead or payload. When PYLD&JUST is logic one, the justification service bits and the tributary justification bits are indicated as payload. When PYLD&JUST is logic zero, the justification service and tributary justification bits are indicated as overhead.

WORDERR

The WORDERR bit selects whether the framing bit error indication pulses accumulated in PMON indicate all bit errors in the framing pattern or only one error for one or more errors in the framing pattern. When WORDERR is logic one, the FERR indication to PMON pulses once per frame, accumulating one error for one or more framing bit errors occurred. When WORDERR is logic zero, the FERR indication to PMON pulses for each and every framing bit error that occurs; PMON accumulates all framing bit errors.

WORDBIP

The WORDBIP bit selects whether the parity bit error indication pulses to the E3-TRAN block indicate all bit errors in the BIP-8 pattern or only one error for one or more errors in the BIP-8 pattern. When WORDBIP is logic one, the parity error indication to the E3 TRAN block pulses once per frame, indicating that one or more parity bit errors occurred. When WORDBIP is logic zero, the parity error indication to the E3-TRAN block pulses for each and every parity bit error that occurs. For G.832 applications, this bit should be set to logic one.

Register 03AH, 13AH, 23AH, 33AH: E3 FRMR Framing Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CZDE	0
Bit 3	R/W	LOSE	0
Bit 2	R/W	LCVE	0
Bit 1	R/W	COFAE	0
Bit 0	R/W	OOFE	0

OOFE

The OOFE bit is an interrupt enable. When OOFE is logic one, a change of state of the OOF status generates an interrupt and sets the INTB output to logic zero. When OOFE is logic zero, changes of state of the OOF status are disabled from causing interrupts on the INTB output.

COFAE

The COFAE bit is an interrupt enable. When COFAE is logic one, a change of frame alignment generates an interrupt and sets the INTB output to logic zero. When COFAE is logic zero, changes of frame alignment are disabled from causing interrupts on the INTB output.

LCVE

The LCVE bit is an interrupt enable. When LCVE is logic one, detection of a LCV generates an interrupt and sets the INTB output to logic zero. When LCVE is logic zero, occurrences of LCVs are disabled from causing interrupts on the INTB output.

LOSE

The LOSE bit is an interrupt enable. When LOSE is logic one, a change of state of the loss-of-signal generates an interrupt and sets the INTB output to logic zero. When LOSE is logic zero, occurrences of loss-of-signal are disabled from causing interrupts on the INTB output.

CZDE

The CZDE bit is an interrupt enable. When CZDE is logic one, detection of four consecutive zeros in the HDB3-encoded stream generates an interrupt and sets the INTB output to logic zero. When CZDE is logic zero, occurrences of consecutive zeros are disabled from causing interrupts on the INTB output.

Register 03BH, 13BH, 23BH, 33BH: E3 FRMR Framing Interrupt Indication and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	CZDI	X
Bit 5	R	LOSI	X
Bit 4	R	LCVI	X
Bit 3	R	COFAI	X
Bit 2	R	OOFI	X
Bit 1	R	LOS	X
Bit 0	R	OOF	X

OOF

The OOF-bit indicates the current state of the E3-FRMR. When OOF is logic one, the E3-FRMR is OOF alignment and actively searching for the new alignment. While OOF is high all status indications and overhead extraction continue with the previous known alignment. When OOF is logic zero, the E3-FRMR has found a valid frame alignment and is operating in a maintenance mode, indicating framing bit errors, and extracting and processing overhead bits. During reset, OOF is set to logic one, but the setting may change prior to the register being read.

LOS

The LOS bit indicates the current state of the Loss-Of-Signal detector. When LOS is logic one, the E3-FRMR has received 32 consecutive RCLK cycles with no occurrences of bipolar data on RPOS and RNEG. When LOS is logic zero, the FRMR is receiving valid bipolar data. When the E3-FRMR has declared LOS, the LOS indication is set to logic zero (de-asserted) when the E3-FRMR has received 32 consecutive RCLK cycles containing no occurrences of 4 consecutive zeros. The LOS bit is forced to logic zero if the UNI bit is logic one. During reset, LOS is set to logic zero, but the setting may change prior to the register being read.

OOFI

A logic one OOFI bit indicates a change in the OOF status. The OOFI bit is cleared to logic zero upon the completion of the register read. When OOFI is logic zero, it indicates that no OOF state change has occurred since the last time this register was read.

COFAI

The COFAI bit indicates that a change of frame alignment between the previous alignment and the newly found alignment has occurred. When COFAI is logic one, the last high-to-low transition on the OOF signal resulted in the new frame alignment differing from the previous one. The COFAI bit is cleared to logic zero upon the completion of the register read. When COFAI is logic zero, it indicates that no change in frame alignment has occurred when OOF went low.

LCVI

The LCVI bit indicates that a LCV has occurred. When LCVI is logic one, a LCV on the RPOS and RNEG inputs was detected since the last time this register was read. The LCVI bit is cleared to logic zero upon the completion of the register read. When LCVI is logic zero, it indicates that no LCV was detected since the last register read. When the UNI bit in the Framing Options register is logic one, the LCVI is forced to logic zero.

LOSI

The LOSI bit indicates that a state transition occurred on the LOS status signal. When LOSI is logic one, a high-to-low or low-to-high transition occurred on the LOS status signal since the last time this register was read. The LOSI bit is cleared to logic zero upon the completion of the register read. When LOSI is logic zero, it indicates that no state change has occurred on LOS since the last time this register was read. When the UNI bit in the Framing Options register is logic one, the LOSI is forced to logic zero.

CZDI

The CZDI bit indicates that four consecutive zeros in the HDB3-encoded stream have been detected. CZDI is asserted to a logic one, whenever the CZD signal is asserted. The CZDI bit is cleared to a logic zero upon the completion of the register read. When CZDI is logic zero, it indicates that no occurrences of four consecutive zeros was detected since the last register read. When the UNI bit in the Framing Options register is logic one, the CZDI indication is forced to logic zero.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The indication bits (bits 2,3,4,5,6 of this register) are cleared to logic zero after the register is read; the INTB output is also cleared to logic one if the interrupt was generated by any of these five events.

Register 03CH, 13CH, 23CH, 33CH: E3 FRMR Maintenance Event Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	FERRE	0
Bit 6	R/W	PERRE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	FEBEE	0
Bit 2	R/W	PTYPEE	0
Bit 1	R/W	TIMEMKE	0
Bit 0	R/W	NATUSEE	0

NATUSEE

The NATUSEE bit is an interrupt enable. When NATUSEE is logic one, an interrupt is generated on the INTB output when the National Use bit (bit 12 of the frame in G.751 E3 mode) changes state. When NATUSEE is logic zero, changes in state of the National Use bit does not cause an interrupt on INTB.

TIMEMKE

The TIMEMKE bit is an interrupt enable. When TIMEMKE is logic one, an interrupt is generated on the INTB output when the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) changes state after the selected persistency check is applied. When TIMEMKE is logic zero, changes in state of the Timing Marker bit does not cause an interrupt on INTB.

PTYPEE

The PTYPEE bit is an interrupt enable. When PTYPEE is logic one, an interrupt is generated on the INTB output when the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) change state. When PTYPEE is logic zero, changes in state of the Payload Type bits does not cause an interrupt on INTB.

FEBEE

The FEBEE bit is an interrupt enable. When FEBEE is logic one, an interrupt is generated on the INTB output when the FEBE indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) changes state. When FEBEE is logic zero, changes in state of the FEBE bit does not cause an interrupt on INTB.

FERFE

The FERFE bit is an interrupt enable. When FERFE is logic one, an interrupt is generated on the INTB output when the FERF indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the RAI bit (bit 11 of the frame in G.751) changes state after the selected persistency check is applied. When FERFE is logic zero, changes in state of the FERF or RAI bit does not cause an interrupt on INTB.

AISDE

The AISDE bit is an interrupt enable. When AISDE is logic one, an interrupt is generated on the INTB output when the AISD indication changes state. When AISDE is logic zero, changes in state of the AISD signal does not cause an interrupt on INTB.

PERRE

The PERRE bit is an interrupt enable. When PERRE is logic one, an interrupt is generated on the INTB output when a BIP-8 error (in G.832 mode) is detected. When PERRE is logic zero, occurrences of BIP-8 errors do not cause an interrupt on INTB.

FERRE

The FERRE bit is an interrupt enable. When FERRE is logic one, an interrupt is generated on the INTB output when a framing bit error is detected. When FERRE is logic zero, occurrences of framing bit errors do not cause an interrupt on INTB.

Register 03DH, 13DH, 23DH, 33DH: E3 FRMR Maintenance Event Interrupt Indication

Bit	Type	FunctioIn	Defaut
Bit 7	R	FERRI	0
Bit 6	R	PERRI	0
Bit 5	R	AISDI	0
Bit 4	R	FERFI	0
Bit 3	R	FEBEI	0
Bit 2	R	PTYPEI	0
Bit 1	R	TIMEMKI	0
Bit 0	R	NATUSEI	0

NATUSEI

The NATUSEI bit is a transition Indication. When NATUSEI is logic one, a change of state of the National Use bit (bit 12 of the frame in G.751 E3 mode) has occurred. When NATUSEI is logic zero, no change of state of the National Use bit has occurred since the last time this register was read.

TIMEMKI

The TIMEMKI bit is a transition indication. When TIMEMKI is logic one, a change in state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) has occurred. When TIMEMKI is logic zero, no changes in the state of the Timing Marker bit occurred since the last time this register was read.

PTYPEI

The PTYPEI bit is a transition indication. When PTYPEI is logic one, a change of state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) has occurred. When PTYPEI is logic zero, no changes in the state of the Payload Type bits has occurred since the last time this register was read.

FEBEI

The FEBEI bit is a transition indication. When FEBEI is logic one, a change of state of the FEBE indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) has occurred. When FEBEI is logic zero, no changes in the state of the FEBE bit has occurred since the last time this register was read.

FERFI

The FERFI bit is a transition indication. When FERFI is logic one, a change of state of the FERF indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the RAI bit (bit 12 of the frame in G.751) has occurred. When FERFI is logic zero, no changes in the state of the FERF or RAI bit has occurred since the last time this register was read.

AISDI

The AISDI bit is a transition indication. When AISDI is logic one, a change in state of the AISD indication has occurred. When AISDI is logic zero, no changes in the state of the AISD signal has occurred since the last time this register was read.

PERRI

The PERRI bit is an event indication. When PERRI is logic one, the occurrence of one or more BIP-8 errors (in G.832 mode) has been detected. When PERRI is logic zero, no occurrences of BIP-8 errors have occurred since the last time this register was read.

FERRI

The FERRI bit is an event indication. When FERRI is logic one, the occurrence of one or more framing bit error has been detected. When FERRI is logic zero, no occurrences of framing bit errors have occurred since the last time this register was read.

The transition/event interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the activity of the maintenance events. The contents of this register are cleared to logic zero after the register is read; the INTB output is also cleared to logic one if the interrupt was generated by any of the Maintenance Event outputs.

Register 03EH, 13EH, 23EH, 33EH: E3 FRMR Maintenance Event Status

Bit	Type	Function	Default
Bit 7	R	AISD	X
Bit 6	R	FERF/RAI	X
Bit 5	R	FEBE	X
Bit 4	R	PTYPE[2]	X
Bit 3	R	PTYPE[1]	X
Bit 2	R	PTYPE[0]	X
Bit 1	R	TIMEMK	X
Bit 0	R	NATUSE	X

NATUSE

The NATUSE bit reflects the state of the extracted National Use bit (bit 12 of the frame in G.751 E3 mode).

TIMEMK

The TIMEMK bit reflects the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte).

PTYPE[2:0]

The PTYPE[2:0] bits reflect the state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte). These bits are not latched and should be read 2 or three times in rapid succession to ensure a coherent binary value.

FEBE

The FEBE bit reflects the state of the FEBE indication bit (bit 2 of the G.832 Maintenance and Adaptation byte).

FERF

The FERF-bit reflects the value of the FERF indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the RAI bit (bit 11 of the frame in G.751) when the value has been the same for either three or 5 consecutive frames.

AISD

The AISD bit reflects the state of the AIS detection circuitry. When AISD is logic one, less than eight zeros (in G.832 mode), or less than 5 zeros (in G.751 mode), were detected during one complete frame period while the FRMR is OOF alignment. When AISD is logic zero, eight or more zeros (in G.832 mode), or 5 or more zeros (in G.751 mode), were detected during one complete frame period, or the FRMR has found frame alignment.

Register 040H, 140H, 240H, 340H: E3 TRAN Framing Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	FORMAT[1]	0
Bit 0	R/W	FORMAT[0]	0

FORMAT[1:0]

The FORMAT[1:0] bits determine the framing mode used for framing pattern when generating the formatted output data stream. The FORMAT[1:0] bits select one of two framing formats:

Table 12 E3 TRAN FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

Reserved

The Reserved bit must be programmed to logic zero for correct operation.

Reserved

The Reserved bits must be programmed to logic zero for correct operation.

Register 041H, 141H, 241H, 341H: E3 TRAN Status and Diagnostic Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PYLD&JUST	0
Bit 5	R/W	CPERR	0
Bit 4	R/W	DFERR	0
Bit 3	R/W	DLCV	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TAIS	0
Bit 0	R/W	NATUSE	1

NATUSE

The NATUSE bit determines the default value of the National Use bit inserted into the G.751 E3 frame overhead. The value of the NATUSE bit is logically ORed with the bit collected once per frame from the internal HDLC transmitter (if TNETOP is set to logic one). When TNETOP is logic zero, the NATUSE bit controls the value of the National Use bit. When NATUSE is logic one, the National Use bit (bit 12 in G.75) is forced to logic one regardless of the bit input from the internal HDLC transmitter or the setting of TNETOP. When NATUSE is logic zero, the National Use bit is set to the value sampled from the internal HDLC transmitter if TNETOP is logic zero. Otherwise, the National Use bit will be set to logic zero. If the E3 TRAN is configured for G.832 mode, this bit is ignored.

TAIS

The TAIS bit enables AIS signal transmission. When TAIS is logic one, the all 1's AIS signal is transmitted. When TAIS is logic zero, the normal data is transmitted.

Reserved

The Reserved bit must be programmed to logic zero for proper operation.

DLCV

The DLCV bit selects whether a LCV is generated for diagnostic purposes. When DLCV changes from logic zero to logic one, single LCV is generated; in HDB3, the LCV is generated by causing a bipolar violation pulse of the same polarity to the previous bipolar violation. To generate another LCV, the DLCV register bit must be first be written to logic zero and then to logic one again.

DFERR

The DFERR bit selects whether the framing pattern is corrupted for diagnostic purposes. When DFERR is logic one, the framing pattern inserted into the output data stream is inverted. When DFERR is logic zero, the unaltered framing pattern inserted into the output data stream.

CPERR

The CPERR bit enables continuous generation of BIP-8 errors for diagnostic purposes. When CPERR is logic one, the calculated BIP-8 value is continuously inverted according to the error mask specified by the BIP-8 Error Mask register and inserted into the G.832 EM byte. When CPERR is logic zero, the calculated BIP-8 value is altered only once, according to the error mask specified by the BIP-8 Error Mask register, and inserted into the EM byte.

PYLD&JUST

The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing modes G.751 is indicated as overhead or payload. When PYLD&JUST is logic one, the justification service bits and the tributary justification bits are indicated as payload. When PYLD&JUST is logic zero, the justification service and tributary justification bits are indicated as overhead.

Register 042H, 142H, 242H, 342H: E3 TRAN BIP-8 Error Mask

Bit	Type	Function	Default
Bit 7	R/W	MBIP[7]	0
Bit 6	R/W	MBIP[6]	0
Bit 5	R/W	MBIP[5]	0
Bit 4	R/W	MBIP[4]	0
Bit 3	R/W	MBIP[3]	0
Bit 2	R/W	MBIP[2]	0
Bit 1	R/W	MBIP[1]	0
Bit 0	R/W	MBIP[0]	0

MBIP[7:0]

The MBIP[7:0] bits act as an error mask to cause the transmitter to insert up to eight BIP-8 errors. The contents of this register are XORed with the calculated BIP-8 byte and inserted into the G.832 EM byte of the frame. A logic one in any MBIP bit position causes that bit position in the EM byte to be inverted. Writing this register with a mask value causes that mask to be applied only once; if continuous BIP-8 errors are desired, the CPERR bit in the Status and Diagnostic Options register can be used.

Register 043H, 143H, 243H, 343H: E3 TRAN Maintenance and Adaptation Options

Bit	Type	Function	Default
Bit 7	R/W	FERF/RAI	0
Bit 6	R/W	FEBE	0
Bit 5	R/W	PTYPE[2]	0
Bit 4	R/W	PTYPE[1]	0
Bit 3	R/W	PTYPE[0]	0
Bit 2	R/W	TUMFRM[1]	0
Bit 1	R/W	TUMFRM[0]	0
Bit 0	R/W	TIMEMK	0

TIMEMK

The TIMEMK bit determines the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TIMEMK is set to logic one, the Timing Marker bit in the MA byte is set to logic one. When TIMEMK is set to logic zero, the Timing Marker bit in the MA byte is set to logic zero.

TUMFRM[1:0]

The TUMFRM[1:0] bits reflect the value to be inserted in the Tributary Unit Multiframe bits (bits 6, and 7 of the G.832 Maintenance and Adaptation byte). These bits are logically ORed with the TUMFRM[1:0] overhead signals from the TOH input before being inserted in the MA byte.

PTYPE[2:0]

The PTYPE[2:0] bits reflect the value to be inserted in the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte).

FEBE

The FEBE bit reflects the value to be inserted in the FEBE indication bit (bit 2 of the G.832 Maintenance and Adaptation byte). The FEBE bit value is logically ORed with the FEBE indications generated by the FRMR for any detected BIP-8 errors. When the FEBE bit is logic one, bit 2 of the G.832 MA byte is set to logic one; when the FEBE bit is logic zero, any BIP-8 error indications from the FRMR causes bit 2 of the MA byte to be set to logic one.

FERF/RAI

The FERF/RAI bit reflects the value to be inserted in the FERF indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the RAI bit (bit 11 of the frame in G.751). The FERF/RAI bit is logically ORed with the LOS, OOF, AIS, and LCD indications from the E3 FRMR when the LOSEN, OOFEN, AISEN, and LCDEN register bits (in the S/UNI-4xD3FData Link and FERF/RAI Control register) are set to logic one respectively. When the OR of the two signals is logic one, the FERF or RAI bit in the frame is set to logic one; when neither signal is logic one, the FERF or RAI bit is set to logic zero.

Register 044H, 144H, 244H, 344H: J2-FRMR Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	UNI	0
Bit 5	R/W	REFRAME	0
Bit 4	R/W	FLOCK	0
Bit 3	R/W	CRC_REFR	0
Bit 2	R/W	SFRME	0
Bit 1	R/W	LOSTHR[1]	1
Bit 0	R/W	LOSTHR[0]	1

UNI

When the UNI bit is set to logic zero, the J2-FRMR expects unipolar data on the RDATI input and LCV indications on the RLCV input. When UNI is logic zero, the J2-FRMR expects bipolar B8ZS encoded data on the RPOS and RNEG inputs. When UNI is set to logic one, then the LOS, LOSI, and EXZI indications cannot be used.

REFRAME

Writing the REFRAME bit logic one forces the J2-FRMR to declare LOF, and begin searching for a new alignment. In order to force another reframe, REFRAME must be written with logic zero, and then logic one again.

FLOCK

When the FLOCK bit is set to logic one, the J2-FRMR is prevented from declaring LOF and searching for a new frame alignment due to framing-pattern errors. In this case, the J2-FRMR will only search for frame alignment when the REFRAME register bit transitions from logic zero to logic one.

CRC_REFR

When the CRC Reframe Enable bit is set to logic one, an alternate framing algorithm is enabled, which uses the CRC-5 check to detect framing to a mimic pattern in the payload or signaling bits. The framer, once it has seen at least one correct framing pattern, begins looking for correct CRC-5s as well. If it observes three consecutive correct framing patterns, and two correct CRC-5 sequences, then frame is declared. Otherwise, a reframe is initiated. When CRC_REFR is set to logic zero, the framing algorithm simply searches for three consecutive correct framing patterns.

SFRME

When the Single Framing Bit Error (SFRME) bit is set to logic one, then the J2-FRMR will indicate (to the PMON) a single framing error for every J2 multiframe which contains one or more framing errors. When the SFRME bit is set to logic zero, the J2-FRMR will identify every framing error to the PMON.

LOSTHR[1:0]

The LOS Threshold bits select the number of consecutive zeroes required before the J2-FRMR will declare LOS, and the number of bit periods without an occurrence of excess zeroes that must pass before the J2-FRMR will de-assert LOS. The thresholds are described in Table 13:

Table 13 J2 FRMR LOS Threshold Configurations

LOSTHR[1]	LOSTHR[0]	Threshold
0	0	15
0	1	31
1	0	63
1	1	255

Thus, if LOSTHR[1:0] = 11 binary, LOS will be declared after the 255th consecutive binary zero, and de-asserted when 255 bit periods have passed without an occurrence of a string of eight or more consecutive zeroes.

Register 045H, 145H, 245H, 345H: J2-FRMR Status

Bit	Type	Function	Default
Bit 7	R	LOS	X
Bit 6	R	LOF	X
Bit 5		Unused	X
Bit 4	R	RAI	X
Bit 3	R	RLOF	X
Bit 2		Unused	X
Bit 1	R	PHYAIS	X
Bit 0	R	PLDAIS	X

LOS, LOF, RAI, RLOF, PHYAIS, PLDAIS

These register bits reflect the current state of the LOS, LOF, RAI (RAI), Remote LOF (RLOF, also known as the a-bit), Physical AIS (PHYAIS), and Payload AIS (PLDAIS) conditions.

Register 046H, 146H, 246H, 346H: J2-FRMR Alarm Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LOSE	0
Bit 6	R/W	LOFE	0
Bit 5	R/W	COFAE	0
Bit 4	R/W	RAIE	0
Bit 3	R/W	RLOFE	0
Bit 2	R/W	RLOF_THR	1
Bit 1	R/W	PHYAISE	0
Bit 0	R/W	PLDAISE	0

LOSE

When LOSE is logic one, the J2-FRMR will generate an interrupt when the LOS condition changes state. Note: The LOS bit is not valid when the UNI bit is set in the J2-FRMR Configuration register.

LOFE

When LOFE is logic one, the J2-FRMR will generate an interrupt when LOF changes state.

COFAE

When COFAE is logic one, the J2-FRMR will generate an interrupt when a change of frame alignment occurs.

RAIE

When RAIE is logic one, the J2-FRMR will generate an interrupt when RAI changes state.

RLOFE

When RLOFE is logic one, the J2-FRMR will generate an interrupt when RLOF changes state.

RLOF_THR

The RLOF Threshold bit determines the number of consecutive a-bits that are required for the state of RLOF to change. When RLOF_THR is logic zero, RLOF is asserted when the a-bit has been logic one for three consecutive frames, and de-asserted when the a-bit has been logic zero for three consecutive frames. When RLOF_THR is logic one, RLOF is asserted when the a-bit has been logic one for five consecutive frames, and de-asserted when the a-bit has been logic zero for five consecutive frames. The default setting is that five consecutive a-bits are required.

PHYAISE

When PHYAISE is logic one, the J2-FRMR will generate an interrupt when a change is detected in the Physical AIS condition.

PLDAISE

When PLDAISE is logic one, the J2-FRMR will generate an interrupt when a change is detected in the Payload AIS condition.

Register 047H, 147H, 247H, 347H: J2-FRMR Alarm Interrupt Status

Bit	Type	Function	Default
Bit 7	R	LOSI	X
Bit 6	R	LOFI	X
Bit 5	R	COFAI	X
Bit 4	R	RAII	X
Bit 3	R	RLOFI	X
Bit 2		Unused	X
Bit 1	R	PHYAISI	X
Bit 0	R	PLDAISI	X

LOSI

The LOSI bit is set to logic one if a change occurs in the LOS condition. LOSI is cleared when this register is read.

LOFI

The LOFI bit is set to logic one if a change occurs in the state of LOF. LOFI is cleared when this register is read.

COFAI

The COFAI bit is set to logic one if a change in frame alignment occurs. COFAI is cleared when this register is read.

RAII

The RAII bit is set to logic one if a change in the value of RAI occurs. RAII is cleared when this register is read.

RLOFI

The RLOFI bit is set to logic one if a change in the value of RLOF occurs. RLOFI is cleared when this register is read.

PHYAISI

The PHYAISI bit is set to logic one if a change in the condition of PHYAIS occurs. PHYAISI is cleared when this register is read.

PLDAISI

The PLDAISI bit is set to logic one if a change in the condition of PLDAIS occurs. PLDAISI is cleared when this register is read.

Register 048H, 148H, 248H, 348H: J2-FRMR Error/Xbit Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	CRCEE	0
Bit 6	R/W	FRMEE	0
Bit 5	R/W	BPVE	0
Bit 4	R/W	EXZE	0
Bit 3	R/W	XBITE	0
Bit 2		Unused	X
Bit 1	R/W	XBIT_DEB	0
Bit 0	R/W	XBIT_THR	0

CRCEE

When CRCEE is logic one, the J2-FRMR will generate an interrupt if a multiframe fails its CRC-5 check.

FRMEE

When FRMEE is logic one, the J2-FRMR will generate an interrupt upon the reception of an errored framing bit.

BPVE

When BPVE is logic one, the J2-FRMR will generate an interrupt upon the reception of a bipolar violation which is not part of a valid B8ZS code (when UNI is set to logic zero in the J2-FRMR Configuration register) or on the reception of a logic one on RLCV (when UNI is set to logic one).

EXZE

When EXZE is logic one, the J2-FRMR will generate an interrupt upon the reception of a string of eight-or-more consecutive zeroes. EXZE has no effect when UNI is set to logic one in the J2-FRMR Configuration register.

XBITE

When XBITE is logic one, the J2-FRMR will generate an interrupt when any of the x-bits (X1, X2, X3) change state. Because the XBIT interrupt is generated when the x-bit indications change, the interrupt is debounced along with them via the XBIT_DEB and XBIT_THR bits.

XBIT_DEB

When XBIT_DEB is set to logic zero, the x-bit indications in the J2-FRMR Error/Xbit Interrupt Status register reflect the most recent value of the x-bits. When XBIT_DEB is set to logic one, the x-bit indications change value only when an x-bit has maintained its value for three or five consecutive multiframes, depending on the setting of XBIT_THR.

XBIT_THR

When XBIT_THR is set to logic one, then XBIT_THR controls the debouncing threshold of the x-bit indications in the J2-FRMR Error/Xbit Interrupt Status register. When XBIT_THR is logic zero, the threshold is set to three consecutive multiframes; when XBIT_THR is logic one, the threshold is set to five consecutive multiframes.

Register 049H, 149H, 249H, 349H: J2-FRMR Error/Xbit Interrupt Status

Bit	Type	Function	Default
Bit 7	R	CRCEI	X
Bit 6	R	FRMEI	X
Bit 5	R	BPVI	X
Bit 4	R	EXZI	X
Bit 3	R	XBITI	X
Bit 2	R	X3	X
Bit 1	R	X2	X
Bit 0	R	X1	X

CRCEI

The CRCEI bit is set to logic one if a failed CRC-5 check occurs. CRCEI is cleared when this register is read.

FRMEI

The FRMEI bit is set to logic one if an errored framing bit occurs. FRMEI is cleared when this register is read.

BPVI

The BPVI bit is set to logic one if a bipolar violation that is not part of a valid B8ZS code occurs (when UNI is logic zero in the J2-FRMR Configuration register) or if a 0 to 1 transition is detected on RLCV (when UNI is logic one). BPVI is cleared when this register is read.

EXZI

The EXZI bit is set to logic one upon reception of eight-or-more consecutive zeroes. EXZI remains logic zero while UNI is set to logic one in the J2_FRMR Configuration Register. EXZI is cleared when this register is read.

XBITI

The XBITI bit is set to logic one if a change in the debounced (if XBIT_DEB is set to logic one) x-bits (X1, X2, and X3) is detected. XBITI is cleared when this register is read.

X1, X2, X3

The X1, X2, and X3 bits reflect the most recent (debounced if XBIT_DEB is set to logic one) value of bits 785, 786, and 787 respectively of frame three of each multiframe. These bits are the spare or ‘x-bits’

Register 04CH, 14CH, 24CH, 34CH: J2-TRAN Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	X3SET	1
Bit 2	R/W	X2SET	1
Bit 1	R/W	X1SET	1
Bit 0	R/W	RLOF	0

RLOF

The RLOF-bit controls the state of the A-bit. When RLOF is a logic one, the A-bit is also set to logic one. When RLOF is a logic zero, the A-bit is set to logic zero. The A-bit in the transmit stream may also be set to logic one if an LOF condition in the J2 FRMR is detected and the RBLEN-bit is logic one in the S/UNI-4xD3F Data Link and FERF/RAI Control register.

X1SET

The X1SET bit controls the state of the X1 bit (bit 785 in the third frame of a J2 multiframe). When X1SET is a logic one, the X1 bit is set to logic one. When X1SET is a logic zero, the X1 bit is set to logic zero.

X2SET

The X2SET bit controls the state of the X2 bit (bit 786 in the third frame of a J2 multiframe). When X2SET is a logic one, the X2 bit is set to logic one. When X2SET is a logic zero, the X2 bit is set to logic zero.

X3SET

The X3SET bit controls the state of the X3 bit (bit 787 in the third frame of a J2 multiframe). When X3SET is a logic one, the X3 bit is set to logic one. When X3SET is a logic zero, the X3 bit is set to logic zero.

Reserved

The reserved register bits should be set to logic zero for proper operation.

Register 04DH, 14DH, 24DH, 34DH: J2-TRAN Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PLDAIS	0
Bit 4	R/W	PHYAIS	0
Bit 3	R/W	DCRC	0
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBPV	0
Bit 0	R/W	DFERR	0

DFERR

The DFERR bit controls the insertion of framing alignment signal errors. When DFERR is set to logic one, the framing alignment signal is inverted. When DFERR is set to logic zero, the framing alignment signal is not inverted.

DBPV

The DBPV bit controls the insertion of single bipolar violations. When DBPV bit transitions from 0 to 1, a violation is generated by masking the first violation pulse of a B8ZS signature. To generate another violation, this bit must first be written to 0 and then to logic one again. When DBPV is a logic zero, no violation is generated.

DLOS

When set to logic one, the DLOS bit forces the unipolar and bipolar outputs of the J2 TRAN to be all-zeros. When DLOS is logic zero, the outputs of the J2 TRAN operate normally.

DCRC

When set to logic one, a the CRC-5 check bits ($e_{1\text{-}5}$) are inverted before transmission. DCRC inverts the $e_{1\text{-}5}$ bits even if CDIS of the J2 TRAN Configuration register is set to logic one.

PHYAIS

When set to logic one, PHYAIS will cause the J2 TRAN to transmit an all 1's AIS.

PLDAIS

When set to logic one, PLDAIS will cause the J2 TRAN to insert all-ones in the payload data bits. When PLDAIS is a logic zero, data is processed normally through the J2 TRAN.

Register 04EH, 14EH, 24EH, 34EH: J2-TRAN TS97 Signaling

Bit	Type	Function	Default
Bit 7	R/W	TS97[1]	1
Bit 6	R/W	TS97[2]	1
Bit 5	R/W	TS97[3]	1
Bit 4	R/W	TS97[4]	1
Bit 3	R/W	TS97[5]	1
Bit 2	R/W	TS97[6]	1
Bit 1	R/W	TS97[7]	1
Bit 0	R/W	TS97[8]	1

TS97[1:8]

The TS97[1:8] bits control what is inserted into the J2 timeslot 97 bits. TS97[1] is the first bit of timeslot 97 transmitted.

Register 04FH, 14FH, 24FH, 34FH: J2-TRAN TS98 Signaling

Bit	Type	Function	Default
Bit 7	R/W	TS98[1]	1
Bit 6	R/W	TS98[2]	1
Bit 5	R/W	TS98[3]	1
Bit 4	R/W	TS98[4]	1
Bit 3	R/W	TS98[5]	1
Bit 2	R/W	TS98[6]	1
Bit 1	R/W	TS98[7]	1
Bit 0	R/W	TS98[8]	1

TS98[1:8]

The TS98[1:8] bits control what is inserted into the J2 timeslot 98. TS98[1] is the first bit of timeslot 98 transmitted.

Register 050H, 150H, 250H,350H: RDLC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN

The EN-bit controls the overall operation of the RDLC. When EN is set to logic one, RDLC is enabled; when set to logic zero, RDLC is disabled. When RDLC is disabled, the RDLC FIFO buffer and interrupts are all cleared. When RDLC is enabled, it will immediately begin looking for flags.

TR

Setting the terminate reception (TR) bit to logic one forces the RDLC to immediately terminate the reception of the current data frame, empty the RDLC FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN-bit from logic one to logic zero and back to logic one. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic zero after the register write operation is completed and a rising and falling edge occurs on the internal datalink clock input. If the RDLC Configuration register is read after this time, the TR bit value returned will be logic zero.

MEN

Setting the Match Enable (MEN) bit to logic one enables the detection and storage in the RDLC FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Match Address registers, or the universal all-ones address. When the MEN-bit is logic zero, all packets received are written into the RDLC FIFO.

MM

Setting the Match Mask (MM) bit to logic one ignores the PA[1:0] bits of the Primary Address Match register, the SA[1:0] bits of the Secondary Address Match register, and the two least significant bits of the universal all-ones address when performing the address comparison.

Reserved

This register bit should be set to logic zero for proper operation.

Register 051H, 151H, 251H, 351H: RDLC Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC[6:0]

The INTC[6:0] bits control the assertion of FIFO fill level set point interrupts. The value of INTC[6:0] = ‘b0000000 sets the interrupt FIFO fill level to 128.

INTE

The Interrupt Enable bit (INTE) must set to logic one to allow the internal interrupt status to be propagated to the INTB output. When the INTE bit is logic zero the RDLC will not assert INTB.

The contents of the Interrupt Control register should only be changed when the EN-bit in the RDLC Configuration register is logic zero. This prevents any erroneous interrupt generation.

Register 052H, 152H, 252H, 352H: RDLC Status

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/10 that of the clock selected by the LINESYSCLK bit of the S/UNI-4xD3F Miscellaneous register (09BH, 19BH, 29BH, 39BH).

INTR

The interrupt (INTR) bit reflects the status of the internal RDLC interrupt. If the INTE bit in the RDLC Interrupt Control register is set to logic one, a RDLC interrupt (INTR is a logic one) will cause INTB to be asserted low. The INTR register bit will be set to logic one when one of the following conditions occurs:

- The number of bytes specified in the RDLC Interrupt Control register are received on the data link and are written into the FIFO.
- RDLC FIFO buffer overrun is detected.
- The last byte of a packet is written into the RDLC FIFO.
- The last byte of an aborted packet is written into the RDLC FIFO.
- Transition of receiving all-ones to receiving flags is detected.

PBS[2:0]

The packet byte status (PBS[2:0]) bits indicate the status of the data last

Read from the FIFO as indicated in Table 14:

Table 14 RDLC PBS[2:0] Data Status

PBS[2:0]	Data Status
000	The data byte read from the FIFO is not special.
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.

PBS[2:0]	Data Status
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Unused.
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet.
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN

The Packet In (PKIN) bit is logic one when the last byte of a non-aborted packet is written into the FIFO. The PKIN-bit is cleared to logic zero after the RDLC Status register is read.

COLS

The Change of Link Status (COLS) bit is set to logic one if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic zero by reading this register or by clearing the EN-bit in the RDLC Configuration register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic one then the RDLC FIFO must be read until empty. The status of the data link is determined by the PBS[2:0] bits associated with the data read from the RDLC FIFO.

OVR

The overrun (OVR) bit is set to logic one when data is written over unread data in the RDLC FIFO buffer. This bit is not reset to logic zero until after the Status register is read. While the OVR bit is logic one, the RDLC and RDLC FIFO buffer are held in the reset state, causing the COLS and PKIN-bits to be reset to logic zero.

FE

The FIFO buffer empty (FE) bit is set to logic one when the last RDLC FIFO buffer entry is read. The FE bit goes to logic zero when the FIFO is loaded with new data.

Register 053H, 153H, 253H, 353H: RDLC Data

Bit	Type	Function	Default
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/10 that of the clock selected by the LINESYSCLK bit of the S/UNI-4xD3F Miscellaneous register (09BH, 19BH, 29BH, 39BH).

RD[7:0]

RD[7:0] contains the received data link information. RD[0] corresponds to the first received bit of the data link message.

This register reads from the RDLC 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status register is logic zero.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the RDLC Status register is read.

Register 054H, 154H, 254H, 354H: RDLC Primary Address Match

Bit	Type	Function	Default
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

PA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first received bit of the data link message. The MM-bit in the Configuration register is used mask off PA[1:0] during the address comparison.

Register 055H, 155H, 255H, 355H: RDLC Secondary Address Match

Bit	Type	Function	Default
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

SA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first received bit data link message. The MM-bit in the Configuration register is used mask off SA[1:0] during the address comparison.

Register 058H, 158H, 258H, 358H: TDPR Configuration

Bit	Type	Function	Default
Bit 7	R/W	FLGSHARE	1
Bit 6	R/W	FIFOCLR	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	R/W	EOM	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	1
Bit 0	R/W	EN	0

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the S/UNI-4xD3F Miscellaneous register (09BH, 19BH, 29BH, 39BH).

EN

The EN-bit enables the TDPR functions. When EN is set to logic one, the TDPR is enabled and flag sequences are sent until data is written into the TDPR Transmit Data register. When the EN-bit is set to logic zero, the TDPR is disabled and an all-ones Idle sequence is transmitted on the datalink.

CRC

The CRC enable bit controls the generation of the CCITT_CRC frame check sequence (FCS). Setting the CRC bit to logic one enables the CCITT-CRC generator and appends the 16-bit FCS to the end of each message. When the CRC bit is set to logic zero, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT

The Abort (ABT) bit controls the sending of the seven consecutive-ones HDLC abort code. Setting the ABT bit to a logic one causes the 01111111 code (the 0 is transmitted first) to be transmitted after the current byte from the TDPR FIFO is transmitted. The TDPR FIFO is then reset. All data in the TDPR FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic zero. At least one Abort sequence will be sent when the ABT bit transitions from logic zero to logic one.

EOM

The EOM-bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM-bit is automatically cleared upon a write to the TDPR Transmit Data register.

Reserved

This bit should be set to logic zero for proper operation.

FIFOCLR

The FIFOCLR bit resets the TDPR FIFO. When set to logic one, FIFOCLR will cause the TDPR FIFO to be cleared.

FLGSHARE

The FLGSHARE bit configures the TDPR to share the opening and closing flags between successive frames. If FLGSHARE is logic one, then the opening and closing flags between successive frames are shared. If FLGSHARE is logic zero, then separate closing and opening flags are inserted between successive frames.

Register 059H, 159H, 259H, 359H: TDPR Upper Transmit Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	UTHR[6]	1
Bit 5	R/W	UTHR[5]	0
Bit 4	R/W	UTHR[4]	0
Bit 3	R/W	UTHR[3]	0
Bit 2	R/W	UTHR[2]	0
Bit 1	R/W	UTHR[1]	0
Bit 0	R/W	UTHR[0]	0

UTHR[6:0]

The UTHR[6:0] bits define the TDPR FIFO fill level which will automatically cause the bytes stored in the TDPR FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR FIFO fill level is below UTHR[6:0] + 1.

Register 05AH, 15AH, 25AH, 35AH: TDPR Lower Interrupt Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	LINT[6]	0
Bit 5	R/W	LINT[5]	0
Bit 4	R/W	LINT[4]	0
Bit 3	R/W	LINT[3]	0
Bit 2	R/W	LINT[2]	1
Bit 1	R/W	LINT[1]	1
Bit 0	R/W	LINT[0]	1

LINT[6:0]

The LINT[6:0] bits define the TDPR FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR FIFO level decrements to empty or to a value less than LINT[6:0], LFILLI and BLFILL register bits will be set to logic one. LFILLI will cause an interrupt on INTB if LFILLE is set to logic one.

Register 05BH, 15BH, 25BH, 35BH: TDPR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	FULLE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	UDRE	0
Bit 0	R/W	LFILLE	0

LFILLE

The LFILLE enables a transition to logic one on LFILLI to generate an interrupt on INTB. If LFILLE is a logic one, a transition to logic one on LFILLI will generate an interrupt on INTB. If LFILLE is a logic zero, a transition to logic one on LFILLI will not generate an interrupt on INTB.

UDRE

The UDRE enables a transition to logic one on UDRI to generate an interrupt on INTB. If UDRE is a logic one, a transition to logic one on UDRI will generate an interrupt on INTB. If UDRE is a logic zero, a transition to logic one on UDRI will not generate an interrupt on INTB.

OVRE

The OVRE enables a transition to logic one on OVRI to generate an interrupt on INTB. If OVRE is a logic one, a transition to logic one on OVRI will generate an interrupt on INTB. If OVRE is a logic zero, a transition to logic one on OVRI will not generate an interrupt on INTB.

FULLE

The FULLE enables a transition to logic one on FULLI to generate an interrupt on INTB. If FULLE is a logic one, a transition to logic one on FULLI will generate an interrupt on INTB. If FULLE is a logic zero, a transition to logic one on FULLI will not generate an interrupt on INTB.

Reserved

This bit should be set to logic zero for proper operation.

Register 05CH, 15CH, 25CH, 35CH: TDPR Interrupt Status/UDR Clear

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FULL	X
Bit 5	R	BLFILL	X
Bit 4	R	Unused	X
Bit 3	R	FULLI	X
Bit 2	R	OVRI	X
Bit 1	R	UDRI	X
Bit 0	R	LFILLI	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the S/UNI-4xD3F Miscellaneous register (09BH, 19BH, 29BH, 39BH).

LFILLI

The LFILLI bit will transition to logic one when the TDPR FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR Lower Interrupt Threshold register. LFILLI will assert INTB if it is a logic one and LFILLE is programmed to logic one. LFILLI is cleared when this register is read.

UDRI

The UDRI bit will transition to logic one when the TDPR FIFO underruns. That is, the TDPR is in the process of transmitting a packet when it runs out of data to transmit. UDRI will assert INTB if it is a logic one and UDRE is programmed to logic one. UDRI is cleared when this register is read.

OVRI

The OVRI bit will transition to logic one when the TDPR FIFO overruns. That is, the TDPR FIFO is already full when another data byte is written to the TDPR Transmit Data register. OVRI will assert INTB if it is a logic one and OVRE is programmed to logic one. OVRI is cleared when this register is read.

FULLI

The FULLI bit will transition to logic one when the TDPR FIFO is full. FULLI will assert INTB if it is a logic one and FULLE is programmed to logic one. FULLI is cleared when this register is read.

BLFILL

The BLFILL bit is set to logic one if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL

The FULL bit reflects the current condition of the TDPR FIFO. If FULL is a logic one, the TDPR FIFO already contains 128-bytes of data and can accept no more.

Register 05DH, 15DH, 25DH, 35DH: TDPR Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD[7]	X
Bit 6	R/W	TD[6]	X
Bit 5	R/W	TD[5]	X
Bit 4	R/W	TD[4]	X
Bit 3	R/W	TD[3]	X
Bit 2	R/W	TD[2]	X
Bit 1	R/W	TD[1]	X
Bit 0	R/W	TD[0]	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the S/UNI-4xD3F Miscellaneous register (09BH, 19BH, 29BH, 39BH).

TD[7:0]

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

Register 090H, 190H, 290H, 390H: TTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	Reserved	0

Reserved

The reserved bit should be set to logic zero for proper operation.

NOSYNC

The NOSYNC bit disables synchronization to the Trail Trace message. When NOSYNC is set high, synchronization is disabled and the bytes of the Trail Trace message are captured by the TTB in a circular buffer. When NOSYNC is set low, the TTB synchronizes to the byte with the most significant bit set high and places that byte in the first location in the capture buffer page.

TNULL

The transmit null (TNULL) bit controls the insertion of all-zeros into the outgoing Trail Trace message. The null insertion should be used when microprocessor accesses that change the outgoing trail trace message are being performed. When TNULL is set high, an all-zeros byte is inserted to the transmit stream. When this bit is set low, the contents of the transmit trace buffer are sent.

PER5

The receive trace identifier persistency bit (PER5) controls the number of times that persistency check is made in order to accept the received message. When this bit is set high, five identical message required in order to accept the message. When this bit set low, three unchanged consecutive messages are required.

RTIMIE

The receive trace identifier mismatch interrupt enable (RTIMIE) controls the activation of the interrupt output when comparison between the accepted trace identifier message and the expected trace identifier message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state will activate the interrupt output. When RTIMIE set low, trail trace message match state changes will not affect INTB.

RTIUIE

The receive trace identifier unstable interrupt enable (RTIUIE) control the activation of the interrupt output when the receive trace identifier message changes state from stable to unstable and vice versa. When RTIUIE is set high, changes in the state of the trail trace message unstable indication will activate the interrupt output. When RTIUIE set low, trail trace unstable state changes will not effect INTB.

RRAMACC

The receive RAM access (RRAMACC) control bit is used by the microprocessor to identify that the access from the microprocessor is to the receive trace buffers (addresses 0 - 127) or to the transmit trace buffer (addresses 128 - 191). When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

ZEROEN

The zero enable bit (ZEROEN) enables TIM assertion and removal based on an all-zeros path trace message string. When ZEROEN is set high, all-zeros path trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all-zeros path trace message strings are ignored.

Register 091H, 191H, 291H, 391H: TTB Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

RTIMV

The receive trace identifier mismatch value status bit (RTIMV) is set high when the accepted message differs from the expected message. RTIMV is set low when the accepted message is equal to the expected message. A mismatch is not declared if the accepted trail trace message string is all-zeros.

RTIMI

The receive trace identifier mismatch indication status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read.

RTIUV

The receive trace identifier unstable value status bit (RTIUV) is set high when eight messages that differ from its immediate predecessor are received. RTIUV is set low and the unstable message count is reset when three or five (depending on PER5 control bit) consecutive identical messages are received.

RTIUI

The receive trace identifier unstable indication status bit (RTIUV) is set high when the stable/unstable status of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read.

BUSY

The BUSY bit reports whether a previously initiated indirect read or write to the trail trace RAM has been completed. BUSY is set high upon writing to the TTB Indirect Address register, and stays high until the access has completed. At this point, BUSY is set low. This register should be polled to determine when either new data is available in the TTB Indirect Data register after an indirect read, or when the TTB is ready to accept another write access.

Register 092H, 192H, 292H, 392H: TTB Indirect Address

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

A[6:0]

The indirect read address bits (A[6:0]) indexes into the trail trace identifier buffers. When RRAMACC is set high, decimal addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive G.832 E3 stream. The receive expected page contains the expected trace identifier message downloaded from the microprocessor. When RRAMACC is set low, decimal addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted in the TR bytes of the G.832 E3 transmit stream. In this case A[6] is a don't care (for example, address 0 and address 64 are indexes to the same location in the buffer). Note: Only the first 16 addresses need to be written with the trail trace message to be transmitted.

RWB

The access control bit (RWB) selects between an indirect read or write access to the static page of the trail trace message buffer. Writing to this indirect address register initiates an external microprocessor access to the static page of the trail trace message buffer. When RWB is set high, a read access is initiated. The data read is available upon completion of the access in the TTB Indirect Data register. When RWB is set low, a write access is initiated. The data in the TTB Indirect Data register will be written to the addressed location in the static page.

Register 093H, 193H, 293H, 393H: TTB Indirect Data

Bit	Type	Function	Default
Bit 7	R/W	D[7]	X
Bit 6	R/W	D[6]	X
Bit 5	R/W	D[5]	X
Bit 4	R/W	D[4]	X
Bit 3	R/W	D[3]	X
Bit 2	R/W	D[2]	X
Bit 1	R/W	D[1]	X
Bit 0	R/W	D[0]	X

D[7:0]

The indirect data bits (D[7:0]) contain either the data read from a message buffer after an indirect read operation has completed, or the data to be written to the RAM for an indirect write operation. Note: The write data must be set up in this register before an indirect write is initiated. Data read from this register reflects the value written until the completion of a subsequent indirect read operation.

Register 094H, 194H, 294H, 394H: TTB EXPLD Type Label

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	EXPLD[2]	0
Bit 1	R/W	EXPLD[1]	0
Bit 0	R/W	EXPLD[0]	0

EXPLD[2:0]

The EXPLD[2:0] bits contain the expected payload type label bits of the G.832 E3 Maintenance and Adaptation (MA) byte. The EXPLD[2:0] bits are compared with the received payload type label extracted from the receive stream. A payload type label mismatch (PLDM) is declared if the received payload type bits differs from the expected payload type. If enabled, an interrupt is asserted upon declaration and removal of PLDM.

For compatibility with old equipment that inserts 000B for unequipped or 001B for equipped, regardless of the payload type, the receive payload type label mismatch mechanism is based on Table 15:

Table 15 TTB Payload Type Match Configurations

Expected	Received	Action
000	000	Match
000	001	Mismatch
000	XXX	Mismatch
001	000	Mismatch
001	001	Match
001	XXX	Match
XXX	000	Mismatch
XXX	001	Match
XXX	XXX	Match
XXX	YYY	Mismatch

Note:

1. XXX, YYY = anything except 000B or 001B, and XXX is not equal to YYY.

Reserved

The reserved bits must be written to logic zero for proper operation.

Register 095H, 195H, 295H, 395H: TTB Payload Type Label Control/Status

Bit	Type	Function	Default
Bit 7	R/W	RPLDUIE	0
Bit 6	R/W	RPLDMIE	0
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	RPLDUI	X
Bit 2	R	RPLDUV	X
Bit 1	R	RPLDMI	X
Bit 0	R	RPLDMV	X

RPLDMV

The receive payload type label mismatch status bit (RPLDMV) reports the match/mismatch status between the expected and the received payload type label. RPLDMV is set high when the received payload type bits differ from the expected payload type written to the TTB Expected Payload Type Label register. The PLDMV bit is set low when the received payload type matches the expected payload type.

RPLDMI

The receive payload type label mismatch interrupt status bit (RPLDMI) is set high when the match/mismatch status between the received and the expected payload type label changes state. This bit (and the interrupt) is cleared when this register is read.

RPLDUV

The receive payload type label unstable status bit (RPLDUV) reports the stable/unstable status of the payload type label bits in the receive stream. RPLDUV is set high when five labels that differ from its immediate predecessor are received. RPLDUV is set low and the unstable label count is reset when five consecutive identical labels are received.

RPLDUI

The receive payload type label unstable interrupt status bit (RPLDUI) is set high when the stable/unstable status of the path signal label changes state. This bit (and the interrupt) is cleared when this register is read.

RPLDMIE

The receive payload type label mismatch interrupt enable bit (RPLDMIE) controls the activation of the interrupt output when the comparison between received and the expected payload type label changes state from match to mismatch and vice versa. When RPLDMIE is set high, changes in match state activates the interrupt output. When RPLDMIE is set low, changes from match to mismatch or mismatch to match will not generate an interrupt.

RPLDUIE

The receive payload type label unstable interrupt enable bit (RPLDUIE) controls the activation of the interrupt output when the received payload type label changes state from stable to unstable and vice versa. When RPLDUIE is set high, changes in stable state activates the interrupt output. When RPLDUIE is set low, changes in the stable state will not generate and interrupt.

Register 098H, 198H, 298H, 398H: RBOC Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	FEACE	0

FEACE

The FEACE bit enables the generation of an interrupt when a valid far end alarm and control (FEAC) code is detected. When a logic one is written to FEACE, the interrupt generation is enabled.

AVC

The AVC bit position selects the validation criterion used in determining a valid FEAC code. When a logic zero is written to AVC, a FEAC code is validated when eight out of the last 10 received codes are identical. The FEAC code is removed when 2 out of the last 10 received code do not match the validated code.

When a logic one is written to AVC, a FEAC code is validated when four out of the last five received codes are identical. The FEAC code is removed when a single received FEACs does not match the validated code.

IDLE

The IDLE bit enables the generation of an interrupt when a validated FEAC is removed. When a logic one is written to IDLE, the interrupt generation is enabled.

Register 099H, 199H, 299H, 399H: RBOC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	IDLI	X
Bit 6	R	FEACI	X
Bit 5	R	FEAC[5]	X
Bit 4	R	FEAC[4]	X
Bit 3	R	FEAC[3]	X
Bit 2	R	FEAC[2]	X
Bit 1	R	FEAC[1]	X
Bit 0	R	FEAC[0]	X

FEAC[5:0]

The FEAC[5:0] bits contain the received far end alarm and control channel codes. The FEAC[5:0] bits are set to all-ones (“111111”) when no code has been validated.

FEACI

The FEACI bit is set to logic one when a new FEAC code is validated. The FEAC code value is contained in the FEAC[5:0] bits. The FEACI bit position is set to logic zero when this register is read.

IDLI

The IDLI bit is set to logic one when a validated FEAC code is removed. The FEAC[5:0] bits are set to all-ones when the code is removed. The IDLI bit position is set to logic zero when this register is read.

Register 09AH, 19AH, 29AH, 39AH: XBOC Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	FEAC[5]	1
Bit 4	R/W	FEAC[4]	1
Bit 3	R/W	FEAC[3]	1
Bit 2	R/W	FEAC[2]	1
Bit 1	R/W	FEAC[1]	1
Bit 0	R/W	FEAC[0]	1

FEAC[5:0]

FEAC[5:0] contain the six bit code that is transmitted on the far end alarm and control channel (FEAC). The transmitted code consists of a sixteen bit sequence that is repeated continuously. The sequence consists of eight ones followed by a zero, followed by the six bit code sequence transmitted in order FEAC0, FEAC1, .., FEAC5, followed by a zero. The all-ones sequence is inserted in the FEAC channel when FEAC[5:0] is written with all-ones.

Note: If configured for J2 transmission format (TFRM[1:0] is 10 binary) and any of Reserved, AISEN, OOFEN, LOSEN are set to logic one in the S/UNI-4xD3FData Link and FERF/RAI Control, FEAC[5:0] in this register must all be set to logic one for proper RAI transmission PHYAIS, LOF, or LOS by the J2 FRMR. Otherwise, the BOC code configured by the FEAC[5:0] bits of this register will be transmitted instead of the RAI.

Register 09BH, 19BH, 29BH, 39BH: S/UNI-4xD3F Miscellaneous

Bit	Type	Function	Default
Bit 7	R/W	AISOOF	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TPRBS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TCELL	0
Bit 2	R/W	LOC_RESET	0
Bit 1	R/W	FORCELOS	0
Bit 0	R/W	LINESYSCLK	0

LINESYSCLK

LINESYSCLK is used to select the high-speed system clock which the TDPR and RDLC transmit and receive HDLC controllers use as a reference. If LINESYSCLK is set to logic one, then the RDLC uses the receive line clock (RCLK[x]) and the TDPR uses the transmit line clock (TICLK[x]) as its high-speed system reference clock respectively. **This bit must be set to logic one for proper operation.**

The read/write access rate to the RDLC and TDPR are limited by their high-speed reference clock frequency. Data and Configuration settings can be written into the TDPR at a maximum rate equal to 1/8 of its high-speed reference clock frequency. Data and status indications can be read from the TDPR at a maximum rate equal to 1/8 of its high-speed reference clock frequency. Data and status indications can be read from the RDLC at a maximum rate equal to 1/10 of its high-speed reference clock frequency.

Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read and write the TDPR and RDLC registers.

FORCELOS

FORCELOS is used to force a LOS condition on the transmit unipolar or bipolar data outputs TPOS/TDATO[x] and TNEG[x]. When FORCELOS is logic one, the TPOS/TDATO[x] and TNEG[x] outputs will be forced to logic zero. When FORCELOS is logic zero, the TPOS/TDATO[x] and TNEG[x] outputs will operate normally.

LOC_RESET

LOC_RESET performs a software local reset of the corresponding quadrant of the S/UNI-4xD3F. When LOC_RESET is logic one, the corresponding quadrant of the S/UNI-4xD3F is held in a reset state. When LOC_RESET is logic zero, the quadrant is in normal operational mode.

The LOC_RESET bit for quadrant 1 (register 09BH) also resets the chip level Utopia bus. While the LOC_RESET for quadrant 1 is set to logic one, the S/UNI-4xD3F ’s Utopia bus will be held in a reset state, and will not function. In applications where the Utopia bus is required, the LOC_RESET for quadrant 1 should not be permanently set to logic one.

TCELL

When the TCELL bit is a logic one, the TPOHFP/TFPO/TMFPO/TGAPCLK/TCELL[4:1] pin takes on the TCELL function, and pulses once for every transmitted cell (idle or unassigned).

Reserved

The reserved bit should be set to logic zero for proper operation.

TPRBS

register bit TPRBS is used to insert a pseudo-random binary sequence into the transmit stream in place of other payload data. The exact nature of the PRBS is configurable through the PRGD registers (xA0H to xAFH).

Reserved

The reserved bit should be set to logic zero for proper operation.

AISOOF

The AISOOF-bit allows the receive data output stream on RDATO[x] to be forced to all 1’s when the DS3, E3, or J2 FRMR loses frame. When AISOOF is set to logic one, RDATO[x] will be forced to all 1’s when frame alignment is lost. When AISOOF is set to logic zero, RDATO[x] will continue to output raw data even when frame alignment is lost.

Note: AISOOF is only valid in framer-only mode (FRMRONLY=1, S/UNI-4xD3F Configuration 1 register).

Register 09CH, 19CH, 29CH, 39CH: S/UNI-4xD3F FRMR LOF Status

Bit	Type	Function	Default
Bit 7	R	FRMLOF	X
Bit 6	R/W	FRMLOFE	0
Bit 5	R	FRMLOFI	X
Bit 4	R/W	J2SIGTHRU	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

FRMLOFI

The FRMLOFI bit shows that a transition has occurred on the FRMLOF state. When FRMLOFI is logic one, the FRMLOF state has changed since the last read of this register. The FRMLOFI bit is cleared whenever this register is read.

FRMLOFE

The FRMLOFE bit enables the generation of an interrupt due to a change in the FRMLOF state. When FRMLOFE is a logic one, the interrupt is enabled.

FRMLOF

The FRMLOF-bit shows the current state of the E3/T3 LOF or the J2 Extended LOF indication (depending on which mode is enabled). When FRMLOF is logic one, the framer has lost frame synchronization for greater than 1ms, 2ms, or 3ms depending on the setting of the LOFINT[1:0] bits in the S/UNI-4xD3F Receive Configuration register.

J2SIGTHRU

The J2SIGTHRU bit allows the signaling bits in timeslot 97 and 98 on the TDATI[x] stream to pass transparently through the J2 TRAN. When J2SIGTHRU is logic one, timeslots 97 and 98 are passed transparently through from TDATI[x]. When J2SIGTHRU is logic zero, timeslots 97 and 98 are sourced from the J2 TRAN TS97 Signaling and J2 TRAN TS98 Signaling registers.

If J2SIGTHRU is set to logic one and TPRBS (S/UNI-4xD3F Miscellaneous register) is also set to logic one, the transmitted PRBS will continue through timeslots 97 and 98.

J2SIGTHRU is only valid in framer-only mode (FRMRONLY=1, S/UNI-4xD3F Configuration 1 register).

Register 0A0H, 1A0H, 2A0H, 3A0H: PRGD Control

Bit	Type	Function	Default
Bit 7	R/W	PDR[1]	0
Bit 6	R/W	PDR[0]	0
Bit 5	R/W	QRSS	0
Bit 4	R/W	PS	0
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

PDR[1:0]

The PDR[1:0] bits select the content of the four pattern detector registers (at addresses xACH to xAFH) to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in Table 16:

Table 16 PRGD Pattern Detector Register Configuration

PDR[1:0]	PDR#1	PDR#2	PDR#3	PDR#4
00, 01	Pattern Receive (LSB)	Pattern Receive	Pattern Receive	Pattern Receive (MSB)
10	Error Count (LSB)	Error Count	Error Count	Error Count (MSB)
11	Bit Count (LSB)	Bit Count	Bit Count	Bit Count (MSB)

QRSS

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic one, a one is forced in the TDATO stream when the following 14 bit positions are all-zeros. When QRSS is a logic zero, the zero suppression feature is disabled.

PS

The PS bit selects the generated pattern. When PS is a logic one, a repetitive pattern is generated. When PS is a logic zero, a pseudo-random pattern is generated.

The PS bit must be programmed to the desired setting before programming any other PRGD registers, or the transmitted pattern may be corrupted. Any time the setting of the PS bit is changed, the rest of the PRGD registers should be reprogrammed.

TINV

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic one, the data is inverted. When TINV is a logic zero, the data is not inverted

RINV

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic one, the received data is inverted before being processed by the pattern detector. When RINV is a logic zero, the received data is not inverted

AUTOSYNC

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when six or more bit errors are detected in the last 64 bit periods. When AUTOSYNC is a logic one, the auto resync feature is enabled. When AUTO SYNC is a logic zero, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low-to-high transition on MANSYNC initiates the resynchronization.

Register 0A1H, 1A1H, 2A1H, 3A1H: PRGD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic one, the interrupt is enabled.

BEE

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic one, the interrupt is enabled.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic one, the interrupt is enabled.

SYNCV

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic one the pattern detector is synchronized (the pattern detector has observed at least 32 consecutive error-free bit periods). When SYNCV is a logic zero, the pattern detector is out-of-sync (the pattern detector has detected six or more bit errors in a 64 bit period window).

SYNCI

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic one, then the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic zero when this register is read.

BEI

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic one, at least one bit error has been detected. BEI is set to logic zero when this register is read.

XFERI

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic one in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing to the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update register (006H). XFERI is set to logic zero when this register is read.

OVR

The OVR bit is the overrun status of the pattern detector registers. A logic one in this bit position indicates that a previous transfer (indicated by XFERI being logic one) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic zero when this register is read.

Register 0A2H, 1A2H, 2A2H, 3A2H: PRGD Length

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PL[4]	0
Bit 3	R/W	PL[3]	0
Bit 2	R/W	PL[2]	0
Bit 1	R/W	PL[1]	0
Bit 0	R/W	PL[0]	0

PL[4:0]

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

Register 0A3H, 1A3H, 2A3H, 3A3H: PRGD Tap

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PT[4]	0
Bit 3	R/W	PT[3]	0
Bit 2	R/W	PT[2]	0
Bit 1	R/W	PT[1]	0
Bit 0	R/W	PT[0]	0

PT[4:0]

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Register 0A4H, 1A4H, 2A4H, 3A4H: PRGD Error Insertion

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EVENT	0
Bit 2	R/W	EIR[2]	0
Bit 1	R/W	EIR[1]	0
Bit 0	R/W	EIR[0]	0

EVENT

A low-to-high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

EIR[2:0]

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in Table 17:

Table 17 PRGD Generated Bit Error Rate Configurations

EIR[2:0]	Generated Bit Error Rate
000	No errors inserted
001	10^{-1}
010	10^{-2}
011	10^{-3}
100	10^{-4}
101	10^{-5}
110	10^{-6}
111	10^{-7}

Register 0A8H, 1A8H, 2A8H, 3A8H: Pattern Insertion #1

Bit	Type	Function	Default
Bit 7	R/W	PI[7]	0
Bit 6	R/W	PI[6]	0
Bit 5	R/W	PI[5]	0
Bit 4	R/W	PI[4]	0
Bit 3	R/W	PI[3]	0
Bit 2	R/W	PI[2]	0
Bit 1	R/W	PI[1]	0
Bit 0	R/W	PI[0]	0

Register 0A9H, 1A9H, 2A9H, 3A9H: Pattern Insertion #2

Bit	Type	Function	Default
Bit 7	R/W	PI[15]	0
Bit 6	R/W	PI[14]	0
Bit 5	R/W	PI[13]	0
Bit 4	R/W	PI[12]	0
Bit 3	R/W	PI[11]	0
Bit 2	R/W	PI[10]	0
Bit 1	R/W	PI[9]	0
Bit 0	R/W	PI[8]	0

Register 0AAH, 1AAH, 2AAH, 3AAH: Pattern Insertion #3

Bit	Type	Function	Default
Bit 7	R/W	PI[23]	0
Bit 6	R/W	PI[22]	0
Bit 5	R/W	PI[21]	0
Bit 4	R/W	PI[20]	0
Bit 3	R/W	PI[19]	0
Bit 2	R/W	PI[18]	0
Bit 1	R/W	PI[17]	0
Bit 0	R/W	PI[16]	0

Register 0ABH, 1ABH, 2ABH, 3ABH: Pattern Insertion #4

Bit	Type	Function	Default
Bit 7	R/W	PI[31]	0
Bit 6	R/W	PI[30]	0
Bit 5	R/W	PI[29]	0
Bit 4	R/W	PI[28]	0
Bit 3	R/W	PI[27]	0
Bit 2	R/W	PI[26]	0
Bit 1	R/W	PI[25]	0
Bit 0	R/W	PI[24]	0

PI[31:0]

PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] should be set to 0xFFFFFFFF. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 to #3 should be loaded with the desired data before pattern register #4 is written.

Register 0ACH, 1ACH, 2ACH, 3ACH: PRGD Pattern Detector #1

Bit	Type	Function	Default
Bit 7	R	PD[7]	0
Bit 6	R	PD[6]	0
Bit 5	R	PD[5]	0
Bit 4	R	PD[4]	0
Bit 3	R	PD[3]	0
Bit 2	R	PD[2]	0
Bit 1	R	PD[1]	0
Bit 0	R	PD[0]	0

Register 0ADH, 1ADH, 2ADH, 3ADH: PRGD Pattern Detector #2

Bit	Type	Function	Default
Bit 7	R	PD[15]	0
Bit 6	R	PD[14]	0
Bit 5	R	PD[13]	0
Bit 4	R	PD[12]	0
Bit 3	R	PD[11]	0
Bit 2	R	PD[10]	0
Bit 1	R	PD[9]	0
Bit 0	R	PD[8]	0

Register 0AEH, 1AEH, 2AEH, 3AEH: PRGD Pattern Detector #3

Bit	Type	Function	Default
Bit 7	R	PD[23]	0
Bit 6	R	PD[22]	0
Bit 5	R	PD[21]	0
Bit 4	R	PD[20]	0
Bit 3	R	PD[19]	0
Bit 2	R	PD[18]	0
Bit 1	R	PD[17]	0
Bit 0	R	PD[16]	0

Register 0AFH, 1AFH, 2AFH, 3AFH: PRGD Pattern Detector #4

Bit	Type	Function	Default
Bit 7	R	PD[31]	0
Bit 6	R	PD[30]	0
Bit 5	R	PD[29]	0
Bit 4	R	PD[28]	0
Bit 3	R	PD[27]	0
Bit 2	R	PD[26]	0
Bit 1	R	PD[25]	0
Bit 0	R	PD[24]	0

PD[31:0]

PD[31:0] contain the pattern detector data. The values contained in these registers are determined by the PDR[1:0] bits in the control register.

When PDR[1:0] is set to 00 or 01, PD[31:0] contain the pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0}. PD[31] contains the first of the 32 received bits, PD[0] contains the last of the 32 received bits.

When PDR[1:0] is set to 10, PD[31:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval. Note: Bit errors are not accumulated while the pattern detector is out-of-sync.

When PDR[1:0] is set to 11, PD[31:0] contain the bit counter holding register. The value in this register represents the total number of bits that have been received since the last accumulation interval.

The values of PD[31:0] are updated whenever one of the four PRGD Pattern Detector registers is written or when register 006H, the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update register is written.

Register 40CH: S/UNI-4xD3F Identification

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Device_ID	1
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

This register provides a device identification to distinguish the S/UNI-4xD3F from a S/UNI-4xD3F in applications where the S/UNI-4xD3F is used for prototype purposes.

DEVICE_ID

The DEVICE_ID bit allows software to identify the device as a S/UNI-4xD3F. A logic one identifies the device as a S/UNI-4xD3F, whereas a logic zero identifies the device as a S/UNI-4xD3F. To access this register, the IOTST bit in the S/UNI-4xD3F Master Test register must first be set to logic one. The Device_ID bit can now be read. A logic zero must then be written back to the IOTST bit to put the device back into normal mode of operation.

12 Test Features Description

The test mode registers, shown in Table 18, are used for production and board testing.

During production testing, the test mode registers are used to apply test vectors. In this case, the test mode registers (as opposed to the normal mode registers) are selected when A[10] is high.

During board testing, the digital output pins and the data bus are held in a high-impedance state by simultaneously asserting (low) the CSB, RDB, and WRB inputs. All of the TSBs for the S/UNI-4xD3F are placed in test mode 0 so that device inputs may be read and device outputs may be forced through the microprocessor interface. Refer to the section "Test Mode 0" for details.

Note: The S/UNI-4xD3F supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port that can be used for board testing. All digital device inputs may be read and all digital device outputs may be forced through this JTAG test port.

Table 18 Test Mode Register Memory Map

Address 000H-3FFH 400H				**Register** Normal Mode Registers Master Test Register
410H	510H	610H	710H	PMON Test Register 0
411H	511H	611H	711H	PMON Test Register 1
430H	530H	630H	730H	DS3 FRMR Test Register 0
431H	531H	631H	731H	DS3 FRMR Test Register 1
432H	532H	632H	732H	DS3 FRMR Test Register 2
433H	533H	633H	733H	DS3 FRMR Test Register 3
434H	534H	634H	734H	DS3 TRAN Test Register 0
435H	535H	635H	735H	DS3 TRAN Test Register 1
436H	536H	636H	736H	DS3 TRAN Test Register 2
438H	538H	638H	738H	E3 FRMR Test Register 0
439H	539H	639H	739H	E3 FRMR Test Register 1
43AH	53AH	63AH	73AH	E3 FRMR Test Register 2
440H	540H	640H	740H	E3 TRAN Test Register 0
441H	541H	641H	741H	E3 TRAN Test Register 1
442H	542H	642H	742H	E3 TRAN Test Register 2
444H	544H	644H	744H	J2 FRMR Test Register 0
445H	545H	645H	745H	J2 FRMR Test Register 1
446H	546H	646H	746H	J2 FRMR Test Register 2
447H	547H	647H	747H	J2 FRMR Test Register 3
44CH	54CH	64CH	74CH	J2 TRAN Test Register 0
44DH	54DH	64DH	74DH	J2 TRAN Test Register 1
44EH	54EH	64EH	74EH	J2 TRAN Test Register 2

Address				Register
44FH	54FH	64FH	74FH	J2 TRAN Test Register 3
450H	550H	650H	750H	RDLC Test Register 0
451H	551H	651H	751H	RDLC Test Register 1
452H	552H	652H	752H	RDLC Test Register 2
453H	553H	653H	753H	RDLC Test Register 3
454H	554H	654H	754H	RDLC Test Register 4
458H	558H	658H	758H	TDPR Test Register 0
459H	559H	659H	759H	TDPR Test Register 1
45AH	55AH	65AH	75AH	TDPR Test Register 2
45BH	55BH	65BH	75BH	TDPR Test Register 3
490H	590H	690H	790H	TTB Test Register 0
491H	591H	691H	791H	TTB Test Register 1
492H	592H	692H	792H	TTB Test Register 2
498H	598H	698H	798H	RBOC Test Register 0
499H	599H	699H	799H	RBOC Test Register 1
49AH	59AH	69AH	79AH	XBOC Test Register 1
49BH	59BH	69BH	79BH	XBOC Test Register 0
4A0H	5A0H	6A0H	7A0H	PRGD Test Register 0
4A1H	5A1H	6A1H	7A1H	PRGD Test Register 1
4A2H	5A2H	6A2H	7A2H	PRGD Test Register 2
4A3H	5A3H	6A3H	7A3H	PRGD Test Register 3

Notes

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.
2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 400H: S/UNI-4xD3F Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	W	A_TM[9]	X
Bit 5	W	A_TM[8]	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-4xD3F test features. All bits, except PMCTST and A_TM[9:8], are reset to zero by a hardware reset of the S/UNI-4xD3F. The S/UNI-4xD3F Master Test register is not affected by a software reset (via the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update register (006H)).

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-4xD3F. While the HIZIO bit is a logic one, all output pins of the S/UNI-4xD3F except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-4xD3F for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the “Test Mode 0 Details” in the “Test Features” section).

DBCTRL

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-4xD3F to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST

The PMCTST bit is used to configure the S/UNI-4xD3F for PMC Sierra's manufacturing tests. When PMCTST is set to logic one, the S/UNI-4xD3F microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

A_TM[9:8]

The state of the A_TM[9:8] bits internally replace the input address lines A[9:8] respectively when PMCTST is set to logic one. This allows for more efficient use of the PMC manufacturing test vectors.

12.1 JTAG Test Port

The S/UNI-4xD3F JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to section 13.12.

Table 19 Instruction Register

Note: Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 20 Identification Register

Length	Version	Part Number	Manufacturers ID Code	Device ID
32 bits	2H	7346H	0CDH	273460CDH

Table 21 Boundary Scan Register

Note: Length - 198 bits

Pin/Enable	Register Bit	Cell Type	ID Bit	Pin/Enable	Register Bit	Cell Type	ID Bit
VSS	0	I	0	RX_OEB[4]	66	OUT_CELL	(0)
VSS	1		0	TICLK[4;1]	67:70	IN_CELL	(0)
VSS	2		1	TFPI4:1]	71:74	IN_CELL	(0)
VSS	3		0	TDATI[4:1]	75:78	IN_CELL	(0)
VSS	4		0	VSS	79:82		(0)
VSS	5		1	N/C	83:86		(0)
VSS	6		1	TFPO[4:1]	87:90	OUT_CELL	(0)
VSS	7		1	RDATO[4:1]	91:94	OUT_CELL	(0)
VSS	8		0	ROVRHD4:1]	95:98	OUT_CELL	(0)
VSS	9		0	RSCLK[4:1]	99:102	OUT_CELL	(0)
VSS	10		1	REF8KO[4:1]	103:106	OUT_CELL	(0)
VSS	11		1	FRMSTAT[4:1]	107:110	OUT_CELL	(0)
VSS	12		0	REF8KI	111	IN_CELL	(0)
VSS	13		1	ROHCLK[4:1]	112:115	OUT_CELL	(0)
VSS	14		0	ROHFP[4:1]	116:119	OUT_CELL	(0)
VSS	15		0	ROH[4:1]	120:123	OUT_CELL	(0)
VSS	16		0	TOHFP[4:1]	124:127	OUT_CELL	(0)
VSS	17		1	TOHCLK[4:1]	128:131	OUT_CELL	(0)
VSS	18		1	TOHINS[4:1]	132:135	IN_CELL	(0)
VSS	19		0	TOH[4:1]	136:139	IN_CELL	(0)
VSS	20		0	RCLK[4:1]	140:143	IN_CELL	(0)
VSS	21		0	RNEG[4:1]	144;147	IN_CELL	(0)
VSS	22		0	RPOS[4:1]	148:151	IN_CELL	(0)
VSS	23		0	TCLK[4:1]	152:155	OUT_CELL	(0)
VSS	24		1	TNEG[4:1]	156:159	OUT_CELL	(0)
N/C	25		1	TPOS[4:1]	160:163	OUT_CELL	(0)
Reserved	26	OUT_CELL	0	INTB	164	OUT_CELL	(0)
N/C	27		0	RSTB	165	IN_CELL	(0)
N/C	28		1	WRB	166	IN_CELL	(0)
N/C	29		1	RDB	167	IN_CELL	(0)
N/C	30		0	ALE	168	IN_CELL	(0)
VSS	31		1	CSB	169	IN_CELL	(0)
VSS	32		(1)	A[10:0]	170:180	IN_CELL	(0)
VSS	33		(1)	D[7]	181	IO_CELL	(0)
VSS	34		(0)	DOENB [7][5]	182	OUT_CELL	(0)
N/C	35		(0)	D[6]	183	IO_CELL	(0)

Pin/Enable	Register Bit	Cell Type	ID Bit	Pin/Enable	Register Bit	Cell Type	ID Bit
N/C	36		(0)	DOENB[6][5]	184	OUT_CELL	(0)
N/C	37		(0)	D[5]	185	IO_CELL	(0)
N/C	38		(0)	DOENB [5][5]	186	OUT_CELL	(0)
N/C	39		(0)	D[4]	187	IO_CELL	(0)
Reserved	40	OUT_CELL	(0)	DOENB [4][5]	188	OUT_CELL	(0)
N/C	41		(0)	D[3]	189	IO_CELL	(0)
VSS	42		(0)	DOENB [3][5]	190	OUT_CELL	(0)
VSS	43		(0)	D[2]	191	IO_CELL	(0)
VSS	44		(0)	DOENB [2][5]	192	OUT_CELL	(0)
VSS	45		(0)	D[1]	193	IO_CELL	(0)
VSS	46		(0)	DOENB [1][5]	194	OUT_CELL	(0)
VSS	47		(0)	D[0]	195	IO_CELL	(0)
VSS	48		(0)	DOENB [0][5]	196	OUT_CELL	(0)
N/C	49		(0)	HIZ[6]	197	OUT_CELL	(0)
N/C	50:65		(0)				

Notes

1. The DOENB signals will set the corresponding bidirectional signal (the one preceding the DOENB in the boundary scan chain — see note 1 also) to an output when set to logic zero. When set to logic one, the bidirectional signal will be tri-stated.
2. *HIZ* will set all outputs not controlled by RX_OEB and DOENB to tri-state when set to logic one. When set to logic zero, those outputs will be driven.

13 Operation

13.1 Software Initialization Sequence

Using the following software initialization sequence puts the S/UNI-4xD3F in normal power consumption state. PMC-Sierra™ strongly recommends using this reset sequence to guarantee the device's long term reliability.

Note: After a reset, the S/UNI-4xD3F may start using more power than is required. While the device's normal operations are not altered, the excessive power consumption can cause the device to give off high levels of heat, which in turn, could lead to future problems with the device.

To initialize the device:

1. Reset the S/UNI-4xD3F.

2. Set IOTST (bit 2) in the Master Test register to '1' (by writing 00000100 to register 400H).

3. Perform the following series of writes:
   - 00000101 to test register 461H
   - 00000101 to test register 561H
   - 00000101 to test register 661H
   - 00000101 to test register 761H

   - 01000000 to test register 462H
   - 01000000 to test register 562H
   - 01000000 to test register 662H
   - 01000000 to test register 762H
   - 10101010 to test register 463H
   - 10101010 to test register 563H
   - 10101010 to test register 663H
   - 10101010 to test register 763H

   - 00000011 to test register 481H
   - 00000011 to test register 581H
   - 00000011 to test register 681H
   - 00000011 to test register 781H

- 10000000 to test register 480H
- 10000000 to test register 580H
- 10000000 to test register 680H
- 10000000 to test register 780H
- 10101010 to test register 482H
- 10101010 to test register 582H
- 10101010 to test register 682H
- 10101010 to test register 782H

4. Toggle REF8KI (pin T3) signal at least eight times (this provides the clock to the RAM).
5. Set IOTST (bit 2) in the Master Test register to '0' (by writing 00000000 to register 400H).
6. Resume normal device programming.

13.2 Register Settings for Basic Configurations

Table 22 Register Settings for Basic Configurations

Mode of Operation	S/UNI-4xD3F Registers (values in Hexidecimal)														
	x00	x02	x03	x04	x08	x0C	x30	x34	x38	x39	x40	x41	x44	x4C	x9B
T3 C-bit framer only[1]	50	00	00	78	00	00	83	01	--	--	--	--	--	--	01
T3 M23 framer only[1]	50	00	00	78	00	00	82	00	--	--	--	--	--	--	01
E3 G.832 framer only[1]	50	40	40	78	00	00	--	--	04	00	01	01	--	--	01
E3 G.751 framer only[1]	50	40	40	78	00	00	--	--	00	00	00	01	--	--	01
J2 framer only[1]	50	80	80	78	00	00	--	--	--	--	--	--	03	0E	01

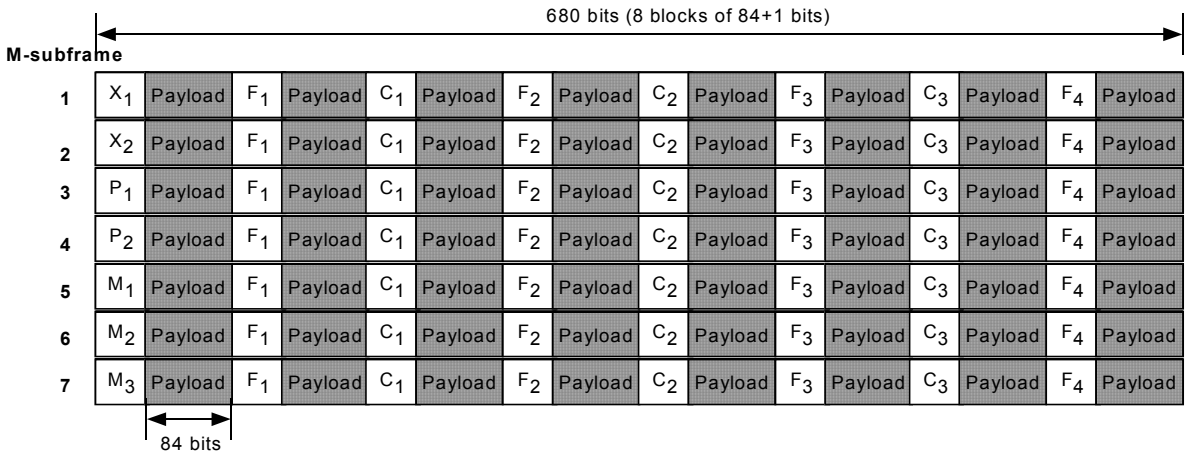
Notes

1. In framer only modes, TGAPCLK[x] and RGAPCLK[x] are enabled by programming register x01H to 0CH.
2. Unipolar mode is selected for DS3, E3, and J2 modes by setting the TUNI bit to logic one in register x02H and the UNI bit in x30H, x38H, and x44H respectively. When the DS3, E3, or J2 framers are bypassed, unipolar mode is selected by default.

13.3 DS3 Frame Format

The S/UNI-4xD3F supports both M23 and C-bit parity DS3 framing formats. An overview of the DS3 frame format is in Figure 5.

Figure 5 DS3 Frame Structure



The DS3 receiver decodes a B3ZS-encoded signal and provides indications of LCVs. The B3ZS decoding algorithm and the LCV definition are software selectable.

While in-frame, the DS3 receiver continuously checks for LCVs, M-bit or F-bit framing bit errors, and P-bit parity errors.

When C-bit parity mode is selected, both C-bit parity errors and FEBEs are accumulated. When the C-bit parity framing format is detected, both the FEAC channel and the PMDL are extracted. HDLC messages in the PMDL are received by an internal data link receiver.

The DS3 transmitter allows for the insertion of the overhead bits into a DS3 bit stream and produces a B3ZS-encoded signal. Status signals such as FERF, AIS, and idle signal can be inserted when the transmission of these signals is enabled

The processing of the overhead bits in the DS3 frame is described in Table 23. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH[x], TOHINS[x], TOHFP[x], and TOHCLK[x] signals. In the receive direction, most of the overhead bits are brought out serially on the ROH[x] data stream.

Table 23 DS3 Frame Overhead Operation

Control Bit	Transmit Operation	Receive Operation
Xx: X-Bit Channel	Inserts the FERF signal on the X-bits.	Monitors and detects changes in the state of the FERF signal on the X-bits.
Px: P-Bit Channel	Calculates the parity for the payload data over the previous M-frame and inserts it into the P1 and P2 bit positions.	Calculates the parity for the received payload. Errors are accumulated in internal registers.
Mx: M-Frame Alignment Signal	Generates the M-frame alignment signal (M1=0, M2=1, M3=0).	Finds the M-frame alignment by searching for the F-bits and the M-bits. OOF is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Fx:	Generates the M-subframe signal (F1=1,	Finds M-frame alignment by searching for

Control Bit	Transmit Operation	Receive Operation
M-subframe Alignment Signal	F2=0, F3=0, F4=1).	the F-bits and the M-bits. OOF is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Cx: C-Bit Channels M23 Operation	In M23 framer-only mode, passed through transparently. This excludes the C-bit Parity ID bit, which toggles every M-frame.	Indicates whether an M23 or C-bit parity format is received. The state of the C-bit parity ID bit is stored in a register.
C-bit Parity Operation	The C-bit Parity ID bit is forced to logic one. The second C-bit in M-subframe 1 is set to logic one. The third C-bit in M-subframe 1 provides a FEAC signal. The FEAC channel is sourced by the XBOC block. The 3 C-bits in M-subframe 3 carry path parity information. The value of these 3 C-bits is the same as that of the P-bits. The 3 C-bits in M-subframe 4 are the FEBE bits. The 3 C-bits in M-subframe 5 contain the 28.2 Kbit/s path maintenance datalink. The remaining C-bits are unused and set to logic one.	The FEAC channel on the third C-bit in M-subframe 1 is detected by the RBOC block. Path parity errors and FEBEs on the C-bits in M-subframes 3 and 4 are accumulated in counters. The PMDL signal is extracted by the receive HDLC controller.

13.4 G.751 E3 Frame Format

The S/UNI-4xD3F provides support for the G.751 E3 frame format, shown in Figure 6.

Figure 6 G.751 E3 Frame Structure

The processing of the overhead bits in the G.751 E3 frame is described in Table 24. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user-supplied data stream using the TOH[x], TOHINS[x], TOHFP[x], and TOHCLK[x] signals. In the receive direction, most of the overhead bits are brought out serially on the ROH[x] data stream.

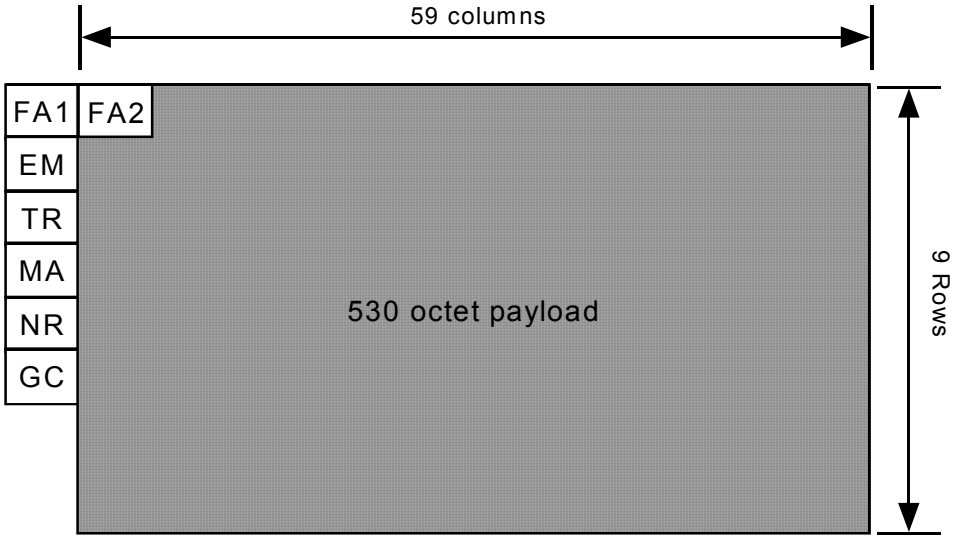
Table 24 G.751 E3 Frame Overhead Operation

Control Bit	Transmit Operation	Receive Operation
Frame Alignment Signal	Inserts the frame alignment signal 1111010000b.	Finds frame alignment by searching for the frame alignment signal. When the pattern has been detected for three consecutive frames, an in-frame condition is declared. When errors are detected in four consecutive frames, an OOF condition is declared.
RAI: RAI	Optionally asserts the RAI signal under a register control or when LOS, OOF, AIS and LCD conditions are detected.	Extracts the RAI signal and outputs it on the ROH output pin. The state of the RAI signal is also written to a register bit.
Na: National Use Bit	Asserts the National Use bit under a register control or from the internal HDLC controller.	Extracts the National Use bit and stores the value in a register bit.
Cjk: Justification Service Bits	When the device is configured as an E3 G.751 framer device, can be inserted on the TDATI[x] input pin the same way as normal payload data.	Extracts the Justification Service Bits on the ROH output pin when they are configured as overhead.
Jk: Tributary Justification Bits	When the device is configured as a E3 G.751 framer, can be inserted on the TDATI[x] input pin the same way as normal payload data.	Extracts the Tributary Justification Bits on the ROH output pin when they are configured as overhead.

13.5 G.832 E3 Frame Format

The S/UNI-4xD3F provides support for the G.832 E3 frame format. The G.832 E3 frame format is shown in Figure 7.

Figure 7 G.832 E3 Frame Structure



The processing of the overhead bits in the G.832 E3 frame is described in Table 25. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH[x], TOHINS[x], TOHFP[x], and TOHCLK[x] signals. In the receive direction, the overhead bits are brought out serially on the ROH[x] data stream.

Table 25 G.832 E3 Frame Overhead Operation

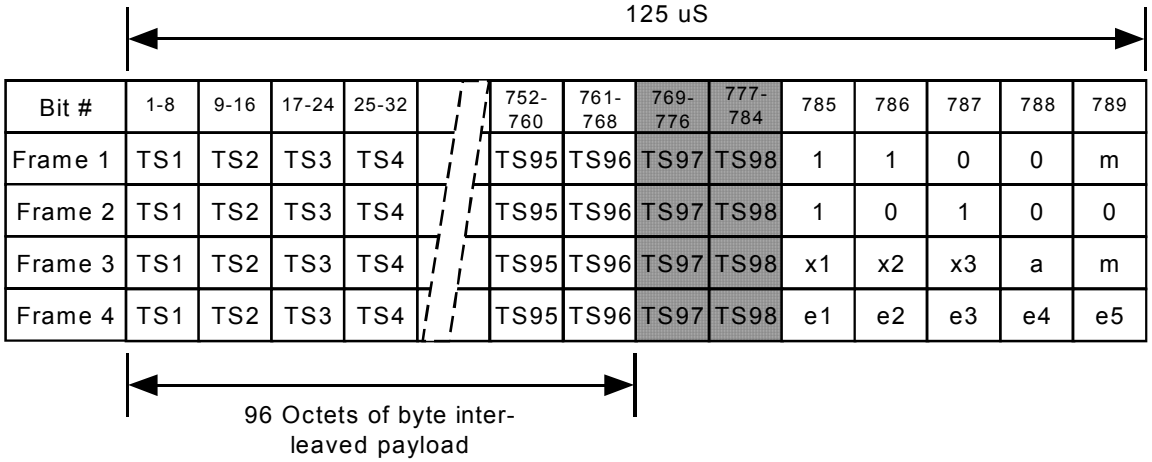
Control	Transmit Operation	Receive Operation
FA1, FA2: Frame Alignment Pattern	Inserts the G.832 E3 frame alignment pattern (F628H).	Searches the receive stream for the G.832 E3 frame alignment pattern. When the pattern is detected for two consecutive frames, an in-frame condition is declared.
EM: Error Monitor, BIP-8	Inserts the calculated BIP-8 by computing even parity over all transmit bits, including the overhead bits of the previous 125 µs frame.	Computes the incoming BIP-8 value over one 125 µs frame. The result is held and compared against the value in the EM byte of the subsequent frame.
TR: Trail Trace	Inserts the 16-byte trail access point identifier specified in internal registers.	Extracts the repetitive trail access point identifier and verifies that the same pattern is received. Compares the received pattern to the expected pattern programmed in a register.

Control	Transmit Operation	Receive Operation
MA: Maintenance and Adaptation Byte	Inserts the FERF, FEBE, Payload Type bits, Tributary Unit Multiframe Indicator bits and the Timing Marker bit as programmed in a register or as indicated by detection of receive OOF or BIP-8 errors.	Extracts and reports the FERF-bit value when it has been the same for three or five consecutive frames. Also extracts and accumulates FEBE occurrences and extracts the Payload Type, Tributary Unit Multiframe, and Timing Market indicator bits and reports them through microprocessor-accessible registers.
NR: Network Operator Byte	Inserts the Network Operator byte from the TOH overhead stream or optionally from the TDPR. All eight bits of the Network Operator byte are inserted from TOH or from the TDPR.	Extracts the Network Operator byte and outputs it on ROH or optionally terminates it in the RDLC. All eight bits of the Network Operator byte are extracted and presented on ROH or to the RDLC.
GC: General Purpose Communication Channel	Inserts the GC byte from the TOH overhead stream or optionally from the TDPR block.	Extracts the GC byte and outputs it on ROH or optionally terminates it in the RDLC block.

13.6 J2 Frame Format

The S/UNI-4xD3F provides support for the G.704 and NTT J2 frame format. The J2 frame format consists of 789 bits frames each 125 us long, consisting of 96 bytes of payload, two reserved bytes, and five F-bits. The frames are grouped into five frame multiframes as shown in Figure 8.

Figure 8 J2 Frame Structure



The J2 framer decodes a unipolar or B8ZS encoded signal and frames to the resulting 6,312 Kbit/s J2 bit stream. Once in frame, the J2 framer provides indications of frame and multiframe boundaries and marks overhead bits, x-bits, m-bits and reserved channels (TS97 and TS98). Indications of LOS, bipolar violations, excessive zeroes, change of frame alignment, framing errors, and CRC errors are provided and accumulated in internal counters.

The J2 transmitter inserts the overhead bits into a J2 bit stream and produces a B8ZS-encoded signal. The J2 transmitter adheres to the framing format specified in G.704 and the NTT Technical Reference for High Speed Digital Leased Circuit Services.

The processing of the overhead bits in the J2 frame is described in Table 26. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data using the TOH[x], TOHINS[x], TOHFP[x], and TOHCLK[x] signals. In the receive direction, the overhead bits are brought out serially on the ROH[x] data stream.

Table 26 J2 Frame Overhead Operation

Control	Transmit Operation	Receive Operation
TS97-TS98: Signaling channels	Inserts the signaling bytes from either register bits or from the TOH and TOHINS inputs. These bits can be optionally inserted via TDATI input when in-frame only.	Extracts signaling bytes on the ROH output.
Frame Alignment Signal	Inserts the frame alignment signal automatically.	Finds J2 frame alignment by searching for the frame alignment signal.
M-bits: 4kHz Data Link	Inserts the 4 KHz data link signal from the internal HDLC controller or from the bit oriented code generator.	Extracts the 4 KHz data link signal for the internal HDLC controller.
X-bits: Spare Bits	Inserts the spare bits via register bits or via TOH and TOHINS input pins.	Extracts and presents the x-bits on register bits. The X-bit states can be debounced and presented on the ROH output pin. An interrupt change can be generated to signal a change in the X-bit state.
A-bit: Remote LOF Indication	Inserts the A-bit via register bit. The A-bit can be optionally be asserted when the J2 framer is in LOF condition.	Extracts and presents the A-bit on a register bit. The A-bit state can be debounced and presented on the ROH output pin. An interrupt can be generated to signal a change in the A-bit state.
E1-E5: CRC-5 Check Sequence	Automatically calculates and inserts the CRC-5 check sequence.	Calculates the CRC-5 check sequence for the received data stream. Discrepancies with the received CRC-5 code can be configured to generate an interrupt. CRC-5 errors are accumulated in an internal counter.

13.7 Servicing Interrupts

The S/UNI-4xD3F will assert INTB to logic zero when a condition that is configured to produce an interrupt occurs. To determine the condition that caused this interrupt to occur, use the procedure that follows:

1. Read the INT[4:1] bits of the S/UNI-4xD3F Clock Activity Monitor and Interrupt Identification register (007H) to identify which quadrant of the S/UNI-4xD3F produced the interrupt. For example, a logic one on the INT[3] register bit indicates that quadrant number 3 of the S/UNI-4xD3F produced the interrupt.

2. Having identified the quadrant which produced the interrupt, read the S/UNI-4xD3F Interrupt Status register (005H, 105H, 205H, and 305H) to identify which block in the quadrant produced the interrupt. For example, a logic one on the TDPRI register bit in register 205H indicates that the TDPR block in quadrant number 3 of the S/UNI-4xD3F produced the interrupt.

3. Service the interrupt.

4. If the INTB pin is still logic zero, then there are still interrupts to be serviced. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

13.8 Using the Performance Monitoring Features

The PMON block is provided for performance monitoring purposes. The PMON block monitors DS3, E3, and J2 performance primitives. The counters have been sized not to saturate if polled every second in the PMON block.

Primitives for DS3, E3, and J2 are accumulated independently of the cell-based primitives. The accumulation interval is initiated by writing to one of the PMON event counter registers. After this is done, a number of RCLK clock periods (three for J2 mode, 255 for DS3 mode, 500 for G.832 E3 mode, and three for G.751 E3 mode) must be allowed to elapse for the PMON counter values to be properly transferred and then read.

A write to the S/UNI-4xD3F Identification, Master Reset, and Global Monitor Update registers causes the PMON counter to latch and a new accumulation period to start in all four quadrants of the device. A maximum of 67 RCLK[x] clock periods must be allowed to elapse for the event count registers to be properly transferred.

13.9 Using the TDPR Internal PMDL Transmitter

The access rate to the TDPR registers is limited by the rate of the internal high-speed system clock selected by the LINESYSCLK register bit of the S/UNI-4xD3F Miscellaneous register (09BH, 19BH, 29BH, 39BH). Consecutive accesses to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data registers should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 1/8 that of the selected TDPR high-speed system clock. This time is used by the high-speed system clock to sample the event, write the FIFO, and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (for example, jitter in the line clock) must be considered when determining the procedure used to read and write the TDPR registers.

Upon reset of the S/UNI-4xD3F, the TDPR should be disabled by setting the EN-bit in the TDPR Configuration register to its default of logic zero. An HDLC all-ones idle signal will be sent while in this state.

Initialize the TDPR by setting the TDPR Configuration register:

1. If FCS generation is desired, set the CRC bit to logic one.

2. If the block is to be used in interrupt driven mode, then enable interrupts by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable register to logic one.

3. Set the TDPR operating parameters in the TDPR Upper and Lower Transmit Threshold registers to the desired values. Setting the TDPR Upper Transmit Threshold value will set the value at which the TDPR will automatically begin the transmission of HDLC packets even if no complete packets are in the FIFO. Transmission will continue until the current packet is transmitted and the number of bytes the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC packets (packets with EOM attached) in its FIFO.

4. Set the EN-bit to logic one to enable the TDPR can be enabled by setting the EN-bit to logic one. If no message is sent after the EN-bit is set to logic one, continuous flags will be sent.

5. Set and clear the FIFOCLR bit to initialize the TDPR FIFO.

The TDPR can be used in a polled- or interrupt-driven mode for data transfer to determine when writes can or must be done to the TDPR Transmit Data register. In the polled mode, the processor controlling the TDPR must periodically read the TDPR Interrupt Status register. In the interrupt-driven mode, the processor controlling the TDPR uses the INTB output, the S/UNI-4xD3F Clock Activity Monitor and Interrupt Identification register, and the S/UNI-4xD3F Interrupt Status register to identify TDPR interrupts.

13.9.1 TDPR Polling Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic one so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic zero since packet transmission is set to work with a periodic polling procedure.

To transmit HDLC packets in polling mode:

1. Wait until data is available to be transmitted, then go to step 2.

2. Read the TDPR Interrupt Status register.

   If FULL=1, then the TDPR FIFO is full and no further bytes can be written. Continue polling the TDPR Interrupt Status register until either FULL=0 or BLFILL=1. Then, go to either step c or d depending on your implementation preference.

   If BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data register. Go to step e.

   If FULL=0, then the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data register. Go to step e.

If more data bytes are to be transmitted in the packet, then go to step b.

If all bytes in the packet have been sent, then set the EOM-bit in the TDPR Configuration register to logic one. Go to step a.

13.9.2 TDPR Interrupt-driven Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold.

The CRC bit can be set to logic one so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to a value that will give sufficient warning of an underrun. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic one so an interrupt on INTB is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun.

Use the following procedure to transmit HDLC packets in the interrupt-driven mode:

1. Wait for data to be transmitted. Once data is available to be transmitted, then go to step 2.

2. Write the data byte to the TDPR Transmit Data register.

3. If all bytes in the packet have been sent, then set the EOM-bit in the TDPR Configuration register to logic one. Go to step 1.

If there are more bytes in the packet to be sent, then go to step 2.

While performing steps 1 to 3, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine, described in the following section, should be immediately followed.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold register. Unless an error condition occurs, transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

13.9.3 TDPR Interrupt Routine

Upon assertion of INTB, the source of the interrupt must first be identified by reading the S/UNI-4xD3F Clock Activity Monitor and Interrupt Identification register (007H) and the S/UNI-4xD3F Interrupt Status registers (005H, 105H, 205H, 305H).

Once the source of the interrupt has been identified as TDPR, the following procedure must be done:

1. Read the TDPR Interrupt Status register.

2. If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic one, one abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. To re-enable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear register should be written with any value.

   If OVRI=1, then the FIFO has overflowed. The packet for the last byte written into the FIFO has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. Either a timer can be used to determine when sufficient bytes are available in the FIFO or you may wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit. If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes), the OVRI is set, an abort signal is scheduled to be transmitted. The FIFO is emptied and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data register occurs. This write contains the first byte of the next packet to be transmitted.

   If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either use a timer to determine when sufficient bytes are available in the FIFO or wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

   If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, write it to the TDPR Transmit Data register before an underrun occurs. If there is no more data to transmit, then set an EOM at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

   If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

13.10 Using the RDLC Internal Data Link Receiver

The access rate to the RDLC registers is limited by the rate of the internal high-speed system clock selected by the LINESYSCLK register bit of the S/UNI-4xD3F Miscellaneous registers (09BH, 19BH, 29BH, 39BH). Consecutive accesses to the RDLC Status and RDLC Data registers should be accessed at a rate no faster than 1/10 that of the selected RDLC high-speed system clock. This time is used by the high-speed system clock to sample the event and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (for example, jitter in the receive line clock) must be considered when determining the procedure used to read RDLC registers.

Upon system power-up, the RDLC should be disabled by setting the EN-bit in the Configuration register to its default of logic zero. The RDLC Interrupt Control register should then be initialized to enable the INT output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic one, the RDLC Status register must be continuously polled to check the interrupt status (INTR) bit. After a write to the RDLC Interrupt Control register, the RDLC can be enabled at any time by setting the EN-bit in the RDLC Configuration register to logic one.

When the RDLC is enabled, it assumes the link status is idle (all-ones) and immediately begins searching for flags. When the first flag is found, an interrupt is generated and a dummy byte is written into the FIFO buffer, which provides alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO, which provides alignment of link down status with the data read from the FIFO. The controlling processor must check the COLS bit in the RDLC Status register for a change in the link status. If the COLS bit is set to logic one, the FIFO must be emptied to determine the current link status. Note: The first flag and abort status encoded in the PBS bits are used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register is being read the PKIN-bit will be logic one. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register is read, the PKIN-bit is cleared to logic zero. If this register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic one and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt-driven mode to determine when to read the RDLC Data register for the transfer of frame data. In the polled mode, the processor controlling the RDLC must periodically read the RDLC Status register. In the interrupt-driven mode, the processor controlling the RDLC uses the S/UNI-4xD3F INTB output, the S/UNI-4xD3F Clock Activity Monitor and Interrupt Identification register, and the S/UNI-4xD3F Interrupt Status registers.

13.10.1 RDLC Interrupt-driven Mode

In an interrupt-driven data transfer from the RDLC to the processor, the INTB output of the S/UNI-4xD3F is connected to the interrupt input of the processor. The processor interrupt service routine verifies what block generated the interrupt by reading the S/UNI-4xD3F Clock Activity Monitor and Interrupt Identification register, and the S/UNI-4xD3F Interrupt Status registers. Once it has identified that the RDLC has generated the interrupt, it processes the data in the following order:

1. Reads the RDLC Status register. The INTR bit should be logic one.

    a) If OVR = 1, then discards last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

If COLS = 1, then sets the EMPTY FIFO software flag.

If PKIN = 1, increments the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

2. Reads the RDLC Data register.

3. Reads the RDLC Status register.
   - If OVR = 1, then discards last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.
   - If COLS = 1, then sets the EMPTY FIFO software flag.
   - If PKIN = 1, increments the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

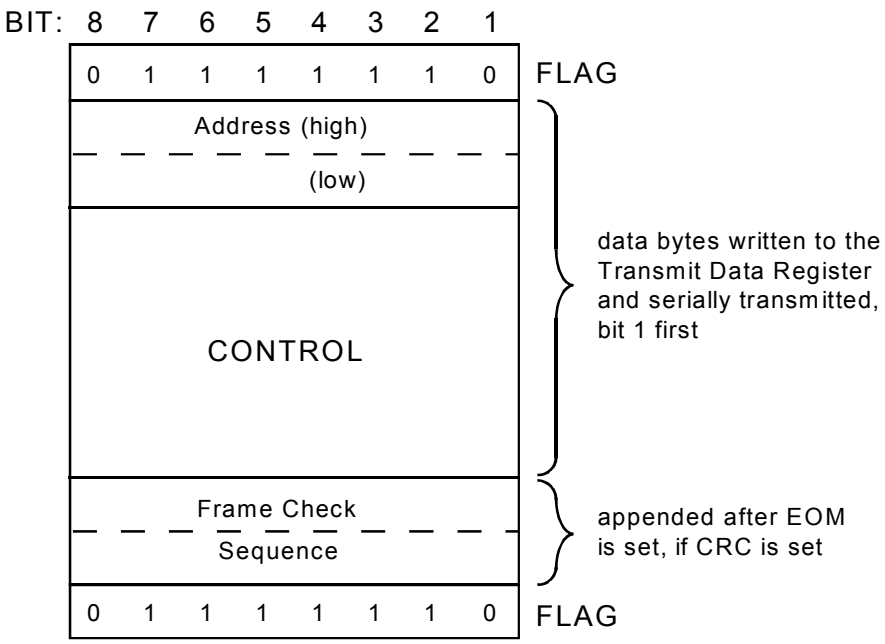
4. Starts the processing of FIFO data. Uses the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.
   - If PBS[2:0] = 001, discards data byte read in step 3 and sets the LINK ACTIVE software flag.
   - If PBS[2:0] = 010, discards the data byte read in step 3 and clears the LINK ACTIVE software flag.
   - If PBS[2:0] = 1XX, stores the last byte of the packet, decrements the PACKET COUNT, and checks the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.
   - If PBS[2:0] = 000, stores the packet data.
   - If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, goes to step 3 or else clears the EMPTY FIFO software flag and leaves this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all-ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

13.10.2 RDLC Polled Mode

If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

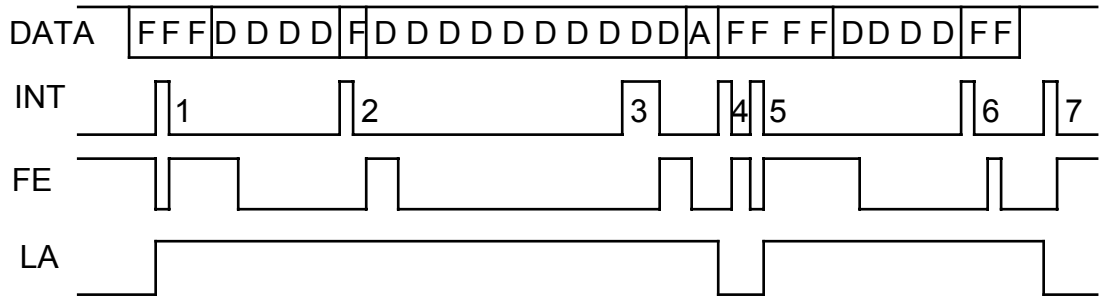
Figure 9 Typical Data Frame



Bit 1 is the first serial bit to be received. When enabled, the primary, secondary and universal addresses are compared with the high order packet address to determine a match.

Figure 10 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence. The cause of each interrupt and the processing required at each point is described in the following paragraphs.

Figure 10 Example Multi-Packet Operational Sequence



Notes

1. *F* is the flag sequence (01111110).
2. *A* is the abort sequence (01111111).
3. *D* is the packet data bytes.
4. *INT* is the active high interrupt output.
5. *FE* is the internal FIFO empty status.

6. *LA* is the state of the LINK ACTIVE software flag.

At points 1 and 5 the first flag after all-ones or abort is detected. A dummy byte is written in the FIFO, FE goes low, and an interrupt goes high. When the interrupt is detected by the processor it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed. The LINK ACTIVE (LA) software flag is set to logic one.

At points 2 and 6 the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor, it reads the data and status registers until the FIFO becomes empty. The interrupt is removed as soon as the RDLC Status register is read since the FIFO fill level of 8 bytes has not been exceeded. It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO. The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3 the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

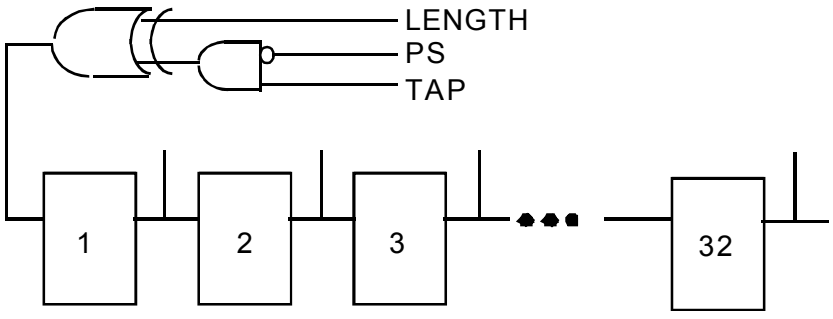
At points 4 or 7 an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed. The LINK ACTIVE software flag is cleared.

13.11 PRGD Pattern Generation

A pseudo-random or repetitive pattern is inserted or extracted in the DS3, E3, J2, or Arbitrary framing format payload.

The pattern generator can be configured to generate pseudo random patterns or repetitive patterns as shown in Figure 11:

Figure 11 PRGD Pattern Generator



The pattern generator consists of a 32-bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0], when the PS bit is low). When PS is high, the pattern detector functions as a re-circulating shift register, with length determined by PL[4:0].

13.11.1 Generating and Detecting Repetitive Patterns with PRGD

When a repetitive pattern (such as 1-in-8) is to be generated or detected, the PS bit must be set to logic one and the pattern length register must be set to (N-1), where N is the length of the desired repetitive pattern. Refer to section 13.11.2 for examples of programming common repetitive sequences.

For pattern generation, the desired pattern must be written into the PRGD Pattern Insertion registers. The repetitive pattern will then be continuously generated and the generated pattern will be inserted in the output data stream. Note: The phase of the pattern cannot be guaranteed.

For pattern detection, the PRGD will determine if a repetitive pattern of the length specified in the pattern length register exists in the input stream. It does so by loading the first N-bits from the data stream, and then monitoring to see if the pattern loaded repeats itself error free for the subsequent 48-bit periods. It will repeat this process until it finds a repetitive pattern of length N, at which point it begins counting errors (and possibly re-synchronizing) in the same way as for pseudo-random sequences.

Note: The PRGD does *not* look for the pattern loaded into the Pattern Insertion registers, but rather automatically detects any repetitive pattern of the specified length. The precise pattern detected can be determined by initiating a PRGD update, setting PDR[1:0] = 00 in the PRGD Control register, and reading the Pattern Detector registers, which will then contain the 32 bits detected immediately prior to the strobe.

13.11.2 Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T O.151. The register configurations required to generate these patterns and others are indicated in the Table 27 and Table 28.

Table 27 Pseudo Random Pattern Generation (PS bit = 0)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
$2^3 - 1$	00	02	FF	FF	FF	FF	0	0
$2^4 - 1$	00	03	FF	FF	FF	FF	0	0
$2^5 - 1$	01	04	FF	FF	FF	FF	0	0
$2^6 - 1$	04	05	FF	FF	FF	FF	0	0
$2^7 - 1$	00	06	FF	FF	FF	FF	0	0
$2^7 - 1$ (Fractional T1 LB Activate)	03	06	FF	FF	FF	FF	0	0
$2^7 - 1$ (Fractional T1 LB Deactivate)	03	06	FF	FF	FF	FF	1	1

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
2^9 -1 (O.153)	04	08	FF	FF	FF	FF	0	0
2^{10} -1	02	09	FF	FF	FF	FF	0	0
2^{11} -1 (O.152, O.153)	08	0A	FF	FF	FF	FF	0	0
2^{15} -1 (O.151)	0D	0E	FF	FF	FF	FF	1	1
2^{17} -1	02	10	FF	FF	FF	FF	0	0
2^{18} -1	06	11	FF	FF	FF	FF	0	0
2^{20} -1 (O.153)	02	13	FF	FF	FF	FF	0	0
2^{20} -1 (O.151 QRSS bit=1)	10	13	FF	FF	FF	FF	0	0
2^{21} -1	01	14	FF	FF	FF	FF	0	0
2^{22} -1	00	15	FF	FF	FF	FF	0	0
2^{23} -1 (O.151)	11	16	FF	FF	FF	FF	1	1
2^{25} -1	02	18	FF	FF	FF	FF	0	0
2^{28} -1	02	1B	FF	FF	FF	FF	0	0
2^{29} -1	01	1C	FF	FF	FF	FF	0	0
2^{31} -1	02	1E	FF	FF	FF	FF	0	0

Table 28 Repetitive Pattern Generation (PS bit = 1)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
All-ones	00	00	FF	FF	FF	FF	0	0
All-zeros	00	00	FE	FF	FF	FF	0	0
Alternating ones/zeros	00	01	FE	FF	FF	FF	0	0
Double alternating ones/zeros	00	03	FC	FF	FF	FF	0	0
3 in 24	00	17	22	00	20	FF	0	0
1 in 16	00	0F	01	00	FF	FF	0	0
1 in 8	00	07	01	FF	FF	FF	0	0
1 in 4	00	03	F1	FF	FF	FF	0	0
Inband loopback activate	00	04	F0	FF	FF	FF	0	0
Inband loopback deactivate	00	02	FC	FF	FF	FF	0	0

Notes (For the Pseudo Random and Repetitive Pattern Generation Tables)

1. The PS bit and the QRSS bit are contained in the PRGD Control register
2. *TR* is the PRGD Tap register
3. *LR* is the PRGD Length register
4. *IR#1* is the PRGD Pattern Insertion #1 register
5. *IR#2* is the PRGD Pattern Insertion #2 register
6. *IR#3* is the PRGD Pattern Insertion #3 register
7. *IR#4* is the PRGD Pattern Insertion #4 register

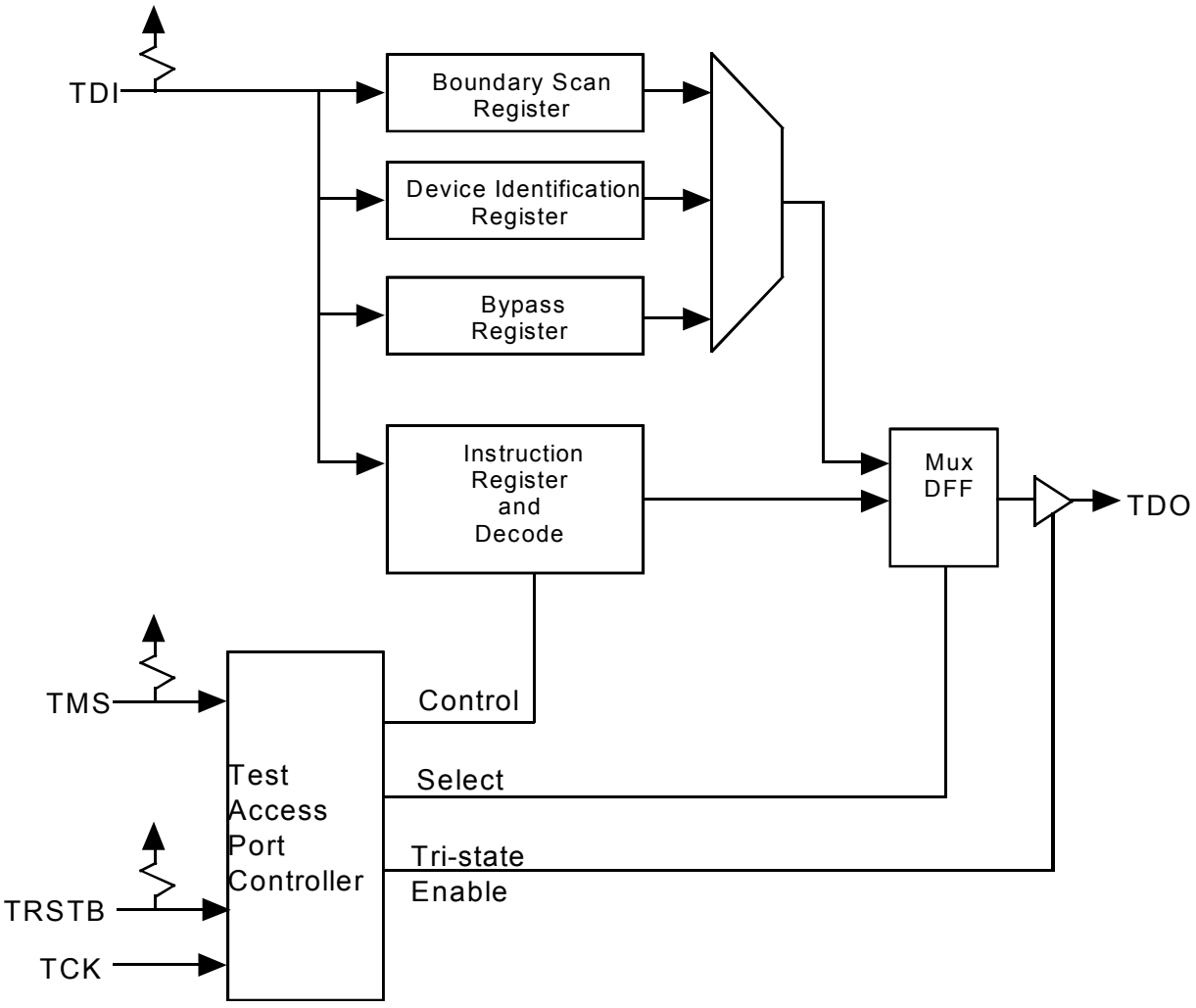
8. The TINV bit and the RINV bit are contained in the PRGD Control register

13.12 JTAG Support

The S/UNI-4xD3F supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The TAP consists of the five standard pins (TRSTB, TCK, TMS, TDI, and TDO) used to control the TAP controller and the boundary scan registers.

The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 12.

Figure 12 Boundary Scan Architecture



The boundary scan architecture consists of:

- A TAP controller
- An instruction register with instruction decode
- A bypass register
- A device identification register
- A boundary scan register

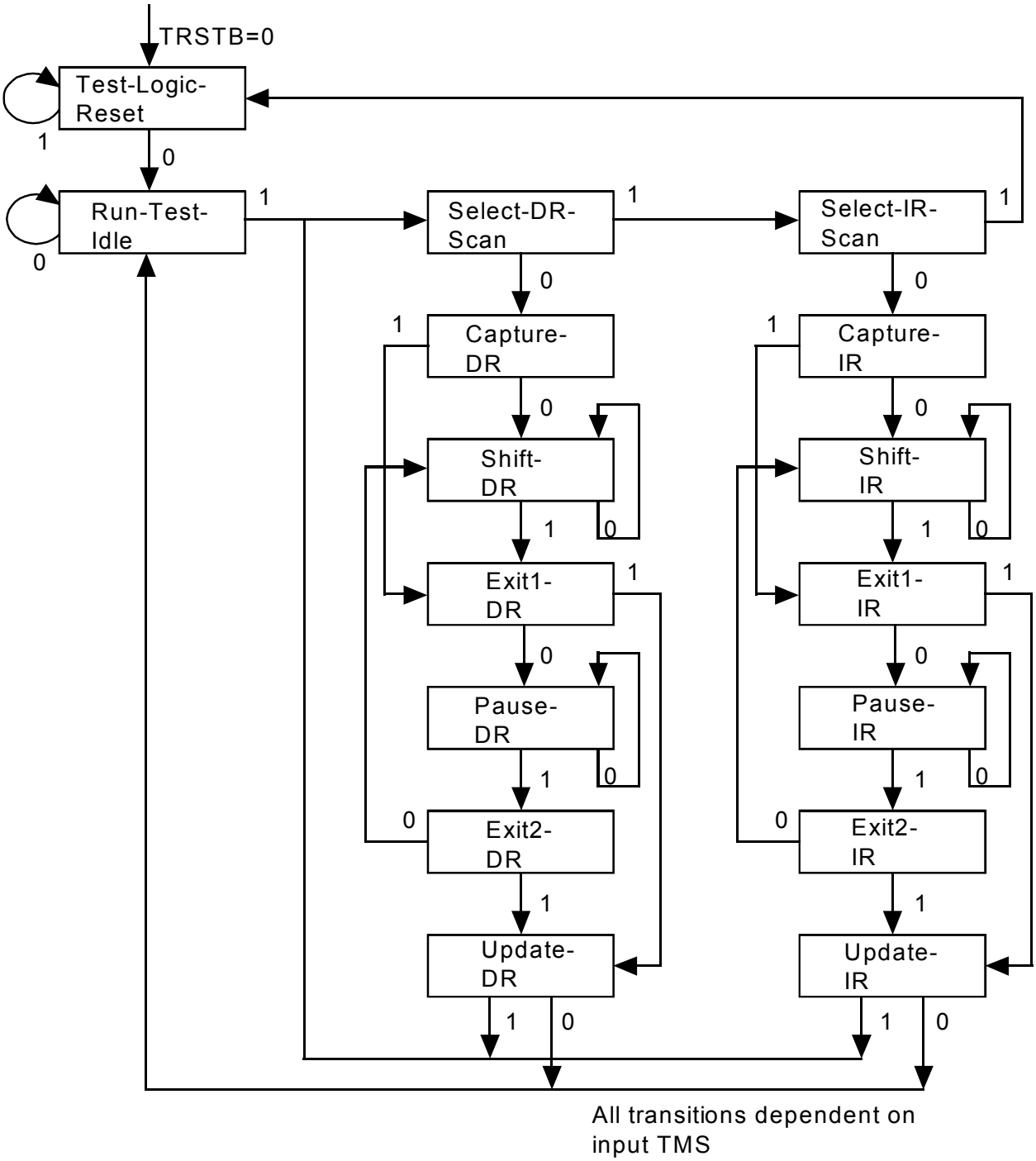
The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.12.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is shown in Figure 13.

Figure 13 TAP Controller Finite State Machine



Notes

1. *Test-Logic-Reset* is the state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for five TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

2. *Run-Test-Idle* is used to execute tests.
3. *Capture-DR* is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.
4. *Shift-DR* is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.
5. *Update-DR* is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.
6. *Capture IR* is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.
7. *Shift-IR* is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.
8. *Update-IR* is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.
9. *Pause-DR* and *Pause-IR* are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

13.12.2 Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

The bypass instruction (BYPASS) shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

The external test instruction (EXTEST) allows interconnection testing with other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs are sampled by loading the boundary scan register using the Capture-DR state. The sampled values are then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs are controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

The sample instruction (SAMPLE) samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs are sampled by loading the boundary scan register using the Capture-DR state. The sampled values are then viewed by shifting the boundary scan register using the Shift-DR state.

The identification instruction (IDCODE) is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

The single transport chain instruction (STCTEST) is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13.12.3 Boundary Scan Cell Description

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan register table located in section 12.1.

Figure 14 Input Observation Cell (IN_CELL)

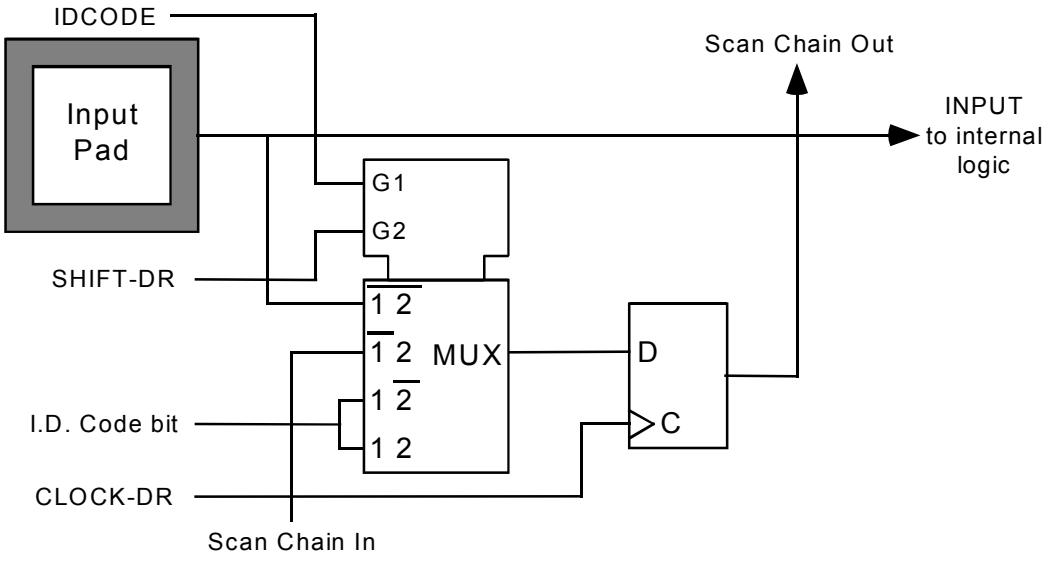


Figure 15 Output Cell (OUT_CELL)

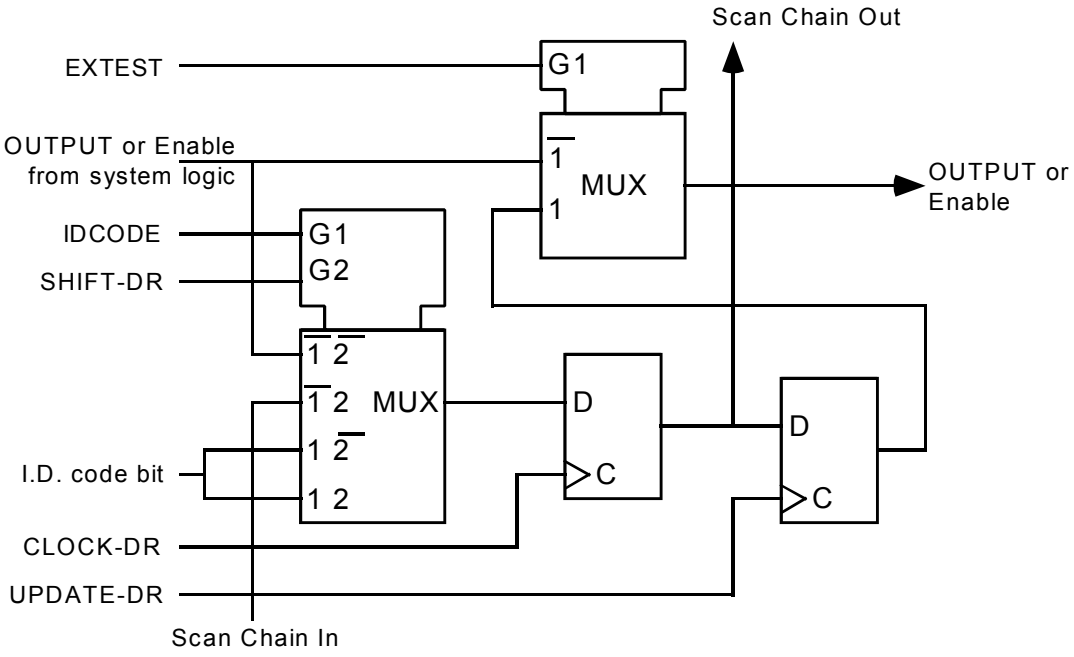


Figure 16 Bi-directional Cell (IO_CELL)

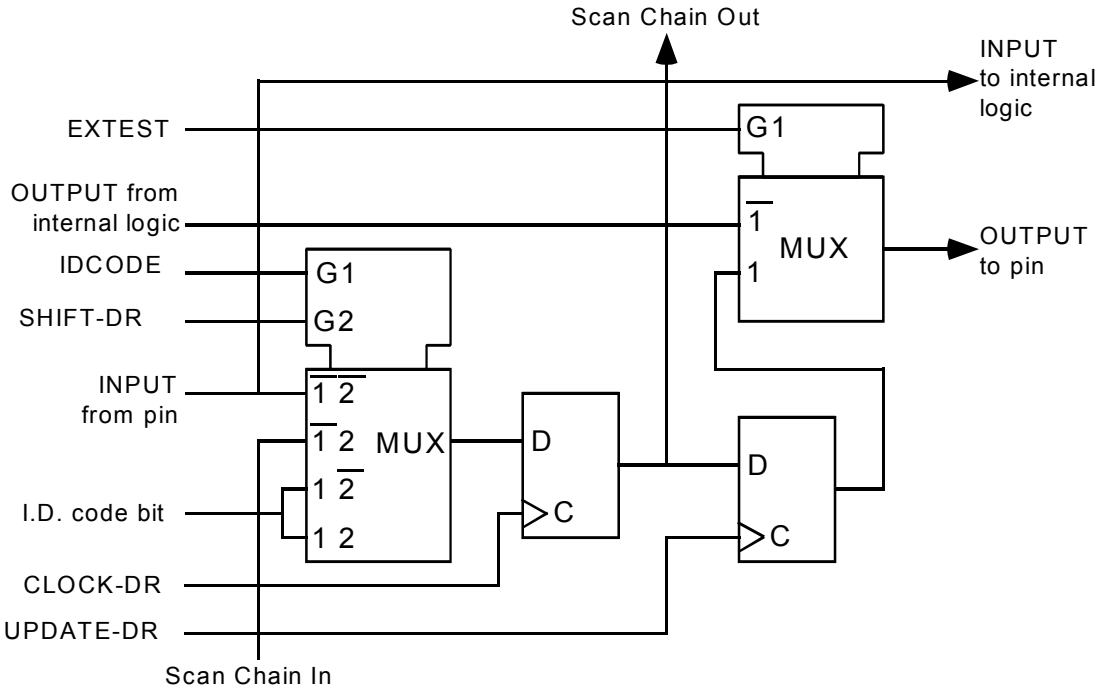
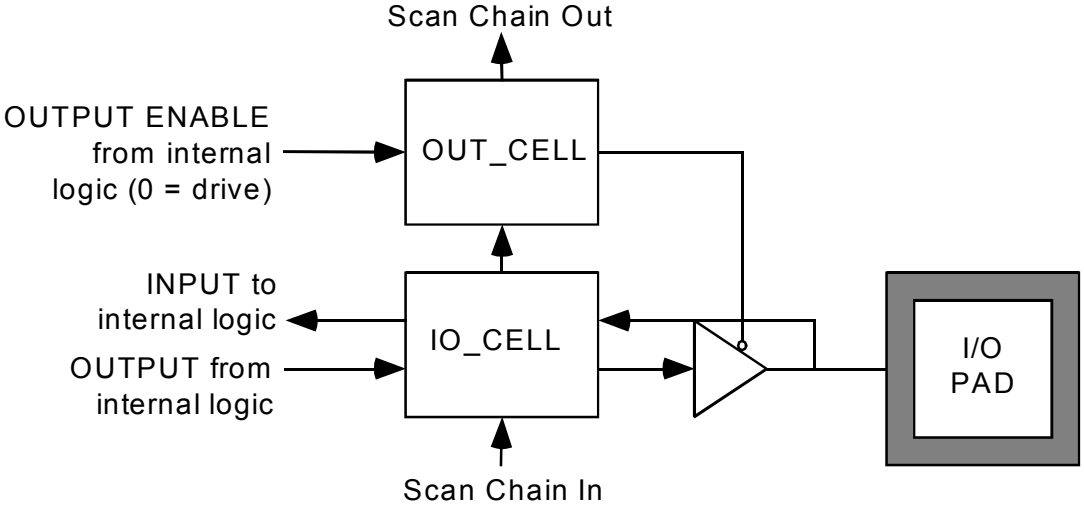


Figure 17 Layout of Output Enable and Bi-directional Cells

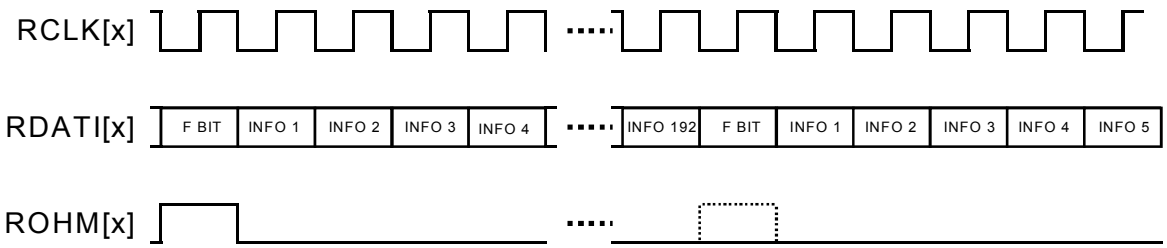


14 Functional Timing

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines. That is, polarity control bits in the S/UNI-4xD3F registers are set to their default states.

The Receive DS1 Stream diagram shown in Figure 18 illustrates the expected DS1 overhead indicators on ROHM[x] when the S/UNI-4xD3F is configured for DS1 direct-mapped frame formats. Frame pulses on ROHM[x] are not required to be present. Once internally synchronized by a pulse on ROHM[x], the S/UNI-4xD3F can use its internal timeslot counter for DS1 overhead bit identification. The ATM cell stream is contained in RDATI[x], along with a framing bit placeholder every 193 bit periods. An upstream DS1 framer (such as the PM4341A T1XC or PM4344 TQUAD) must be used to identify the DS1 framing bit position.

Figure 18 Receive DS1 Stream



The expected Receive E1 Stream for direct-mapped applications is shown in Figure 19. Frame pulses on ROHM[x] are not required to be present every frame. Once internally synchronized by a pulse on ROHM[x], the S/UNI-4xD3F can use its internal timeslot counter for E1 overhead bit identification. The ATM cell stream is contained in RDATI[x], along with a framing bit placeholder every 256 bit periods. An upstream E1 framer (such as the PM6341A E1XC or PM6344 EQUAD) must be used to identify the E1 framing bit position.

Figure 19 Receive E1 Stream

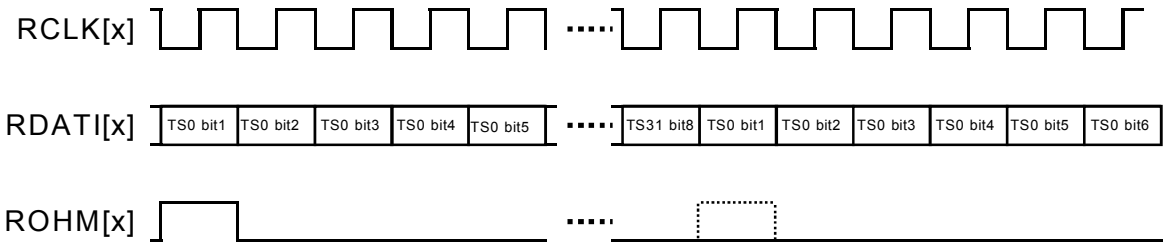


Figure 20, the Receive Bipolar DS3 Stream, shows the operation of the S/UNI-4xD3F while processing a B3ZS encoded DS3 stream on inputs RPOS[x] and RNEG[x]. It is assumed that the first bipolar violation (on RNEG[x]) illustrated corresponds to a valid B3ZS signature. A LCV is declared upon detection of three consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid B3ZS signature.

Figure 20 Receive Bipolar DS3 Stream

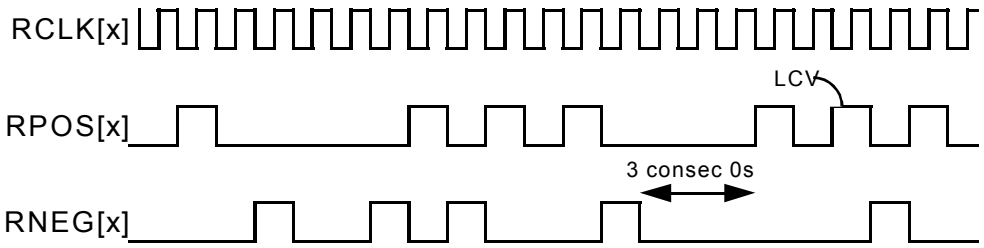


Figure 21, the Receive Unipolar DS3 Stream diagram, shows the complete DS3 receive signal on the RDATI[x] input. LCV indications, detected by an upstream B3ZS decoder, are indicated on input RLCV[x]. RLCV[x] is sampled each bit period. The PMON LCV Event Counter is incremented each time a logic one is sampled on RLCV[x].

Figure 21 Receive Unipolar DS3 Stream

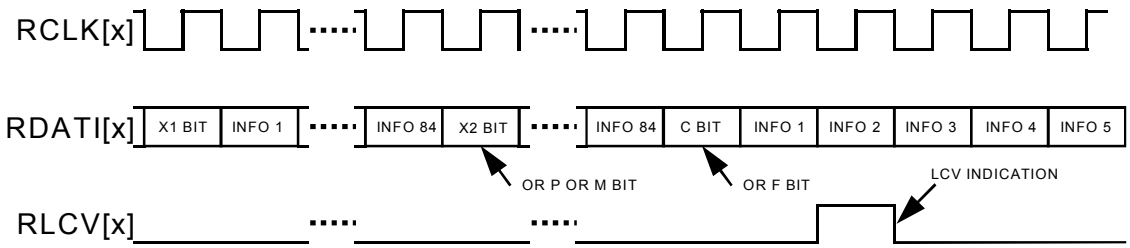


Figure 22, the Receive Bipolar E3 Stream diagram, shows the operation of the S/UNI-4xD3F while processing an HDB3-encoded E3 stream on inputs RPOS[x] and RNEG[x]. It is assumed that the first bipolar violation (on RNEG[x]) illustrated corresponds to a valid HDB3 signature. A LCV is declared upon detection of four consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid HDB3 signature.

Figure 22 Receive Bipolar E3 Stream

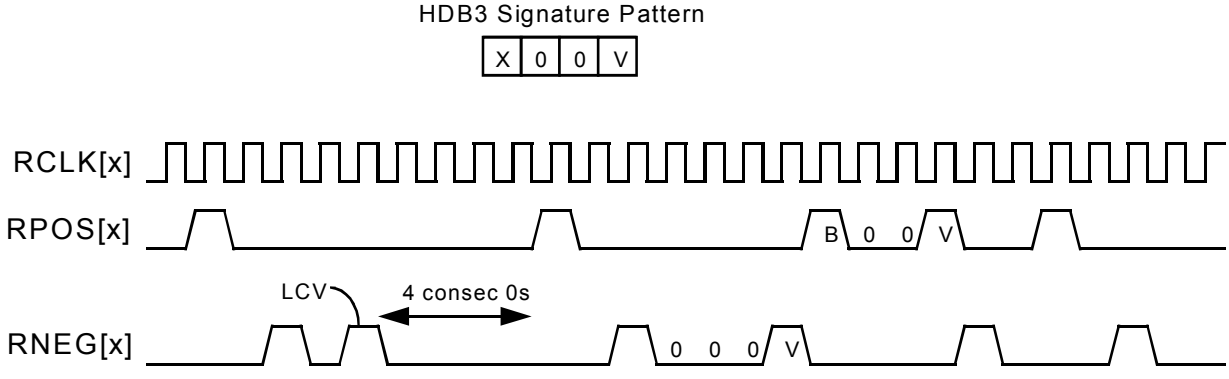


Figure 23, the Receive Unipolar E3 Stream diagram, shows the unipolar E3 receive signal on the RDATI[x] input. LCV indications, detected by an upstream HDB3 decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON LCV Event Counter is incremented each time a logic one is sampled on RLCV.

Figure 23 Receive Unipolar E3 Stream

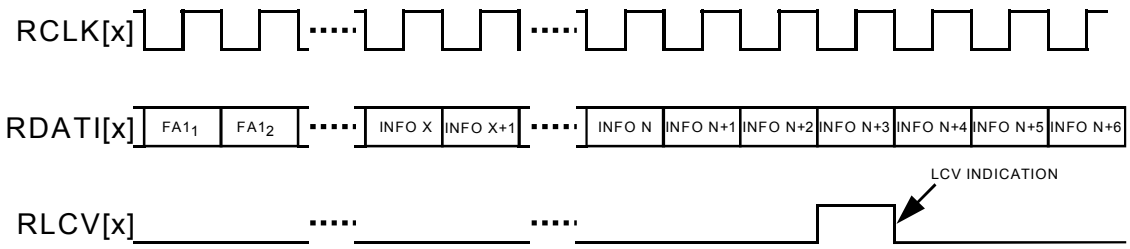


Figure 24, the Receive Bipolar J2 Stream diagram, shows the operation of the S/UNI-4xD3F while processing a B8ZS-encoded J2 stream on inputs RPOS and RNEG. It is assumed that the first bipolar violation (on RNEG) illustrated corresponds to a valid B8ZS signature. A LCV is declared upon detection of a bipolar violation which is not part of a valid B8ZS signature. An excessive zeros indication is given when 8 or more consecutive zeros are detected.

Figure 24 Receive Bipolar J2 Stream

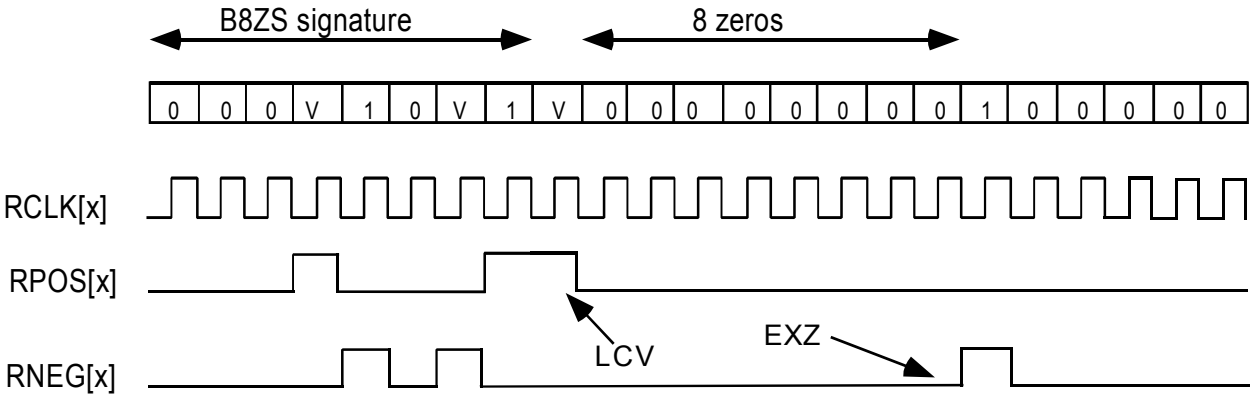


Figure 25, the Receive Unipolar J2 Stream diagram, shows the unipolar J2 receive signal on the RDATI[x] input. LCV indications, detected by an upstream B8ZS decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON LCV Event Counter is incremented each time a logic one is sampled on RLCV.

Figure 25 Receive Unipolar J2 Stream

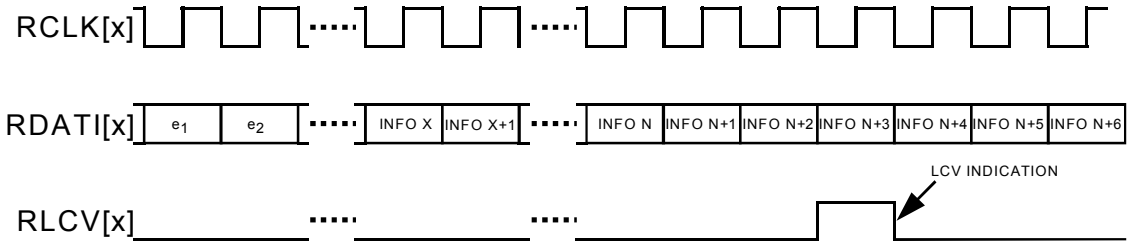


Figure 26, the generic receive stream diagram, illustrates how ROHM is used to mark the location of the transmission system overhead bits in the RDATI[x] stream. RDATI[x] and ROHM[x] are both sampled on the rising edge of RCLK[x].

Figure 26 Generic Receive Stream

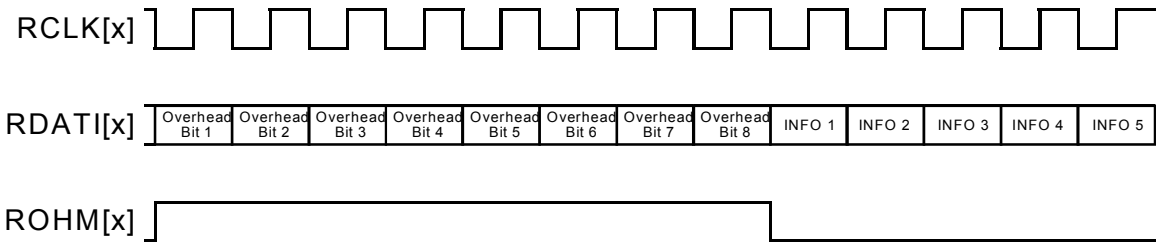


Figure 27, the Receive DS3 Overhead diagram, shows the extraction of the DS3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and M-frame position indicator (ROHFP). The DS3 M-frame can be divided into seven M-subframes, with each subframe containing eight overhead bits.

Figure 27 Receive DS3 Overhead

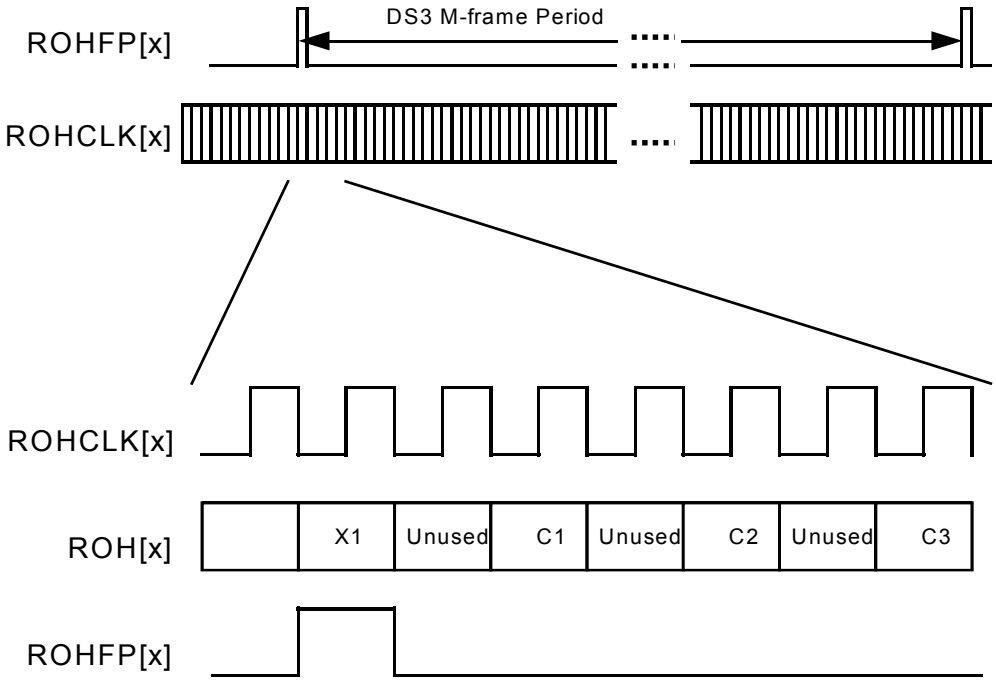


Table 29 illustrates the overhead bit order on ROH.

Table 29 DS3 Receive Overhead Bits

M-subframe	DS3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	X_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
2	X_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
3	P_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
4	P_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
5	M_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
6	M_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
7	M_3	N/U	C_1	N/U	C_2	N/U	C_3	N/U

The DS3 framing bits (F-bits) are not extracted on the overhead port. The bit positions corresponding to the F-bits in the extracted stream are marked N/U in the above table. The ROH stream is invalid when the DS3 frame alignment is lost.

Figure 28, the Receive G.832 E3 Overhead diagram, shows the extraction of the G.832 E3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP).

Figure 28 Receive G.832 E3 Overhead

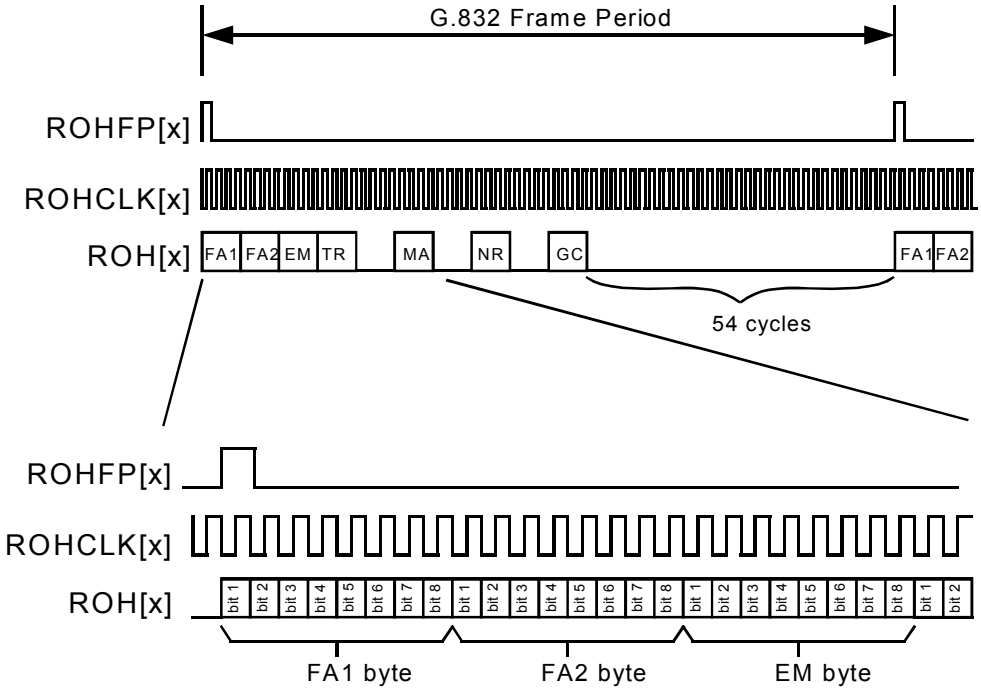


Figure 29, the Receive G.751 E3 Overhead diagram, shows the extraction of the G.751 E3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP). The justification indication bits (C_{jk}) along with the justification opportunity bits (J_1-J_4) are extracted when they are treated as overhead (PYLD&JUST bit in the E3 FRMR Maintenance Options register set to logic zero).

Figure 29 Receive G.751 E3 Overhead

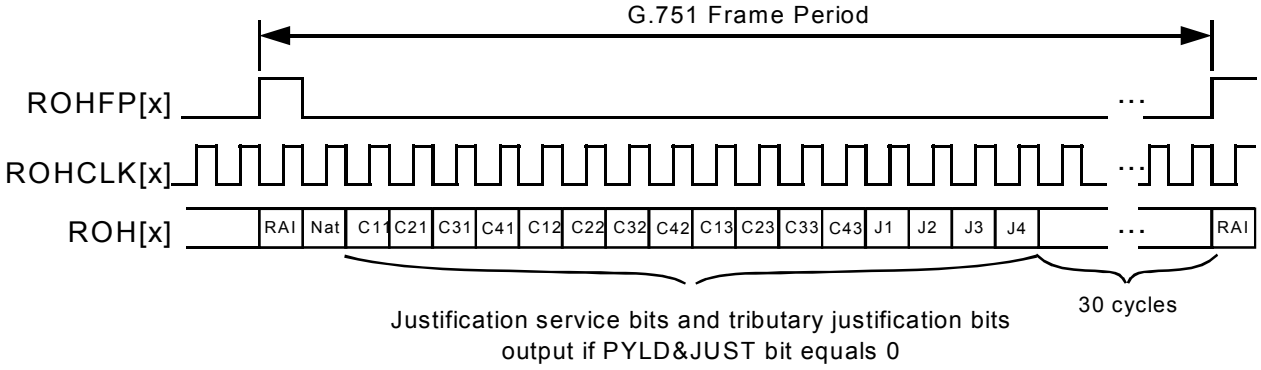


Figure 30, the Receive J2 Overhead diagram, shows the extraction of the J2 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP). ROHCLK is a gapped clock with a maximum instantaneous rate equal to the RCLK frequency. ROHFP pulses on the first bit of TS97 in the first frame of each J2 multiframe.

Figure 30 Receive J2 Overhead

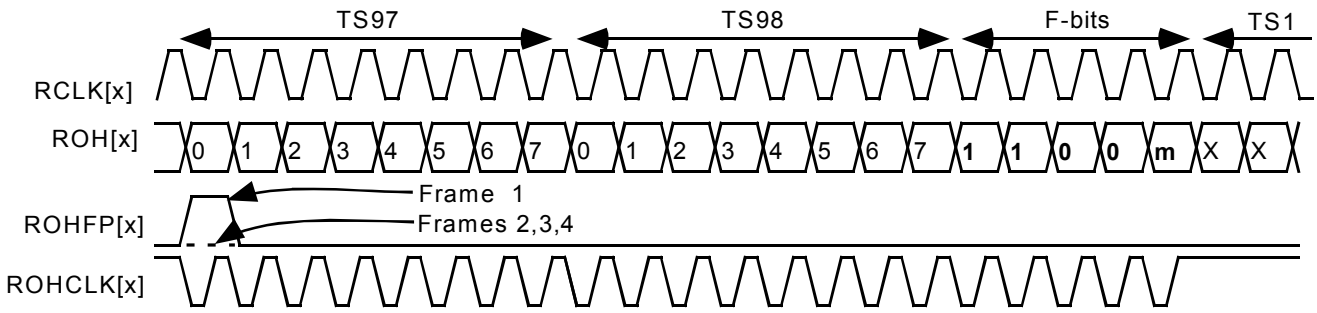


Figure 31, the Transmit DS1 Stream diagram, illustrates the generation of DS1 overhead indicators on TOHM when the S/UNI-4xD3F is configured for DS1 frame formats. The S/UNI-4xD3F flywheels using its internal timeslot counter to generate TOHM. The ATM cell stream is inserted in TDATO, along with a framing bit placeholder every 193 bit periods. An upstream DS1 framer (such as the PM4341A T1XC or PM4344 TQUAD) must be used to insert the appropriate DS1 framing pattern. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 31 Transmit DS1 Stream

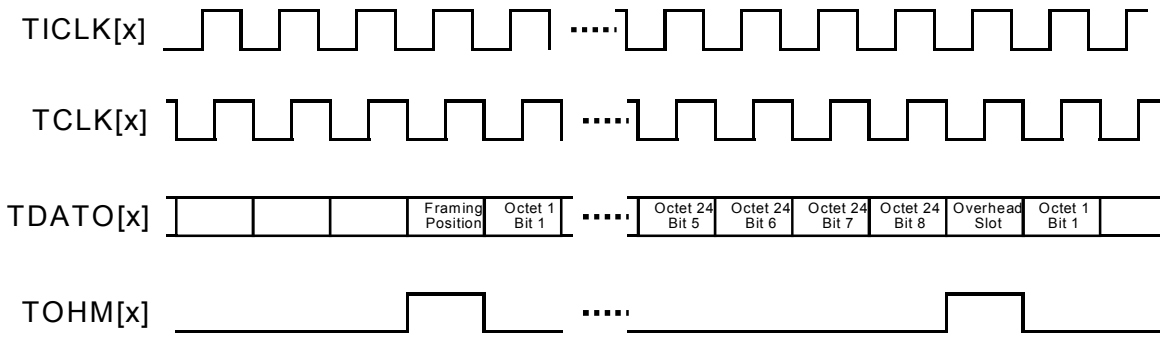


Figure 32, the Transmit E1 Stream diagram, illustrates the generation of E1 frame alignment indicators on TOHM when the S/UNI-4xD3F is configured for E1 frame formats. The S/UNI-4xD3F flywheels using its internal timeslot counter to generate TOHM. The ATM cell stream is inserted in TDATO, along with a framing bit placeholder every 256 bit periods. An upstream E1 framer (such as the PM6341A E1XC or PM6344 EQUAD) must be used to insert the appropriate E1 framing pattern. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 32 Transmit E1 Stream

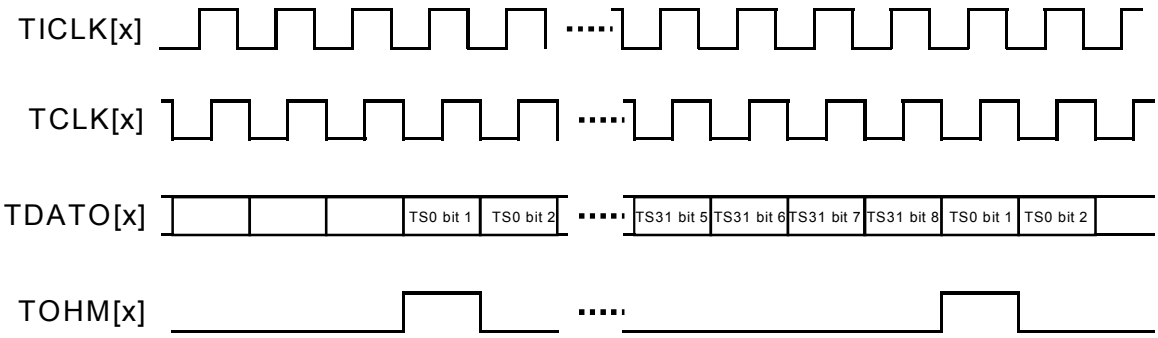


Figure 33, the Transmit Bipolar DS3 Stream diagram, illustrates the generation of a bipolar DS3 stream. The B3ZS encoded DS3 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a DS3 line interface unit. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 33 Transmit Bipolar DS3 Stream

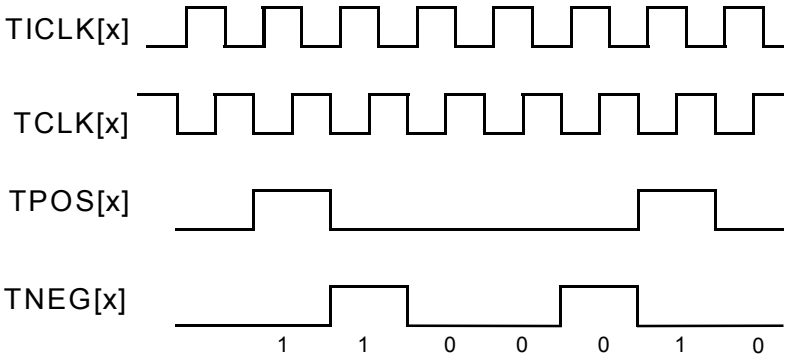


Figure 34, the Transmit Unipolar DS3 Stream diagram, illustrates the unipolar DS3 stream generation. The ATM cell stream, along with valid DS3 overhead bits is contained in TDATO. The TOHM output marks the M-frame boundary (the X1 bit) in the transmit stream. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 34 Transmit Unipolar DS3 Stream

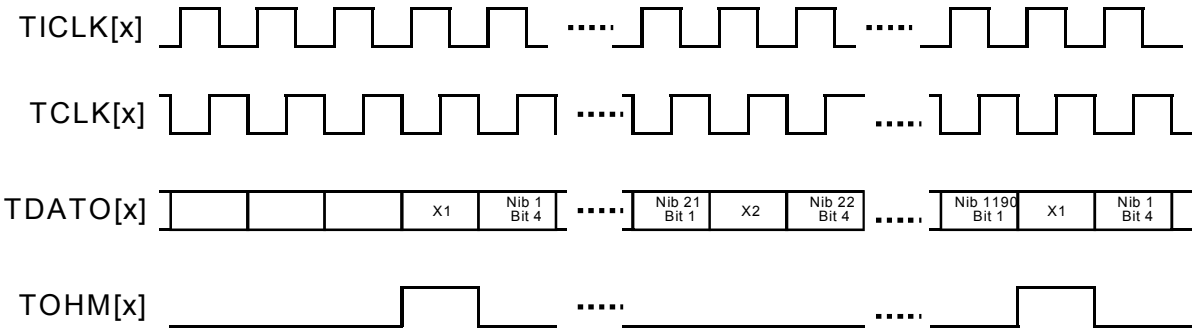


Figure 35, the Transmit Bipolar E3 Stream diagram, illustrates the generation of a bipolar E3 stream. The HDB3 encoded E3 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a E3 line interface unit. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 35 Transmit Bipolar E3 Stream

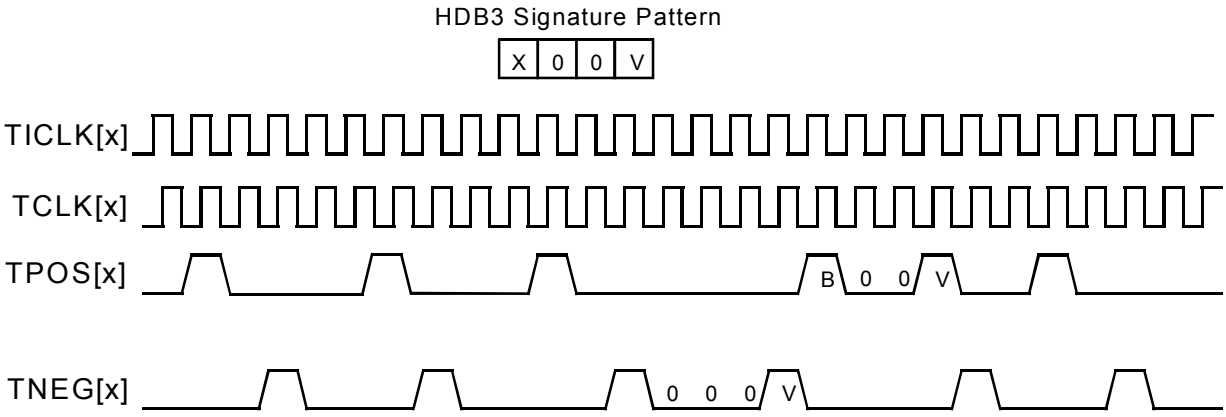


Figure 36, the Transmit Unipolar E3 Stream diagram, illustrates the unipolar E3 stream generation. The ATM cell stream, along with valid E3 overhead bits is contained in TDATO. The TOHM output shown marks the G.832 frame boundary (the first bit of the FA1 frame alignment byte) in the transmit stream. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals..

Figure 36 Transmit Unipolar E3 Stream

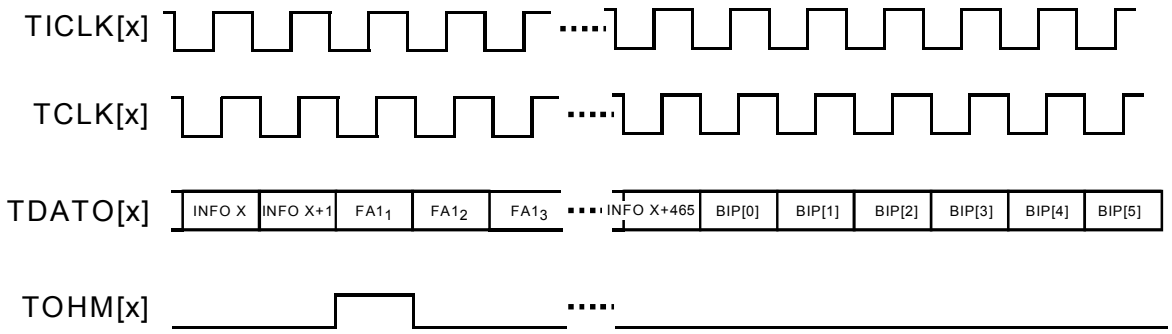


Figure 37, the Transmit Bipolar J2 Stream diagram, illustrates the generation of a bipolar J2 stream. The B8ZS encoded J2 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a J2 line interface unit. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 37 Transmit Bipolar J2 Stream

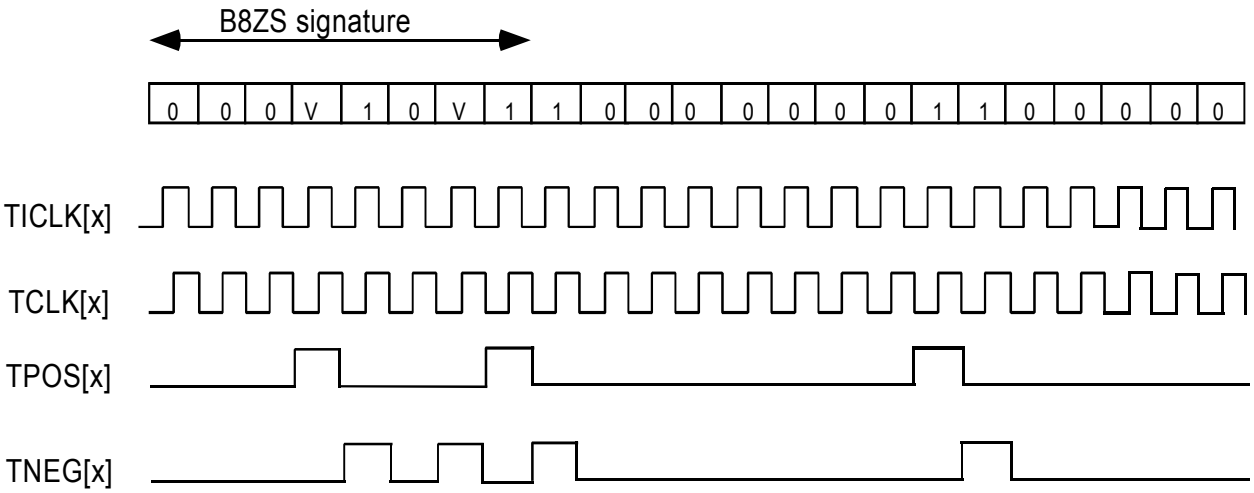


Figure 38, the Transmit Unipolar J2 Stream diagram, illustrates the unipolar J2 stream generation. The ATM cell stream, along with valid J2 overhead bits is contained in TDATO. The TOHM output shown marks the J2 multiframe boundary (the first frame-alignment bit of each J2 multi-frame) in the transmit stream. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 38 Transmit Unipolar J2 Stream

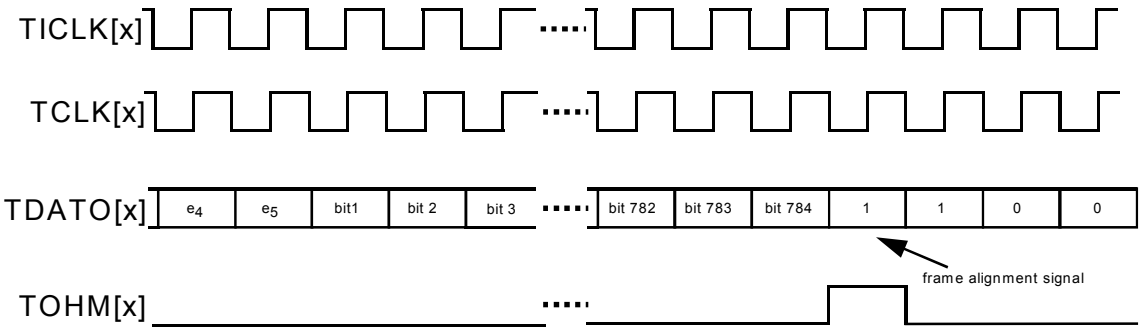
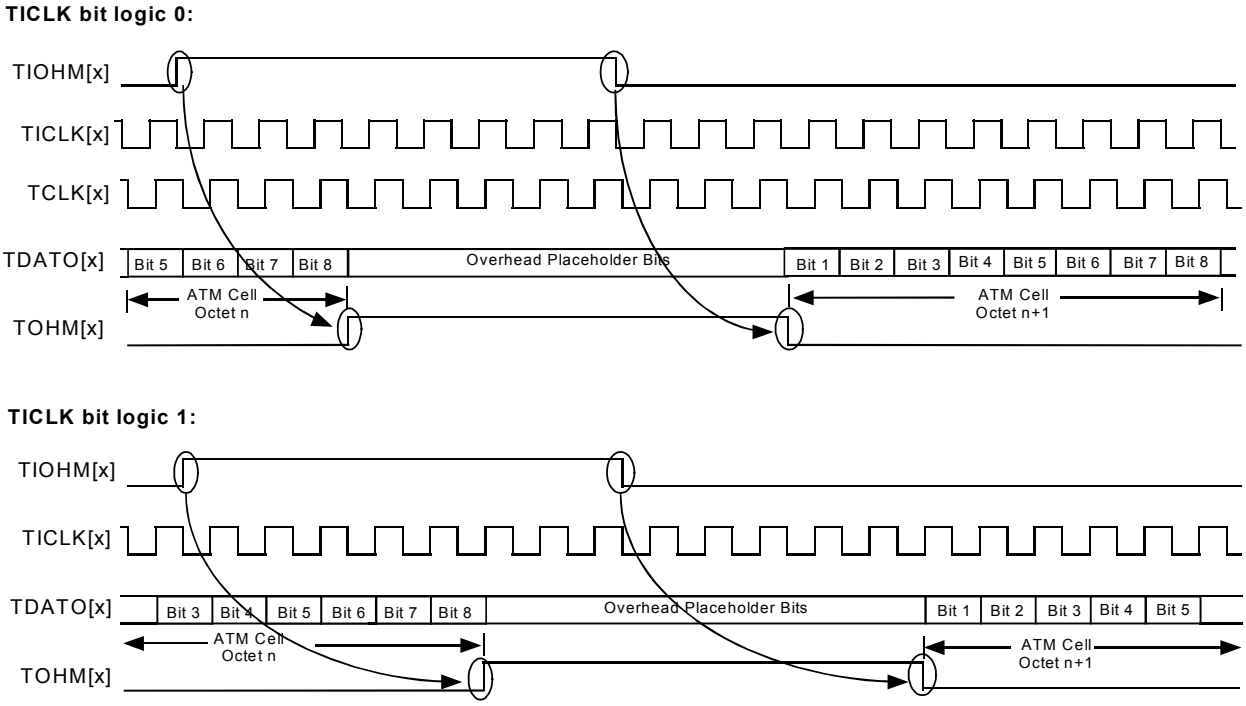


Figure 39, the Generic Transmit Stream diagram, illustrates overhead indication positions when interfacing to a non-PLCP based transmission system not supported by the S/UNI-4xD3F. The overhead bit placeholder positions are indicated using the TIOHM input. The ATM cells presented in the TDATO transmit stream are held off to include the overhead placeholders. The location of these placeholder positions is indicated by TOHM. A downstream framer inserts the correct overhead information in the placeholder positions.

Figure 39 Generic Transmit Stream



The delay between TIOHM and TOHM is dependent on the state of the TICLK bit of the S/UNI-4xD3F Transmit Configuration register. If the TICLK bit is a logic zero, TOHM is updated on the falling TCLK edge. TCLK is a flow-through version of TICLK and the propagation delay between TICLK and TCLK may vary depending on specific configurations. If the TICLK bit is a logic one, TOHM is presented on the fifth rising edge of TICLK after the rising edge which samples TIOHM.

Figure 40, the Transmit DS3 Overhead diagram, shows the insertion of DS3 overhead bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic one once per DS3 M-frame period (during the X1 bit position). In Figure 40, the data sampled on TOH during the X1, C1, F2, and C2 bit positions is inserted into the DS3 overhead bits in the transmit stream. The F1, F3, and C3 overhead bits are internally generated by the S/UNI-4xD3F.

Figure 40 Transmit DS3 Overhead

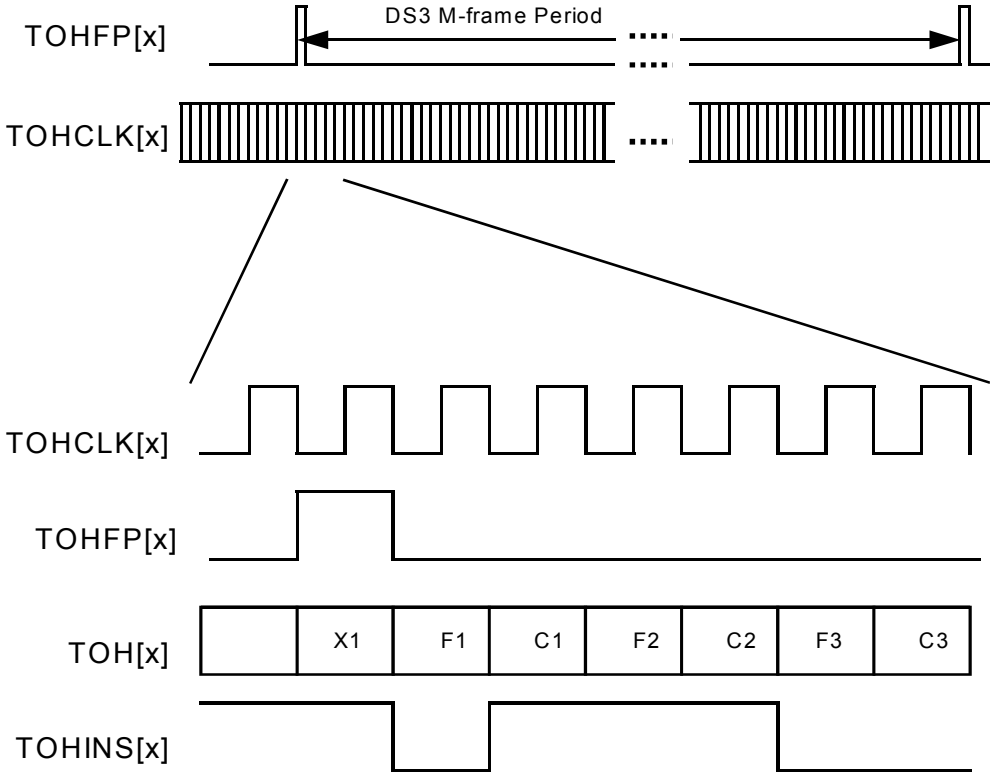


Table 30 illustrates the overhead bit order on TOH:

Table 30 DS3 Transmit Overhead Bits

M-subframe	DS3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	F_4

Figure 41, the Transmit G.832 E3 Overhead diagram, shows the insertion of G.832 E3 overhead bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic one once per G.832 frame period (during the first bit position of the FA1 byte). Figure 41, the bit data sampled on TOH during each byte position while TOHINS is logic one is inserted into the G.832 E3 overhead bits in the transmit stream. Note: If an entire byte is to be replaced with data from the TOH stream, TOHINS must be held logic one for the duration of that byte position. Also note: The EM byte behaves as an error mask, that is the binary value sampled on TOH in the EM byte location is not inserted directly into the transmit overhead but, rather, the value is XORed with the calculated BIP-8 and inserted in the transmit overhead. Asserting TOHINS during the “gaps” in the TOH stream has no effect.

Figure 41 Transmit G.832 E3 Overhead

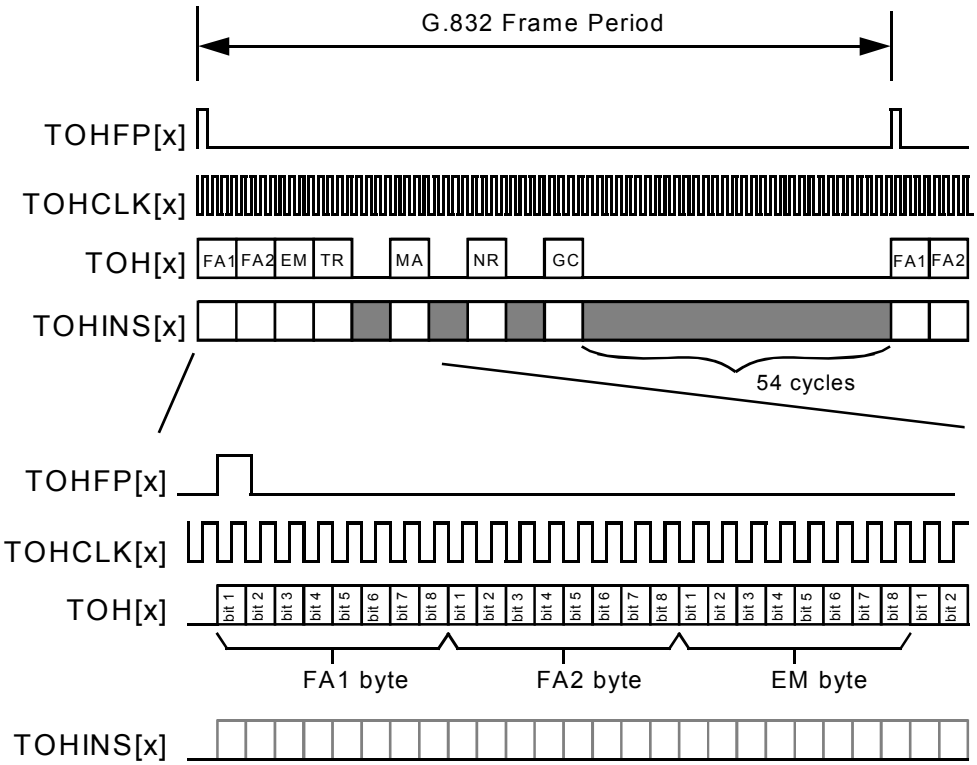
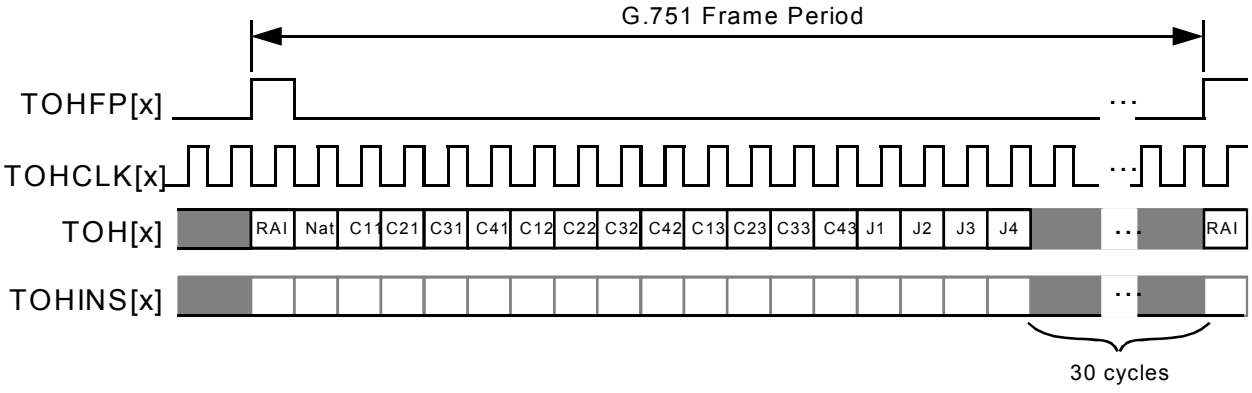


Figure 42, the Transmit G.751 E3 Overhead diagram, shows the insertion of G.751 overhead bits RAI, the National Use Bit, and the stuff indication and opportunity bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic one once per G.751 E3 frame period (during the RAI bit position). In Figure 42, the data sampled on TOH during the RAI, National Use, or stuff bit positions while TOHINS is logic one is inserted into the G.751 E3 overhead bits in the transmit stream.

Figure 42 Transmit G.751 E3 Overhead



The PYLD&JUST bit in the E3 TRAN Status and Diagnostics Options register has no affect on the insertion of the justification service and the tributary justification bits through the TOH and the TOHINS inputs.

Figure 43, the Transmit J2 Overhead diagram, shows the insertion of J2 overhead bits using the TOH and TOHINS inputs. The TOHFP output is set to logic one once per J2 multiframe (for the first bit of TS97 in the first frame of the J2 multiframe). TOHCLK is a gapped clock which will pulse at a maximum instantaneous rate equal to the TICLK frequency. When TOHINS is a logic one, the TOH input pin state replaces that generated within the J2 TRAN block. TOH and TOHINS are sampled on the rising TOHCLK clock edge.

Figure 43 Transmit J2 Overhead

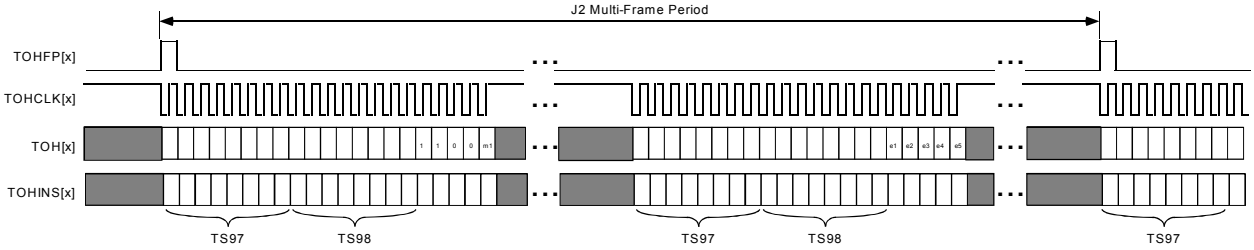
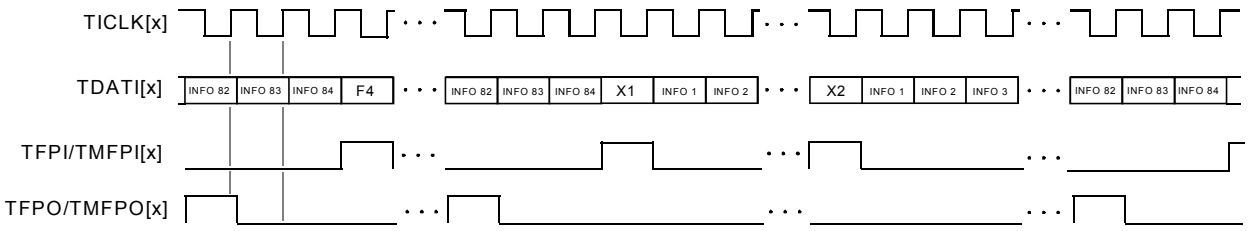


Figure 44 and Figure 45, the Framer Mode DS3 Transmit Input Stream diagrams, show the expected format of the inputs TDATI and TFPI/TMFPI along with TICLK and the output TFPO/TMFPO when the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is set, and the S/UNI-4xD3F is configured for the DS3 transmit format.

Figure 44 Framer Mode DS3 Transmit Input Stream



If the TXMFPI register bit is logic zero, then TFPI is valid, and the S/UNI-4xD3F will expect TFPI to pulse for every DS3 overhead bit with alignment to TDATI. If the TXMFPI register bit is logic one, then TMFPI is valid, and the S/UNI-4xD3F will expect TMFPI to pulse once every DS3 M-frame with alignment to TDATI. If the TXMFPO register bit is logic zero, then TFPO is valid, and the S/UNI-4xD3F will pulse TFPO once every 85 TICLK cycles, providing upstream equipment with a reference DS3 overhead pulse. If the TXMFPO register bit is logic one, then TMFPO is valid and the S/UNI-4xD3F will pulse TMFPO once every 4760 TICLK cycles, providing upstream equipment with a reference M-frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN-bit in the S/UNI-4xD3F Configuration 2 register is set to logic one, as in Figure 45. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

Figure 45 TGAPCLK Framer Mode DS3 Transmit Input Stream

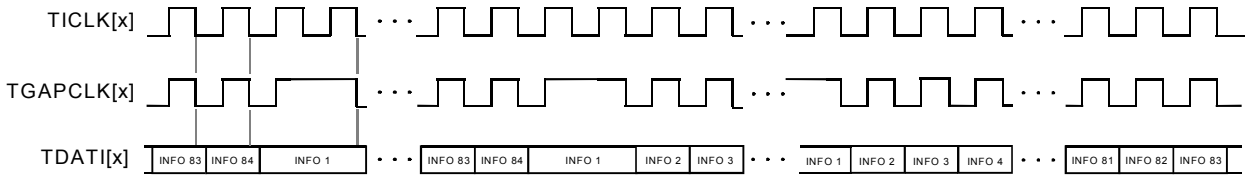
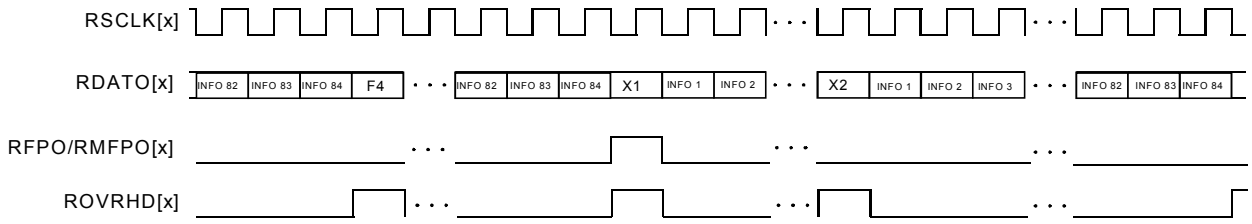


Figure 46 and Figure 47, the Framer Mode DS3 Receive Output Stream diagrams, show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is set. Figure 46 shows the data streams when the S/UNI-4xD3F is configured for the DS3 receive format. If the RXMFPO and 8KREFO register bits are logic zero, RFPO is valid and will pulse high for one RSCLK cycle on first bit of each M-subframe with alignment to the RDATO data stream. If the RXMFPO register bit is a logic one (as shown in Figure 46) and the 8KREFO register bit is logic zero, RMFPO is valid and will pulse high on the X1 bit of the RDATO data output stream. ROVRHD will be high for every overhead bit position on the RDATO data stream.

Figure 46 Framer Mode with DS3 Receive Output Stream



As shown in Figure 47 the RGAPCLK output is available in place of RSCLK when the RXGAPEN-bit in the S/UNI-4xD3F Configuration 2 register is set to logic one. RGAPCLK remains high during the overhead bit positions and RDATO does not change.

Figure 47 RGAPCLK and Framer Mode with DS3 Receive Output Stream

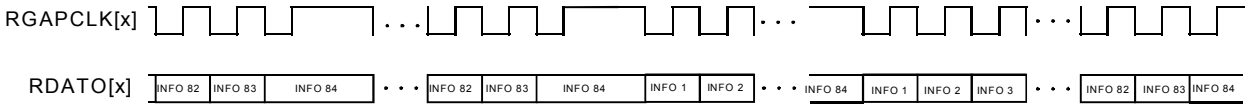
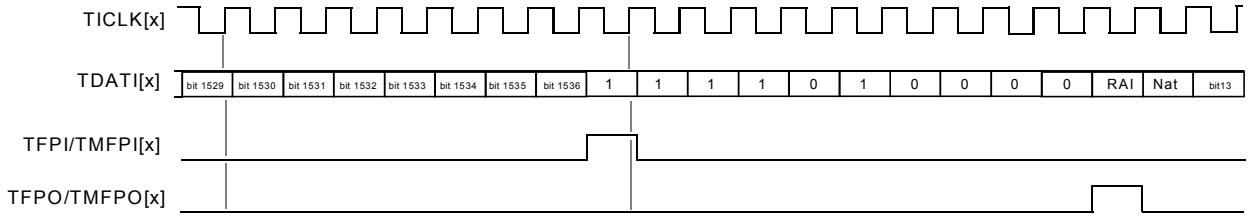


Figure 48 and Figure 49, the Framer Mode G.751 E3 Transmit Input Stream diagrams, show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is set, and the S/UNI-4xD3F is configured for the E3 G.751 transmit format.

Figure 48 Framer Mode G.751 E3 Transmit Input Stream



TFPI or TMFPI pulses high for one TICLK cycle and is aligned to the first bit of the frame alignment signal in the G.751 E3 input data stream on TDATI. TFPO or TMFPO will pulse high for one out of every 1536 TICLK cycles, providing upstream equipment with a reference frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN-bit in the S/UNI-4xD3F Configuration 2 register is set to logic one, as in Figure 49. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

Figure 49 TGAPCLK Framer Mode with G.751 E3 Transmit Input Stream

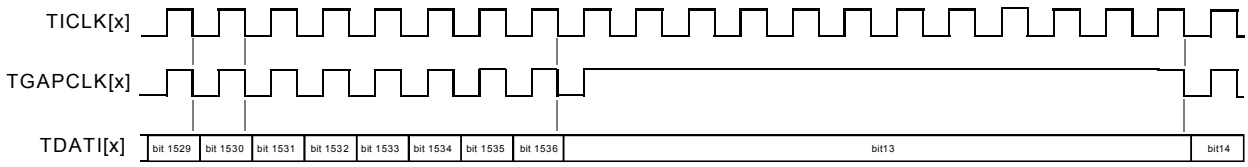
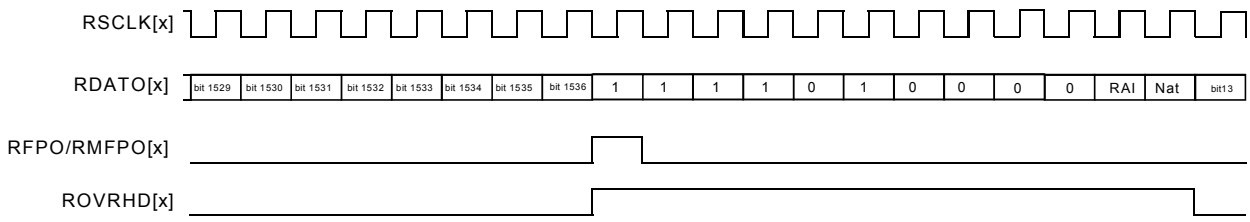


Figure 50 and Figure 51, the Framer Mode G.751 E3 Receive Output Stream diagrams, show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY and the 8KREFO bits in the S/UNI-4xD3F Configuration 1 register are set to logic one and logic zero respectively. Figure 50 shows the data streams when the S/UNI-4xD3F is configured for the E3 G.751 receive format. RFPO or RMFPO pulses high for one RSCLK cycle and is aligned to the first bit of the framing alignment signal in the G.751 E3 output data stream on RDATO. ROVRHD will be high for every overhead bit position on the RDATO data stream. If the PYLD&JUST register bit in the E3 FRMR Maintenance Options register is set to logic zero, the C_{jk} and P_k bits in the RDATO stream will be marked as overhead bits. If the PYLD&JUST register bit is set to logic one, the C_{jk} and P_k bits in the RDATO stream will be marked as payload.

Figure 50 Framer Mode G.751 E3 Receive Output Stream



The RGAPCLK output is available in place of RSCLK when the RXGAPEN-bit in the S/UNI-4xD3F Configuration 2 register is set to logic one. RGAPCLK remains high during the overhead bit positions as shown in Figure 51.

Figure 51 RGAPCLK Framer Mode G.751 E3 Receive Output Stream

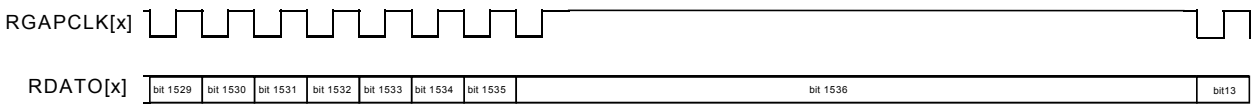
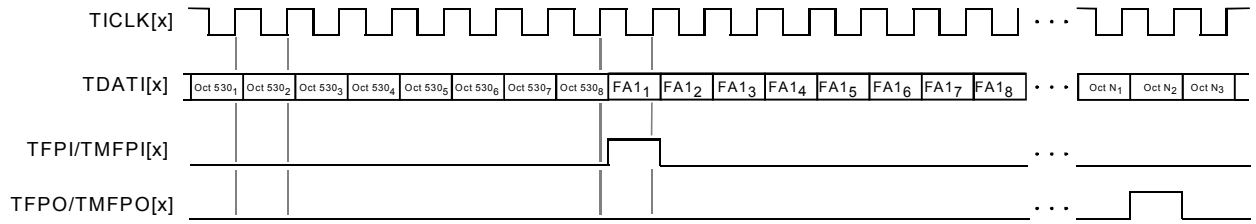


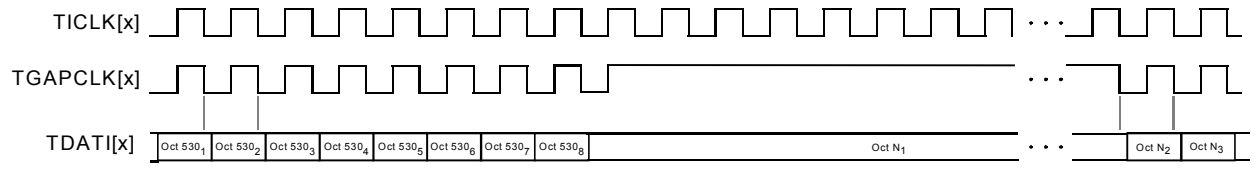
Figure 52 and Figure 53, the Framer Mode G.832 E3 Transmit Input Stream diagrams, show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is set, and the S/UNI-4xD3F is configured for the E3 G.832 transmit format. TFPI or TMFPI pulses high for one TICLK cycle and is aligned to the first bit of the FA1 byte in the G.832 E3 input data stream on TDATI. TFPO or TMFPO will pulse high for one out of every 4296 TICLK cycles, providing upstream equipment with a reference frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI.

Figure 52 Framer Mode G.832 E3 Transmit Input Stream



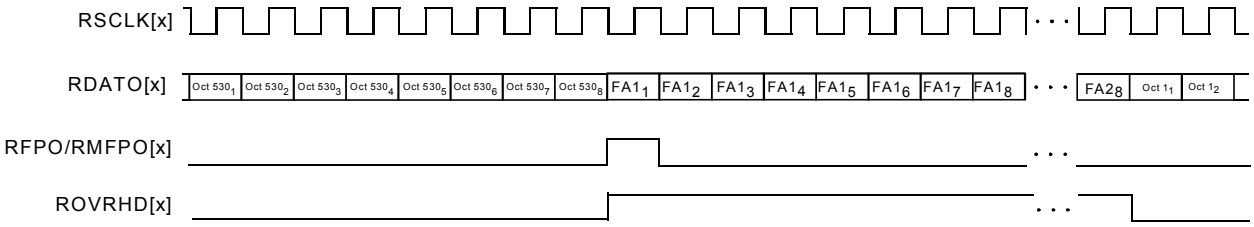
The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN-bit in the S/UNI-4xD3F Configuration 2 register is set to logic one, as in Figure 53. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

Figure 53 TGAPCLK Framer Mode with G.832 E3 Transmit Input Stream



The Framer Mode G.832 E3 Receive Output Stream diagrams (Figure 54 and Figure 55) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is set. Figure 54 shows the data streams when the S/UNI-4xD3F is configured for the E3 G.832 receive format. RFPO or RMFPO pulses high for one RSCLK cycle and is aligned to the first bit of the FA1 byte in the G.832 E3 output data stream on RDATO. ROVRHD will be high for every overhead bit position on the RDATO data stream.

Figure 54 Framer Mode G.832 E3 Receive Output Stream



The RGAPCLK output is available in place of RSCLK when the RXGAPEN-bit in the S/UNI-4xD3F Configuration 2 register is set to logic one. RGAPCLK remains high during the overhead bit positions as shown in Figure 55.

Figure 55 RGAPCLK Framer Mode G.832 E3 Receive Output Stream

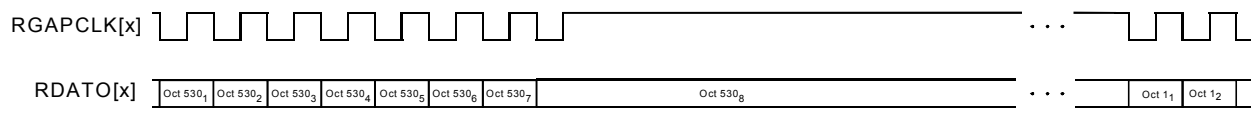
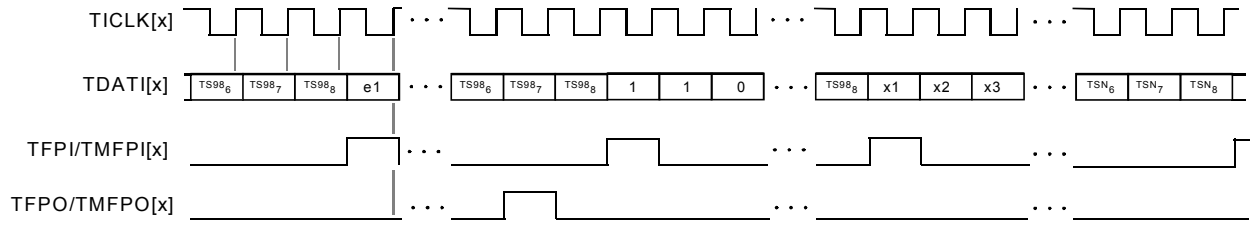


Figure 56 and Figure 57, the Framer Mode J2 Transmit Input Stream diagrams, show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is set, and the S/UNI-4xD3F is configured for the J2 transmit format. If the TXMFPI register bit is logic zero, then TFPI is valid (as shown in Figure 56).

Figure 56 Framer Mode J2 Transmit Input Stream



The S/UNI-4xD3F will expect TFPI to pulse once every J2 frame with alignment to the first frame alignment bit on TDATI. If the TXMFPI register bit is logic one, then TMFPI is valid. The S/UNI-4xD3F will expect TMFPI to pulse once every J2 multiframe with alignment to the first frame alignment bit on TDATI. If the TXMFPO register bit is logic zero, then TFPO is valid. The S/UNI-4xD3F will pulse TFPO once every 789 TICLK cycles, providing upstream equipment with a reference frame pulse. If the TXMFPO register bit is logic one, then TMFPO is valid and the S/UNI-4xD3F will pulse TMFPO once every 3156 TICLK cycles, providing upstream equipment with a reference multiframe pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN-bit in the S/UNI-4xD3F Configuration 2 register is set to logic one, as in Figure 57. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

Figure 57 TGAPCLK Framer Mode J2 Transmit Input Stream

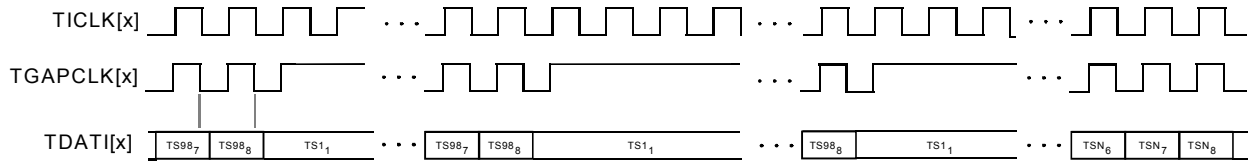
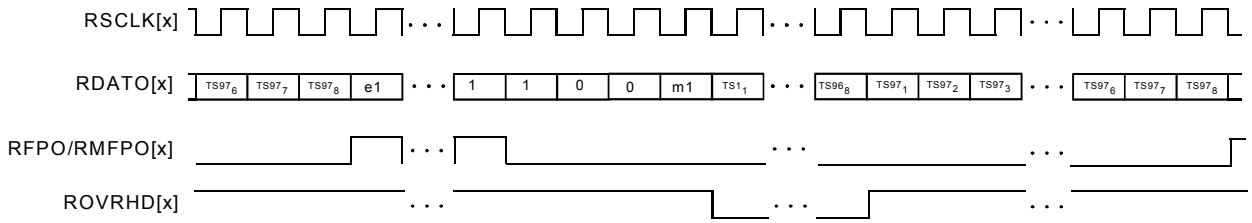


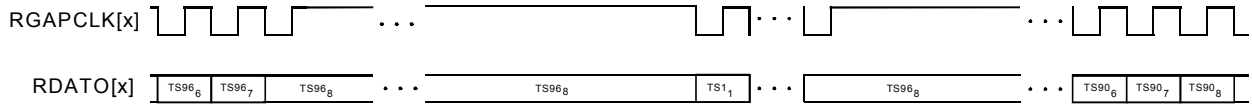
Figure 58 and Figure 59, the Framer Mode J2 Receive Output Stream diagrams, show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY bit in the S/UNI-4xD3F Configuration 1 register is set. Figure 58 shows the data streams when the S/UNI-4xD3F is configured for the J2 receive format. If the RXMFPO register bit is a logic zero, RFPO is valid and will pulse high for one RSCLK cycle once each J2 frame with alignment to the first frame alignment bit on the RDATO data stream (as shown in Figure 58).

Figure 58 Framer Mode J2 Receive Output Stream



If the RXMFPO register bit is a logic one, RMFPO is valid and will pulse high once each J2 multiframe aligned to the first frame alignment bit on the RDATO data output stream. ROVRHD will be high for every overhead bit position on the RDATO data stream. The RGAPCLK output is available in place of RSCLK when the RXGAPEN-bit in the S/UNI-4xD3F Configuration 2 register is set to logic one. RGAPCLK remains high during the overhead bit positions as shown in Figure 59.

Figure 59 RGAPCLK Framer Mode J2 Receive Output Stream



15 Absolute Maximum Ratings

Table 31 Absolute Maximum Ratings

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Supply VDD with respect to GND	-0.3 V to 4.6 V
Voltage on BIAS with respect to GND	VDD - 0.3 V to 5.5 V
Voltage on Any Pin	-0.3 V to BIAS +0.3 V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

16 D.C. Characteristics

T_A = -40°C to +85°C, V_{DD} = 3.3 V ±10%, V_{DD} < BIAS < 5.5 V
(Typical Conditions: T_A = 25°C, V_{DD} = 3.3V, V_{BIAS} = 5 V)

Table 32 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	2.97	3.3	3.63	Volts	
BIAS	5V Tolerant Bias	VDD	5.0	5.5	Volts	
I_{BIAS}	Current into 5V Bias		6.0		µA	V_{BIAS} = 5.5V
V_{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0		BIAS	Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		0.23	0.4	Volts	Guaranteed output Low voltage at VDD=2.97V and I_{OL}=maximum rated for pad. [4, 5, 6]
V_{OH}	Output or Bi-directional High Voltage	2.4	2.93		Volts	Guaranteed output High voltage at VDD=2.97V and I_{OH}=maximum rated current for pad. [4, 5, 6]
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TCK, TDI, TMS, and REF8KI.
V_{T+}	Reset Input High Voltage	2.0			Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TCK, TDI, TMS, and REF8KI.
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TCK, TDI, TMS, and REF8KI.
I_{ILPU}	Input Low Current	-100	-60	-10	µA	V_{IL} = GND. [1, 3]
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. [1. 3]
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. [2, 3]
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. [2, 3]
C_{IN}	Input Capacitance		6		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		6		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		6		pF	t_A=25°C, f = 1 MHz
I_{DDOP7}	Operating Current		268.3	330	mA	V_{DD} = 3.63V, Outputs Unloaded (DS3 framer only)
I_{DDOP8}	Operating Current		259.9	330	mA	V_{DD} = 3.63V, Outputs Unloaded (E3 framer only)
I_{DDOP9}	Operating Current		37.1	75	mA	V_{DD} = 3.63V, Outputs Unloaded (J2 framer only)

Notes

1. Input pin or bi-directional pin with internal pull-up resistor.

2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. The outputs TCLK[4:1], TPOS/TDATO[4:1], TNEG/TOHM[4:1], TFPO/TMFPO/TGAPCLK[4:1], RDATO[4:1], ROVRHD[4:1], RSCLK/RGAPCLK[4:1], and REF8KO/ RFPO/RMFPO[4:1] have 6 mA drive capability.
5. The data bus outputs, D[7:0], and all outputs not specified above have 3 mA drive capability.

17 Microprocessor Interface Timing Characteristics

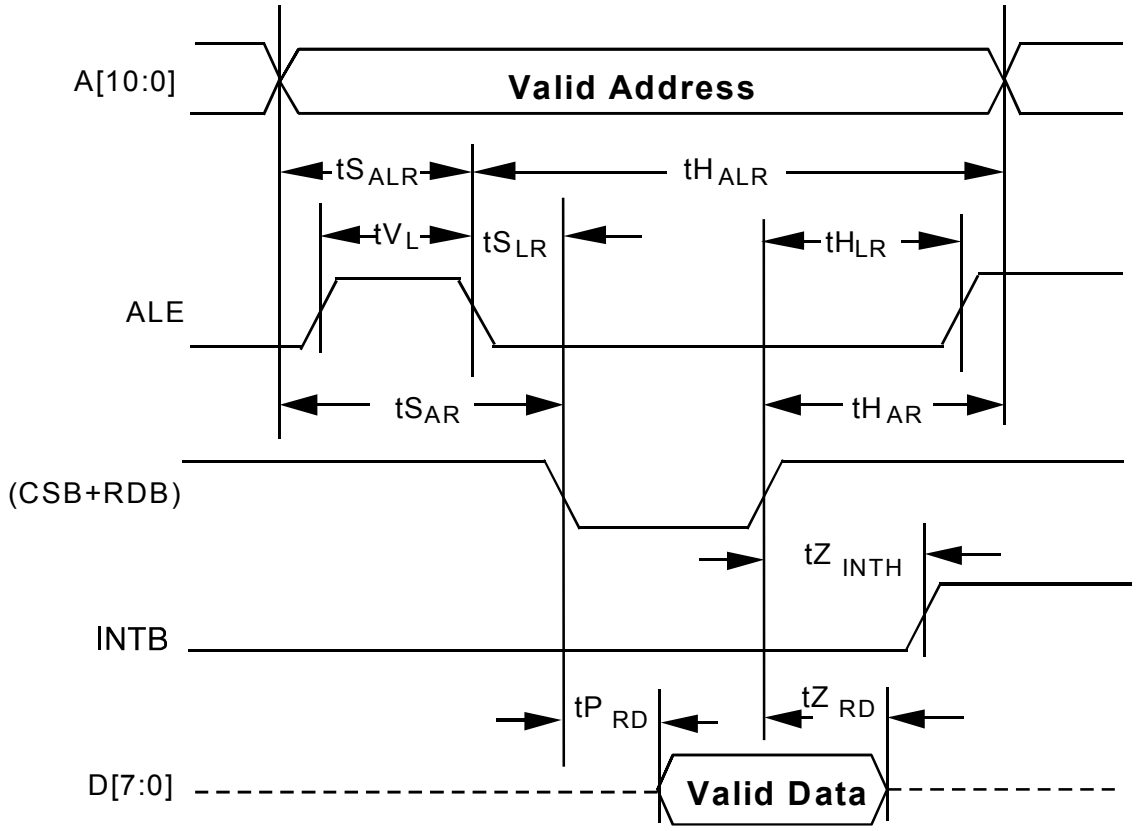
(T_A = -40°C to +85°C, V_{DD} = 3.3 V ±10%)

Table 33 Microprocessor Interface Read Access

Refer to Figure 60

Symbol	Parameter	Min	Max	Units
t_{SAR}	Address to Valid Read Set-up Time	10		ns
t_{HAR}	Address to Valid Read Hold Time	5		ns
t_{SALR}	Address to Latch Set-up Time	10		ns
t_{HALR}	Address to Latch Hold Time	10		ns
t_{VL}	Valid Latch Pulse Width	5		ns
t_{SLR}	Latch to Read Set-up	0		ns
t_{HLR}	Latch to Read Hold	5		ns
t_{PRD}	Valid Read to Valid Data Propagation Delay		70	ns
t_{ZRD}	Valid Read Negated to Output Tri-state		20	ns
t_{ZINTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 60 Microprocessor Interface Read Timing



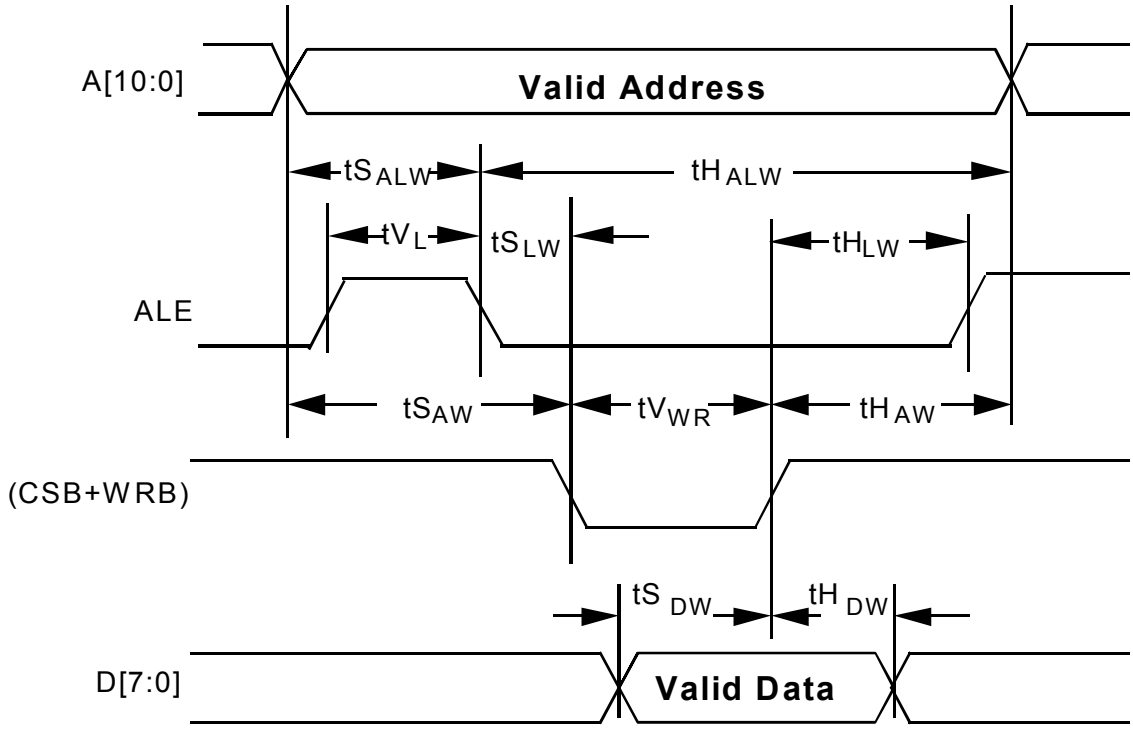
Notes

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 34 Microprocessor Interface Write Access (Figure 65)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 61 Microprocessor Interface Write Timing



Notes

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.

4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

18 A.C. Timing Characteristics

(T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%)

Table 35 RSTB Timing (Figure 62)

Symbol	Description	Min	Typical	Max	Units
$^{tV}_{RSTB}$	RSTB Pulse Width[4]		100		ns

Figure 62 RSTB Timing

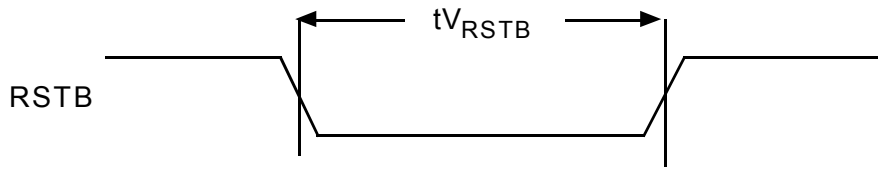
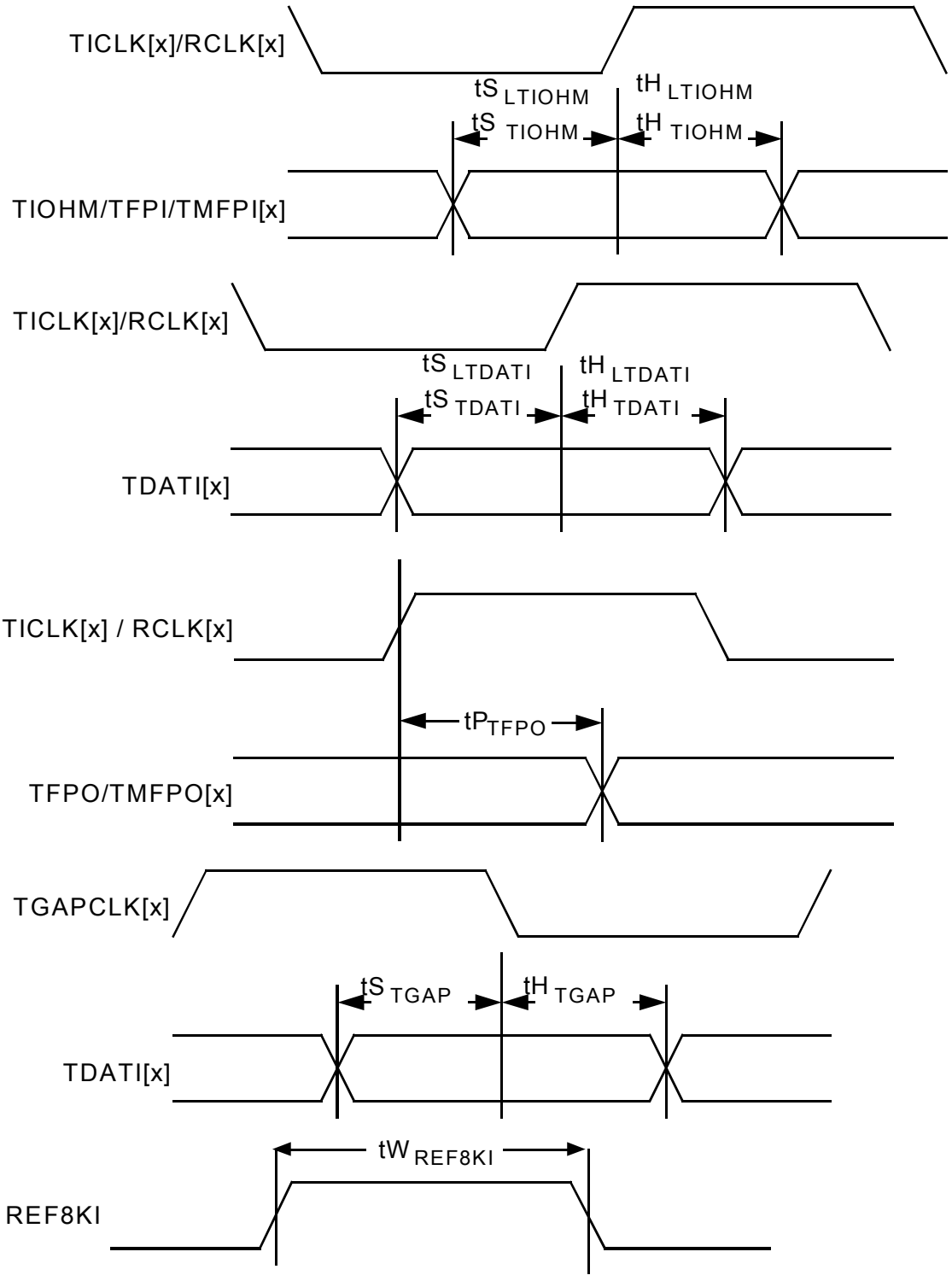


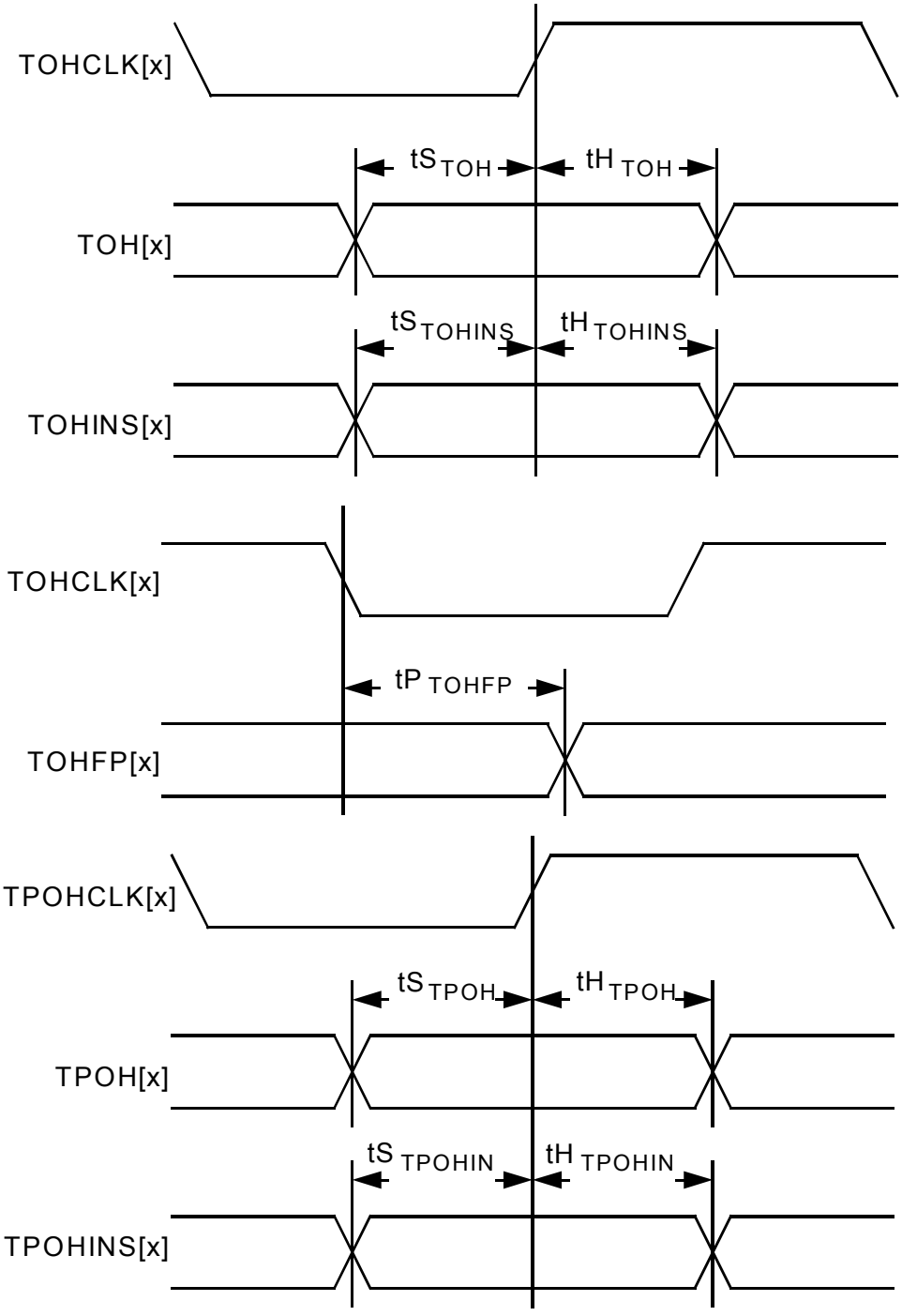
Table 36 Transmit Interface Timing (Figure 63)

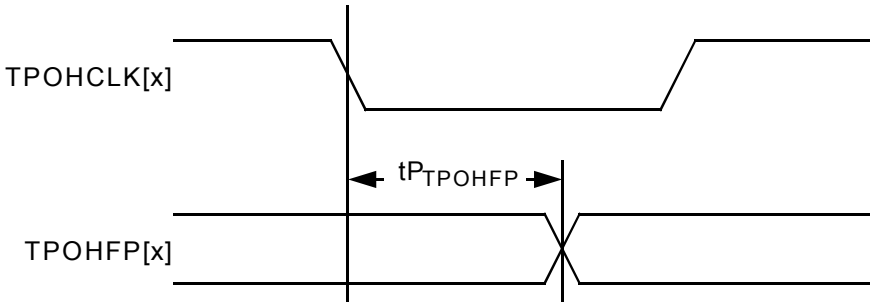
Symbol	Description	Min	Type	Max	Units
$^{f}_{TICLK}$	TICLK[x] Frequency: DS3 Framer (TFRM[1:0] = 00) E3 Framer (TFRM[1:0] = 01) J2 Framer (TFRM[1:0] = 10) framer bypass (TFRM[1:0] = 11)			 52 35 7 52	MHz
$^{t0}_{TICLK}$	TICLK[x] minimum pulse width low: DS3 Framer (TFRM[1:0] = 00) E3 Framer (TFRM[1:0] = 01) J2 Framer (TFRM[1:0] = 10) framer bypass (TFRM[1:0] = 11)	 7.7 11 57 7.7			ns
$^{t1}_{TICLK}$	TICLK[x] minimum pulse width high: DS3 Framer (TFRM[1:0] = 00) E3 Framer (TFRM[1:0] = 01) J2 Framer (TFRM[1:0] = 10) framer bypass (TFRM[1:0] = 11)	 7.7 11 57 7.7			ns
$^{tS}_{TIOHM}$	TIOHM/TFPI/TMFPI[x] to TICLK[x] Set-up Time	5			ns
$^{tH}_{TIOHM}$	TIOHM/TFPI/TMFPI[x] to TICLK[x] Hold Time	1			ns
$^{tS}_{TDATI}$	TDATI[x] to TICLK[x] Set-up Time	5			ns
$^{tH}_{TDATI}$	TDATI[x] to TICLK[x] Hold Time	1			ns
$^{tS}_{LTIOHM}$	TIOHM/TFPI/TMFPI[x] to RCLK[x] Set-up Time (LOOPT=1)	5			ns
$^{tH}_{LTIOHM}$	TIOHM/TFPI/TMFPI[x] to RCLK[x] Hold Time (LOOPT=1)	1			ns
$^{tS}_{LTDATI}$	TDATI[x] to RCLK[x] Set-up Time (LOOPT=1)	5			ns
$^{tH}_{LTDATI}$	TDATI[x] to RCLK[x] Hold Time (LOOPT=1)	1			ns

Symbol	Description	Min	Type	Max	Units
tP_{TFPO}	TICLK[x] to TFPO/TMFPO[x] Prop Delay, or RCLK[x] to TFPO/TMFPO[x] Prop Delay when loop timing is used.	2		16	ns
tS_{TGAP}	TDATI[x] to TGAPCLK[x] Set-up Time	3			ns
tH_{TGAP}	TDATI[x] to TGAPCLK[x] Hold Time	2			ns
tW_{REF8KI}	REF8KI pulse width[4]		15		ns
tS_{TOH}	TOH[x] to TOHCLK[x] Set-Up Time	20			ns
tH_{TOH}	TOH[x] to TOHCLK[x] Hold Time	20			ns
tS_{TOHINS}	TOHINS[x] to TOHCLK[x] Set-Up Time	20			ns
tH_{TOHINS}	TOHINS[x] to TOHCLK[x] Hold Time	20			ns
tP_{TOHFP}	TOHCLK[x] to TOHFP[x] Prop Delay	-15		20	ns
tS_{TPOH}	TPOH[x] to TPOHCLK[x] Set-Up Time	20			ns
tH_{TPOH}	TPOH[x] to TPOHCLK[x] Hold Time	20			ns
tS_{TPOHIN}	TPOHINS[x] to TPOHCLK[x] Set-Up Time	20			ns
tH_{TPOHIN}	TPOHINS[x] to TPOHCLK[x] Hold Time	20			ns
tP_{TPOHFP}	TPOHCLK[x] to TPOHFP[x] Prop Delay	-15		20	ns
tP_{TPOS}	TCLK[x] Edge to TPOS/TDATO[x] Prop Delay	-1		4.5	ns
tP_{TNEG}	TCLK[x] Edge to TNEG/TOHM[x] Prop Delay	-1		4.5	ns
tP_{TPOS2}	TICLK[x] High to TPOS/TDATO[x] Prop Delay	2		13	ns
TP_{TNEG2}	TICLK[x] High to TNEG/TOHM[x] Prop Delay	2		13	ns

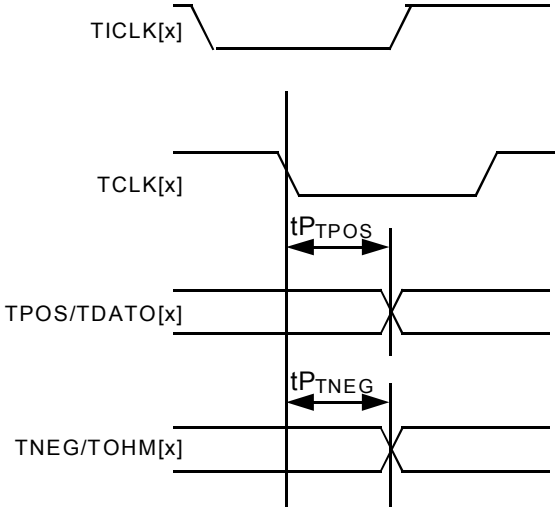
Figure 63 Transmit Interface Timing



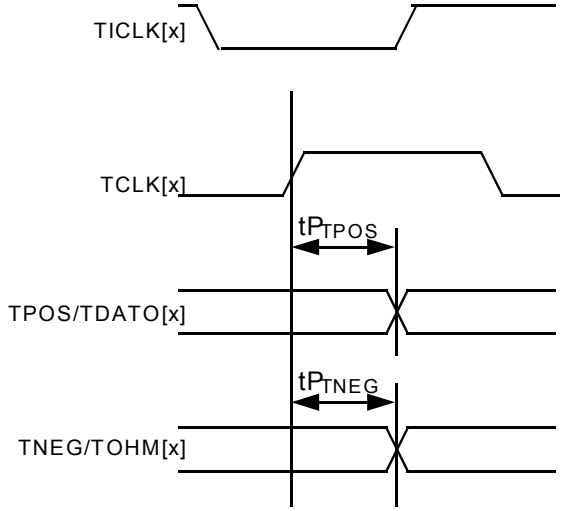

TOHCLK[x]
tS TOH
tH TOH
TOH[x]
tS TOHINS
tH TOHINS
TOHINS[x]
TOHCLK[x]
tP TOHFP
TOHFP[x]
TPOHCLK[x]
tS TPOH
tH TPOH
TPOH[x]
tS TPOHIN
tH TPOHIN
TPOHINS[x]



TICLK=0, TCLKINV=0



TICLK=0, TCLKINV=1



TICLK=1, TCLKINV=X

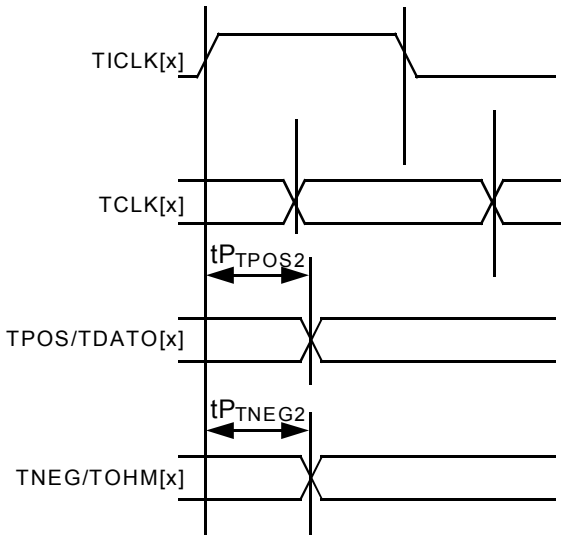
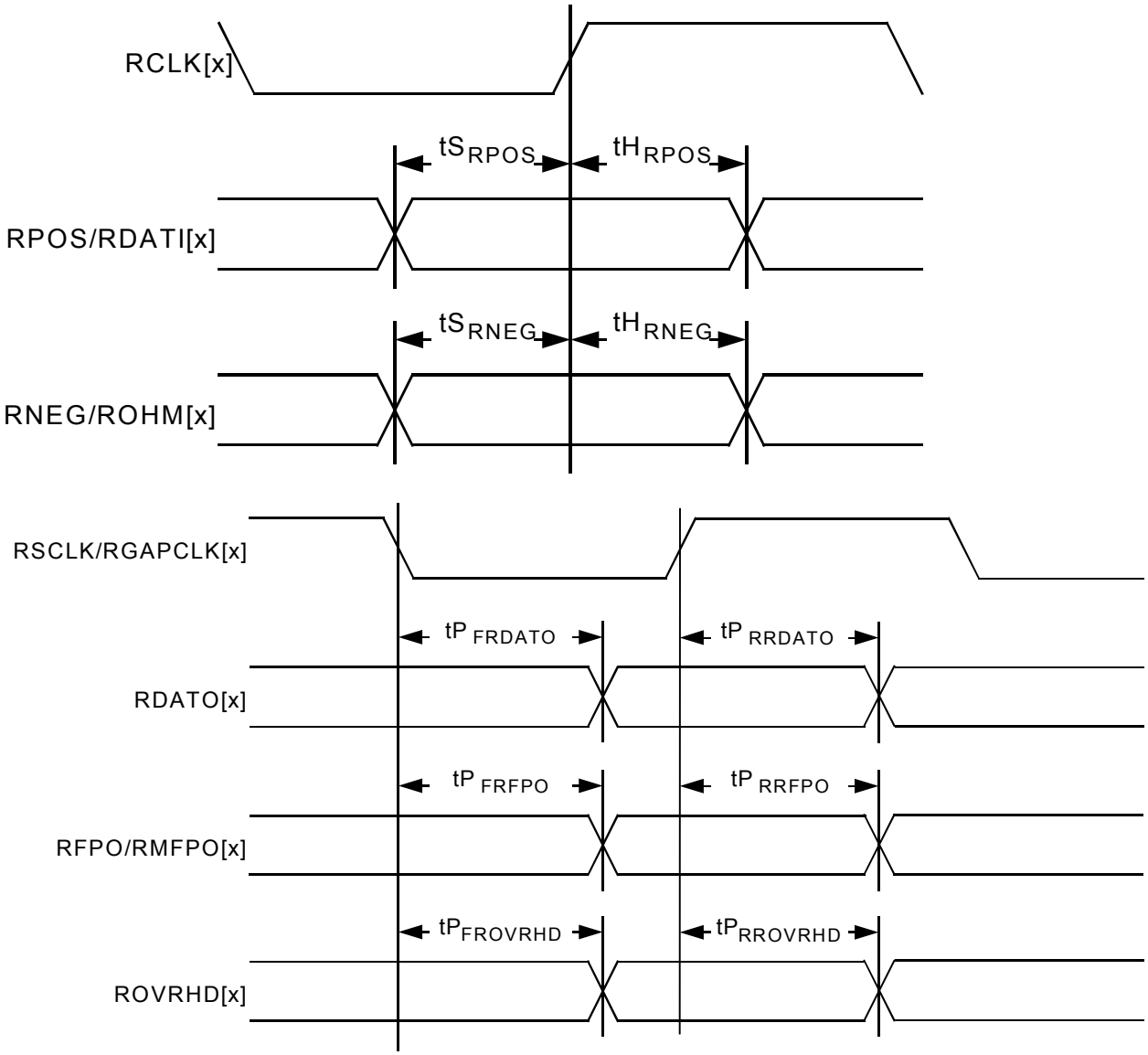


Table 37 Receive Interface Timing (Figure 64)

Symbol	Description	Min	Max	Units
F_{RCLK}	RCLK[x] Frequency: DS3 Framer (RFRM[1:0] = 00) E3 Framer (RFRM[1:0] = 01) J2 Framer (RFRM[1:0] = 10) framer bypass (RFRM[1:0] = 11)		 52 35 7 52	MHz
$t0_{RCLK}$	RCLK[x] minimum pulse width low: DS3 Framer (RFRM[1:0] = 00) E3 Framer (RFRM[1:0] = 01) J2 Framer (RFRM[1:0] = 10) framer bypass (RFRM[1:0] = 11)	 7.7 11 57 7.7		ns
$t1_{RCLK}$	RCLK[x] minimum pulse width high: DS3 Framer (RFRM[1:0] = 00) E3 Framer (RFRM[1:0] = 01) J2 Framer (RFRM[1:0] = 10) framer bypass (RFRM[1:0] = 11)	 7.7 11 57 7.7		ns
tS_{RPOS}	RPOS/RDATI Set-up Time	4		ns
tH_{RPOS}	RPOS/RDATI Hold Time	1		ns
tS_{RNEG}	RNEG/ROHM Set-Up Time	4		ns
tH_{RNEG}	RNEG/ROHM Hold Time	1		ns
tP_{RRDATO}	RSCLK[x]/RGAPCLK[x] rising edge to RDATO[x] Prop Delay	2	13	ns
tP_{RRFPO}	RSCLK[x] rising edge to RFPO/RMFPO[x] Prop Delay	1	13	ns
$tP_{RROVRHD}$	RSCLK[x] rising edge to ROVRHD[x] Prop Delay	1	13	ns
tP_{FRDATO}	RSCLK[x]/RGAPCLK[x] falling edge to RDATO[x] Prop Delay	-2	10	ns
tP_{FRFPO}	RSCLK[x] falling edge to RFPO/RMFPO[x] Prop Delay	-2	10	ns
$tP_{FROVRHD}$	RSCLK[x] falling edge to ROVRHD[x] Prop Delay	-2	10	ns
tP_{ROH}	ROHCLK[x] Low to ROH[x] Prop Delay	-15	20	ns
tP_{ROHFP}	ROHCLK[x] Low to ROHFP[x] Prop Delay	-15	20	ns
tP_{RPOH}	RPOHCLK[x] Low to RPOH[x] Prop Delay	-15	20	ns
tP_{RPOHFP}	RPOHCLK[x] Low to RPOHFP[x] Prop Delay	-15	20	ns

Figure 64 Receive Interface Timing



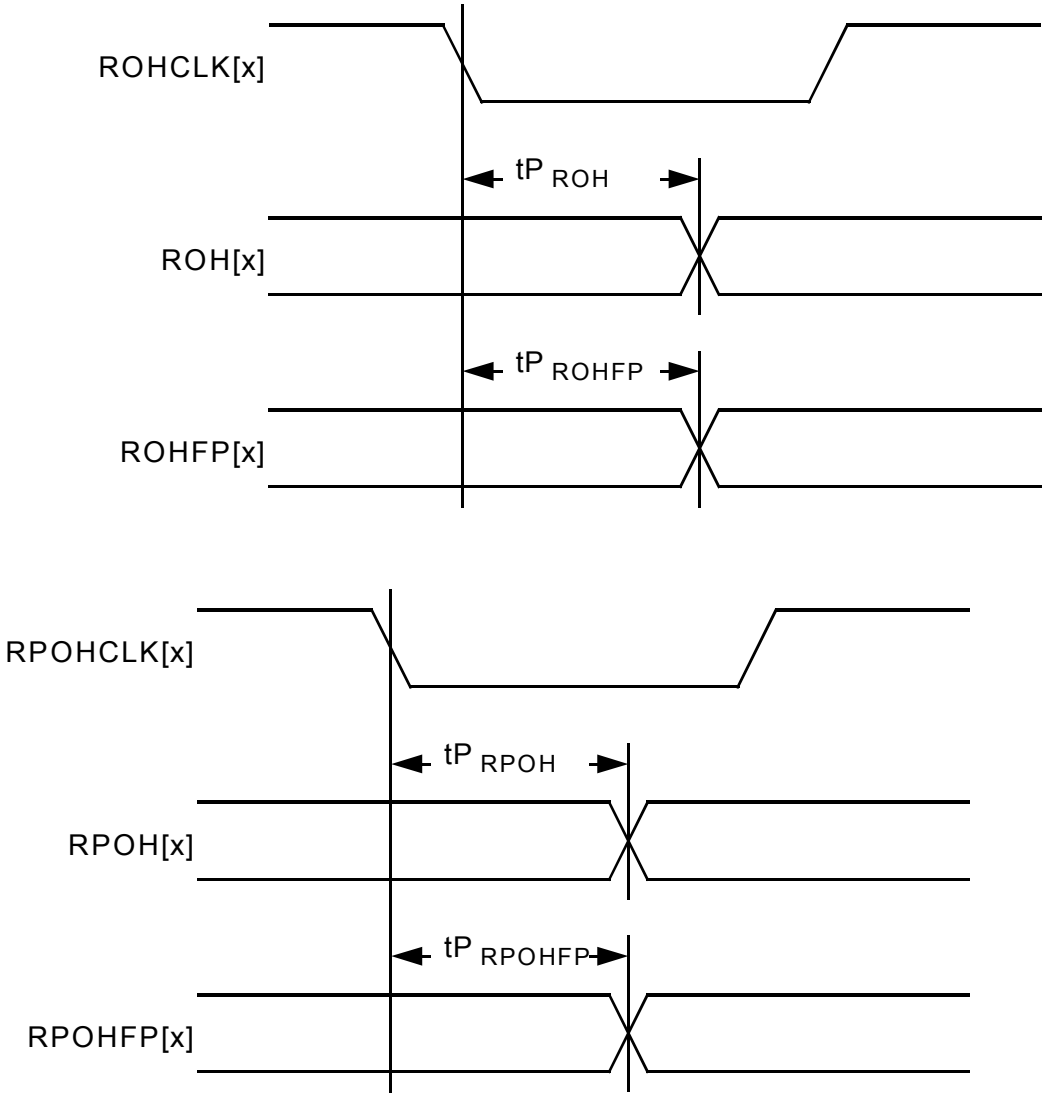
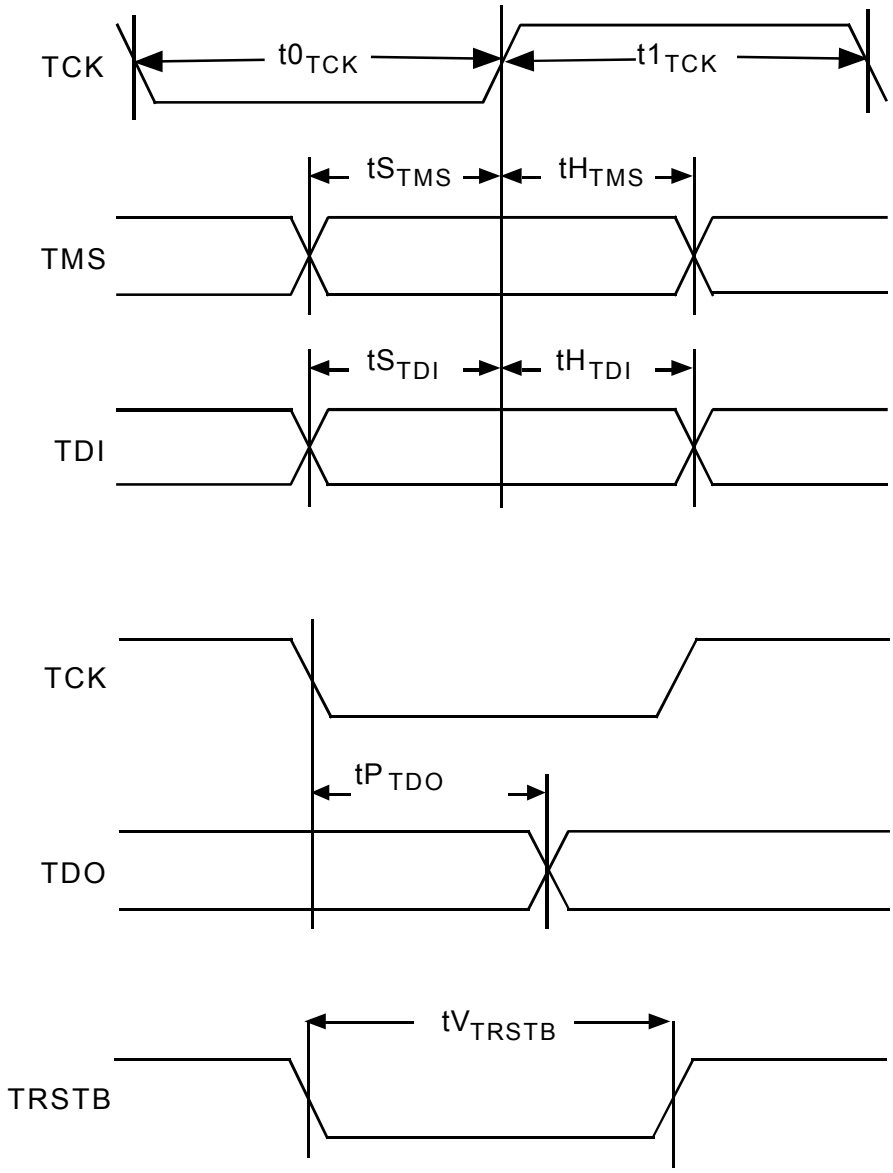


Table 38 JTAG Port Interface (Refer to Figure 65)

Symbol	Description	Min	Typical	Max	Units
$t1_{TCK}$	TCK high pulse width[5]				ns
$t0_{TCK}$	TCK low pulse width[5]	100			ns
tS_{TMS}, tS_{TDI}	TMS and TDI Set-up time to TCK[1]	50			ns
TH_{TMS}, TH_{TDI}	TMS and TDI Hold time to TCK[2]	50			ns
TP_{TDO}	TCK Low to TDO Valid[6,7]	2		50	ns
TV_{TRSTB}	TRSTB minimum pulse width[4,5]		100		ns

Figure 65 JTAG Port Interface Timing



Notes (on Input Timing)

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. It is recommended that the load on TGAPCLK[x] be kept less than 50pF. A larger load on these pins may result in functional failures.
4. This parameter is guaranteed by design. No production tests are done on this parameter.
5. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes (on Output Timing)

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

19 Ordering and Thermal Information

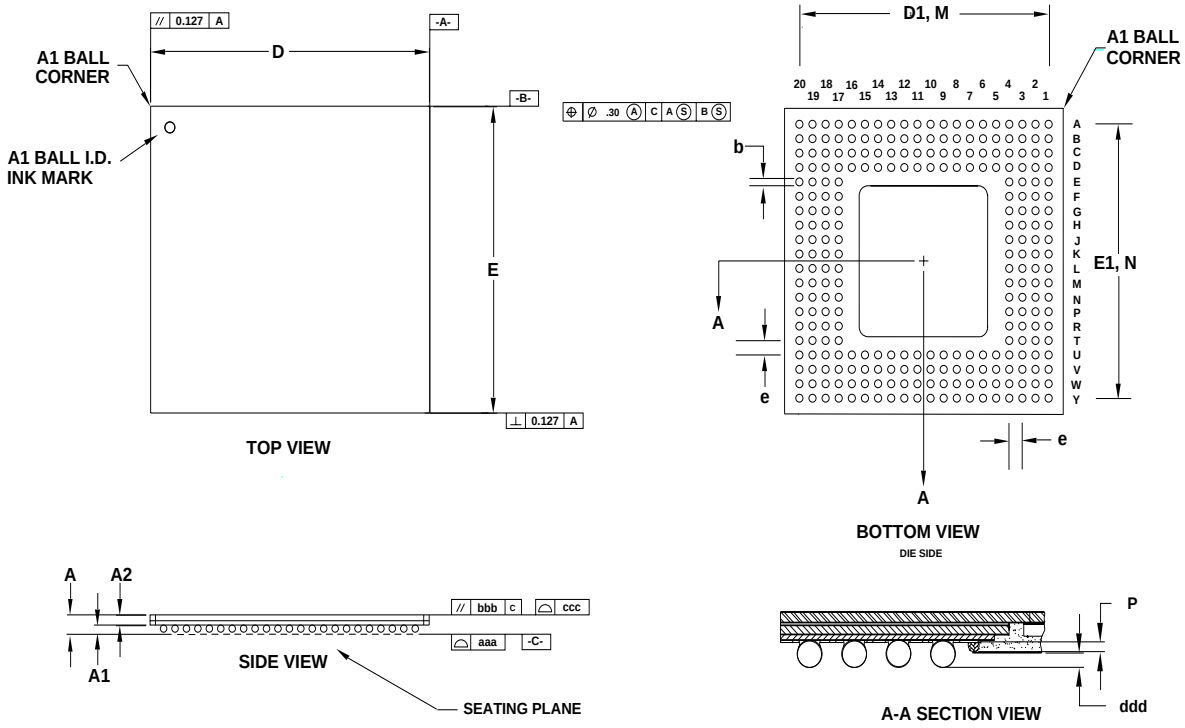
Table 39 Packaging Information

Part No.	Description
PM7347-BI	256-pin Ball Grid Array (SBGA)

Table 40 Thermal Information

Part No.	Ambient Temperature	Theta Ja	Theta Jc
PM7347-BI	-40°C to 85°C	19 °C/W	5 °C/W

20 Mechanical Information



Notes: 1) ALL DIMENSIONS IN MILLIMETER.

2) DIMENSION aaa DENOTES COPLANARITY

3) DIMENSION bbb DENOTES PARALLEL

4) DIMENSION ccc DENOTES FLATNESS

PACKAGE TYPE: 256 PIN THERMAL BALL GRID ARRAY															
BODY SIZE: 27 x 27 x 1.45 MM															
Dim.	A	A1	A2	D	D1	E	E1	M,N	e	b	aaa	bbb	ccc	ddd	P
Min.	1.32	0.56	0.76	26.90	24.03	26.90	24.03			0.60				0.15	0.20
Nom.	1.45	0.63	0.82	27.00	24.13	27.00	24.13	20x20	1.27	0.75				0.33	0.30
Max.	1.58	0.70	0.88	27.10	24.23	27.10	24.23			0.90	0.15	0.15	0.20	0.50	0.35

Notes