PM5383

S/UNI-12xJET

Saturn User Network Interface Device For J2/E3/T3

Data Sheet

Preliminary

Issue No. 2: July 2002

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U.S. Patent No. 6,098,195. Other relevant patent grants may also exist.

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1	July 2002	Updated all sections: Pin Description, Functional Description, Operation, Functional Timing, AC Timing, Ordering and Thermal, Mechanical, and Power Consumption.
1	October 2001	Document created.

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1 Definitions

The following table defines the abbreviations for the S/UNI-12xJET.

Term	Definition
AIS	Alarm Indication Signal
ASSP	Application Specific Standard Product
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BIP	Byte Interleaved Parity
CBI	Common Bus Interface
CMOS	Complementary Metal Oxide Semiconductor
COFA	Change of Frame Alignment
CPPM	Cell and PLCP Performance Monitor
CRC	Cyclic Redundancy Check
CSU	Clock Synthesis Unit
D3E3MA	DS3 / E3 TO STS-1 Mapper / Synchronizer
D3E3MD	STS-1 TO E3 / DS3 Demapper / Desynchronizer
DCC	Data Communication Channel
DLL	Digital Delay Lock Loop
DS1	Digital Signal Level 1
DS3	Digital Signal Level 3
E3-FRMR	ITU-T G.832 E3, G.751 E3 Framer
E3-TRAN	CCITT G.832 E3, G.751 E3 Transmitter
ERDI	Enhanced Remote Defect Indication
ESD	Electrostatic Discharge
EXZS	Excess Zeros
FAS	Framing Alignment Signal
F-bit	Framing Bit
FCS	Frame Check Sequence
FEAC	Far-End Alarm Control
FEBE	Far-End Block Error also referred to as REI
FEBE	Far-End Block Error
FERF	Far End Receive Failure
FERR	Framing Bit Error
FIFO	First-In First-Out
GFC	Generic Flow Control
HCS	Header Check Sequence
HDLC	High-level Data Link Layer
ISDN	Integrated Services Digital network
ITU	International Telecommunications Union
J2-FRMR	J2 Framer

Term	Definition
J2-TRAN	J2 Transmitter
JAT	Digital Jitter Attenuator
JTAG	Joint Test Action Group
LAIS	Line AIS also referred to as AIS-L
LAN	Local Area Network
LCD	Loss of Cell Delineation
LCD	Loss of Cell Delineation
LCV	Line Code Violation
LOF	Loss of Frame
LOH	Line Overhead
LOP	Loss of Pointer
LOS	Loss of Signal
LOT	Loss of Transition
LRDI	Line RDI also referred to as RDI-L
NC	No Connect, indicates an unused pin
NDF	New Data Flag
NNI	Network-Network Interface
NRZ	Non Return to Zero
ODL	Optical Data Link
OOF	Out of Frame
PERR	Parity Error
PHY	Physical Layer
PLCP	Physical Layer Convergence Procedure
PLL	Phase-Locked Loop
PMDL	Path Maintenance Data Link
PMON	E3/T3 Performance Monitor
POS	Packet Over SONET
PPP	Point-to-Point Protocol
PRGD	Pseudo Random Sequence Generator/ Detector
PRGM	DS3 Drop Side Mapper
PSL	Path Signal Label
PSLM	Path Signal Label Mismatch
RAI	Receive Alarm Indication
RBOC	Bit Oriented Code Detector
RDI	Remote Defect Indication
RDLC	Data Link Receiver
RED	Receive Error Detection
RHPP	Receive High Order Path Processor
RRMP	Receive Regenerator and Multiplexer Section Processor
RTTP	Receive Trail Trace Processor

Term	Definition
RXCP	Receive ATM Cell Processor
RXFP	Receive Packet over SONET Frame Processor
SARC	SONET/SDH Alarm Reporting Controller
SBER	SONET/SDH Bit Error Monitoring
SD	Signal Degrade (alarm)
SDH	Synchronous Digital Hierarchy
SF	Signal Fail
SMDS	Switched Multi-Megabit Data Service
SOH	Section Overhead
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelope
SPLR	SMDS PLCP Layer Receiver
SPLT	SMDS PLCP Layer Transmitter
SPTB	SONET/SDH Path Trace Buffer
SVCA	SONET/SDH Virtual Container Aligner
T3-FRMR	T3 (DS3) Framer
T3-TRAN	Transmitter T3 (DS3)
TAP	Test Access Port
TAPI	Transmit Add bus Pointer Interpreter
TDPR	Transmit Data Link Controller with Performance Report Interface
THPP	Transmit High Order Path Processor
TIM	Trace Identifier Mismatch
TIU	Trace Identifier Unstable
TOH	Transport Overhead
TRMP	Transmit Regenerator and Multiplexer Processor
TSBGA	Tape Super Ball Grid Array
TTTP	Transmit Trail Trace Processor
TXCP	Transmit ATM Cell Processor
TXFP	Transmit Packet Over SONET Frame Processor
UI	Unit Interval
UNI	User-Network Interface
VCI	Virtual Connection Indicator
VPI	Virtual Path Indicator
WAN	Wide Area Network
XBOC	Bit-Oriented Code Transmitter
XOR	Exclusive OR logic operator

2 Features

2.1 General

- Single chip 12-channel ATM User Network Interface operating at 44.736 Mbit/s, 34.368 Mbit/s, and 6.312 Mbit/s conforming to AF-PHY-0054.000, AF-PHY-0034.000 , and AF-PHY-0029.000. Each line can be individually configured for the desired rate and data formats.
- Single chip 12-channel HDLC User Network Interface operating at 44.736 Mbit/s, 34.368 Mbit/s, and 6.312 Mbit/s. Each line can be individually configured for the desired rate and data formats.
- Provides a duplex 8-bit 77.76 MHz STS-12/STM-4 line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.
- Provides a duplex 8-bit 77.76 MHz TelecomBus compatible interface which may be combined with three other S/UNI-12xJET devices to form a 32-bit 77.76MHz STS-48/STM-16 TelecomBus compatible interface.
- Support is provided for SMDS, bit-HDLC and ATM mappings into various rate transmission systems as follows:

Table 1 Supported Serial Operating Formats

Rate	Format	Framer Only	SMDS PLCP Mapping	Direct Mapping
T3 (44.736 Mbit/s)	C-bit Parity	Yes	Yes	Yes
	M23	Yes	Yes	Yes
E3 (34.368 Mbit/s)	G.751	Yes	Yes	Yes
	G.832	Yes	n/a	Yes
J2 (6.312 Mbit/s)	G.704 & NTT	Yes	n/a	Yes
E1 (2.048 Mbit/s)	CRC-4	External	Yes	Yes
	PCM30	External	Yes	Yes
T1 (1.544 Mbit/s)	ESF	External	Yes	Yes
	SF	External	Yes	Yes
Arbitrary Cell Rate (up to 52 Mbit/s)		Bypass	n/a	Yes

- Provides termination for SONET Section, Line and Path overhead or SDH Regenerator Section, Multiplexer Section and High Order Path overhead.
- Synchronizes DS3 and E3 serial streams to SONET/SDH payloads, accommodating plesiochronous timing offsets between the line and system timing references, through appropriate bit stuffing.
- Desynchronizes DS3 and E3 serial streams from SONET/SDH payloads, accommodating plesiochronous timing offsets between the line and system timing references, through appropriate processing of bit stuffing and pointer movements.

- Single chip ATM and packet process capable of processing rates up to STS-12c/STM-4-4c payloads.
- Implements the ATM Forum User Network Interface Specification AF-UNI-0010.02 and the ATM physical layer for Broadband ISDN according to ITU-T Recommendation I.432 series on arbitrary SONET/SDH payloads including STS-1/STM-0/STS-3c/STM-1/STS-12c/STM-4-4c payloads.
- Implements the Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615, RFC 1619, and RFC 1662 on arbitrary SONET/SDH payloads including STS-1/STM-0/STS-3c/STM-1/STS-12c/STM-4-4c payloads.
- Implements ATM Direct Cell Mapping into DS1, DS3, E1, E3, and J2 transmission systems according to ITU-T Recommendation G.804.
- Implements bit HDLC Mapping into DS1, DS3, E1, E3, and J2 transmission systems according to ITU-T Recommendation G.804.
- Implements the Physical Layer Convergence Protocol (PLCP) for DS1 and DS3 transmission systems according to the ATM Forum AF-UNI-0010.02 and Telcordia TR-TSV-000773, TR-TSV-000772, and E1 and E3 transmission systems according to the ETSI 300-269 and ETSI 300-270.
- Provides on-chip DS3, E3 (G.751 and G.832), and J2 framers.
- May be configured to be used solely as a DS3, E3, or J2 Framer.
- Provides support for an arbitrary rate external transmission system interface up to a maximum rate of 52 Mbit/s, which enables the S/UNI-12xJET to be used as a 12-channel ATM cell delineator.
- Provides support for an arbitrary rate external transmission system interface up to a maximum rate of 52 Mbit/s, which enables the S/UNI-12xJET to be used as a 12-channel bit-HDLC processor.
- Compatible with PMC-Sierra T1/E1 frame/line interface chips for DS1 and E1 applications.
- Provides programmable pseudo-random test pattern generation, detection, and analysis features.
- Provides integral transmit data link and receive data link HDLC controllers with 128-byte FIFO depths for each serial channel.
- Provides performance-monitoring counters suitable for accumulation periods of up to 1 second.
- Provides a 16-bit microprocessor interface for configuration, control and status monitoring.
- Provides a standard 5-signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 3.3 V / 1.8 V CMOS technology with 5 V tolerant inputs.
- Available in a high-density 580-pin TSBGA package (35 mm x 35 mm) with 1 mm ball pitch.

2.2 System Side Interface

- Provides a UTOPIA Level 2 compatible 16-bit wide System Interface (clocked up to 52 MHz) with parity support for ATM applications.
- Provides a POS-PHY Level 2™ 16-bit System Interface (clocked up to 52 MHz) for HDLC packet and ATM applications.
- Provides UTOPIA Level 3 compatible 32-bit wide System Interface (clocked up to 104 MHz) with parity support for ATM applications.
- Provides POS-PHY Level 3™ 32-bit System Interface (clocked up to 104 MHz) for HDLC packet and ATM applications.
- Provides a four-cell (5 cell in Level 3 operation) FIFO for each channel in each direction for rate decoupling between the line and a higher layer processing entity for ATM applications. FIFO latency may be reduced by changing the number of operational cells per FIFO.
- Provides a 256 byte (320 byte in Level 3 operation) FIFO for each channel in each direction for rate decoupling between the line, and a higher layer processing entity for packet applications. FIFO fill level and reporting characteristics are programmable.

2.3 Serial Receiver

- Provides frame synchronization for the M23 or C-bit parity DS3 applications, alarm detection, and accumulates line code violations, framing errors, parity errors, path parity errors and FEBE events. In addition, far end alarm channel codes are detected, and an integral HDLC receiver is provided to terminate the path maintenance data link.
- Provides frame synchronization for the G.751 or G.832 E3 applications, alarm detection, and accumulates line code violations, framing errors, parity errors, and FEBE events. In addition, in G.832, the Trail Trace is detected and an integral HDLC receiver is provided to terminate either the Network Requirement or the General Purpose data link.
- Provides frame synchronization for G.704 and NTT 6.312 Mbit/s J2 applications, alarm detection, and accumulates line code violations, framing errors, and CRC parity errors. An integral HDLC receiver is provided to terminate the data link.
- Provides a receive HDLC controller with a 128-byte FIFO to accumulate data link information.
- Provides detection of yellow alarm and loss of frame (LOF), and accumulates BIP-8 errors, framing errors and FEBE events.
- Provides programmable pseudo-random test-sequence detection (up to 2^{32}-1 bit length patterns conforming to ITU-T O.151 standards) and analysis features.

2.4 Receive ATM Processor

- Provides frame synchronization, cell delineation and extraction for DS3, G.751 E3, G.832 E3, and G.704 and NTT J2 ATM direct-mapped formats.
- Provides PLCP frame synchronization, path overhead extraction, and cell extraction for DS1 PLCP, DS3 PLCP, E1 PLCP, and G.751 E3 PLCP formatted streams.

- Provides ATM framing using cell delineation. ATM cell delineation may optionally be disabled to allow passing of all cell bytes regardless of cell delineation status.
- Extracts ATM cells from the arbitrary STS-1/STM-0/STS-3c/STM-1/STS-12c/STM-4-4c SONET/SDH payloads using ATM cell delineation.
- Provides ATM cell payload descrambling.
- Performs header check sequence (HCS) error detectionand idle/unassigned cell filtering.
- Detects out of cell Delineation (OCD) and loss of cell delineation (LCD) alarms.
- Counts number of received cells, idle cells, erred cells and dropped cells.

2.5 Receive Bit HDLC Processor

- Supports packet based link layer protocols using bit synchronous HDLC framing like PPP, HDLC and Frame Relay.
- Performs flag sequence detection and terminates the received HDLC frames.
- Performs frame check sequence (FCS) validation for CRC-16.ISO-3309 and CRC-32 polynomials.
- Performs bit-destuffing of the HDLC stream.
- Detects for packet abort sequence.
- Checks for minimum and maximum packet lengths. Optionally deletes short packets and marks those exceeding the maximum length as erred.

2.6 Receive Byte HDLC Processor

- Supports packet based link layer protocols using byte synchronous HDLC framing like PPP, HDLC and Frame Relay.
- Extract frames from the arbitrary STS-1/STM-0/STS-3c/STM-1/STS-12c/STM-4-4c SONET/SDH payloads.
- Performs self-synchronous POS data descrambling on the arbitrary received payloads using the $x^{43}+1$ polynomial.
- Performs flag sequence detection and terminates the received POS frames.
- Performs frame check sequence (FCS) validation for CRC-16.ISO-3309 and CRC-32 polynomials.
- Performs control escape destuffing of the HDLC stream.
- Detects packet abort sequences.
- Checks for minimum and maximum packet lengths. Optionally deletes short packets and marks those exceeding the maximum length as erred.

2.7 Serial Transmitter

- Provides frame insertion for the M23 or C-bit parity DS3 applications, alarm insertion, and diagnostic features. In addition, far end alarm channel codes may be inserted, and an integral HDLC transmitter is provided to insert the path maintenance data link.
- Provides frame insertion for the G.751 or G.832 E3 applications, alarm insertion, and diagnostic features. In addition, for G.832, the Trail Trace is inserted, and an integral HDLC transmitter is provided to insert either the Network Requirement or the General Purpose data link.
- Provides frame insertion for G.704 6.312 Mbit/s J2 applications, alarm insertion, and diagnostic features. An integral HDLC transmitter is provided to insert the path maintenance data link.
- Provides a transmit HDLC controller with a 128-byte FIFO for data links information.
- Provides frame insertion and path overhead insertion for DS1, DS3, E1 or E3 based HDLC formats. In addition, alarm insertion and diagnostic features are provided.
- Provides programmable pseudo-random test sequence generation (up to 2^{32}-1 bit length sequences conforming to ITU-T O.151 standards). Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from 10^{-1} to 10^{-7}.

2.8 Transmit ATM Processor

- Provides frame insertion and path overhead insertion for DS1, DS3, E1 or E3 based PLCP formats. In addition, alarm insertion and diagnostic features are provided.
- Provides an 8 kHz reference input for locking the transmit PLCP frame rate to an externally applied frame reference.
- Insert ATM cells into arbitrary STS-1/STM-0/STS-3c/STM-1/STS-12c/STM-4-4c SONET/SDH payloads.
- Provides optional ATM cell scrambling, HCS generation/insertion, programmable idle cell insertion, diagnostics features and accumulates transmitted cells read from the FIFO.

2.9 The Transmit Bit HDLC Processor

- Supports any packet based link layer protocol using bit synchronous HDLC framing like PPP, HDLC and Frame Relay.
- Encapsulates packets within a HDLC frame.
- Performs flag sequence insertion.
- Performs bit stuffing for transparency processing.
- Performs frame check sequence generation using the CRC-16.ISO-3309 and CRC-32 polynomials.
- Aborts packets under the direction of the host or when the FIFO underflows.

2.10 The Transmit Byte HDLC Processor

- Supports any packet based link layer protocol using byte synchronous HDLC framing like PPP, HDLC and Frame Relay.
- Insert frames into arbitrary STS-1/STM-0/STS-3c/STM-1/STS-12c/STM-4-4c SONET/SDH payloads.
- Performs self-synchronous POS data scrambling using the $x^{43}+1$ polynomial.
- Encapsulates packets within a POS frame.
- Performs flag sequence insertion.
- Performs byte stuffing for transparency processing.
- Performs frame check sequence generation using the CRC-16.ISO-3309 and CRC-32 polynomials.
- Aborts packets under the direction of the host or when the FIFO underflows.

2.11 DS3/E3 Synchronizer

- Configurable to receive a serial data stream at either DS3 (44.736 Mbit/s) rate or E3 (34.368 Mbit/s) rate.
- Maps the DS3/E3 serial data stream into an STS-1/STM-0 SPE using either AU-3 mapping or TUG-3 mapping.
- Inserts DS3 and E3 AIS via a microprocessor register bit or automatic alarm controls.
- Provides an integral path maintenance data-link controller with a 128-byte FIFO for each channel.
- Sets all fixed stuff bits to zeros or ones as per microprocessor register bit.
- Controls elastic store overflow and underflow conditions.
- Performs C bit encoding for stuff request with selectable lock and fast lock modes of operation.
- Meets ITU and ANSI mapping jitter specifications.
- Can accommodate frequency offsets between the 6.48 MHz SONET clock and the E3/DS3 clock up to +/- 100 ppm.

2.12 DS3/E3 Desynchronizer

- Extracts DS3 / E3 data from an STS-1/STM-0 SPE and outputs nominal rate E3 (34 368 kb/s) or DS3 (44 736 kb/s) serial data streams.
- Capable of demapping DS3 / E3 data using either AU-3 mapping or TUG-3 mapping.
- Generates smooth DS3 / E3 clock and data, using a free-running external reference clock, that are compliant with ITU and ANSI demapping jitter specifications.

- Absorbs pointer movements and DS3 / E3 payload bit stuffs in an elastic store, and controls outgoing clock phase using the smooth clock generator circuit with selectable lock and fast lock modes of operation.
- Detects elastic store FIFO underrun and overrun conditions. The elastic store has an auto center mechanism that separates the read and write pointers under normal operating conditions and after underrun / overflow events occur.
- Provides an integral path maintenance data-link controller with a 128-byte FIFO for each channel.
- Supports AIS generation in both DS3 and E3 modes.
- Can tolerate frequency offsets between the 6.48 MHz SONET clock and the external reference DS3 / E3 clock up to +/- 100 ppm.

2.13 SERDES Interface

- Provides a duplex 8-bit 77.76 MHz STS-12/STM-4 line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.

2.14 TelecomBus/Add-Drop Interface

- Provides a duplex 77.76 MHz 8-bit wide ingress and egress parallel TelecomBus line side interfaces.
- Provides capacity to carry an STS-12/STM-4 stream on the TelecomBus interface.
- TelecomBus interfaces indicates/accepts the location of the section trace byte (J0), optionally the path trace byte(s) (J1) and all synchronous payload envelope bytes in the byte serial stream.
- TelecomBus accommodates phase and frequency differences between the receive/transmit streams and the DROP/ADD busses via pointer adjustments.
- Provides a limited time slot interchange function to interchange or groom paths on the Telecom ADD and DROP buses.

2.15 Section and Line / SDH Regenerator and Multiplexer Section

- Frames to the SONET/SDH receive stream and inserts the framing bytes (A1, A2) and the section trace byte (J0) into the transmit stream; descrambles the receive stream and scrambles the transmit stream.
- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1, B2 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1). Inserts line remote error indications (REI) into the M1 byte based on received B2 errors.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.
- The entire SONET/SDH transport overhead is extracted to and inserted from dedicated pins. The transport overhead bytes may be sourced from internal registers or from the bit serial transport overhead input stream. Transport overhead insertion may also be disabled.

- Extracts and serializes on dedicated pins the data communication channels (D1-D3 or D4-D12) and inserts the corresponding signals into the transmit stream.
- Extracts and filters the automatic protection switch (APS) channel (K1, K2) bytes into internal registers. Inserts the APS channel into the transmit stream.
- Extracts and filters the synchronization status message (S1) byte into an internal register. Inserts the synchronization status message byte into the transmit stream.
- Extracts a 16 or 64 byte section trace (J0) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the accepted message via the microprocessor port. Inserts a 16 byte or 64 byte section trace (J0) message using an internal register bank for the transmit stream.
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI), line alarm indication signal (AIS), and protection switching byte failure alarms on the receive stream.
- Configurable to force Line AIS in the transmit stream.
- Provides automatic transmit line RDI insertion following detection of various received alarms (LOS, LOF, LAIS, SD, SF, STIM, STIU).

2.16 SONET Path / SDH High Order Path

- Interprets any legal mix of STS (AU and TU3) pointer bytes (H1, H2, and H3), extracts the synchronous payload envelope(s) and processes the path overhead for the receive stream.
- Generates any legal mix of STS (AU and TU3) pointer bytes (H1, H2, and H3) and inserts the path overhead for the transmit stream.
- Detects loss of pointer (LOP), path alarm indication signal (PAIS) and path (normal and enhanced) remote defect indication (RDI) for the receive stream. Optionally inserts path alarm indication signal (PAIS) and path remote defect indication (RDI) in the transmit stream.
- Extracts and inserts the entire SONET/SDH path overhead to and from dedicated pins. The path overhead bytes may be sourced from internal registers or from the bit serial path overhead input stream. Path overhead insertion may also be disabled.
- Extracts the received path payload label (C2) byte into an internal register and detects for payload label unstable (PLU), payload label mismatch (PLM), payload unequipped (UNEQ) and payload defect indication (PDI). Inserts the path payload label (C2) byte from an internal register for the transmit stream.
- Extracts a 16 byte or 64 byte path trace (J1) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the captured, accepted and expected message via the microprocessor port. Inserts a 16 byte or 64 byte path trace (J1) message using an internal register bank for the transmit stream.
- Calculates received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream.

- Counts received path remote error indications (REI) for performance monitoring purposes. Optionally inserts the path REI count into the path status byte (G1) based on bit or block BIP-8 errors detected in the receive path.
- Provides automatic transmit path RDI and path Enhanced RDI insertion following detection of various received alarms (LAIS, LOP, LOPC, PAIS, PAISC, PTIM, PTIU, PLM, PLU, UNEQ, PDI).
- Provides automatic DROP bus path AIS insertion following detection of various received alarms (LAIS, LOP, LOPC, PAIS, PAISC, PTIM, PTIU, PLM, PLU, UNEQ, PDI).

2.17 Bypass and Loopback Features

- Allows bypassing of the DS3, E3, and J2 framers to enable transmission system external processing by an external device.
- Allows bypassing of the PLCP and ATM functions to enable use of the S/UNI-12xJET as a twelve-channel DS3, E3, or J2 framer.
- Provides for diagnostic loopbacks, line loopbacks, and payload loopbacks.

2.18 Device Interworking

Other PMC-Sierra devices that implement the POS-PHY Level 3 interface include:

- S/UNI 2488: SATURN User Network Interface for 2488 Mbit/s
- S/UNI 4x622: Quad Channel OC-12c ATM and POS
- S/UNI 2xGE: Dual Gigabit Ethernet Controller
- S/UNI MACH48: Multi-Service Access Device for Channelized Interfaces
- S/UNI ATLAS-3200 - 2.488G ATM Layer Solution

3 Applications

- ATM or SMDS Switches, Multiplexers, and Routers
- SONET/SDH Mux E3/DS3 Tributary Interfaces
- PDH Mux J2/E3/DS3 Line Interfaces
- DS3/E3/J2 Digital Cross Connect Interfaces
- DS3/E3/J2 PPP Internet Access Interfaces
- DS3/E3/J2 Frame Relay Interfaces
- SONET/SDH Add/Drop Multiplexers with data processing capabilities
- Multi-Service Switches.

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5 Application Examples

The S/UNI® 12xJET device provides a complete physical layer solution for the aggregation, transport and termination of up to 12 channels of DS3/E3 and J2 protocols. The S/UNI 12xJET provides substantial functional flexibility due to its broad processing capabilities and vast array of supported interfaces (Utopia 2, POS-PHY™ Level 2, UTOPIA 3, POS-PHY Level 3™, Telecom bus, Parallel OC-12 SERDES, DS3/E3/J2 serial). As such, the S/UNI 12xJET is applicable in both next generation equipment as well as line card upgrades to in-field systems. The following sections provide high level descriptions and diagrams for potential applications, including:

- 12 x DS3, E3, J2 ATM Termination
- 12 x DS3, E3, J2 Packet Termination
- Channelized OC-12 SONET/SDH with DS3, E3 and J2 ATM/HDLC
- Channelized OC-12 SONET/SDH serial multiplexer
- Channelized OC-48 SONET/SDH serial multiplexer
- 48xDS3/E3 Aggregation Metro Core MSPP Application
- Channelized OC-12 SONET/SDH with Add/Drop capabilities
- Sub rate processing using S/UNI 12xJET

The S/UNI-12xJET device can be configured as strictly an ATM physical layer device. On the line side, it connects to one or more J2/E3/T3 line interface units and on the system side, the S/UNI-12xJET interfaces to the ATM layer device over a 16-bit wide UTOPIA Level 2 interface (shown in Figure 1) or 32-bit wide UTOPIA Level 3 interface (shown in Figure 2).

Figure 1 Typical S/UNI-12xJET ATM (UTOPIA Level 2) Application

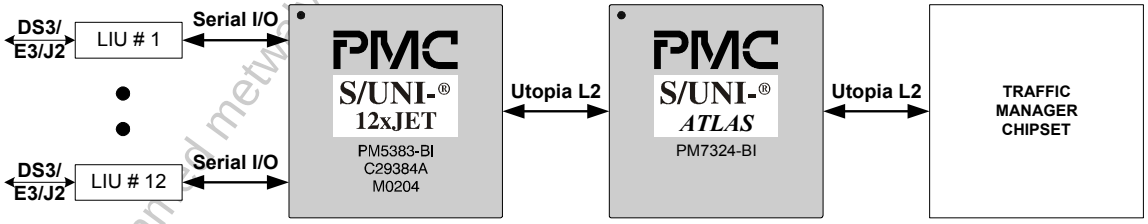
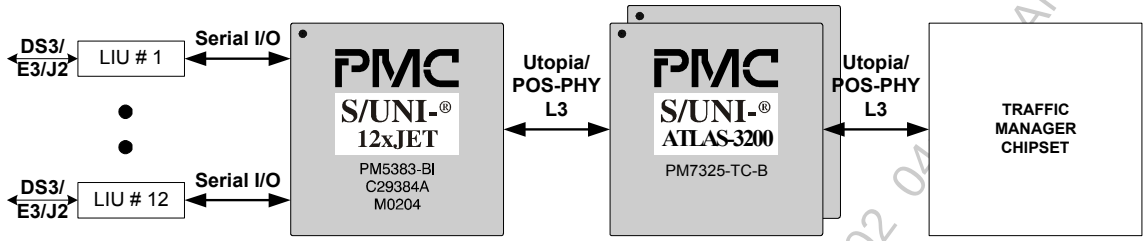


Figure 2 Typical S/UNI-12xJET ATM (UTOPIA or POS-PHY Level 3) Application

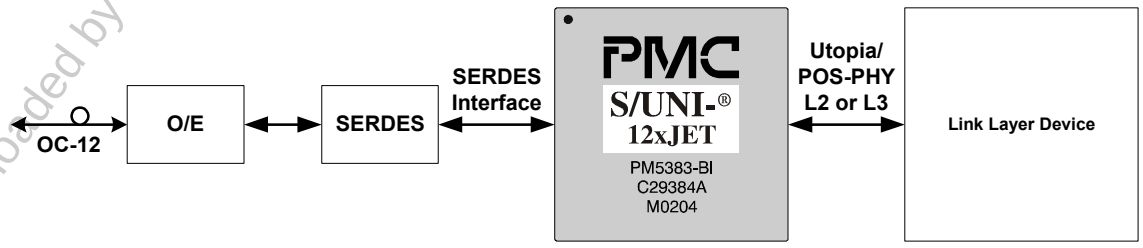


The S/UNI-12xJET can be configured as packet and/or ATM physical layer device. On the line side, it connects to one or more J2/E3/T3 line interface units and on the system side, the S/UNI-12xJET interfaces to the layer device over a 16-bit wide POS-PHY™ Level 2 interface or 32-bit wide POS-PHY Level 3™ interface (shown in Figure 3).

Figure 3 Typical S/UNI-12xJET Packet (POS-PHY Level 2) Application

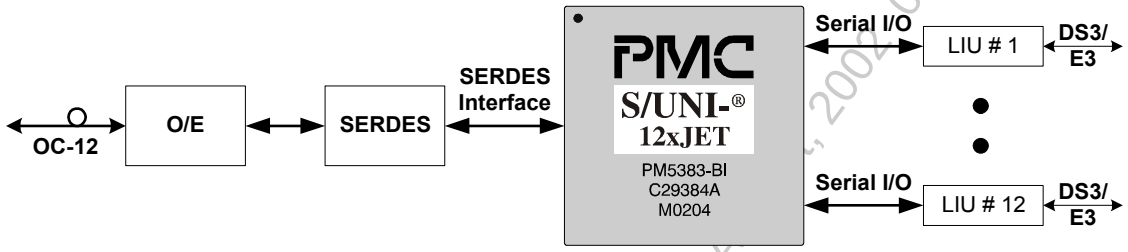
The S/UNI-12xJET can be configured as packet and/or ATM physical layer device for SONET/SDH applications requiring ATM, POS, DS3 or E3. On the line side, it connects to an external serializer-deserializer (SERDES) with clock synthesis and clock recovery using the duplex 8-bit 77.76MHz interface. On the system side, the S/UNI-12xJET interfaces to the link layer device over either a UTOPIA Level 2, UTOPIA Level 3, POS-PHY Level 2, or POS-PHY Level 3 interface (shown in Figure 4).

Figure 4 Typical S/UNI-12xJET OC-12 SONET/SDH with DS3/E3/ATM/HDLC Packet Application



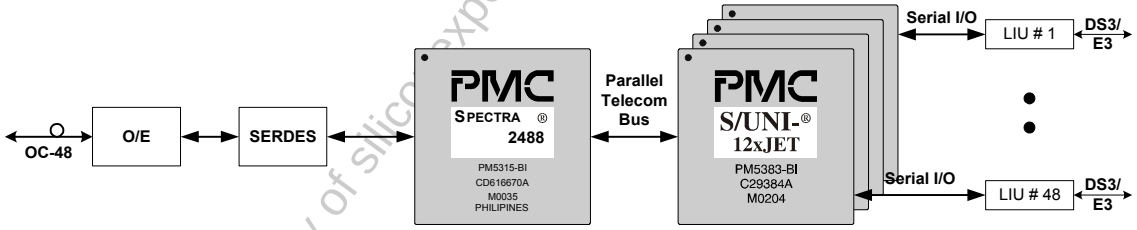
The S/UNI-12xJET can be configured as DS3 and/or E3 transport device, for SONET/SDH applications. On the line side, it connects to an external SERDES with clock synthesis and clock recovery using the duplex 8-bit 77.76MHz interface. On the system side, the S/UNI-12xJET connects to one or more E3/DS3 line interface units as shown in Figure 5.

Figure 5 Typical S/UNI-12xJET OC-12 SONET/SDH Serial Multiplex Application



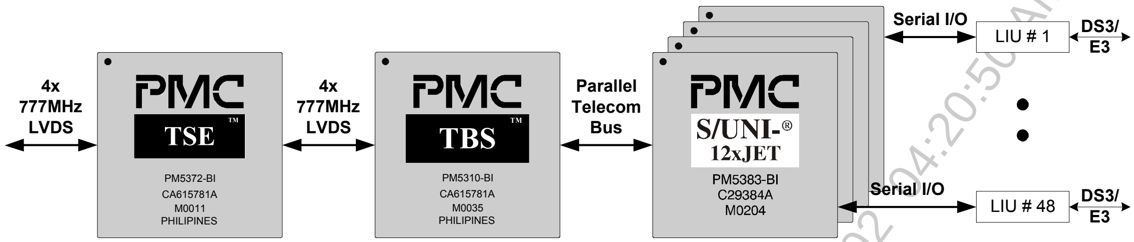
The S/UNI-12xJET can be used for STS-48/STM-16 SONET/SDH applications. As shown in Figure 6, four S/UNI-12xJET devices can be used to connect to an STS-48/STM-16 SONET/SDH processor such as a PM5315 SPECTRA-2488. The four 8-bit 77.76MHz duplex buses are combined to form the required 32-bit 77.76MHz duplex bus.

Figure 6 Typical S/UNI-12xJET OC-48 SONET/SDH Serial Multiplex Application



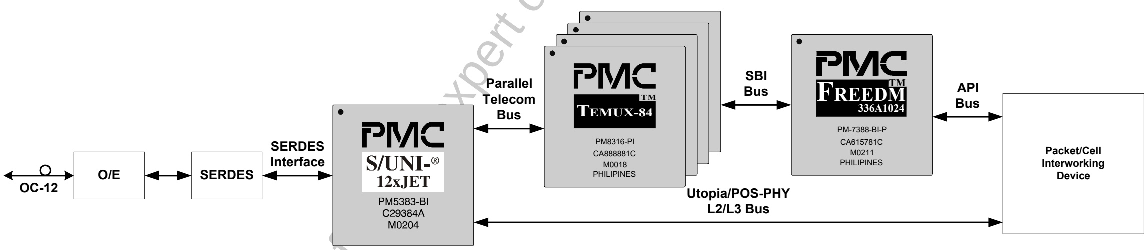
The S/UNI-12xJET can be used for 48xDS3/E3 Transport Termination Line cards in an Aggregation Metro Core MSPP Application. As shown in Figure 7, four S/UNI-12xJET devices can be used to connect to a TelecomBus Serializer (TBS) PM5310 to make up a transport termination line card. The serialized TelecomBus can then be sent to a Transmission Switching Element (TSE) PM5312 as part of a MSPP application.

Figure 7 Typical S/UNI-12xJET 48xDS3/E3 Aggregation Metro Core MSPP Application



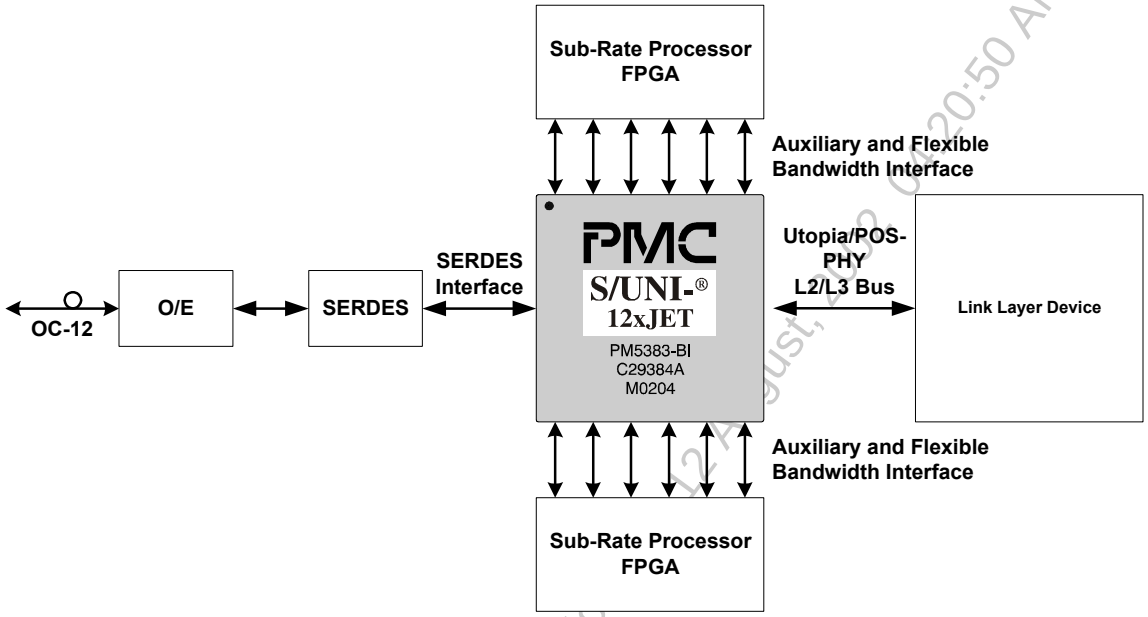
The S/UNI-12xJET can be used to fully or partially terminate SONET/SDH applications requiring ATM, POS, DS3 or E3. As shown in Figure 4, the S/UNI-12xJET is able to terminate ATM, POS, DS3 or E3 traffic from an OC-12 SONET/SDH network. Using the duplex 8-bit parallel TelecomBus interface as an Add/Drop bus, the S/UNI-12xJET is able to terminate a OC-12 SONET/SDH stream and interoperate with other devices, such as the PM8316 TEMUX-84™ device. This mode, shown in Figure 8, allows for higher channelization and/or other services to be provided over the same OC-12 SONET/SDH network.

Figure 8 Typical S/UNI-12xJET OC-12 SONET/SDH with Add/Drop Capabilities Application



The S/UNI-12xJET can be used in conjunction with external programmable logic (FPGA) to support sub-rate processing applications, such as fractional DS3. Data from/to the cell/frame processors within the S/UNI-12xJET is routed through the flexible bandwidth interface to allow an external FPGA to perform sub-rate processing on the data. The data is then routed through the Auxiliary Serial Interface to the DS3/E3 framer and transmitter blocks. A typical sub-rate processing application is shown in Figure 9.

Figure 9 Typical S/UNI-12xJET Sub-rate Processing Application



6 Block Diagram

Figure 10 S/UNI-12xJET Block Diagram

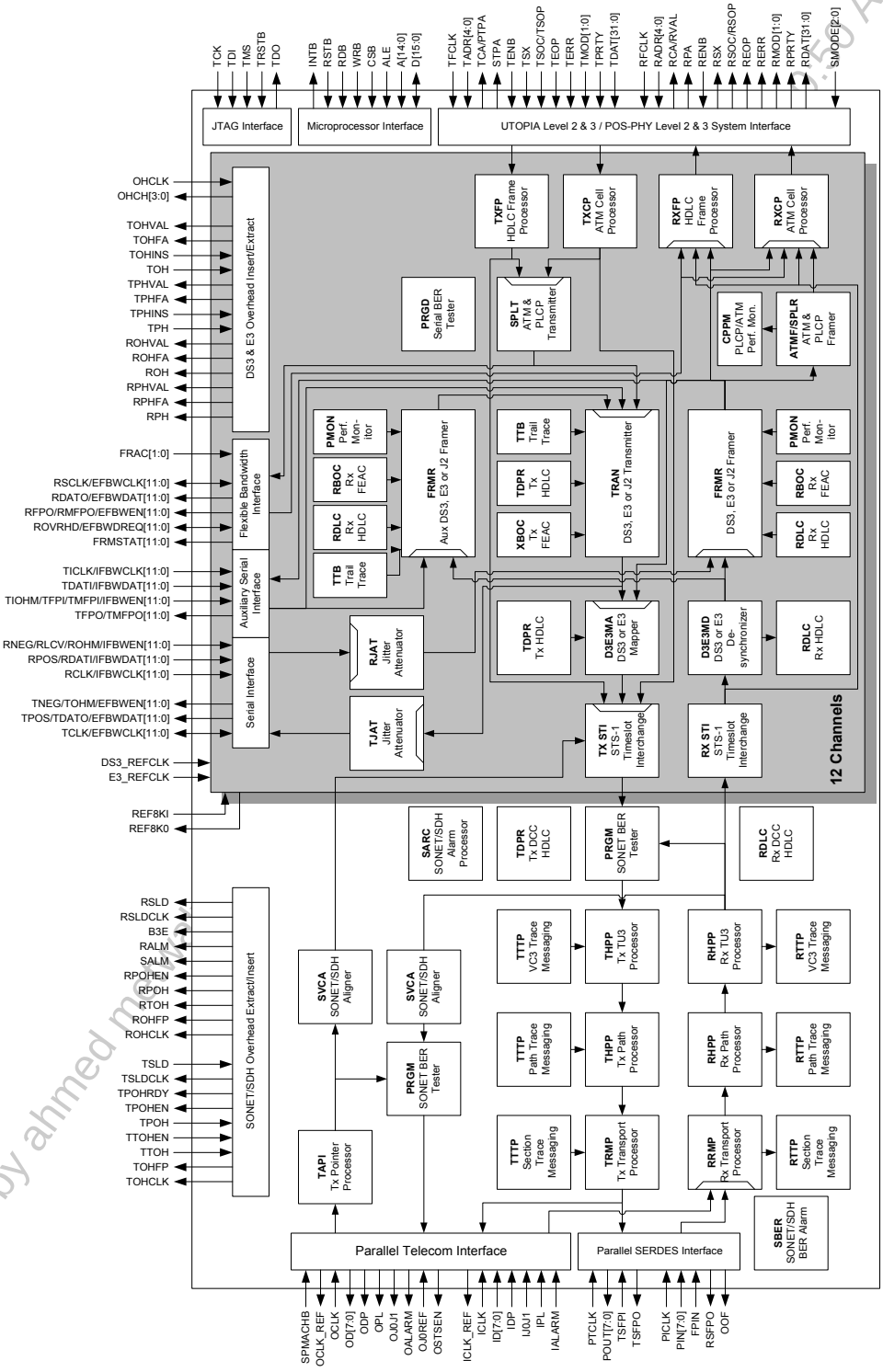


Figure 11 S/UNI-12xJET Diagnostic Loopbacks

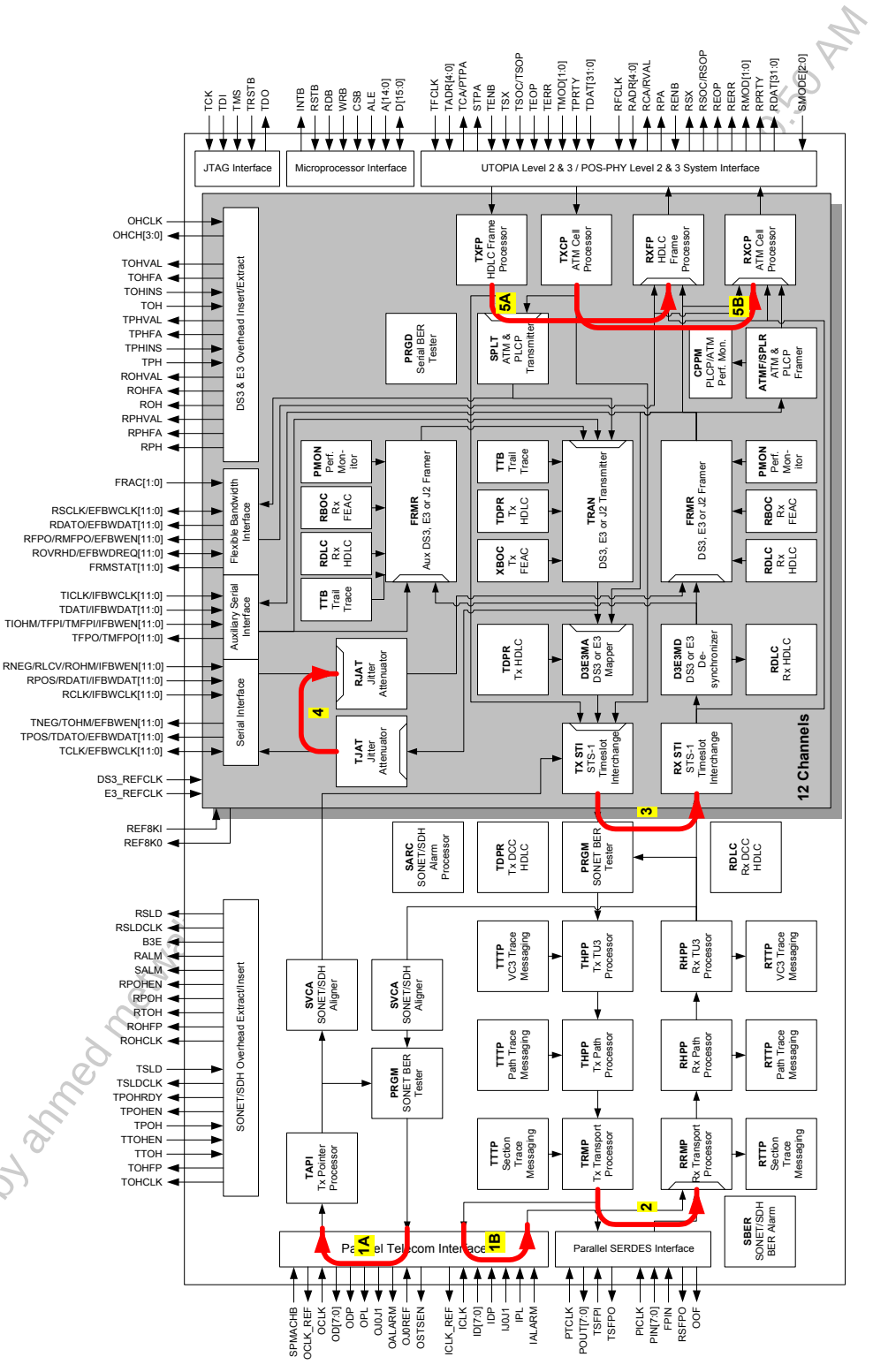
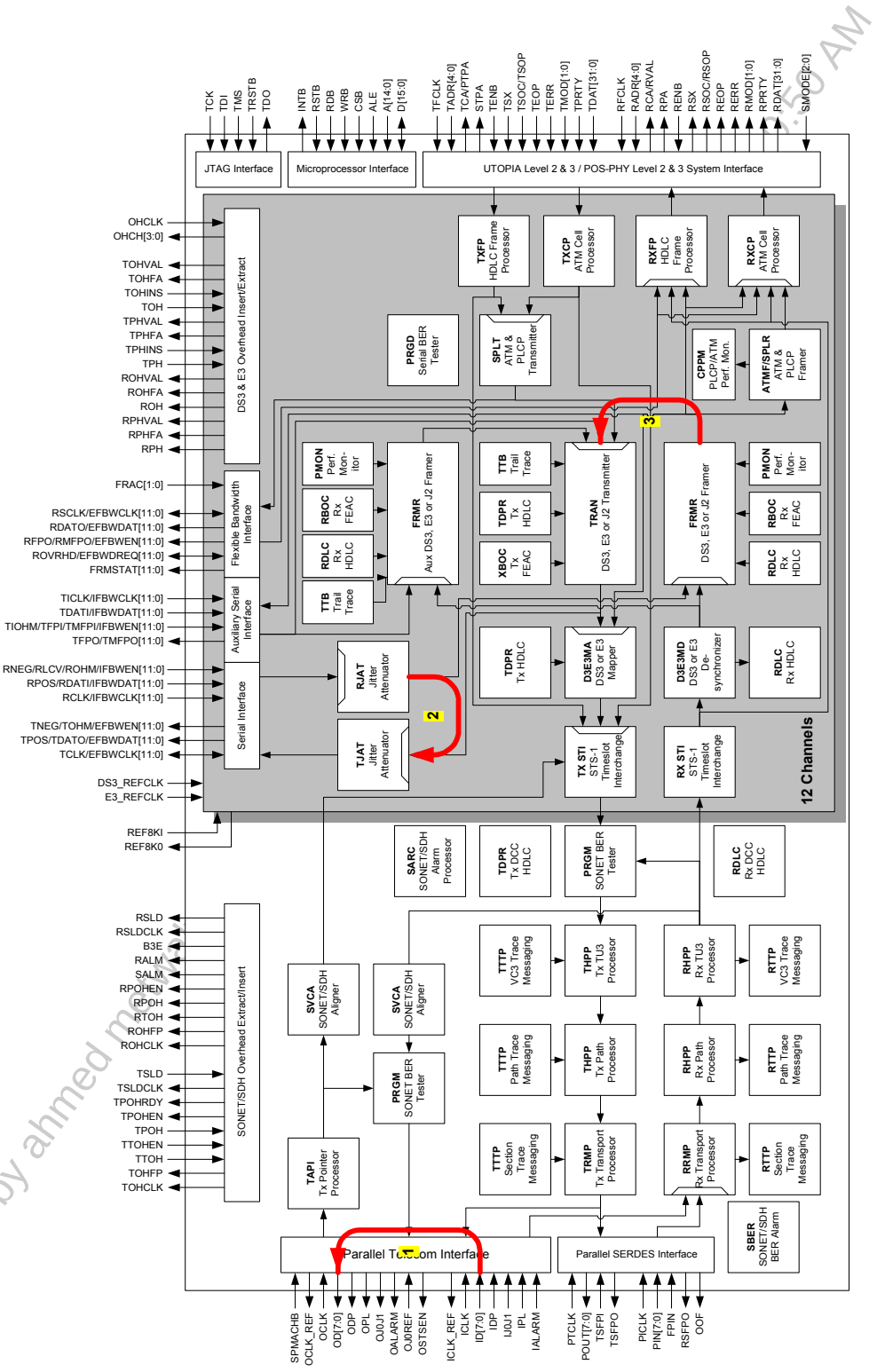


Figure 12 S/UNI-12xJET Line Loopbacks



7 Description

7.1 Serial Framer/Transmitter Processing

The PM5383 S/UNI-12xJET is a 12-channel ATM and packet physical layer processor with integrated DS3, E3, and J2 framers. HDLC sub-layer DS1, DS3, E1, and E3 processing is supported. Both ATM cell delineation and bit-synchronous HDLC for packet delineation are supported. Mixtures of DS3 and E3 modes are allowed, as well as mixtures of ATM/PLCP, HDLC, and bit-synchronous HDLC packet delineation.

The S/UNI-12xJET contains integral DS3, E3 and J2 framers. DS3 framing and error accumulation is in accordance with ANSI T1.107 and T1.107a specifications. E3 framing and error accumulation is in accordance with ITU-T Recommendations G.832 and G.751. J2 framing and error accumulation is in accordance with ITU-T Recommendation G.704 and I.432.

For DS3, E3 and J2 transmission system processing, the S/UNI-12xJET provides a generic interface for physical sub-layer processing and supports both bipolar and unipolar data encoding with serial line rate clocks. When configured for DS1 or E1 transmission system sub-layer processing, the S/UNI-12xJET accepts and outputs unipolar signals with appropriate clock and frame pulse signals for physical sub-layer processing.

The S/UNI-12xJET detects problems on the serial links such as line code violations, loss of signal, framing bit errors, parity errors, path parity errors, AIS, far end receive failure, CRC failures and idle code applicable for each protocol. Appropriate events are counted for performance monitoring and alarm generation purposes. Bit-synchronous HDLC receivers and trace messages are provided to support data link support when necessary. The S/UNI-12xJET allows the DS3, E3 and J2 overhead to be extracted to pins allowing external custom processing.

The S/UNI-12xJET performs various tasks such as frame insertion, parity calculations, path parity calculation, AIS generation, CRC insertion, idle code insertion. PRBS insertion and verification allows performance verification of a serial link. Bit-synchronous HDLC transmitters and trace messages are provided to support data link support when necessary. The S/UNI-12xJET allows the custom DS3 and E3 overhead to be inserted from external generators or from internal registers.

The S/UNI-12xJET also supports diagnostic options that allow it to insert, when appropriate for the transmit framing format, parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, all-zeros, AIS, Remote Alarm Indications, and Remote End Alarms.

7.2 ATM/Bit-HDLC Processing

The S/UNI-12xJET provides ATM cell generation and ATM cells delineation using the PLCP framing format, or by using the header check sequence octet in the ATM cell header. Non-PLCP-based cell delineation is accomplished with bit, nibble, or byte-wide search algorithms. A generic physical interface supporting arbitrary rates for serial ATM processing is provided at rates up to 52 Mbit/s.

In the PLCP receive direction, framing, path overhead extraction and cell extraction are provided. BIP-8 error events, frame octet error events and far end block error events are accumulated. In the PLCP transmit direction, the S/UNI-12xJET provides overhead insertion using inputs or internal registers, DS3 nibble and E3 byte stuffing, automatic BIP-8 octet generation and insertion and automatic far end block error insertion. Diagnostic features for BIP-8 error, framing error and far end block error insertion are also supported.

The S/UNI-12xJET also provides bit-synchronous HDLC packet generation and delineation. HDLC packets are automatically aborted when FIFO underrun events occur. Both 16-bit and 32-bit FCS generation and verification are supported by the device. A generic physical interface supporting arbitrary rates for serial bit-synchronous HDLC processing is provided at rates up to 52 Mbit/s.

7.3 SONET/SDH Processing

The S/UNI-12xJET can be configured to use a duplex 8-bit 77.76 MHz parallel line-side interface for direct connection to an external clock recovery, clock synthesis and serializer-deserializer for STS-12/STM-4 applications. The device can also be configured as a duplex 8-bit 77.76 MHz TTL compatible TelecomBus interface, and may then be combined with three other S/UNI-12xJET devices to form a 32-bit 77.76MHz STS-48/STM-16 TelecomBus compatible interface. The parallel TelecomBus interface is compatible with SONET/SDH framers such as the SPECTRA-2488.

The device performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section and line BIPs (B1, B2) as required to allow performance monitoring at the far end. Line remote error indications (M1) are optionally inserted. A 16 or 64 byte section trace (J0) message may be inserted. In addition, the S/UNI-12xJET generates the transmit payload pointers (H1, H2), creates and inserts the path BIP, optionally inserts a 16 or 64 byte path trace (J1) message, and optionally inserts the path status byte (G1).

In addition to basic processing of the transmit SONET/SDH overhead, the S/UNI-12xJET provides convenient access to all overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of overhead. The S/UNI-12xJET also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors and BIP errors, which are useful for system diagnostics and tester applications.

The S/UNI-12xJET implements ATM, Packet over SONET/SDH (byte-synchronous HDLC), DS3 and E3 mapping functions for a channelized STS-12/STM-4 stream. The stream can consist of a single STS-12c/STM-4c or a combination of STS-3c/STM-4c, STS-1/STM-0, DS3 mapped and E3 mapped channels. Arbitrary STS-1 assignments are support for ATM and POS applications requiring non-standard concatenated payloads.

Incoming SPE (VC) payloads may be desynchronized into DS3 or E3 streams that meet applicable jitter and wander specifications. Incoming DS3 or E3 streams may be mapped into outgoing SPE (VC) payloads using intelligent bit-stuff algorithms. The S/UNI-12xJET supports mapping into DS3 and E3 streams and into AU3 and AU4 SPE via TU3 payloads.

7.4 System Side Interfaces

The S/UNI-12xJET supports UTOPIA Level 2, UTOPIA Level 3, POS-PHY Level 2 and POS-PHY Level 3 system interfaces for ATM and HDLC packet data. ATM cells are buffered in 4-cell per-channel FIFOs in Level 2 operation and 5-cell per-channel FIFOs in Level 3 operation. Packet data is buffered in 256-byte per-channel FIFOs in Level 2 operation and 320-byte per-channel FIFOs in Level 3 operation. Performance information such as the number of cells/packets transmitted /received and number of erred cells/packets are accumulated. Mixed channel configurations for ATM and packet operation are supported using the POS-PHY Level 3 mode.

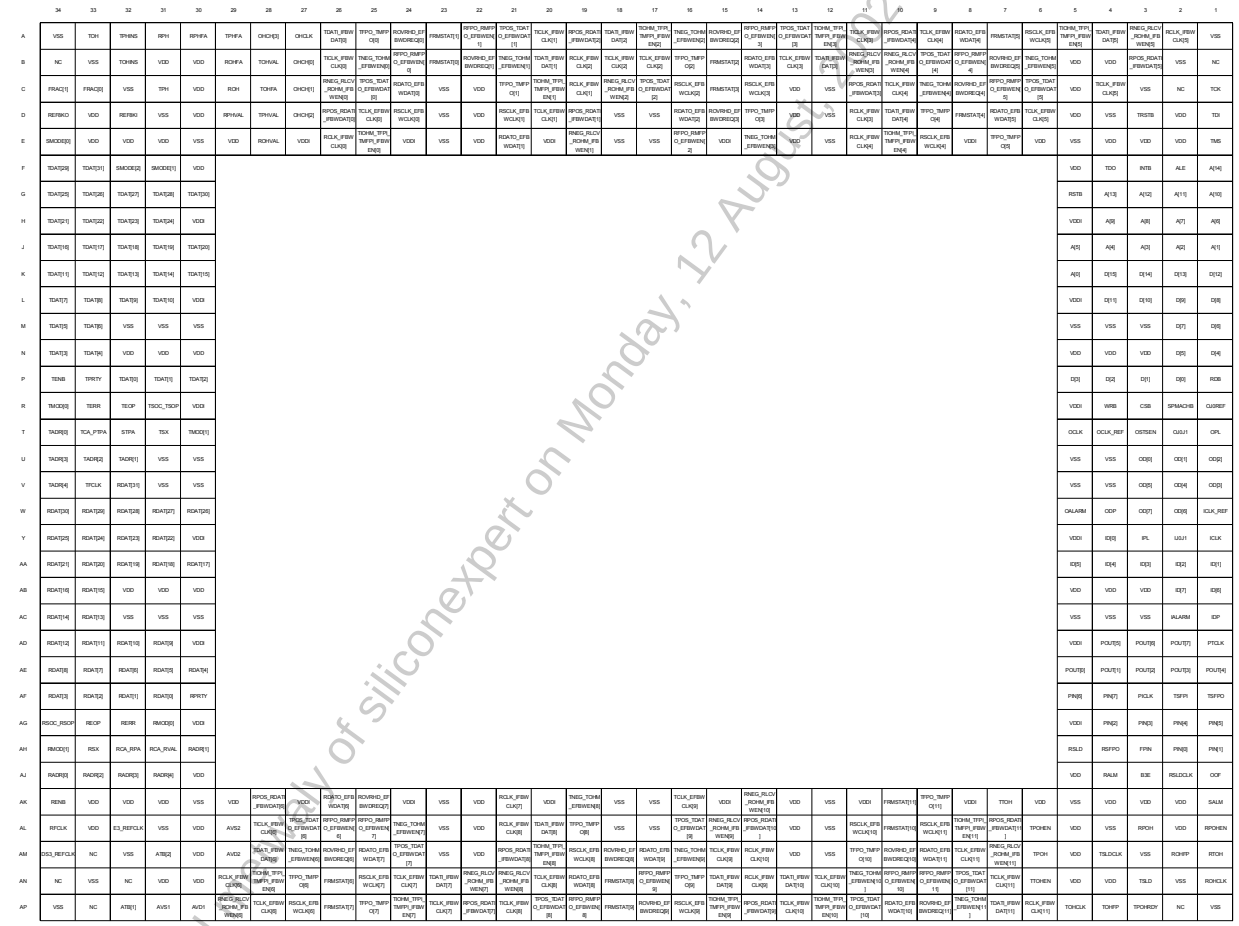
The S/UNI-12xJET is configured, controlled and monitored via a generic 16-bit microprocessor bus interface. The S/UNI-12xJET also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI-12xJET is implemented in low power, +1.8 Volt, CMOS technology with 3.3V TTL compatible digital inputs and 3.3V TTL/CMOS compatible digital outputs. The S/UNI-12xJET is packaged in a 580-pin TSBGA package.

8 Pin Diagram

The S/UNI-12xJET is packaged in a 580-pin TSBGA package having a body size of 35mm by 35mm and a pitch of 1mm.

8.1 Pin Diagram (Bottom View)



8.2 Pin Diagram Top Right (Bottom View)

	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
A	VSS	TOH	TPHINS	RPH	RPHFA	TPHFA	OHCH[3]	OHCLK	TDATI_IFBWDAT[0]	TFPO_TMFPO[0]	ROVRHD_EFBWDREQ[0]	FRMSTAT[1]	RFPO_RMFPO_EFBWEN[1]	TPOS_TDATO_EFBWDAT[1]	TICLK_IFBWCLK[1]	RPOS_RDATI_IFBWDAT[2]	TDATI_IFBWDAT[2]
B	NC	VSS	TOHINS	VDD	VDD	ROHFA	TOHVAL	OHCH[0]	TICLK_IFBWCLK[0]	TNEG_TOHM_EFBWEN[0]	RFPO_RMFPO_EFBWEN[0]	FRMSTAT[0]	ROVRHD_EFBWDREQ[1]	TNEG_TOHM_EFBWEN[1]	TDATI_IFBWDAT[1]	RCLK_IFBWCLK[2]	TICLK_IFBWCLK[2]
C	FRAC[1]	FRAC[0]	VSS	TPH	VDD	ROH	TOHFA	OHCH[1]	RNEG_RLCV_ROHM_IFBWEN[0]	TPOS_TDATO_EFBWDAT[0]	RDATO_EFBWDAT[0]	VSS	VDD	TFPO_TMFPO[1]	TIOHM_TFPI_TMFPI_IFBWEN[1]	RCLK_IFBWCLK[1]	RNEG_RLCV_ROHM_IFBWEN[2]
D	REF8KO	VDD	REF8KI	VSS	VDD	RPHVAL	TPHVAL	OHCH[2]	RPOS_RDATI_IFBWDAT[0]	TCLK_EFBWCLK[0]	RSCLK_EFBWCLK[0]	VSS	VDD	RSCLK_EFBWCLK[1]	TCLK_EFBWCLK[1]	RPOS_RDATI_IFBWDAT[1]	VSS
E	SMODE[0]	VDD	VDD	VDD	VSS	VDD	ROHVAL	VDDI	RCLK_IFBWCLK[0]	TIOHM_TFPI_TMFPI_IFBWEN[0]	VDDI	VSS	VDD	RDATO_EFBWDAT[1]	VDDI	RNEG_RLCV_ROHM_IFBWEN[1]	VSS
F	TDAT[29]	TDAT[31]	SMODE[2]	SMODE[1]	VDD												
G	TDAT[25]	TDAT[26]	TDAT[27]	TDAT[28]	TDAT[30]												
H	TDAT[21]	TDAT[22]	TDAT[23]	TDAT[24]	VDDI												
J	TDAT[16]	TDAT[17]	TDAT[18]	TDAT[19]	TDAT[20]												
K	TDAT[11]	TDAT[12]	TDAT[13]	TDAT[14]	TDAT[15]												
L	TDAT[7]	TDAT[8]	TDAT[9]	TDAT[10]	VDDI												
M	TDAT[5]	TDAT[6]	VSS	VSS	VSS												
N	TDAT[3]	TDAT[4]	VDD	VDD	VDD												
P	TENB	TPRTY	TDAT[0]	TDAT[1]	TDAT[2]												
R	TMOD[0]	TERR	TEOP	TSOC_TSOP	VDDI												
T	TADR[0]	TCA_PTPA	STPA	TSX	TMOD[1]												
U	TADR[3]	TADR[2]	TADR[1]	VSS	VSS												

8.3 Pin Diagram Bottom Right (Bottom View)

	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
V	TADR[4]	TFCLK	RDAT[31]	VSS	VSS												
W	RDAT[30]	RDAT[29]	RDAT[28]	RDAT[27]	RDAT[26]												
Y	RDAT[25]	RDAT[24]	RDAT[23]	RDAT[22]	VDDI												
AA	RDAT[21]	RDAT[20]	RDAT[19]	RDAT[18]	RDAT[17]												
AB	RDAT[16]	RDAT[15]	VDD	VDD	VDD												
AC	RDAT[14]	RDAT[13]	VSS	VSS	VSS												
AD	RDAT[12]	RDAT[11]	RDAT[10]	RDAT[9]	VDDI												
AE	RDAT[8]	RDAT[7]	RDAT[6]	RDAT[5]	RDAT[4]												
AF	RDAT[3]	RDAT[2]	RDAT[1]	RDAT[0]	RPRTY												
AG	RSOC_RSOP	REOP	RERR	RMOD[0]	VDDI												
AH	RMOD[1]	RSX	RCA_RPA	RCA_RVAL	RADR[1]												
AJ	RADR[0]	RADR[2]	RADR[3]	RADR[4]	VDD												
AK	RENB	VDD	VDD	VDD	VSS	VDD	RPOS_RDATI_IFBWDAT[6]	VDDI	RDATO_EFBWDAT[6]	ROVRHD_EFBWDREQ[7]	VDDI	VSS	VDD	RCLK_IFBWCLK[7]	VDDI	TNEG_TOHM_EFBWEN[8]	VSS
AL	RFCLK	VDD	E3_REFCLK	VSS	VDD	AVS2	TICLK_IFBWCLK[6]	TPOS_TDATO_EFBWDAT[6]	RFPO_RMFPO_EFBWEN[6]	RFPO_RMFPO_EFBWEN[7]	TNEG_TOHM_EFBWEN[7]	VSS	VDD	RCLK_IFBWCLK[8]	TDATI_IFBWDAT[8]	TFPO_TMFPO[8]	VSS
AM	DS3_REFCLK	NC	VSS	ATB[2]	VDD	AVD2	TDATI_IFBWDAT[6]	TNEG_TOHM_EFBWEN[6]	ROVRHD_EFBWDREQ[6]	RDATO_EFBWDAT[7]	TPOS_TDATO_EFBWDAT[7]	VSS	VDD	RPOS_RDATI_IFBWDAT[8]	TIOHM_TFPI_TMFPI_IFBWEN[8]	RSCLK_EFBWCLK[8]	ROVRHD_EFBWDREQ[8]
AN	NC	VSS	NC	VDD	VDD	RCLK_IFBWCLK[6]	TIOHM_TFPI_TMFPI_IFBWEN[6]	TFPO_TMFPO[6]	FRMSTAT[6]	RSCLK_EFBWCLK[7]	TCLK_EFBWCLK[7]	TDATI_IFBWDAT[7]	RNEG_RLCV_ROHM_IFBWEN[7]	RNEG_RLCV_ROHM_IFBWEN[8]	TCLK_EFBWCLK[8]	RDATO_EFBWDAT[8]	FRMSTAT[8]
AP	VSS	NC	ATB[1]	AVS1	AVD1	RNEG_RLCV_ROHM_IFBWEN[6]	TCLK_EFBWCLK[6]	RSCLK_EFBWCLK[6]	FRMSTAT[7]	TFPO_TMFPO[7]	TIOHM_TFPI_TMFPI_IFBWEN[7]	TICLK_IFBWCLK[7]	RPOS_RDATI_IFBWDAT[7]	TICLK_IFBWCLK[8]	TPOS_TDATO_EFBWDAT[8]	RFPO_RMFPO_EFBWEN[8]	FRMSTAT[9]

8.4 Pin Diagram Bottom Left (Bottom View)

												VSS	VSS	OD[5]	OD[4]	OD[3]	V
												OALARM	ODP	OD[7]	OD[6]	ICLK_REF	W
												VDDI	ID[0]	IPL	IJOJ1	ICLK	Y
												ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	AA
												VDD	VDD	VDD	ID[7]	ID[6]	AB
												VSS	VSS	VSS	IALARM	IDP	AC
												VDDI	POUT[5]	POUT[6]	POUT[7]	PTCLK	AD
												POUT[0]	POUT[1]	POUT[2]	POUT[3]	POUT[4]	AE
												PIN[6]	PIN[7]	PICLK	TSFPI	TSFPO	AF
												VDDI	PIN[2]	PIN[3]	PIN[4]	PIN[5]	AG
												RSLD	RSFPO	FPIN	PIN[0]	PIN[1]	AH
												VDD	RALM	B3E	RSLDCLK	OOF	AJ
VSS	TCLK_EFBWCLK[9]	VDDI	RNEG_RLCV_ROHM_IFBWEN[10]	VDD	VSS	VDDI	FRMSTAT[11]	TFPO_TMFPO[11]	VDDI	TTOH	VDD	VSS	VDD	VDD	VDD	SALM	AK
VSS	TPOS_TDATO_EFBWDAT[9]	RNEG_RLCV_ROHM_IFBWEN[9]	RPOS_RDATI_IFBWDAT[10]	VDD	VSS	RSCLK_EFBWCLK[10]	FRMSTAT[10]	RSCLK_EFBWCLK[11]	TIOHM_TFPI_TMFPI_IFBWEN[11]	RPOS_RDATI_IFBWDAT[11]	TPOHEN	VDD	VSS	RPOH	VDD	RPOHEN	AL
RDATO_EFBWDAT[9]	TNEG_TOHM_EFBWEN[9]	TICLK_IFBWCLK[9]	RCLK_IFBWCLK[10]	VDD	VSS	TFPO_TMFPO[10]	ROVRHD_EFBWDREQ[10]	RDATO_EFBWDAT[11]	TCLK_EFBWCLK[11]	RNEG_RLCV_ROHM_IFBWEN[11]	TPOH	VDD	TSLDCLK	VSS	ROHFP	RTOH	AM
RFPO_RMFPO_EFBWEN[9]	TFPO_TMFPO[9]	TDATI_IFBWDAT[9]	RCLK_IFBWCLK[9]	TDATI_IFBWDAT[10]	TCLK_EFBWCLK[10]	TNEG_TOHM_EFBWEN[10]	RFPO_RMFPO_EFBWEN[10]	RFPO_RMFPO_EFBWEN[11]	TPOS_TDATO_EFBWDAT[11]	TICLK_IFBWCLK[11]	TTOHEN	VDD	VDD	TSLD	VSS	ROHCLK	AN
ROVRHD_EFBWDREQ[9]	RSCLK_EFBWCLK[9]	TIOHM_TFPI_TMFPI_IFBWEN[9]	RPOS_RDATI_IFBWDAT[9]	TICLK_IFBWCLK[10]	TIOHM_TFPI_TMFPI_IFBWEN[10]	TPOS_TDATO_EFBWDAT[10]	RDATO_EFBWDAT[10]	ROVRHD_EFBWDREQ[11]	TNEG_TOHM_EFBWEN[11]	TDATI_IFBWDAT[11]	RCLK_IFBWCLK[11]	TOHCLK	TOHFP	TPOHRDY	NC	VSS	AP
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

8.5 Pin Diagram Top Left (Bottom View)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
TIOHM_TFPI_TMFPI_IFBWEN[2]	TNEG_TOHM_EFBWEN[2]	ROVRHD_EFBWDREQ[2]	RFPO_RMFPO_EFBWEN[3]	TPOS_TDATO_EFBWDAT[3]	TIOHM_TFPI_TMFPI_IFBWEN[3]	TICLK_IFBWCLK[3]	RPOS_RDATI_IFBWDAT[4]	TCLK_EFBWCLK[4]	RDATO_EFBWDAT[4]	FRMSTAT[5]	RSCLK_EFBWCLK[5]	TIOHM_TFPI_TMFPI_IFBWEN[5]	TDATI_IFBWDAT[5]	RNEG_RLCV_ROHM_IFBWEN[5]	RCLK_IFBWCLK[5]	VSS	A
TCLK_EFBWCLK[2]	TFPO_TMFPO[2]	FRMSTAT[2]	RDATO_EFBWDAT[3]	TCLK_EFBWCLK[3]	TDATI_IFBWDAT[3]	RNEG_RLCV_ROHM_IFBWEN[3]	RNEG_RLCV_ROHM_IFBWEN[4]	TPOS_TDATO_EFBWDAT[4]	RFPO_RMFPO_EFBWEN[4]	ROVRHD_EFBWDREQ[5]	TNEG_TOHM_EFBWEN[5]	VDD	VDD	RPOS_RDATI_IFBWDAT[5]	VSS	NC	B
TPOS_TDATO_EFBWDAT[2]	RSCLK_EFBWCLK[2]	FRMSTAT[3]	RSCLK_EFBWCLK[3]	VDD	VSS	RPOS_RDATI_IFBWDAT[3]	TICLK_IFBWCLK[4]	TNEG_TOHM_EFBWEN[4]	ROVRHD_EFBWDREQ[4]	RFPO_RMFPO_EFBWEN[5]	TPOS_TDATO_EFBWDAT[5]	VDD	TICLK_IFBWCLK[5]	VSS	NC	TCK	C
VSS	RDATO_EFBWDAT[2]	ROVRHD_EFBWDREQ[3]	TFPO_TMFPO[3]	VDD	VSS	RCLK_IFBWCLK[3]	TDATI_IFBWDAT[4]	TFPO_TMFPO[4]	FRMSTAT[4]	RDATO_EFBWDAT[5]	TCLK_EFBWCLK[5]	VDD	VSS	TRSTB	VDD	TDI	D
VSS	RFPO_RMFPO_EFBWEN[2]	VDDI	TNEG_TOHM_EFBWEN[3]	VDD	VSS	RCLK_IFBWCLK[4]	TIOHM_TFPI_TMFPI_IFBWEN[4]	RSCLK_EFBWCLK[4]	VDDI	TFPO_TMFPO[5]	VDD	VSS	VDD	VDD	VDD	TMS	E
												VDD	TDO	INTB	ALE	A[14]	F
												RSTB	A[13]	A[12]	A[11]	A[10]	G
												VDDI	A[9]	A[8]	A[7]	A[6]	H
												A[5]	A[4]	A[3]	A[2]	A[1]	J
												A[0]	D[15]	D[14]	D[13]	D[12]	K
												VDDI	D[11]	D[10]	D[9]	D[8]	L
												VSS	VSS	VSS	D[7]	D[6]	M
												VDD	VDD	VDD	D[5]	D[4]	N
												D[3]	D[2]	D[1]	D[0]	RDB	P
												VDDI	WRB	CSB	SPIMACHB	CJ0REF	R
												OCLK	OCLK_REF	OSTSEN	CJ0J1	OPL	T
												VSS	VSS	OD[0]	OD[1]	OD[2]	U

9 Pin Description

9.1 Modes, Clocking and Frame Pulses

Pin Name	Type	Pin No.	Function
SMODE[0] SMODE[1] SMODE[2]	Input	E34 F31 F32	System Side Interface Mode Select (SMODE[2:0]). SMODE[2:0] selects the bus protocol of the system side interface. ”000” UTOPIA Level 2 (16-bit bus). ”001” POS-PHY Level 2 (16-bit bus). ”010” UTOPIA Level 3 (32-bit bus). ”011” POS-PHY Level 3 (32-bit bus). ”100” UTOPIA Level 2 (16-bit no tristate). ”101” POS-PHY Level 2 (16-bit no tristate). ”110” Reserved. ”111” Reserved. For all Level 3 modes, bus output pins do not tristate (high impedance) when the interface is paused (as the bus connectivity is normally point-to-point). However, for Level 2 modes, the bus output pins may be programmed to tristate when the interface is deselected or not tristate similar to the Level 3 modes. SMODE[2:0] is an asynchronous input.
SPMACHB	Input	R2	TelecomBus Data Flow Configuration (SPMACHB). SPMACHB configures the TelecomBus to operate as an Add/Drop TelecomBus interface (SPECTRA Mode) or the primary line interface (MACH Mode). The SPMACHB bit in Register 0x1801 is exclusive-ORed (XOR) with the SPMACHB input pin to provide software control. When the XOR result of SPMACHB bit and pin is low, the TelecomBus is configured as the primary line interface, sourced/sinked from the path processors RHPP/THPP. When the XOR result of SPMACHB bit and pin is high, the TelecomBus is configured as a standard add/drop bus, sourced/sinked through the SVCA SONET/SDH aligners. SPMACHB is an asynchronous input.

Pin Name	Type	Pin No.	Function
FRAC[0] FRAC[1]	Input	C33 C34	Serial and Auxiliary Interface Configuration (FRAC). FRAC configures the Serial and Auxiliary interfaces for framer-only operation, external payload processing operation, or cell/packet delineation operation. An example of external payload processing is fractional DS3 processing. When FRAC[1:0] is "00", the Auxiliary interface pins can be used to source/sink serial DS3/E3/J2 data (frame-only operation). When FRAC[1:0] is "01", the Serial and Auxiliary interface pins allow external serial payload processing for all 12 channels. When FRAC[1:0] is "10", the Auxiliary interface pins allow external serial payload processing for 6 channels. When FRAC[1:0] is "11", the Auxiliary interface pins allow cell/packet delineation operation on all 12 channels. FRAC[1:0] is an asynchronous input.
OHCLK	Input	A27	Serial Overhead Insertion/Extraction Clock (OHCLK). OHCLK is a nominal 77.76MHz free-running clock that controls the line side overhead insertion and extraction interface.
OHCH[0] OHCH[1] OHCH[2] OHCH[3]	Output	B27 C27 D27 A28	Serial Overhead Insertion/Extraction Channel (OHCH[3:0]). OHCH[3:0] shows which channel's overhead control information (TOHVAL, TOHFA, TPHVAL, TPHFA, ROHVAL, ROHFA, ROH, RPHVAL, RPHFA and RPH) is being updated. Channel numbers 0 to 11 are valid while channel numbers 12 to 15 are reserved and must be ignored. OHCH[3:0] is updated on the rising edge of OHCLK.
DS3_ REFCLK	Input	AM34	DS3 Serial Jitter Attenuation Reference Clock (DS3_REFCLK). DS3_REFCLK is a nominal 44.736MHz free-running clock with 50% duty cycle. Each channel has independent control over which Serial Jitter Attenuation Reference Clock to be used (DS3_REFCLK or E3_REFCLK).
E3_REFCLK	Input	AL32	E3 Serial Jitter Attenuation Reference Clock (E3 REFCLK). E3_REFCLK is a nominal 34.368MHz free-running clock with 50% duty cycle. Each channel has independent control over which Serial Jitter Attenuation Reference Clock to be used (DS3_REFCLK or E3_REFCLK).

Pin Name	Type	Pin No.	Function
REF8KI	Input	D32	Reference 8 kHz Input (REF8KI). The PLCP frame rate is locked to an external 8 kHz reference applied on this input. An internal phase-frequency detector compares the transmit PLCP frame rate with the externally applied 8 kHz reference and adjusts the PLCP frame rate. The REF8KI input must transition high once every 125 μs for correct operation. The REF8KI input is treated as an asynchronous signal and must be "glitch-free". If the LOOPT register bit is high, the PLCP frame rate is locked to the RPHFA signal instead of the REF8KI input.
REF8KO	Output	D34	Reference 8kHz Output (REF8KO). REF8KO is an 8kHz reference derived from one of the selected receive clocks RCLK[11:0]. A free-running divide-down counter is used to generate REF8KO so it will not glitch on reframe actions. REF8KO will pulse high for approximately one RCLK cycle every 125 μs. REF8KO should be treated as a glitch-free asynchronous signal.

9.2 Transmit Serial Line Side Interface

Pin Name	Type	Pin No.	Function
TCLK[0] TCLK[1] TCLK[2] TCLK[3] TCLK[4] TCLK[5] TCLK[6] TCLK[7] TCLK[8] TCLK[9] TCLK[10] TCLK[11]	I/O	D25 D20 B17 B13 A9 D6 AP28 AN24 AN20 AK16 AN12 AM8	Transmit Output Clock (TCLK[11:0]). TCLK[11:0] provides the transmit direction timing for the serial line interfaces when FRAC[1:0] is not in external payload processing for 12 channels mode. TCLK[11:0] is always driven as an output in these modes. When a channel is configured for framer mode (slave), the specified TCLK[11:0] is a buffered version of associated TICLK[11:0]. When a channel is configured for source clocking (master), the specified TCLK[11:0] is derived from the REFCLK input using the internal digital PLL (JAT). TCLK/EFBWCLK[11:0] pin function selections are controlled by FRAC[1:0] mode pins.
TPOS[0] TPOS[1] TPOS[2] TPOS[3] TPOS[4] TPOS[5] TPOS[6] TPOS[7] TPOS[8] TPOS[9] TPOS[10] TPOS[11]	Output	C25 A21 C17 A13 B9 C6 AL27 AM24 AP20 AL16 AP11 AN8	Transmit Digital Positive Pulse (TPOS[11:0]). TPOS[11:0] contains the positive pulses transmitted on the B3ZS-encoded DS3, HDB3-encoded E3, or B8ZS-encoded J2 transmission system when the dual-rail output format is selected and FRAC[1:0] is not in external payload processing for 12 channels mode. The TPOS/TDATO/EFBWDAT[11:0] pin function selections are controlled by the FRAC[1:0] mode pins and TFRM[1:0] and the TUNI bits in the S/UNI-12xJET Channel Transmit Configuration Registers. Output signal polarity controls are provided by the TPOSINV bit in the S/UNI-12xJET Channel Transmit Configuration Registers. TPOS/TDATO/EFBWDAT[11:0] are updated on the rising edge of TCLK/EFBWCLK[11:0].
TDATO[0] TDATO[1] TDATO[2] TDATO[3] TDATO[4] TDATO[5] TDATO[6] TDATO[7] TDATO[8] TDATO[9] TDATO[10] TDATO[11]	Output	C25 A21 C17 A13 B9 C6 AL27 AM24 AP20 AL16 AP11 AN8	Transmit Data (TDATO[11:0]). TDATO[11:0] contains the transmit data stream when the single-rail (unipolar) output format is enabled or when a non-DS3/E3/J2 based transmission system is selected and FRAC[1:0] is not in external payload processing for 12 channels mode. The TPOS/TDATO/EFBWDAT[11:0] pin function selections are controlled by the FRAC[1:0] mode pins and TFRM[1:0] and the TUNI bits in the S/UNI-12xJET Channel Transmit Configuration Registers. Output signal polarity controls are provided by the TPOSINV bit in the S/UNI-12xJET Channel Transmit Configuration Registers. TPOS/TDATO/EFBWDAT[11:0] are updated on the rising edge of TCLK/EFBWCLK[11:0].

Pin Name	Type	Pin No.	Function
TNEG[0] TNEG[1] TNEG[2] TNEG[3] TNEG[4] TNEG[5] TNEG[6] TNEG[7] TNEG[8] TNEG[9] TNEG[10] TNEG[11]	Output	B25 B21 A16 E14 C9 B6 AM27 AL24 AK19 AM16 AN11 AP8	Transmit Digital Negative Pulse (TNEG[11:0]). TNEG[11:0] contains the negative pulses transmitted on the B3ZS-encoded DS3, HDB3-encoded E3, or B8ZS-encoded J2 transmission system when the dual-rail NRZ output format is selected and FRAC[1:0] is not in external payload processing for 12 channels mode. The TNEG/TOHM/EFBWEN[11:0] pin function selections are controlled by the FRAC[1:0] mode pins and TFRM[1:0] and the TUNI bits in the S/UNI-12xJET Channel Transmit Configuration Registers. Output signal polarity controls are provided by the TNEGINV bit in the S/UNI-12xJET Channel Transmit Configuration Registers. TNEG/TOHM/EFBWEN[11:0] are updated on the rising edge of TCLK/EFBWCLK[11:0].
TOHM[0] TOHM[1] TOHM[2] TOHM[3] TOHM[4] TOHM[5] TOHM[6] TOHM[7] TOHM[8] TOHM[9] TOHM[10] TOHM[11]	Output	B25 B21 A16 E14 C9 B6 AM27 AL24 AK19 AM16 AN11 AP8	Transmit Overhead Mask (TOHM[11:0]). TOHM[11:0] indicates the position of overhead bits (non-payload bits) in the transmission system stream aligned with TDATO[11:0]. TOHM[11:0] indicates the location of the M-frame boundary for DS3, the position of the frame boundary for E3, and the position of the multi-frame boundary for J2 when the single-rail (unipolar) NRZ input format is enabled and FRAC[1:0] is not in external payload processing for 12 channels mode. When a PLCP formatted signal is transmitted, TOHM[11:0] is set high once per transmission frame, and indicates the DS1 or E1 frame alignment. When a non-PLCP, non-DS3, non-E3, non-J2 based signal is transmitted, TOHM[11:0] is a delayed version of the TIOHM[11:0] input, and indicates the position of each overhead bit in the transmission frame. The TNEG/TOHM/EFBWEN[11:0] pin function selections are controlled by the FRAC[1:0] mode pins and TFRM[1:0] and the TUNI bits in the S/UNI-12xJET Channel Transmit Configuration Registers. Output signal polarity controls are provided by the TNEGINV bit in the S/UNI-12xJET Channel Transmit Configuration Registers. TNEG/TOHM/EFBWEN[11:0] are updated on the rising edge of TCLK/EFBWCLK[11:0].

9.3 Receive Serial Line Side Interface

Pin Name	Type	Pin No.	Function
RCLK[0] RCLK[1] RCLK[2] RCLK[3] RCLK[4] RCLK[5] RCLK[6] RCLK[7] RCLK[8] RCLK[9] RCLK[10] RCLK[11]	Input	E26 C19 B19 D11 E11 A2 AN29 AK21 AL21 AN14 AM14 AP6	Receive Input Clock (RCLK[11:0]). RCLK[11:0] provide the receive direction timing for the serial line interfaces when FRAC[1:0] is not in external payload processing for 12 channels mode. RCLK[11:0] are the externally recovered transmission system baud rate clock. RCLK/IFBWCLK[11:0] pin function selections are controlled by FRAC[1:0] mode pins. RCLK is a free-running clock with nominal 50% duty cycle. The frequency of RCLK depends on the mode of operation of the particular slice. For DS3 operation RCLK frequency is 44.736MHz, for E3 operation RCLK frequency is 34.368MHz, for J2 operation RCLK frequency is 6.312 MHz, for E1 operation RCLK frequency is 2.048 MHz, and for T1 operation RCLK frequency is a nominal 1.544 MHz.
RPOS[0] RPOS[1] RPOS[2] RPOS[3] RPOS[4] RPOS[5] RPOS[6] RPOS[7] RPOS[8] RPOS[9] RPOS[10] RPOS[11]	Input	D26 D19 A19 C11 A10 B3 AK28 AP22 AM21 AP14 AL14 AL7	Receive Digital Positive Pulse (RPOS[11:0]). RPOS[11:0] contains the positive pulses received on the B3ZS-encoded DS3, the HDB3-encoded E3, or the B8ZS-encoded J2 transmission system when the dual-rail NRZ input format is selected and FRAC[1:0] is not in external payload processing for 12 channels mode. The RPOS/RDATI/IFBWDAT[11:0] pin function selections are controlled by FRAC[1:0] mode pins, the RFRM[1:0] bits in the S/UNI-12xJET Channel Receive Configuration Registers and by the UNI bits in the DS3 FRMR, the E3 FRMR, or the J2 FRMR Configuration Registers. Signal polarity controls are provided by the RPOSINV bit in the S/UNI-12xJET Channel Receive Configuration Registers. RPOS/RDATI/IFBWDAT[11:0] are sampled on the rising edge of RCLK/IFBWCLK[11:0].
RDATI[0] RDATI[1] RDATI[2] RDATI[3] RDATI[4] RDATI[5] RDATI[6] RDATI[7] RDATI[8] RDATI[9] RDATI[10] RDATI[11]	Input	D26 D19 A19 C11 A10 B3 AK28 AP22 AM21 AP14 AL14 AL7	Receive Data (RDATI[11:0]). RDATI[11:0] contains the data stream when the single-rail (unipolar) NRZ input format is enabled or when a non-DS3/E3/J2 based transmission system is being processed (for example RDATI may contain a DS1 or E1 stream). The mode pins FRAC[1:0] must not be in external payload processing for 12 channels mode. The RPOS/RDATI/IFBWDAT[11:0] pin function selections are controlled by the FRAC[1:0] mode pins, RFRM[1:0] bits in the S/UNI-12xJET Channel Receive Configuration Registers and by the UNI bits in the DS3 FRMR, the E3 FRMR, or the J2 FRMR Configuration Registers. Signal polarity controls are provided by the RPOSINV bit in the S/UNI-12xJET Channel Receive Configuration Registers. RPOS/RDATI/IFBWDAT[11:0] are sampled on the rising edge of RCLK/IFBWCLK[11:0].

Pin Name	Type	Pin No.	Function
RNEG[0] RNEG[1] RNEG[2] RNEG[3] RNEG[4] RNEG[5] RNEG[6] RNEG[7] RNEG[8] RNEG[9] RNEG[10] RNEG[11]	Input	C26 E19 C18 B11 B10 A3 AP29 AN22 AN21 AL15 AK14 AM7	Receive Digital Negative Pulse (RNEG[11:0]). RNEG[11:0] contains the negative pulses received on the B3ZS encoded DS3, the HDB3-encoded E3, or the B8ZS-encoded J2 transmission system when the dual-rail NRZ input format is selected and FRAC[1:0] is not in external payload processing for 12 channels mode. The RNEG/RLCV/ROHM/IFBWEN[11:0] pin function selections are controlled by the FRAC[1:0] mode pins, the RFRM[1:0] bits in the S/UNI-12xJET Channel Receive Configuration Registers, the UNI bits in the DS3 FRMR, E3 FRMR, or J2 FRMR Configuration Registers, and the PLCPEN and EXT bits in the SPLR Configuration register. Signal polarity controls are provided by the RNEGINV bit in the S/UNI-12xJET Channel Receive Configuration Registers. RNEG/RLCV/ROHM/IFBWEN[11:0] are sampled on the rising edge of RCLK/IFBWCLK[11:0].
RLCV[0] RLCV[1] RLCV[2] RLCV[3] RLCV[4] RLCV[5] RLCV[6] RLCV[7] RLCV[8] RLCV[9] RLCV[10] RLCV[11]	Input	C26 E19 C18 B11 B10 A3 AP29 AN22 AN21 AL15 AK14 AM7	Receive Line Code Violation (RLCV[11:0]). RLCV[11:0] contains line code violation indications when the single-rail (unipolar) NRZ input format is enabled for DS3, E3, or J2 applications. Each line code violation is represented by an RCLK[11:0] period-wide pulse. The mode pins FRAC[1:0] must not be in external payload processing for 12 channels mode. The RNEG/RLCV/ROHM/IFBWEN[11:0] pin function selections are controlled by the FRAC[1:0] mode pins, RFRM[1:0] bits in the S/UNI-12xJET Channel Receive Configuration Registers, the UNI bits in the DS3 FRMR, E3 FRMR, or J2 FRMR Configuration Registers, and the PLCPEN and EXT bits in the SPLR Configuration register. Signal polarity controls are provided by the RNEGINV bit in the S/UNI-12xJET Channel Receive Configuration Registers. RNEG/RLCV/ROHM/IFBWEN[11:0] are sampled on the rising edge of RCLK/IFBWCLK[11:0].

Pin Name	Type	Pin No.	Function
ROHM[0] ROHM[1] ROHM[2] ROHM[3] ROHM[4] ROHM[5] ROHM[6] ROHM[7] ROHM[8] ROHM[9] ROHM[10] ROHM[11]	Input	C26 E19 C18 B11 B10 A3 AP29 AN22 AN21 AL15 AK14 AM7	Receive Overhead Mask (ROHM[11:0]). When a DS1 or E1 PLCP or ATM direct-mapped signal is received, ROHM[11:0] is pulsed once per transmission frame, and indicates the DS1 or E1 frame alignment relative to the RDATI[11:0] data stream. When an alternate frame-based signal is received, ROHM[11:0] indicates the position of each overhead bit in the transmission frame. The mode pins FRAC[1:0] must not be in external payload processing for 12 channels mode. The RNEG/RLCV/ROHM/IFBWEN[11:0] pin function selections are controlled by the RFRM[1:0] bits in the S/UNI-12xJET Channel Receive Configuration Registers, the UNI bits in the DS3 FRMR, E3 FRMR, or J2 FRMR Configuration Registers, and the PLCPEN and EXT bits in the SPLR Configuration register. Signal polarity controls are provided by the RNEGINV bit in the S/UNI-12xJET Channel Receive Configuration Registers. RNEG/RLCV/ROHM/IFBWEN[11:0] are sampled on the rising edge of RCLK/IFBWCLK[11:0].

9.4 Transmit Serial Overhead Insertion

Pin Name	Type	Pin No.	Function
TOHVAL	Output	B28	Transmit Overhead Insertion Valid (TOHVAL). TOHVAL shows whether or not data is valid on the TOHFA and whether TOH and TOHINS can be sampled for the DS3/E3 channel displayed on OHCH[3:0]. J2 channel overhead insertion is not supported. TOHVAL is updated on the rising edge of OHCLK.
TOHFA	Output	C28	Transmit DS3/E3 Overhead Frame Alignment (TOHFA). TOHFA is used to align the individual overhead bits in the transmit overhead data stream, TOH, to the DS3 M-frame or the E3 frame of the channel specified by OHCH[3:0]. For DS3, TOHFA is high during the X1 overhead bit position in the TOH stream. For G.832 E3, TOHFA is high during the first bit of the FA1 byte. For G.751 E3, TOHFA is high during the RAI overhead bit position in the TOH stream. TOHFA is updated on the rising edge of OHCLK.
TOHINS	Input	B32	Transmit DS3/E3 Overhead Insertion (TOHINS). TOHINS controls the insertion of the DS3 or E3, overhead bits from the TOH input for the channel specified by OHCH[3:0]. In order for the bit to be inserted, TOHVAL must also be high. When TOHINS is high, the overhead bit in the TOH stream is inserted in the transmitted DS3 or E3 frame. When TOHINS is low, the DS3 or E3 overhead bit is generated and inserted internally. If TOHINS is high, the TOH input has precedence over the internal data link transmitter, or any internal register bit setting. TOHINS is sampled on the rising edge of OHCLK.

Pin Name	Type	Pin No.	Function
TOH	Input	A33	Transmit DS3/E3 Overhead Data (TOH). When configured for DS3 operation, TOH contains the overhead bits (C, F, X, P, and M) that may be inserted in the transmit DS3 stream specified by OHCH[3:0]. When configured for G.832 E3 operation, TOH contains the overhead bytes (FA1, FA2, EM mask, TR, MA, NR, and GC) that may be inserted in the transmit G.832 E3 stream specified by OHCH[3:0]. When configured for G.751 E3 operation, TOH contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) that may be inserted in the transmit G.751 E3 stream specified by OHCH[3:0]. If TOHINS is high, the TOH input has precedence over the internal data link transmitter, or any other internal register bit setting. TOH is sampled on the rising edge of OHCLK.
TPHVAL	Output	D28	PLCP Overhead Insertion Valid (TPHVAL). TPHVAL shows whether or not data is valid on the TPHFA and whether TPH and TPHINS can be sampled for the channel displayed on OHCH[3:0]. TPHVAL is updated on the rising edge of OHCLK.
TPHFA	Output	A29	Transmit PLCP Overhead Frame Alignment (TPHFA). The TPHFA output locates the individual PLCP path overhead bits in the transmit overhead data stream, TPH for the channel specified by OHCH[3:0]. TPHFA is high while bit 1 (the most significant bit) of the path user channel octet (F1) is present in the TPH stream. TPHFA is updated on the rising edge of OHCLK.
TPHINS	Input	A32	Transmit PLCP Overhead Insertion (TPHINS). TPHINS controls the insertion of PLCP overhead octets on the TPH input for the channel specified by OHCH[3:0]. When TPHINS is high, the overhead bit in the TPH stream is inserted in the transmit PLCP frame. When TPHINS is low, the PLCP path overhead bit is generated and inserted internally. Note, when operating in G.751 E3 PLCP mode, bits 8, 7 and 6 of the C1 octet should not be manipulated. TPHINS is sampled on the rising edge of OHCLK.

Pin Name	Type	Pin No.	Function
TPH	Input	C31	Transmit PLCP Overhead Data (TPH). TPH contains the PLCP path overhead octets (Zn, F1, B1, G1, M1, M2, and C1) for the channel specified by OHCH[3:0] which may be inserted in the transmit PLCP frame. The octet data on TPH is shifted in order from the most significant bit (bit 1) to the least significant bit (bit 8). TPH is sampled on the rising edge of OHCLK.

9.5 Receive Serial Overhead Extraction

Pin Name	Type	Pin No.	Function
ROHVAL	Output	E28	Receive Overhead Extraction Valid (ROHVAL). ROHVAL shows if data is valid on ROHFA and ROH for the DS3/E3/J2 channel specified by OHCH[3:0]. ROHVAL is updated on the rising edge of OHCLK.
ROHFA	Output	B29	Receive DS3/E3/J2 Overhead Frame Alignment (ROHFA). ROHFA locates the individual overhead bits in the received overhead data stream, ROH, for the channel specified by OHCH[3:0]. ROHFA is high during the X1 overhead bit position in the ROH stream when processing a DS3 stream. ROHFA is high during the first bit of the FA1 byte when processing a G.832 E3 stream. ROHFA is high during the RAI overhead bit position when processing a G.751 E3 stream. ROHFA is high during the first bit in Timeslot 97 in the first frame of the 4-frame multi-frame when processing a J2 stream. ROHFA is updated on the rising edge of OHCLK.
ROH	Output	C29	Receive DS3/E3/J2 Overhead Data (ROH). ROH contains the overhead bits (C, F, X, P, and M) extracted from the received DS3 stream specified by OHCH[3:0]. ROH contains the overhead bytes (FA1, FA2, EM, TR, MA, NR, and GC) extracted from the received G.832 E3 streams specified by OHCH[3:0]. ROH contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) extracted from the received G.751 E3 stream specified by OHCH[3:0]. ROH contains the overhead bits (Framing, X_{1-3}, A, M, E_{1-5}) extracted from the received J2 stream specified by OHCH[3:0]. ROH is updated on the rising edge of OHCLK.
RPHVAL	Output	D29	Receive PLCP Extraction Valid (RPHVAL). RPHVAL shows if data is valid on RPHFA and RPH for the DS3/E3/J2 channel specified by OHCH[3:0]. RPHVAL is updated on the rising edge of OHCLK.

Pin Name	Type	Pin No.	Function
RPHFA	Output	A30	Receive PLCP Overhead Frame Alignment (RPHFA). RPHFA locates the individual PLCP path overhead bits in the receive overhead data stream, RPH, for the channel specified by OHCH[3:0]. RPHFA is high while bit 1 (the most significant bit) of the path user channel octet (F1) is present in the RPH stream. RPHFA is updated on the rising edge of OHCLK.
RPH	Output	A31	Receive PLCP Overhead Data (RPH). RPH contains the PLCP path overhead octets (Zn, F1, B1, G1, M1, M2, and C1) extracted from the received PLCP frame of the channel specified by OHCH[3:0] when the PLCP layer is in-frame. When the PLCP layer is in the loss of frame state, RPH is forced to all ones for the channel. The octet data on RPH is shifted out in order from the most significant bit (bit 1) to the least significant bit (bit 8). RPH is updated on the rising edge of OHCLK

9.6 Transmit TelecomBus Interface

Pin Name	Type	Pin No.	Function
OCLK	Input	T5	Transmit Outgoing System Clock (OCLK). OCLK is the master TelecomBus transmit clock for the S/UNI-12xJET device. OCLK is nominally a 77.76 MHz clock, with a 50% duty cycle.
OD[0] OD[1] OD[2] OD[3] OD[4] OD[5] OD[6] OD[7]	Tristate Output	U3 U2 U1 V1 V2 V3 W2 W3	Outgoing Data (OD[7:0]). OD[7:0] carries the SONET/SDH OC-12 frame data in byte serial format. OD[7] is the most significant bit, corresponding to bit 1 of each SONET/SDH octet, the bit transmitted first. OD[0] is the least significant bit, corresponding to bit 8 of each SONET/SDH octet, the bit transmitted last. The TTBZ in conjunction with the STSEN[12:1] bits in register 0x180D tristates OD[7:0], ODP and OPL outputs OD[7:0] is updated on the rising edge of OCLK.
ODP	Tristate Output	W4	Outgoing Data Parity (ODP). ODP reports the parity of the corresponding outgoing data bus (OD[7:0]). ODP reports even parity by default, however it may be configured for odd parity and to report parity over incoming data bus and the control signals (OPL and OJ0J1) via microprocessor control. The TTBZ in conjunction with the STSEN[12:1] bits in register 0x180D tristates OD[7:0], ODP and OPL outputs ODP is updated on the rising edge of OCLK.
OPL	Tristate Output	T1	Outgoing Payload Active (OPL). OPL distinguishes between transport overhead / section overhead bytes from synchronous payload / high order virtual container bytes in the corresponding outgoing data bus (OD[7:0]). The TTBZ in conjunction with the STSEN[12:1] bits in register 0x180D tristates OD[7:0], ODP and OPL outputs OPL is set high to mark each payload / HO-VC byte on OD[7:0] and set low to mark each transport overhead / section overhead byte on OD[7:0]. OPL is updated on the rising edge of OCLK.

Pin Name	Type	Pin No.	Function
OJ0J1	Output	T2	Outgoing Composite Transport and Payload Frame Pulse (OJ0J1). OJ0J1 identifies the STS/STM frame and the synchronous payload envelope / high order virtual container frame boundaries on the corresponding outgoing data bus (OD[7:0]). OJ0J1 is set high when OPL is set low to mark the J0 byte of the STS/STM frame on the OD[7:0] bus. OJ0J1 is set high when OPL is set high to mark the each J1 byte of the SPE / HO-VC frame on the OD[7:0] bus. The J0 position on OJ0J1 will be aligned to OJ0REF as configured by the OJ0REFDLY register. OJ0J1 is updated on the rising edge of OCLK
OALARM	Output	W5	Outgoing Alarm (OALARM). OALARM identifies STS/STM or tributaries on the corresponding outgoing data bus (OD[7:0]) that are in alarm state. OALARM is set high when the stream on OD[7:0] is in alarm (for instance, AIS) and is set low when the stream is out of alarm state. OALARM is updated on the rising edge of OCLK.
OJ0REF	Input	R1	Outgoing Transport J0 Frame Pulse Reference (OJ0REF). OJ0REF is used to reference the S/UNI-12xJET to a J0 byte location as configured in the OJ0REFDLY registers. OJ0REF is expected to be high for 1 clock cycle every 9720 OCLK cycles and aligns the J0 position on OJ0J1. When not used, OJ0REF must be tied low. OJ0REF is sampled on the rising edge of OCLK.
OSTSEN	Output	T3	Outgoing STS Enable (OSTSEN). OSTSEN is asserted high whenever the S/UNI 12xJET is sourcing a valid STS timeslot on the Transmit TelecomBus. This pin is intended to control an external multiplexer when multiple devices are driving the Transmit Telecom Bus. OSTEN is updated on the rising edge of OCLK.
OCLK_REF	Output	T4	Outgoing System Clock Reference (OCLK_REF). OCLK_REF is a reference clock for the parallel TelecomBus DROP interface when SPMACHB is 1. OCLK_REF is an internally buffered version of PTCLK, a 77.76 MHz, nominally 50% duty cycle, non-gapped clock.

9.7 Receive TelecomBus Interface

Pin Name	Type	Pin No.	Function
ICLK	Input	Y1	Receive Incoming System Clock (ICLK). ICLK is the master TelecomBus receive clock for the S/UNI-12xJET device. OCLK is nominally a 77.76 MHz clock, with a 50% duty cycle.
ID[0] ID[1] ID[2] ID[3] ID[4] ID[5] ID[6] ID[7]	Input	Y4 AA1 AA2 AA3 AA4 AA5 AB1 AB2	Incoming Data (ID[7:0]). ID[7:0] carries the SONET/SDH OC-12 frame data in byte serial format. ID[7] is the most significant bit, corresponding to bit 1 of each SONET/SDH octet, the bit received first. ID[0] is the least significant bit, corresponding to bit 8 of each SONET/SDH octet, the bit received last. ID][7:0] is sampled on the rising edge of ICLK.
IDP	Input	AC1	Incoming Data Parity (IDP). IDP reports the parity of the corresponding incoming data bus (ID[7:0]). IDP reports even parity by default, however it may be configured for odd parity and to report parity over incoming data bus and the control signals (IPL and IJ0J1) via microprocessor control. IDP is sampled on the rising edge of ICLK.
IPL	Input	Y3	Incoming Payload Active (IPL). IPL distinguishes between transport overhead / section overhead bytes from synchronous payload / high order virtual container bytes in the corresponding incoming data bus (ID[7:0]). IPL is set high to mark each payload / HO-VC byte on ID[7:0] and set low to mark each transport overhead / section overhead byte on ID[7:0]. IPL is sampled on the rising edge of ICLK.
IJ0J1	Input	Y2	Incoming Composite Transport and Payload Frame Pulse (IJ0J1). IJ0J1 identifies the STS/STM frame and the synchronous payload envelope / high order virtual container frame boundaries on the corresponding incoming data bus (ID[7:0]). IJ0J1 is set high when IPL is set low to mark the J0 byte of the STS/STM frame on the ID[7:0] bus. IJ0J1 is set high when IPL is set high to mark the each J1 byte of the SPE / HO-VC frame on the ID[7:0] bus. IJ0J1 is sampled on the rising edge of ICLK.

Pin Name	Type	Pin No.	Function
IALARM	Input	AC2	Incoming Alarm Status (IALARM). IALARM identifies STS/STM streams on the corresponding incoming data bus (ID[7:0]) that are in alarm state. Definition of the alarm condition depends on the amount of SONET/SDH processing performed by the S/UNI-12xJET. IALARM is set high when the stream on ID[7:0] is in alarm state (for instance, PAIS) and is set low when the stream is out of alarm state. IALARM is sampled on the rising edge of ICLK.
ICLK_REF	Output	W1	Incoming System Clock Reference (ICLK_REF). ICLK_REF is a reference clock for the parallel TelecomBus ADD interface when SPMACHB is 1. ICLK_REF is an internally buffered version of PICLK, a 77.76 MHz, nominally 50% duty cycle, non-gapped clock.

9.8 Transmit SONET/SDH Interface

Pin Name	Type	Pin No.	Function
PTCLK	Input	AD1	Parallel Transmit Clock (PTCLK). PTCLK provides timing for S/UNI-12xJET transmit function operation when using an external SERDES device. PTCLK must be a 77.76 MHz nominally 50% duty cycle clock free-running (non gapped) clock.
POUT[0] POUT[1] POUT[2] POUT[3] POUT[4] POUT[5] POUT[6] POUT[7]	Output	AE5 AE4 AE3 AE2 AE1 AD4 AD3 AD2	Parallel Outgoing Stream (POUT[7:0]). POUT[7:0] carries the scrambled STS-12c/STM-4-4c stream in byte-serial format. POUT[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). POUT[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). POUT[7:0] is updated on the rising edge of PTCLK.
TSFPI	Input	AF2	Outgoing Framing Position Input (TSFPI). The active-high TSFPI signal is used as a reference for the SONET/SDH frame position on the POUT[7:0] bus. TSFPI must be asserted for 1 clock cycle every 9720 PTCLK cycles. When not used, TSFPI must be tied low. TSFPI is sampled on the rising edge of PTCLK.
TSFPO	Output	AF1	Outgoing Framing Position Output (TSFPO). TSFPO signal indicates the SONET/SDH frame alignment on the POUT[7:0] bus. TSFPO is asserted for one PTCLK clock cycle to indicate the SONET/SDH frame position on the POUT[7:0] bus. The byte on the POUT[7:0] bus indicated by TSFPO is the fist payload byte after J0/Z0 byte of the SONET/SDH frame. TSFPO is updated on the rising edge of PTCLK.

9.9 Receive SONET/SDH Interface

Pin Name	Type	Pin No.	Function
PICLK	Input	AF3	Parallel Input Clock (PICLK). PICLK provides timing for S/UNI-12xJET receive function operation when using an external SERDES device. PICLK must be a 77.76 MHz nominally 50% duty cycle clock free-running (non gapped) clock.
PIN[0] PIN[1] PIN[2] PIN[3] PIN[4] PIN[5] PIN[6] PIN[7]	Input	AH2 AH1 AG4 AG3 AG2 AG1 AF5 AF4	Parallel Incoming Stream (PIN[7:0]). The PIN[7:0] bus carries the byte-serial STS-12c/STM-4-4c stream from an external SERDES device. PIN[7] is the most significant bit (corresponding to bit 1 of each serial byte, the first bit received). PIN[0] is the least significant bit (corresponding to bit 8 of each serial byte, the last bit received). PIN[7:0] is sampled on the rising edge of PICLK.
FPIN	Input	AH3	Incoming Framing Position Input (FPIN). The active-high FPIN signal indicates the SONET/SDH frame position on the PIN[7:0] bus. The byte on the PIN[7:0] bus indicated by FPIN is the third A2 of the SONET/SDH framing pattern. The location of FPIN is also programmable using FPINDLY[13:0] in the S/UNI-12xJET Receive SERDES Synchronization Delay Register (0x1FF4) OOF forces an external SERDES device to look for framing pattern in order to find a new byte and frame alignment. The frame alignment is indicated by the FPIN input. FPIN is sampled on the rising edge of PICLK.
RSFPO	Output	AH4	Incoming Framing Position Output (RSFPO). The active-high RSFPO signal may be used as a reference for SONET/SDH frame position for the incoming PIN[7:0] bus. RSFPO is asserted for one clock cycle per SONET/SDH frame. RSFPO is updated on the rising edge of PICLK.

Pin Name	Type	Pin No.	Function
OOF	Output	AJ1	Out of Frame Indication (OOF). The active high OOF signal indicates when the out of frame condition is declared by an external SERDES device. OOF is set high while the S/UNI-12xJET is searching for frame. OOF is set low while the S/UNI-12xJET is in frame. OOF forces an external SERDES device to look for framing pattern is order to find a new byte and frame alignment. The framer alignment is indicated by the FPIN input. OOF is updated on the rising edge of PICLK.

9.10 Transmit SONET/SDH Overhead Insertion

Pin Name	Type	Pin No.	Function
TOHCLK	Output	AP5	Transmit Overhead Clock (TOHCLK). TOHCLK provides timing for the transmit section, line and path overhead insertion. TOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. TOHCLK has a 33% high duty cycle. TOHFP and TPOHRDY are updated on the falling edge of TOHCLK. TTOH, TTOHEN, TPOH and TPOHEN are sampled on the rising edge of TOHCLK.
TOHFP	Output	AP4	Transmit Overhead Frame Pulse (TOHFP). TOHFP provides timing for the transmit section, line and path overhead insertion. TOHFP is used to indicate the most significant bit (MSB) on TSLD, TTOH and TPOH. TOHFP is set high when the MSB of the: D1 or D4 byte should be present on TSLD. First A1 byte should be present on TTOH. First J1 byte should be present on TPOH. TOHFP can be sampled on the rising edge of TSLDCLK and TOHCLK. TOHFP is updated on the falling edge of TOHCLK.
TTOH	Input	AK7	Transmit Transport Overhead (TTOH). The transmit transport overhead (TTOH) signal contains the transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) to be transmitted and the error masks to be applied on B1, B2, H1 and H2. TTOH is sampled on the rising edge of TOHCLK..

Pin Name	Type	Pin No.	Function
TTOHEN	Input	AN6	Transmit Transport Overhead Insert Enable (TTOHEN). TTOHEN controls the insertion of the transmit transport overhead data which is inserted in the outgoing stream. When TTOHEN is high during the most significant bit of a TOH byte on TTOH, the sampled TOH byte is inserted into the corresponding transport overhead byte positions (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2 bytes). When TTOHEN is low during the most significant bit of a TOH byte on TTOH, that sampled byte is ignored and the default values are inserted into these transport overhead bytes. When TTOHEN is high during the most significant bit of the H1, H2, B1 or B2 TOH byte positions on TTOH, the sampled TOH byte is logically XORed with the associated incoming byte to force bit errors on the outgoing byte. A logic low bit in the TTOH byte allows the incoming bit to go through while a bit set to logic high will toggle the incoming bit. A low level on TTOHEN during the MSB of the TOH byte disables the error forcing for the entire byte. TTOHEN is sampled on the rising edge of TOHCLK.
TPOH	Input	AM6	Transmit Path Overhead (TPOH). TPOH signal contains the path overhead bytes (J1, C2, G1, F2, Z3, Z4, and Z5) to be transmitted in the SONET/SDH path overhead and the error masks to be applied on B3 and H4 on the outgoing TelecomBus stream. A path overhead byte is accepted for transmission when TPOHEN set high by an external source, indicating a valid byte, and when TPOHRDY is set high. TPOH will be ignored when TPOHEN is set low. When TPOHRDY is set low, the byte must be re-presented at the next opportunity. Path Overhead must presented at every opportunity for correct operation. TPOH is sampled on the rising edge of TOHCLK.

Pin Name	Type	Pin No.	Function
TPOHEN	Input	AL6	Transmit Path Overhead Insert Enable (TPOHEN). TPOHEN controls the insertion of the transmit path overhead data which is inserted in the outgoing stream. TPOHEN shall be set high during the most significant bit of a POH byte to indicate valid data on the TPOH input. This byte will be accepted for transmission if TPOHRDY is also set high. If TPOHRDY is set low, the byte is rejected and must be re-presented at the next opportunity. Accepted bytes sampled on TPOH are inserted into the corresponding path overhead byte positions (for the J1, C2, G1, F2, Z3, Z4, and Z5 bytes). The byte on TPOH is ignored when TPOHEN is set low during the most significant bit position. When the byte at the B3 or H4 byte position on TPOH is accepted, it is used as an error mask to modify the corresponding transmit B3 or H4 path overhead byte, respectively. The accepted error mask is XORed with the corresponding B3 or H4 byte before it is transmitted. Path Overhead must presented at every opportunity for correct operation. TPOHEN is sampled on the rising edge of the TOHCLK.
TPOHRDY	Output	AP3	Transmit Path Overhead Insert Ready (TPOHRDY). TPOHRDY signal indicates if the TPOH is ready to accept the applied byte. TPOHRDY is set high during the most significant bit of a POH byte to indicate readiness to accept the byte on the TPOH input. This byte will be accepted if TPOHEN is also set high. If TPOHEN is set low, the byte is invalid and is ignored. TPOHRDY is set low to indicate that the S/UNI-12xJET is unable to accept the byte, and expects the byte to be re-presented at the next opportunity. Path Overhead must presented at every opportunity for correct operation. TPOHRDY is updated on the falling edge of TOHCLK.

Pin Name	Type	Pin No.	Function
TSLDCLK	Output	AM4	Transmit section or Line Data Communication Channel Clock (TSLDCLK). TSLDCLK is used to clock in the transmit section or line DCC (TSLD). When section DCC is selected, TSLDCLK is a nominal 192 kHz clock with 50% duty cycle. When line DCC is selected, TSLDCLK is a nominal 576 kHz clock with 50% duty cycle. TSLD is sampled on the rising edge of TSLDCLK and TOHFP is used to identify the MSB of the D1 or the D4 byte on TSLD.
TSLD	Input	AN3	Transmit section or Line Data Communication Channel Data (TSLD). TSLD signal contains the section DCC (D1-D3) or the line DCC (D4-D12) to be transmitted. TSLD is sampled on the rising edge of TSLDCLK. TOHFP is used to identify the MSB of the D1 or the D4 byte on TSLD. The TTOH and TTOHEN inputs take precedence over TSLD.

9.11 Receive SONET/SDH Overhead Extraction

Pin Name	Type	Pin No.	Function
ROHCLK	Output	AN1	Receive Overhead Clock (ROHCLK). ROHCLK signal provides timing for the receive section, line and path overhead extraction. ROHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. ROHCLK has a 33% high duty cycle.
ROHFP	Output	AM2	Receive Overhead frame Pulse (ROHFP) ROHFP provides timing for the receive section, line and path overhead extraction. ROHFP is used to indicate the most significant bit (MSB) on RSLD, RTOH, RPOH and the first possible path BIP error on B3E. ROHFP is set high when the MSB of the: D1 or D4 byte is present on RSLD. First A1 byte is present on RTOH. First J1 byte is present on RPOH. ROHFP is updated on the falling edge of ROHCLK.
RTOH	Output	AM1	Receive Transport Overhead (RTOH). RTOH contains the received transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) extracted from the incoming TelecomBus stream. RTOH is updated on the falling edge of ROHCLK.
RPOH	Output	AL3	Receive Path Overhead (RPOH). RPOH contains the received path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the SONET/SDH path overhead of the incoming TelecomBus stream. The RPOHEN signal is set high to indicate valid path overhead bytes on RPOH. RPOH is updated on the falling edge of ROHCLK.
RPOHEN	Output	AL1	Receive Path Overhead Enable (RPOHEN). RPOHEN signal indicates valid path overhead bytes on RPOH. When RPOHEN signal is set high, the corresponding path overhead byte presented on RPOH is valid. When RPOHEN is set low, the corresponding path overhead byte presented on RPOH is invalid. RPOHEN is updated on the falling edge of ROHCLK.

Pin Name	Type	Pin No.	Function
SALM	Output	AK1	Section Alarm Indication (SALM). SALM signal is set high when an out of frame (OOF), loss of signal (LOS), loss of frame (LOF), line alarm indication signal (AIS-L), line remote defect indication (RDI-L), APS byte failure, section trace identifier mismatch (TIM-S), section trace identifier unstable (TIU-S), signal fail (SF) or signal degrade (SD) alarm is detected. Each alarm indication can be independently enabled using bits in the SARC RSALM registers. SALM is updated on the falling edge of ROHCLK.
RALM	Output	AJ4	Receive Alarm Indication (RALM) RALM signal is set high for the corresponding path when a section alarm, path loss of pointer (LOP-P), path alarm indication signal (AIS-P), path remote defect indication (RDI-P), path enhance remote defect indication (ERDI-P), path label mismatch (PLM), path label unstable (PLU), path unequipped (UNEQ), path payload defect indication (PDI-P), path trace identifier mismatch (TIM-P) or path trace identifier unstable (TIU-P) alarm is detected. Each alarm indication can be independently enabled using bits in the SARC RPALM registers. RALM is updated on the falling edge of ROHCLK.
B3E	Output	AJ3	Bit interleaved Parity Error (B3E). B3E signal carries the path BIP-8 errors detected for each SONET/SDH payload. B3E is set high for one ROHCLK clock cycle for each path BIP-8 error detected (up to eight errors per path per frame). When BIP-8 errors are treated on a block basis, B3E is set high for one ROHCLK clock cycle for up to eight path BIP-8 errors detected (up to one error per path per frame). Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed path BIP-8 byte of the previous frame. B3E is updated on the falling edge of ROHCLK.

Pin Name	Type	Pin No.	Function
RSLDCLK	Tristate Output	AJ2	Receive section or Line Data Communication Channel Clock (RSLDCLK). RSLDCLK is used to update the receive section or line DCC (RSLD). When section DCC is selected, RSLDCLK is a nominal 192 kHz clock with 50% duty cycle. When line DCC is selected, RSLDCLK is a nominal 576 kHz clock with 50% duty cycle. The RSLDSEL bit in the RRMP 1990H registers selects the section or line DCC and the RSLDTS bit tri-states RSLDCLK and RSLD outputs. RSLD is updated on the falling edge of RSLDCLK. ROHFP may be used to identify the MSB of the D1 or the D4 byte on RSLD.
RSLD	Tristate Output	AH5	Receive section or Line Data Communication Channel Data (RSLD). RSLD contains the received section DCC (D1-D3) or line DCC (D4-D12). The RSLDSEL bit in the RRMP 1990H registers selects the section or line DCC and the RSLDTS bit tri-states RSLDCLK and RSLD outputs. RSLD is updated on the falling edge of RSLDCLK. The signal should be sampled externally on the rising edge of RSLDCLK. ROHFP is used to identify the MSB of the D1 or the D4 byte on RSLD.

9.12 Transmit Serial Auxiliary Interface

Pin Name	Type	Pin No.	Function
TICLK[0] TICLK[1] TICLK[2] TICLK[3] TICLK[4] TICLK[5] TICLK[6] TICLK[7] TICLK[8] TICLK[9] TICLK[10] TICLK[11]	Input	B26 A20 B18 A11 C10 C4 AL28 AP23 AP21 AM15 AP13 AN7	Transmit Input Clock (TICLK[11:0]). TICLK[11:0] provides the transmit direction timing when FRAC[1:0] is configured for frame-only or external serial payload processing for 12 channels. TICLK[11:0] is the externally generated transmission system baud rate clock. TICLK[11:0] are used to generate the serial line interface clocking. In this mode, TCLK[11:0] is either a buffered version of TICLK[11:0] or a jitter attenuated version from the outgoing PLL (JAT). For SONET/SDH mapping applications, TICLK[11:0] are used to generate the outgoing mapped DS3/E3 streams on the TelecomBus interface. TICLK/IFBWCLK[11:0] pin function selections are controlled by FRAC[1:0] mode pins. TICLK is a free-running clock with a maximum frequency of 52 MHz and a nominal 50% duty cycle. The frequency of TICLK depends on the mode of operation of the particular slice. For DS3 operation TICLK frequency is 44.736MHz, for E3 operation TICLK frequency is 34.368MHz, for J2 operation TICLK frequency is 6.312 MHz, for E1 operation TICLK frequency is 2.048 MHz, and for T1 operation TICLK frequency is a nominal 1.544 MHz.
TDATI[0] TDATI[1] TDATI[2] TDATI[3] TDATI[4] TDATI[5] TDATI[6] TDATI[7] TDATI[8] TDATI[9] TDATI[10] TDATI[11]	Input	A26 B20 A18 B12 D10 A4 AM28 AN23 AL20 AN15 AN13 AP7	Framer Transmit Data (TDATI[11:0]). TDATI[11:0] contains the serial data to be transmitted when the S/UNI-12xJET is configured for framer operations and FRAC[1:0] is configured for frame-only or external serial payload processing for 12 channels. When configured for framer-only modes, TDATI[11:0] are used to generate the serial line interface data. For SONET/SDH mapping applications, TDATI[11:0] are used to generate the outgoing mapped DS3/E3 streams on the TelecomBus interface. TDATI/IFBWDAT[11:0] pin function selections are controlled by FRAC[1:0] mode pins. TDATI/IFBWDAT[11:0] are sampled on the rising edge of TICLK[11:0].

Pin Name	Type	Pin No.	Function
TIOHM[0] TIOHM[1] TIOHM[2] TIOHM[3] TIOHM[4] TIOHM[5] TIOHM[6] TIOHM[7] TIOHM[8] TIOHM[9] TIOHM[10] TIOHM[11]	Input	E25 C20 A17 A12 E10 A5 AN28 AP24 AM20 AP15 AP12 AL8	Transmit Input Overhead Mask (TIOHM[11:0]). TIOHM[11:0] indicates the position of overhead bits when not configured for DS1, DS3, E1, E3, or J2 transmission system streams and FRAC[1:0] is configured for frame-only or external serial payload processing for 12 channels. When configured for framer-only modes, TIOHM[11:0] are used to generate the serial line interface data. For SONET/SDH mapping applications, TIOHM[11:0] are used to generate the outgoing mapped DS3/E3 streams on the TelecomBus interface. TIOHM[11:0] is delayed internally to produce the TOHM[11:0] output. When configured for operation over a DS1, a DS3, an E1, an E3, or a J2 transmission system sub-layer, TIOHM[11:0] is not required, and should be set to logic 0. When configured for other transmission systems, TIOHM[11:0] is set to logic 1 for each overhead bit position. TIOHM[11:0] is set to logic 0 if the transmission system contains no overhead bits. TIOHM/TFPI/TMFPI/IFBWEN[11:0] pin function selections are controlled by FRAC[1:0] mode pins. TIOHM[11:0] are sampled on the rising edge of TICLK[11:0].
TFPI[0] TFPI[1] TFPI[2] TFPI[3] TFPI[4] TFPI[5] TFPI[6] TFPI[7] TFPI[8] TFPI[9] TFPI[10] TFPI[11]	Input	E25 C20 A17 A12 E10 A5 AN28 AP24 AM20 AP15 AP12 AL8	Framer Transmit Frame Pulse (TFPI[11:0]). TFPI[11:0] indicate the position of all overhead bits in each DS3 M-subframe, the first bit in each G.751 E3 or G.832 E3 frame, or the first framing bit in each J2 frame. TFPI[11:0] is not required to pulse at every frame boundary in E3 or J2 modes. FRAC[1:0] must be configured for frame-only or external serial payload processing for 12 channels. When configured for framer-only modes, TFPI[11:0] are used to generate the serial line interface data. For SONET/SDH mapping applications, TFPI[11:0] are used to generate the outgoing mapped DS3/E3 streams on the TelecomBus interface. TIOHM/TFPI/TMFPI/IFBWEN[11:0] pin function selections are controlled by FRAC[1:0] mode pins. TFPI[11:0] are sampled on the rising edge of TICLK[11:0].

Pin Name	Type	Pin No.	Function
TMFPI[0] TMFPI[1] TMFPI[2] TMFPI[3] TMFPI[4] TMFPI[5] TMFPI[6] TMFPI[7] TMFPI[8] TMFPI[9] TMFPI[10] TMFPI[11]	Input	E25 C20 A17 A12 E10 A5 AN28 AP24 AM20 AP15 AP12 AL8	Framer Transmit Multi-frame Pulse (TMFPI[11:0]). TMFPI[11:0] indicate the position of the first bit in each DS3 M-frame, the first bit in each E3 frame, or the first framing bit in each J2 multi-frame. TMFPI[11:0] is not required to pulse at every multi-frame boundary. FRAC[1:0] must be configured for frame-only or external serial payload processing for 12 channels. When configured for framer-only modes, TMFPI[11:0] are used to generate the serial line interface data. For SONET/SDH mapping applications, TMFPI[11:0] are used to generate the framing information for outgoing mapped DS3/E3 streams into SONET/SDH. TIOHM/TFPI/TMFPI/IFBWEN[11:0] pin function selections are controlled by FRAC[1:0] mode pins. TMFPI[11:0] are sampled on the rising edge of TICLK[11:0].
TFPO[0] TFPO[1] TFPO[2] TFPO[3] TFPO[4] TFPO[5] TFPO[6] TFPO[7] TFPO[8] TFPO[9] TFPO[10] TFPO[11]	Output	A25 C21 B16 D14 D9 E7 AN27 AP25 AL19 AN16 AM11 AK9	Framer Transmit Frame Pulse Reference (TFPO[11:0]). When configured for framer-only mode, TFPO[11:0] are used to generate the serial line interface data. For SONET/SDH mapping applications, TFPO[11:0] are used to generate the outgoing TelecomBus stream. TFPO[11:0] pulses high for 1 out of every 85 clock cycles when configured for DS3, giving a free-running mark for all overhead bits in the frame. TFPO[11:0] pulses high for 1 out of every 1536 clock cycles when configured for G.751 E3, giving a free-running reference G.751 indication. TFPO[11:0] pulses high for 1 out of every 4296 clock cycles when configured for G.832 E3, giving a free-running reference G.832 frame indication. TFPO[11:0] pulses high for 1 out of every 789-clock cycles when configured for J2, giving a free-running reference frame indication. TFPO[11:0] are updated on the rising edge of TICLK[11:0] or RCLK[11:0] if loop-timed of the serial line interface.

Pin Name	Type	Pin No.	Function
TMFPO[0] TMFPO[1] TMFPO[2] TMFPO[3] TMFPO[4] TMFPO[5] TMFPO[6] TMFPO[7] TMFPO[8] TMFPO[9] TMFPO[10] TMFPO[11]	Output	A25 C21 B16 D14 D9 E7 AN27 AP25 AL19 AN16 AM11 AK9	Framer Transmit Multi-frame Pulse Reference (TMFPO[11:0]). When configured for framer-only mode, TMFPO[11:0] are used to generate the serial line interface data. For SONET/SDH mapping applications, TMFPO[11:0] are used to generate the outgoing TelecomBus stream. TMFPO[11:0] pulses high for 1 out of every 4760 clock cycles when configured for DS3, giving a free-running reference M-frame indication. TMFPO[11:0] pulses high for 1 out of every 3156 clock cycles when configured for J2, giving a free-running reference multi-frame indication. TMFPO[11:0] behaves the same as TFPO[11:0] for E3 applications. TMFPO[11:0] are updated on the rising edge of TICLK[11:0] or RCLK[11:0] if loop-timed.

9.13 Receive Serial Auxiliary Interface

Pin Name	Type	Pin No.	Function
RSCLK[0] RSCLK[1] RSCLK[2] RSCLK[3] RSCLK[4] RSCLK[5] RSCLK[6] RSCLK[7] RSCLK[8] RSCLK[9] RSCLK[10] RSCLK[11]	I/O	D24 D21 C16 C14 E9 A6 AP27 AN25 AM19 AP16 AL11 AL9	Framer Recovered Clock (RSCLK[11:0]). RSCLK[11:0] are the recovered line rate clock and timing reference for RDAT0[11:0], RFPO/RMFPO[11:0] and ROVRDHD[11:0] when FRAC[1:0] is configured for frame-only or external serial payload processing for 12 channels. RSCLK[11:0] is always driven as an output in these modes. When configured for framer-only modes, RSCLK[11:0] are either a buffered version of the RCLK[11:0] or a jitter attenuated version for the incoming PLL (JAT). For SONET/SDH demapping applications, RSCLK[11:0] are generated from the incoming TelecomBus stream. RSCLK/EFBWCLK[11:0] pin function selections are controlled by FRAC[1:0] mode pins. RSCLK[11:0] are the recovered clock and timing reference for RDATO[11:0], RFPO / RMFPO[11:0], and ROVRHD[11:0].
RDATO[0] RDATO[1] RDATO[2] RDATO[3] RDATO[4] RDATO[5] RDATO[6] RDATO[7] RDATO[8] RDATO[9] RDATO[10] RDATO[11]	Output	C24 E21 D16 B14 A8 D7 AK26 AM25 AN19 AM17 AP10 AM9	Framer Receive Data (RDATO[11:0]). RDATO[11:0] are the received data aligned to RFPO/RMFPO[11:0] and ROVRHD[11:0] when FRAC[1:0] is configured for frame-only or external serial payload processing for 12 channels. When configured for framer-only modes, RDATO[11:0] are delayed versions of the serial line interface data inputs. For SONET/SDH demapping applications, RDATO[11:0] are generated from the incoming TelecomBus stream. RDATO[11:0] are the received data aligned to RFPO/RMFPO[11:0] and ROVRHD[11:0]. RDATO/EFBWDAT[11:0] pin function selections are controlled by FRAC[1:0] mode pins. RDATO[11:0] are updated on the rising edge of RSCLK[11:0].

Pin Name	Type	Pin No.	Function
RFPO[0] RFPO[1] RFPO[2] RFPO[3] RFPO[4] RFPO[5] RFPO[6] RFPO[7] RFPO[8] RFPO[9] RFPO[10] RFPO[11]	Output	B24 A22 E16 A14 B8 C7 AL26 AL25 AP19 AN17 AN10 AN9	Framer Receive Frame Pulse/Multi-frame Pulse (RFPO[11:0]). RFPO[11:0] are aligned to RDATO[11:0] and indicate the position of the first bit in each DS3 M-subframe, the first bit in each G.751 E3 or G.832 E3 frame, or the first framing bit in each J2 frame. FRAC[1:0] must be configured for frame-only or external serial payload processing for 12 channels. When configured for framer-only mode, RFPO[11:0] are derived from the incoming serial line side interfaces. For SONET/SDH demapping applications, RFPO[11:0] are generated from the incoming TelecomBus stream. RFPO/RMFPO/EFBWEN[11:0] pin function selections are controlled by FRAC[1:0] mode pins. RFPO[11:0] are updated on the rising edge of RSCLK[11:0].
RMFPO[0] RMFPO[1] RMFPO[2] RMFPO[3] RMFPO[4] RMFPO[5] RMFPO[6] RMFPO[7] RMFPO[8] RMFPO[9] RMFPO[10] RMFPO[11]	Output	B24 A22 E16 A14 B8 C7 AL26 AL25 AP19 AN17 AN10 AN9	Framer Receive Frame Pulse/Multi-frame Pulse (RFPO/RMFPO[11:0]). When configured for framer-only modes, RMFPO[11:0] are derived from the incoming serial line side interfaces. For SONET/SDH demapping applications, RMFPO[11:0] are generated from the incoming TelecomBus stream. FRAC[1:0] must be configured for frame-only or external serial payload processing for 12 channels. RMFPO[11:0] are aligned to RDATO[11:0] and indicates the position of the first bit in each DS3 M-frame, the first bit in each G.751 or G.832 E3 multi-frame, or the first framing bit in each J2 multi-frame. RFPO/RMFPO/EFBWEN[11:0] pin function selections are controlled by FRAC[1:0] mode pins. RMFPO[11:0] are updated on the rising edge of RSCLK[11:0].
ROVRHD[0] ROVRHD[1] ROVRHD[2] ROVRHD[3] ROVRHD[4] ROVRHD[5] ROVRHD[6] ROVRHD[7] ROVRHD[8] ROVRHD[9] ROVRHD[10] ROVRHD[11]	I/O	A24 B22 A15 D15 C8 B7 AM26 AK25 AM18 AP17 AM10 AP9	Framer Receive Overhead Indication (ROVRHD[11:0]). ROVRHD[11:0] are high whenever the data on RDATO[11:0] corresponds to an overhead bit position. FRAC[1:0] must be configured for frame-only mode. When configured for framer-only modes, ROVRHD[11:0] are derived from the incoming serial line side interfaces. For SONET/SDH demapping applications, ROVRHD[11:0] are generated from the incoming TelecomBus stream. ROVRHD/EFBWDREQ[11:0] pin function selections are controlled by FRAC[1:0] mode pins. ROVRHD[11:0] are updated on the rising edge of RSCLK[11:0].

Pin Name	Type	Pin No.	Function
FRMSTAT[0] FRMSTAT[1] FRMSTAT[2] FRMSTAT[3] FRMSTAT[4] FRMSTAT[5] FRMSTAT[6] FRMSTAT[7] FRMSTAT[8] FRMSTAT[9] FRMSTAT[10] FRMSTAT[11]	Output	B23 A23 B15 C15 D8 A7 AN26 AP26 AN18 AP18 AL10 AK10	Framer Status (FRMSTAT[11:0]). FRMSTAT[11:0] is an active high signal which can be configured to show when one of the J2, E3, DS3, or PLCP framers have detected certain conditions. The FRMSTAT[11:0] outputs can be programmed via the STATSEL[2:0] bits in the S/UNI-12xJET Configuration registers to indicate: E3/DS3 Loss of Frame or J2 extended Loss of Frame, E3/DS3 Out of Frame or J2 Loss of Frame, PLCP Loss of Frame, PLCP Out of Frame, AIS, Loss of Signal, and DS3 Idle. As well, for applications using the SONET/SDH TelecomBus interface, the FRMSTAT[11:0] may be configured to assert on selected SONET/SDH alarms. FRMSTAT[11:0] should be treated as glitch free asynchronous signals.

9.14 Ingress Flexible Bandwidth Interface

Pin Name	Type	Pin No.	Function
IFBWCLK[0] IFBWCLK[1] IFBWCLK[2] IFBWCLK[3] IFBWCLK[4] IFBWCLK[5] IFBWCLK[6] IFBWCLK[7] IFBWCLK[8] IFBWCLK[9] IFBWCLK[10] IFBWCLK[11]	Input	(See Section 9.3 and Section 9.12 for Pin No.)	Ingress Flexible Bandwidth Clocks (IFBWCLK[11:0]). IFBWCLK clocks provide the timing for an arbitrary bandwidth payload to be inserted into the receive cell/packet processors and migrate to the Receive System Side Interface. IFBWCLK[11:0] may have a maximum frequency of 51.84 MHz and may be gapped if required. TICLK/IFBWCLK[11:0] or RCLK/IFBWCLK[11:0] pin function selections are controlled by FRAC[1:0] mode pins. When FRAC[1:0] mode is framer-only mode (“00”), this interface is unused. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“01”), RCLK/IFBWCLK[11:0] pins are the source of the IFBWCLK[11:0]. When FRAC[1:0] mode is external serial payload processing for six channels (“10”) all odd channels TICLK/IFBWCLK[11:0] are the source of the even channel’s IFBWCLK[11:0]. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“11”), TICLK/IFBWCLK[11:0] are the source of IFBWCLK[11:0]. Each IFBWCLK samples the associated IFBWDAT[11:0] and IFBWEN[11:0] on the rising edge.
IFBWDAT[0] IFBWDAT[1] IFBWDAT[2] IFBWDAT[3] IFBWDAT[4] IFBWDAT[5] IFBWDAT[6] IFBWDAT[7] IFBWDAT[8] IFBWDAT[9] IFBWDAT[10] IFBWDAT[11]	Input	(See Section 9.3 and Section 9.12 for Pin No.)	Ingress Flexible Bandwidth Data (IFBWDAT[11:0]). IFBWDAT[n] provides bit serial data to be inserted into the receive cell/packet processors and migrate to the Receive System Side Interface for slice n. When IFBWEN[n] input is sampled high, IFBWDAT[n] is accepted in the device. TDATI/IFBWDAT[11:0] or RPOS/RDATI/IFBWDAT[11:0] pin function selections are controlled by FRAC[1:0] mode pins. When FRAC[1:0] mode is framer-only mode (“00”), this interface is unused. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“01”), RPOS/RDAT/IFBWDAT[11:0] pins are the source of the IFBWDAT[11:0]. When FRAC[1:0] mode is external serial payload processing for six channels (“10”) all odd channels TDATI/IFBWDAT[11:0] are the source of the even channel’s IFBWDAT[11:0]. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“11”), TDATI/IFBWDAT[11:0] are the source of IFBWDAT[11:0]. IFBWDAT[11:0] are sampled on the rising edge of the associated IFBWCLK[11:0] input.

Pin Name	Type	Pin No.	Function
IFBWEN[0] IFBWEN[1] IFBWEN[2] IFBWEN[3] IFBWEN[4] IFBWEN[5] IFBWEN[6] IFBWEN[7] IFBWEN[8] IFBWEN[9] IFBWEN[10] IFBWEN[11]	Input	(See Section 9.3 and Section 9.12 for Pin No.)	Ingress Flexible Bandwidth Enable (IFBWEN[11:0]). IFBWEN indicates a valid bit on the associated IFBWDAT input. When IFBWEN is logic high, IFBWDAT is valid, otherwise IFBWDAT is invalid. TIOHM/TFPI/TMFPI/IFBWEN[11:0] or RNEG/RLCV/ROHM/IFBWEN[11:0] pin function selections are controlled by FRAC[1:0] mode pins. When FRAC[1:0] mode is framer-only mode (“00”), this interface is unused. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“01”), RNEG/RLCV/ROHM/IFBWEN[11:0] pins are the source of the IFBWEN[11:0]. When FRAC[1:0] mode is external serial payload processing for six channels (“10”) all odd channels TIOHM/TFPI/TMFPI/IFBWEN[11:0] are the source of the even channel’s IFBWEN[11:0]. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“11”), TIOHM/TFPI/TMFPI/IFBWEN [11:0] are the source of IFBWEN[11:0]. IFBWEN[11:0] are sampled on the rising edge of the associated IFBWCLK[11:0] input.

9.15 Egress Flexible Bandwidth Interface

Pin Name	Type	Pin No.	Function
EFBWCLK[0] EFBWCLK[1] EFBWCLK[2] EFBWCLK[3] EFBWCLK[4] EFBWCLK[5] EFBWCLK[6] EFBWCLK[7] EFBWCLK[8] EFBWCLK[9] EFBWCLK[10] EFBWCLK[11]	Input	(See Section 9.2 and Section 9.13 for Pin No.)	Egress Flexible Bandwidth Clocks (EFBWCLK[11:0]). EFBWCLK clocks provide the timing for an arbitrary bandwidth payload to be extracted from the transmit cell/packet processors whose original source is the Transmit System Side Interface. EFBWCLK[11:0] may have a maximum frequency of 51.84 MHz and may be gapped if required. RSCLK/EFBWCLK[11:0] or TCLK/EFBWCLK[11:0] pin function selections are controlled by FRAC[1:0] mode pins. When FRAC[1:0] mode is framer-only mode (“00”), this interface is unused. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“01”), TCLK/EFBWCLK[11:0] pins are the source of the EFBWCLK[11:0]. When FRAC[1:0] mode is external serial payload processing for six channels (“10”) all odd channels RSCLK/EFBWCLK[11:0] are the source of the even channel’s EFBWCLK[11:0]. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“11”), RSCLK/EFBWCLK[11:0] are the source of EFBWCLK[11:0]. Each EFBWCLK samples the associated EFBWDREQ[11:0] and updates EFBWDAT[11:0] and EFBWEN[11:0] on the rising edge.

Pin Name	Type	Pin No.	Function
EFBWDREQ[0] EFBWDREQ[1] EFBWDREQ[2] EFBWDREQ[3] EFBWDREQ[4] EFBWDREQ[5] EFBWDREQ[6] EFBWDREQ[7] EFBWDREQ[8] EFBWDREQ[9] EFBWDREQ[10] EFBWDREQ[11]	Input	(See Section 9.13 for Pin No.)	Egress Flexible Bandwidth Data Requests (EFBWDREQ[11:0]). EFBWDREQ provide a data request to extract serial data out of the transmit cell/packet processors through EFBWDAT. When EFBWDREQ is asserted high for an EFBWCLK cycle, a single bit of data is requested. In response to sampling EFBWDREQ high, the associated EFBWDAT output will either present an available bit no more than 16 EFBWCLK cycles later with an accompanying assertion of the associated EFBWEN or ignore the request if no data is ready. In many applications, every request will be acknowledged with data. In applications where the source data is fixed, it is permissible to hold EFBWDREQ high in which case EFBWEN identifies valid bytes. ROVRHD/EFBWDREQ[11:0] pin function selections are controlled by FRAC[1:0] mode pins. When FRAC[1:0] mode is framer-only mode (“00”), this interface is unused. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“01”), ROVRHD/EFBWDREQ[11:0] pins are the source of the EFBWDREQ[11:0]. When FRAC[1:0] mode is external serial payload processing for six channels (“10”) all odd channels ROVRHD/EFBWDREQ[11:0] are the source of the even channel’s EFBWDREQ[11:0]. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“11”), ROVRHD/EFBWDREQ[11:0] are the source of EFBWDREQ[11:0]. EFBWDREQ[11:0] are sampled on the rising edge of the associated EFBWCLK[11:0].

Pin Name	Type	Pin No.	Function
EFBWDAT[0] EFBWDAT[1] EFBWDAT[2] EFBWDAT[3] EFBWDAT[4] EFBWDAT[5] EFBWDAT[6] EFBWDAT[7] EFBWDAT[8] EFBWDAT[9] EFBWDAT [10] EFBWDAT [11]	Output	(See Section 9.2 and Section 9.13 for Pin No.)	Egress Flexible Bandwidth Data (EFBWDAT[11:0]). EFBWDAT is a bit serial data stream from the transmit cell/packet processors. When EFBWEN output is high, EFBWDAT is valid. RDATO/EFBWDAT[11:0] or TPOS/TDATO/EFBWDAT [11:0] pin function selections are controlled by FRAC[1:0] mode pins. When FRAC[1:0] mode is framer-only mode (“00”), this interface is unused. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“01”), TPOS/TDATO/EFBWDAT[11:0] pins are the sink for EFBWDAT[11:0]. When FRAC[1:0] mode is external serial payload processing for six channels (“10”) all odd channels RDATO/EFBWDAT[11:0] are the sink for even channel’s EFBWDAT[11:0]. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“11”), RDATO/EFBWDAT[11:0] are the sink for EFBWDAT[11:0]. EFBWDAT[11:0] are updated on the rising edge of the associated EFBWCLK[11:0] input.
EFBWEN[0] EFBWEN[1] EFBWEN[2] EFBWEN[3] EFBWEN[4] EFBWEN[5] EFBWEN[6] EFBWEN[7] EFBWEN[8] EFBWEN[9] EFBWEN[10] EFBWEN[11]	Output	(See Section 9.2 and Section 9.13 for Pin No.)	Egress Flexible Bandwidth Enable (EFBWEN[11:0]). EFBWEN indicates a valid bit on the associated EFBWDAT output. When EFBWEN is logic high, EFBWDAT is valid, otherwise EFBWDAT is invalid. RFPO/RMFPO/EFBWEN[11:0] or TNEG/TOHM /EFBWEN[11:0] pin function selections are controlled by FRAC[1:0] mode pins. When FRAC[1:0] mode is framer-only mode (“00”), this interface is unused. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“01”), TNEG/TOHM/EFBWEN[11:0] pins are the sink for EFBWEN[11:0]. When FRAC[1:0] mode is external serial payload processing for six channels (“10”) all odd channels RFPO/RMFPO/EFBWEN[11:0] are the sink for the even channel’s EFBWEN[11:0]. When FRAC[1:0] mode is external serial payload processing for all 12 channels (“11”), RFPO/RMFPO/EFBWEN [11:0] are the sink for EFBWEN[11:0]. EFBWEN[11:0] are updated on the rising edge of the associated EFBWCLK[11:0] input.

9.16 Transmit System Side Interface

Pin Name	Type	Pin No.	Function
TFCLK	Input	V33	The UTOPIA transmit FIFO write clock (TFCLK) is used to write ATM cells to the cell transmit FIFO. In UTOPIA Level 3 operation, TFCLK must cycle at a 104 MHz to 60 MHz instantaneous rate, and must be a free running clock (cannot be gapped). In UTOPIA Level 2 operation, TFCLK must cycle at a 52 MHz to 30 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
			The POS-PHY transmit FIFO write clock (TFCLK) is used to write packet data into the packet FIFO. In POS-PHY Level 3 operation, TFCLK must cycle at a 104 MHz to 60 MHz instantaneous rate, and must be a free running clock (cannot be gapped). In POS-PHY Level 2 operation, TFCLK must cycle at a 52 MHz to 30 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15] TDAT[16] TDAT[17] TDAT[18] TDAT[19] TDAT[20] TDAT[21] TDAT[22] TDAT[23] TDAT[24] TDAT[25] TDAT[26] TDAT[27] TDAT[28] TDAT[29] TDAT[30] TDAT[31]	Input	P32 P31 P30 N34 N33 M34 M33 L34 L33 L32 L31 K34 K33 K32 K31 K30 J34 J33 J32 J31 J30 H34 H33 H32 H31 G34 G33 G32 G31 F34 G30 F33	The UTOPIA transmit cell data (TDAT[31:0]) bus carries the ATM cell octets that are written to the transmit FIFO. In UTOPIA Level 3 operation, the TDAT[31:0] bus is considered valid only when TENB is simultaneously asserted. TDAT[31] is the first bit transmitted and TDAT[0] is the last bit transmitted. In UTOPIA Level 2 operation, the TDAT[15:0] bus is considered valid only when TENB is simultaneously asserted. TDAT[31:16] is ignored. TDAT[31:0] is sampled on the rising edge of TFCLK.
			The POS-PHY transmit packet data (TDAT[31:0]) bus carries the POS packet octets that are written to the transmit FIFO. In POS-PHY Level 3 operation, the packet data sample on TDAT[31:0] is considered valid when TENB is sampled low. The value sampled on TDAT[7:0] is also used to select a PHY channel when TENB and TSX are sampled high. TDAT[31] is the first bit transmitted and TDAT[0] is the last bit transmitted. In POS-PHY Level 2 operation, the TDAT[15:0] bus is considered valid only when TENB is simultaneously asserted. TDAT[31:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TPRTY	Input	P33	The UTOPIA transmit bus parity (TPRTY) signal indicates the parity on the TDAT bus. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are inserted in the transmit stream, so the TPRTY input may be unused. In UTOPIA Level 3 operation, TPRTY is calculated over TDAT[31:0]. In UTOPIA Level 2 operation, TPRTY is calculated over TDAT[15:0]. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.
			The POS-PHY transmit bus parity (TPRTY) signal indicates the parity on the TDAT bus. A parity error is indicated by a status bit and a maskable interrupt. Packets with parity errors are inserted in the transmit stream, so the TPRTY input may be unused. In POS-PHY Level 3 operation, TPRTY is calculated over TDAT[31:0]. In POS-PHY Level 2 operation, TPRTY is calculated over TDAT[15:0]. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.
TENB	Input	P34	The UTOPIA transmit write enable (TENB) signal is an active low input which is used to initiate writes to the transmit FIFOs. When TENB is sampled high, the data sampled on TDAT, TRPTY and TSOC is invalid. When TENB is sampled low, the information sampled on TDAT, TPRTY and TSOC is valid and is written into the FIFO. A high to low transition on TENB is needed in conjunction with TADR to select the transmit PHY. TENB is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
			The POS-PHY transmit write enable (TENB) signal is an active low input which is used to initiate writes to the transmit FIFOs. When TENB is sampled high, the information sampled on TDAT, TPRTY, TSOP, TEOP, TMOD and TERR is invalid. When TENB is sampled low, the information sampled on TDAT, TPRTY, TSOP, TEOP, TMOD and TERR is valid and is written into the FIFO. For Level 3 operation, TSX is ignored when TENB is low. For Level 2 operation, TSX is ignored. TENB is sampled on the rising edge of TFCLK.
TSOC	Input	R31	The UTOPIA transmit start of cell (TSOC) signal marks the start of a cell structure on the TDAT bus. When TSOC is sampled high, the first word of the ATM cell structure is sampled on the TDAT bus. TSOC should be present for each cell structure. TSOC is considered valid only when TENB is simultaneously asserted. TSOC is sampled on the rising edge of TFCLK.
TSOP			The POS-PHY transmit start of packet (TSOP) signal. indicates the start of a packet on the TDAT bus. When TSOP is sampled high, the first word of the packet is sampled on TDAT bus. TSOP is required to be present at all instances for proper operation. TSOP is considered valid only when TENB is simultaneously asserted. TSOP is sampled on the rising edge of TFCLK.
TEOP	Input	R32	The POS-PHY transmit end of packet (TEOP) marks the end of packet on the TDAT bus when configured for packet data. TEOP sampled high indicates the last word of the packet is sampled on the TDAT bus. The TMOD bus indicates how many valid bytes of packet data are in the last word. It is legal to set TSOP high at the same time as TEOP is high in order to support small packets. TEOP is only valid when TENB is simultaneously asserted. TEOP is only used for POS-PHY operation and is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TERR	Input	R33	The POS-PHY transmit error (TERR) is used to indicate that the current packet must be aborted. Packets marked with TERR will be appended with the HDLC abort sequence when transmitted. TERR sampled high when TEOP is sampled high marks the current packet to be aborted. TERR is only considered valid when TENB and TEOP are simultaneously asserted. TERR is only used for POS-PHY operation and is sampled on the rising edge of TFCLK.
TMOD[0] TMOD[1]	Input	R34 T30	The POS-PHY transmit word modulo (TMOD) signal indicates the number of valid bytes of data on TDAT bus during POS-PHY operation. TMOD is only used for POS-PHY operation and is ignored for channels carrying ATM traffic when TEOP is high. For POS-PHY Level 3 operation, the value sampled on the TMOD[1:0] bus when TEOP is sampled high specifies the number of valid byte of packet data on TDAT[31:0]. ”00” TDAT[31:0] valid ”01” TDAT[31:8] valid ”10” TDAT[31:16] valid ”11” TDAT[31:24] valid For POS-PHY Level 2 operation, the value sampled on TMOD[0] when TEOP is sampled high specifies the number of valid bytes of packet data on TDAT[15:0]. When TMOD[0] is low, TDAT[15:0] is valid. When TMOD[0] is low, TDAT[15:8] is valid. TMOD[1] is ignored for Level 2 operation. TMOD is considered valid only when TENB and TEOP are simultaneously asserted. TMOD is sampled on the rising edge of TFCLK.
TSX	Input	T31	The POS-PHY transmit start of transfer (TSX) indicates when the in-band port address is present on the TDAT bus during POS-PHY Level 3 operation. When TSX and TENB are sampled high, the value sampled on TDAT[7:0] is the address of the transmit PHY channel to be selected. Subsequent data transfers on the TDAT bus will fill the channel FIFO buffer specified by this in-band address. The value sampled on TSX is considered valid only when TENB is sampled high. TSX is only used for POS-PHY operation. TSX must be tied low in UTOPIA and POS-PHY Level 2 operation. TSX is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
STPA	Output	T32	The POS-PHY selected transmit packet available (STPA) signal provides status indication of when cell space is available in the transmit FIFO. The channel selected using TSX is reported on STPA. When STPA transitions high, it indicates that the transmit FIFO has enough room to store a configurable number of data bytes. When STPA transitions low, it indicates that the transmit FIFO is either full or near full. STPA is updated on the rising edge of TFCLK.
TADR[0] TADR[1] TADR[2] TADR[3] TADR[4]	Input	T34 U32 U33 U34 V34	The UTOPIA transmit port address select (TADR) is used to select the channel whose FIFO fill status is to be polled or the channel for which a UTOPIA cell transfer is desired. For Level 3 operation, when TENB transitions from high to low, the value sampled on TADR[3:0] selects the channel FIFO that the ATM cell is written to. During all other conditions, the fill status of the channel FIFO with the address sampled on TADR[4:0] is reported on TCA on the following clock cycle. For Level 2 operation, when TENB transitions from high to low, the value sampled on TADR[4:0] selects the channel FIFO which the ATM cell is written to. During all other conditions, the fill status of the channel FIFO with the address sampled on TADR[4:0] is immediately reported on TCA. TADR[4:0] is sampled on the rising edge of TFCLK.
			The POS-PHY transmit port address select (TADR) is used to select the channel whose FIFO fill status is to be polled. For Level 3 operation, the address sampled on TADR[3:0] specifies the channel FIFO being polled. The PTPA output is updated on the following clock cycle with the channel's fill level based on the programmable thresholds. For Level 2 operation, when TENB transitions from high to low, the value sampled on TADR[4:0] selects the channel FIFO that the packet data is written to. During all other conditions, the fill status of the channel FIFO with the address sampled on TADR[4:0] is immediately reported on PTPA. TADR[4:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TCA	Output	T33	The UTOPIA transmit cell available (TCA) signal provides status indication of when cell space is available in the transmit FIFO. TCA is used to poll the channel FIFOs to determine the number of free ATM cell buffers that are in the FIFO. When TCA is high, the channel FIFO can accept at least one more ATM cell. When TCA is low, the channel FIFO fill level exceeds a specified threshold. Note that regardless of the threshold, a channel FIFO can store 4 ATM cells. For Level 3 operation, the address sampled on TADR[3:0] will cause TCA to be updated with the channel information on the following clock cycle. For Level 2 operation, the address sampled on TADR[4:0] will cause TCA to be immediately updated with the channel information. TCA is updated on the rising edge of TFCLK.
PTPA			The POS-PHY polled transmit packet available (PTPA) signal provides status indication of when cell space is available in the transmit FIFO. The TADR address is used to determine which channel to report on PTPA. When PTPA transitions high, it indicates that the transmit FIFO has enough room to store a configurable number of data bytes. When PTPA transitions low, it indicates that the transmit FIFO is either full or near full. For Level 3 operation, the PTPA output is updated on the following clock cycle based on the FIFO fill level. For Level 2 operation, the PTPA output is updated immediately based on the FIFO fill level. PTPA is updated on the rising edge of TFCLK.

9.17 Receive System Side Interface

Pin Name	Type	Pin No.	Function
RFCLK	Input	AL34	The UTOPIA receive FIFO read clock (RFCLK). is used to read ATM cells from the cell receive FIFO. In UTOPIA Level 3 operation, RFCLK must cycle at a 104 MHz to 60 MHz instantaneous rate, and must be a free running clock (cannot be gapped). In UTOPIA Level 2 operation, RFCLK must cycle at a 52 MHz to 30 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
			The POS-PHY receive FIFO read clock (RFCLK). is used to read packet data from the packet FIFO. In POS-PHY Level 3 operation, RFCLK must cycle at a 104 MHz to 60 MHz instantaneous rate, and must be a free running clock (cannot be gapped). In POS-PHY operation, RFCLK must cycle at a 52 MHz to 30 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15] RDAT[16] RDAT[17] RDAT[18] RDAT[19] RDAT[20] RDAT[21] RDAT[22] RDAT[23] RDAT[24] RDAT[25] RDAT[26] RDAT[27] RDAT[28] RDAT[29] RDAT[30] RDAT[31]	Output	AF31 AF32 AF33 AF34 AE30 AE31 AE32 AE33 AE34 AD31 AD32 AD33 AD34 AC33 AC34 AB33 AB34 AA30 AA31 AA32 AA33 AA34 Y31 Y32 Y33 Y34 W30 W31 W32 W33 W34 V32	The UTOPIA receive cell data (RDAT[31:0]) bus carries the ATM cell octets that are read from the receive FIFO. In UTOPIA Level 3 operation, RDAT[31:0] is updated on the following clock cycle after RENB is sampled low. In UTOPIA Level 2 operation, RDAT[15:0] is updated on the following clock cycle after RENB is sampled low. RDAT[31:15] is ignored. RDAT[31:0] is updated on the rising edge of RFCLK.
			The POS-PHY receive packet data (RDAT[31:0]) bus carries the POS packet octets that are read from the receive FIFO. In POS-PHY Level 3 operation, the packet data on RDAT[31:0] is updated on the following clock cycle when RENB is sampled low. RDAT[31] is the first bit received and RDAT[0] is the last bit received. For general POS-PHY Level 3 operation, the value on RDAT[7:0] is also used to report the PHY channel when RSX is high. For POS-PHY Level 2 operation, the RDAT[15:0] bus is updated on the following clock cycle when RENB is sampled low. RDAT[31:0] is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RPRTY	Output	AF30	The UTOPIA receive parity (RPRTY) signal indicates the parity of the RDAT bus. Odd or even parity may be selected using software control. The value on RPRTY is updated on the following clock cycle when RENB is sampled low. For UTOPIA Level 3 operation, RPRTY is calculated over RDAT[31:0]. For UTOPIA Level 2 operation, RPRTY is calculated over RDAT[15:0]. RPRTY is updated on the rising edge of RFCLK.
			The POS-PHY receive parity (RPRTY) indicates the parity of the RDAT[31:0] bus. Odd or even parity may be selected using software control. The value on RPRTY is updated on the next clock cycle when RENB is sampled low. For POS-PHY Level 3 operation, RPRTY is calculated over RDAT[31:0]. For POS-PHY Level 2 operation, RPRTY is calculated over RDAT[15:0]. RPRTY is updated on the rising edge of RFCLK.
RENB	Input	AK34	The UTOPIA receive read enable (RENB) is used to initiate reads from the receive FIFO. The system may de-assert RENB if it is unable to accept more cells. In UTOPIA operation, when RENB is sampled low, RDAT, RRPTY and RSOC are updated on the following RFCLK cycle. When RENB is sampled high, the information on RDAT, RPRTY and RSOC_RSOP is held on the next clock cycle. RENB is also used for selected the channel to read data. When RENB transitions from high to low, the channel address on RADR selects the channel to read from. RENB is sampled on the rising edge of RFCLK.
			The POS-PHY receive read enable (RENB) is used to initiate reads from the receive FIFO. During a data transfer, RVAL must be monitored since it will indicate if the data is valid. The system may de-assert RENB at any time if it is unable to accept more data. In POS-PHY operation, the information on RDAT, RPRTY, RSOP, REOP, RMOD, RERR, RVAL and RSX is held on the following clock cycle when RENB is sampled high. When RENB is sampled low, the values on RDAT, RPRTY, RSOP, REOP, RMOD, RERR, RVAL and RSX are valid and are updated on the following clock cycle. RENB is sampled on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RSOC	Output	AG34	The UTOPIA receive start of cell (RSOC) signal marks the start of a cell structure on the RDAT bus. In UTOPIA operation, the first word of the cell structure is present on the RDAT bus when RSOC is high. RSOC is updated on the following clock cycle when RENB is sampled low. RSOC is updated on the rising edge of RFCLK.
RSOP			The POS-PHY receive start of packet (RSOP) indicates the start of a packet on the RDAT bus. In POS-PHY operation, the first word of the packet is on the RDAT bus when RSOP is high. RSOP is updated on the following clock cycle when RENB is sampled low. RSOP is updated on the rising edge of RFCLK
REOP	Output	AG33	The POS-PHY receive end of packet (REOP) marks the end of packet on the RDAT bus. It is legal for RSOP to be high at the same time REOP is high to support small packets. REOP set high indicates the last word of the packet is on the RDAT bus. The RMOD bus indicates how many valid bytes of packet data are in the last word. It is legal for RSOP to be high at the same time as REOP is high in order to support small packets. The value on REOP is updated on the next clock cycle when RENB is sampled low. REOP is only used for POS-PHY operation and is updated on the rising edge of RFCLK.
RERR	Output	AG32	The POS-PHY receive error (RERR) indicates that the current packet is invalid due to an error such as invalid FCS, excessive length or received HDLC abort sequence. RERR is high when REOP is high marking the current packet as erred. RERR is low when REOP is low. The value on RERR is updated on the next clock rising edge when RENB is sampled low. RERR is only used for POS-PHY operation and is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RMOD[0] RMOD[1]	Output	AG31 AH34	The POS-PHY receive modulo (RMOD) indicates the number of valid bytes of data on RDAT bus during POS-PHY operation. For POS-PHY Level 3 operation, the value on the RMOD[1:0] bus when REOP is high specifies the number of valid bytes of packet data on RDAT[31:0]. RMOD is set to "00" when REOP is low. "00" RDAT[31:0] valid "01" RDAT[31:8] valid "10" RDAT[31:16] valid "11" RDAT[31:24] valid For POS-PHY Level 2 operation, the value RMOD[0] when REOP is high specifies the number of valid bytes of packet data on RDAT[15:0]. When RMOD[0] is low, RDAT[15:0] is valid. When RMOD[0] is high, RDAT[15:8] is valid. RMOD[1] must be ignored in Level 2 operation. The value on RMOD[1:0] is updated on the next clock rising edge when RENB is sampled low. RMOD[1:0] is only used for POS-PHY operation and is updated on the rising edge of RFCLK.
RSX	Output	AH33	The POS-PHY receive start of transfer (RSX) indicates when the in-band port address is present on the RDAT[31:0] bus during POS-PHY Level 3 operation. When RSX is high, the value on RDAT[7:0] is the address of the receive PHY channel being selected. Subsequent data transfers on the RDAT[31:0] bus will read the channel FIFO buffer specified by this in-band address. The value on RSX is updated on the next clock rising edge when RENB is sampled low. RSX is only used for POS-PHY operation and is updated on the rising edge of RFCLK.
RADR[0] RADR[1] RADR[2] RADR[3] RADR[4]	Input	AJ34 AH30 AJ33 AJ32 AJ31	The UTOPIA receive port address select (RADR[4:0]) is used to select the channel whose FIFO fill status is to be polled or the channel for which a UTOPIA cell transfer is desired. For Level 3 operation, RENB transitions from high to low, the value sampled on RADR[3:0] selects the channel FIFO that the ATM cell is read from. During all other conditions, the fill status of the channel FIFO with the address sampled on RADR[4:0] is reported on RCA on the following clock cycle. For Level 2 operation, RENB transitions from high to low, the value sampled on RADR[4:0] selects the channel FIFO that the ATM cell is read from. During all other conditions, the fill status of the channel FIFO with the address sampled on RADR[4:0] is immediately reported on RCA. RADR[4:0] is sampled on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RCA	Output	AH31	The UTOPIA Level 3 receive cell available (RCA) is used to determine the fill status of each channel FIFO during UTOPIA Level 3 operation. RCA is used to poll the channel FIFOs to determine the number of ATM cells that are in the FIFO. The address sampled on RADR[3:0] will cause RCA to be updated with the channel information on the following clock cycle. When RCA is set high, the channel FIFO has at least one complete ATM cell. When RCA is set low, the channel FIFO does not contain a complete ATM cell. RCA is updated on the rising edge of RFCLK.
RVAL			The POS-PHY receive data valid (RVAL) signal indicates when the POS-PHY bus is valid during POS-PHY. In Level 3 operation, when RVAL is high and RENB is low, the values on RDAT, RPRTY, RSOP, REOP, RERR and RMOD are valid. When RVAL is low, the values on RDAT, RPRTY, RSOP, REOP, RERR and RMOD are invalid and must be ignored. In Level 2 operation, RVAL will transition low on a FIFO empty condition or on an end of packet. Once de-asserted, RVAL will remain low until RENB is de-asserted. No data will be removed from the receive FIFO while RVAL is held low. The value on RVAL is updated on the next clock rising edge when RENB is sampled low. RVAL is updated on the rising edge of RFCLK.
RCA	Output	AH32	The UTOPIA Level 2 receive cell available (RCA) is used to determine the fill status of each channel FIFO during UTOPIA Level 2 operation. RCA is used to poll the channel FIFOs to determine the number of ATM cells that are in the FIFO. The address sampled on RADR[3:0] will cause RCA to be updated with the channel information on the following clock cycle. When RCA is set high, the channel FIFO has at least one complete ATM cell. When RCA is set low, the channel FIFO does not contain a complete ATM cell. RCA is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RPA			The POS-PHY receive packet available (RPA) provides a direct status indication of when a programmable number of bytes of data is available in the receive FIFO. In POS-PHY Level 3 operation, RPA is ignored as the RVAL signal identifies valid data on the RDAT[7:0] bus. In POS-PHY Level 2 operation, the receive FIFO has at least one end of packet or a programmable minimum number of bytes to be read when RPA is high. RPA is otherwise low. The RPA may incorrectly indicate the FIFO fill level is above the high water mark after an end of packet is transferred over RDAT[15:0]. See the Functional Timing section for more details of using RVAL with RPA to prevent data corruption. RPA is updated on the rising edge of RFCLK.

9.18 Microprocessor Interface Signals

Pin Name	Type	Pin No.	Function
CSB	Input	R3	Active-Low Chip Select (CSB). The CSB signal is low during S/UNI-12xJET register accesses. When CSB is high, the RDB and WRB inputs are ignored. When CSB is low, the RDB and WRB are valid. CSB must be high when RSTB is low to properly reset the chip. If CSB is not required (i.e., registers accesses are controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
WRB	Input	R4	Active-Low Write Strobe (WRB). The WRB signal is low during S/UNI-12xJET register write accesses. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
RDB	Input	P1	Active-Low Read Enable (RDB). The RDB signal is low during S/UNI-12xJET register read accesses. The S/UNI-12xJET drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7] D[8] D[9] D[10] D[11] D[12] D[13] D[14] D[15]	I/O	P2 P3 P4 P5 N1 N2 M1 M2 L1 L2 L3 L4 K1 K2 K3 K4	Bi-Directional Data Bus (D[15:0]). The D[15:0] bus is used during S/UNI-12xJET register read and write accesses.

Pin Name	Type	Pin No.	Function
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10] A[11] A[12] A[13]	Input	K5 J1 J2 J3 J4 J5 H1 H2 H3 H4 G1 G2 G3 G4	Address Bus (A[13:0]). The address bus A[13:0] selects specific registers during S/UNI-12xJET register accesses.
A[14]	Input	F1	Test Register Select (A[14]). The test register select (A[14]) signal selects between normal and test mode register accesses. A[14] is high during test mode register accesses and is low during normal mode register accesses.
RSTB	Input	G5	Active-Low Reset Signal (RSTB). The RSTB signal provides an asynchronous S/UNI-12xJET reset. RSTB is a Schmitt triggered input with an integral pull-up resistor. CSB must be held high when RSTB is low in order to properly reset this chip.
ALE	Input	F2	Address Latch Enable (ALE). The ALE is active-high and latches the address bus A[14:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-12xJET to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	Output	F3	Active-Low Interrupt Signal (INTB). The INTB signal is set low when a S/UNI-12xJET interrupt source is active and that source is unmasked. The S/UNI-12xJET may be enabled to report many alarms or events via interrupts. Examples of interrupt sources are loss of signal (LOS), loss of frame (LOF), line AIS, line remote defect indication (LRDI) detect, loss of pointer (LOP), path AIS, path remote defect indication and others. INTB is tri-stated when all the enabled interrupt sources are acknowledged via an appropriate register access. INTB is an open drain output.

9.19 JTAG Interface Signals

Pin Name	Type	Pin No.	Function
TCK	Input	C1	Test Clock (TCK). The TCK signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	E1	Test Mode Select (TMS). The TMS signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	D1	Test Data Input (TDI). The TDI signal carries test data into the S/UNI-12xJET via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Output	F4	Test Data Output (TDO). The TDO signal carries test data out of the S/UNI-12xJET via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output, which is inactive except when shifting boundary scan data is in progress.
TRSTB	Input	D3	Active Low Test Reset (TRSTB). The TRSTB signal provides an asynchronous S/UNI-12xJET test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. Note that when not being used, TRSTB must be tied low or connected to the RSTB input.

9.20 Power and Ground

Pin Name	Type	Pin No.	Function
ATB[1] ATB[2]	Analog	AP32 AM31	The receive and transmit analog test ports (ATB[1:0]). These pins are used for manufacturing testing only and should be tied to the analog ground plane (AVS).
AVD1 AVD2	Analog Power	AP30 AM29	The analog power (AVD[3:0]) pins for the analog core. The AVD pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.

Pin Name	Type	Pin No.	Function
AVS1 AVS2	Analog Power	AP31 AL29	The analog ground (AVS[3:0]) pins for the analog core. The AVS pins should be connected to the analog ground of the analog power supply. Please see the Operation section for detailed information.
VDDI	Digital Power		The core digital power (VDDI) pins should be connected to a well-decoupled +1.8 V digital power supply. Pin No. E27, E24, E20, E15, E8, H30, H5, L30, L5, R30, R5, Y30, Y5, AD30, AD5, AG30, AG5, AK27, AK24, AK20, AK15, AK11, AK8
VDD	Digital Power		The I/O digital power (VDD) pins should be connected to a well-decoupled +3.3 V digital power supply. Pin No. B31, B30, B5, B4, C30, C22, C13, C5, D33, D30, D22, D13, D5, D2, E33, E32, E31, E29, E22, E13, E6, E4, E3, E2, F30, F5, N32, N31, N30, N5, N4, N3, AB32, AB31, AB30, AB5, AB4, AB3, AJ30, AJ5, AK33, AK32, AK31, AK29, AK22, AK13, AK6, AK4, AK3, AK2, AL33, AL30, AL22, AL13, AL5, AL2, AM30, AM22, AM13, AM5, AN31, AN30, AN5, AN4
VSS	Digital Power		The I/O digital ground (VSS) pins should be connected to the digital ground of the digital power supply. Pin No. A34, A1, B33, B2, C32, C23, C12, C3, D31, D23, D18, D17, D12, D4, E30, E23, E18, E17, E12, E5, M32, M31, M30, M5, M4, M3, U31, U30, U5, U4, V31, V30, V5, V4, AC32, AC31, AC30, AC5, AC4, AC3, AK30, AK23, AK18, AK17, AK12, AK5, AL31, AL23, AL18, AL17, AL12, AL4, AM32, AM23, AM12, AM3, AN33, AN2, AP34, AP1
NC	No Connect		The No Connect (NC) pins are unused and do not need to be connected Pin No. B1, B34, C2, AM33, AN32, AN34, AP2, AP33

Notes on Pin Description:

1. All digital inputs and bi-directional signals present minimum capacitive loading and operate at TTL logic levels except the inputs marked as Analog.
2. All digital outputs and bi-directional signals have 8mA drive strength.
3. It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.
4. It is mandatory that every digital power pin (VDDI and VDD sets) be connected to printed circuit board power planes to ensure reliable device operation.
5. All analog power and ground pins can be sensitive to noise. They must be isolated from the digital power and ground. Care must be taken to correctly decouple these pins. Please refer to section 17 Power Information for more information.

6. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in section 17 Power Information.

10 Functional Description

10.1 Receive Regenerator and Multiplexer Processor (RRMP)

The Receive Regenerator and Multiplexer Processor (RRMP) block extracts and processes the transport overhead of the received data stream.

The RRMP frames to the data stream by operating with an upstream pattern detector (external SERDES) that searches for occurrences of the A1/A2 framing pattern and generates the FPIN signal. Once the SRLI has found an A1/A2 framing pattern, the RRMP monitors for the next occurrence of the framing pattern 125µs later. Two framing pattern algorithms are provided to improve performance in the presence of bit errors. In algorithm 1, the RRMP declares frame alignment (removes OOF defect) when 12 A1 and 12 A2 bytes are seen error-free. In algorithm 2, the RRMP declares frame alignment (removes OOF defect) when one A1 byte and the first four bits of one A2 byte are seen error-free. Once in frame, the RRMP monitors the framing pattern and declares OOF when one or more bit errors in the framing pattern are detected for four consecutive frames. Again, depending upon the algorithm, either 24 framing bytes or 12 framing bits are examined for bit errors in the framing pattern.

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment, the performance of each algorithm is dominated by the alignment algorithm used in the SRLI, which always examines 3 A1 and 3 A2 framing bytes. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the RRMP continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 1.3 seconds and the second algorithm provides a 99.75% probability that the mean time between OOF occurrences is 7 minutes.

The RRMP also detects loss of frame (LOF) defect and loss of signal (LOS) defect. LOF is declared when an out of frame (OOF) condition exists for a total period of 3ms during which there is no continuous in frame period of 3 ms. LOF is removed when an in frame condition exists for a continuous period of 3 ms. LOS is declared when a continuous period of 20 µs without transitions on the received data stream is detected. LOS is removed when two consecutive framing patterns are found (based on algorithm 1 or algorithm 2) and during the intervening time (one frame), there are no continuous periods of 20 µs without transitions on the received data stream.

The RRMP calculates the section BIP-8 error detection code on the scrambled data of the complete frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of STS-1 (STM-0) #1 of the following frame after descrambling. Any difference indicates a section BIP-8 error. The RRMP accumulates section BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block section BIP-8 errors can be accumulated.

The RRMP optionally descrambles the received data stream.

The RRMP calculates the line BIP-8 error detection codes on the de-scrambled line overhead and synchronous payload envelope bytes of the constituent STS-1 (STM-0). The line BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B2 byte of the constituent STS-1 (STM-0) of the following frame after descrambling. Any difference indicates a line BIP-8 error. The RRMP accumulates line BIP-8 errors in a microprocessor readable 24 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-24 errors can be accumulated.

The RRMP extracts the line remote error indication (REI-L) errors from the M1 byte of STS-1 (STM-0) #3 and accumulates them in a microprocessor readable 24 bits saturating counter (up to 1 second accumulation time). Optionally, block line REI errors can be accumulated.

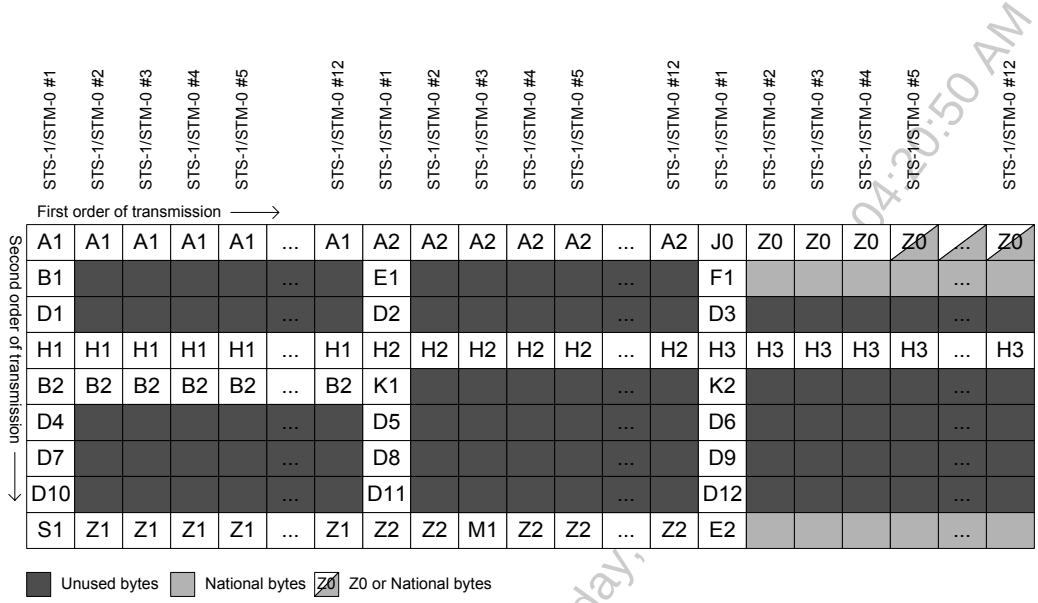
The RRMP extracts and filters the K1/K2 APS bytes for three frames. The filtered K1/K2 APS bytes are accessible through microprocessor readable registers. The RRMP also monitors the unfiltered K1/K2 APS bytes to detect APS byte failure (APSBF-L) defect, line alarm indication signal (AIS-L) defect and line remote defect indication (RDI-L) defect. APS byte failure is declared when twelve consecutive frames have been received where no three consecutive frames contain identical K1 bytes. The APS byte failure is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the K1/K2 APS register. Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The RRMP extracts and filters the synchronization status message (SSM) for eight frames. The filtered SSM is accessible through microprocessor readable registers.

RRMP optionally inserts line alarm indication signal (AIS-L).

The RRMP extracts and serially outputs all the transport overhead (TOH) bytes on the RTOH port. The TOH bytes are output in the same order that they are received (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). ROHCLK is the generated output clock used to provide timing for the RTOH port. ROHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling ROHFP high with the rising edge of ROHCLK identifies the MSB of the first A1 byte.

Figure 13 STS-12 (STM-4) on RTOH



The RRMP optionally serially outputs the line DCC bytes on the RSLD port. RSLD is selectable to output either the section DCC bytes (D4-D12) or the line DCC bytes (D1-D3). RSLDCLK is the generated output clock used to provide timing for the RSLD port. If RSLD carries the line DCC, RSLDCLK is a nominal 576 kHz clock or if RSLD carries the section DCC, RSLDCLK is a nominal 192 kHz clock. Sampling ROHFP high identifies the MSB of the first DCC byte on RSLD (D1 or D4).

A maskable interrupt is activated to indicate any change in the status of out of frame (OOF), loss of frame (LOF), loss of signal (LOS), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), synchronization status message (COSSM), APS bytes (COAPS) and APS byte failure (APSBF) or any errors in section BIP-8, line BIP-8 and line remote error indication (REI-L).

The RRMP block provides de-scrambled data and frame alignment indication signals for use by the RHPP.

10.2 Receive Trail Trace Processor (RTTP)

The Receive Trail trace Processor (RTTP) block monitors the trail trace messages of the receive data stream for trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect. Three trail trace algorithms are defined.

The first algorithm is BELLCORE compliant. The algorithm detects trace identifier mismatch (TIM) defect on a 16 or 64 byte trail trace message. A TIM defect is declared when none of the last 20 messages matches the expected message. A TIM defect is removed when 16 of the last 20 messages match the expected message. The expected trail trace message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the expected message is matched when the trail trace message is all zeros.

The second algorithm is ITU compliant. The algorithm detects trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect on a 16 or 64 byte trail trace message. The current trail trace message is stored in the captured page of the RTTP. If the length of the message is 16 bytes, the RTTP synchronizes on the MSB of the message. The byte with the MSB set high is placed in the first location of the captured page. If the length of the message is 64 bytes, the RTTP synchronizes on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the message. The following byte is placed in the first location of the captured page.

A persistent trail trace message is declared when an identical message is receive for 3 or 5 consecutive multi-frames (16 or 64 frames). A persistent message becomes the accepted message. The accepted message is stored in the accepted page of the RTTP. A TIU defect is declared when one or more erroneous bytes are detected in a total of 8 messages without any persistent message in between. A TIU defect is removed when a persistent message is received.

A TIM defect is declared when the accepted message does not match the expected message. A TIM defect is removed when the accepted message matches the expected message. The expected message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the algorithm declares a match trail trace message when the accepted message is all zeros.

The third algorithm is not BELLCORE/ITU compliant. The algorithm detects trace identifier unstable (TIU) on a single continuous trail trace byte. A TIU defect is declared when one or more erroneous bytes are detected in three consecutive 16 byte windows. The first window starts on the first erroneous byte. A TIU defect is removed when an identical byte is received for 48 consecutive frames. A maskable interrupt is activated to indicate any change in the status of trace identifier unstable (TIU) and trace identifier mismatch (TIM).

10.3 Receive High Order Path Processor (RHPP)

The Receive High Order Path Processor (RHPP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (virtual container), and path level alarm and performance monitoring.

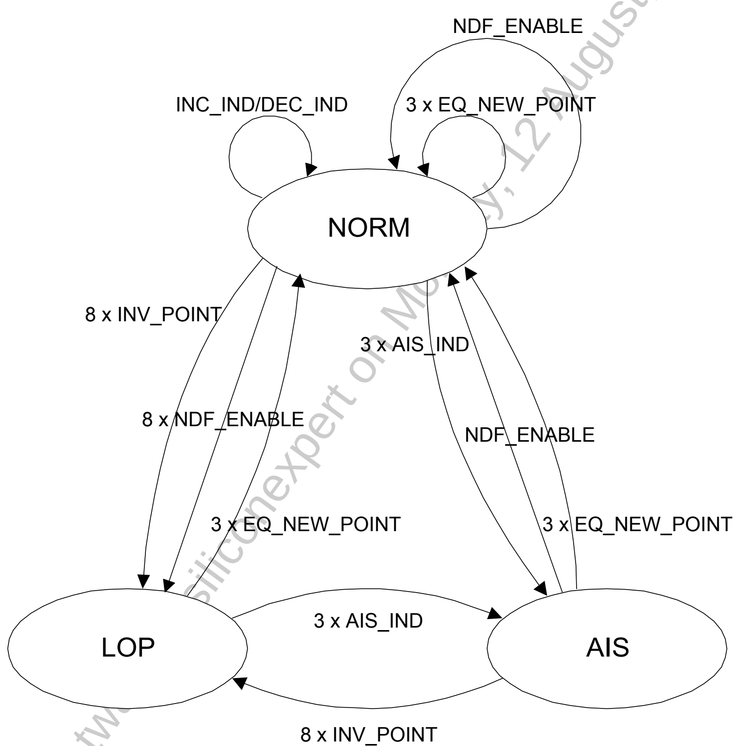
10.3.1 Pointer Interpreter

The pointer interpreter extracts and validates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the synchronous payload envelop bytes (SPE) of the constituent STS-1/3c/12c (VC3/4/4-4c) payloads. The pointer interpreter is a time multiplexed finite state machine that can process any mixed of STS-1/3c/12c (AU3/4/4-4c) pointers. Within the pointer interpretation algorithm three states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)
- LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, non-consecutively received indications do not activate the transitions between states.

Figure 14 Pointer Interpretation State Diagram



The following events (indications) are defined:

NORM_POINT: disabled NDF + ss + offset value equal to active offset.

NDF_ENABLE: enabled NDF + ss + offset value in range of 0 to 782.

AIS_IND: H1 = FFh + H2 = FFh.

INC_IND: disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.

DEC_IND: disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.

INV_POINT: not any of the above (i.e.: not NORM_POINT, not NDF_ENABLE, not AIS_IND, not INC_IND and not DEC_IND).

NEW_POINT: disabled NDF + ss + offset value in range of 0 to 782 but not equal to active offset.

Notes on event (indication) definitions:

1. Active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.

2. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.

3. Disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100 and 0111.

4. The remaining six NDF bit patterns (0000, 0011, 0101, 1010, 1100, 1111) result in an INV_POINT indication.

5. ss bits are unspecified in SONET and have bit pattern 10 in SDH.

6. The use of ss bits in definition of indications may be optionally disabled.

7. The requirement for previous NDF_ENABLE, INC_IND or DEC_IND be more than 3 frames ago may be optionally disabled.

8. NEW_POINT is also an INV_POINT.

9. The requirement for the pointer to be within the range of 0 to 782 in 8 X NDF_ENABLE may be optionally disabled.

10. LOP is not declared if all the following conditions exist:
    - The received pointer is out of range (>782)
    - The received pointer is static
    - The received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification
    - When the received pointer returns to an in-range value, the S/UNI-12xJET will interpret it correctly.

The transitions indicated in the state diagram are defined as follows:

INC_IND/DEC_IND: offset adjustment (increment or decrement indication)

3 x EQ_NEW_POINT: three consecutive equal NEW_POINT indications

NDF_ENABLE:	single NDF_ENABLE indication
3 x AIS_IND:	three consecutive AIS indications
8 x INV_POINT:	eight consecutive INV_POINT indications
8 x NDF_ENABLE	eight consecutive NDF_ENABLE indications

Notes on transitions indicated in state diagram:

1. The transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.
2. 3 x EQ_NEW_POINT takes precedence over other events and may optionally reset the INV_POINT count.
3. All three offset values received in 3 x EQ_NEW_POINT must be identical.
4. "Consecutive event counters" are reset to zero on a change of state (except the INV_POINT counter).

LOP is declared on entry to the LOP_state after eight consecutive invalid pointers or eight consecutive NDF enabled indications. Path AIS is optionally inserted in the DROP BUS when LOP is declared. The alarm condition is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local S/UNI-12XJET to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in the DROP bus G1 byte is set to indicate the LOP alarm to the THPP in a remote S/UNI-12XJET.

PAIS is declared on entry to the AIS_state after three consecutive AIS indications. Path AIS is inserted in the DROP bus when AIS is declared. The alarm condition is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local S/UNI-12XJET to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in the DROP bus G1 byte is set to indicate the PAIS alarm to the THPP in a remote S/UNI-12XJET.

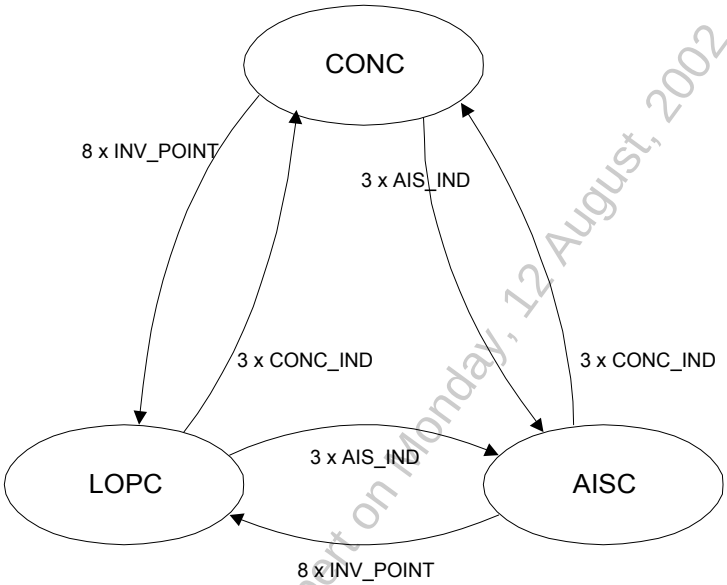
10.3.2 Concatenation Pointer Interpreter State Machine

The concatenation pointer interpreter extracts and validates the H1 and H2 concatenation bytes. The concatenation pointer interpreter is a time multiplexed finite state machine that can process any mixed of STS-1/3c/12c (AU3/4/4-4c) pointers. Within the pointer interpretation algorithm three states are defined as shown below.

- CONC_state (CONC)
- AISC_state (AISC)
- LOPC_state (LOPC)

The transitions between the states will be consecutive events (indications), e.g. three consecutive AIS indications to go from the CONC_state to the AISC_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER.

Figure 15 Concatenation Pointer Interpretation State Diagram



The following events (indications) are defined:

- CONC_IND: enabled NDF + dd + "1111111111"
- AIS_IND: H1 = FFh + H2 = FFh
- INV_POINT: not any of the above (i.e.: not CONC_IND and not AIS_IND)

Notes on event (indications) definitions:

1. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.
2. The remaining eleven NDF bit patterns (0000, 0010, 0011, 0100, 0101, 0110, 0111, 1010, 1100, 1110, 1111) result in an INV_POINT indication.
3. dd bits are unspecified in SONET/SDH.

The transitions indicated in the state diagram are defined as follows:

- 3 X CONC_IND: three consecutive CONC indications
- 3 x AIS_IND: three consecutive AIS indications
- 8 x INV_POINT: eight consecutive INV_POINT indications

Notes on transitions indicated in state diagram:

1. "Consecutive event counters are reset to zero on a change of state.

LOPC is declared on entry to the LOPC_state after eight consecutive pointers with values other than concatenation indications. Path AIS is optionally inserted in the DROP bus when LOPC is declared. The alarm condition is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local S/UNI-12XJET to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in the DROP bus G1 byte is set to indicate the LOP alarm to the THPP in a remote S/UNI-12XJET.

PAISC is declared on entry to the AISC_state after three consecutive AIS indications. Path AIS is optionally inserted in the DROP bus when AISC is declared. The alarm condition is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local S/UNI-12XJET to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in the DROP bus G1 byte is set to indicate the PAIS alarm to the THPP in a remote S/UNI-12xJET.

10.3.3 Error Monitoring

The RHPP calculates the path BIP-8 error detection codes on the STS-1/3c/12c (VC-3/4/4-4c) payloads. When processing a VC-3 payload, the two fixed stuff columns can be excluded from the BIP-8 calculation if the FSBIPDIS register bit is set. The path BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B3 byte of each constituent STS (VC) payload of the following frame. Any differences indicate a path BIP-8 error. The RHPP accumulates path BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-8 errors can be accumulated.

The RHPP extracts the path remote error indication (REI-P) errors from bits 1, 2, 3 and 4 of the path status byte (G1) and accumulates them in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block REI errors can be accumulated.

The RHPP monitors the path signal label byte (C2) payload to validate change in the accepted path signal label (APSL). The same PSL byte must be received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register) before being considered accepted.

The RHPP also monitors the path signal label byte (C2) to detect path payload label unstable (PLU-P) defect. A PSL unstable counter is increment every time the received PSL differs from the previously received PSL (an erroneous PSL will cause the counter to be increment twice, once when the erroneous PSL is received and once when the error free PSL is received). The PSL unstable counter is reset when the same PSL value is received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). PLU-P is declared when the PSL unstable counter reaches five. PLU-P is removed when the PSL unstable counter is reset.

The RHPP also monitors the path signal label byte (C2) to detect path payload label mismatch (PLM-P) defect. PLM-P is declared when the accepted PSL does not match the expected PSL according to Table 2. PLM-P is removed when the accepted PSL match the expected PSL according to Table 2. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path unequipped (UNEQ-P) defect. UNEQ-P is declared when the accepted PSL is 00H and the expected PSL is not 00H. UNEQ-P is removed when the accepted PSL is not 00H or when the accepted PSL is 00H and the expected PSL is 00H. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a register programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path payload defect indication (PDI-P) defect. PDI-P is declared when the accepted PSL is a PDI defect that matches the expected PDI defect. PPDI is removed when the accepted PSL is not a PDI defect or when the accepted PSL is a PDI defect that does not match the expected PDI defect. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). Table 3 gives the expected PDI defect based on the programmable PDI and PDI range register values.

Table 2 PLM-P, UNEQ-P and PDI-P Defects Declaration

Expected PSL		Accepted PSL			PLM-P	UNEQ-P	PDI-P
00	Unequipped	00	Unequipped		Match	Inactive	Inactive
		01	Equipped non specific		Mismatch	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Mismatch	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive
01	Equipped non specific	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Match	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	$=_{exp}$PDI	Match	Inactive
				$!=_{exp}$PDI	$!=_{exp}$PDI	Mismatch	Inactive
02 - FF	Equipped specific PDI	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific	$=_{exp}$PSL	Match	Inactive	Inactive
				$!=_{exp}$PSL	Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Match	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive

Table 3 Expected PDI Defect Based on PDI and PDI Range Values

PDI register value	DPI range register value	Expected PDI	PDI register value	DPI range register value	Expected PDI
00000	Disable	None	01111	Disable	EF
	Enable			Enable	E1-EF
00001	Disable	E1	10000	Disable	F0
	Enable	E1-E1		Enable	E1-F0
00010	Disable	E2	10001	Disable	F1
	Enable	E1-E2		Enable	E1-F1
00011	Disable	E3	10010	Disable	F2
	Enable	E1-E3		Enable	E1-F2
00100	Disable	E4	10011	Disable	F3
	Enable	E1-E4		Enable	E1-F3
00101	Disable	E5	10100	Disable	F4
	Enable	E1-E5		Enable	E1-F4
00110	Disable	E6	10101	Disable	F5
	Enable	E1-E6		Enable	E1-F5
00111	Disable	E7	10110	Disable	F6
	Enable	E1-E7		Enable	E1-F6
01000	Disable	E8	10111	Disable	F7
	Enable	E1-E8		Enable	E1-F7
01001	Disable	E9	11000	Disable	F8
	Enable	E1-E9		Enable	E1-F8
01010	Disable	EA	11001	Disable	F9
	Enable	E1-EA		Enable	E1-F9
01011	Disable	EB	11010	Disable	FA
	Enable	E1-EB		Enable	E1-FA
01100	Disable	EC	11011	Disable	FB
	Enable	E1-EC		Enable	E1-FB
01101	Disable	ED	11100	Disable	FC
	Enable	E1-ED		Enable	E1-FC
01110	Disable	EE			
	Enable	E1-EE			

The RHPP monitors bits 5, 6 and 7 of the path status byte (G1) to detect to detect path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) defects.

RDI-P is declared when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). RDI-P is removed when bit 5 of the G1 byte is set low for five or ten consecutive frames. ERDI-P is declared when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). ERDI-P is removed when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

The RHPP extracts and serially outputs all the path overhead (POH) bytes on the time multiplexed RPOH port. The POH bytes are output in the same order that they are received (J1, B3, C2, G1, F2, H4, Z3, Z4 and N1). ROHCLK is the generated output clock used to provide timing for the RPOH port. ROHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling ROHFP high with the rising edge of ROHCLK identifies the MSB of the first J1 byte.

10.4 SONET/SDH Bit Error Rate Monitor (SBER)

The SBER block provides two independent bit error rate-monitoring circuits (BERM block). The SBER block is used to monitor the Multiplexer Section BIP (B2) with one BERM block dedicated to monitor the Signal Degrade (SD) alarm and the other BERM block dedicated to monitor the Signal Fail (SF) alarm. These alarms can then be used to control system level features such as Automatic Protection Switching (APS).

The BERM block utilizes a sliding window based algorithm.

10.5 SONET/SDH Alarm Reporting Controller (SARC)

The SARC block receives all the section, line, and path defects detected by the receive overhead processors and, according to user specific configuration, generates consequent action indications.

- Receive section alarm (SALM) indication: SALM is asserted when an OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.
-
- Receive path alarm (RALM) indication: RALM is asserted when a SALM, , AIS-P, LOP-P, PLU-P, PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.

10.6 Receive Time Slot Interchange (RX STI)

The RX_STI determines which STS-1 Timeslots are to be provisioned for a particular channel. An incoming DROP bus is provided to the RX_STI. The RX_STI will remove data from the DROP bus and provide it to the channel data processors. In addition, the RX_STI allows unique STS configurations (with a granularity of STS-1 or STS-3) for virtual concatenation using external SONET path processors.

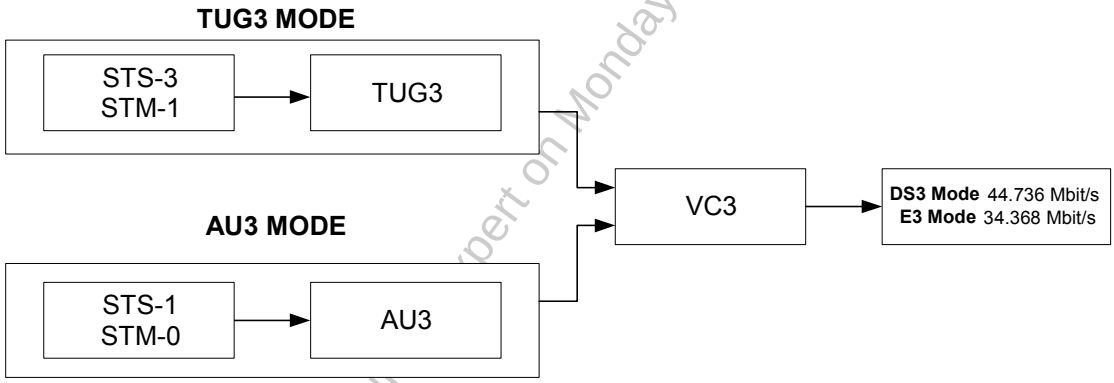
- The RX_STI is not a complete Time Slot Interchange in that it does not re-order timeslots; however, the RX_STI does allow any channel to receive data on any of the timeslots in chronological order starting from the master timeslot.

10.7 DS3/E3 Desynchronizer (D3E3MD)

The D3E3MD block extracts DS3 or E3 data from an STS-1 / STM0 SPE and outputs a nominal rate DS3 or E3 clock and serial data stream.

The D3E3MD is capable of demapping DS3 / E3 payloads from SONET SPEs mapped as AU3s or TUG3s. The desired demapping mode of the incoming SPE is selected via the AU3TUG3B normal mode register bit. Thus, four possible demapping modes of operation are possible : (1) AU3 -> DS3, (2) AU3 -> E3, (3) TUG3 -> DS3, and TUG3 -> E3. The decomposition of the incoming SONET frame into DS3 / E3 data is depicted in Figure 16.

Figure 16 Demapping Structure



The locations of specific payload bytes within the incoming STS-1 frame, as well as negative and positive pointer justifications, are calculated. Positive and negative SPE and TU3 pointer justification events are registered as interrupts which are visible as normal mode register bits.

The D3E3MD decomposes the incoming STS-1 data stream into a VC3 structure. If the D3E3MD is in AU3 mode, the VC3 is demapped from the STS-1 payload by removing 2 fixed stuff columns. If the D3E3MD is in TUG3 mode, the VC3 is extracted from the STS-1 payload by removing 1 VC4 POH column, and a column that consists of H1, H2, H3, and fixed stuff bytes (see Figure 61).

In DS3 or E3 mode, the D3E3MD demaps the incoming DS3 or E3 payload from a VC-3. The DS3 or E3 payload is always demapped from a VC-3, regardless of whether the SPE has been mapped according to AU3 or TUG3 specifications. The format of the incoming DS3 over VC-3 mapping is shown in Figure 58. The format of the incoming E3 over VC-3 mapping is shown in Figure 59.

When SONET defects is detected or the AISGEN normal mode register bit is set high, the extracted DS3 / E3 payload is overwritten by an Alarm Indication Signal (AIS) and the outgoing clock is held constant at 44.736 MHz in DS3 mode and 34.368 MHz in E3 mode. The AIS pattern is described in section 13.15

10.7.1 FIFO

DS3 / E3 Data bits extracted from the STS-1 SPE are assembled into bytes and written into a 54 byte FIFO. The depth of the FIFO has been chosen to account for the DPLL loop bandwidth, worst case maximum consecutive pointer justifications in the same direction, ppm offsets between the read and write clocks, and payload gaps. In addition, with a 1Hz loop bandwidth the D3E3MD can also tolerate periodic pointer justifications in the same direction that are spaced 7.5 ms apart, as per the GR-253 2000 DS3 specifications.

The FIFO is used to monitor the phase error and aids in regulating the outgoing clock frequency. When an overflow or an underflow occur, the FIFO control block generates interrupt signals (FOVRI and FUDRI, respectively). A normal mode register bit is provided so that the FIFO may be reset by software (FIFORST).

10.7.2 Digital PLL

A Digital Phase Locked Loop (DPLL) is used to generate the output DS3/E3 clock. The DPLL consists of a phase detector, a phase modulator, and a clock generator. The default loop bandwidth of the DPLL has been selected to be approximately 1 Hz. A normal mode register bit (LOOPBW) exists which increases the loop bandwidth of the DPLL to approximately 64 Hz, if faster lock is required, at the expense of increased jitter. A second normal mode register bit LOOPBW2 reduces the default loop bandwidth from 1 Hz to 0.6 Hz, if greater jitter attenuation than that of the default loop bandwidth is desired. The PLLRST normal mode register bit provides an asynchronous reset for the DPLL circuits, if it is desired to reset the PLL without resetting the other logic in the D3E3MD.

10.7.3 Transfer Function

Jitter transfer is defined as the ratio of jitter on the output signal (serial DS3/E3) to the jitter applied to the input signal (DS3/E3 mapped into SONET). Requirements for jitter transfer are given in terms of a jitter transfer mask, which represents the maximum acceptable jitter gain (in dB) for a specified range of jitter frequencies.

Typical transfer function of the D3E3MD is depicted in Figure 17.

Figure 17 Typical D3E3MD Jitter Transfer Function

TBD

The system (including the D3E3MD) intrinsic jitter, pointer jitter, jitter tolerance, mapping wander, and pointer wander characteristics are described in section 19.11 DS3/E3 Serial Interface Timing Characteristics.

The D3E3MD may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the D3E3MD. Access to these registers is via a generic microprocessor bus.

10.8 DS3/E3 Jitter Attenuator (JAT)

The JAT receives serial data and clock from an external source, measures the phase difference between the DS3/E3 reference clock and the external received clock implementing a digital PLL that performs the jitter attenuating function.

10.8.1 Digital PLL

The digital PLL is composed of three sections: delay line, phase detector and control state machine.

To initialize the JAT, it takes a maximum 192 DS3/E3 reference clock (DS3_REFCLK or E3_REFCLK) cycles. When the initialization is complete, the state machine will set the RUN signal high indicating the outgoing data stream is reasonably stable.

This PLL performs the jitter attenuation of the incoming phase with a bandwidth set by the normal mode registers. The PLL supports a glitchless software reset function. Maximum reset time is 384 (DS3_REFCLK or E3_REFCLK) cycles.

10.8.2 FIFO

The FIFO acts as an elastic storage element, which receives data at a rate determined by the incoming clock and transmits this data at a rate determined by the outgoing clock. The FIFO is comprised of two banks of 128 registers, a write and read address pointer, overflow and underflow monitors, and optional centering circuitry.

When the internal PLL is providing the outgoing clock, the FIFO can be used as an elastic store to bridge between data burst and smooth data environments. The FIFO has a self-centering circuit, which sets up the read pointer operating range to be at least 8 UI away from the end of the 128 bit registers.

The self-centering circuit is active for 224 incoming clock cycles after an overrun event, an underrun event, or after the CENT option is enabled. While this circuit is active, if a fast incoming clock causes the read pointer to come within 8 UI of overflowing, the pointer is inhibited from incrementing. Conversely, if a fast outgoing clock causes the read pointer to come within 8 UI of underflowing, the pointer is inhibited from decrementing. After this circuit is disengaged, the read pointers can wander closer than 8 UI the end of the registers during peak phase shifts without corrupting data.

The LIMIT option can be enabled to force the PLL to pass through jitter un-attenuated when the FIFO is reading from the 1st bit or writing to the 128th bit of the registers. If the LIMIT option is enabled and the read address pointer comes within one UI of the end of the registers, the appropriate LIMIT flag will cause the PLL outputs outgoing clock to lead, if approaching overflow, or lag, if approaching underflow. This option prevents data from being lost during high phase shift conditions.

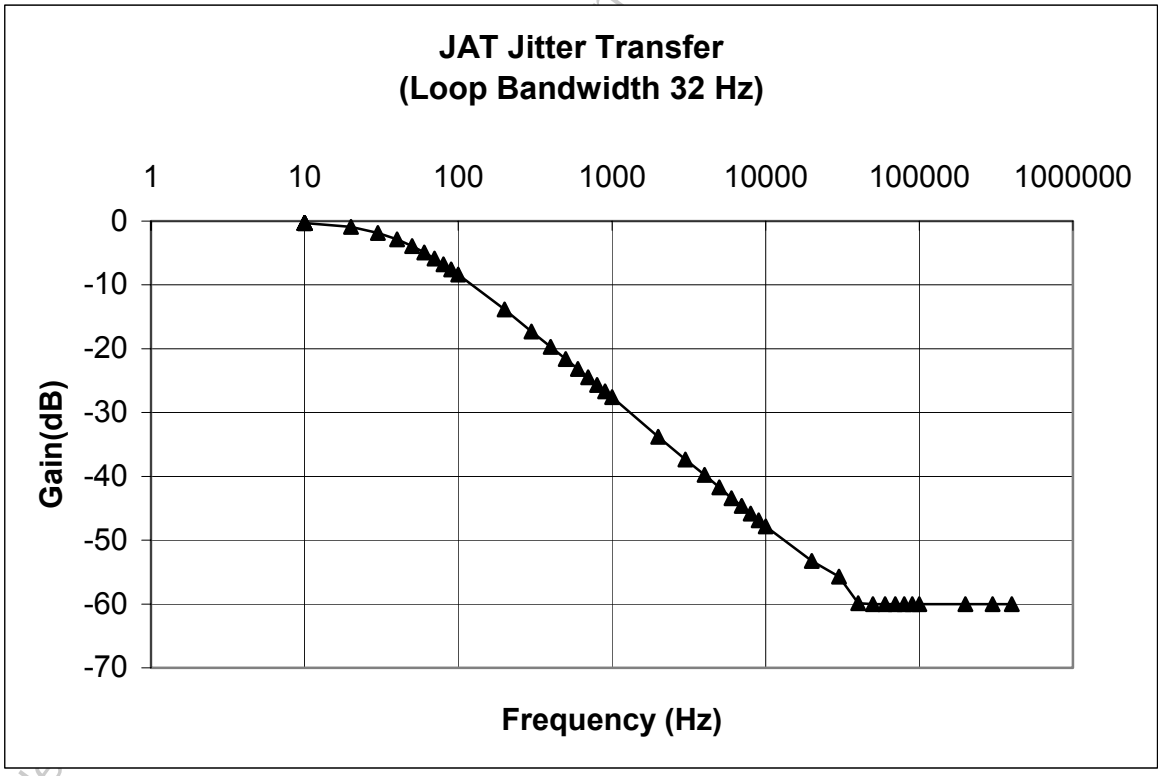
The SHIFT option can be enabled to force the PLL to auto-center the FIFO fill level. The FIFO peak fill and empty levels are measured periodically and the PLL is pushed in the direction such that the FIFO average fill level moves more centered in the FIFO. The rate that the FIFO peaks levels are measured is less than the PLL loop bandwidth to prevent jitter variations from affecting the control loop.

When an attempt is made to read data from the FIFO when the FIFO is already empty, the UNDRI register will be set. Similarly, when an attempt is made to write data to the FIFO when the FIFO is already full, the OVERI register will be set.

10.8.3 Transfer Function

Jitter transfer is defined as the ratio of jitter on the output signal to the jitter applied to the input signal. A typical transfer function of the JAT is depicted in Figure 18. Note that the JAT loop bandwidth selected is 32 Hz and the tester equipment used to measure the jitter transfer does not go beyond –60 dB.

Figure 18 Typical JAT Jitter Transfer Function



The system (including the TJAT and RJAT) intrinsic jitter, pointer jitter, jitter tolerance, mapping wander, and pointer wander characteristics are described in section 19.11 DS3/E3 Serial Interface Timing Characteristics.

The JAT may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the JAT. Access to these registers is via a generic microprocessor bus.

10.9 DS3 Framer

The DS3 Framer (T3-FRMR) Block integrates circuitry required for decoding a B3ZS-encoded signal and framing to the resulting DS3 bit stream. The T3-FRMR is directly compatible with the M23 and C-bit parity DS3 applications.

The T3-FRMR decodes a B3ZS-encoded signal and provides indications of line code violations. The B3ZS decoding algorithm and the LCV definition can be independently chosen through software. A loss of signal (LOS) defect is also detected for B3ZS encoded streams. LOS is declared when inputs RPOS and RNEG contain zeros for 175 consecutive RCLK cycles. LOS is removed when the ones density on RPOS and/or RNEG is greater than 33% for 175 ±1 RCLK cycles.

The framing algorithm examines five F-bit candidates simultaneously. When at least one discrepancy has occurred in each candidate, the algorithm examines the next set of five candidates. When a single F-bit candidate remains in a set, the first bit in the supposed M-subframe is examined for the M-frame alignment signal (i.e., the M-bits, M1, M2, and M3 are following the 010 pattern). Framing is declared, and out-of-frame is removed, if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. During the examination of the M-bits, the X-bits and P-bits are ignored. The algorithm gives a maximum average reframe time of 1.5 ms.

While the T3-FRMR is synchronized to the DS3 M-frame, the F-bit and M-bit positions in the DS3 stream are examined. An out-of-frame defect is detected when 3 F-bit errors out of 8 or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration Register), or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. The M-bit error criteria for OOF can be disabled by the MBDIS bit in the DS3 FRMR Configuration register. In the presence of a high bit error rate, the 3 out of 8 consecutive F-bits out-of-frame ratio provides more robust operation than the 3 out of 16 consecutive F-bits ratio. Either out-of-frame criteria allows an out-of-frame defect to be detected quickly when the M-subframe alignment patterns are lost, or optionally, when the M-frame alignment pattern is lost.

Also, line code violations, M-bit or F-bit framing bit errors, and P-bit parity errors are indicated while in frame. When C-bit parity mode is enabled, both C-bit parity errors and far end block errors are indicated. These error indications, as well as the line code violation and excessive zeros indication, are accumulated over 1 second intervals with the Performance Monitor (PMON). Note that the framer is an off-line framer, indicating both OOF and COFA events. Even if an OOF is indicated, the framer will continue indicating performance monitoring information based on the previous frame alignment.

Three DS3 maintenance signals (a RED alarm condition, the alarm indication signal, and the idle signal) are detected by the T3-FRMR. The maintenance detection algorithm employs a simple integrator with a 1:1 slope that is based on the occurrence of "valid" M-frame intervals. For the RED alarm, an M-frame is said to be a "valid" interval if it contains a RED defect, defined as an occurrence of an OOF or LOS event during that M-frame. For AIS and IDLE, an M-frame interval is "valid" if it contains AIS or IDLE, defined as the occurrence of less than 15 discrepancies in the expected signal pattern (1010... for AIS, 1100... for IDLE) while valid frame alignment is maintained. This discrepancy threshold ensures the detection algorithms operate in the presence of a 10^{-3} bit error rate.

For AIS, the expected pattern may be selected to be:

1. The framed "1010" signal; the framed arbitrary DS3 signal and the C-bits all zero;

2. The framed "1010" signal and the C-bits all zero; the framed all-ones signal (with overhead bits ignored);

3. Or the unframed all-ones signal (with overhead bits equal to ones).

Each "valid" M-frame causes an associated integration counter to increment; "invalid" M-frames cause a decrement. With the "slow" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 127, which results in a detection time of 13.5 ms. With the "fast" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 21, which results in a detection time of 2.23 ms (i.e., 1.5 times the maximum average reframe time). RED, AIS, or IDLE are removed when the respective counter decrements to 0. DS3 Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

Valid X-bits are extracted by the T3-FRMR to provide indication of far end receive failure (FERF). A FERF defect is detected if the extracted X-bits are equal and are logic 0 (X1=X2=0); the defect is removed if the extracted X-bits are equal and are logic 1 (X1=X2=1). If the X-bits are not equal, the FERF status remains in its previous state. The extracted FERF status is buffered for 2 M-frames before being reported within the DS3 FRMR Status register. This buffer ensures a better than 99.99% chance of freezing the FERF status on a correct value during the occurrence of an out of frame.

When the C-bit parity application is enabled, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted. Codes in the FEAC channel are detected by the Bit Oriented Code Detector (RBOC). HDLC messages in the Path Maintenance Data Link are received by the Data Link Receiver (RDLC).

The T3-FRMR can be enabled to automatically assert the RAI indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or RED, or AIS. The T3-FRMR can also be enabled to automatically insert C-bit Parity FEBE upon detection of receive C-bit parity error.

The T3-FRMR extracts the entire DS3 overhead (56 bits per M-frame) using the ROH output, along with the OHCLK, and ROHFA outputs.

The T3-FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the T3-FRMR. Access to these registers is via a generic microprocessor bus.

10.10 E3 Framer

The E3 Framer (E3-FRMR) Block integrates circuitry required for decoding an HDB3-encoded signal and framing to the resulting E3 bit stream. The E3-FRMR is directly compatible with the G.751 and G.832 E3 applications.

The E3-FRMR searches for frame alignment in the incoming serial stream based on either the G.751 or G.832 formats. For the G.751 format, the E3-FRMR expects to see the selected framing pattern error-free for three consecutive frames before declaring INFRAME. For the G.832 format, the E3-FRMR expects to see the selected framing pattern error-free for two consecutive frames before declaring INFRAME. Once the frame alignment is established, the incoming data is continuously monitored for framing bit errors and byte interleaved parity errors (in G.832 format).

While in-frame, the E3-FRMR also extracts various overhead bytes and processes them according to the framing format selected.

10.10.1 In G.832 E3 Format, the E3-FRMR Extracts:

1. The Trail Trace bytes and outputs them as a serial stream for further processing by the Trail Trace Buffer (TTB) block.

2. The FERF bit and indicates an alarm when the FERF bit is a logic 1 for 3 or 5 consecutive frames. The FERF indication is removed when the FERF bit is a logic 0 for 3 or 5 consecutive frames.

3. The FEBE bit and outputs it for accumulation in PMON.

4. The Payload Type bits and buffers them so that they can be read by the microprocessor.

5. The Timing Marker bit and asserts the Timing Marker indication when the value of the extracted bit has been in the same state for 3 or 5 consecutive frames.

6. The Network Operator byte and presents it as a serial stream for further processing by the RDLC block when the RNETOP bit in the Channel Data Link and FERF/RAI Control register is logic 1. The byte is also brought out on the ROH output with the associated OHCH[3:0] using the overhead clock, OHCLK. All 8 bits of the Network Operator byte are extracted and presented on the overhead output and, optionally, presented to the RDLC.

7. The General Purpose Communication Channel byte and presents it to the RDLC when the RNETOP bit in the S/UNI-12xJET Data Link and FERF Control register is logic 0 The byte is also brought out on the ROH output with the associated OHCH[3:0] using the overhead clock, OHCLK.

10.10.2 In G.751 E3 Mode, the E3-FRMR Extracts:

1. The Remote Alarm Indication bit (bit 11 of the frame) and indicates a Remote Alarm when the RAI bit is a logic 1 for 3 or 5 consecutive frames. Similarly, the Remote Alarm is removed when the RAI bit is logic 0 for 3 or 5 consecutive frames.

2. The National Use reserved bit (bit 12 of the frame) and presents it as a serial stream for further processing in the RDLC when the RNETOP bit in the Channel Data Link and FERF/RAI Control register is logic 0. The bit is also brought out on the ROH output with the associated OHCH[3:0] using the overhead clock, OHCLK. Optionally, an interrupt can be generated when the National Use bit changes state.

Further, while in-frame, the E3-FRMR indicates the position of all the overhead bits in the incoming digital stream to the ATMF/SPLR block. For G.751 mode, the tributary justification bits can optionally be identified as either overhead or payload for payload mappings that take advantage of the full bandwidth.

The E3-FRMR declares out of frame alignment if the framing pattern is in error for four consecutive frames. The E3-FRMR is an "off-line" framer, where all frame alignment indications, all overhead bit indications, and all overhead bit processing continue based on the previous alignment. Once the framer has determined the new frame alignment, the out-of-frame indication is removed and a COFA indication is declared if the new alignment differs from the previous alignment.

The E3-FRMR detects the presence of AIS in the incoming data stream when less than 8 zeros in a frame are detected while the framer is OOF in G.832 mode, or when less than 5 zeros in a frame are detected while OOF in G.751 mode. This algorithm provides a probability of detecting AIS in the presence of a 10^{-3} BER as 92.9% in G.832 and 98.0% in G.751.

Loss of signal is declared when no marks have been received for 32 consecutive bit periods. Loss of signal is de-asserted after 32 bit periods during which there is no sequence of four consecutive zeros.

E3 Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

The E3-FRMR can also be enabled to automatically assert the RAI/FERF indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or AIS. The E3-FRMR can also be enabled to automatically insert G.832 FEBE upon detection of receive BIP-8 errors.

10.11 J2 Framer

The J2-FRMR integrates circuitry to decode a unipolar or B8ZS encoded signal and frame to the resulting 6312 Kbps J2 bit stream. Having found frame, the J2-FRMR extracts a variety of overhead and data-link information from the J2 bit stream.

The J2 format consists of 789-bit frames, each 125µs long, consisting of 96 bytes of payload, 2 reserved bytes, and 5 F-bits. The frames are grouped into 4-frame multi-frames. The multi-frame format is given in Table 4.

Table 4 J2 Framer Multi-frame Format

Bit #	1-8	...	761-768	769-776	777-784	785	786	787	788	789
Frm. 1	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	1	1	0	0	m
Frm. 2	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	1	0	1	0	0
Frm. 3	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	x1	x2	x3	a	m
Frm. 4	TS1[1:8]	...	TS96[1:8]	TS97[1:8]	TS98[1:8]	e1	e2	e3	e4	e5

TS1 .. TS96 : Byte interleaved payload

TS97, TS98: Reserved channels for signaling

Frame Alignment Signal: Represented as binary ones and zeroes

m : 4-kHz data link

x1, x2, x3: Spare bits, usually logic 1

a : Remote Loss of Frame alarm bit, active high

e1..e5: CRC-5 check sequence. The entire 3156-bit multi-frame, including the CRC-5 check sequence, should have a remainder of 0 when divided by $x^5 + x^4 + x^2 + 1$

The J2-FRMR frames to a J2 signal with an average reframe time of 5.07 ms. An alternate framing algorithm that uses the CRC-5 check to detect static mimic patterns is available. Once in frame, the J2-FRMR provides indications of frame and multi-frame boundaries, and marks overhead bits, x-bits, m-bits, and reserved channels (TS97 and TS98). Indications of loss of signal, bipolar violations, excessive zeroes, change of frame alignment, framing errors, and CRC errors are provided and may be accumulated by the PMON (with the exception of change of frame alignment); maskable interrupts are available to alert the microprocessor to the occurrence of any of these events. In addition to marking x-bit values, J2-FRMR provides microprocessor access to the x-bits, and will optionally generate an interrupt when any of the x-bits changes state. The m-bits and the associated clock can either be extracted through the RDLC or through the ROH and OHCLK output pins of the S/UNI-12xJET. The m-bits are also presented to the RBOC for detection of any generic bit-oriented codes.

Status signals such as Physical AIS, Payload AIS, Remote Alarm Indication in m-bits, and Remote Loss of Frame (a-bit) are detected by the J2-FRMR. In addition to providing indication signals of these states, the J2-FRMR will optionally generate an interrupt when any of these status signals changes.

J2 LOS is declared when no marks have been received for one of 15, 31, 63, or 255 consecutive bit periods. J2 LOS is cleared when either 15, 31, 63, or 255 consecutive bit periods have passed without an excessive zeros (8 or more consecutive zeros) detection as required by ITU-T G.775.

J2 LOF is declared when 7 or more consecutive multi-frames with erred framing patterns are received. The J2 LOF is cleared when 3 or more consecutive multi-frames with correct framing patterns are received. A framing algorithm that takes into account the CRC calculation is also available. The framing algorithms are described in the following text.

J2 Physical Layer AIS is declared when 2 or less zeros are detected in a sequence of 3156 bits. It is cleared when 3 or more zeros are detected in a sequence of 3156 bits as required by ITU-T G.775.

J2 Payload AIS is detected when the incoming J2 payload has 2 or less zeros in a sequence of 3072 bits. It is cleared when 3 or more zeros are detected in a sequence of 3072 bits.

The J2-FRMR may be forced to re-frame by microprocessor control. Similarly, the microprocessor may disable the J2-FRMR from reframing due to framing bit errors.

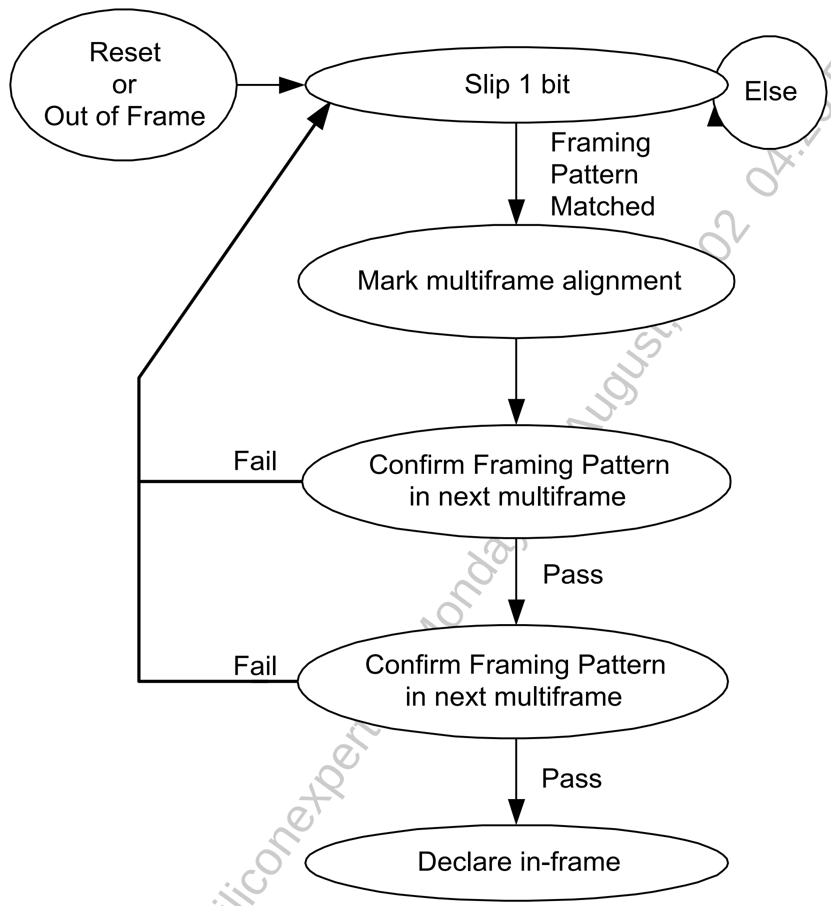
The J2-FRMR may be configured, and all sources of interrupts may be masked or acknowledged, via internal registers. These internal registers are accessed via a generic microprocessor bus.

10.11.1 J2 Frame Find Algorithms

The J2-FRMR searches for frame alignment using one of two algorithms, as selected by the CRC_REFR bit in the J2-FRMR Configuration Register.

When the CRC_REFR bit is set to logic 0, the J2-FRMR uses only the frame alignment sequence to find frame, searching for three consecutive correct frame alignment sequences. The frame find block searches for the entire 9-bit sequence (spread over two multi-frames) at the same time, greatly reducing the time required to find frame alignment. The framing process with CRC-REFR cleared is illustrated in Figure 19.

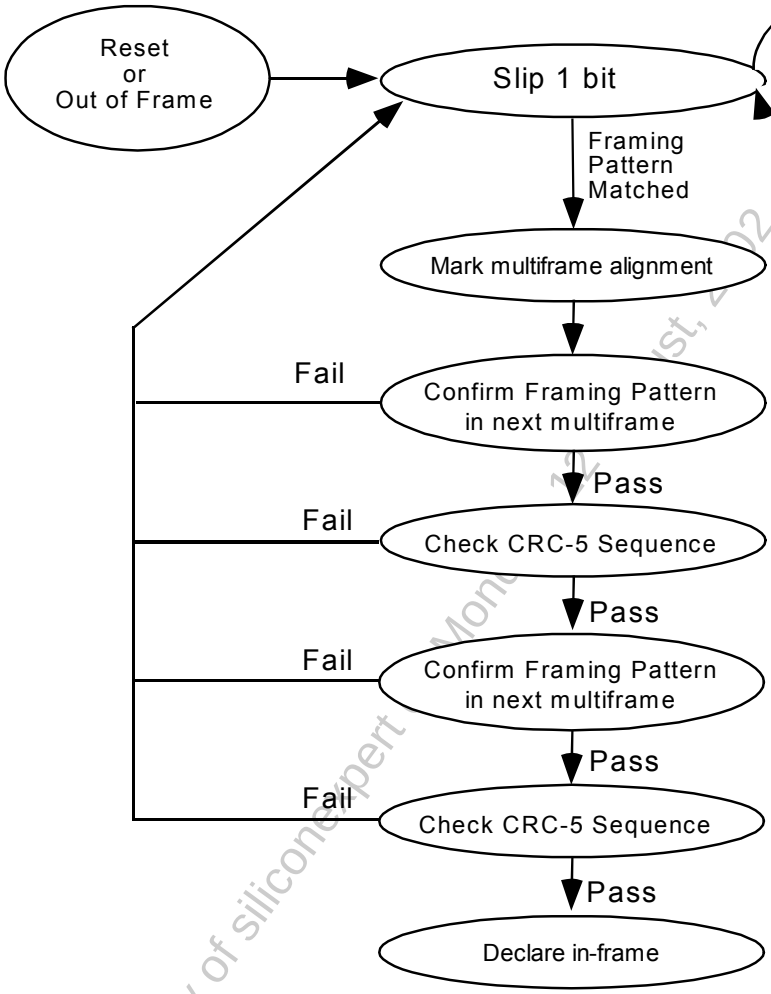
Figure 19 Framing Algorithm (CRC_REFR = 0)



Using this algorithm, the J2-FRMR will, on average, find frame in 5.07ms when starting the search in the worst possible position, given a 10^{-4} error rate and no static mimic patterns.

When the CRC_REFR bit is set to logic 1, in addition to requiring three consecutive correct framing patterns, the J2-FRMR requires that the first two CRC-5 checks be correct or a reframe is initiated. To speed the process, the CRC-5 and frame alignment checks are run concurrently, as illustrated in Figure 20.

Figure 20 Framing Algorithm (CRC_REFR = 1)



Using this algorithm, the J2-FRMR will find frame in 10.22ms, on average when starting the search in the worst possible position, given a 10^{-4} error rate and no static mimic patterns. The algorithm will reject 99.90% of mimic patterns. Further protection against mimic patterns is available by monitoring the rate of CRC-5 errors.

Once frame alignment is found and a change of frame alignment occurs, the block sets the LOF indication low. The block declares loss of frame alignment if 7 consecutive FASs have been received in error. In the presence of a random 10^{-3} bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of 1.65 years. The Frame Find Block can be forced to initiate a frame search at any time when the REFRAME bit in the J2-FRMR Configuration. Conversely, when the FLOCK bit is set to logic 1, the J2-FRMR will never declare Loss of Frame or search for a new frame alignment due to excess framing bit errors.

J2 extended Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

10.12 Performance Monitor Accumulator (PMON)

The Performance Monitor (PMON) Block interfaces directly with:

- Either the DS3 Framer (T3-FRMR) to accumulate line code violation (LCV) events, parity error (PERR) events, path parity error (CPERR) events, far end block error (FEBE) events, excess zeros (EXZS), and framing bit error (FERR) events using saturating counters;
- The E3 Framer (E3-FRMR) to accumulate LCV, PERR (in G.832 mode), FEBE and FERR events;
- Or the J2 Framer (J2-FRMR) to accumulate LCVs, CRC errors (in the PERR counter), Framing bit errors (FERR), and excess zeros (EXZS).

The PMON stops accumulating error signals from the E3, DS3, or J2 Framers once frame synchronization is lost.

When an accumulation interval is signaled by a write to the PMON register address space or a write to the S/UNI-12xJET Channel Identification, Master Reset, and Global Monitor Update register, the PMON transfers the current counter values into microprocessor accessible holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

When counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled. If the holding registers have not been read since the last interrupt, an overrun status bit is set. In addition, a register is provided to indicate changes in the PMON counters since the last accumulation interval.

10.13 Bit-Oriented Code Detector (RBOC)

The Bit-Oriented Code Detector is only used in DS3 C-bit Parity or J2 mode.

The Bit-Oriented Code Detector (RBOC) Block detects the presence of 63 of the 64 possible bit-oriented codes (BOCs) contained in the DS3 C-bit parity far-end alarm and control (FEAC) channel or in the J2 data link signal stream. The 64th code ("111111") is similar to the HDLC flag sequence and is ignored.

Bit-oriented codes (BOCs) are received on the FEAC channel as 16-bit sequences each consisting of 8 ones, a zero, 6 code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are validated when repeated at least 10 times. The RBOC can be enabled to declare a code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable Register. The RBOC declares that the code is removed if two code sequences containing code values different from the detected code are received in a moving window of ten code periods.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all ones ("111111") when no valid code is detected. The RBOC can be programmed to generate an interrupt when a detected code has been validated and when the code is removed.

10.14 Facility Data Link Receiver (RDLC)

The RDLC is a microprocessor peripheral used to receive LAPD/HDLC frames on any serial HDLC bit stream that provides data and clock information such as the DS3 C-bit parity Path Maintenance Data Link, the E3 G.832 Network Requirement byte or the General Purpose data link (selectable using the RNETOP bit in the S/UNI-12xJET Data Link and FERF/RAI Control register), the E3 G.751 Network Use bit, the J2 m-bit Data Link, the DS3 Mapping Overhead Communication Channel, or the Receive SONET/SDH Path DCC Channel.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-16.ISO-3309 frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128 byte-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status Register contains bits that indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status Register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

10.15 PLCP Layer Receiver (SPLR)

The PLCP Layer Receiver (SPLR) Block integrates circuitry to support DS1, DS3, E1, and G.751 E3 PLCP frame processing. The SPLR provides framing for PLCP based transmission formats.

The SPLR frames to DS1, DS3, E1, and G.751 E3 based PLCP frames with maximum average reframe times of 635 µs, 22 µs, 483 µs, and 32 µs respectively. Framing is declared (out of frame is removed) upon finding 2 valid, consecutive sets of framing (A1 and A2) octets and 2 valid and sequential path overhead identifier (POHID) octets. While framed, the A1, A2, and POHID octets are examined. OOF is declared when an error is detected in both the A1 and A2 octets or when 2 consecutive POHID octets are found in error. LOF is declared when an OOF state persists for more than 25 ms, 1 ms, 20 ms, or 1 ms for DS1, DS3, E1, or G.751 E3 PLCP formats respectively. If the OOF events are intermittent, the LOF counter is decremented at a rate 1/12 (DS3 PLCP), 1/10 (E1, DS1 PLCP) or 1/9(G.751 E3 PLCP) of the incrementing rate. LOF is thus removed when an in-frame state persists for more than 250 ms for a DS1 signal, 12 ms for a DS3 signal, 200 ms for an E1 signal, or 9 ms for a G.751 E3 signal. When LOF is declared, PLCP reframe is initiated.

When in frame, the SPLR extracts the path overhead octets and outputs them bit serially on output RPH, along with the OHCLK and RPHFA outputs. Framing octet errors and path overhead identifier octet errors are indicated as frame errors. Bit interleaved parity errors and far end block errors are indicated. The yellow signal bit is extracted and accumulated to indicate yellow alarms. Yellow alarm is declared when 10 consecutive yellow signal bits are set to logical 1; it is removed when 10 consecutive received yellow signal bits are set to logical 0. The C1 octet is examined to maintain nibble alignment with the incoming transmission system sub-layer bit stream.

10.16 ATM Cell Delineator (ATMF)

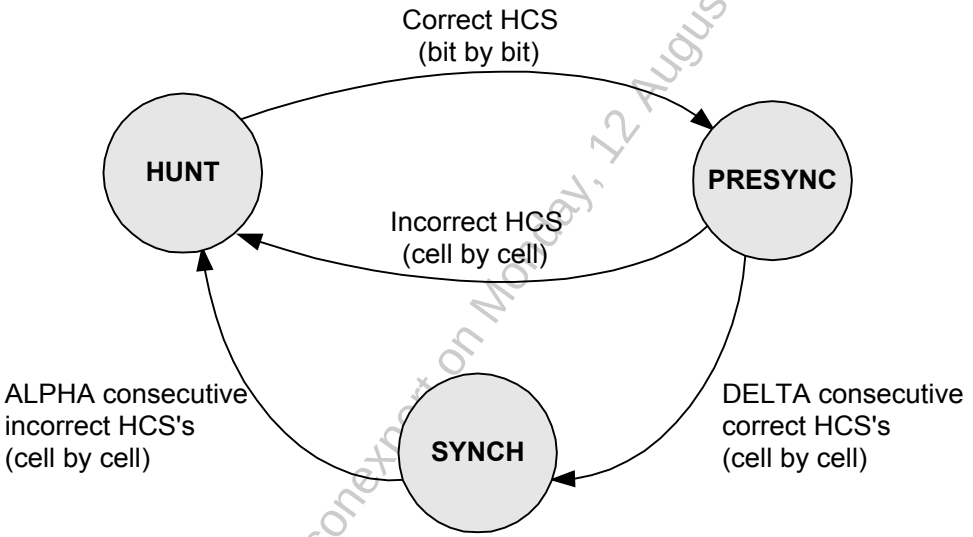
The ATM Cell Delineator (ATMF) Block integrates circuitry to support HCS-based cell delineation for non-PLCP based transmission formats. The ATMF block accepts a bit serial cell stream from an upstream transmission system sub-layer entity (such as the T3-FRMR, E3-FRMR, or J2-FRMR Block) and performs cell delineation to locate the cell boundaries. For PLCP applications, ATM cell positions are fixed relative to the PLCP frame but the ATMF still performs cell delineation to locate the cell boundaries.

Cell delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the ATM cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries.

The ATMF performs a sequential bit-by-bit, a nibble-by-nibble (DS-3 direct mapped), or a byte-by-byte (J2 and E3 direct-mapped) hunt for a correct HCS sequence. This state is referred to as the HUNT state. When receiving a bit serial cell stream from an upstream transmission system sub-layer entity, the bit, nibble, or byte boundaries are determined from the location of the overhead.

When a correct HCS is found, the ATMF locks on the particular cell boundary and assumes the PRESYNC state. This state verifies that the previously detected HCS pattern was not a false indication. If the HCS pattern was a false indication, then an incorrect HCS should be received within the next DELTA cells. At that point, a transition back to the HUNT state is executed. If an incorrect HCS is not found in this PRESYNC period, then a transition to the SYNC state is made. In this state, synchronization is not relinquished until ALPHA consecutive incorrect HCS patterns are found. In such an event, a transition is made back to the HUNT state. The state diagram of the cell delineation process is shown in Figure 21.

Figure 21 Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6 as recommended in ITU-T Recommendation I.432. These values result in a maximum average time to frame of 127 µs for a DS3 stream carrying ATM cells directly mapped into the DS3 information payload.

Loss of cell delineation (LCD) is detected by counting the number of incorrect cells while in the HUNT state. The counter value is stored in the RXCP LCD Count Threshold register. The threshold has a default value of 360 which results in a DS3 application detection time of 3.5 ms, an E3 G.832 application detection time of 4.5 ms and E3 G.751 application detection time of 5.0 ms, a J2 application time of 24.8ms, an E1 application detection time of 77 ms, and a DS1 application detection time of 100 ms. If the counter value is set to zero, the LCD signal is sent to the SARC and counted for every incorrect cell.

10.17 Receive Cell Processor (RXCP)

The Receive Cell Processor (RXCP) Block integrates circuitry to support scrambled or unscrambled cell payloads, scrambled or unscrambled cell headers, header check sequence (HCS) verification, idle cell filtering, and performance monitoring.

When interacting with the PDH payloads, the RXCP operates upon a delineated cell stream. For PLCP based transmissions systems, cell delineation is performed by the SPLR. For non-PLCP based transmission systems, cell delineation is performed by the ATMF. Framing status indications from these blocks ensure that cells are not written to the RXCP while the SPLR is in the loss of frame state, or cells are not written to the RXCP while the ATMF is in the HUNT or PRESYNC states.

When interacting with SONET payloads, Cells are assumed to be byte-aligned to the synchronous payload envelope. The RXCP performs cell delineation similar to the ATMF block on byte boundaries, see Figure 21. The values of ALPHA and DELTA determine the robustness of the delineation process. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in an average time to delineation of 32 µs for the STS-3c/STM-1 rate.

The RXCP descrambles the cell payload field using the self synchronizing de-scrambler with a polynomial of $x^{43} + 1$. Optionally, the header portion of the cells can also be de-scrambled. Note that cell payload scrambling is enabled by default in the S/UNI-12xJET, as required by ITU-T Recommendation I.432, but may be disabled to ensure backwards compatibility with older equipment.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RXCP verifies the received HCS using the accumulation polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result as required by the ATM Forum UNI specification and ITU-T Recommendation I.432.

The RXCP can be programmed to drop all cells containing an HCS error or to filter cells based on the HCS and the cell header. Filtering according to a particular HCS and the GFC, PTI and CLP bits of the ATM cell header (the VCI and VPI bits must be all logic 0) is programmable through the RXCP registers. More precisely, filtering is performed when filtering is enabled or when HCS errors are found when HCS checking is enabled. Otherwise, all cells are passed on regardless of any error conditions. Cells can be blocked if the HCS pattern is invalid or if the filtering 'Match Pattern' and 'Match Mask' registers are programmed with a certain blocking pattern. ATM Idle cells are filtered by default. For ATM cells, Null cells (Idle cells) are identified by the standardized header pattern of 'H00, 'H00, 'H00 and 'H01 in the first 4 octets followed by the valid HCS octet.

Note that the dropping of cells due to HCS errors only occurs while the ATMF is in the SYNC state.

Cell delineation can optionally be disabled, allowing the RXCP to pass all data bytes it receives.

The Performance Monitor consists of 8-bit saturating HCS error event counter and a 24-bit saturating receive cell counter. The error counter accumulates HCS errors. The 24-bit receive cell counter counts all cells written into the receive FIFO. Filtered cells are not counted.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counter be polled at least once per second so as not to miss any counted events.

10.18 Receive Byte HDLC Frame Processor (RXFP)

The Receive POS Frame Processor (RXFP) performs packet extraction, performs packet payload descrambling, and provides performance monitoring functions.

10.18.1 Overhead Removal

The overhead removal consists of stripping SONET/SDH overhead bytes from the data stream. Once overhead bytes are removed, the data stream consists of POS frame octets that can be fed directly to the de-scrambler or the POS Frame Delineation block.

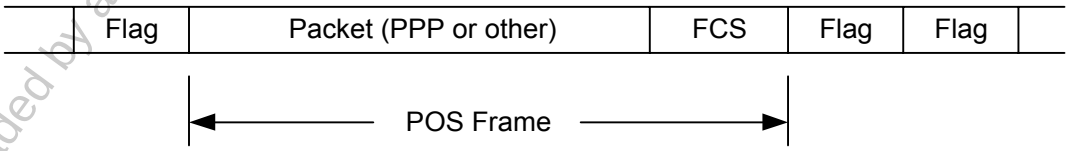
10.18.2 De-scrambler

When enabled, the self-synchronous de-scrambler operates on the POS Frame data, descrambling the data with the polynomial $x^{43} + 1$. Descrambling is performed on the raw data stream before any POS frame delineation or byte destuffing is performed. Data scrambling can provide for a more robust system, preventing the injection of hostile patterns into the data stream.

10.18.3 POS Frame Delineation

The POS Frame Delineation is performed on the de-scrambled data and consists of arranging the POS framed octets. Frame boundaries are found by searching for the Flag Character (0x7E). Flags are also used to fill inter-packet spacing. This block removes the Flag Sequence and passes the data onto the Byte Destuffing block. The POS Frame format is shown on Figure 22.

Figure 22 Packet Over SONET/SDH Frame Format



In the event of a FIFO overflow caused by the FIFO being full while a packet is being received, the packet is marked with an error so it can be discarded by the system. Subsequent bytes associated with this now aborted frame are discarded. Reception of POS data resumes when a Start of Packet is encountered and the FIFO level is below the programmable Reception Initialization Level (RIL[7:0]).

10.18.4 Byte Destuffing

The byte destuffing algorithm searches for the Control Escape character (0x7D). These characters, listed in Table 5, are added for transparency in the transmit direction and must be removed to recover the user data. When the Control Escape character is encountered, it is removed and the following data byte is XORed with 0x20. Therefore, any escaped data byte will be processed properly by the S/UNI-12xJET.

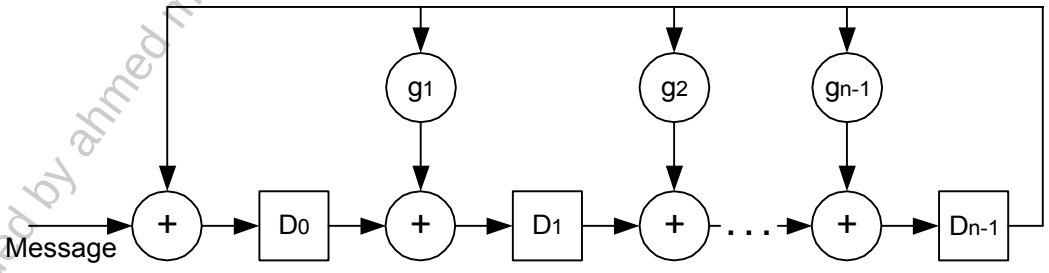
Table 5 HDLC Byte Sequences

Data Value	Sequence
0x7E (Flag Sequence)	0x7D 0x5E
0x7D (Control Escape)	0x7D 0x5D
HDLC Aborted Packet	0x7D 0x7E

10.18.5 FCS Check

The FCS Generator performs a CRC-16.ISO-3309 or CRC-32 calculation on the whole POS frame after byte destuffing and data descrambling scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-16.ISO-3309 or CRC-32 function. The CRC-16.ISO-3309 is two bytes in size and has a generating polynomial $g(x) = 1 + x^5 + x^{12} + x^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(x) = 1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$. The first FCS bit transmitted is the coefficient of the highest term. Packets with FCS errors are marked as such and should be discarded by the system.

Figure 23 Byte HDLC CRC Decode



10.18.6 Performance Monitor

The Performance Monitor consists of four 16-bit saturating error event counters and one 24-bit saturating received good packet counter. One of the error event counters accumulates FCS errors. The second error event counter accumulates minimum length violation packets. The third error event counter accumulates maximum length violation packets. The fourth error event counter accumulates aborted packets. The 24-bit receive good packet counter counts all error free packets.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, whichever is appropriate, so that a new period of accumulation can begin without loss of any events. The counters should be polled at least once per second so error events will not be missed.

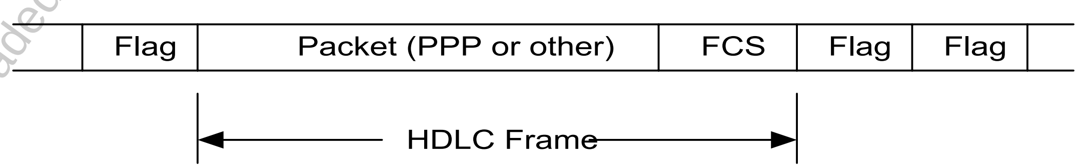
The RXFP monitors the packets for both minimum and maximum length errors. When a packet size is smaller than MINPL[7:0], the packet is marked with an error but is still written into the FIFO. Malformed packets, that is packets that do not at least contain the FCS field plus one byte, are treated differently. If a malformed packet is received and FCS stripping is enabled, the packet is discarded, not written in the FIFO, and counted as a minimum packet size violation. If a malformed packet is received and FCS stripping is disabled, it is written into the FIFO since, in this case, the misformed packet criteria is reduced to one byte, but will still count as a minimum packet size violation. When the packet size exceeds MAXPL[15:0] the packet is marked with an error and the bytes beyond the maximum count are discarded.

10.19 Receive Bit HDLC Frame Processor (RXFP)

10.19.1 Bit HDLC Framer

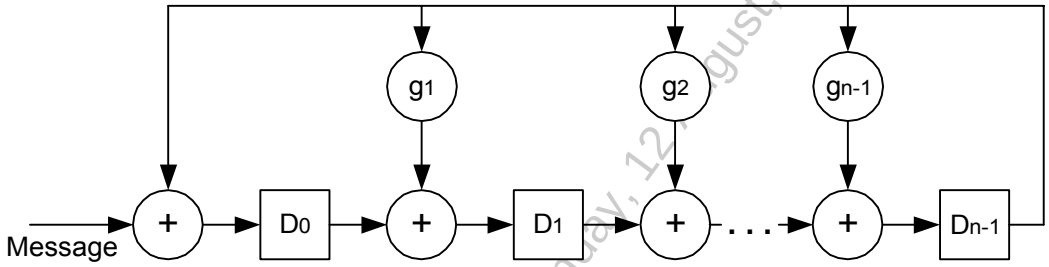
Figure 24 shows a diagram of the synchronous HDLC protocol supported by RXFP. The incoming stream is examined for flag bytes (01111110 bit pattern), which delineate the opening and closing of the HDLC packet. The packet is bit de-stuffed which discards a "0" bit which directly follows five contiguous "1" bits. The resulting HDLC packet size must be a multiple of an octet (8 bits) and within the expected maximum packet length limit. A HDLC packet is aborted when seven contiguous "1" bits (with no inserted "0" bits) are received. An idle HDLC stream is when at least fifteen contiguous "1" bits (with no inserted "0" bits) are received. At least one flag byte must exist at the start and end of each HDLC packet for packet delineation. Contiguous flag sequences or HDLC idle may be used as an "interframe time fill" between packets . Adjacent flag sequences may share zeros.

Figure 24 Bit HDLC Frame



The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-16.ISO-3309 or CRC-32 function. Figure 25shows a CRC encoder block diagram using the generating polynomial $g(X) = 1 + g_1X + g_2X^2 + \ldots + g_{n-1}X^{n-1} + X^n$. The CRC-16.ISO-3309 is two bytes in size and has a generating $g(X) = 1 + X^5 + X^{12} + X^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The CRC registers are preset to all ones and are then modified by the incoming data stream. The first FCS bit received is the coefficient of the highest term.

Figure 25 Bit HDLC CRC Generator



10.19.2 Performance Monitor

The Performance Monitor consists of four 16-bit saturating error event counters and one 24-bit saturating received good packet counter. One of the error event counters accumulates FCS errors. The second error event counter accumulates minimum length violation packets. The third error event counter accumulates maximum length violation packets. The fourth error event counter accumulates aborted packets. The 24-bit receive good packet counter counts all error free packets.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, whichever is appropriate, so that a new period of accumulation can begin without loss of any events. The counters should be polled at least once per second so error events will not be missed.

The RXFP monitors the packets for both minimum and maximum length errors. When a packet size is smaller than MINPL[7:0], the packet is marked with an error but is still written into the FIFO. Malformed packets, that is packets that do not at least contain the FCS field plus one byte, are treated differently. If a malformed packet is received and FCS stripping is enabled, the packet is discarded, not written in the FIFO, and counted as a minimum packet size violation. If a malformed packet is received and FCS stripping is disabled, it is written into the FIFO since, in this case, the misformed packet criteria is reduced to one byte, but will still count as a minimum packet size violation. When the packet size exceeds MAXPL[15:0] the packet is marked with an error and the bytes beyond the maximum count are discarded.

10.20 Receive UTOPIA Level 2 ATM Interface

The UTOPIA Level 2 compatible interface accepts a read clock (RFCLK) and read enable signal (RENB). The interface indicates the start of a cell (RSOC) and the receive cell available status (RCA) when data is read from the receive FIFO (using the rising edges of RFCLK). The RCA status changes from available to unavailable when the FIFO is either empty (when RCALEVEL0 is high) or near empty (when RCALEVEL0 is low). This interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while RCA is a logic zero will output invalid data. The FIFO is reset on FIFO overrun, causing up to 4 cells to be lost.

10.21 Receive POS-PHY Level 2 Interface

The POS-PHY Level 2 compatible interface is an extension to the UTOPIA 2 interface to allow for the transfer of packets. POS-PHY byte-level transfer mode is supported.

The RSOP signal is used to identify the start of a packet. The RPA signal notifies the system side that data is in the receive FIFO (when a programmable number of bytes in a single packet is received or when an end of packet is available). The RDATA[11:0] bus transfers the data from the FIFO across the system interface. The RPRTY signal determines the parity on the RDAT bus (selectable as odd or even parity). RFCLK is used to read words from the FIFO interface and RENB is used to initiate reads from the receive FIFO. Signal REOP (Receive End of Packet) is used to identify the end of a packet. Signal RMOD (Receive Mod) is provided to indicate whether 1 or 2 bytes are valid on the final word transfer when in 16-bit mode (REOP is asserted). Signal RERR (Receive Error) is provided to indicate that an error in the received packet has occurred. (The error may have several causes, including an abort sequence and an FCS error).

The receive data valid signal, RVAL, plays a special role in this interface. The data signals shall be considered valid only when RVAL is asserted. RVAL is asserted when a data transfer is initiated, conditional to RPA also being asserted. Once the transfer is initiated, RVAL will remain asserted until either the FIFO is empty or an end of packet is encountered. Once de-asserted, RVAL will remain low until the current PHY is deselected and another or the same PHY is reselected. RVAL allows the link layer device to align data transfers with packet boundaries, making it easier to manage packet buffers. RVAL should be used at all times when RENB is low to qualify the receive data stream due to RPA falsely indicating data in the FIFO. See the Functional Timing section for more information.

10.22 Receive UTOPIA Level 3 Interface

The Receive UTOPIA/POS-PHY Level 3 Interface (RUL3) provides FIFO management at the S/UNI-12xJET receive cell interface during UTOPIA Level 3 operation. Each channel receive FIFO may contain up to sixteen cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include filling the receive FIFO, indicating when the receive FIFO contains cells, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun conditions.

The UTOPIA Level 3 compatible interface accepts a read clock (RFCLK) and read enable signal (RENB). The RADR[3:0] bus with RCA is used to poll the channel FIFOs for fill status. As well, channels are selected using the RADR[3:0] and falling edge of RENB. The interface indicates the start of a cell (RSOC) when data is read on the receive RDAT[31:0] bus. The RPRTY signal reports the parity on the RDAT[31:0] bus (selectable as odd or even parity). This interface also indicates FIFO overruns via a maskable interrupt and register bits.

10.23 Receive POS-PHY Level 3 Interface

The Receive UTOPIA/POS-PHY Level 3 Interface (RUL3) provides FIFO management at the S/UNI-12xJET receive interface during POS-PHY Level 3 operation. Each channel receive FIFO contains 1024 bytes. The FIFO provides the system rate decoupling function between the transmission system physical layer and the link layer, and handles timing differences caused by the removal of escape characters.

In general, the management functions include filling the receive FIFO, indicating when the receive FIFO contains packet data or cells, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun conditions.

The interface accepts a read clock (RFCLK) and read enable signal (RENB) when data is read from the receive FIFO (using the rising edge of the RFCLK). The start of packet RSOP marks the first byte of receive packet data on the RDAT[31:0]. The RPRTY signal determines the parity on the RDAT[31:0] bus (selectable as odd or even parity). The end of a packet is indicated by the REOP signal with the RMOD[1:0] signals indicating the number of valid bytes on RDAT[31:0]. Signal RERR is provided to indicate that an error in the received packet has occurred. The error may have several causes including an abort sequence or a FCS error).

The RVAL signal is used to indicate when RSOP, REOP, RERR, RMOD[1:0] and RDAT[31:0] are valid. This interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while RVAL is low are ignored and will output invalid data. RVAL will not assert until RENB is asserted.

10.24 Cell and PLCP Performance Monitor (CPPM)

The Cell and PLCP Performance Monitor (CPPM) Block interfaces directly to the SPLR to accumulate bit interleaved parity error events, framing octet error events, and far end block error events in saturating counters. When the PLCP framer (SPLR) declares loss of frame, bit interleaved parity error events, framing octet error events, far end block error events, and header check sequence error events are not counted.

When an accumulation interval is signaled by a write to the CPPM register address space or to the S/UNI-12xJET Identification, Master Reset, and Global Monitor Update register (register 006), the CPPM transfers the current counter values into holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

10.25 Pseudo-Random Sequence Generator/Detector (PRGD)

The Pseudo-Random Sequence Generator/Detector (PRGD) block is a software programmable test pattern generator, receiver and analyzer. Two types of test patterns, pseudo-random and repetitive, conform to ITU-T O.151.

The PRGD can be programmed to generate any pseudo-random pattern up to 2^{32}-1 bits in length or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rate between 10^{-1} to 10^{-7}.

The PRGD can be programmed to check for the presence of the generated pseudo-random pattern. The PRGD can perform an auto-synchronization to the expected pattern, and generate interrupts on detection and loss of the specified pattern. The PRGD can accumulate the total number of bits received and the total number of bit errors in two saturating 32-bit counters. The counters accumulate over an interval defined by writes to the S/UNI-12xJET Identification/Master Reset, and Global Monitor Update register (register 006) or by writes to any PRGD accumulation register. When an accumulation is forced by either method, then the holding registers are updated and the counters reset to begin accumulating for the next interval. The counters are reset in such a way that no events are missed. The data is then available in the holding registers until the next accumulation. In addition to the two counters, a record of the 32 bits received immediately prior to the accumulation is available.

The PRGD may also be programmed to check for repetitive sequences. When configured to detect a pattern of length N bits, the PRGD will load N bits from the detected stream and determine whether the received pattern repeats itself every N subsequent bits. Should it fail to find such a pattern, it will continue loading and checking until it finds a repetitive pattern. All the features (error counting, auto-synchronization, etc.) available for pseudo-random sequences are also available for repetitive sequences. Whenever a PRGD accumulation is forced, the PRGD stores a snapshot of the 32 bits received immediately prior to the accumulation. This snapshot may be examined in order to determine the exact nature of the repetitive pattern received by PRGD.

The pseudo-random or repetitive pattern can be inserted/extracted in the PLCP payload (if PLCP framing is enabled) or in the DS3, E3, J2, or Arbitrary framing format payload (if PLCP framing is disabled). It cannot be inserted into the ATM cell payload.

10.26 Transmit Regenerator Multiplexer Processor (TRMP)

The Transmit Regenerator and Multiplexer Processor (TRMP) block inserts the transport overhead bytes in the transmit data stream.

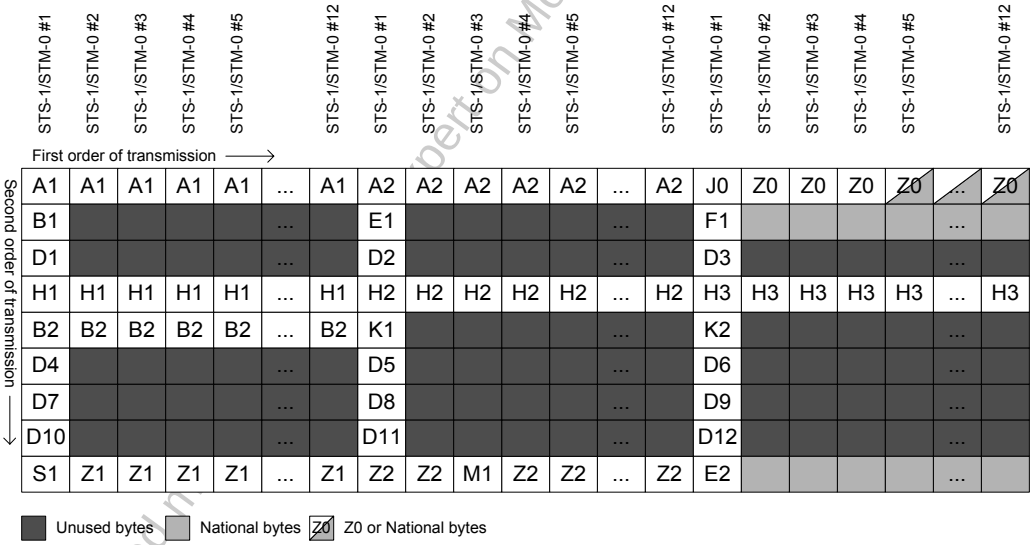
The TRMP accumulates the line BIP-8 errors detected by the RRMP during the last receive frame. The line BIP-8 errors are returned to the far end as line remote error indication (REI-L) during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one or two line BIP-8 errors can be accumulated per transmit frame (if configured for block BIP mode). The minimum value between the maximum REI-L given in Table 6 and the accumulator count is returned as the line REI-L in the M1 byte of STS-1 (STM-0) #3. Optionally, block BIP-24 errors can be accumulated.

Table 6 Maximum Line REI Errors per Transmit Frame

SONET/SDH	Maximum Single BIP-8 errors LREIBLK=0	Maximum Block BIP-24 errors LREIBLK=1
STS-3/STM-1	0001 1000	0000 0001
STS-12/STM-4	0110 0000	0000 0100

The TRMP serially inputs all the transport overhead (TOH) bytes from the TTOH port. The TOH bytes must be input in the same order that they are transmitted (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). TOHCLK is the generated output clock used to provide timing for the TTOH port. TOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling TOHFP high with the rising edge of TOHCLK identifies the MSB of the first A1 byte. TTOHEN port is used to validate the byte insertion on a byte per byte basis. When TTOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TTOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

Figure 26 STS-12 (STM-4) On TTOH



The TRMP serially inputs the line DCC bytes from the TSLD ports. TSLD is selectable to input either the section DCC bytes (D4-D12) or the line DCC bytes (D1-D3). TSLDCLK is the generated output clock used to provide timing for the TSLD port. If TSLD carries the line DCC, TSLDCLK is a nominal 576 kHz clock or if TSLD carries the section DCC, TSLDCLK is a nominal 192 kHz clock. Sampling TOHFP high identifies the MSB of the first DCC byte on TSLD (D1 or D4).

The TRMP also inserts most of the transport overhead bytes from internal registers. Since there are multiple sources for the same overhead byte, the TOH bytes must be prioritized according to Table 7 before being inserted into the data stream.

Table 7 TOH Insertion Priority

BYTE	HIGHEST priority						LOWEST priority
A1		76h (A1ERR=1)	F6h (A1A2EN=1)	TTOH (TTOHEN=1)			A1 pass through
A2			28h (A1A2EN=1)	TTOH (TTOHEN=1)			A2 pass through
J0	STS-1/STM-0 # (J0Z0INCEN=1)	J0[7:0] (TRACEEN=1)	J0V (J0REGEN=1)	TTOH (TTOHEN=1)			J0 pass through
Z0	STS-1/STM-0 # (J0Z0INCEN=1)		Z0V (Z0REGEN=1)	TTOH (TTOHEN=1)			Z0 pass through
B1				Calculated B1 XOR TTOH (TTOHEN=1 & B1MASKEN=1) TTOH (TTOHEN=1 & B1MASKEN=0)			Calculated B1 XOR B1MASK
E1			E1V (E1REGEN=1)	TTOH (TTOHEN=1)			E1 pass through
F1			F1V (F1REGEN=1)	TTOH (TTOHEN=1)			F1 pass through
D1-D3			D1D3V (D1D3REGEN=1)	TTOH (TTOHEN=1)	TSLD (TSLDSEL=0 & TSLDEN=1)		D1-D3 pass through
H1				H1 pass through XOR TTOH (TTOHEN=1 & HMASKEN=1) TTOH (TTOHEN=1 & HMASKEN=0)			H1 pass through XOR H1MASK
H2				H2 pass through XOR TTOH (TTOHEN=1 & HMASKEN=1) TTOH (TTOHEN=1 & HMASKEN=0)			H2 pass through XOR H2MASK
H3				TTOH (TTOHEN=1)			H3 pass through
B2				Calculated B2 XOR TTOH (TTOHEN=1 & B2MASKEN=1) TTOH (TTOHEN=1 & B2MASKEN=0)			Calculated B2 XOR B2MASK
K1		APS[15:8] (APSEN=1)	K1V (K1K2REGEN=1)	TTOH (TTOHEN=1)			K1 pass through
K2		APS[7:0] (APSEN=1)	K2V (K1K2REGEN=1)	TTOH (TTOHEN=1)			K2 pass through
D4-D12			D4D12V (D4D12REGEN=1)	TTOH (TTOHEN=1)	TSLD (TSLDSEL=1 & TSLDEN=1)		D4-D12 pass through
S1			S1V (S1REGEN=1)	TTOH (TTOHEN=1)			S1 pass through
Z1			Z1V (Z1REGEN=1)	TTOH (TTOHEN=1)			Z1 pass through

BYTE	HIGHEST priority						LOWEST priority
Z2			Z2V (Z2REGEN=1)	TTOH (TTOHEN=1)			Z2 pass through
M1			LREI[7:0] (LREIEN=1)	TTOH (TTOHEN=1)			M1 pass through
E2			E2V (E2REGEN=1)	TTOH (TTOHEN=1)			E2 pass through
National			NATIONALV (NATIONALEN=1)	TTOH (TTOHEN=1)			National pass through
Unused			UNUSEDV (UNUSEDEN=1)	TTOH (TTOHEN=1)			Unused pass through
PLD							PLD pass through

The Z0DEF register bit defines the Z0/NATIONAL growth bytes for row #1. When Z0DEF is set to logic one, the Z0/NATIONAL bytes are defined according to ITU. When Z0DEF is set to logic zero, the Z0/NATIONAL bytes are defined according to BELLCORE.

Table 8 Z0/National Growth Bytes Definition for Row #1

TRMP mode	Type	Z0DEF = 1	Z0DEF = 0
STS-3/STM-1	Z0	None	From STS-1/STM-0 #2 to #3
	National	From STS-1/STM-0 #2 to #3	None
STS-12/STM-4 master mode	Z0	From STS-1/STM-0 #2 to #4	From STS-1/STM-0 #2 to #12
	National	From STS-1/STM-0 #5 to #12	None

The H1, H2, B1 and B2 bytes input from the TTOH port are inserted or are used as a mask to toggle bits in the corresponding H1, H2, B1 and B2 bytes depending on the HMASK B1MASK and B2MASK register bits. When the HMASK, B1MASK or B2MASK register bit is set low and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is inserted in place of the corresponding byte. When the HMASK, B1MASK or B2MASK register bit is set high and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is XORed with the corresponding path payload pointer (already in the data stream) or the calculated BIP-8 byte before being inserted.

The TRMP inserts the APS bytes detected by the RRMP during the last receive frame. The APS bytes are returned to the far end by the TRMP during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one, or two APS bytes can be sampled per transmit frame. The last received APS bytes are transmitted.

The TRMP inserts the line remote defect indication (RDI-L) into the data stream. When line RDI must be inserted, the "110" pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1 (STM-0) #1. Line RDI insertion has priority over TOH byte insertion. The TRMP also inserts the line alarm indication signal (AIS-L) into the data stream. When line AIS must be inserted, all ones are inserted in the line overhead and in the payload (all bytes of the frame except the section overhead bytes). Line AIS insertion has priority over line RDI insertion and TOH byte insertion.

The TRMP calculates the line BIP-8 error detection codes on the transmit data stream. One line BIP-8 error detection code is calculated for each of the constituent STS-1 (STM-0). The line BIP-8 byte is calculated on the unscrambled bytes of the STS-1 (STM-0) except for the 9 SOH bytes. The line BIP-8 byte is based on a bit interleaved parity calculation using even parity. For each STS-1 (STM-0), the calculated BIP-8 error detection code is inserted in the B2 byte of the following frame before scrambling.

The TRMP optionally scrambles the transmit data stream.

The TRMP calculates the section BIP-8 error detection code on the transmit data stream. The section BIP-8 byte is calculated on the scrambled bytes of the complete frame. The section BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B1 byte of STS-1 (STM-0) #1 of the following frame before scrambling.

10.27 Transmit Trail trace Processor (TTTP)

The Transmit Trail trace Processor (TTTP) block generates the trail trace messages to be transmitted. The TTTP can generate a 16 or 64 byte trail trace message. The message is sourced from an internal RAM and must have been previously written by an external micro processor. Optionally, the trail trace message can be reduced to a single continuous trail trace byte.

The trail trace message must include synchronization because the TTTP does not add synchronization. The synchronization mechanism is different for a 16 byte message and for a 64 byte message. When the message is 16 bytes, the synchronization is based on the MSB of the trail trace byte. Only one of the 16 bytes has its MSB set high. The byte with its MSB set high is considered the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of trail trace message. The byte following the CR/LF bytes is considered the first byte of the message.

To avoid generating an unstable/mismatch message, the TTTP forces the message to all zeros while the microprocessor updates the internal RAM.

10.28 Transmit High Order Path Processor (THPP)

The Transmit High Order Path Processor (THPP) block inserts the path overhead bytes in the transmit data stream.

The THPP accumulates the path BIP-8 errors detected by the RHPP during the last receive frame. The path BIP-8 errors are returned to the far end as path remote error indication (REI-P) during the next transmit frame. Because the RHPP and the THPP are in two different clock domains, none, one, or two path BIP-8 errors can be accumulated per transmit frame (if configured for block BIP mode). The minimum value between the maximum REI-P and the accumulator count is returned as the path REI in the G1 byte. Optionally, block BIP-8 errors can be accumulated.

The THPP serially inputs all the path overhead (POH) bytes from the TPOH port. The POH bytes must be input in the same order that they are transmitted (J1, B3, C2, G1, F2, H4, F3, K3 and N1). TOHCLK is the generated output clock used to provide timing for the TPOH port. TOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling TOHFP high with the rising edge of TOHCLK identifies the MSB of the first J1 byte. The TPOHEN port is used to validate the byte insertion on a byte per byte basis. When TPOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TPOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

The THPP calculates the path BIP-8 error detection code on the transmit data stream. The path BIP-8 byte is calculated on all the payload bytes. The path BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B3 byte of the following frame.

10.29 Transmit Add Telecom Bus Pointer Interpreter (TAPI)

The Transmit Add Telecom Bus Pointer Interpreter (TAPI) block takes a SONET/SDH data stream from the ADD TelecomBus bus, interprets the STS-1/3c/12c/48c (AU3/4/4-4c/4-16c) pointers, indicates the J1 byte locations and detects alarm conditions (e.g. PAIS).

The TAPI block allows the S/UNI-12xJET to operate with TelecomBus like back plane systems which do not indicate the J1 byte positions. The TAPI block can be enabled using the TAPIDIS bit in the S/UNI-12xJET 0x1806 register. When enabled, the TAPI takes a SONET/SDH data stream from the System Side Interface block, processes the stream and identifies the J1 byte locations.

10.30 SONET/SDH Virtual Container Aligner (SVCA)

The SONET/SDH Virtual Container Aligner (SVCA) block aligns the payload data from an incoming SONET/SDH data stream to a new transport frame reference. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the incoming data stream and that of the outgoing data stream.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the incoming data stream and the outgoing data stream are accommodated by pointer adjustments in the outgoing data stream.

10.30.1 Elastic Store

The Elastic Store performs rate adaptation between the line side interface and the system side interface. The entire incoming payload, including path overhead bytes, is written into a first-in-first-out (FIFO) buffer at the incoming byte rate. Each FIFO word stores a payload data byte and a one bit tag labeling the J1 byte. Incoming pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the outgoing byte rate by the Pointer Generator. Analogously, outgoing pointer justifications are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the addresses relative to FIFO thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the outgoing data stream for three frames to alert downstream elements of data corruption.

10.30.2 Pointer Generator

The Pointer Generator generates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the synchronous payload envelop bytes (SPE) of the constituent STS-1/3c/12c/48c (VC3/4/4-4c/4-16c) payloads. The pointer generator is a time multiplexed finite state machine that can process any mixed of STS-1/3c/12c/48c (AU3/4/4-4c/4-16c) pointers. Within the pointer generator algorithm, five states are defined as shown below

NORM_state (NORM)

AIS_state (AIS)

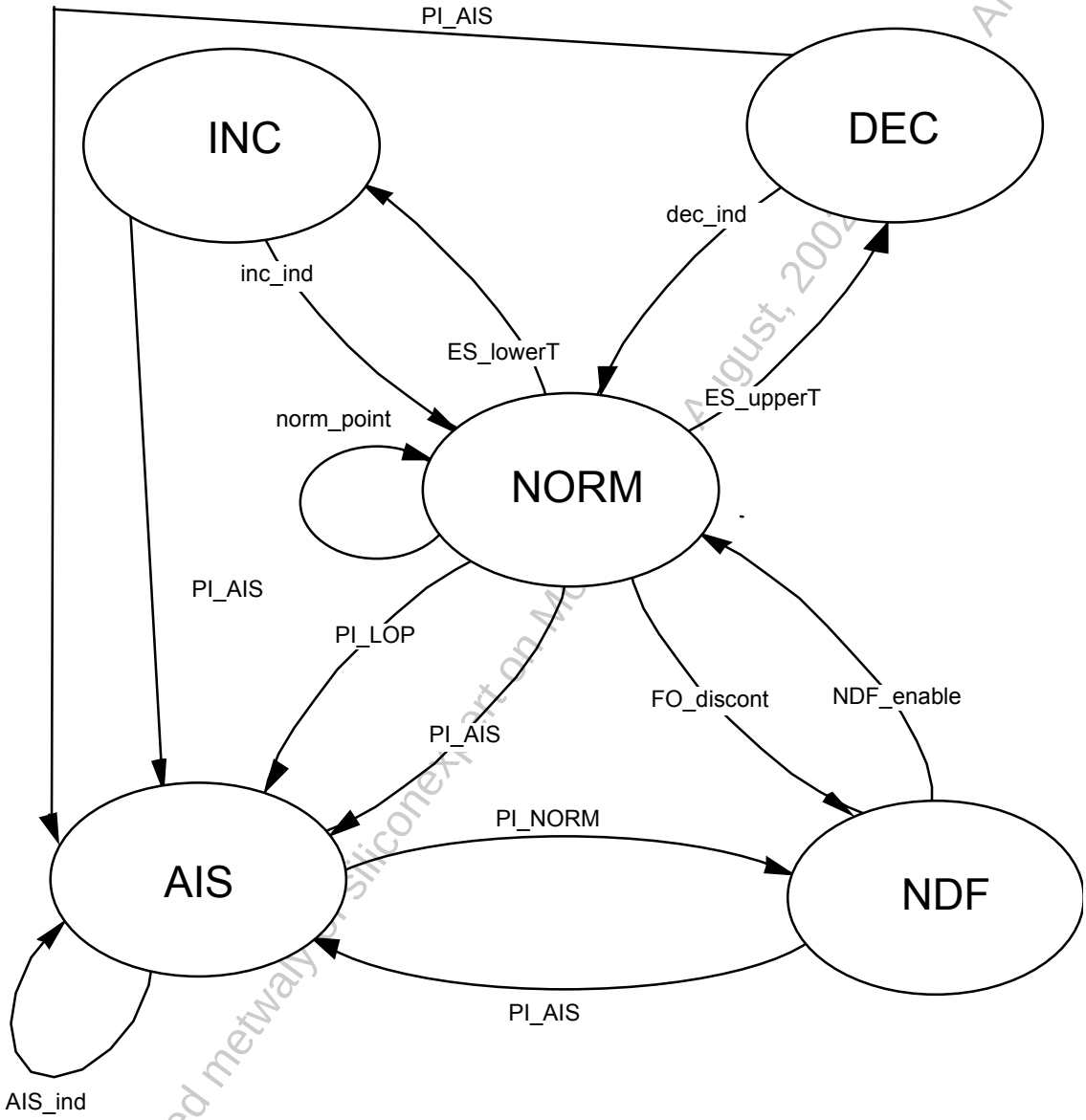
NDF_state (NDF)

INC_state (INC)

DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store (ES) block. The transition to/from the AIS state are controlled by the pointer interpreter (PI) in the Receive High Order Path Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 27 Pointer Generation State Diagram



The following events, indicated in the state diagram, are defined

ES_lowerT: ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

ES_upperT: ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

FO_discont: frame offset discontinuity

PI_AIS: PI in AIS state

PI_LOP: PI in LOP state

PI_NORM: PI in NORM state

Note 1 A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined as follows

inc_ind: transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.

dec_ind: transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.

NDF_enable: accept new offset as active offset, transmit the pointer with NDF enabled and new offset.

norm_point: transmit the pointer with NDF disabled and active offset.

AIS_ind: active offset is undefined, transmit an all-1's pointer and payload.

Note 1 active offset is defined as the phase of the SPE (VC).

Note 2 the SS bits are undefined in SONET, and has bit pattern 10 in SDH

Note 3 enabled NDF is defined as the bit pattern 1001.

Note 4 disabled NDF is defined as the bit pattern 0110.

10.31 SONET/SDH PRBS Generator and Monitor (PRGM)

The SONET/SDH Pseudo-Random bit sequence Generator and Monitor (PRGM) block generates and monitors an unframed 2^{23}-1 payload test sequence on the TelecomBus ADD or DROP bus.

The PRGM can generate PRBS in an STS-1/3c/12c (AU3/4/4—4c) payload. The path overhead column, the fixed stuff columns #2 to #4 in an STS-12c (AU-4-4c) payload, and the fixed stuff column #30 and #59 in an STS-1 (AU3) payload do not contain any PRBS data. The PRGM generator can be configured to preserve payload framing and overwrite the payload bytes or can be configured to autonomously generate payload framing and overwrite the payload bytes.

The PRBS monitor of the PRGM block monitors the recovered payload data for the presence of an unframed 2^{23}-1 test sequence and accumulates pattern errors based on this pseudo-random pattern. The PRGM declares synchronization when a sequence of 32 correct pseudo-random patterns (bytes) are detected consecutively. Pattern errors are only counted when the PRGM is in synchronization with the input sequence. When 16 consecutive pattern errors are detected, the PRGM will fall out of synchronization and will continuously attempt to re-synchronize to the input sequence until it is successful.

A maskable interrupt is activated to indicate any change in the synchronization status.

10.32 Transmit STS-1 Time Slot Interchange (TX_STI)

The TX_STI determines which STS-1 Timeslots are to be provisioned for a particular channel. An incoming ADD bus is provided to the TX_STI. The TX_STI will overwrite the data on the ADD bus in the timeslots provisioned for that particular slice with data from the channel. In addition, the TX_STI allows unique STS configurations (with a granularity of STS-1 or STS-3) for virtual concatenation using external SONET path processors.

- The TX_STI is not a complete Time Slot Interchange in that it does not re-order timeslots; however, the TX_STI does allow any channel to provide data on any of the timeslots in chronological order starting from the master timeslot.

10.33 DS3/E3 Mapper (D3E3MA)

The D3E3MA accepts either a DS3 or E3 serial stream and maps it into an STS-1 SPE via TUG-3 or AU-3 mapping. The D3E3MA performs the DS3/E3 to STS-1 mapping, and keeps mapping jitter within ITU and ANSI specifications.

10.33.1 FIFO

The Elastic Store FIFO is 32 bytes deep. The Elastic Store FIFO can be reset via normal mode register bit. Upon reset, overflow or underflow, the FIFO read and write pointers are set as far away from each other as possible. The Elastic Store FIFO also maintains FIFO centering through simple peak detection, or through a secondary centering method which maintains the FIFO fill level at an optimal operation position.

Both FIFO centering mechanisms can be enabled/disabled via normal mode register bit GAPCALCB and FIFOCTRB.

10.33.2 AIS Generator

The AIS Generator creates the E3 and DS3 Alarm Indication Signal that is inserted into the bit stream to indicate failure conditions. The AIS Generator is controlled via normal mode register bits (DS3E3B, AISGEN) and upstream AIS generation signals. The AIS pattern is described in section 13.15

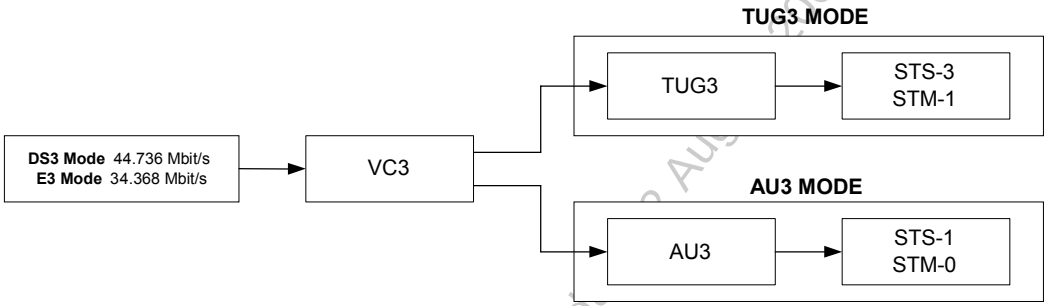
During AIS mode, the stuff commands from the DPLL are ignored and nominal stuffing is applied by driving the respective outputs accordingly. Nominal Rate stuffing requires the insertion of an information bit into the stuff opportunity position 3 times per STS-1 frame.

10.33.3 Mapper

The Mapper block receives E3 or DS3 payload data from the FIFO, maps the data according to Figure 28 and outputs the data to the downstream block. The Mapper also performs Overhead Communication Channel Insertion.

The D3E3MA supports a variety of mapping structures (AU3 or TUG3) and perform either DS3 or E3 mapping. These mapping modes can be set via the normal mode register bits DS3E3B and AU3TUG3B. Regardless of the incoming data source (AIS or FIFO) the D3E3MA first maps the DS3 or E3 stream to a common VC-3 structure. The VC-3 is then mapped to an STS-1/ STM-0 SPE via AU3 or into 1/3 of a STS-3/STM-1 via TUG3. The overall mapping structure implemented is depicted in Figure 28.

Figure 28 Mapping Structure



In DS3 or E3 mode, the D3E3MA maps the incoming DS3 or E3 payload into a VC-3. The DS3 or E3 payload is always demapped from a VC-3, regardless of whether the SPE has been mapped according to AU3 or TUG3 specifications. The asynchronous DS3 to VC-3 mapping is shown in Figure 58. The asynchronous E3 to VC-3 mapping is shown in Figure 59.

Both the AU3 and TUG3 mapping modes are illustrated in Figure 61.

The overhead communications channel is inserted from the microprocessor interface via TDPR_MAP block. The insertion of the Overhead communication channel is only valid during DS3 operation. If the D3E3MA is operating in E3 mode, the Overhead Communication Channel is ignored.

10.33.4 DPLL

The Digital Phase Lock Loop (DPLL) tracks changes in frequency between the serial DS3/E3 clock and the SONET clock, and provides information to the mapper regarding stuff opportunities.

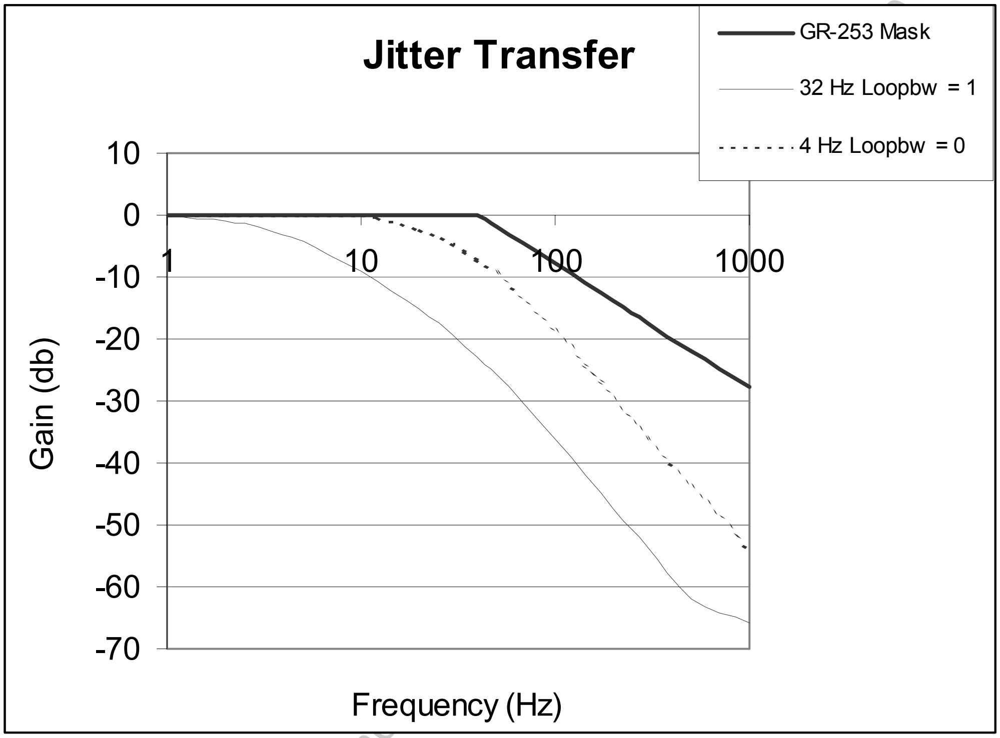
The DPLL has two modes for locking to the incoming signal: fast and normal. Under fast operation the loop bandwidth is increased causing the DPLL to lock more quickly to a change in frequency, but consequently the DPLL is less sensitive to small variations in frequency. The loop bandwidth can be selected via normal mode register bit LOOPBW.

10.33.5 Transfer Function

Jitter transfer is defined as the ratio of jitter on the output signal (DS3/E3 mapped into SONET) to the jitter applied to the input signal (serial DS3/E3). Requirements for jitter transfer are given in terms of a jitter transfer mask, which represents the maximum acceptable jitter gain (in dB) for a specified range of jitter frequencies.

Typical D3E3MA jitter transfer characteristics are show in the Figure 29.

Figure 29 Typical D3E3MA Jitter Transfer



The system (including the D3E3MA) intrinsic jitter, pointer jitter, jitter tolerance, mapping wander, and pointer wander characteristics are described in section 19.11 DS3/E3 Serial Interface Timing Characteristics.

The D3E3MA may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the D3E3MA. Access to these registers is via a generic microprocessor bus.

10.34 DS3 Transmitter

The DS3 Transmitter (T3-TRAN) Block integrates circuitry required to insert the overhead bits into a DS3 bit stream and produce a B3ZS-encoded signal. The T3-TRAN is directly compatible with the M23 and C-bit parity DS3 formats.

Status signals such as far end receive failure (FERF), the alarm indication signal, and the idle signal can be inserted when their transmission is enabled by internal register bits. FERF can also be automatically inserted on detection of any combination of LOS, OOF or RED, or AIS by the T3-FRMR.

A valid pair of P-bits is automatically calculated and inserted by the T3-TRAN. When C-bit parity mode is selected, the path parity bits and far end block error (FEBE) indications are automatically inserted.

When enabled for C-bit parity operation, the FEAC channel is sourced by the XBOC bit-oriented code transmitter. The path maintenance data link messages are sourced by the TDPR data link transmitter. These overhead signals can also be overwritten by using the TOH and TOHINS inputs.

When enabled for M23 operation, the C-bits are forced to logic 1 with the exception of the C-bit Parity ID bit (first C-bit of the first M-subframe), which is forced to toggle every M-frame.

The T3-TRAN supports diagnostic modes in which it inserts parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, or all-zeros.

User control of each of the overhead bits in the DS3 frame is provided. Overhead bits may be inserted on a bit-by-bit basis from a user supplied data stream. An overhead clock (at 526 kHz) and a DS3 overhead alignment output are provided to allow for control of the user provided stream.

10.35 E3 Transmitter

The E3 Transmitter (E3-TRAN) Block integrates circuitry required to insert the overhead bits into an E3 bit stream and produce an HDB3-encoded signal. The E3-TRAN is directly compatible with the G.751 and G.832 framing formats.

The E3-TRAN generates the frame alignment signal and inserts it into the incoming serial stream based on either the G.751 or G.832 formats and an alignment pulse applied to it by the SPLT block. All overhead and status bits in each frame format can be individually controlled by register bits or by the transmit overhead stream. While in certain framing format modes, the E3-TRAN generates various overhead bytes according to the following:

10.35.1 In G.832 E3 Format, the E3-TRAN:

1. Inserts the BIP-8 byte calculated over the preceding frame.

2. Inserts the Trail Trace bytes through the Trail Trace Buffer (TTB) block.

3. Inserts the FERF bit via a register bit or, optionally, when the E3-FRMR declares OOF, or when the loss of cell delineation (LCD) defect is declared.

4. Inserts the FEBE bit, which is set to logic 1 when one or more BIP-8 errors are detected by the receive framer. If there are no BIP-8 errors indicated by the E3-FRMR, the E3-TRAN sets the FEBE bit to logic 0.

5. Inserts the Payload Type bits based on the register value set by the microprocessor.

6. Inserts the Tributary Unit multi-frame indicator bits either via the TOH overhead stream or by register bit values set by the microprocessor.

7. Inserts the Timing Marker bit via a register bit.

8. Inserts the Network Operator (NR) byte from the TDPR block when the TNETOP bit in the Channel Data Link and FERF/RAI Control register is logic 1; otherwise, the NR byte is set to all ones. The NR byte can be overwritten by using the TOH and TOHINS input pins. All 8 bits of the Network Operator byte are available for use as a data link.

9. Inserts the General Purpose Communication Channel (GC) byte from the TDPR block when the TNETOP bit in the Channel Data Link and FERF/RAI Control register is logic 0; otherwise, the byte is set to all ones. The GC byte can be overwritten by using the TOH and TOHINS input pins.

10.35.2 In G.751 E3 Mode, the E3-TRAN:

1. Inserts the Remote Alarm Indication bit (bit 11 of the frame) either via a register bit or, optionally, when the E3-FRMR declares OOF.

2. Inserts the National Use reserved bit (bit 12 of the frame) either as a fixed value through a register bit or from the TDPR block as configured by the TNETOP bit in the Channel Data Link and FERF/RAI Control register and the NATUSE bit in the E3 TRAN Configuration register.

3. Optionally identifies the tributary justification bits and stuff opportunity bits as either overhead or payload to SPLT for payload mappings that take advantage of the full bandwidth.

4. Further, the E3-TRAN can provide insertion of bit errors in the framing pattern or in the parity bits, and insertion of single line code violations for diagnostic purposes. Most of the overhead bits can be overwritten by using the TOH and TOHINS input pins.

10.36 J2 Transmitter

The J2 Transmitter (J2-TRAN) Block integrates circuitry required to insert the overhead bits into a J2 bit stream and produce a B8ZS-encoded signal. The J2-TRAN is directly compatible with the framing format specified in G.704 and NTT Technical Reference for High-Speed Digital Leased Circuit Services.

The J2-TRAN generates the frame alignment signal and inserts it into the incoming serial stream. All overhead and status bits in each frame format can be individually controlled by either register bits or by the transmit overhead stream.

10.36.1 The J2-TRAN:

1. Inserts the CRC-5 bits calculated over the preceding multi-frame.

2. Inserts the x-bits through microprocessor programmable register bits.

3. Inserts the a-bit through a microprocessor programmable register bit.

4. Inserts the m-bit data link through the TDPR block.

5. Inserts payload AIS or physical layer AIS through microprocessor programmable register bits.

6. Inserts RAI over the m-bits, overwriting HDLC frames, by using the XBOC block or through automatic activation upon detection of certain remote alarm conditions.

The J2-TRAN allows overwriting of any of the overhead bits by using the TOH, TOHINS, TOHFA, and OHCLK overhead signals. Further, the J2-TRAN can provide insertion of single bit errors in the framing pattern or in the CRC-5 bits, and insertion of single line code violations for diagnostic purposes.

10.37 Bit Oriented Code Generator (XBOC)

The Bit Oriented Code Generator (XBOC) Block transmits 63 of the possible 64 bit oriented codes (BOC) in the C-bit parity Far End Alarm and Control (FEAC) channel. A BOC is a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. The code to be transmitted is programmed by writing the XBOC Code Register. The 64th code (111111) is similar to the HDLC idle sequence and is used to disable the transmission of any bit oriented codes. When transmission is disabled, the FEAC channel is set to all ones.

10.38 Trail Trace Buffer (TTB)

The Trail Trace Buffer (TTB) extracts and sources the trail trace message carried in the TR byte of the G.832 E3 stream. The message is used by the OS to prevent delivery of traffic from the wrong source and is 16 bytes in length. The 16-byte message is framed by the PTI Multi-frame Alignment Signal (TMFAS = 'b10000000 00000000). One bit of the TMFAS is placed in the most significant bit of each message byte. In the receive direction, the trail trace message is extracted from the serial overhead stream output by the E3-FRMR. The extracted message is stored in the internal RAM for review by an external microprocessor. By default, the TTB will write the byte of a 16-byte message with its most significant bit set high to the first location in the RAM. The extracted trail trace message is checked for consistency between consecutive multi-frames. A message received unchanged three or five times (programmable) is accepted for comparison with the copy previously written into the internal RAM by the external microprocessor. Alarms are raised to indicate reception of unstable and mismatched messages. In the transmit direction, the TTB sources the trail trace message from the internal RAM for insertion into the TR byte by the E3-TRAN.

The TTB also extracts the Payload Type label carried in the MA byte of the G.832 E3 stream. The label is used to ensure that the adaptation function at the trail termination sink is compatible with the adaptation function at the trail termination source. The Payload Type label is checked for consistency between consecutive multi-frames. A Payload Type label received unchanged for five frames is accepted for comparison with the copy previously written into the TTB by the external microprocessor. Alarms are raised to indicate reception of unstable and mismatched Payload Type label bits.

10.39 Facility Data Link Transmitter (TDPR)

The Facility Data Link Transmitter (TDPR) provides a serial data link for the C-bit parity path maintenance data link in DS3, the serial Network Operator byte or the General Purpose data link in G.832 E3, the National Use bit data link in G.751 E3, the m-bit data link in J2, the DS3 Mapping Overhead Communication Channel, or the Transmit SONET/SDH Path DCC Channel.

The TDPR is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag and abort sequence insertion. Upon completion of the message, a CRC-16.ISO-3309 frame check sequence (FCS) can be appended, followed by flags. If the TDPR transmit data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits flags (01111110) until data is ready to be transmitted. Data bytes to be transmitted are written into the TDPR Transmit Data Register. The TDPR automatically begins transmission of data when at least one complete packet is written into its FIFO. All complete packets of data will be transmitted if no error condition occurs. After the last data byte of a packet, if CRC insertion has been enabled, the CRC FCS and a flag are transmitted. If CRC insertion has not been enabled only a flag is transmitted. The TDPR then returns to the transmission of flag characters until the next packet is available for transmission. The TDPR will also force transmission of the FIFO data once the FIFO depth has surpassed the programmable upper limit threshold. Transmission commences regardless of whether or not a packet has been completely written into the FIFO. The user must be careful to avoid overfilling the FIFO. Underruns can only occur if the packet length is greater than the programmed upper limit threshold because, in such a case, transmission will begin before a complete packet is stored in the FIFO.

An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data. Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort sequences (01111111 sequence where the 0 is transmitted first) can be continuously transmitted at any time by setting a control bit. During packet transmission, an underrun situation can occur if data is not written to the TDPR Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted and the controlling processor is notified via the UDR register bit. An abort sequence will also be transmitted if the user overflows the FIFO with a packet of length greater than 128 bytes. Overflows where other complete packets are still stored in the FIFO will not generate an abort. Only the packet that caused the overflow is corrupted and an interrupt is generated to the user via the OVR register bit. The other packets remain unaffected.

When the TDPR is disabled, a logical 1 (Idle) is inserted in the path maintenance data link.

10.40 SMDS PLCP Layer Transmitter (SPLT)

The SMDS PLCP Layer Transmitter (SPLT) Block integrates circuitry to support DS1, DS3, E1, and G.751 E3 based PLCP frame insertion.

The SPLT automatically inserts the framing (A1, A2) and path overhead identification (POHID) octets and provides registers or automatic generation of the F1, B1, G1, M2, M1 and C1 octets.

Registers are provided for the path user channel octet (F1) and the path status octet (G1). The bit interleaved parity octet (B1) and the FEBE sub-field are automatically inserted.

The DQDB management information octets, M1 and M2 are generated. The type 0 and type 1 patterns described in TA-TSY-000772 are automatically inserted. The type 1 page counter may be reset using a register bit in the SPLT Configuration register. Note that this feature is not required for the ATM Forum compliant DS3 UNI. For this application, the M1 and M2 octets must be set to all zeros.

The PLCP transmit frame C1 cycle/stuff counter octet and the transmit stuffing pattern can be referenced to the REF8KI input pin. Alternately, a fixed stuffing pattern may be inserted into the C1 cycle/stuff counter octet. A looped timing operating mode is provided where the transmit PLCP timing is derived from the received timing. In this mode, the C1 stuffing is generated based on the received stuffing pattern as determined by the SPLR block. When DS1 or E1 PLCP format is enabled, the pattern 00H is inserted.

When DS3 PLCP format is enabled, the C1 octet indicates the phase of the 375 µs nibble stuffing opportunity cycle. During frame one of the three frame cycle, the pattern FFH is inserted in the C1 octet, indicating a 13 nibble trailer length. During frame two, the pattern 00H is inserted, indicating a 14 nibble trailer length. During frame three, the pattern 66H or 99H is inserted, indicating a 13 or 14 nibble trailer length respectively.

When configured for G.751 E3 PLCP frame format, the C1 octet is used to indicate the number of octets stuffed in the trailer. The following table shows the C1 octet pattern for each of the possible octet stuff lengths:

Stuff Length	C1(Hex)
17	3B
18	4F
19	75
20	9D
21	A7

The SPLT block generates a stuff length pattern of 18, 19 or 20 octets determined by the phase alignment of the start of the G.751 E3 frame and the start of the E3 PLCP frame. The REF8KI input is provisioned to loop time the PLCP transmit frame to an externally applied 8 kHz reference.

The Zn growth octets are set to 00H. The Zn octets may be inserted from an external device via the path overhead stream input, TPH.

10.41 Transmit Cell Processor (TXCP)

The Transmit Cell Processor (TXCP) Block integrates circuitry to support ATM cell payload scrambling, header check sequence (HCS) generation, and idle/unassigned cell generation.

The TXCP scrambles the cell payload field using the self synchronizing scrambler with polynomial $x^{43} + 1$. The header portion of the cells may optionally also be scrambled. Note that although cell payload scrambling is required by ITU-T Recommendation I.432, it may be disabled in the S/UNI-12xJET. The ATM Forum DS3 UNI specification also requires that cell payloads be scrambled for the DS3 physical layer interface. However, to ensure backwards compatibility with older equipment, the payload scrambling may be disabled.

The HCS is generated using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the calculated HCS octet as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432. The resultant octet optionally overwrites the HCS octet in the transmit cell. When the transmit FIFO is empty, the TXCP inserts idle/unassigned cells. The idle/unassigned cell header is fully programmable using five internal registers. Similarly, the 48 octet information field is programmed with an 8 bit repeating pattern using an internal register.

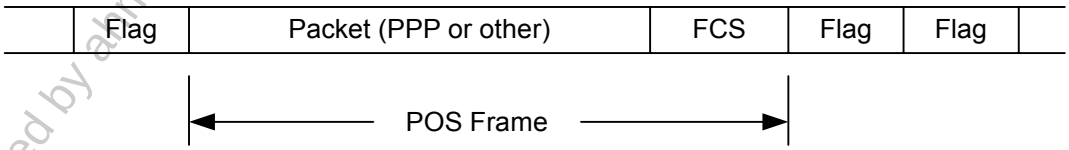
10.42 Transmit POS Frame Processor (TXFP)

The Transmit POS Frame Processor (TXFP) provides rate adaptation by transmitting flag sequences (0x7E) between packets, provides FCS generation and insertion, performs packet data scrambling, and provides performance monitoring functions.

10.42.1 POS Frame Generator

The POS Frame Generator uses the SONET/SDH sequencer to create the POS frames to be transmitted. The POS frame format is shown in Figure 30. Flags are inserted whenever the Transmit FIFO is empty and there is no data to transmit. When there is enough data to be transmitted, the block operates normally; it removes packets from the Transmit FIFO and transmits them. In addition, FCS generation, error insertion, byte stuffing, and scrambling can be optionally enabled.

Figure 30 Packet Over SONET/SDH Frame Format



In the event of a FIFO underflow caused by the FIFO being empty while a packet is being transmitted, the packet is aborted by transmitting the Abort Sequence. The Abort Sequence consists of an Escape Control character (0x7D) followed by the Flag Sequence (0x7E). Bytes associated with this aborted frame are still read from the FIFO but are discarded and replaced with the Flag Sequence in the outgoing data stream. Transmission of data resumes at the start of the next packet encountered in the FIFO data stream.

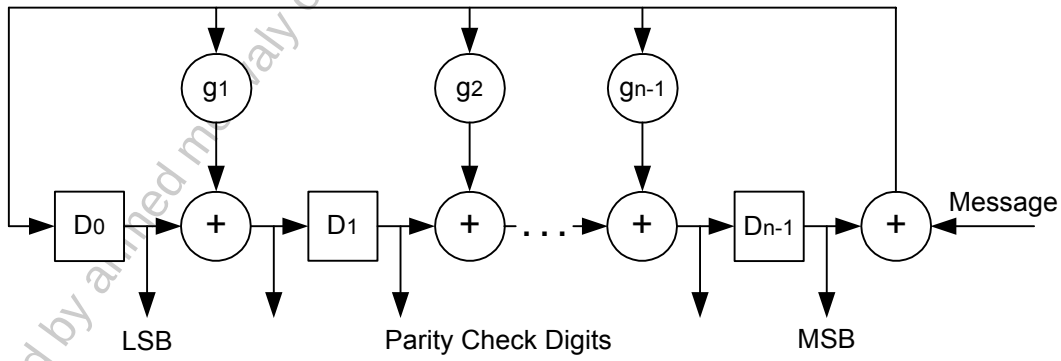
The POS Frame Generator also performs inter-packet gapping by inserting a programmable number of Flag Sequence characters between each POS frame transmission. Inter-packet gapping can be used to control the system effective data transmission rate if required.

For correct operation, the TXFP only supports packets ranging in size from 2 bytes to 65534 bytes in length.

10.42.2 FCS Generator

The FCS Generator performs a CRC-16.ISO-3309 or CRC-32 calculation on the whole POS frame before byte stuffing and data scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-16.ISO-3309 or CRC-32 function. The CRC-16.ISO-3309 is two bytes in size and has a generating polynomial $g(x) = 1 + x^5 + x^{12} + x^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(x) = 1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$. The first FCS bit transmitted is the coefficient of the highest term. When transmitting a packet from the Transmit FIFO, the FCS Generator appends the result after the last data byte, before the closing flag. Note that the Frame Check Sequence is the ones complement of the CRC register after calculation ends. FCS calculation and insertion can be disabled.

Figure 31 Byte HDLC CRC Generator



An error insertion mechanism is provided for system diagnosis purposes. Error insertion is performed by inverting the resulting FCS value before transmission. This will cause an FCS Error at the far end.

10.42.3 Byte Stuffing

The POS Frame generator provides transparency by performing byte stuffing. This operation is done after the FCS calculation. Two characters are being escaped, the Flag Sequence (0x7E) and the Escape Character itself (0x7D). When a character is being escaped, it is XORed with 0x20 before transmission and preceded by the Control Escape (0x7D) character.

Table 9 HDLC Byte Sequences

Data Value	Sequence
0x7E (Flag Sequence)	0x7D 0x5E
0x7D (Control Escape)	0x7D 0x5D
HDLC Abort Sequence	0x7D 0x7E

10.42.4 Data Scrambling

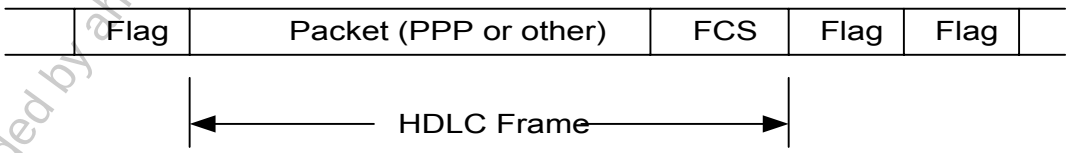
The Scrambler will optionally scramble the whole packet data, including the FCS and the flags. Scrambling is performed after the POS frame is formed using a parallel implementation of the self-synchronous scrambler polynomial, $x^{43}+1$. On reset, the scrambler is set to all ones to ensure scrambling on start-up. The scrambler may optionally be completely disabled. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

10.43 Transmit Bit HDLC Cell Processor (TXFP)

10.43.1 Bit HDLC Frame Generator

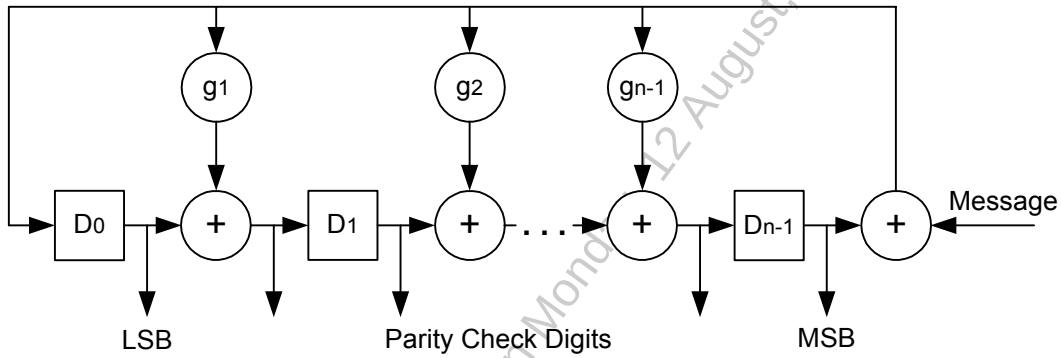
Figure 32 shows a diagram of the bit-synchronous HDLC protocol supported by TXFP. If the channel is provisioned for CRC generation, the FCS bytes are added to the packet information by TXFP. The resulting HDLC packet is bit stuffed which adds a "0" bit directly following five contiguous "1" bits. A HDLC packet is aborted when seven contiguous "1" bits (with no inserted "0" bits) are transmitted. Transmitting at least fifteen contiguous "1" bits (with no inserted "0" bits) is an HLDC idle. At least one flag sequence must exist at the start and end of each HDLC packet for packet delineation. Contiguous flag sequence or HDLC idle between packets is used as an "interframe time fill". Adjacent flag sequences do not share zeros.

Figure 32 Bit HDLC Frame Format



The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-16.ISO-3309 or CRC-32 function. Figure 33 shows a CRC encoder block diagram using the generating polynomial $g(X) = 1 + g_1X + g_2X^2 + \ldots + g_{n-1}X^{n-1} + X^n$. The CRC-16.ISO-3309 is two bytes in size and has a generating $g(X) = 1 + X^5 + X^{12} + X^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The first FCS bit transmitted is the coefficient of the highest term.

Figure 33 Bit HDLC CRC Generator



10.44 Transmit UTOPIA Level 2 ATM Interface

The UTOPIA Level 2 compatible interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication, and the parity bit (TPRTY), when data is written to the transmit FIFO (using the rising edges of TFCLK). The interface provides the transmit cell available status (TCA), which can transition from "available" to "unavailable" when the transmit FIFO is near full (when TCALEVEL0 is low) or when the FIFO is full (when TCALEVEL0 is high) and can accept no more writes. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells by the FIFODP[1:0] bits of the TXCP Configuration 2 register. If the programmed depth is less than four, more than one cell may be written after TCA is asserted as the TXCP still allows four cells to be stored in its FIFO.

This interface also indicates FIFO overruns via a maskable interrupt and register bit, but write accesses while TCA is low are not processed. The TXCP automatically transmits idle cells until a full cell is available to be transmitted.

10.45 Transmit POS-PHY Level 2 Interface

The POS-PHY Level 2 compatible interface is an extension to the UTOPIA 2 interface to allow for the transfer of packets. POS-PHY byte-level transfer mode is supported.

The TSOP signal is used to identify the start of a packet; the TPA signal notifies the system side that the transmit FIFO is not full (the POS processor will not start transmitting a packet until a programmable number of bytes for a single packet or the entire packet is in the FIFO; the TDAT[15:0] bus transfers the data to the FIFO from the system interface; the TPRTY signal determines the parity on the TDAT bus (selectable as odd or even parity); TFCLK is used to write words to the FIFO interface; and finally TENB is used to initiate writes to the transmit FIFO. The TXCP automatically transmits idle flag characters until sufficient data is available in the transmit FIFO to start transmission.

The TEOP signal (Transmit End of Packet) is used to identify the end of a packet. The TMOD signal (Transmit Mod) is provided to indicate whether 1 or 2 bytes of the final word transferred are valid (when TEOP is asserted). The TERR signal (Transmit Error) is provided to error a packet that has begun transmission (the packet will be aborted).

10.46 Transmit UTOPIA Level 3 Interface

The Transmit UTOPIA/POS-PHY Level 3 Interface (TUL3) provides FIFO management and the S/UNI-12xJET transmit cell interface. Each channel receive FIFO may contain up to sixteen cells. The FIFO depth may be programmed from 16 to 1 cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include emptying cells from the transmit FIFO, indicating when the transmit FIFO is full, maintaining the transmit FIFO read and write pointers, and detecting a FIFO overrun condition.

The UTOPIA Level 3 compatible interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication and the parity bit (TPRTY) when data is written to the transmit. The TADR[4:0] bus with TCA is used to poll the channel FIFOs for fill status. As well, channels are selected using the TADR[4:0] and falling edge of TENB. To reduce FIFO latency, the FIFO depth at which TCA indicates “full” can be set to one, two, three or four cells by the FIFODP[3:0] bits of the TUL3. If the programmed depth is less than 16, more than one cell may be written after TCA is asserted as the TUL3 still allows 16 cells to be stored in its FIFO.

The interface also indicates FIFO overruns via a maskable interrupt and register bits. The TXCP automatically transmits idle cells until a full cell is available to be transmitted.

10.47 Transmit POS-PHY Level 3 Interface

The Transmit UTOPIA/POS-PHY Level 3 Interface (TUL3) provides FIFO management at the S/UNI-12xJET transmit packet interface. Each channel transmit FIFO contains 1024 bytes. The FIFO provides the system rate decoupling function between the transmission system physical layer and the link layer, and handles timing differences caused by the insertion of escape characters.

The POS-PHY Level 3 compatible interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of packet (TSOP) indication, the end of packet (TEOP) indication, erred packet (TERR) indication and the parity bit (TPRTY) when data is written to the transmit FIFO (using the rising edges of the TFCLK). The TADR[4:0] bus with TPA is used to poll the channel FIFOs for fill status. As well, channels are selected using the TADR[4:0] and falling edge of TENB. The POS processor will not start transmitting a packet until a programmable number of bytes for a single packet or the entire packet is in the FIFO. A packet may be aborted by asserting the TERR signal at the end of the packet.

The interface also indicates FIFO overruns via a maskable interrupt and register bits. The TXCP automatically transmits idle flag characters until sufficient data is available in the transmit FIFO to start transmission.

10.48 Transmit TelecomBus Interface

The Output Parallel TelecomBus Interface maps payload on a SONET/SDH template of an STS-12/STM-4 bus. Markers for J0/J1 byte locations are given to signal the frame alignment. Payload and non-payload bytes are also marked appropriately. Alarm conditions can also be indicated on the interface. The interface is clocked with the 77.76 MHz OCLK. The output J0/J1 byte alignment on the parallel TelecomBus is aligned to the input OJ0REF signal. When used as a Drop TelecomBus (SPECTRA Mode), SPMACHB is set high, the outgoing clock OCLK_O may be used to clock the Drop TelecomBus Interface such that the line side (Receive SERDES PICLK) and Drop TelecomBus interface (OCLK) are synchronized.

10.49 Receive TelecomBus Interface

The input parallel TelecomBus Interface samples a SONET/SDH stream on an 8-bit STS-12/STM-4 bus. Markers for J0/J1 byte locations are given to indicate the frame alignment. Payload and non-payload bytes are also marked appropriately. AIS alarm conditions are also given on the interface. The interface is clocked with the 77.76 MHz ICLK. When used as an Add TelecomBus (SPECTRA Mode), SPMACHB is set high, the outgoing clock ICLK_O may be used to clock the Add TelecomBus Interface such that the line side (Transmit SERDES PTCLK) and Add TelecomBus interface (ICLK) are synchronized.

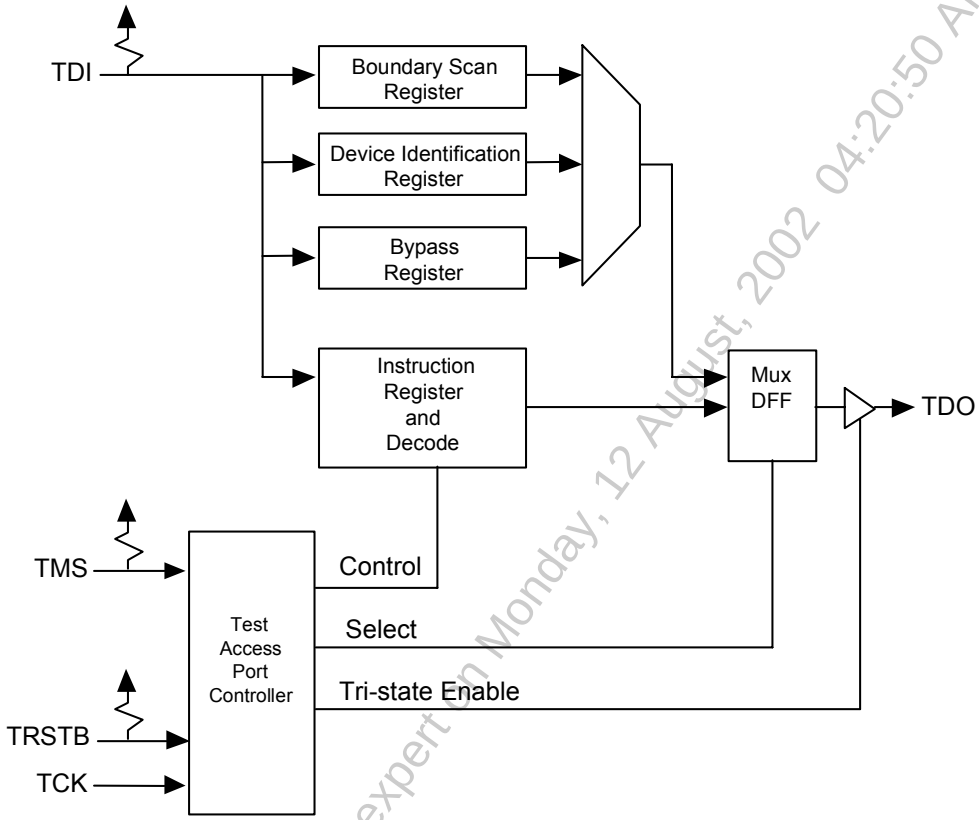
10.50 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-12xJET identification code is 053820CD hexadecimal when read from the JTAG port.

10.50.1 JTAG Support

The S/UNI-12xJET supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 34 Boundary Scan Architecture



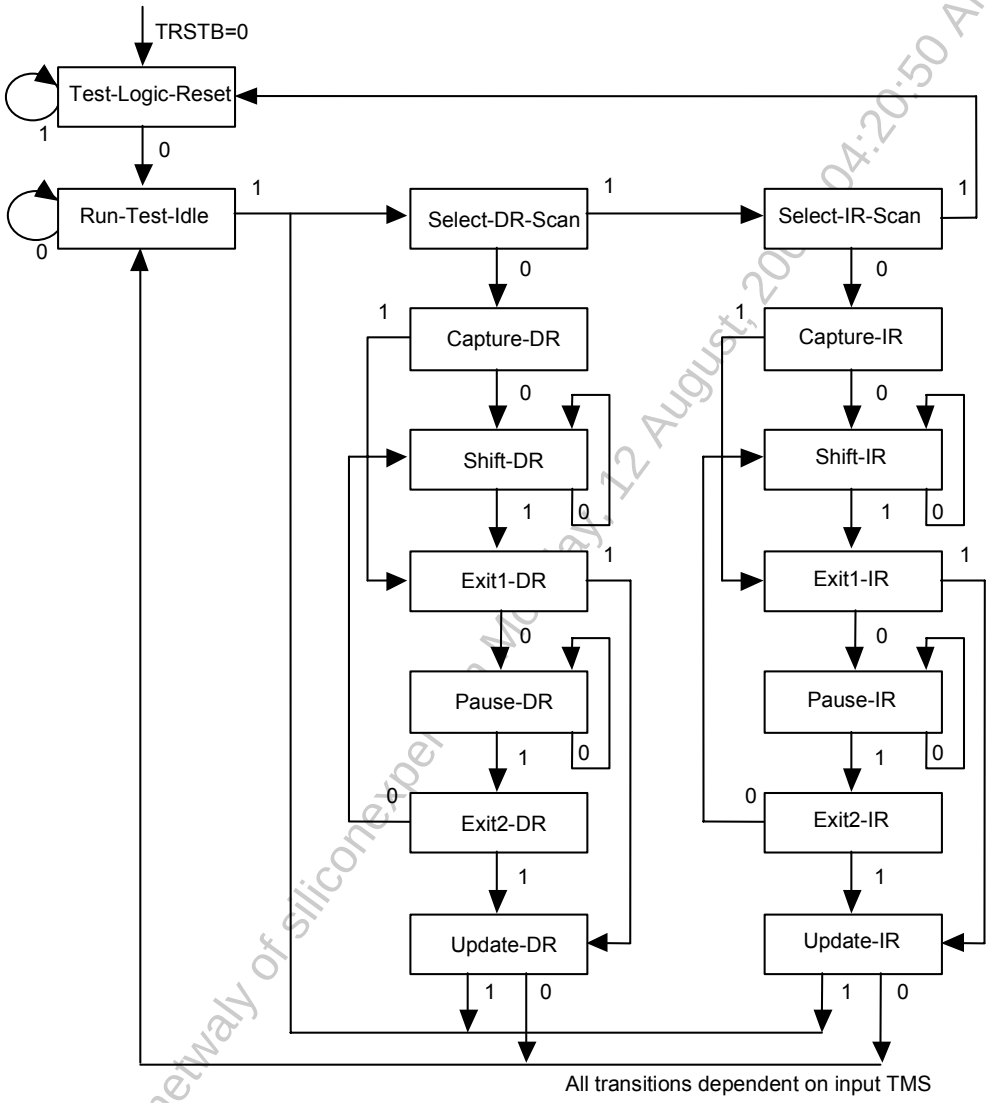
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

10.50.2 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 35 TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

10.50.3 Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

10.51 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-12xJET. The description for the Registers for the S/UNI-12xJET are located in PMC-2010960, Saturn User Network Interface (12xJET) Device for J2/E3/T3 Engineering Document Register Description.

For all register accesses, CSB must be low.

As show by the top level register map in Document PMC-2010960, the Level 3 System Interface registers are located together in memory similar to a channel interface. Document PMC-2010960 lists the registers for the Level 3 System Interface.

11 Normal Mode Register Description

Please refer to Document PMC-2012190 "Saturn User Network Interface (12xJET) Device for J2/E3/T3 Data Sheet Register Description" for register description.

12 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-12xJET. Test mode registers (as opposed to normal mode registers) are selected when A[13] is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-12xJET are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI-12xJET also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Please refer to Document PMC-2010960 "Saturn User Network Interface (12xJET) Device for J2/E3/T3 Engineering Document Register Description" for test register description.

12.1 JTAG Test Port

The S/UNI-12xJET JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 10 Instruction Register (Length - 3 Bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 11 Identification Register

Parameter	Value
Length	32 bits

Parameter	Value
Version Number	0H
Part Number	5382H
Manufacturer's Identification Code	0CDH
Device Identification	053820CDH

Table 12 Boundary Scan Register

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
FRAC[0]	635	IN_CELL	OEB_RALM	317	OUT_CELL
FRAC[1]	634	IN_CELL	RALM	316	OUT_CELL
REF8KI	633	IN_CELL	OEB_B3E	315	OUT_CELL
OEB_REF8KO	632	OUT_CELL	B3E	314	OUT_CELL
REF8KO	631	OUT_CELL	OEB_RSLDCLK	313	OUT_CELL
SMODE[0]	630	IN_CELL	RSLDCLK	312	OUT_CELL
SMODE[1]	629	IN_CELL	OEB_RSLD	311	OUT_CELL
SMODE[2]	628	IN_CELL	RSLD	310	OUT_CELL
TDAT[31]	627	IN_CELL	OEB_OOF	309	OUT_CELL
TDAT[30]	626	IN_CELL	OOF	308	OUT_CELL
TDAT[29]	625	IN_CELL	OEB_RSFPO	307	OUT_CELL
TDAT[28]	624	IN_CELL	RSFPO	306	OUT_CELL
TDAT[27]	623	IN_CELL	FPIN	305	IN_CELL
TDAT[26]	622	IN_CELL	PIN[0]	304	IN_CELL
TDAT[25]	621	IN_CELL	PIN[1]	303	IN_CELL
TDAT[24]	620	IN_CELL	PIN[2]	302	IN_CELL
TDAT[23]	619	IN_CELL	PIN[3]	301	IN_CELL
TDAT[22]	618	IN_CELL	PIN[4]	300	IN_CELL
TDAT[21]	617	IN_CELL	PIN[5]	299	IN_CELL
TDAT[20]	616	IN_CELL	PIN[6]	298	IN_CELL
TDAT[19]	615	IN_CELL	PIN[7]	297	IN_CELL
TDAT[18]	614	IN_CELL	PICLK	296	IN_CELL
TDAT[17]	613	IN_CELL	TSFPI	295	IN_CELL
TDAT[16]	612	IN_CELL	OEB_TSFPO	294	OUT_CELL
TDAT[15]	611	IN_CELL	TSFPO	293	OUT_CELL
TDAT[14]	610	IN_CELL	OEB_POUT[0]	292	OUT_CELL
TDAT[13]	609	IN_CELL	POUT[0]	291	OUT_CELL
TDAT[12]	608	IN_CELL	OEB_POUT[1]	290	OUT_CELL
TDAT[11]	607	IN_CELL	POUT[1]	289	OUT_CELL
TDAT[10]	606	IN_CELL	OEB_POUT[2]	288	OUT_CELL
TDAT[9]	605	IN_CELL	POUT[2]	287	OUT_CELL
TDAT[8]	604	IN_CELL	OEB_POUT[3]	286	OUT_CELL

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
TDAT[7]	603	IN_CELL	POUT[3]	285	OUT_CELL
TDAT[6]	602	IN_CELL	OEB_POUT[4]	284	OUT_CELL
TDAT[5]	601	IN_CELL	POUT[4]	283	OUT_CELL
TDAT[4]	600	IN_CELL	OEB_POUT[5]	282	OUT_CELL
TDAT[3]	599	IN_CELL	POUT[5]	281	OUT_CELL
TDAT[2]	598	IN_CELL	OEB_POUT[6]	280	OUT_CELL
TDAT[1]	597	IN_CELL	POUT[6]	279	OUT_CELL
TDAT[0]	596	IN_CELL	OEB_POUT[7]	278	OUT_CELL
TPRTY	595	IN_CELL	POUT[7]	277	OUT_CELL
TENB	594	IN_CELL	PTCLK	276	IN_CELL
TSOC_TSOP	593	IN_CELL	IALARM	275	IN_CELL
TEOP	592	IN_CELL	IDP	274	IN_CELL
TERR	591	IN_CELL	ID[7]	273	IN_CELL
TMOD[0]	590	IN_CELL	ID[6]	272	IN_CELL
TMOD[1]	589	IN_CELL	ID[5]	271	IN_CELL
TSX	588	IN_CELL	ID[4]	270	IN_CELL
OEB_STPA	587	OUT_CELL	ID[3]	269	IN_CELL
STPA	586	OUT_CELL	ID[2]	268	IN_CELL
OEB_TCA_PTPA	585	OUT_CELL	ID[1]	267	IN_CELL
TCA_PTPA	584	OUT_CELL	ID[0]	266	IN_CELL
TADR[0]	583	IN_CELL	IPL	265	IN_CELL
TADR[1]	582	IN_CELL	IJ0J1	264	IN_CELL
TADR[2]	581	IN_CELL	ICLK	263	IN_CELL
TADR[3]	580	IN_CELL	OEB_OALARM	262	OUT_CELL
TADR[4]	579	IN_CELL	OALARM	261	OUT_CELL
TFCLK	578	IN_CELL	OEB_ODP	260	OUT_CELL
OEB_RDAT[31]	577	OUT_CELL	ODP	259	OUT_CELL
RDAT[31]	576	OUT_CELL	OEB_OD[7]	258	OUT_CELL
OEB_RDAT[30]	575	OUT_CELL	OD[7]	257	OUT_CELL
RDAT[30]	574	OUT_CELL	OEB_OD[6]	256	OUT_CELL
OEB_RDAT[29]	573	OUT_CELL	OD[6]	255	OUT_CELL
RDAT[29]	572	OUT_CELL	OEB_ICLK_REF	254	OUT_CELL
OEB_RDAT[28]	571	OUT_CELL	ICLK_REF	253	OUT_CELL
RDAT[28]	570	OUT_CELL	OEB_OD[5]	252	OUT_CELL
OEB_RDAT[27]	569	OUT_CELL	OD[5]	251	OUT_CELL
RDAT[27]	568	OUT_CELL	OEB_OD[4]	250	OUT_CELL
OEB_RDAT[26]	567	OUT_CELL	OD[4]	249	OUT_CELL
RDAT[26]	566	OUT_CELL	OEB_OD[3]	248	OUT_CELL
OEB_RDAT[25]	565	OUT_CELL	OD[3]	247	OUT_CELL

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
RDAT[25]	564	OUT_CELL	OEB_OD[2]	246	OUT_CELL
OEB_RDAT[24]	563	OUT_CELL	OD[2]	245	OUT_CELL
RDAT[24]	562	OUT_CELL	OEB_OD[1]	244	OUT_CELL
OEB_RDAT[23]	561	OUT_CELL	OD[1]	243	OUT_CELL
RDAT[23]	560	OUT_CELL	OEB_OD[0]	242	OUT_CELL
OEB_RDAT[22]	559	OUT_CELL	OD[0]	241	OUT_CELL
RDAT[22]	558	OUT_CELL	OEB_OPL	240	OUT_CELL
OEB_RDAT[21]	557	OUT_CELL	OPL	239	OUT_CELL
RDAT[21]	556	OUT_CELL	OEB_OJ0J1	238	OUT_CELL
OEB_RDAT[20]	555	OUT_CELL	OJ0J1	237	OUT_CELL
RDAT[20]	554	OUT_CELL	OEB_OSTSEN	236	OUT_CELL
OEB_RDAT[19]	553	OUT_CELL	OSTSEN	235	OUT_CELL
RDAT[19]	552	OUT_CELL	OEB_OCLK_REF	234	OUT_CELL
OEB_RDAT[18]	551	OUT_CELL	OCLK_REF	233	OUT_CELL
RDAT[18]	550	OUT_CELL	OCLK	232	IN_CELL
OEB_RDAT[17]	549	OUT_CELL	OJ0REF	231	IN_CELL
RDAT[17]	548	OUT_CELL	SPMACHB	230	IN_CELL
OEB_RDAT[16]	547	OUT_CELL	CSB	229	IN_CELL
RDAT[16]	546	OUT_CELL	WRB	228	IN_CELL
OEB_RDAT[15]	545	OUT_CELL	RDB	227	IN_CELL
RDAT[15]	544	OUT_CELL	OEB_D[0]	226	OUT_CELL
OEB_RDAT[14]	543	OUT_CELL	D[0]	225	IO_CELL
RDAT[14]	542	OUT_CELL	OEB_D[1]	224	OUT_CELL
OEB_RDAT[13]	541	OUT_CELL	D[1]	223	IO_CELL
RDAT[13]	540	OUT_CELL	OEB_D[2]	222	OUT_CELL
OEB_RDAT[12]	539	OUT_CELL	D[2]	221	IO_CELL
RDAT[12]	538	OUT_CELL	OEB_D[3]	220	OUT_CELL
OEB_RDAT[11]	537	OUT_CELL	D[3]	219	IO_CELL
RDAT[11]	536	OUT_CELL	OEB_D[4]	218	OUT_CELL
OEB_RDAT[10]	535	OUT_CELL	D[4]	217	IO_CELL
RDAT[10]	534	OUT_CELL	OEB_D[5]	216	OUT_CELL
OEB_RDAT[9]	533	OUT_CELL	D[5]	215	IO_CELL
RDAT[9]	532	OUT_CELL	OEB_D[6]	214	OUT_CELL
OEB_RDAT[8]	531	OUT_CELL	D[6]	213	IO_CELL
RDAT[8]	530	OUT_CELL	OEB_D[7]	212	OUT_CELL
OEB_RDAT[7]	529	OUT_CELL	D[7]	211	IO_CELL
RDAT[7]	528	OUT_CELL	OEB_D[8]	210	OUT_CELL
OEB_RDAT[6]	527	OUT_CELL	D[8]	209	IO_CELL
RDAT[6]	526	OUT_CELL	OEB_D[9]	208	OUT_CELL

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
OEB_RDAT[5]	525	OUT_CELL	D[9]	207	IO_CELL
RDAT[5]	524	OUT_CELL	OEB_D[10]	206	OUT_CELL
OEB_RDAT[4]	523	OUT_CELL	D[10]	205	IO_CELL
RDAT[4]	522	OUT_CELL	OEB_D[11]	204	OUT_CELL
OEB_RDAT[3]	521	OUT_CELL	D[11]	203	IO_CELL
RDAT[3]	520	OUT_CELL	OEB_D[12]	202	OUT_CELL
OEB_RDAT[2]	519	OUT_CELL	D[12]	201	IO_CELL
RDAT[2]	518	OUT_CELL	OEB_D[13]	200	OUT_CELL
OEB_RDAT[1]	517	OUT_CELL	D[13]	199	IO_CELL
RDAT[1]	516	OUT_CELL	OEB_D[14]	198	OUT_CELL
OEB_RDAT[0]	515	OUT_CELL	D[14]	197	IO_CELL
RDAT[0]	514	OUT_CELL	OEB_D[15]	196	OUT_CELL
OEB_RPRTY	513	OUT_CELL	D[15]	195	IO_CELL
RPRTY	512	OUT_CELL	A[0]	194	IN_CELL
OEB_RSOC_RSOP	511	OUT_CELL	A[1]	193	IN_CELL
RSOC_RSOP	510	OUT_CELL	A[2]	192	IN_CELL
OEB_REOP	509	OUT_CELL	A[3]	191	IN_CELL
REOP	508	OUT_CELL	A[4]	190	IN_CELL
OEB_RERR	507	OUT_CELL	A[5]	189	IN_CELL
RERR	506	OUT_CELL	A[6]	188	IN_CELL
OEB_RMOD[0]	505	OUT_CELL	A[7]	187	IN_CELL
RMOD[0]	504	OUT_CELL	A[8]	186	IN_CELL
OEB_RMOD[1]	503	OUT_CELL	A[9]	185	IN_CELL
RMOD[1]	502	OUT_CELL	A[10]	184	IN_CELL
OEB_RSX	501	OUT_CELL	A[11]	183	IN_CELL
RSX	500	OUT_CELL	A[12]	182	IN_CELL
OEB_RCA_RPA	499	OUT_CELL	A[13]	181	IN_CELL
RCA_RPA	498	OUT_CELL	A[14]	180	IN_CELL
OEB_RCA_RVAL	497	OUT_CELL	ALE	179	IN_CELL
RCA_RVAL	496	OUT_CELL	OEB_INTB	178	OUT_CELL
RADR[0]	495	IN_CELL	INTB	177	OUT_CELL
RADR[1]	494	IN_CELL	RCLK_IFBWCLK[5]	176	IN_CELL
RADR[2]	493	IN_CELL	RPOS_RDATI_IFBWDAT[5]	175	IN_CELL
RADR[3]	492	IN_CELL	RNEG_RLCV_ROHM_IFBWEN[5]	174	IN_CELL
RADR[4]	491	IN_CELL	TICLK_IFBWCLK[5]	173	IN_CELL
RENB	490	IN_CELL	TDATI_IFBWDAT[5]	172	IN_CELL
RFCLK	489	IN_CELL	TIOHM_TFPI_TMFPI_IFBWEN[5]	171	IN_CELL

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
DS3_REFCLK	488	IN_CELL	OEB_TCLK_EFBWCLK[5]	170	OUT_CELL
E3_REFCLK	487	IN_CELL	TCLK_EFBWCLK[5]	169	IO_CELL
RCLK_IFBWCLK[6]	486	IN_CELL	OEB_TPOS_TDATO_EFBWDAT[5]	168	OUT_CELL
RPOS_RDATI_IFBWDAT[6]	485	IN_CELL	TPOS_TDATO_EFBWDAT[5]	167	OUT_CELL
RNEG_RLCV_ROHM_IFBWEN[6]	484	IN_CELL	OEB_TNEG_TOHM_EFBWEN[5]	166	OUT_CELL
TICLK_IFBWCLK[6]	483	IN_CELL	TNEG_TOHM_EFBWEN[5]	165	OUT_CELL
TDATI_IFBWDAT[6]	482	IN_CELL	OEB_TFPO_TMFPO[5]	164	OUT_CELL
TIOHM_TFPI_TMFPI_IFBWEN[6]	481	IN_CELL	TFPO_TMFPO[5]	163	OUT_CELL
OEB_TCLK_EFBWCLK[6]	480	OUT_CELL	OEB_RSCLK_EFBWCLK[5]	162	OUT_CELL
TCLK_EFBWCLK[6]	479	IO_CELL	RSCLK_EFBWCLK[5]	161	IO_CELL
OEB_TPOS_TDATO_EFBWDAT[6]	478	OUT_CELL	OEB_RDATO_EFBWDAT[5]	160	OUT_CELL
TPOS_TDATO_EFBWDAT[6]	477	OUT_CELL	RDATO_EFBWDAT[5]	159	OUT_CELL
OEB_TNEG_TOHM_EFBWEN[6]	476	OUT_CELL	OEB_RFPO_RMFPO_EFBWEN[5]	158	OUT_CELL
TNEG_TOHM_EFBWEN[6]	475	OUT_CELL	RFPO_RMFPO_EFBWEN[5]	157	OUT_CELL
OEB_TFPO_TMFPO[6]	474	OUT_CELL	OEB_ROVRHD_EFBWDREQ[5]	156	OUT_CELL
TFPO_TMFPO[6]	473	OUT_CELL	ROVRHD_EFBWDREQ[5]	155	IO_CELL
OEB_RSCLK_EFBWCLK[6]	472	OUT_CELL	OEB_FRMSTAT[5]	154	OUT_CELL
RSCLK_EFBWCLK[6]	471	IO_CELL	FRMSTAT[5]	153	OUT_CELL
OEB_RDATO_EFBWDAT[6]	470	OUT_CELL	OEB_FRMSTAT[4]	152	OUT_CELL
RDATO_EFBWDAT[6]	469	OUT_CELL	FRMSTAT[4]	151	OUT_CELL
OEB_RFPO_RMFPO_EFBWEN[6]	468	OUT_CELL	OEB_ROVRHD_EFBWDREQ[4]	150	OUT_CELL
RFPO_RMFPO_EFBWEN[6]	467	OUT_CELL	ROVRHD_EFBWDREQ[4]	149	IO_CELL
OEB_ROVRHD_EFBWDREQ[6]	466	OUT_CELL	OEB_RFPO_RMFPO_EFBWEN[4]	148	OUT_CELL
ROVRHD_EFBWDREQ[6]	465	IO_CELL	RFPO_RMFPO_EFBWEN[4]	147	OUT_CELL
OEB_FRMSTAT[6]	464	OUT_CELL	OEB_RDATO_EFBWDAT[4]	146	OUT_CELL
FRMSTAT[6]	463	OUT_CELL	RDATO_EFBWDAT[4]	145	OUT_CELL

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
OEB_FRMSTAT[7]	462	OUT_CELL	OEB_RSCLK_EFBWCLK[4]	144	OUT_CELL
FRMSTAT[7]	461	OUT_CELL	RSCLK_EFBWCLK[4]	143	IO_CELL
OEB_ROVRHD_EFBWDREQ[7]	460	OUT_CELL	OEB_TFPO_TMFPO[4]	142	OUT_CELL
ROVRHD_EFBWDREQ[7]	459	IO_CELL	TFPO_TMFPO[4]	141	OUT_CELL
OEB_RFPO_RMFPO_EFBWEN[7]	458	OUT_CELL	OEB_TNEG_TOHM_EFBWEN[4]	140	OUT_CELL
RFPO_RMFPO_EFBWEN[7]	457	OUT_CELL	TNEG_TOHM_EFBWEN[4]	139	OUT_CELL
OEB_RDATO_EFBWDAT[7]	456	OUT_CELL	OEB_TPOS_TDATO_EFBWDAT[4]	138	OUT_CELL
RDATO_EFBWDAT[7]	455	OUT_CELL	TPOS_TDATO_EFBWDAT[4]	137	OUT_CELL
OEB_RSCLK_EFBWCLK[7]	454	OUT_CELL	OEB_TCLK_EFBWCLK[4]	136	OUT_CELL
RSCLK_EFBWCLK[7]	453	IO_CELL	TCLK_EFBWCLK[4]	135	IO_CELL
OEB_TFPO_TMFPO[7]	452	OUT_CELL	TIOHM_TFPI_TMFPI_IFBWEN[4]	134	IN_CELL
TFPO_TMFPO[7]	451	OUT_CELL	TDATI_IFBWDAT[4]	133	IN_CELL
OEB_TNEG_TOHM_EFBWEN[7]	450	OUT_CELL	TICLK_IFBWCLK[4]	132	IN_CELL
TNEG_TOHM_EFBWEN[7]	449	OUT_CELL	RNEG_RLCV_ROHM_IFBWEN[4]	131	IN_CELL
OEB_TPOS_TDATO_EFBWDAT[7]	448	OUT_CELL	RPOS_RDATI_IFBWDAT[4]	130	IN_CELL
TPOS_TDATO_EFBWDAT[7]	447	OUT_CELL	RCLK_IFBWCLK[4]	129	IN_CELL
OEB_TCLK_EFBWCLK[7]	446	OUT_CELL	RCLK_IFBWCLK[3]	128	IN_CELL
TCLK_EFBWCLK[7]	445	IO_CELL	RPOS_RDATI_IFBWDAT[3]	127	IN_CELL
TIOHM_TFPI_TMFPI_IFBWEN[7]	444	IN_CELL	RNEG_RLCV_ROHM_IFBWEN[3]	126	IN_CELL
TDATI_IFBWDAT[7]	443	IN_CELL	TICLK_IFBWCLK[3]	125	IN_CELL
TICLK_IFBWCLK[7]	442	IN_CELL	TDATI_IFBWDAT[3]	124	IN_CELL
RNEG_RLCV_ROHM_IFBWEN[7]	441	IN_CELL	TIOHM_TFPI_TMFPI_IFBWEN[3]	123	IN_CELL
RPOS_RDATI_IFBWDAT[7]	440	IN_CELL	OEB_TCLK_EFBWCLK[3]	122	OUT_CELL
RCLK_IFBWCLK[7]	439	IN_CELL	TCLK_EFBWCLK[3]	121	IO_CELL
RCLK_IFBWCLK[8]	438	IN_CELL	OEB_TPOS_TDATO_EFBWDAT[3]	120	OUT_CELL
RPOS_RDATI_IFBWDAT[8]	437	IN_CELL	TPOS_TDATO_EFBWDAT[3]	119	OUT_CELL

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
RNEG_RLCV_ROHM_IFBWEN[8]	436	IN_CELL	OEB_TNEG_TOHM_EFBWEN[3]	118	OUT_CELL
TICLK_IFBWCLK[8]	435	IN_CELL	TNEG_TOHM_EFBWEN[3]	117	OUT_CELL
TDATI_IFBWDAT[8]	434	IN_CELL	OEB_TFPO_TMFPO[3]	116	OUT_CELL
TIOHM_TFPI_TMFPI_IFBWEN[8]	433	IN_CELL	TFPO_TMFPO[3]	115	OUT_CELL
OEB_TCLK_EFBWCLK[8]	432	OUT_CELL	OEB_RSCLK_EFBWCLK[3]	114	OUT_CELL
TCLK_EFBWCLK[8]	431	IO_CELL	RSCLK_EFBWCLK[3]	113	IO_CELL
OEB_TPOS_TDATO_EFBWDAT[8]	430	OUT_CELL	OEB_RDATO_EFBWDAT[3]	112	OUT_CELL
TPOS_TDATO_EFBWDAT[8]	429	OUT_CELL	RDATO_EFBWDAT[3]	111	OUT_CELL
OEB_TNEG_TOHM_EFBWEN[8]	428	OUT_CELL	OEB_RFPO_RMFPO_EFBWEN[3]	110	OUT_CELL
TNEG_TOHM_EFBWEN[8]	427	OUT_CELL	RFPO_RMFPO_EFBWEN[3]	109	OUT_CELL
OEB_TFPO_TMFPO[8]	426	OUT_CELL	OEB_ROVRHD_EFBWDREQ[3]	108	OUT_CELL
TFPO_TMFPO[8]	425	OUT_CELL	ROVRHD_EFBWDREQ[3]	107	IO_CELL
OEB_RSCLK_EFBWCLK[8]	424	OUT_CELL	OEB_FRMSTAT[3]	106	OUT_CELL
RSCLK_EFBWCLK[8]	423	IO_CELL	FRMSTAT[3]	105	OUT_CELL
OEB_RDATO_EFBWDAT[8]	422	OUT_CELL	OEB_FRMSTAT[2]	104	OUT_CELL
RDATO_EFBWDAT[8]	421	OUT_CELL	FRMSTAT[2]	103	OUT_CELL
OEB_RFPO_RMFPO_EFBWEN[8]	420	OUT_CELL	OEB_ROVRHD_EFBWDREQ[2]	102	OUT_CELL
RFPO_RMFPO_EFBWEN[8]	419	OUT_CELL	ROVRHD_EFBWDREQ[2]	101	IO_CELL
OEB_ROVRHD_EFBWDREQ[8]	418	OUT_CELL	OEB_RFPO_RMFPO_EFBWEN[2]	100	OUT_CELL
ROVRHD_EFBWDREQ[8]	417	IO_CELL	RFPO_RMFPO_EFBWEN[2]	99	OUT_CELL
OEB_FRMSTAT[8]	416	OUT_CELL	OEB_RDATO_EFBWDAT[2]	98	OUT_CELL
FRMSTAT[8]	415	OUT_CELL	RDATO_EFBWDAT[2]	97	OUT_CELL
OEB_FRMSTAT[9]	414	OUT_CELL	OEB_RSCLK_EFBWCLK[2]	96	OUT_CELL
FRMSTAT[9]	413	OUT_CELL	RSCLK_EFBWCLK[2]	95	IO_CELL
OEB_ROVRHD_EFBWDREQ[9]	412	OUT_CELL	OEB_TFPO_TMFPO[2]	94	OUT_CELL
ROVRHD_EFBWDREQ[9]	411	IO_CELL	TFPO_TMFPO[2]	93	OUT_CELL

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
OEB_RFPO_RMFPO_EFBWEN[9]	410	OUT_CELL	OEB_TNEG_TOHM_EFBWEN[2]	92	OUT_CELL
RFPO_RMFPO_EFBWEN[9]	409	OUT_CELL	TNEG_TOHM_EFBWEN[2]	91	OUT_CELL
OEB_RDATO_EFBWDAT[9]	408	OUT_CELL	OEB_TPOS_TDATO_EFBWDAT[2]	90	OUT_CELL
RDATO_EFBWDAT[9]	407	OUT_CELL	TPOS_TDATO_EFBWDAT[2]	89	OUT_CELL
OEB_RSCLK_EFBWCLK[9]	406	OUT_CELL	OEB_TCLK_EFBWCLK[2]	88	OUT_CELL
RSCLK_EFBWCLK[9]	405	IO_CELL	TCLK_EFBWCLK[2]	87	IO_CELL
OEB_TFPO_TMFPO[9]	404	OUT_CELL	TIOHM_TFPI_TMFPI_IFBWEN[2]	86	IN_CELL
TFPO_TMFPO[9]	403	OUT_CELL	TDATI_IFBWDAT[2]	85	IN_CELL
OEB_TNEG_TOHM_EFBWEN[9]	402	OUT_CELL	TICLK_IFBWCLK[2]	84	IN_CELL
TNEG_TOHM_EFBWEN[9]	401	OUT_CELL	RNEG_RLCV_ROHM_IFBWEN[2]	83	IN_CELL
OEB_TPOS_TDATO_EFBWDAT[9]	400	OUT_CELL	RPOS_RDATI_IFBWDAT[2]	82	IN_CELL
TPOS_TDATO_EFBWDAT[9]	399	OUT_CELL	RCLK_IFBWCLK[2]	81	IN_CELL
OEB_TCLK_EFBWCLK[9]	398	OUT_CELL	RCLK_IFBWCLK[1]	80	IN_CELL
TCLK_EFBWCLK[9]	397	IO_CELL	RPOS_RDATI_IFBWDAT[1]	79	IN_CELL
TIOHM_TFPI_TMFPI_IFBWEN[9]	396	IN_CELL	RNEG_RLCV_ROHM_IFBWEN[1]	78	IN_CELL
TDATI_IFBWDAT[9]	395	IN_CELL	TICLK_IFBWCLK[1]	77	IN_CELL
TICLK_IFBWCLK[9]	394	IN_CELL	TDATI_IFBWDAT[1]	76	IN_CELL
RNEG_RLCV_ROHM_IFBWEN[9]	393	IN_CELL	TIOHM_TFPI_TMFPI_IFBWEN[1]	75	IN_CELL
RPOS_RDATI_IFBWDAT[9]	392	IN_CELL	OEB_TCLK_EFBWCLK[1]	74	OUT_CELL
RCLK_IFBWCLK[9]	391	IN_CELL	TCLK_EFBWCLK[1]	73	IO_CELL
RCLK_IFBWCLK[10]	390	IN_CELL	OEB_TPOS_TDATO_EFBWDAT[1]	72	OUT_CELL
RPOS_RDATI_IFBWDAT[10]	389	IN_CELL	TPOS_TDATO_EFBWDAT[1]	71	OUT_CELL
RNEG_RLCV_ROHM_IFBWEN[10]	388	IN_CELL	OEB_TNEG_TOHM_EFBWEN[1]	70	OUT_CELL
TICLK_IFBWCLK[10]	387	IN_CELL	TNEG_TOHM_EFBWEN[1]	69	OUT_CELL
TDATI_IFBWDAT[10]	386	IN_CELL	OEB_TFPO_TMFPO[1]	68	OUT_CELL
TIOHM_TFPI_TMFPI_IFBWEN[10]	385	IN_CELL	TFPO_TMFPO[1]	67	OUT_CELL

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
OEB_TCLK_EFBWCLK[10]	384	OUT_CELL	OEB_RSCLK_EFBWCLK[1]	66	OUT_CELL
TCLK_EFBWCLK[10]	383	IO_CELL	RSCLK_EFBWCLK[1]	65	IO_CELL
OEB_TPOS_TDATO_EFBWDAT[10]	382	OUT_CELL	OEB_RDATO_EFBWDAT[1]	64	OUT_CELL
TPOS_TDATO_EFBWDAT[10]	381	OUT_CELL	RDATO_EFBWDAT[1]	63	OUT_CELL
OEB_TNEG_TOHM_EFBWEN[10]	380	OUT_CELL	OEB_RFPO_RMFPO_EFBWEN[1]	62	OUT_CELL
TNEG_TOHM_EFBWEN[10]	379	OUT_CELL	RFPO_RMFPO_EFBWEN[1]	61	OUT_CELL
OEB_TFPO_TMFPO[10]	378	OUT_CELL	OEB_ROVRHD_EFBWDREQ[1]	60	OUT_CELL
TFPO_TMFPO[10]	377	OUT_CELL	ROVRHD_EFBWDREQ[1]	59	IO_CELL
OEB_RSCLK_EFBWCLK[10]	376	OUT_CELL	OEB_FRMSTAT[1]	58	OUT_CELL
RSCLK_EFBWCLK[10]	375	IO_CELL	FRMSTAT[1]	57	OUT_CELL
OEB_RDATO_EFBWDAT[10]	374	OUT_CELL	OEB_FRMSTAT[0]	56	OUT_CELL
RDATO_EFBWDAT[10]	373	OUT_CELL	FRMSTAT[0]	55	OUT_CELL
OEB_RFPO_RMFPO_EFBWEN[10]	372	OUT_CELL	OEB_ROVRHD_EFBWDREQ[0]	54	OUT_CELL
RFPO_RMFPO_EFBWEN[10]	371	OUT_CELL	ROVRHD_EFBWDREQ[0]	53	IO_CELL
OEB_ROVRHD_EFBWDREQ[10]	370	OUT_CELL	OEB_RFPO_RMFPO_EFBWEN[0]	52	OUT_CELL
ROVRHD_EFBWDREQ[10]	369	IO_CELL	RFPO_RMFPO_EFBWEN[0]	51	OUT_CELL
OEB_FRMSTAT[10]	368	OUT_CELL	OEB_RDATO_EFBWDAT[0]	50	OUT_CELL
FRMSTAT[10]	367	OUT_CELL	RDATO_EFBWDAT[0]	49	OUT_CELL
OEB_FRMSTAT[11]	366	OUT_CELL	OEB_RSCLK_EFBWCLK[0]	48	OUT_CELL
FRMSTAT[11]	365	OUT_CELL	RSCLK_EFBWCLK[0]	47	IO_CELL
OEB_ROVRHD_EFBWDREQ[11]	364	OUT_CELL	OEB_TFPO_TMFPO[0]	46	OUT_CELL
ROVRHD_EFBWDREQ[11]	363	IO_CELL	TFPO_TMFPO[0]	45	OUT_CELL
OEB_RFPO_RMFPO_EFBWEN[11]	362	OUT_CELL	OEB_TNEG_TOHM_EFBWEN[0]	44	OUT_CELL
RFPO_RMFPO_EFBWEN[11]	361	OUT_CELL	TNEG_TOHM_EFBWEN[0]	43	OUT_CELL
OEB_RDATO_EFBWDAT[11]	360	OUT_CELL	OEB_TPOS_TDATO_EFBWDAT[0]	42	OUT_CELL
RDATO_EFBWDAT[11]	359	OUT_CELL	TPOS_TDATO_EFBWDAT[0]	41	OUT_CELL

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
OEB_RSCLK_EFBWCLK[11]	358	OUT_CELL	OEB_TCLK_EFBWCLK[0]	40	OUT_CELL
RSCLK_EFBWCLK[11]	357	IO_CELL	TCLK_EFBWCLK[0]	39	IO_CELL
OEB_TFPO_TMFPO[11]	356	OUT_CELL	TIOHM_TFPI_TMFPI_IFBWEN[0]	38	IN_CELL
TFPO_TMFPO[11]	355	OUT_CELL	TDATI_IFBWDAT[0]	37	IN_CELL
OEB_TNEG_TOHM_EFBWEN[11]	354	OUT_CELL	TICLK_IFBWCLK[0]	36	IN_CELL
TNEG_TOHM_EFBWEN[11]	353	OUT_CELL	RNEG_RLCV_ROHM_IFBWEN[0]	35	IN_CELL
OEB_TPOS_TDATO_EFBWDAT[11]	352	OUT_CELL	RPOS_RDATI_IFBWDAT[0]	34	IN_CELL
TPOS_TDATO_EFBWDAT[11]	351	OUT_CELL	RCLK_IFBWCLK[0]	33	IN_CELL
OEB_TCLK_EFBWCLK[11]	350	OUT_CELL	OHCLK	32	IN_CELL
TCLK_EFBWCLK[11]	349	IO_CELL	OEB_OHCH[0]	31	OUT_CELL
TIOHM_TFPI_TMFPI_IFBWEN[11]	348	IN_CELL	OHCH[0]	30	OUT_CELL
TDATI_IFBWDAT[11]	347	IN_CELL	OEB_OHCH[1]	29	OUT_CELL
TICLK_IFBWCLK[11]	346	IN_CELL	OHCH[1]	28	OUT_CELL
RNEG_RLCV_ROHM_IFBWEN[11]	345	IN_CELL	OEB_OHCH[2]	27	OUT_CELL
RPOS_RDATI_IFBWDAT[11]	344	IN_CELL	OHCH[2]	26	OUT_CELL
RCLK_IFBWCLK[11]	343	IN_CELL	OEB_OHCH[3]	25	OUT_CELL
TTOH	342	IN_CELL	OHCH[3]	24	OUT_CELL
TTOHEN	341	IN_CELL	OEB_TOHVAL	23	OUT_CELL
TPOH	340	IN_CELL	TOHVAL	22	OUT_CELL
TPOHEN	339	IN_CELL	OEB_TOHFA	21	OUT_CELL
OEB_TOHCLK	338	OUT_CELL	TOHFA	20	OUT_CELL
TOHCLK	337	OUT_CELL	OEB_TPHVAL	19	OUT_CELL
OEB_TOHFP	336	OUT_CELL	TPHVAL	18	OUT_CELL
TOHFP	335	OUT_CELL	OEB_TPHFA	17	OUT_CELL
OEB_TPOHRDY	334	OUT_CELL	TPHFA	16	OUT_CELL
TPOHRDY	333	OUT_CELL	OEB_ROHVAL	15	OUT_CELL
OEB_TSLDCLK	332	OUT_CELL	ROHVAL	14	OUT_CELL
TSLDCLK	331	OUT_CELL	OEB_ROHFA	13	OUT_CELL
TSLD	330	IN_CELL	ROHFA	12	OUT_CELL
OEB_ROHCLK	329	OUT_CELL	OEB_ROH	11	OUT_CELL
ROHCLK	328	OUT_CELL	ROH	10	OUT_CELL
OEB_ROHFP	327	OUT_CELL	OEB_RPHVAL	9	OUT_CELL

Pin/Enable	Reg. Bit	Cell Type	Pin/Enable	Reg. Bit	Cell Type
ROHFP	326	OUT_CELL	RPHVAL	8	OUT_CELL
OEB_RTOH	325	OUT_CELL	OEB_RPHFA	7	OUT_CELL
RTOH	324	OUT_CELL	RPHFA	6	OUT_CELL
OEB_RPOH	323	OUT_CELL	OEB_RPH	5	OUT_CELL
RPOH	322	OUT_CELL	RPH	4	OUT_CELL
OEB_RPOHEN	321	OUT_CELL	TPHINS	3	IN_CELL
RPOHEN	320	OUT_CELL	TPH	2	IN_CELL
OEB_SALM	319	OUT_CELL	TOHINS	1	IN_CELL
SALM	318	OUT_CELL	TOH	0	IN_CELL

Notes

1. Each output has its own output enable (OEB*)
2. When set high, INTB will be set to high impedance
3. FRAC[0] is the first bit in the boundary scan chain. TOH is the first bit out of the boundary scan chain.

12.2 Boundary Scan Cell Description

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located in the TEST FEATURES DESCRIPTION - JTAG Test Port section.

Figure 36 Input Observation Cell (IN_CELL)

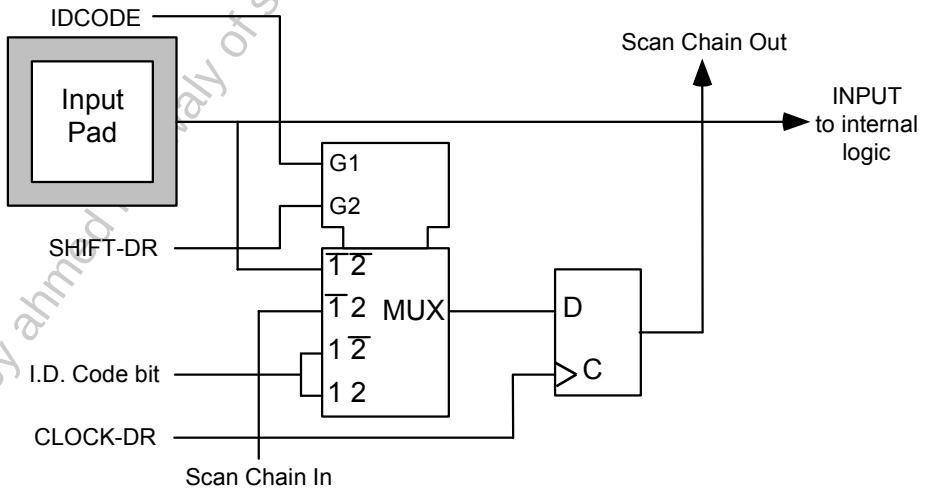


Figure 37 Output Cell (OUT_CELL)

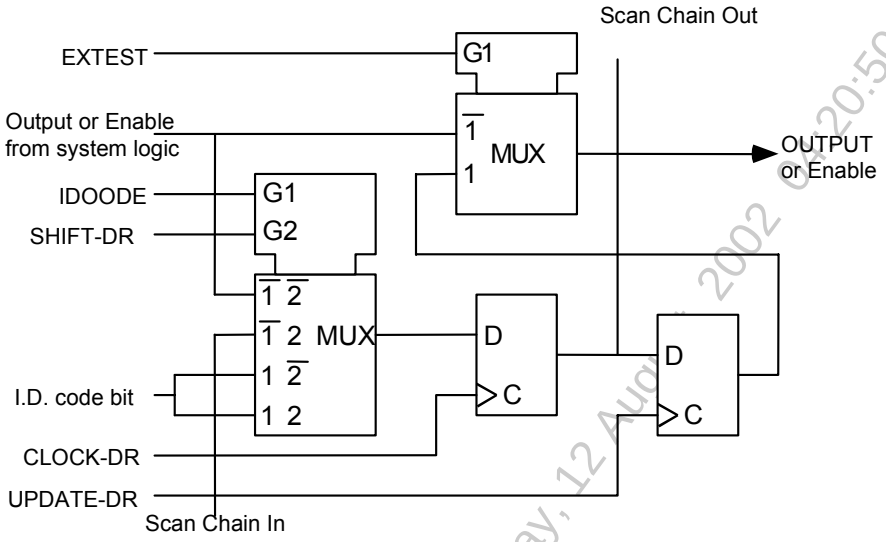


Figure 38 Bi-directional Cell (IO_CELL)

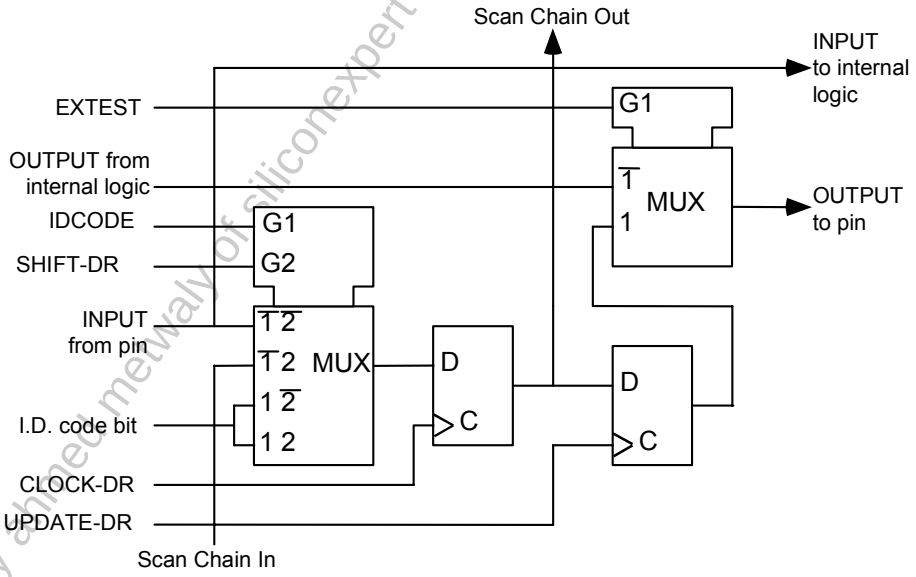
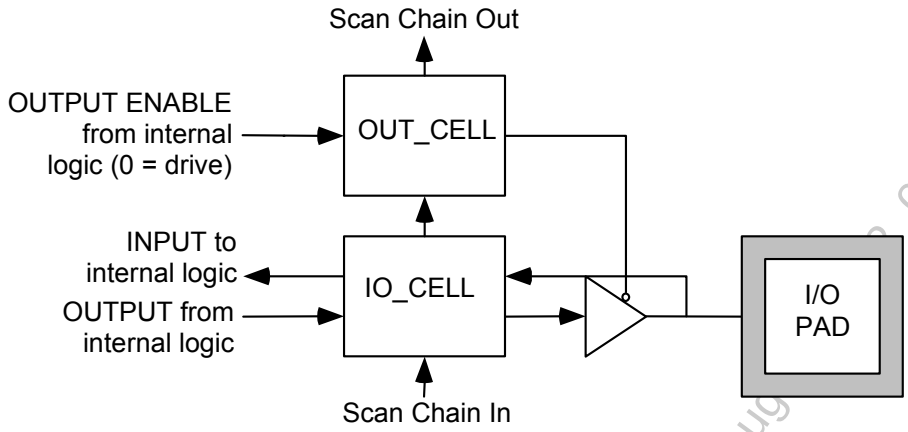


Figure 39 Layout of Output Enable and Bi-directional Cells



13 Operation

13.1 System Interface Configurations

The System Interface can be configured to be a UTOPIA Level 2, POS-PHY Level 2, UTOPIA Level 3, or POS-PHY Level 3 interface.

Table 13 System Interface Configurations

Mode	SMODE[2:0]	Data Formats
UTOPIA Level 2	"000" – tristate when interface is deselected "100" – not tristated when interface is de-selected	ATM
POS-PHY Level 2	"001" – tristate when interface is deselected "101" – not tristated when interface is de-selected	POS (Byte HDLC), HDLC (Bit-HDLC)
UTOPIA Level 3	"010" – never tristated.	ATM
POS-PHY Level 3	"011" – never tristated	ATM, POS, HDLC

In UTOPIA Level 2 and 3 modes of operation, only ATM is allowed, thus all slices must be in ATM mode.

In POS-PHY Level 2 or 3 modes of operation, POS, or Bit-HDLC can be processed. ATM may also be processed in POS-PHY Level 3. These modes of operation can be configured on a per channel basis.

By default, when configured for Utopia all channels start up in ATM mode, when configured for POS-PHY, all channels start up in POS mode.

For Level 2 interfaces, the Transmit and receive mode of operation is determined by the Channel Transmit/Receive Address Configuration Slice Registers 0x106 and 0x107 respectively (Bits – TXATMBPOS/RXATMBPOS). In Level 2 mode, the addresses that tristate the Level 2 interfaces are specified in the Transmit Receive L2 Tristate Control Registers, 0x1FF0, 0x1FF1, 0x1FF2, and 0x1FF3. All slices must have Channel Configuration #1 (0x0000) Register DS27_53 set to logic 1.

For Level 3 interfaces, the RUL3 and TUL3 Mode Configuration Registers; 0x1818, 0x1819, 0x181A, 0x181B, 0x1829, 0x182A, 0x182B, 0x182C, determine the mode of operation (Bits – PATM[0:11]). For Level 3 ATM Modes,0x062 RCALEVEL0 must be set to 0.

Table 14 System Interface Basic Configurations

Operating Mode	S/UNI-12xJET Channel Register Values (Values in Hexadecimal)			
	Receive		Transmit	
	Address(es)	Data	Address(es)	Data
ATM (UL3 – Utopia Level 3) (POS3 – POS-PHY Level 3)	0x1810*	0x0000	0x1820*	0x0000
	0x1818, 0x1819, 0x181A, 0x181B*	0x0000 UL3 0x000F POS3	0x1829, 0x182A, 0x182B, 0x182B*	0x0000 UL3 0x000F POS3
ATM Slice (For slice N, add N * 0x200)	0x0107**	0x0000	0x0106**	0x0000
	0x0060	0x0004	0x0080	0x0004
	0x0061	0x0000	0x0081	0x0000
	0x0062	0x0010***	0x108	0x0201
	0x0140	0x0013	0x0161	0x0013
POS	0x1810*	0x0000	0x1820*	0x0000
	0x1818, 0x1819, 0x181A, 0x181B*	0x0000	0x1829, 0x182A, 0x182B, 0x182B*	0x0000
POS Slice (For slice N, add N * 0x200)	0x0107**	0x0040	0x0106**	0x0040
	0x0062	0x0011	0x0080	0x0005
	0x0109	0x0000	0x0108	0x0000
	0x0140	0x0012	0x0161	0x0012
HDLC	0x1810*	0x0000	0x1820*	0x0000
	0x1818, 0x1819, 0x181A, 0x181B*	0x0000	0x1829, 0x182A, 0x182B, 0x182B*	0x0000
HDLC Slice (For slice N, add N * 0x200)	0x0107**	0x0040	0x0106**	0x0040
	0x0062	0x0011	0x0080	0x0005
	0x0109	0x0001	0x0108	0x0001
	0x0140	0x0010	0x0161	0x0010

* Necessary for configuring ATM/(POS/HDLC) Modes with Level 3 Interfaces.

** Necessary for configuring ATM/(POS/HDLC) Modes with Level 2 Interfaces.

*** In Level 3 interfaces, this register must be set to 0x00

13.2 Framer, Transmitter, and Auxiliary Framer Basic Configurations

Table 15 Framer, AUX Framer, and Transmitter Register Settings for Basic Configurations

Operating Mode (For slice N, add N*0x200)	S/UNI-12xJET Channel Register Values (Values in Hexadecimal)					
	Framer/ TX		AUX Framer/ TX		Transmitter / TX	
	Address	Data	Address	Data	Address	Data
T3 C-bit ADM	0x0003	0x0000			0x0000	0x00C0

Operating Mode (For slice N, add N*0x200)	S/UNI-12xJET Channel Register Values (Values in Hexadecimal)					
	Framer/ TX		AUX Framer/ TX		Transmitter / TX	
	Address	Data	Address	Data	Address	Data
	0x0004	0x00F8			0x0002	0x0000
	0x0008	0x0000			0x000C	0x0000
	0x0030	0x0083	0x0180	0x0083	0x0034	0x0001
	0x0061	0x0004				
T3 M23 ADM	0x0003	0x0000			0x0000	0x00C0
	0x0004	0x00F8			0x0002	0x0000
	0x0008	0x0000			0x000C	0x0000
	0x0030	0x0082	0x0180	0x0082	0x0034	0x0000
	0x0061	0x0004				
T3 C-bit PLCP	0x0003	0x0000			0x0000	0x0040
	0x0004	0x00F8			0x0002	0x0000
	0x0008	0x0004			0x000C	0x0004
	0x0030	0x0083	0x0180	0x0083	0x0034	0x0001
	0x0061	0x0000				
T3 M23 PLCP	0x0003	0x0000			0x0000	0x0040
	0x0004	0x00F8			0x0002	0x0000
	0x0008	0x0004			0x000C	0x0004
	0x0030	0x0082	0x0180	0x0082	0x0034	0x0000
	0x0061	0x0000				
T3 C-bit framer only*	0x0003	0x0000			0x0000	0x0050
	0x0004	0x0078			0x0002	0x0000
	0x0008	0x0000			0x000C	0x0000
	0x0030	0x0083	0x0180	0x0083	0x0034	0x0001
T3 M23 framer only*	0x0003	0x0000			0x0000	0x0050
	0x0004	0x0078			0x0002	0x0000
	0x0008	0x0000			0x000C	0x0000
	0x0030	0x0082	0x0180	0x0082	0x0034	0x0000
E3 G.832 ADM	0x0003	0x0040			0x0000	0x00C0
	0x0004	0x00F8			0x0002	0x0040
	0x0008	0x0000			0x000C	0x0000
	0x0038	0x0004	0x0188	0x0004	0x0040	0x0001
	0x0039	0x0000	0x0189	0x0000	0x0041	0x0001
	0x0061	0x0008			--	--
E3 G.832 framer only*	0x0003	0x0040			0x0000	0x0050
	0x0004	0x0078			0x0002	0x0040
	0x0008	0x0000			0x000C	0x0000
	0x0038	0x0004	0x0188	0x0004	0x0040	0x0001
	0x0039	0x0000	0x0189	0x0000	0x0041	0x0001

Operating Mode (For slice N, add N*0x200)	S/UNI-12xJET Channel Register Values (Values in Hexadecimal)					
	Framer/ TX		AUX Framer/ TX		Transmitter / TX	
	Address	Data	Address	Data	Address	Data
E3 G.751 ADM	0x0003	0x0040			0x0000	0x00C0
	0x0004	0x00F8			0x0002	0x0040
	0x0008	0x0000			0x000C	0x0000
	0x0038	0x0000	0x0188	0x0000	0x0040	0x0000
	0x0039	0x0000	0x0189	0x0000	0x0041	0x0001
	0x0061	0x0008				
E3 G.751 PLCP	0x0003	0x0040			0x0000	0x0040
	0x0004	0x00F8			0x0002	0x0040
	0x0008	0x0044			0x000C	0x0044
	0x0038	0x0000	0x0188	0x0000	0x0040	0x0000
	0x0039	0x0004	0x0189	0x0004	0x0041	0x0001
	0x0061	0x0000				
E3 G.751 framer only*	0x0003	0x0040			0x0000	0x0050
	0x0004	0x0078			0x0002	0x0040
	0x0008	0x0000			0x000C	0x0000
	0x0038	0x0000	0x0188	0x0000	0x0040	0x0000
	0x0039	0x0000	0x0189	0x0000	0x0041	0x0001
J2 ADM	0x0003	0x0080			0x0000	0x00C0
	0x0004	0x00F8			0x0002	0x0080
	0x0008	0x0000			0x000C	0x0000
	0x0044	0x0003	0x0190	0x0003	0x004C	0x000E
	0x0061	0x0008				
J2 framer only*	0x0003	0x0080			0x0000	0x0050
	0x0004	0x0078			0x0002	0x0080
	0x0008	0x0000			0x000C	0x0000
	0x0044	0x0003	0x0190	0x0003	0x004C	0x000E
E1 PLCP	0x0003	0x00C0			0x0000	0x0040
	0x0008	0x00C4			0x0002	0x00C0
	0x0061	0x0000			0x000C	0x00C4
E1 ADM	0x0003	0x00C0			0x0000	0x0040
	0x0008	0x00C0			0x0002	0x00C0
	0x0061	0x0000			0x000C	0x00C0
T1 PLCP	0x0003	0x00C0			0x0000	0x0040
	0x0008	0x0084			0x0002	0x00C0
	0x0061	0x0000			0x000C	0x0084
T1 ADM	0x0003	0x00C0			0x0000	0x0040
	0x0008	0x0080			0x0002	0x00C0
	0x0061	0x0000			0x000C	0x0080

Operating Mode (For slice N, add N*0x200)	S/UNI-12xJET Channel Register Values (Values in Hexadecimal)					
	Framer/ TX		AUX Framer/ TX		Transmitter / TX	
	Address	Data	Address	Data	Address	Data
External Framer ADM*	0x0003	0x00C0			0x0000	0x0040
	0x0008	0x0001			0x0002	0x00C0
	0x0061	0x0000			0x000C	0x0001

* In Framer Only Modes, 0x009B needs to be set to 0x0001, in all other modes 0x009B needs to be set to 0x0000.

- The appropriate reference clock must be selected via register 0x113, DS3BE3 bit. T3/DS3 modes must select the DS3 reference clock, and E3 modes must select the E3 reference clock. For J2, E1, and T1 modes no external reference clock is necessary, these only use the serial clocks.
- Byte, nibble, or bit alignment of the ATM Cell bytes to the line overhead is configured using the TOCTA bit in register x00, and the FORM[1:0] bits in register x0CH.
- Unipolar mode is selected for DS3, E3, and J2 modes by setting the TUNI bit to logic 1 in register x02H and the UNI bit in x30, x38, and x44H respectively. When the DS3, E3, or J2 framers are bypassed, unipolar mode is selected by default.
- Bit, Nibble, and Byte alignment of the ATM cell octets to the arbitrary external frame overhead is set using the ALIGN[1:0] bits of register x61H.

13.3 Slice Operation Configurations

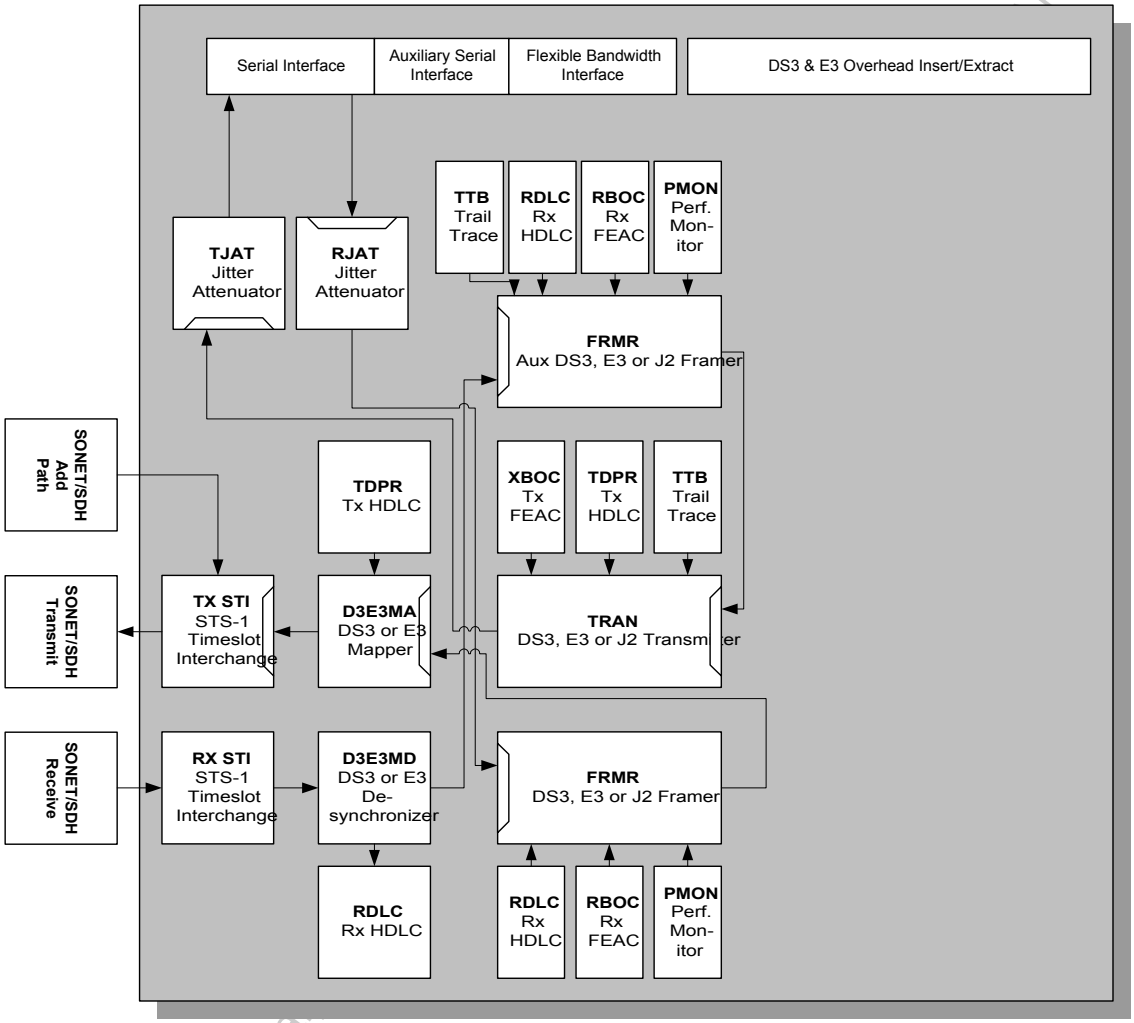
13.3.1 Clear Channel PDH Over SONET/SDH

Clear channel PDH over SONET/SDH makes use of the serial interfaces and the SONET/SDH paths.

Transmit path is from SONET/SDH, through the DS3E3 Desynchronizer, through the Auxiliary FRMR, through the TRAN, and through the TJAT to the transmit serial interface. The TJAT and AUX FRMR may be bypassed via register control. When the Auxiliary FRMR is bypassed, the AUX FRMR monitors the data-path but will not change it. When the Auxiliary FRMR is in the data-path, the Auxiliary FRMR frames and will modify the data-path.

Receive path is from the receive serial interface, through the RJAT, through the FRMR, through the DS3E3 Mapper to SONET/SDH. The RJAT may be bypassed via register control.

Figure 40 Clear Channel PDH Over SONET/SDH Data Path



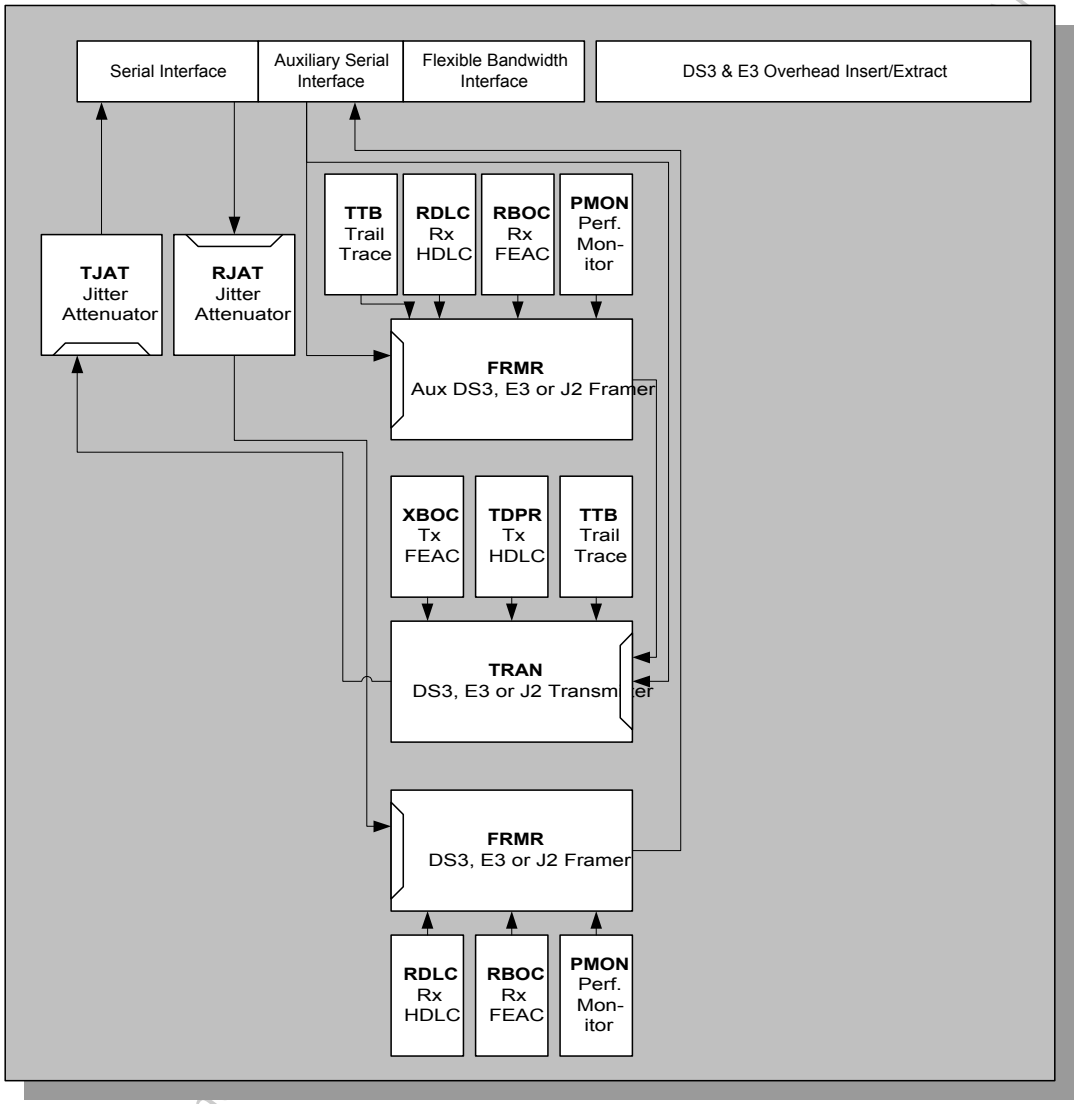
13.3.2 PDH Framer Only

PDH Framer Only mode uses the serial and auxiliary serial interfaces.

The transmit path starts at the auxiliary serial interface, through the TRANS and/or Auxiliary FRMR, and through the TJAT to the transmit serial interface. The TJAT may be bypassed via register control, and the Auxiliary FRMR can be used as the true data path, or for monitoring purposes while the data path passes through the TRANS.

The receive path starts at the receive serial interface, through the RJAT, through the FRMR, to the receive auxiliary serial interface. The RJAT may be bypassed via register control.

Figure 41 PDH Framer Only Data Path



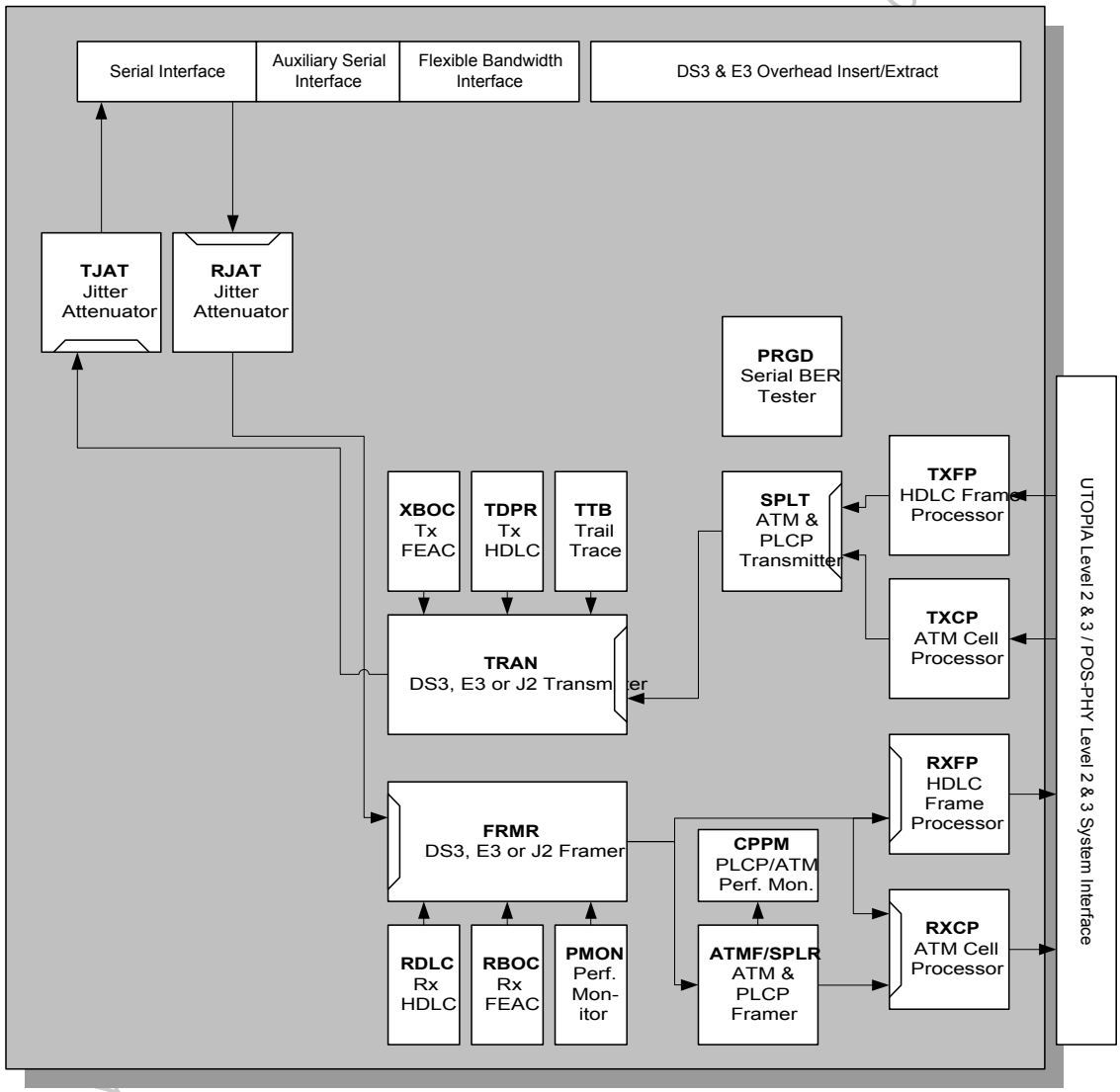
13.3.3 Cell/Packet over PDH

Cell/Packet over PDH uses the serial interfaces and the system interfaces (Utopia Level2/3, and POS-PHY Level 2/3).

The transmit path starts at the transmit system interface, through the TXCP or TXFP based on ATM or Packet/HDLC mode, through the ATM & PLCP transmitter, through the TRANS, and through the TJAT to the transmit serial interface. The TJAT may be bypassed via register control. The SPLT ATM and PLCP transmitter are to only be used in ATM Mode.

The receive path starts at the receive serial interface, through the RJAT, through the FRMR, through the ATM & PLCP Framer and RXCP or only through the RXFP to the receive system interface. The RJAT may be bypassed via register control. The ATM & PLCP Framer are only used in ATM Mode.

Figure 42 Cell/Packet Over PDH Data Path



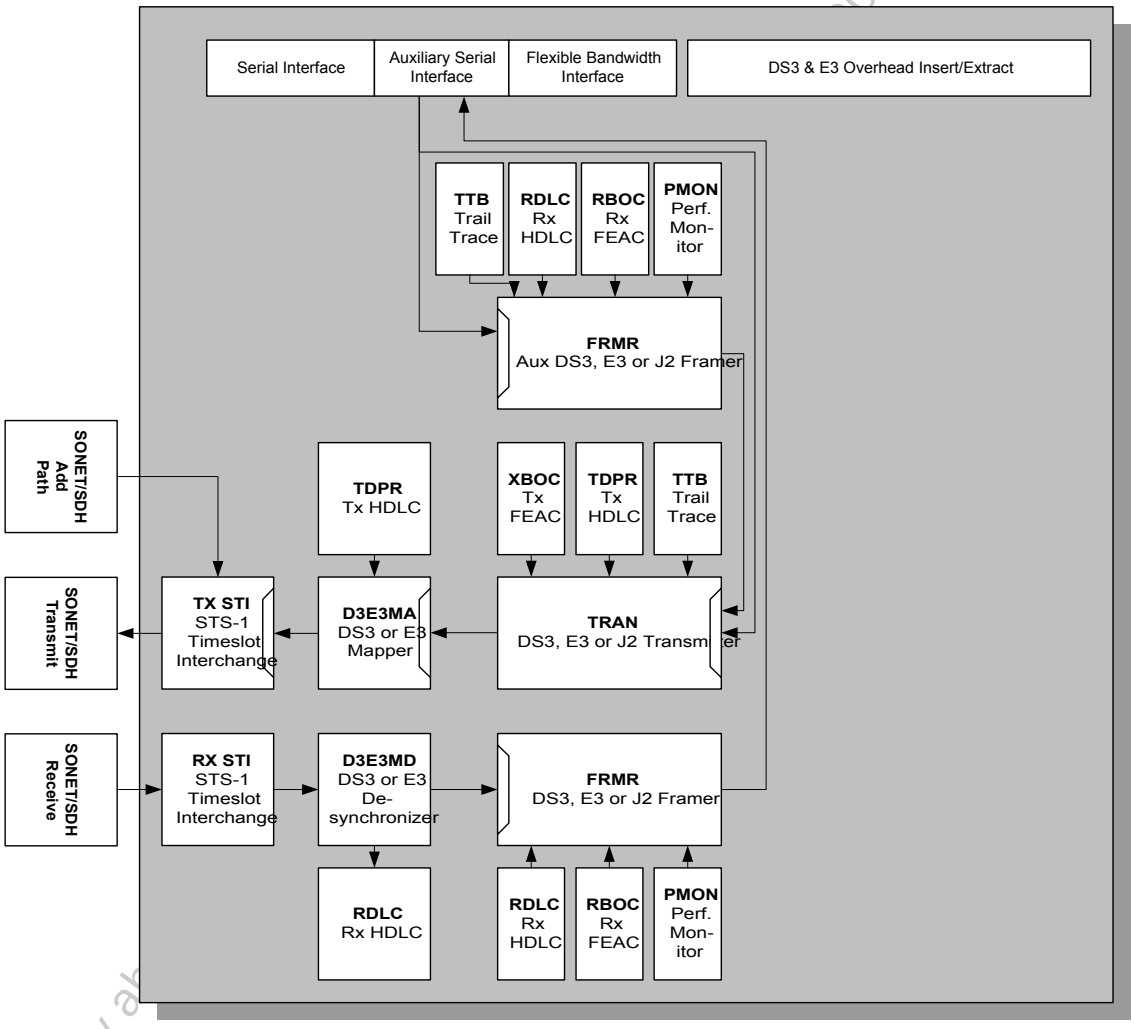
13.3.4 AUX Interface PDH Over SONET/SDH

The AUX Interface PDH over SONET/SDH uses the auxiliary serial interfaces and the SONET/SDH interface.

Transmit path is from the transmit auxiliary serial interface, through the AUX FRMR and/or the TRAN, through the DS3E3 Mapper to SONET/SDH. The Auxiliary FRMR may be used for monitoring purposes while the data path passes through the TRANS.

Receive path is from SONET/SDH, through the DS3E3 De-synchronizer, through the FRMR, to the receive auxiliary serial interface.

Figure 43 AUX Interface PDH Over SONET/SDH Data Path



13.3.5 Cell/Packet Delineation Only

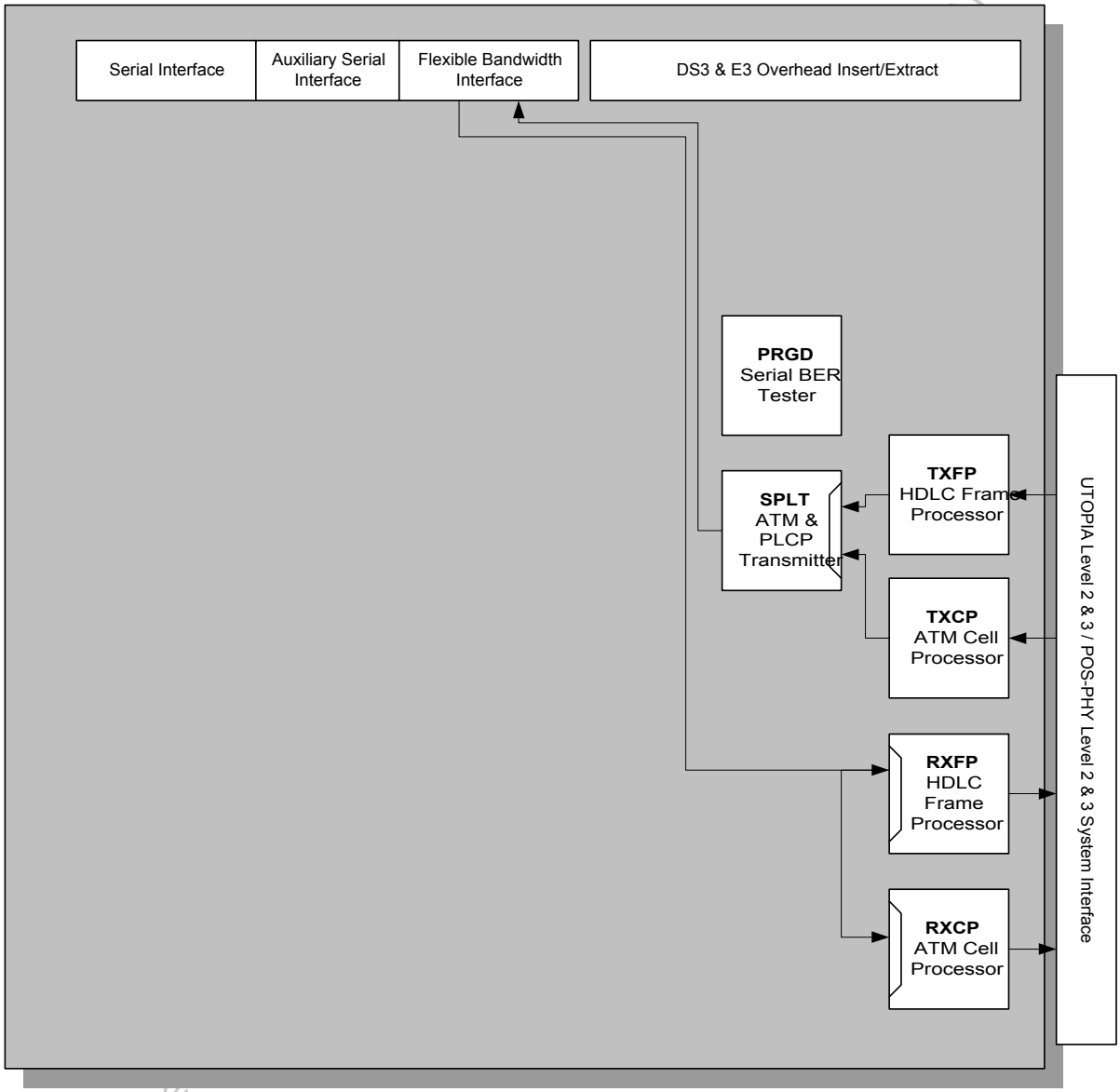
Cell/Packet Delineation Only mode uses the Flexible Bandwidth Interfaces and the system interfaces (Utopia Level2/3, and POS-PHY Level 2/3).

The transmit path starts at the transmit system interface, through the TXCP or TXFP based on ATM or Packet/HDLC mode, through the ATM & PLCP transmitter, the egress flexible bandwidth interface. The SPLT ATM and PLCP transmitter are used to serialize the stream only. The SPLT must be placed in EXT mode such that no framing and PLCP processing is performed.

The receive path starts at the ingress flexible bandwidth interface, through the RXCP or the RXFP to the receive system interface.

To remove the interaction between the FRMR and RXCP/RXFP, RFRM[1:0] bits in the Channel Receive Configuration Register (0x003 for channel 0) must be set to '11' arbitrary framing format. This removes the ability of the FRMR to force HUNT in the RXCP and squelch data input into the RXFP when the data-path has not achieved frame in the FRMR.

Figure 44 Cell/Packet Delineation Only Data Path



13.3.6 Cell/Packet over SONET/SDH

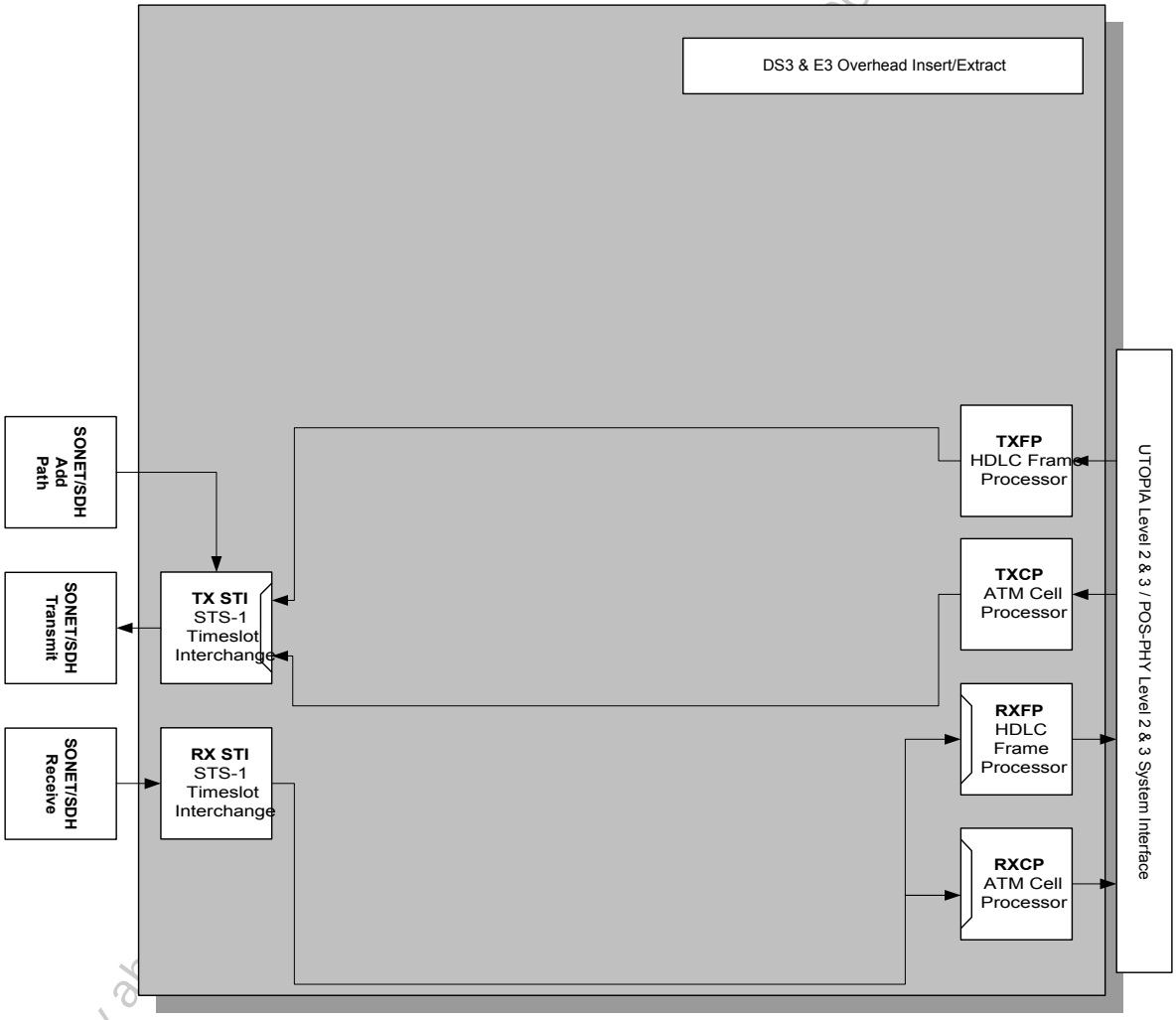
Cell/Packet over SONET/SDH mode uses the SONET/SDH interfaces and the system interfaces (Utopia Level2/3, and POS-PHY Level 2/3). Note that only ATM and Packet modes are available in Cell/Packet over SONET/SDH, and the Bit-HDLC mode configurations are bypassed.

The transmit path starts at the transmit system interface, through the TXCP or TXFP based on ATM or Packet mode, to the SONET/SDH interface.

The receive path starts at the SONET/SDH interface, progresses through the RXCP or the RXFP to the receive system interface.

Each slice may be configured to process an STS-1/STM-0, or an STS-3c/STM-1 or a STS-12c/STM-4-4c payload using the TX STI and RX STI, however the full bandwidth for all the slices may not exceed an STS-12c/STM-4-4c worth of data.

Figure 45 Cell/Packet Over SONET/SDH Data Path



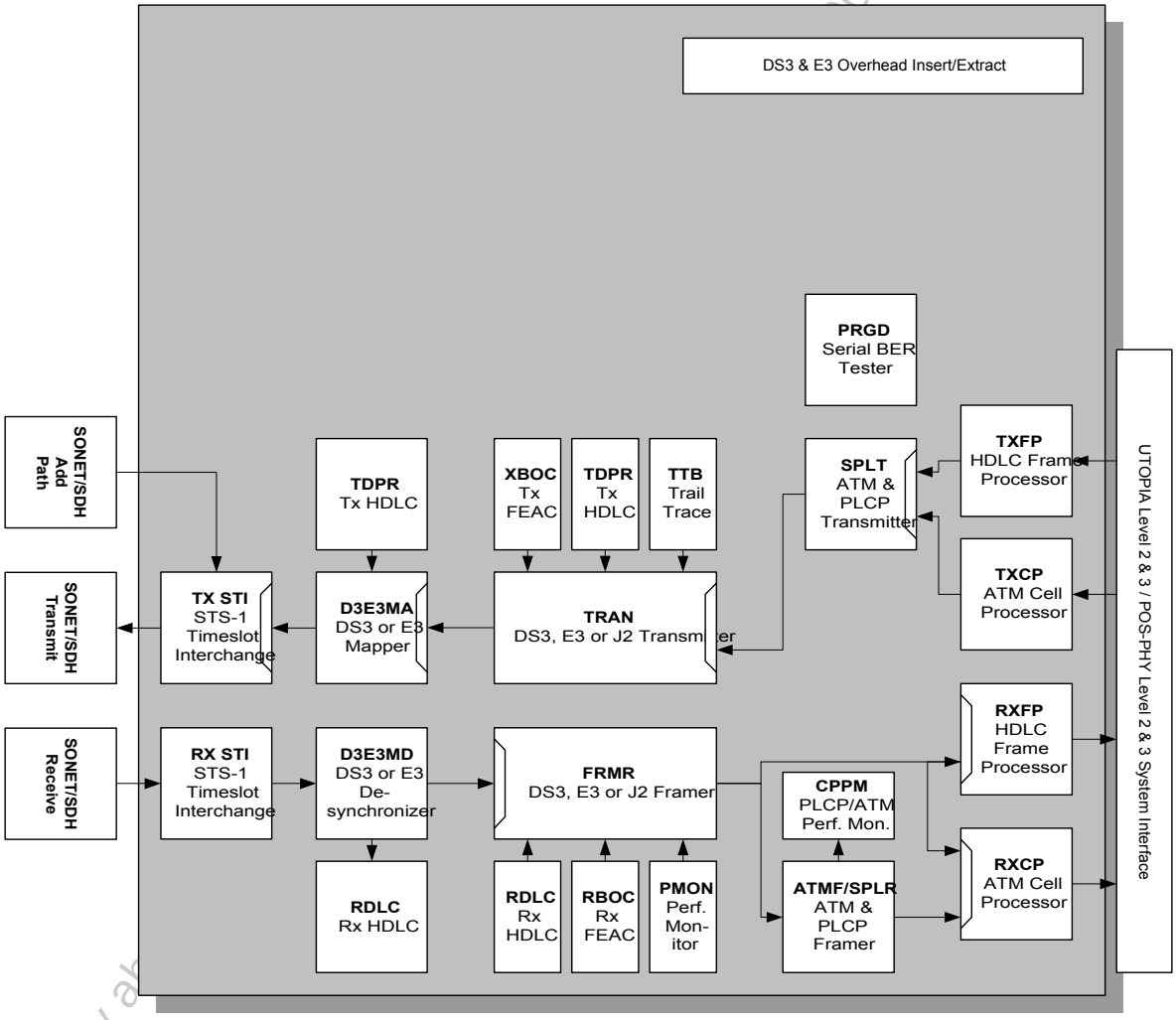
13.3.7 Cell/Packet over PDH over SONET/SDH

Cell/Packet over PDH over SONET/SDH uses the SONET/SDH interfaces and the system interfaces (Utopia Level2/3, and POS-PHY Level 2/3). Although this mode of operation does not use the Serial or Auxiliary Interfaces, TICLK of the Auxiliary Interface is necessary for clocking the TRAN and associated blocks.

The transmit path starts at the transmit system interface, through the TXCP or TXFP based on ATM or Packet/HDLC mode, through the ATM & PLCP transmitter, through the TRAN, through the DS3E3 Mapper to SONET/SDH.

The receive path starts from SONET/SDH interface, through the DS3E3 De-synchronizer, through the FRMR, through the RXCP or the RXFP to the receive system interface.

Figure 46 Cell/Packet Over PDH Over SONET/SDH



13.3.8 Cell/Packet Over PDH Over SONET/SDH With External Processing

Cell/Packet over PDH over SONET/SDH with External Processing utilizes the SONET/SDH interfaces, the Auxiliary Serial Interfaces, the Flexible Bandwidth Interface, and the system interfaces (Utopia Level2/3, and POS-PHY Level 2/3). This mode may be used for sub-rate processing; for example sub-rate DS3 processing, for twelve or six channels based on the FRAC[1:0] mode pins.

The transmit path starts at the transmit system interface, through the TXCP or TXFP based on ATM or Packet/HDLC mode, through the ATM & PLCP transmitter, the egress flexible bandwidth interface. The SPLT ATM and PLCP transmitter are used to serialize the stream only. The SPLT must be placed in EXT mode such that no framing and PLCP processing is performed. Once out of the egress flexible bandwidth interface, the transmit path flows back into the device through the transmit auxiliary serial interface, through the Auxiliary FRMR and/or TRANS, through the DS3E3 Mapper to SONET/SDH. The Auxiliary FRMR may be used for monitoring purposes and generation of frame pulse information while the data path passes through the TRANS

The receive path starts from SONET/SDH interface, through the DS3E3 De-synchronizer, through the FRMR, to the receive auxiliary serial interface. Once out of the receive auxiliary serial interface, the transmit path flows back into the device through the ingress flexible bandwidth interface, through the RXCP or the RXFP to the receive system interface.

Although data-path propagates outside the S/UNI-12xJET between the FRMR and RXCP/RXFP blocks, the FRMR may still force HUNT in the RXCP and squelch data input into the RXFP when the data has not achieved frame in the FRMR.

Figure 47 Cell/Packet Over PDH Over SONET/SDH With External Processing Data Path

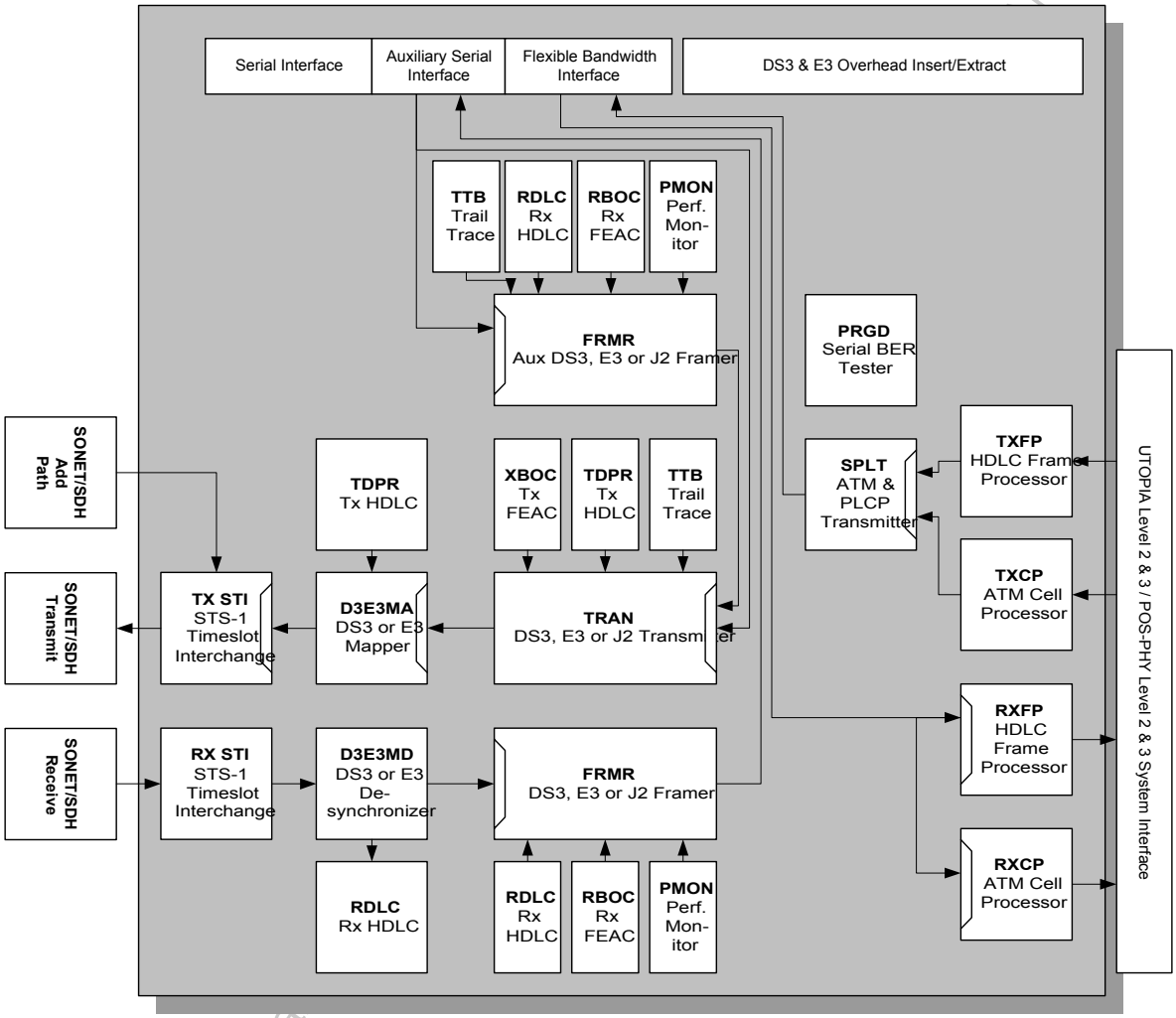


Table 16 Slice Operation Basic Configurations

Operating Mode (For slice N add N*0x200 to Address)	S/UNI-12xJET Channel Register Values	
	Address (in Hex)	Data (in binary)
Clear Channel PDH over SONET/SDH	0x000	0000 0000 1101 0000 (0x00D0)
	0x100	0000 0bbb bbbb bb10
	0x101	0000 0000 0000 0010 (0x0002)
	0x113	0001 c010 1001 0001
PDH Framer Only	0x000	0000 0000 1101 a000
	0x113	0001 c000 0000 000d
Cell/Packet over PDH*	0x000	0000 0000 1100 a000
	0x100	0000 0000 1000 0010 (0x0082)

Operating Mode (For slice N add N*0x200 to Address)	S/UNI-12xJET Channel Register Values	
	Address (in Hex)	Data (in binary)
	0x101	0000 0000 0000 0010 (0x0002)
	0x113	0001 c000 0000 0000
AUX Interface PDH over SONET/SDH	0x000	0000 0000 1101 a000
	0x100	0000 0bbb bbbb bbb0
	0x101	0000 0000 0000 00b0
	0x113	0001 c000 0010 000d
Cell/Packet Delineation Only	0x000	0000 0000 1100 0000 (0x00C0)
	0x003	0000 0000 1100 0000 (0x00C0)
	0x00C	0000 0000 0000 0001 (0x0001)
	0x113	1000 0000 0000 0000 (0x8000)
Cell/Packet over SONET/SDH	0x100	0000 0bbb bbbb bbb1
	0x101	0000 0000 0000 00b1
Cell/Packet over PDH over SONET	0x000	0000 0000 1100 0000 (0x00C0)
	0x100	0000 0bbb bbbb bbb0
	0x101	0000 0000 0000 00b0
	0x113	0001 c000 0010 0000
Cell/Packet over PDH over SONET with external processing	0x000	0000 0000 1101 0000 (0x00D0)
	0x00C	0000 0000 0000 0001 (0x0001)
	0x100	0000 0bbb bbbb bbb0
	0x101	0000 0000 0000 00b0
	0x113	1001 c000 0010 000d

Notes:

1. “a” is the LOOPT register bit. This bit enables the receive serial interface clock (RCLK) to be the timing source for the transmit data path TICLK. This can only be used when FRAC[1:0] is set to “00” and in AUX Interface PDH over SONET/SDH, Cell/Packet over PDH, or PDH Framer Only modes.
2. “b” is the configuration for SONET/SDH AU3/TU3 of the channel and must be considered when programming these registers.
3. “c” is the REFE3DS3B reference clock select, and must be set to the appropriate reference source. 0 for DS3 (default), 1 for E3.
4. “d” is the TRANSEL transmit input select, and must be set to 1 if data-path monitoring is required (using the AUX FRMR) of the transmit path. If data-path monitoring is not required of the transmit path, then this bit must be set to 0.

Cell/Packet over PDH over SONET with external processing is the AUX interface PDH over SONET/SDH and Cell/Packet Delineation Only configurations combined.

13.3.9 PDH Alarm Configurations

The FRMR, and AUX FRMR when used in the data-path, may be programmed to insert alarm conditions and Trail Trace Messaging into the PDH transmit data-path and generate the DS3/E3 AIS patterns when mapping DS3/E3 into SONET/SDH.

For the PDH transmit data-path, the Slice Channel Data-path Configuration Register (0x113) may be configured such that the FEBE alarm generated by the FRMR and/or the AUX FRMR is inserted into the TRAN. For XFEBE, FCLK and TRACE, only one of the framers (FRMR or AUX-FRMR) may be selected to be sent to the TRAN.

For generating AIS patterns, the Channel D3E3MA AISGEN Enable Register (0x117) may be configured such that all or any of the FRMR alarms (LOF, AIS, RBL, OOF, LOS), AUX-FRMR alarms (LOF, AIS, RBL, OOF, LOS), or RJAT ROOL bit will cause the insertion of DS3/E3 AIS when mapping into SONET/SDH.

13.4 Serial, Auxiliary Serial and Flexible Bandwidth Configurations

The FRAC[1:0] input mode pins determine the operational mode of the serial, auxiliary serial and flexible bandwidth interfaces.

The following tables describe the main modes of operation of the S/UNI-12xJET. This is not an all inclusive list. Each operational mode is described above

Table 17 FRAC[1:0] = "00" Framer Only and Clear Channel Modes

Interface Resources	Used	Description	Modes of Operation
Serial	Yes	Each slice has its own receive and transmit serial interface. The interfaces can be interchanged via the internal serial cross connect registers on a per slice level.	Clear Channel PDH over SONET/SDH PDH Framer Only Cell/Packet over PDH
Auxiliary Serial	Yes	Each slice has its own receive and transmit auxiliary interface.	PDH Framer Only AUX Interface PDH over SONET/SDH
Flexible Bandwidth	No		

Table 18 FRAC[1:0] = "01" 12 Channel External Serial Payload Processing

Interface Resources	Used	Description	Modes of Operation
Serial	No		
Auxiliary Serial	Yes	ROVRHD is used by the Flexible Bandwidth Interface, thus overhead calculations must be determined outside the device using the RFPO/RMFPO pin.	AUX Interface PDH over SONET/SDH Cell/Packet over PDH over SONET/SDH with External Processing
Flexible Bandwidth	Yes	The Serial Interface pins in conjunction with the ROVRHD pin are used as the Flexible Bandwidth Interface.	Cell/Packet Delineation Only Cell/Packet over PDH over SONET/SDH with External Processing

Table 19 FRAC[1:0] = "10" Six Channel External Serial Payload Processing

Interface Resources	Used	Description	Modes of Operation
Serial	Yes	Each slice has its own receive and transmit serial interface. The interfaces can be interchanged via the internal serial cross connect registers on a per slice level.	Clear Channel PDH over SONET/SDH PDH Framer Only Cell/Packet over PDH
Auxiliary Serial	Yes	Only 6 channels (even channels 0, 2, 4, 6, 8, 10) Each EVEN slice has its own receive and transmit auxiliary interface.	PDH Framer Only Aux. Interface PDH over SONET/SDH Cell/Packet over PDH over SONET/SDH with External Processing
Flexible Bandwidth	Yes	Only 6 channels (odd channels 1, 3, 5, 7, 9, 11) The ODD slice Auxiliary Interface pins are used as the Flexible Bandwidth Interface. These Flexible Bandwidth Interface pins can be used with either the Interface Number's slice [N], or the even slice before this interface [N-1].	Cell/Packet Delineation Only Cell/Packet over PDH over SONET/SDH with External Processing

For Cell/Packet over PDH over SONET with Sub DS3 or external processing you would use the even channels in this mode, with the serial interfaces in PDH Framer Only mode, and the Flexible Bandwidth interface along with the Auxiliary interface connected as in Figure 43.

Table 20 FRAC[1:0] = "11" 12 Channel Cell/Packet Delineation

Interface Resources	Used	Description	Modes of Operation
Serial	Yes	Each slice has its own receive and transmit serial interface. The interfaces can be interchanged via the internal serial cross connect registers on a per slice level.	Clear Channel PDH over SONET/SDH Cell/Packet over PDH
Auxiliary Serial	No		
Flexible Bandwidth	Yes	The Auxiliary Interface pins are used as the Flexible Bandwidth Interface. These Flexible Bandwidth Interface pins apply only to their associated slice. e.g. Slice N uses IFBWCLK[N].	Cell/Packet Delineation Only Cell/Packet over PDH over SONET/SDH with External Processing

The serial interface is connected via a serial cross connect. Any channel may source any set of serial egress pins, or sink any set of serial ingress pins. There is also the ability to broadcast in both directions when used as a serial interface; for example, the receive serial interface may source multiple channels, and a single channel may source multiple transmit serial interfaces. When the serial pins are used for the flexible bandwidth interface, the serial cross connect must be held in it's default state (cannot be used). Channel Register 0x114 (+ N*0x200 offset for channel N) is used to configure the serial cross connect.

13.4.1 Serial Interface Jitter Attenuation Configuration

The Transmit and Receive Jitter attenuation (TJAT/RJAT) blocks are used in DS3 and E3 modes only. By default the TJAT/RJAT are held in bypass mode. To take either JAT out of bypass mode you must write a zero into the BYPASS bit of the associated JAT configuration register. Other serial modes must keep the TJAT/RJAT in bypass mode.

13.5 DS3/E3 Mapping over SONET/SDH Mapping Configurations

Each slice may be configured to process an STS-1/STM-0, or an STS-3c/STM-1 or a STS-12c/STM-4-4c payload using the TX STI and RX STI, however the full bandwidth for all the slices may not exceed an STS-12c/STM-4-4c worth of data. Virtual concatenation with an STS-1/STM-0 or STS-3c/STM-1 granularity is also possible; however, pointer insertion is not performed, and in the receive direction, the S/UNI-12xJET must receive aligned and ordered virtual concatenation timeslots.

Each slice may also be configured to map DS3 Frames, E3 Frames, or direct mapping into an SONET/SDH Frame.

For the SONET/SDH receive direction RX TSI is configured using Registers Channel Receive Configuration #2, and Channel Receive Timeslot Configuration #1 (0x0101 and 0x0105 respectively for channel 0).

RXAU3TU3 bit in the Channel Receive Configuration #2 register determines whether the slice will process an AU3 or TU3 mapped data stream. For TU3 mode of operation, three slices independently process each of the three data streams within the TU3 frame.

The RXSTSEN bits in the Channel Receive Timeslot Configuration #1 register provide arbitrary STS-1 granularity processing for a given channel. For configurations other than STS-1/STM-0, timeslots must be sent to the RX TSI in proper order; for example, STS-3c(1) must be programmed to a timeslot before STS-3c(2) which must be programmed to a timeslot before STS-3c(3). Timeslots can be rolled at timeslot 11 to timeslot 0, allowing configurations where the first STS-1 granularity payload is not in the first timeslot, however they must be still in order; for example STS-3c(2) is in a timeslot before STS-3c(3) which is in a timeslot before STS-3c(1). Because all timeslots are sent to all channel, a single timeslot, or sets of timeslots may be processed by more than one channel. For TU3 Modes of operation, three independent channels are used to process an entire STS-3c/STM-1.

The DS3/E3 de-mapping is configured through the D3E3MD register set. All DS3 or E3 de-mapping from AU3 or TU3 configuration combinations are all possible. When configured for AU3, each channel carrying a DS3/E3 is de-mapped from an STS-1/STM-0 timeslot. When configured for TU3, an STS-3c/STM-1 contains three independent TU3's that must be processed by independent channels, each channel demapping one of the DS3/E3 streams.

For the SONET/SDH transmit direction, TX TSI is configured using Registers Channel Transmit Configuration #2, Channel Transmit Timeslot Configuration #1, #2, and #3 (0x100, 0x102, 0x103, and 0x104 respectively for channel 0).

The TXAU3TU3 bit in the Channel Transmit Configuration #2 register determines whether the slice will process an AU3 or TU3 mapped data stream. For TU3 mode of operation, three slices independently process each of the three data streams within the TU3 frame.

The TXSTSEN bits in the Channel Transmit Timeslot Configuration #1 register provide arbitrary STS-1 granularity processing for a given channel. For configurations other than STS-1/STM-0, timeslots must be sent to the TX TSI in proper order; for example, STS-3c(1) must be programmed to a timeslot before STS-3c(2) which must be programmed to a timeslot before STS-3c(3). Timeslots can be rolled at timeslot 11 to timeslot 0, allowing configurations where the first STS-1 granularity payload is not in the first timeslot, however they must be still in order; for example STS-3c(2) is in a timeslot before STS-3c(3) which is in a timeslot before STS-3c(1). Because all timeslots are sent to all channel, a single timeslot, or sets of timeslots may be processed by more than one channel. For TU3 Modes of operation, three independent channels are used to process an entire STS-3c/STM-1.

The DS3/E3 mapping is configured through the D3E3MA register set. All DS3 or E3 mapping to AU3 or TU3 configuration combinations are all possible. When configured for AU3, each channel carrying a DS3/E3 is mapped into an STS-1/STM-0 timeslot. When configured for TU3, up to three independent channels map a single DS3/E3 stream into a TU3 and three TU3's are placed into an STS-3c/STM-1.

Table 21 SONET/SDH Timeslot Configuration

Operating Mode (For slice N add N*0x200 to Address)	S/UNI-12xJET Channel Register Values			
	Receive TX STI / D3E3MD		Transmit TX STI / D3E3MA	
	Address(es) (in Hex)	Data (in binary)	Address(es) (in Hex)	Data (in binary)
STS-1/STM-0 Direct Mapped, Channel 0	0x0101	0000 0000 0000 0011	0x0100	0000 0000 0000 0011
	0x0105	0000 0000 0000 0001	0x0102	0000 0000 0000 0001
	0x010D	0000 0000 0000 0000	0x0103	0000 0000 0000 0000
	0x010E	0000 0000 0000 0000	0x0104	0000 0000 0000 0000
STS-1/STM-0 DS3, Channel 0	0x0101	0000 0000 0000 0010	0x0100	0000 0000 0000 0010
	0x0105	0000 0000 0000 0001	0x0102	0000 0000 0000 0001
	0x010D	0000 0000 0000 0000	0x0103	0000 0000 0000 0000
	0x010E	0000 0000 0000 0000	0x0104	0000 0000 0000 0000
	0x0120	0000 0000 0110 0000	0x0128	0000 0000 0110 0000
STS1/STM-0 E3, Channel 0	0x0101	0000 0000 0000 0010	0x0100	0000 0000 0000 0010
	0x0105	0000 0000 0000 0001	0x0102	0000 0000 0000 0001
	0x010D	0000 0000 0000 0000	0x0103	0000 0000 0000 0000
	0x010E	0000 0000 0000 0000	0x0104	0000 0000 0000 0000
	0x0120	0000 0000 0100 0000	0x0128	0000 0000 0100 0000
STS-3c/STM-1(AU4) Direct Mapped Timeslots 1 (Master), 5, 9 on Channel 0	0x0101	0000 0000 0000 0011	0x0100	0000 0000 0000 0011
	0x0105	0000 0001 0001 0001	0x0102	0000 0001 0001 0001
	0x010D	0000 0000 0000 0001	0x0103	0000 0001 0001 0000
	0x010E	0000 0000 0000 0000	0x0104	0000 0000 0000 0000
STS-3c/STM-1 (TU3) Direct Mapped Timeslots 1 (Master), 5, 9 on Channel 0, 1, 2 respectively	0x0101, 0x0301, 0x0501	0000 0000 0000 0001	0x0100, 0x0300, 0x0500	0000 0000 0000 0001
	0x0105	0000 0000 0000 0001	0x0102	0000 0000 0000 0001
	0x0305	0000 0000 0001 0000	0x0302	0000 0000 0001 0000
	0x0505	0000 0001 0000 0000	0x0502	0000 0001 0000 0000
	0x010D	0000 0000 0000 0001	0x0103	0000 0000 0000 0000
	0x030D	0000 0000 0000 0001	0x0303	0000 0000 0001 0000
	0x050D	0000 0000 0000 0001	0x0503	0000 0001 0000 0000
	0x010E	0000 0000 0000 0000	0x0104	0000 0000 0000 0000
	0x030E	0000 0000 0000 0000	0x0304	0000 0000 0001 0000
	0x050E	0000 0000 0000 0000	0x0504	0000 0001 0000 0000
STS-3c/STM-1 (TU3) DS3 Timeslots 1 (Master), 5, 9 on Channel 0, 1, 2 respectively	0x0101, 0x0301, 0x0501	0000 0000 0000 0000	0x0100, 0x0300, 0x0500	0000 0000 0000 0000
	0x0105	0000 0000 0000 0001	0x0102	0000 0000 0000 0001
	0x0305	0000 0000 0001 0000	0x0302	0000 0000 0001 0000
	0x0505	0000 0001 0000 0000	0x0502	0000 0001 0000 0000

Operating Mode (For slice N add N*0x200 to Address)	S/UNI-12xJET Channel Register Values			
	Receive TX STI / D3E3MD		Transmit TX STI / D3E3MA	
	Address(es) (in Hex)	Data (in binary)	Address(es) (in Hex)	Data (in binary)
	0x010D	0000 0000 0000 0001	0x0103	0000 0000 0000 0000
	0x030D	0000 0000 0000 0001	0x0303	0000 0000 0001 0000
	0x050D	0000 0000 0000 0001	0x0503	0000 0001 0000 0000
	0x010E	0000 0000 0000 0000	0x0104	0000 0000 0000 0000
	0x030E	0000 0000 0000 0000	0x0304	0000 0000 0001 0000
	0x050E	0000 0000 0000 0000	0x0504	0000 0001 0000 0000
	0x0120, 0x320, 0x0520	0000 0000 0010 0000	0x0128, 0x328, 0x0528	0000 0000 0010 0000
STS-3c/STM-1 (TU3) E3 Timeslots 1 (Master), 5, 9 on Channel 0, 1, 2 respectively	0x0101, 0x0301, 0x0501	0000 0000 0000 0000	0x0100, 0x0300, 0x0500	0000 0000 0000 0000
	0x0105	0000 0000 0000 0001	0x0102	0000 0000 0000 0001
	0x0305	0000 0000 0001 0000	0x0302	0000 0000 0001 0000
	0x0505	0000 0001 0000 0000	0x0502	0000 0001 0000 0000
	0x010D	0000 0000 0000 0001	0x0103	0000 0000 0000 0000
	0x030D	0000 0000 0000 0001	0x0303	0000 0000 0001 0000
	0x050D	0000 0000 0000 0001	0x0503	0000 0001 0000 0000
	0x010E	0000 0000 0000 0000	0x0104	0000 0000 0000 0000
	0x030E	0000 0000 0000 0000	0x0304	0000 0000 0001 0000
	0x050E	0000 0000 0000 0000	0x0504	0000 0001 0000 0000
	0x0120, 0x320, 0x0520	0000 0000 0000 0000	0x0128, 0x328, 0x0528	0000 0000 0000 0000
STS-12c/STM-4-4c Direct Mapped Timeslot 1 (Master) on Channel 0	0x0101	0000 0000 0000 0011	0x0100	0000 0000 0000 0011
	0x0105	0000 1111 1111 1111	0x0102	0000 1111 1111 1111
	0x010D	0000 0000 0000 0001	0x0103	0000 1111 1111 1110
	0x010E	0000 0000 0000 1110	0x0104	0000 0000 0000 1110
STS-1-2v Direct Mapped Timeslot 1 (Master) for 1v, Timeslot 4 (Master) for 2v. Channel 0	0x0101	0000 0000 0000 0011	0x0100	0000 0000 0000 0011
	0x0105	0000 0000 0001 0001	0x0102	0000 0000 0001 0001
	0x010D	0000 0000 0000 0000	0x0103	0000 0000 0000 0000
	0x010E	0000 0000 0000 0000	0x0104	0000 0000 0000 0000
STS-3c-2v Direct Mapped Timeslot 1 (Master), 2, 3 for 1v Timeslot 5 (Master), 6, 7 for 2v Channel 0	0x0101	0000 0000 0000 0011	0x0100	0000 0000 0000 0011
	0x0105	0000 0000 0111 0111	0x0102	0000 0000 0111 0111
	0x010D	0000 0000 0000 0000	0x0103	0000 0000 0110 0110
	0x010E	0000 0000 0000 0000	0x0104	0000 0000 0000 0000

Operating Mode (For slice N add N*0x200 to Address)	S/UNI-12xJET Channel Register Values			
	Receive TX STI / D3E3MD		Transmit TX STI / D3E3MA	
	Address(es) (in Hex)	Data (in binary)	Address(es) (in Hex)	Data (in binary)
Arbitrary Mode of operation	See comments below 1			

Notes:

1. Arbitrary STS-1 granularity processing is also available for a given channel with SONET/SDH Fixed Stuffs inserted at software programmable locations. Please refer to Channel Transmit/Receive Timeslot Configuration Registers for configuration.

In Table 21, for STS-3c/STM-1 modes, channels 0, 1, 2 are used to process the three data streams in all TU3 modes, AU3-DS3 mode, and AU3-E3 mode.

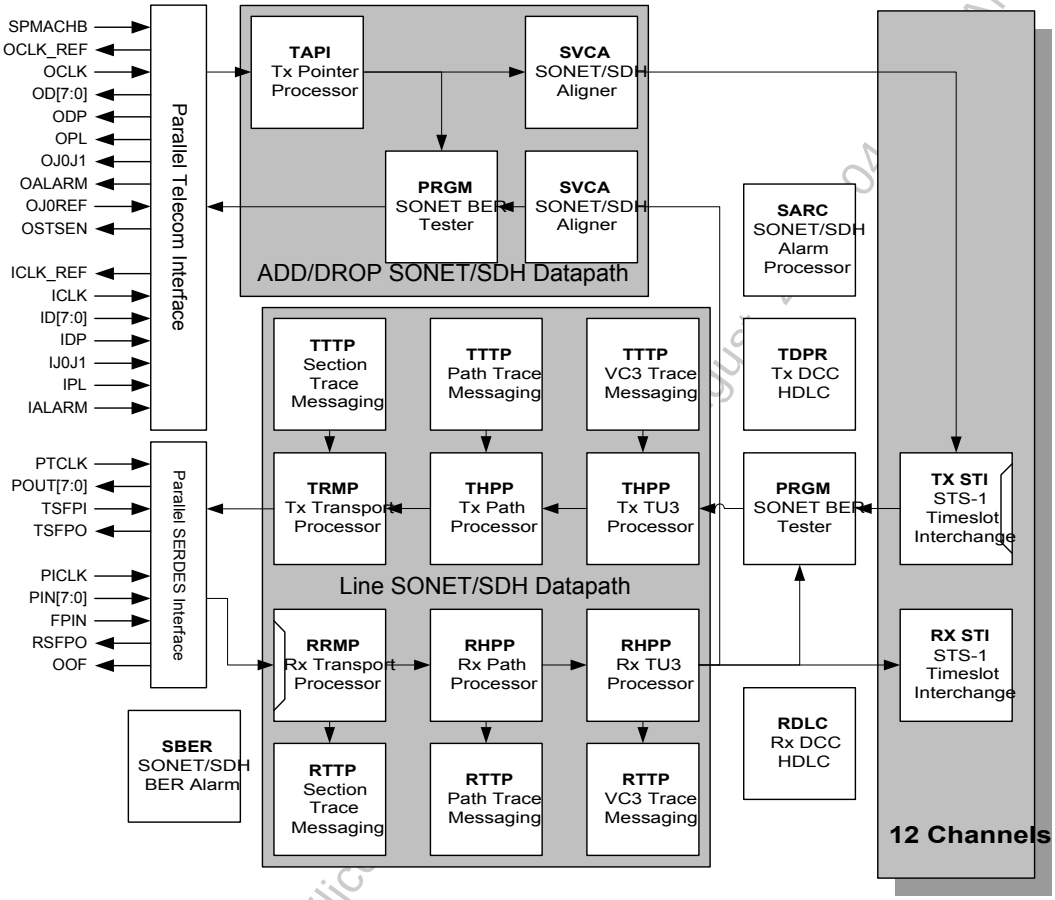
13.6 SONET/SDH Configurations

The SONET/SDH line side has two main modes of operation which are selected based on the value of the SPMACHB input pin. The SPMACHB input pin affects the functionality of the Parallel TelecomBus as well as what portions of the SONET/SDH blocks are in operation. The SONET/SDH blocks are broken into two main data paths, ADD/DROP and LINE. The ADD/DROP data path consists of the TAPI, PRGM, and SVCA blocks. The LINE data path includes the TRMP, THPP, RRMP and RHPP blocks.

13.6.1 Spectra Mode

When SPMACHB is high, the S/UNI-12xJET operates similar to a SPECTRA device. The Parallel TelecomBus is connected directly to the ADD/DROP data path. The ADD data path is routed through each channel's TX STI block and then through the transmit LINE data path to the transmit SERDES interface. Data from the ADD data path may be overwritten by any of the channels before being sent out the transmit LINE data path. The receive SERDES interface is connected to the receive LINE data path which sources data into all of the channels and is broadcast to the DROP data path. A diagram of SPECTRA Mode is shown in Figure 48.

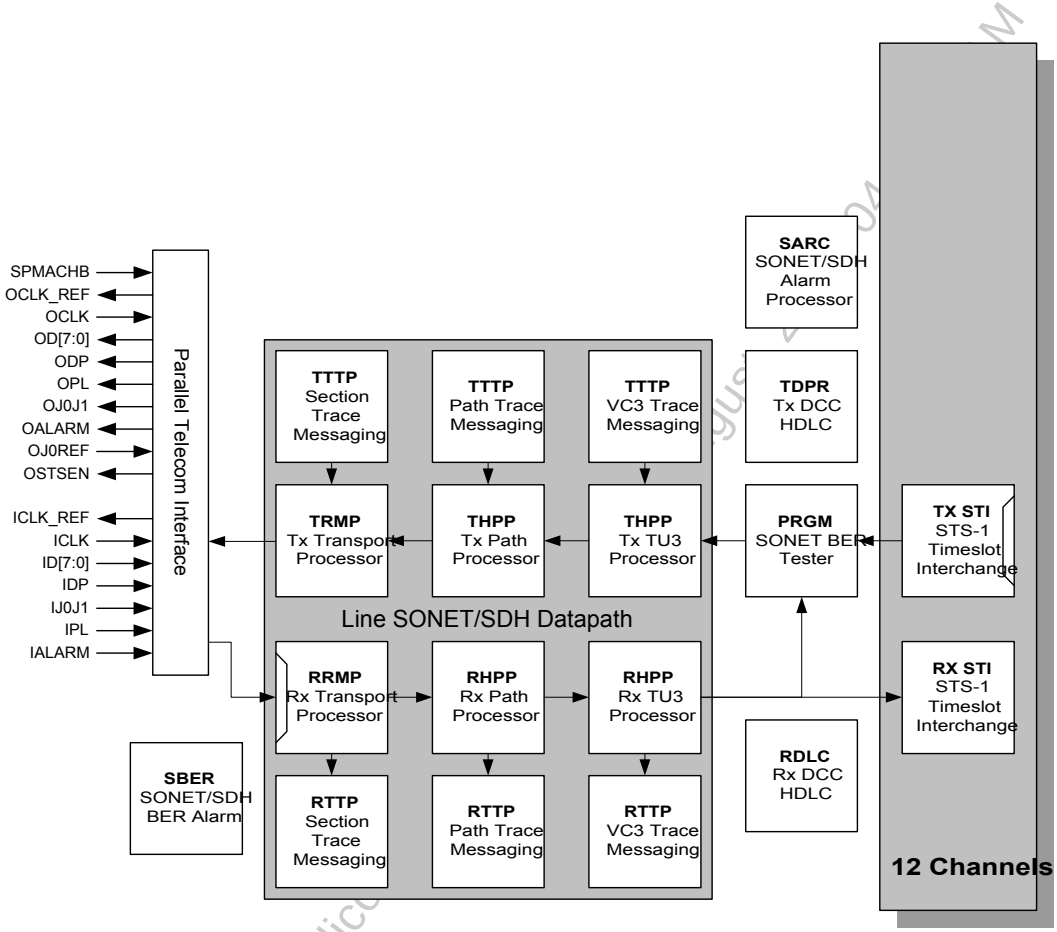
Figure 48 SONET/SDH SPECTRA Mode



13.6.2 Mach Mode

When SPMACHB is low, the S/UNI-12xJET operates similar to a S/UNI-MACH device. The Parallel TelecomBus is connected directly to the LINE data path. In this mode, the SERDES interface is unused, and the ADD/DROP SONET/SDH data path is put in a power savings mode, making the TAPI, PRGM and both SVCAs inoperable. The MACH mode is illustrated in Figure 49.

Figure 49 SONET/SDH MACH Mode



13.6.3 Parallel TelecomBus Interface

The Parallel TelecomBus has the ability to provide tristate control on the outgoing TelecomBus. Using the S/UNI-12xJET Transmit Timeslot Enable Register (0x180D) each timeslot is enabled using the associated STSEN[12:1] bit. When the TTBZ bit is set to zero and the current timeslot is not enabled (timeslot X, STSEN[X] = '0'), OSTSEN is driven to logic 0 and the outgoing parallel TelecomBus signals (OD[7:0], OPL, ODP) are held in tristate. Otherwise, OSTSEN is driven to logic 1 and the outgoing TelecomBus is driven to the values specified by that particular timeslot. This tristate functionality provides a glueless interface with other devices requiring a tristate TelecomBus, such as the TEMUX-84 (PM8316) for T1/E1 over SONET/SDH.

13.6.4 Line Data path Configurations

The Transmit and Receive Line Data paths are configurable such that all or any of the processors may be bypassed. When a processor is bypassed, all data and control pass through the processor without manipulation. The bypasses are used when particular processors are not required because the functionality is performed outside the S/UNI-12xJET. For example, the RRMP and TRMP may be bypassed in MACH Mode to allow an external processor to handle Section and Line Processing.

The RRMP and TRMP must not be bypassed in Spectra mode, because we need to find the J1/J0 locations.

13.7 Loopback Modes

13.7.1 Diagnostic Loopbacks

As shown in Figure 11, there are five main diagnostic loopback modes.

Parallel TelecomBus Diagnostic Loopback (1A, 1B)

Parallel Telecom loopback is configured using TCOM_DLE in 0x180B S/UNI-12xJET Master Loopback Configuration register. Mode 1A is the loopback used when SPMACHB is asserted (Spectra Mode) and mode 1B is the loopback used when SPMACHB is de-asserted (MACH Mode). When using Parallel TelecomBus Diagnostic Loopback in MACH mode, either the TRMP and RRMP must be bypassed with descrambling off, or the (0x1FF4) S/UNI-12xJET Receive SERDES Synchronization Delay register SERDES J0 Delay register must be set appropriately.

TRMP Diagnostic Loopback (2)

TRMP Diagnostic Loopback serves as the only diagnostic loopback for the SERDES interface. This loopback is configured using TRMP_DLE in 0x180B S/UNI-12xJET Master Loopback Configuration register. This loopback is available in both SPECTRA and MACH mode, and takes precedence over the Parallel TelecomBus Diagnostic Loopback in MACH mode.

TX STI Diagnostic Loopback (3)

TX STI Diagnostic loopback allows looping back data from the TXSTI interface to the RXSTI interface. This affects all channels. The TX STI Diagnostic loopback is configured using TXSTI_DLE in 0x180B S/UNI-12xJET Master Loopback Configuration register.

RJAT Diagnostic Loopback (4)

RJAT Diagnostic loopback is a channelized loopback, meaning each channel may be independently configured. The RJAT diagnostic loopback is performed before the serial cross connect, thus will always loop back to the same slice's TJAT. RJAT Diagnostic Loopback is configured using the DIAG bit in RJAT Configuration Register (0x1B0)

TXXP Diagnostic Loopback (5A, 5B)

the TXXP Diagnostic loopback is configured using TXXPDLE in 0x10C Channel Loopback Configuration Register. The TXXP diagnostic loopback is also a channelized loopback, meaning each channel may be independently configured. Mode 5A is the loopback used when packet processing is performed. Mode 5B is the loopback when cell processing is performed.

13.7.2 Line Loopbacks

As shown in Figure 12, there are five line loopback modes.

Parallel TelecomBus Line Loopback (1)

Parallel Telecom line loopback is configured using TCOM_LLE in 0x180B S/UNI-12xJET Master Loopback Configuration register. Both ICLK and OCLK must be connected and phase aligned outside the S/UNI-12xJET for this loopback to operate properly. This loopback operates the same in both Spectra and MACH modes (SPMACHB)

TJAT Line Loopback (2)

TJAT line loopback is a channelized loopback, meaning each channel may be independently configured. The TJAT line loopback is performed after the serial cross connect. TJAT line loopback is configured using the DIAG bit in TJAT Configuration Register (0x1B8)

Payload Line Loopback (3)

The Payload Line loopback is a channelized loopback, meaning each channel may be independently configured. The Payload Line loopback is performed from the FRMR block to the TRAN block, and is configured using the PLOOP bit in Channel Configuration #1 Register (0x000).

13.8 PLCP Frame Formats

The S/UNI-12xJET provides support for four different PLCP frame formats: the DS3 PLCP format, the DS1 frame format, the G.751 E3 frame format, and the E1 frame format. The structure of each of these formats is quite similar, and is illustrated in Figure 50 through Figure 53.

Figure 50 DS3 PLCP Frame Format

A1	A2	P11	Z6	ATM Cell	
A1	A2	P10	Z5	ATM Cell	
A1	A2	P9	Z4	ATM Cell	
A1	A2	P8	Z3	ATM Cell	
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	PLCP Frame Rate 125 μs
A1	A2	P5	F1	ATM Cell	
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	Trailer
Framing (3 octets)			POH	53 octets	13 or 14 nibbles

The DS3 PLCP frame provides the transmission of 12 ATM cells every 125 µs. The PLCP frame is nibble aligned to the overhead bits in the DS3 frame; however, there is no relationship between the start of the PLCP frame and the start of the DS3 M-frame. A trailer is inserted at the end of each PLCP frame. The number of nibbles inserted (13 or 14) is varied continuously such that the resulting PLCP frame rate can be locked to an 8 kHz reference.

Figure 51 DS1 PLCP Frame Format

A1	A2	P9	Z4	ATM Cell	
A1	A2	P8	Z3	ATM Cell	
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	PLCP Frame Rate 3 ms
A1	A2	P5	F1	ATM Cell	
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	Trailer
Framing (3 octets)			POH	53 octets	6 octets

The DS1 PLCP frame provides the transmission of 10 ATM cells every 3 ms. The PLCP frame is octet aligned to the framing bit in the DS1 frame; there is no relationship between the start of the PLCP frame, and the start of the DS1 frame. A trailer is inserted at the end of each PLCP frame. The number of octets inserted is always six, and cannot be varied.

Figure 52 G.751 E3 PLCP Frame Format

A1	A2	P8	Z3		
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	
A1	A2	P5	F1	ATM Cell	PLCP Frame Rate 125 μs
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	Trailer
Framing (3 octets)			POH	53 octets	17,18,19,20, or 21 octets

The G.751 E3 PLCP frame provides the transmission of 9 ATM cells every 125 µs. The PLCP frame is octet aligned to the 16 overhead bits in the ITU-T Recommendation G.751 E3 frame; there is no relationship between the start of the PLCP frame, and the start of the E3 frame. A trailer is inserted at the end of each PLCP frame. The number of octets inserted is nominally 18, 19, or 20, and is based on the number of E3 overhead octets (4, 5, or 6) that have been inserted during the PLCP frame period. The nominal octet stuffing can be varied by ±1 octet to allow the E3 PLCP frame to be locked to an external 8 kHz reference. Thus the trailer can be 17, 18, 19, 20, or 21 octets in length.

Figure 53 E1 PLCP Frame Format

A1	A2	P9	Z4	ATM Cell	
A1	A2	P8	Z3	ATM Cell	
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	PLCP Frame Rate 2.375 ms
A1	A2	P5	F1	ATM Cell	
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	
Framing (3 octets)			POH	53 octets	

The E1 PLCP frame provides the transmission of 10 ATM cells every 2.375 ms. Thirty of the thirty-two available E1 channels are used for transporting the PLCP frame. The remaining two channels are reserved for E1 framing and signaling functions. The PLCP frame is octet aligned to the channel boundaries in the E1 frame. The PLCP frame is aligned to the 125 µs E1 frame (the A1 octet of the first row of the PLCP frame is inserted in timeslot 1 of the E1 frame).

13.8.1 PLCP Path Overhead Octet Processing

Table 22 PLCP Overhead Processing

Overhead Field	Transmit Operation	Receive Operation
A1, A2: Frame Alignment Pattern	Inserts the PLCP frame alignment pattern (F628H)	Searches the receive stream for the PLCP frame alignment pattern. When the pattern has been detected for two consecutive rows, along with two valid, and sequential path overhead identifier octets, the S/UNI-12xJET declares in-frame. Note that the ATM cell boundaries are implicitly known when the PLCP frame is located, thus cell delineation is accomplished by locating the PLCP frame. When errors are detected in both octets in a single row, or when errors are detected in two consecutive path overhead identifier octets, the S/UNI-12xJET declares an out-of-frame defect. The loss-of-frame defect is an integrated version of the out-of-frame defect state.
PO-P11: Path Overhead Identifier	Inserts the path overhead identifier codes in accordance with the PLCP frame alignment. See Table 23.	Identifies the PLCP path overhead bytes by monitoring the sequence of the POI bytes.
Z1-Z6: Growth:	These octets are unused and are nominally programmed with all zeros. Access to these octets is provided by the PLCP transmit overhead access port.	These octets are ignored and are extracted on the RPH pin.
F1: User Channel	This octet is unused and the value inserted in this octet is controlled by an internal register or by TPH pin.	This octet is ignored and is extracted on the RPH pin.
B1: Bit Interleaved Parity	This octet contains an 8-bit interleaved parity (BIP) calculated across the entire PLCP frame (excluding the A1, A2, Pn octets and the trailer). The B1 value is calculated based on even parity and the value inserted in the current frame is the BIP result calculated for the previous frame.	The bit interleaved parity is calculated for the current frame and stored. The B1 octet contained in the subsequent frame is extracted and compared against the calculated value. Differences between the two values provide an indication of the end-to-end bit error rate. These differences are accumulated in a counter in the CPPM block.
G1: Path Status	The first four bit positions provide a PLCP far end block error function and indicates the number of B1 errors detected at the near end. The FEBE field has nine legal values (0000b-1000b) indicating between zero and eight B1 errors. The fifth bit position is used to transmit PLCP yellow alarm. The last three bit positions provide the link status signal used in IEEE-802.6 DQDB implementations. Yellow alarm and link status signal	The G1 byte provides the PLCP FEBE function and is accumulated in an a counter in the CPPM block. PLCP yellow alarm is detected or removed when the yellow bit is set to logic one or zero for ten consecutive frames. The yellow alarm state and the link status signal state are contained in the SPLR Status register.

Overhead Field	Transmit Operation	Receive Operation
	insertion is controlled by the internal registers or by TPH pin.	
M1, M2: Control Information	These octets carry the DQDB layer management information. Internal register controls the nominal value inserted in these octets. These octets are unused in ATM Forum T3 UNI 3.0 specification.	These octets are ignored and are extracted on the RPH pin.
C1: Cycle/Stuff Counter	The coding of this octet depends on the PLCP frame format. For DS1 and E1 PLCP formats, this octet is programmed with all zeros. For the DS3 PLCP format, this octet indicates the number of stuff nibbles (13 or 14) at the end of each PLCP frame. The C1 value is varied in a three frame cycle where the first frame always contains 13 stuff nibbles, the second frame always contains 14 nibbles, and the third frame contains 13 or 14 nibbles. The stuffing may be varied by a nibble so that the PLCP frame rate can be locked to an external 8 kHz timing reference from REF8KI, a loop-timed 8 kHz reference, or fixed stuffing via the FIXSTUFF bit in the SPLT Configuration Register. See Table 24. For the G.751 E3 PLCP format, this octet indicates the number of stuff octets (17 to 21) at the end of the PLCP frame. Depending on the alignment of the G.751 E3 frame to the E3 PLCP frame, 18, 19 or 20 octets are nominally stuffed. The stuffing may be varied by ±1 octet so that the PLCP frame rate can be locked to an external 8 kHz timing reference from REF8KI. The S/UNI-12xJET also supports fixed timing using the FIXSTUFF bit in the SPLT Configuration Register. See Table 25.	Interprets the trailer length according to the selected PLCP frame format and the received C1 code.

Table 23 PLCP Path Overhead Identifier Codes

POI	POI Code (Hex)
P11	2C
P10	29
P9	25
P8	20
P7	1C
P6	19
P5	15
P4	10
P3	0D
P2	08
P1	04
P0	01

Table 24 DS3 PLCP Trailer Length

C1(Hex)	Frame/Trailer Length
FF	1 (13 Nibbles)
00	2 (14 Nibbles)
66	3 (13 Nibbles)
99	3 (14 Nibbles)

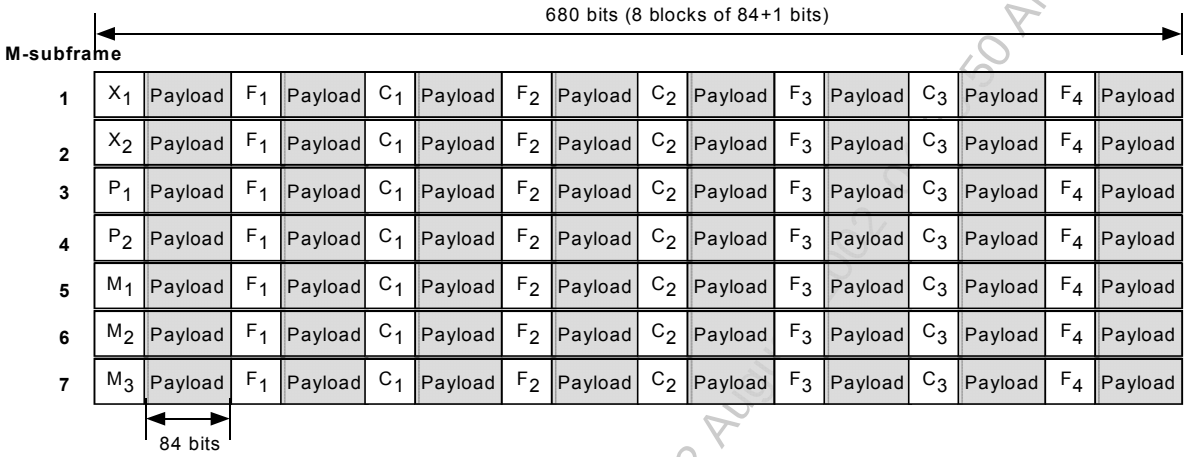
Table 25 E3 PLCP Trailer Length

C1(Hex)	Trailer Length
3B	17 octets
4F	18 octets
75	19 octets
9D	20 octets
A7	21 octets

13.9 DS3 Frame Format

The S/UNI-12xJET supports both M23 and C-bit parity DS3 framing formats. This format can be extended to support direct byte mapping or PLCP mapping of ATM cells. An overview of the DS3 frame format is shown in Figure 54.

Figure 54 DS3 Frame Structure



The DS3 receiver decodes a B3ZS-encoded signal and provides indications of line code violations (LCVs). The B3ZS decoding algorithm and the LCV definition are software selectable.

While in-frame, the DS3 receiver continuously checks for line code violations, M-bit or F-bit framing bit errors, and P-bit parity errors. When C-bit parity mode is selected, both C-bit parity errors and far end block errors are accumulated.

When the C-bit parity framing format is detected, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted. HDLC messages in the Path Maintenance Data Link are received by an internal data link receiver.

The DS3 transmitter allows for the insertion of the overhead bits into a DS3 bit stream and produces a B3ZS-encoded signal. Status signals such as far end receive failure (FERF), the alarm indication signal (AIS) and the idle signal can be inserted when the transmission of these signals is enabled

The processing of the overhead bits in the DS3 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH, TOHINS, TOHFA, and OHCLK signals. In the receive direction, most of the overhead bits our brought out serially on the ROH data stream.

Table 26 DS3 Frame Overhead Operation

Control Bit	Transmit Operation	Receive Operation
Xx: X-Bit Channel	Inserts the FERF signal on the X-bits.	Monitors and detects changes in the state of the FERF signal on the X-bits.
Px: P-Bit Channel	Calculates the parity for the payload data over the previous M-frame and inserts it into the P1 and P2 bit positions.	Calculates the parity for the received payload. Errors are accumulated in internal registers.
Mx:	Generates the M-frame alignment	Finds the M-frame alignment by searching

Control Bit	Transmit Operation	Receive Operation
M-Frame Alignment Signal	signal (M1=0, M2=1, M3=0).	for the F-bits and the M-bits. Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Fx: M-subframe Alignment Signal	Generates the M-subframe signal (F1=1, F2=0, F3=0, F4=1).	Finds M-frame alignment by searching for the F-bits and the M-bits. Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Cx: C-Bit Channels	M23 Operation: The C bits are passed through transparently in M23 framer only mode except for the C-bit Parity ID bit which toggles every M-frame. In M23 ATM applications, the C bits other than the Parity ID bit are forced to logic 1. C-bit Parity Operation: The C-bit Parity ID bit is forced to logic 1. The second C-bit in M-subframe 1 is set to logic 1. The third C-bit in M-subframe 1 provides a far-end alarm and control (FEAC) signal. The FEAC channel is sourced by the XBOC block. The 3 C-bits in M-subframe 3 carry path parity information. The value of these 3 C-bits is the same as that of the P-bits. The 3 C-bits in M-subframe 4 are the FEBE bits. The 3 C-bits in M-subframe 5 contain the 28.2 Kbit/s path maintenance data link. The remaining C-bits are unused and set to logic 1.	The state of the C-bit parity ID bit is stored in a register. This bit indicates whether an M23 or C-bit parity format is received. C-bit Parity Operation: The FEAC channel on the third C-bit in M-subframe 1 is detected by the RBOC block. Path parity errors and FEBEs on the C-bits in M-subframes 3 and 4 are accumulated in counters. The path maintenance data link signal is extracted by the receive HDLC controller.

13.10 G.751 E3 Frame Format

The S/UNI-12xJET provides support for the G.751 E3 frame format. This format can be extended to allow for direct byte mapping or PLCP mapping of ATM cells. The G.751 E3 frame format is shown in Figure 55.

Figure 55 G.751 E3 Frame Structure

1	1	1	1	0	1	0	0	0	0	RAI	Na	372 Payload bits
C_{11}	C_{21}	C_{31}	C_{41}	380 Payload bits								
C_{12}	C_{22}	C_{32}	C_{42}	380 Payload bits								
C_{13}	C_{23}	C_{33}	C_{43}	J_1	J_2	J_3	J_4	376 Payload bits				

The processing of the overhead bits in the G.751 E3 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH, TOHINS, TOHFA, and OHCLK signals. In the receive direction, most of the overhead bits are brought out serially on the ROH data stream.

When used to transport ATM cells in either ATM direct mapping mode or with PLCP framing, bits 13, 14, 15 and 16 of the E3 frame (directly following the RAI and Na bits) are set to 1, 1, 0 and 0.

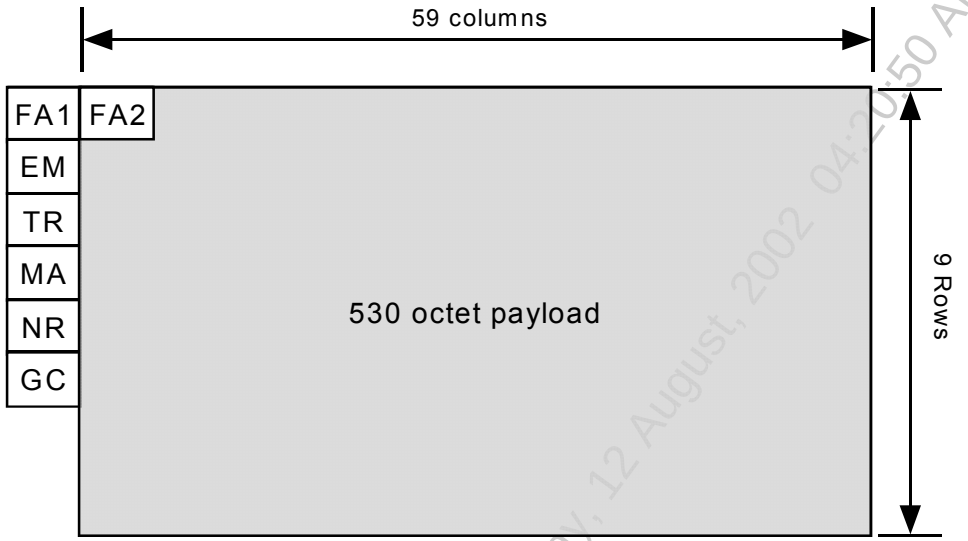
Table 27 G.751 E3 Frame Overhead Operation

Control Bit	Transmit Operation	Receive Operation
Frame Alignment Signal	Inserts the frame alignment signal 1111010000b.	Finds frame alignment by searching for the frame alignment signal. When the pattern has been detected for three consecutive frames, an in-frame condition is declared. When errors are detected in four consecutive frames, an out-of-frame condition is declared.
RAI: Remote Alarm Indication	Optionally asserts the RAI signal under a register control or when LOS, OOF, AIS and LCD conditions are detected.	Extracts the RAI signal and outputs it on the ROH output pin. The state of the RAI signal is also written to a register bit.
Na: National Use Bit	Asserts the National Use bit under a register control or from the internal HDLC controller.	Extracts the National Use bit and stores the value in a register bit.
Cjk: Justification Service Bits	When the device is configured as an E3 G.751 framer device, the Justification Service Bits can be inserted on the TDATI[x] input pin the same way as normal payload data. When the device is configured for ATM application, the Justification Service Bits are used as payload bits.	Extracts the Justification Service Bits on the ROH output pin when the Cjk bits are configured as overhead.
Jk: Tributary Justification Bits	When the device is configured as a E3 G.751 framer, the Tributary Justification Bits can be inserted on the TDATI[x] input pin the same way as normal payload data. When the device is configured for ATM application, the Tributary Justification Bits are used a payload bits.	Extracts the Tributary Justification Bits on the ROH output pin when the Jk bits are configured as overhead.

13.11 G.832 E3 Frame Format

The S/UNI-12xJET provides support for the G.832 E3 frame format. This format can be extended to allow for direct byte mapping of ATM cells. The G.832 E3 frame format is shown in Figure 56.

Figure 56 G.832 E3 Frame Structure



The processing of the overhead bits in the G.832 E3 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH, TOHINS, TOHFA, and OHCLK signals. In the receive direction, the overhead bits are brought out serially on the ROH data stream.

Table 28 G.832 E3 Frame Overhead Operation

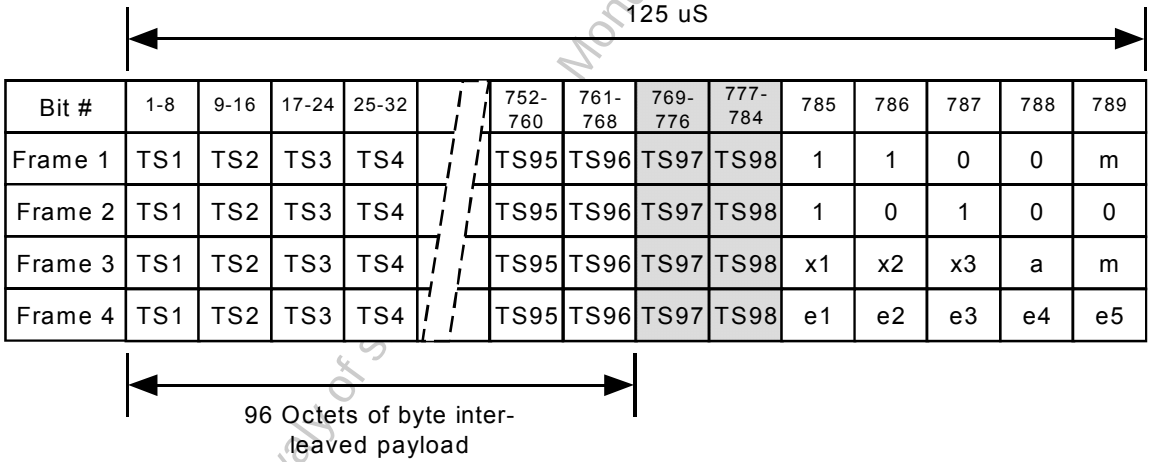
Control	Transmit Operation	Receive Operation
FA1, FA2: Frame Alignment Pattern	Inserts the G.832 E3 frame alignment pattern (F628H).	Searches the receive stream for the G.832 E3 frame alignment pattern. When the pattern is detected for two consecutive frames, an in-frame condition is declared. Note that there is no ATM cell alignment with the G.832 E3 frame. Therefore cell delineation must be performed to locate the ATM cell boundaries.
EM: Error Monitor, BIP-8	Inserts the calculated BIP-8 by computing even parity over all transmit bits, including the overhead bits of the previous 125 µs frame.	Computes the incoming BIP-8 value over one 125 µs frame. The result is held and compared against the value in the EM byte of the subsequent frame.
TR: Trail Trace	Inserts the 16 byte trail access point identifier specified in internal registers.	Extracts the repetitive trail access point identifier and verifies that the same pattern is received. Compares the received pattern to the expected pattern programmed in a register.
MA: Maintenance and Adaptation Byte	Inserts the FERF, FEBE, Payload Type bits, Tributary Unit Multi-frame Indicator bits and the Timing Marker bit as programmed in a register or as indicated by detection of receive OOF or BIP-8 errors.	Extracts and reports the FERF bit value when it has been the same for 3 or 5 consecutive frames. S/UNI-12xJET also extracts and accumulates FEBE occurrences and extracts the Payload Type, and Timing Market indicator bits and reports them through microprocessor accessible registers.
NR: Network Operator	Inserts the Network Operator byte from the TOH overhead stream or optionally	Extracts the Network Operator byte and outputs it on ROH or optionally terminates it in

Control	Transmit Operation	Receive Operation
Byte	from the TDPR. All 8 bits of the Network Operator byte are inserted from TOH or from the TDPR.	the RDLC. All 8 bits of the Network Operator byte are extracted and presented on ROH or to the RDLC.
GC: General Purpose Communication Channel	Inserts the GC byte from the TOH overhead stream or optionally from the TDPR block.	Extracts the GC byte and outputs it on ROH or optionally terminates it in the RDLC block.

13.12 J2 Frame Format

The S/UNI-12xJET provides support for the G.704 and NTT J2 frame format. This format can be extended to allow for direct byte mapping of ATM cells as specified in G.804. The J2 frame format consists of 789 bits frames each 125 us long, consisting of 96 bytes of payload, 2 reserved bytes, and 5 F-bits. The frames are grouped into 4 frame multi-frames as shown in Figure 57.

Figure 57 J2 Frame Structure



The J2 framer decodes a unipolar or B8ZS encoded signal and frames to the resulting 6,312 Kbit/s J2 bit stream. Once in frame, the J2 framer provides indications of frame and multi-frame boundaries and marks overhead bits, x-bits, m-bits and reserved channels (TS97 and TS98). Indications of loss of signal, bipolar violations, excessive zeroes, change of frame alignment, framing errors, and CRC errors are provided and accumulated in internal counters.

The J2 transmitter inserts the overhead bits into a J2 bit stream and produces a B8ZS-encoded signal. The J2 transmitter adheres to the framing format specified in G.704 and NTT Technical Reference for High Speed Digital Leased Circuit Services.

The processing of the overhead bits in the J2 frame is described in the following table. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis by changing registers via the microprocessor interface. In the receive direction, the overhead bits are brought out serially on the ROH data stream.

Table 29 J2 Frame Overhead Operation

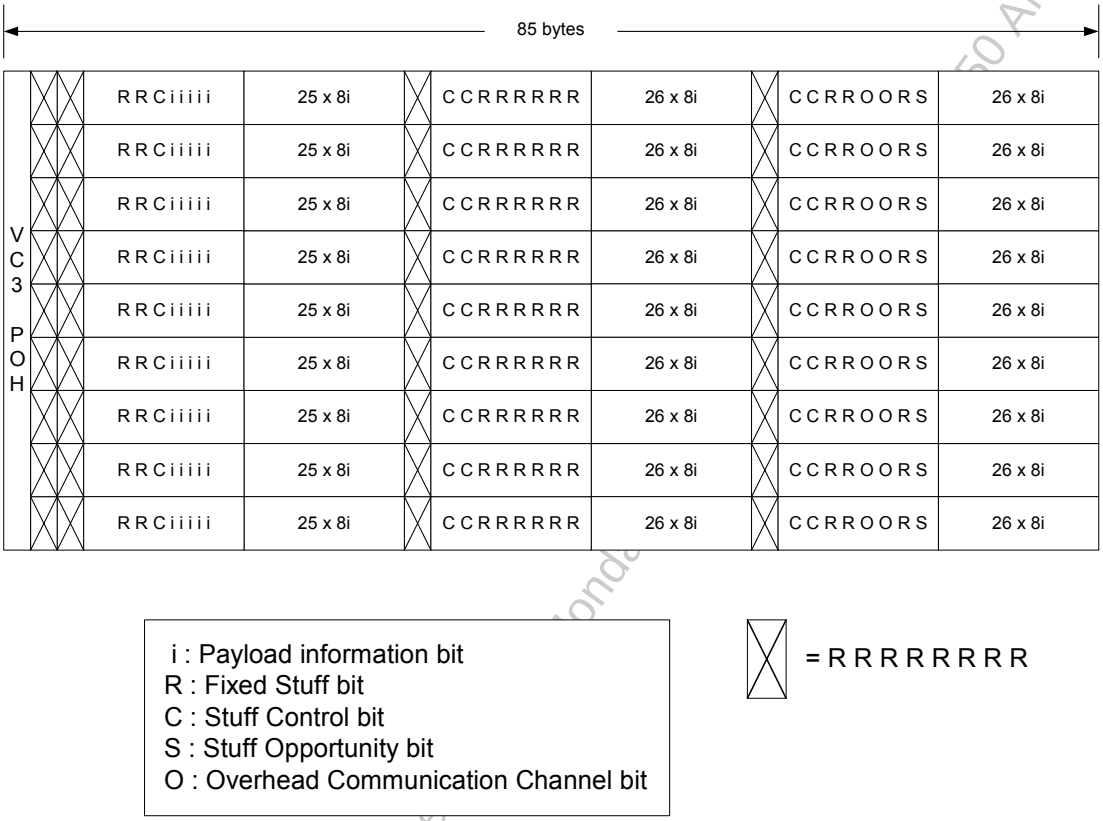
Control	Transmit Operation	Receive Operation
TS1-TS96: Byte Interleaved Payload	Inserts the ATM cells into TS1 to TS96 octets.	Extracts the ATM cell octet payload and performs cell delineation.
TS97-TS98: Signaling channels	Inserts the signaling bytes from either register bits or from the TOH and TOHINS inputs. These bits can be optionally inserted via TDATI input when in framer only mode.	Extracts signaling bytes on the ROH output.
Frame Alignment Signal	Inserts the frame alignment signal automatically.	Finds J2 frame alignment by searching for the frame alignment signal.
M-bits: 4kHz Data Link	Inserts the 4 kHz data link signal from the internal HDLC controller or from the bit oriented code generator.	Extracts the 4 kHz data link signal for the internal HDLC controller.
X-bits: Spare Bits	Inserts the spare bits via register bits or via TOH and TOHINS input pins.	Extracts and presents the x-bits on register bits. The X-bit states can be debounced and presented on the ROH output pin. An interrupt change can be generated to signal a change in the X-bit state.
A-bit: Remote Loss of Frame Indication	Inserts the A-bit via register bit. The A-bit can be optionally be asserted when the J2 framer is in loss of frame condition.	Extracts and presents the A-bit on a register bit. The A-bit state can be debounced and presented on the ROH output pin. An interrupt can be generated to signal a change in the A-bit state.
E1-E5: CRC-5 Check Sequence	Automatically calculates and inserts the CRC-5 check sequence.	Calculates the CRC-5 check sequence for the received data stream. Discrepancies with the received CRC-5 code can be configured to generate an interrupt. CRC-5 errors are accumulated in an internal counter.

13.13 DS3 into VC-3 Mapping Format

The S/UNI-12xJET provides support for the G.707 Asynchronous Mapping of 44, 736 kbits/s (DS3) into a VC-3. The DS3 contained within the VC-3 consists of 9 rows and 85 byte-wide columns. Each row may be regarded as a sub-frame. A sub-frame consists of 1 row containing 621 information bits, 5 stuff control bits, 1 stuff opportunity bit, and 2 overhead communication channel bits. Fixed stuff bytes are used to fill the remaining bytes.

A 3 out of 5 majority vote is used to determine if the incoming stuff control bits contain data or stuff bits. If 3 out of the 5 stuff control bits in a row are set to 1, the stuff opportunity bit for that row is a stuff bit. If 3 out of 5 stuff control bits in a row are set to 0, the stuff opportunity bit for that row contains data. This format is used to adapt the DS3 rate of 44.736 Mbps to that of the STS-1 SPE rate. The format of the incoming DS3 over VC-3 structure is shown in Figure 58 DS3 to VC-3 Mapping.

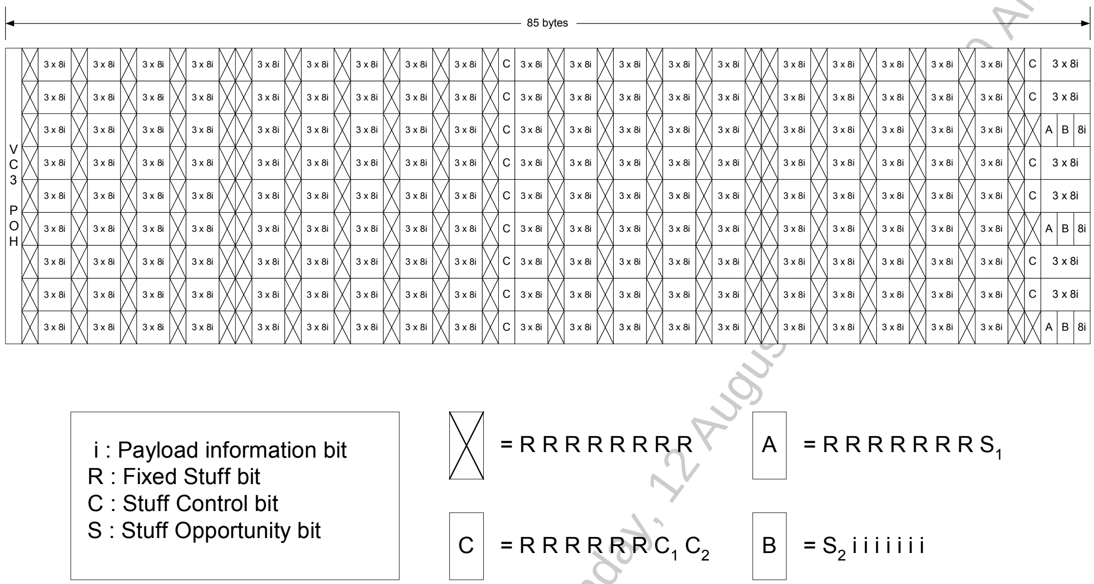
Figure 58 DS3 to VC-3 Mapping



13.14 E3 into VC-3 Mapping Format

The S/UNI-12xJET provides support for the G.707 Asynchronous Mapping of 34,368 kbits/s (E3) into a VC-3. The E3 over VC-3 data consists of 9 rows and 85 byte-wide columns. The 9 rows may be considered as 3 subframes within the VC-3. Each sub-frame consists of 3 rows containing 1431 information bits, 2 sets of 5 stuff control bits (C1, C2), and 2 stuff opportunity bits (S1, S2). Fixed stuff bytes are used to fill the remaining bits. Each set of 5 stuff control bits is associated with a stuff opportunity bit. A 3 out of 5 majority vote is used to determine if the stuff opportunity bits in the sub-frame are data or stuff bits. If 3 out of 5 C1 bits are set to 0, the S1 stuff opportunity bit is a data bit. If 3 out of 5 C1 bits set to 1, the S1 bit is a stuff bit. The same majority vote principle applies to the C2, S2 bits. This format is used to adapt the E3 rate of 34.368 Mbps to that of the STS-1 SPE rate. The asynchronous E3 to VC-3 mapping is shown in Figure 59.

Figure 59 E3 to VC-3 Mapping



13.15 DS3/E3 AIS

The S/UNI-12xJET provides AIS insertion/detection for both E3 and DS3 frames. The E3 AIS frame format adheres to ITU-G.751, and the DS3 AIS frame format adheres to ITU-G.704.

In E3 mode, the output data stream is overwritten with a continuous stream of 1's. In DS3 mode, the AIS pattern consists of repeating 4760 bit M frames, as shown in Figure 60. Each M frame consists of seven 680 bit M-subframes. The M-subframes are partitioned into 8 blocks of 1 overhead bit (X, P, M, F, or C) and 84 data bits (D). The DS3 AIS pattern is shown in Figure 60. The order of transmission is left to right, top to bottom.

Figure 60 DS3 AIS Signal

M-Subframe 680 bits

X_1	84D	F_1	84D	C_1	84D	F_2	84D	C_2	84D	F_3	84D	C_3	84D	F_4	84D
X_2	84D	F_1	84D	C_1	84D	F_2	84D	C_2	84D	F_3	84D	C_3	84D	F_4	84D
P_1	84D	F_1	84D	C_1	84D	F_2	84D	C_2	84D	F_3	84D	C_3	84D	F_4	84D
P_2	84D	F_1	84D	C_1	84D	F_2	84D	C_2	84D	F_3	84D	C_3	84D	F_4	84D
M_1	84D	F_1	84D	C_1	84D	F_2	84D	C_2	84D	F_3	84D	C_3	84D	F_4	84D
M_2	84D	F_1	84D	C_1	84D	F_2	84D	C_2	84D	F_3	84D	C_3	84D	F_4	84D
M_3	84D	F_1	84D	C_1	84D	F_2	84D	C_2	84D	F_3	84D	C_3	84D	F_4	84D

The DS3 AIS signal bits are set as follows:

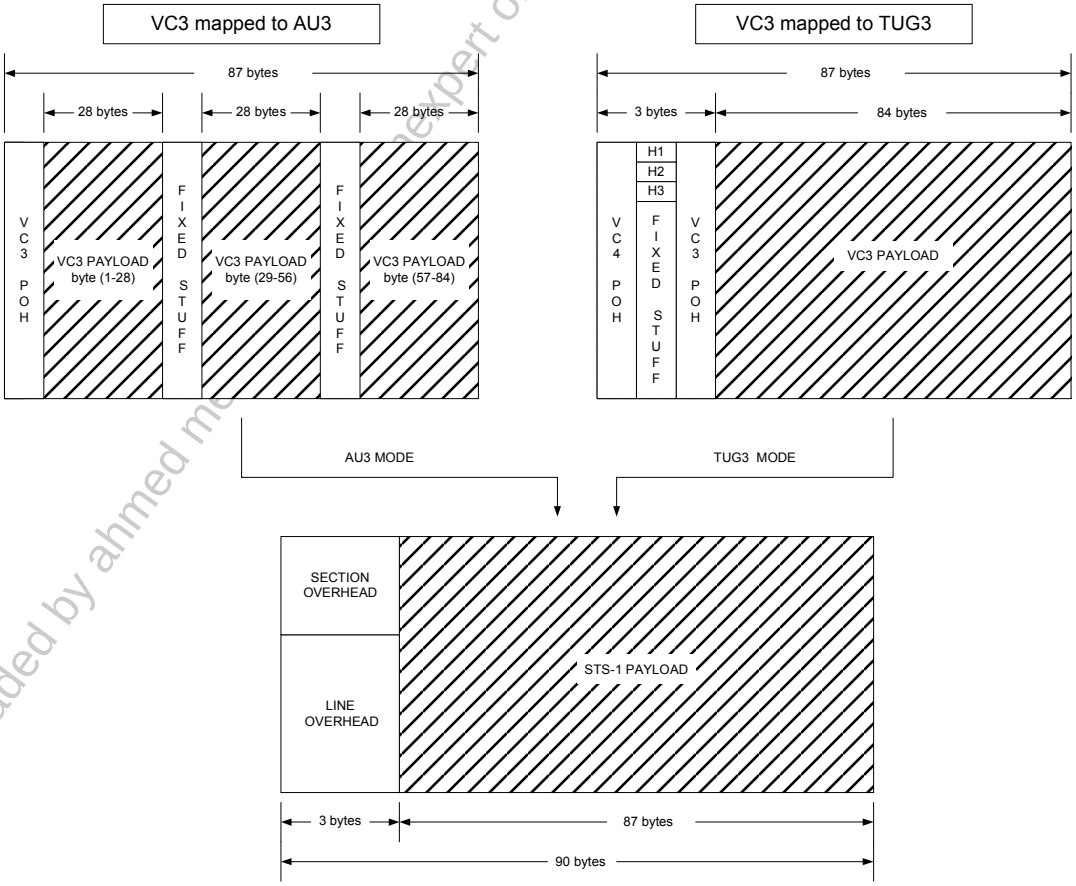
- The M-Frame alignments (M1 M2 M3) = (0 1 0).
- The M-Subframe alignment bits (F1 F2 F3 F4) = (1 0 0 1).
- The Overhead bits (C1 C2 C3) = (0 0 0).
- The Overhead bits (X1 X2) = (1 1).
- The P bits (P1 P2) = (0 0).
- The 84 D bits are set with the repeating pattern 1010…

13.16 Multiplexing of AU-3/TUG-3 into STS-1 Payload Format

The S/UNI-12xJET provides support for the G.707 Multiplexing of AU-3 or TUG-3 into an STS-1 payload. Both DS3 and E3 payloads are always mapped in a VC-3 before being mapped according to AU-3 or TUG-3 specifications

In AU-3 mode, the STS-1 payload contains 2 fixed stuff columns. These fixed stuff columns are located at the 29th and 58th columns in the STS-1 SPE. In TUG3 mode, the STS-1 payload contains 1 VC-4 POH (Path Overhead) column, and a column that consists of H1, H2, H3, and fixed stuff bytes. Figure 61 illustrates the multiplexing of the VC-3 mapped data into an AU-3/TUG-3 and multiplexed into an STS-1 Payload.

Figure 61 AU3 and TUG3 to STS-1 Mapping



13.17 UTOPIA Level 2 ATM Cell Data Structure

ATM cells may be passed to/from the S/UNI-12xJET using a 27 word, 16-bit UTOPIA level 2 compliant data structure. This data structure is shown in and described below.

Figure 62 16-bit Wide, 27 Word ATM Cell Structure

	Bit 15 … Bit 8	Bit 7 … Bit 0
Word 1	H1	H2
Word 2	H3	H4
Word 3	H5	HCS Status/Control
Word 4	Payload 1	Payload 2
Word 5	Payload 3	Payload 4
Word 6	Payload 5	Payload 6
Word 7	Payload 7	Payload 8
Word 8	Payload 9	Payload 10
	⋮	⋮
Word 27	Payload 47	Payload 48

Bit 15 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first two header octets). Word 3 of this structure contains the HCS octet in bits 15 to 8.

In the receive direction, the lower 8 bits of Word 3 contain the HCS status octet. An all-zeros pattern in these 8 bits indicates that the associated header is error free. An all-ones pattern indicates that the header contains an uncorrectable error (if the HCSPASS bit in the RXCP Control Register is set to logic zero, the all-ones pattern will never be passed in this structure). An alternating ones and zeros pattern (0xAA) indicates that the header contained a correctable error. In this case the header passed through the structure is the "corrected" header.

In the transmit direction, the HCS bit in the TXCP Control register determines whether the HCS is calculated internally or is inserted directly from the upper 8 bits of Word 3. The lower 8 bits of Word 3 contain the HCS control octet. The HCS control octet is an error mask that allows the insertion of one or more errors in the HCS octet. A logic one in a given bit position causes the inversion of the corresponding HCS bit position (for example a logic one in bit 7 causes the most significant bit of the HCS to be inverted). The HDCL control octet may be disabled by setting the HCSCTLEB register in the TXCP.

13.18 UTOPIA Level 3 ATM Cell Data Structure

ATM cells on the Level 3 interface use either a 52 byte, 32-bit UTOPIA Level 3 compliant data structure or a 56 byte, 32-bit UTOPIA Level 3 compliant data structure. The data structures are shown Figure 63 and Figure 64.

Figure 63 32-bit Wide, 52 Byte ATM Cell Structure

	Bit 31 Bit 24	Bit 23 Bit 16	Bit 15 Bit 8	Bit 7 Bit 0
Word 1	H1	H2	H3	H4
Word 2	Byte 1	Byte 2	Byte 3	Byte 4
Word 3	Byte 4	Byte 5	Byte 6	Byte 7
Word 4	Byte 8	Byte 9	Byte 10	Byte 11
Word 5	Byte 12	Byte 13	Byte 14	Byte 15
	⋮	⋮	⋮	⋮
Word 13	Byte 45	Byte 46	Byte 47	Byte 48

For the 56 byte ATM cell structure, bit 31 of each word is the most significant bit (which corresponds to the first bit transmitted). The HCS octet (H5) and HCS control bytes are passed through this structure to the TXCP block. The UDF bytes are ignored by the TUL3. The start of cell indications (TSOC and RSOC) are coincident with word 1 of the structure.

Figure 64 32-bit Wide, 56 Byte ATM Cell Structure

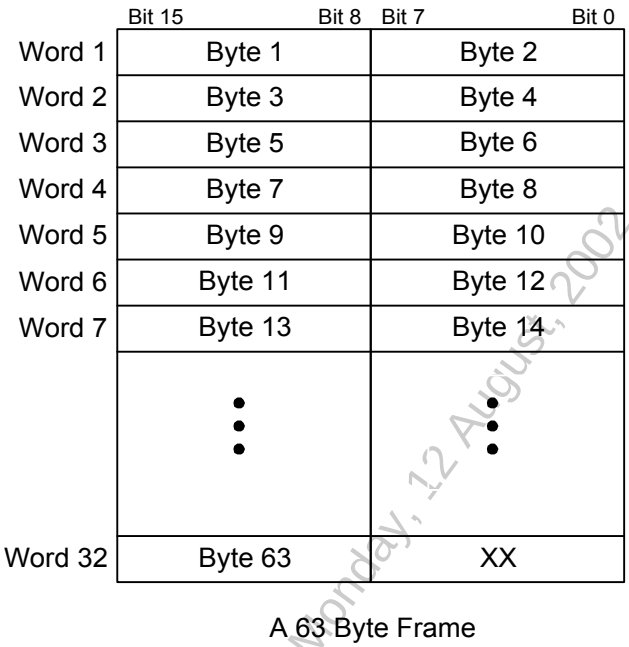
	Bit 31 Bit 24	Bit 23 Bit 16	Bit 15 Bit 8	Bit 7 Bit 0
Word 1	H1	H2	H3	H4
Word 2	H5	HCS Control	UDF	UDF
Word 3	Byte 1	Byte 2	Byte 3	Byte 4
Word 4	Byte 4	Byte 5	Byte 6	Byte 7
Word 5	Byte 8	Byte 9	Byte 10	Byte 11
Word 6	Byte 12	Byte 13	Byte 14	Byte 15
	⋮	⋮	⋮	⋮
Word 14	Byte 45	Byte 46	Byte 47	Byte 48

13.19 POS-PHY Level 2 Data Structure

Packets may be written into the TXFP FIFO and read from the RXFP FIFO using a 16-bit POS-PHY Level 2 defined data structure.

The 16-bit POS-PHY Level 2 data structure is shown in Figure 65. The packet length of 63 bytes is chosen arbitrarily for illustrative purposes only. Other lengths are acceptable. Octets are written in the same order they are to be transmitted or they were received on the SONET/SDH line. Within an octet, the MSB (bit 7) is the first bit to be transmitted. All words are composed of two octets, except the last word of a packet which can have one or two bytes. If the TXFP is configured to not insert the FCS field, then these bytes should be included at the end of the packet. Similarly, if the RXFP is configured to not strip the FCS field, then these bytes will be included at the end of the packet.

Figure 65 A 63 Byte Packet Data Structure



A 63 Byte Frame

13.20 POS-PHY Level 3 Data Structures

The 32-bit POS-PHY Level 3 packet data structure is shown in Figure 66. The packet length of 109 bytes is chosen arbitrarily for illustrative purposes only. Other lengths are acceptable.

Bit 31 of each word is the most significant bit (which corresponds to the first bit transmitted). Octets are written in the same order they are to be transmitted on the SONET line. The start of the packet is marked with TSOP/RSOP set high and the end of the packet is marked with TEOP/REOP set high. All words are composed of four octets, except the last word of a packet, which can have one, two, three or four bytes of valid data, determined by the TMOD[1:0]/RMOD[1:0] signals.

Both the start and the end of the packet are identified by the TSOP/RSOP and TEOP/REOP signals. In transmit direction, all packets marked with TERR and TEOP will be appended by the HDLC abort sequence by the TXFP block. In the receive direction, HDLC aborted packets, invalid packets, illegal length packets are marked by RERR and REOP.

Figure 66 32-Wide, 109 Byte Packet Data Structure

	Bit 31 … Bit 24	Bit 23 … Bit 16	Bit 15 … Bit 8	Bit 7 … Bit 0
Word 1	Byte 1	Byte 2	Byte 3	Byte 4
Word 2	Byte 5	Byte 6	Byte 7	Byte 8
Word 3	Byte 9	Byte 10	Byte 11	Byte 12
Word 4	Byte 13	Byte 14	Byte 15	Byte 16
Word 5	Byte 17	Byte 18	Byte 19	Byte 20
Word 6	Byte 21	Byte 22	Byte 23	Byte 24
	⋮	⋮	⋮	⋮
Word 28	Byte 109	XX	XX	XX

A 109 Byte Packet

When transferring ATM cells over the POS-PHY Level 3 interface, the UTOPIA ATM cell structures are used. The CELLFORM register bit defines the size of the ATM cell structure when a channel is configured for ATM traffic in POS-PHY operation. A single ATM cell structure may be transferred in multiple interface data bursts less than 52/56 bytes in size.

The first word of the ATM cell structure is marked by TSOP/RSOP and the last word of the structure is marked by TEOP/REOP. In the transmit direction, the ATM cell will be transmitted when the entire ATM cell structure is received. In the receive direction, the ATM cell structures will contain complete ATM cells. The TERR signal must be low at all times for the channel. RERR signal will be low at all times for the channel.

13.21 Resetting the RXFF and TXFF FIFOs

Resetting the receive and transmit FIFOs can be accomplished using the FIFORST bits (RXCP FIFO/UTOPIA Control & Configuration, TXCP Configuration 1 registers). When resetting, the FIFORST bit should be written with a logic 1, and held for two or more clock cycles (the longer of two Utopia clock cycles or 16 line clock cycles). After de-asserting FIFORST, data can be safely written to the TXFF after two or more clock cycles have passed.

13.22 Servicing Interrupts

The S/UNI-12xJET will assert INTB to logic 0 when a condition which is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

Read the INT[4:1] bits of the S/UNI-12xJET Clock Activity Monitor and Interrupt Identification register (007) to identify which quadrant of the S/UNI-12xJET produced the interrupt. For example, a logic one on the INT[3] register bit indicates that quadrant number 3 of the S/UNI-12xJET produced the interrupt.

Having identified the quadrant which produced the interrupt, read the S/UNI-12xJET Interrupt Status Register (005, 105, 205, and 305) to identify which block in the quadrant produced the interrupt. For example, a logic one on the TDPRI register bit in register 205H indicates that the TDPR block in quadrant number 3 of the S/UNI-12xJET produced the interrupt.

Service the interrupt.

If the INTB pin is still logic 0, then there are still interrupts to be serviced. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

13.23 Using the Performance Monitoring Features

The PMON and CPPM blocks are provided for performance monitoring purposes. The RXCP and TXCP also contain performance monitor registers. The PMON block is used to monitor DS3, E3, and J2 performance primitives while the CPPM is used to monitor PLCP and idle-cell-based primitives. The RXCP is used to monitor received cell primitives, and the TXCP is used to monitor transmit cell primitives. The counters in the PMON block have been sized as not to saturate if polled every second. The counters in the CPPM blocks have been sized as not to saturate if polled every 1/2 second at line rates up to 44.736 MHz. The counters in the RXCP and TXCP have been sized to not saturate if polled every second at line rates up to 44.736 MHz.

The DS3, E3, and J2 primitives can be accumulated independently of the PLCP and cell-based primitives. An accumulation interval is initiated by writing to one of the PMON event counter register addresses. After writing to a PMON count register, a number of RCLK clock periods (3 for J2 mode, 255 for DS3 mode, 500 for G.832 E3 mode, and 3 for G.751 E3 mode) must be allowed to elapse to permit the PMON counter values to be properly transferred. The PMON registers may then be read.

PLCP and cell-based primitives can be accumulated independent of the DS3, E3, or J2 primitives. An accumulation interval is initiated by writing to one of the CPPM event counter register addresses. After writing to a CPPM count register, a maximum of 67 RCLK clock periods must be allowed to elapse to permit all the CPPM values to be properly transferred. The CPPM registers may then be read.

The RXCP and TXCP accumulate cell-based primitives such as received cells, corrected cell headers, uncorrected cell headers, and transmitted cells. An accumulation interval in each block is initiated by writing to one of the RXCP or TXCP event counter register addresses. After writing to a count register, a maximum of 67 RCLK or TICLK clock periods must be allowed to elapse to permit all the RXCP or TXCP values to be properly transferred. The RXCP or TXCP count registers may then be read.

Writing to the S/UNI-12xJET Channel Identification, Master Reset, and Global Monitor Update register causes the PMON, CPPM, RXCP, and TXCP performance event counters to latch and a new accumulation period to start in all four quadrants of the S/UNI-12xJET. A maximum of 67 RCLK[x] clock periods must be allowed to elapse to permit all the event count registers to be properly transferred.

13.24 Using the Internal FDL Transmitter

It is important to note that the access rate to the TDPR registers is limited by the rate of the internal high-speed system clock selected by the LINESYSCLK register bit of the S/UNI-12xJET Misc. register (09B, 19B, 29B, 39B, 49B, 59B, 69B, 79B, 89B, 99B, A9B, B9B,C9B, D9B, E9B, F9B). Consecutive accesses to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 1/8 that of the selected TDPR high-speed system clock. This time is used by the high-speed system clock to sample the event, write the FIFO, and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the line clock) must be considered when determining the procedure used to read and write the TDPR registers.

Upon reset of the S/UNI-12xJET, the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register to logic 0 (default value). An HDLC all-ones Idle signal will be sent while in this state. The TDPR is enabled by setting the EN bit to logic 1. The FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO. The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register must be properly set. If FCS generation is desired, the CRC bit should be set to logic 1. If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable register to logic 1. The TDPR operating parameters in the TDPR Upper Transmit Threshold and TDPR Lower Interrupt Threshold registers should be set to the desired values. The TDPR Upper Transmit Threshold sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO. Transmission will continue until current packet is transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC packets (packets with EOM attached) in its FIFO. Finally, the TDPR can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of data. In the polled mode the processor controlling the TDPR must periodically read the TDPR Interrupt Status register to determine when to write to the TDPR Transmit Data register. In the interrupt driven mode, the processor controlling the TDPR uses the INTB output, the S/UNI-12xJET Clock Activity Monitor and Interrupt Identification register, and the S/UNI-12xJET Interrupt Status register to identify TDPR interrupts which determine when writes can or must be done to the TDPR Transmit Data register.

Interrupt Driven Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 1 so an interrupt on INTB is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun. The following procedure should be followed to transmit HDLC packets:

Wait for data to be transmitted. Once data is available to be transmitted, then go to step 2.

Write the data byte to the TDPR Transmit Data register.

If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

If there are more bytes in the packet to be sent, then go to step 2.

While performing steps 1 to 4, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine detailed in the following text should be followed immediately.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold register. Unless an error condition occurs, transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

TDPR Interrupt Routine

Upon assertion of INTB, the source of the interrupt must first be identified by reading the S/UNI-12xJET Clock Activity Monitor and Interrupt Identification register (007) and the S/UNI-12xJET Interrupt Status registers (005, 105, 205, 305). Once the source of the interrupt has been identified as TDPR, then the following procedure should be carried out:

Read the TDPR Interrupt Status register.

If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic 1, one Abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. To re-enable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear register should be written with any value.

If OVRI=1, then the FIFO has overflowed. The packet which the last byte written into the FIFO belongs to has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), OVRI is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data register occurs. This write contains the first byte of the next packet to be transmitted.

If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, then it should be written to the TDPR Transmit Data register before an underrun occurs. If there is no more data to transmit, then an EOM should be set at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

Polling Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 0 since packet transmission is set to work with a periodic polling procedure. The following procedure should be followed to transmit HDLC packets:

Wait until data is available to be transmitted, then go to step 2.

Read the TDPR Interrupt Status register.

If FULL=1, then the TDPR FIFO is full and no further bytes can be written. Continue polling the TDPR Interrupt Status register until either FULL=0 or BLFILL=1. Then, go to either step 4 or 5 depending on implementation preference.

If BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data register. Go to step 6.

If FULL=0, then the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data register. Go to step 6.

If more data bytes are to be transmitted in the packet, then go to step 2.

If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

13.25 Using the Internal Data Link Receiver

It is important to note that the access rate to the RDLC registers is limited by the rate of the internal high-speed system clock selected by the LINESYSCLK register bit of the S/UNI-12xJET Misc. register (09B, 19B, 29B, 39B, 49B, 59B, 69B, 79B, 89B, 99B, A9B, B9B,C9B, D9B, E9B, F9B). Consecutive accesses to the RDLC Status and RDLC Data registers should be accessed at a rate no faster than 1/10 that of the selected RDLC high-speed system clock. This time is used by the high-speed system clock to sample the event and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read RDLC registers.

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic 0 (default state). The RDLC Interrupt Control register should then be initialized to enable the INT output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the RDLC Status register must be continuously polled to check the interrupt status (INTR) bit.

After the RDLC Interrupt Control register has been written, the RDLC can be enabled at any time by setting the EN bit in the RDLC Configuration register to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer. This is done to provide alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO. This is done to provide alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS bit in the RDLC Status register for a change in the link status. If the COLS bit is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits is used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register is read, the PKIN bit is cleared to logic 0. If the RDLC Status register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt driven mode for the transfer of frame data. In the polled mode, the processor controlling the RDLC must periodically read the RDLC Status register to determine when to read the RDLC Data register. In the interrupt driven mode, the processor controlling the RDLC uses the S/UNI-12xJET INTB output, the S/UNI-12xJET Clock Activity Monitor and Interrupt Identification register, and the S/UNI-12xJET Interrupt Status registers to determine when to read the RDLC Data register.

In the case of interrupt driven data transfer from the RDLC to the processor, the INTB output of the S/UNI-12xJET is connected to the interrupt input of the processor. The processor interrupt service routine verifies what block generated the interrupt by reading the S/UNI-12xJET Clock Activity Monitor and Interrupt Identification register, and the S/UNI-12xJET Interrupt Status registers. Once it has identified that the RDLC has generated the interrupt, it processes the data in the following order:

RDLC Status register read. The INTR bit should be logic 1.

If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

If COLS = 1, then set the EMPTY FIFO software flag.

If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

Read the RDLC Data register.

Read the RDLC Status register.

If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

If COLS = 1, then set the EMPTY FIFO software flag.

If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

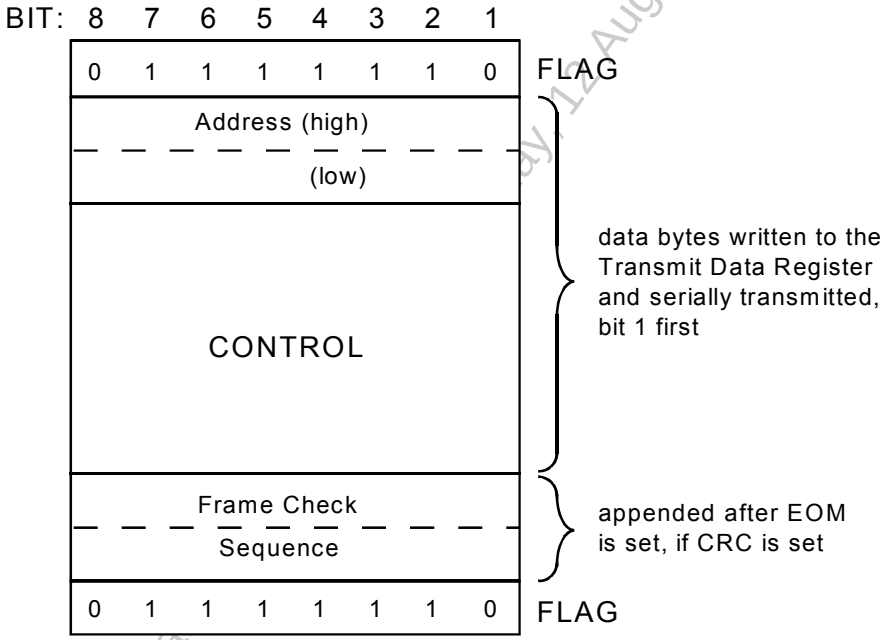
- If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.
- If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.
- If PBS[2:0] = 1XX, store the last byte of the packet, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.
- If PBS[2:0] = 000, store the packet data.

If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

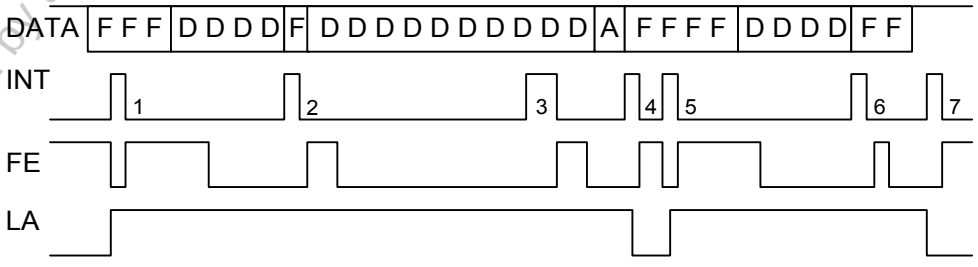
If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

Figure 67 Typical Data Frame



Bit 1 is the first serial bit to be received. When enabled, the primary, secondary and universal addresses are compared with the high order packet address to determine a match.

Figure 68 Example Multi-Packet Operational Sequence



F - flag sequence (01111110)

A - abort sequence (01111111)

D - packet data bytes

INT - active high interrupt output

FE - internal FIFO empty status

LA - state of the LINK ACTIVE software flag

Figure 68 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence. The cause of each interrupt and the processing required at each point is described in the following paragraphs.

At points 1 and 5 the first flag after all ones or abort is detected. A dummy byte is written in the FIFO, FE goes low, and an interrupt goes high. When the interrupt is detected by the processor it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed. The LINK ACTIVE (LA) software flag is set to logic 1.

At points 2 and 6 the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor, it reads the data and status registers until the FIFO becomes empty. The interrupt is removed as soon as the RDLC Status register is read since the FIFO fill level of 8 bytes has not been exceeded. It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO. The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3 the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

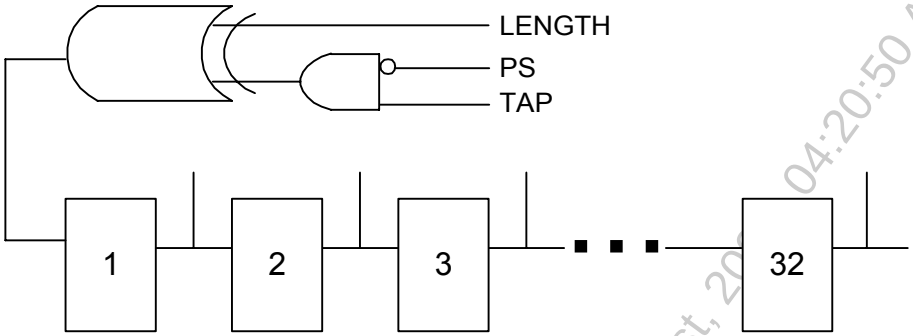
At points 4 or 7 an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed. The LINK ACTIVE software flag is cleared.

13.26 PRGD Pattern Generation

A pseudo-random or repetitive pattern can be inserted/extracted in the PLCP payload (if PLCP framing is enabled) or in the DS3, E3, J2, or Arbitrary framing format payload (if PLCP framing is disabled). It cannot be inserted into the ATM cell payload.

The pattern generator can be configured to generate pseudo random patterns or repetitive patterns as shown in Figure 69 below:

Figure 69 PRGD Pattern Generator



The pattern generator consists of a 32 bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0], when the PS bit is low). When PS is high, the pattern detector functions as a re-circulating shift register, with length determined by PL[4:0].

13.26.1 Generating and Detecting Repetitive Patterns

When a repetitive pattern (such as 1-in-8) is to be generated or detected, the PS bit must be set to logic 1. The pattern length register must be set to (N-1), where N is the length of the desired repetitive pattern. Several examples of programming for common repetitive sequences are given below in the Common Test Patterns section.

For pattern generation, the desired pattern must be written into the PRGD Pattern Insertion registers. The repetitive pattern will then be continuously generated. The generated pattern will be inserted in the output data stream, but the phase of the pattern cannot be guaranteed.

For pattern detection, the PRGD will determine if a repetitive pattern of the length specified in the pattern length register exists in the input stream. It does so by loading the first N bits from the data stream, and then monitoring to see if the pattern loaded repeats itself error free for the subsequent 48 bit periods. It will repeat this process until it finds a repetitive pattern of length N, at which point it begins counting errors (and possibly re-synchronizing) in the same way as for pseudo-random sequences. Note that the PRGD does NOT look for the pattern loaded into the Pattern Insertion registers, but rather automatically detects any repetitive pattern of the specified length. The precise pattern detected can be determined by initiating a PRGD update, setting PDR[1:0] = 00 in the PRGD Control register, and reading the Pattern Detector registers (which will then contain the 32 bits detected immediately prior to the strobe).

13.26.2 Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T O.151. The register configurations required to generate these patterns and others are indicated in the two tables below:

Table 30 Pseudo Random Pattern Generation (PS Bit = 0)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
2^3 –1	00	02	FF	FF	FF	FF	0	0
2^4 –1	00	03	FF	FF	FF	FF	0	0
2^5-1	01	04	FF	FF	FF	FF	0	0
2^6 –1	04	05	FF	FF	FF	FF	0	0
2^7 –1	00	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Activate)	03	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Deactivate)	03	06	FF	FF	FF	FF	1	1
2^9 -1 (O.153)	04	08	FF	FF	FF	FF	0	0
2^{10} –1	02	09	FF	FF	FF	FF	0	0
2^{11} -1 (O.152, O.153)	08	0A	FF	FF	FF	FF	0	0
2^{15} -1 (O.151)	0D	0E	FF	FF	FF	FF	1	1
2^{17} –1	02	10	FF	FF	FF	FF	0	0
2^{18} –1	06	11	FF	FF	FF	FF	0	0
2^{20} -1 (O.153)	02	13	FF	FF	FF	FF	0	0
2^{20} -1 (O.151 QRSS bit=1)	10	13	FF	FF	FF	FF	0	0
2^{21} –1	01	14	FF	FF	FF	FF	0	0
2^{22} –1	00	15	FF	FF	FF	FF	0	0
2^{23} -1 (O.151)	11	16	FF	FF	FF	FF	1	1
2^{25} –1	02	18	FF	FF	FF	FF	0	0
2^{28} –1	02	1B	FF	FF	FF	FF	0	0
2^{29} –1	01	1C	FF	FF	FF	FF	0	0
2^{31} –1	02	1E	FF	FF	FF	FF	0	0

Table 31 Repetitive Pattern Generation (PS Bit = 1)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
All ones	00	00	FF	FF	FF	FF	0	0
All zeros	00	00	FE	FF	FF	FF	0	0
Alternating ones/zeros	00	01	FE	FF	FF	FF	0	0
Double alternating ones/zeros	00	03	FC	FF	FF	FF	0	0
3 in 24	00	17	22	00	20	FF	0	0
1 in 16	00	0F	01	00	FF	FF	0	0
1 in 8	00	07	01	FF	FF	FF	0	0
1 in 4	00	03	F1	FF	FF	FF	0	0

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
Inband loopback activate	00	04	F0	FF	FF	FF	0	0
Inband loopback deactivate	00	02	FC	FF	FF	FF	0	0

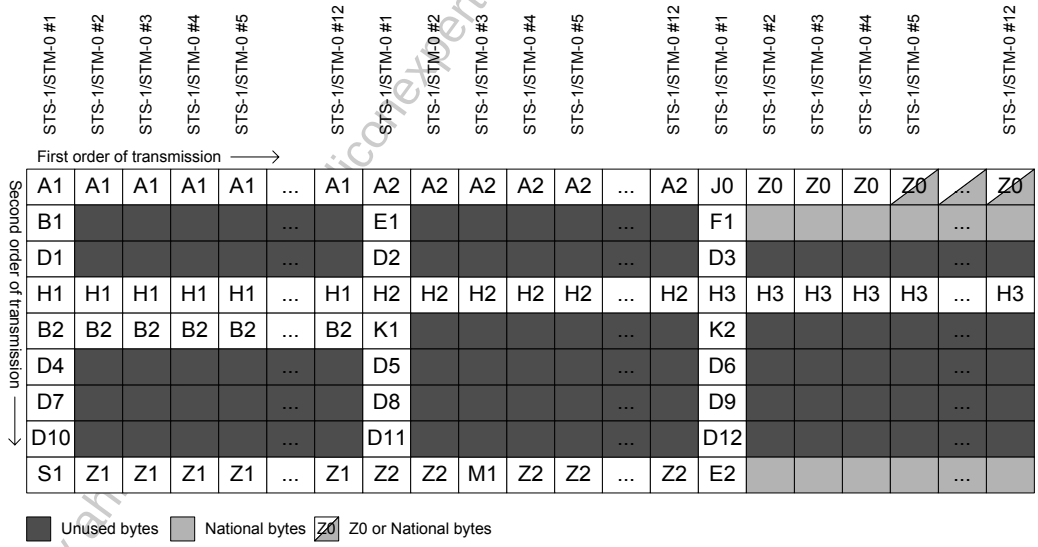
Notes for the Pseudo Random and Repetitive Pattern Generation Tables

- The PS bit and the QRSS bit are contained in the TDPR Control register
- TR = TDPR Tap Register
- LR = TDPR Length Register
- IR#1 = TDPR Pattern Insertion #1 Register
- IR#2 = TDPR Pattern Insertion #2 Register
- IR#3 = TDPR Pattern Insertion #3 Register
- IR#4 = TDPR Pattern Insertion #4 Register
- The TINV bit and the RINV bit are contained in the TDPR Control register

13.27 Transport and Path Overhead Bytes

Under normal operating conditions, the S/UNI-12xJET processes the complete transport overhead present in an STS-12/12c(STM-4) stream. The byte positions processed by the S/UNI-12xJET are indicated below.

Figure 70 STS-12 (STM-4) on RTOH/TTOH



Transport Overhead Bytes

All receive transport overhead bytes are extracted and presented onto the RTOH port. All transmit transport overhead bytes can be inserted via the TTOH port.

A1, A2: The frame alignment bytes (A1, A2) locate the SONET/SDH frame in the serial stream. These bytes are used to byte align the received data.

J0 The J0 byte is currently defined as the section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler. The received section trace message is processed by the SECTION RTTP block and also available on the RTOH port. The transmit section trace message can be programmed in the SECTION TTTP, via the TTOH port or the TRMP block.

Z0: The Z0 bytes are currently defined as the section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler. The received section growth bytes are extracted and available on the RTOH port. The transmit section growth bytes can be inserted via the TTOH port or the TRMP block.

B1: The section bit interleaved parity byte provides a section error monitoring function. In the transmit direction, the TRMP block calculates the B1 code over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling. In the receive direction, the RRMP block calculates the B1 code over the current frame and compares this calculation with the B1 byte received in the following frame. B1 errors are accumulated in the error event counter of the RRMP block .

D1 - D3: The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications. In the transmit direction, the section DCC byte is inserted from a dedicated 192 kbit/s input, TLD and/or TSLD port. Section DCC can also be inserted via the TTOH port or the TRMP block. In the receive direction, the section DCC is extracted on a dedicated 192 kbit/s output, RLD and/or RSLD port. Section DCC is also extracted on the RTOH port.

H1, H2: The pointer value bytes locate the J1 path overhead byte in the SONET/SDH frame. In the transmit direction, the SVCA block inserts a valid pointer with pointer adjustments to accommodate plesiochronous timing offsets between the line and system references. In the receive direction, the pointer is interpreted by the RHPP block to locate the payload. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS state is entered when H1, H2 contain an all ones pattern.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. An all zero pattern is inserted in the transmit direction unless a negative stuff event occurs. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function. In the transmit direction, the TRMP block calculates the B2 codes. The calculated code is then placed in the next frame. In the receive direction, the RRMP block calculates the B2 codes over the current frame and compares this calculation with the B2 codes receive in the following frame. B2 errors are accumulated in the error event counter of the RRMP block.

K1, K2: The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'. In the transmit direction, the K1 and K2 bytes can be inserted via the TTOH port or the TRCP ports. The TRMP block also provides register control for the K1 and K2 bytes block. In the receive direction, the RRMP block provides register access to the filtered APS channel. Protection switch byte failure alarm detection is provided. The K2 byte is also determines the presence of the line AIS, or the line RDI maintenance signals

D4 - D12: The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications. In the transmit direction, the line DCC byte is inserted from a dedicated 576 kbit/s input, TLD. Line DCC can also be inserted via the TTOH port or the TRMP block. In the receive direction, the line DCC is extracted on a dedicated 576 kbit/s output, RLD. Line DCC is also extracted on the RTOH port.

S1: The S1 byte provides the synchronization status message. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of the SONET/SDH signal. Bits 1 through 4 are currently undefined. In the transmit direction, the synchronization status message is inserted from the TRMP block. In the receive direction, the TRMP block provides register access to the synchronization status byte. The S1 byte is also available on the RTOH port.

Z1: The Z1 bytes are allocated for future growth. In the transmit direction, the Z1 growth bytes can be inserted via the TTOH port or the TRMP block. In the receive direction, the Z1 growth bytes are extracted and available on the RTOH port.

M1: The M1 byte provides a line remote error indication (REI) function for remote performance monitoring. In the transmit direction, the M1 byte is internally generated. The number of B2 errors detected in the previous interval is insert from the receive RRMP block or the TRCP port. In the receive direction, a legal REI value is added to the line REI event counter in the RRMP block.

Z2: The Z2 bytes are allocated for future growth. In the transmit direction, Z2 growth bytes can be inserted via the TTOH port or the TRMP block. In the receive direction, Z1 growth bytes are extracted and available on the RTOH port.

Path Overhead Bytes

All receive path overhead bytes are extracted and presented onto the RPOH port. All transmit path overhead bytes can be inserted via the TPOH port.

J1: The Path Trace byte is used to repetitively transmit a 64-byte CLLI message (for SONET/SDH networks), or a 16-byte E.164 address (for SDH networks). When not used, this byte should be set to transmit continuous null characters. Null is defined as the ASCII code, 0x00. The received section trace message is processed by the PATH RTTP block and also available on the RPOH port. The transmit section trace message can be programmed in the PATH TTTP, via the TPOH port or the THPP block.

B3: The path bit interleaved parity byte provides a path error monitoring function. In the transmit direction, the THPP block calculates the B3 code. The calculated code is then placed in the next frame. In the receive direction, the RHPP block calculates the B3 code and compares this calculation with the B3 code received in the following frame. B3 errors are accumulated in an error event counter of the RHPP.

C2: The path signal label indicator identifies the equipped payload type. In the transmit direction, the C2 byte can be inserted via the TPOH port or the THPP block. In the receive direction, the C2 byte is processed by the RHPP block for path signal label mismatch and unstable alarms and also for unequipped and payload defect indication alarms. The C2 byte is also available on the RPOH port.

G1: The path status byte provides a path remote error indication (REI) function, and a path remote defect indication (RDI) function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications. In the transmit direction, the REI and RDI codes are internally generated. The RDI code is inserted from the receive RHPP block or the TRCP port. The number of B3 errors detected in the previous interval is inserted from the THPP block or the TRCP port. In the receive direction, a legal path REI value is added to the path REI event counter in the RHPP block.

H4: The multi-frame indicator byte is a payload specific byte. In the transmit direction, the H4 byte can be inserted via the TPOH port or the THPP block. In the receive direction, the H4 byte is extracted and available on the RPOH port..

Z3 Z4 Z5: The Z3, Z4 and Z5 bytes are allocated for future growth. In the transmit direction, the growth bytes can be inserted via the TPOH port or the THPP block. In the receive direction, the growth bytes are extracted and available on the RPOH port.

13.28 Accessing Indirect Registers

Indirect registers are used to conserve address space in the S/UNI-12xJET. Indirect registers are accessed by writing the indirect address register. The following steps should be followed for writing to indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the desired configurations for the channel into the indirect data registers.

3. Write the channel number (indirect address) to the indirect address register with RWB set to logic 0.

4. Read BUSY. Once it equals 0, the indirect write has been completed.

The following steps should be followed for reading indirect registers:

5. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

6. Write the channel number (indirect address) to the indirect address register with RWB set to logic 1.

7. Read the BUSY bit. If it is equal to logic 0, continue to 4. Otherwise, continue polling the BUSY bit.

8. Read the indirect data registers to find the state of the register bits for the selected channel number.

13.29 Translation from AU4/3x(TUG3/TU3/VC3) into 3x(AU3/VC3)

When used in SPECTRA mode, the S/UNI-12xJET Drop SVCA can be configure to translate AU4/3x(TUG3/TU3/VC3) payloads into 3x(AU3/VC3) payloads to bridge between SDH compliant and SONET compliant networks. The RHPP block interprets the AU4 pointer and terminates the VC4 POH overhead. The RHPP TU3 block interprets the TU3 pointer and terminates the VC3 POH overhead. Then, the SVCA block moves the VC3 fixed stuff columns from columns 1,2 to columns 30,59 (the contains is lost). While performing rate adaptation, the SVCA block also generates three independent AU3 pointers for the DROP TelecomBus interface.

AU3/VC3 (Receive Side) => AU3/VC3 (DROP TelecomBus Interface)

1. Default setting in the RHPP Payload Configuration Register (0x1882) for AU3 pointer interpretation..

2. Default setting in the RHPP TU3 Payload Configuration Register (0x1902) for no TU3 pointer interpretation.

3. Default setting in the SVCA DROP Payload Configuration Register (0x1A92) for AU3 processing.

AU4/VC4 (Receive Side) => AU4/VC4 (DROP TelecomBus Interface)

1. Set the STS3C[4:1] bits in the RHPP Payload Configuration Register (0x1882) for AU4 pointer interpretation..

2. Default setting in the RHPP TU3 Payload Configuration Register (0x1902) for no TU3 pointer interpretation.

3. Set the STS3C[4:1] bits in the SVCA DROP Payload Configuration Register (0x1A92) for AU4 processing.

AU4/3x(TUG3/TU3/VC3) (Receive Side) => 3x(AU3/VC3) (DROP TelecomBus Interface)

1. Set the STS3C[4:1] bits in the RHPP Payload Configuration Register (0x1882) for AU4 pointer interpretation..

2. Set the TUG3[4:1] bits in the RHPP TU3 Payload Configuration Register (0x1902) for TU3 pointer interpretation.

3. Set the STS3C[4:1] and the TUG3[4:1] bits in the SVCA DROP Payload Configuration Register (0x1A92) for AU4/TU3=>AU3 translation.

13.30 Translation from 3x(AU3/VC3) into AU4/3x(TUG3/TU3/VC3)

When used in SPECTRA mode, the S/UNI-12xJET ADD SVCA can be configure to translate 3x(AU3/VC3) payloads into AU4/3x(TUG3/TU3/VC3) payloads to bridge between SONET compliant and SDH compliant networks. The SVCA block moves the VC3 fixed stuff columns from columns 30,59 to columns 1,2 (the contains is lost). While performing rate adaptation, the SVCA block also generates three independent TU3 pointers and a fix AU4 pointer for the transmit side. The THPP TU3 block inserts the VC3 POH overhead. The THPP block inserts the VC4 POH overhead.

AU3/VC3 (ADD TelecomBus Interface) => AU3/VC3 (Transmit Side)

1. Default setting in the SVCA ADD Payload Configuration Register (0x1A82) for AU3 processing.

2. Default setting in the THPP TU3 Payload Configuration Register (0x198A) for no TU3 POH insertion.

3. Default setting in the THPP Payload Configuration Register (0x1982) for AU3 POH insertion..

AU4/VC4 (ADD TelecomBus Interface) => AU4/VC4 (Transmit Side)

1. Set the STS3C[4:1] bits in the SVCA ADD Payload Configuration Register (0x1A82) for AU4 processing.

2. Default setting in the THPP TU3 Payload Configuration Register (0x198A) for no TU3 POH insertion.

3. Set the STS3C[4:1] bits in the THPP Payload Configuration Register (0x1982) for AU4 POH insertion..

3x(AU3/VC3) (ADD TelecomBus Interface) => AU4/3x(TUG3/TU3/VC3) (Transmit Side)

1. Set the STS3C[4:1] and the TUG3[4:1] bits in the SVCA ADD Payload Configuration Register (0x1A82) for AU3 => AU4/TU3 translation.

2. Set the TUG3[4:1] bits in the THPP TU3 Payload Configuration Register (0x198A) for TU3 POH insertion.

3. Set the STS3C[4:1] bits in the THPP Payload Configuration Register (0x1982) for AU4 POH insertion..

13.31 Bit Error Rate Monitor

The S/UNI-12xJET provides two BERM blocks. One can be dedicated to monitoring the Signal Degrade (SD) error rates and the other dedicated to monitoring the Signal Fail (SF) error rates.

The Bit Error Rate Monitor (BERM) block counts and monitors line BIP errors over programmable periods of time (window size). It can monitor to declare an alarm or to clear it if the alarm is already set. A different threshold must be used to declare or clear the alarm, whether or not those two operations are performed at the same BER. The following tables list the recommended content of the BERM registers for OC-12 and different error rates (BER). Both BERMs in the SBER block are equivalent and are programmed similarly. In a normal application they will be set to monitor different BER.

When the SF/SD CMODE bit is 1, this indicates that the clearing monitoring is recommended to be performed using a window size that is 8 times longer than the declaration window size. When the SF/SD CMODE bit is 0 this indicates that the clearing monitoring is recommended to be performed using a window size equal to the declaration window size. In all cases the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. The tables indicate the declare BER, the evaluation period and the recommended CMODE and associated thresholds.

The Saturation threshold is not listed in the table, and is programmed with the value 0xFFFFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts. It enables the user to determine a ceiling value at which the error counters will saturate, letting error bursts pass through within a frame or sub window period.

Table 32 Recommended BERM settings for OC-12 and different BER rates, meeting Bellcore objectives.

OC	Monitored Declare BER	Objective met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
12	10^{-3}	0.008	0	00000007	000828	0001AE
12	10^{-4}	0.008	0	00000007	00016E	000036
12	10^{-5}	0.025	0	00000016	000073	000014
12	10^{-6}	0.250	0	000000DE	000075	000014
12	10^{-7}	2.500	0	000008AE	000075	000014
12	10^{-8}	21.000	0	000048EA	000061	000012
12	10^{-9}	167.000	0	000243DC	00004B	00000F

Table 33 Recommended BERM settings for OC-12 and different BER rates, meeting Bellcore and ITU requirements.

OC	Monitored Declare BER	Requirement met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
12	10^{-3}	0.01	0	00000008	00093C	0001F7
12	10^{-4}	0.10	0	0000002B	00091D	00012C
12	10^{-5}	1.00	0	00000192	000922	00011C
12	10^{-6}	10.00	0	00000F98	000922	00011B
12	10^{-7}	100.00	0	00009BD6	000922	00011A
12	10^{-8}	1,000.00	0	00061647	000922	00011A
12	10^{-9}	10,000.00	0	003CDEAD	000922	00011A

13.32 PRBS Generator and Monitor (PRGM)

A pseudo-random (using the $X^{23}+X^{18}+1$ polynomial) or incrementing pattern can be inserted/extracted in the SONET/SDH payload. The user has the option to monitor a programmable sequence in all the B1 byte positions. The complement of these values are also monitored in the E1 byte positions. This is used to check for mis-configuration of STS-1 cross-connect fabrics. If a known STS-1 originated from a particular STS-1 port, the source can be programmed to send a B1 pattern that would be monitored at the other end.

13.32.1 Mixed Payload (STS-12c, STS-3c, and STS-1)

Each PRGM is designed to process the payload of a STS-12/STM-4 frame in a time-multiplexed manner. Each time division (12 STS-1 paths) can be programmed to a granularity of a STS-1. It is possible to process one STS-12c/STM-4c, twelve STS-1/STM-0 or four STS-3c/STM-1 or a mix of STS-1/STM-0 and STS-3c/STM-1 as long as the aggregate data rate is not more than one STS-12/STM-4 equivalent. The mixed payload configuration can support the three STS-1/STM-0 and STS-3c/STM-1 combinations shown below:

- three STS-1/STM-0 with three STS-3c/STM-1
- six STS-1/STM-0 with two STS-3c/STM-1
- nine STS-1/STM-0 with one STS-3c/STM-1.

The STS-1 path that each one of the payload occupies, cannot be chosen randomly. They must be placed on STS-3c/STM-1 boundaries (group of three STS-1).

13.32.2 Synchronization

Before being able to monitor the correctness of the PRBS payload, the monitor must synchronize to the incoming PRBS. The process of synchronization involves synchronizing the monitoring LFSR to the transmitting LFSR. Once the two are synchronized the monitoring LFSR is able to generate the next expected PRBS bytes. When receiving sequential PRBS bytes (STS-12c/VC-4-4c), the LFSR state is determined after receiving 3 PRBS bytes (24 bits of the sequence). The last 23 of 24 bits (excluding MSB of first received byte) would give the complete LFSR state. The 8 newly generated LFSR bits after a shift by 8 (last 8 XOR products) will produce the next expected PRBS byte.

The implemented algorithm requires four PRBS bytes of the same payload to ascertain the LFSR state. From this recovered LFSR state the next expected PRBS byte is calculated.

An Out of Synchronization and Synchronized State is defined for the monitor. While in progress of synchronizing to the incoming PRBS stream, the monitor is out of synchronization and remains in this state until the LFSR state is recovered and the state has been verified by receiving 4 consecutive PRBS bytes without error. The monitor will then change to the Synchronized State and remains in that state until forced to resynchronize via the RESYNC register bit or upon receiving 4 erred bytes. When forced to resynchronize, the monitor changes to the Out of Synchronization State and tries to regain synchronization.

Upon detecting 4 consecutive PRBS byte errors, the monitor will enter the Out of Synchronization State and automatically try to resynchronize to the incoming PRBS stream. Once synchronized to the incoming stream, it will take 4 consecutive non-erred PRBS bytes to change back into the Synchronized State. The auto synchronization is useful when the input frame alignment of the monitored stream changes. The realignment will affect the PRBS sequence causing all input PRBS bytes to mismatch and forcing the need for a resynchronization of the monitor. The auto resynchronization does this, detecting a burst of errors and automatically re-synchronizing.

13.32.3 Error Detection and Accumulation

By comparing the received PRBS byte with the calculated PRBS byte, the monitor is able to detect bit errors in the payload. A bit error is detected on a comparison mismatch of the two bytes. All bit errors are accumulated in a 16 bit error counter. The error counter will saturate at its maximum value of FFFFh, i.e. it will not wrap around to 0000h if further PRBS byte errors are encountered. The counter is readable via the PRGM Monitor Error Count. An indirect read to that register will initiate a transfer of the error counter into the registers for reading. The error counter is cleared when transferred into the registers and the accumulation starts at zero.

Bit errors are accumulated only when the monitor is in synchronized state. To enter the synchronize state, the monitor must have synchronized to the incoming PRBS stream and received 4 consecutive bytes without errors. Once synchronized, the monitor falls out of synchronization when forced to by programming high the RESYNC register bit, or once it detects 4 consecutive PRBS byte errors. When out of synchronization, detected errors are not accumulated.

13.33 Path Unequipped Configuration

The THPP can be configure to insert all zeros in a payload when the path is define as unequipped.

Setting a payload unequipped for a:

- STS-12C : set UNEQ to logic one and UNEQV to logic zero for path 1 of the THPP.
- STS-3C : set UNEQ to logic one and UNEQV to logic zero for the corresponding STS-3C (VC-4) path 1, 2, 3 or 4 of the THPP.
- STS-1 : set UNEQ to logic one and UNEQV to logic zero for the corresponding STS-1 (VC-3) path of the THPP.
- TUG-3 : set UNEQ to logic one and UNEQV to logic zero for the corresponding VC-3 path of the TU3 THPP.

Note: If, for an unequipped path, the add bus signals (AJ0J1, APL and APAIS) are not valid, the SVCA must be held in reset for the corresponding path in order to avoid AIS-P generation.

Note: For an unequipped path, the THPP fixed stuff columns overwrite must be disable for the corresponding path in order to generate a valid B3.

13.34 Reset Sequence

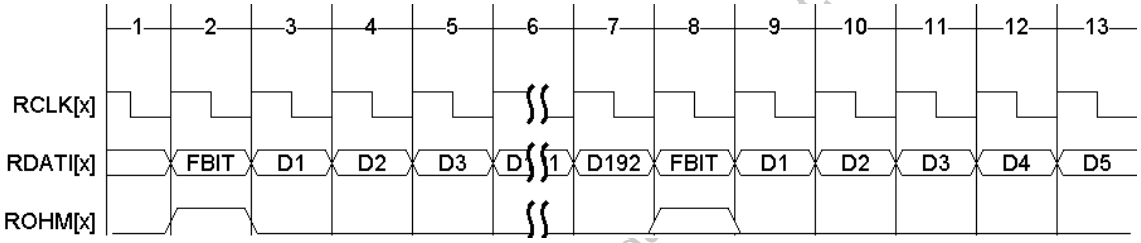
Whenever device reset is de-asserted (either RSTB going high, or writing ‘0’ to the RESET bit), there is a small probability that the TIP bit (Register 0x1801) will lock up. If this lockup occurs, SVCA, RRMP, and RHPP counters will not update, and TIP will never go low. The user must read the TIP bit after each time that device reset is de-asserted. If TIP is ‘1’ for this read, then device reset must be cycled again until TIP is read as ‘0’. Note that a minimum of 516 OCLK, ICLK, PTCLK and PICLK clock cycles must occur after reset being de-asserted for the read of the TIP bit to be valid.

14 Functional Timing

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the S/UNI-12xJET registers are set to their default states).

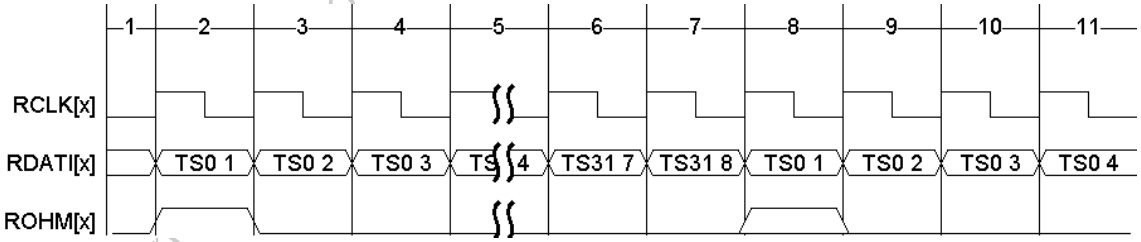
14.1 Receive Serial Formats

Figure 71 Receive DS1 Stream



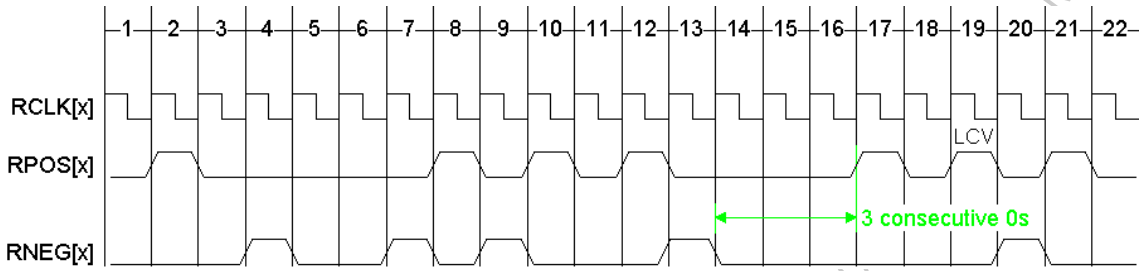
The Receive DS1 Stream diagram (Figure 71) shows the expected DS1 overhead indicators on ROHM[x] when the S/UNI-12xJET is configured for DS1 PLCP or DS1 direct-mapped frame formats. Frame pulses on ROHM[x] are not required to be present. Once internally synchronized by a pulse on ROHM[x], the S/UNI-12xJET can use its internal timeslot counter for DS1 overhead bit identification. The ATM cell stream is contained in RDATI[x], along with a framing bit placeholder every 193 bit periods. An upstream DS1 framer (such as the PM4341A T1XC or PM4344 TQUAD) must be used to identify the DS1 framing bit position.

Figure 72 Receive E1 Stream



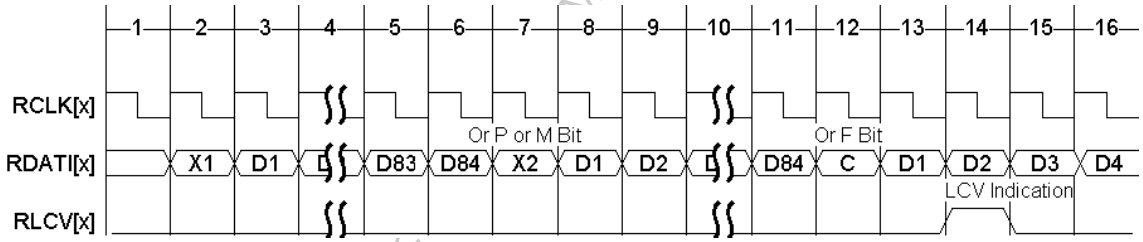
The expected Receive E1 Stream for direct-mapped or PLCP applications is shown in Figure 72. Frame pulses on ROHM[x] are not required to be present every frame. Once internally synchronized by a pulse on ROHM[x], the S/UNI-12xJET can use its internal timeslot counter for E1 overhead bit identification. The ATM cell stream is contained in RDATI[x], along with a framing bit placeholder every 256 bit periods (time slot 0 bit 1 = [TS0 1], time slot 31 bit 7 = [TS31 7]). An upstream E1 framer (such as the PM6341A E1XC or PM6344 EQUAD) must be used to identify the E1 framing bit position.

Figure 73 Receive Bipolar DS3 Stream



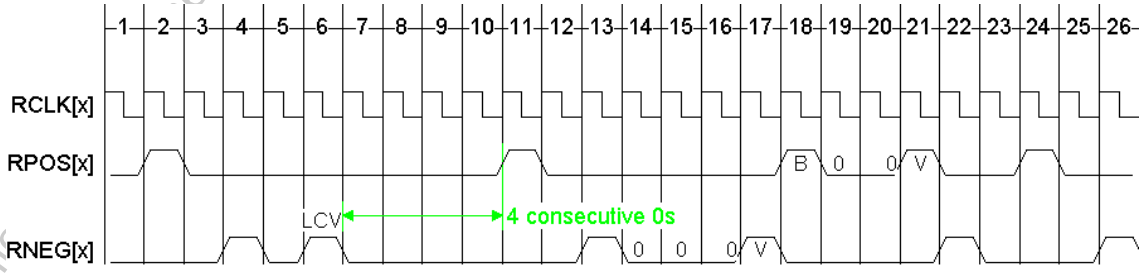
The Receive Bipolar DS3 Stream diagram (Figure 73) shows the operation of the S/UNI-12xJET while processing a B3ZS encoded DS3 stream on inputs RPOS[x] and RNEG[x]. It is assumed that the first bipolar violation (on RNEG[x]) illustrated corresponds to a valid B3ZS signature. A line code violation is declared upon detection of three consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid B3ZS signature.

Figure 74 Receive Unipolar DS3 Stream



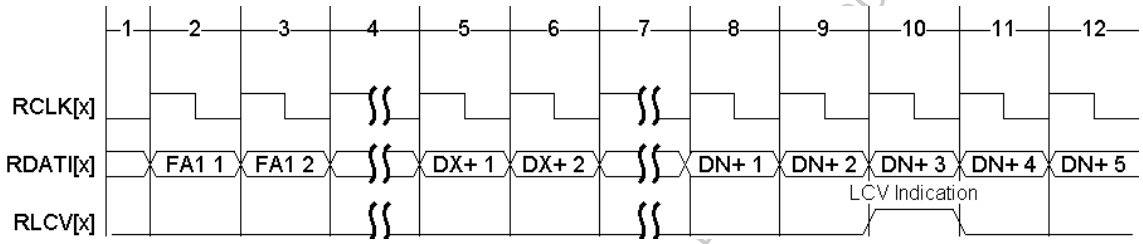
The Receive Unipolar DS3 Stream diagram (Figure 74) shows the complete DS3 receive signal on the RDATI[x] input. Line code violation indications, detected by an upstream B3ZS decoder, are indicated on input RLCV[x]. RLCV[x] is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV[x].

Figure 75 Receive Bipolar E3 Stream



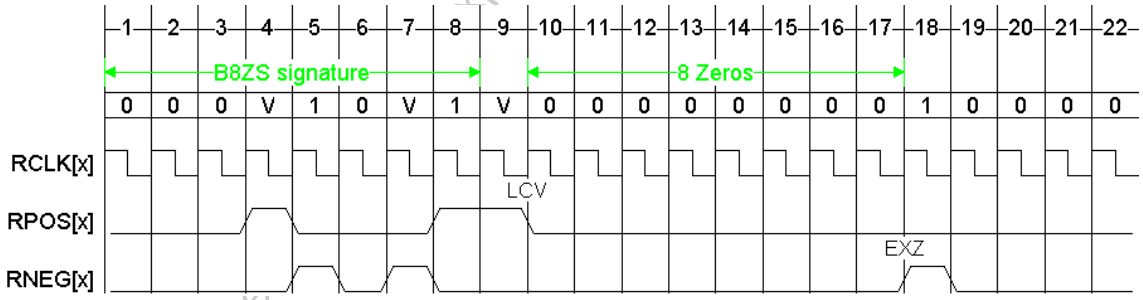
The Receive Bipolar E3 Stream diagram (Figure 75) shows the operation of the S/UNI-12xJET while processing an HDB3-encoded E3 stream on inputs RPOS[x] and RNEG[x]. It is assumed that the first bipolar violation (on RNEG[x]) illustrated corresponds to a valid HDB3 signature (HDB3 Signature Pattern is X00V). A line code violation is declared upon detection of four consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid HDB3 signature.

Figure 76 Receive Unipolar E3 Stream



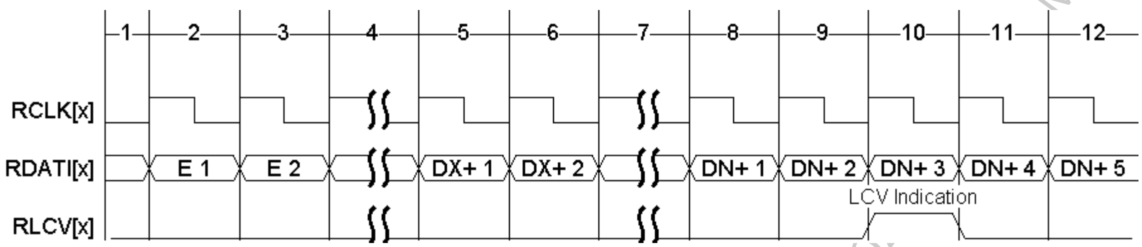
The Receive Unipolar E3 Stream diagram (Figure 76) shows the unipolar E3 receive signal on the RDATI[x] input. Line code violation indications, detected by an upstream HDB3 decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV.

Figure 77 Receive Bipolar J2 Stream



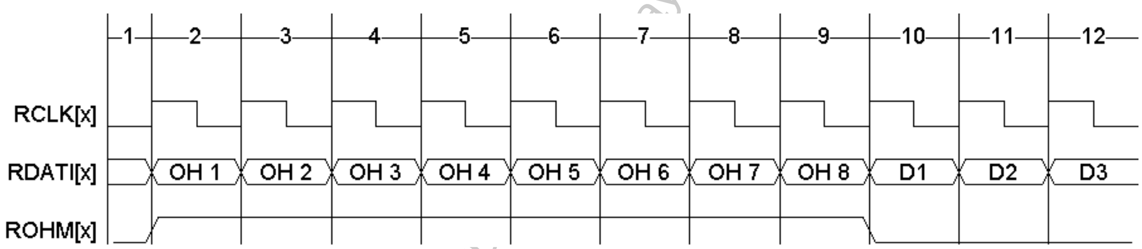
The Receive Bipolar J2 Stream diagram (Figure 77) shows the operation of the S/UNI-12xJET while processing a B8ZS-encoded J2 stream on inputs RPOS and RNEG. It is assumed that the first bipolar violation (on RNEG) illustrated corresponds to a valid B8ZS signature. A line code violation is declared upon detection of a bipolar violation which is not part of a valid B8ZS signature. An excessive zeros indication is given when 8 or more consecutive zeros are detected.

Figure 78 Receive Unipolar J2 Stream



The Receive Unipolar J2 Stream diagram (Figure 78) shows the unipolar J2 receive signal on the RDATI[x] input. Line code violation indications, detected by an upstream B8ZS decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV.

Figure 79 Receive Arbitrary Framing Stream



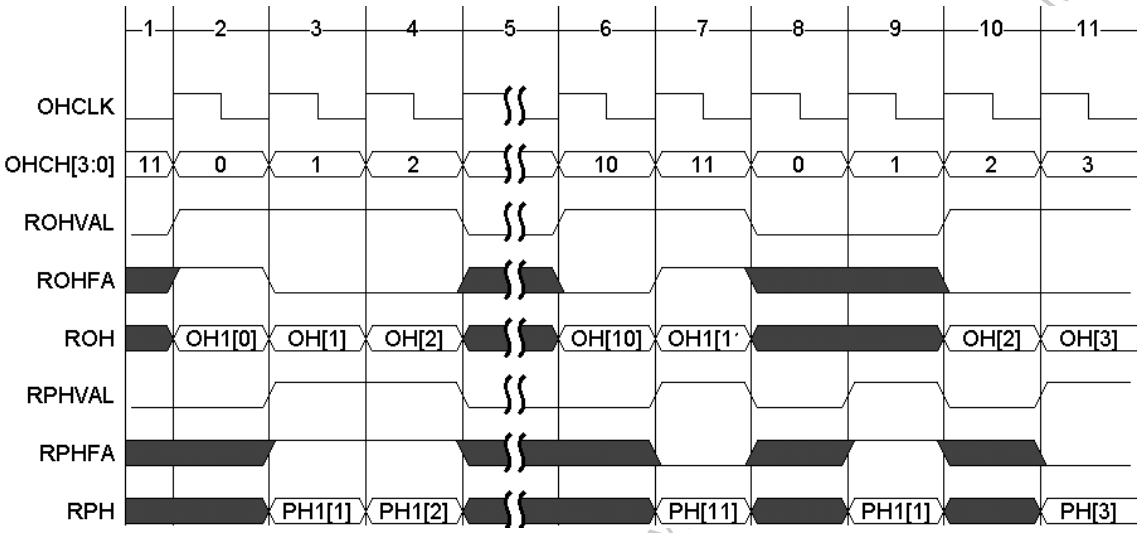
The Receive Arbitrary Framing Stream diagram (Figure 79) illustrates how ROHM is used to mark the location of the transmission system overhead bits in the RDATI[x] stream. RDATI[x] and ROHM[x] are both sampled on the rising edge of RCLK[x].

14.2 Receive Overhead Extraction

On each rising edge of OHCLK, the OHCH[3:0] channel ID increments (and rolls over from 0AH to 00H). If valid data is available for the channel indicated by OHCH[3:0], then the overhead bit for that channel appears on ROH/RPH, and ROHVAL/RPHVAL is high. Otherwise ROHVAL/RPHVAL is low and ROH/RPH and ROHFA/RPHFA is invalid. For each channel, ROHFA/RPHFA signals the beginning of the frame and overhead sequence for the channel in OHCH[3:0].

DS3, E3 and J2 overhead extraction is output on the ROHVAL, ROHFA, and ROH pins. PLCP overhead extraction is output on RPHVAL, RPHFA, and RPH pins. Because different channels may be processing different overhead types, Figure 80 depicts the generic operation of the receive overhead extraction interface. In Figure 80, OH1 [X], on ROH, depicts the first overhead bit for a given channel [X]. Other overhead bits are shown as OH [X] where X is the channel. The order in which the overhead bits are extracted is discussed below. For RPH, PH1 [X], depicts the first overhead bit for a given channel [X], and other overhead bits are shown as PH [X], where X is the channel.

Figure 80 Receive Overhead Extraction Structure



RPHVAL, RPHFA, and RPH operate independently from ROHVAL, ROHFA, and ROH. There is no functional timing relationship between these two sets of overhead extraction pins.

For DS3 overhead extraction, ROHFA is asserted once every 56 bits to mark the X1 bit for each active channel. For each DS3 channel, the order of the overhead bit extraction is shown in Table 34, starting from the top left X1 bit, proceeding to the right, and then from sub-frame 1 to sub-frame 7:

Table 34 DS3 Receive Overhead Bits

M-subframe	DS3 Overhead Bits							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	X_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
2	X_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
3	P_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
4	P_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
5	M_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
6	M_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
7	M_3	N/U	C_1	N/U	C_2	N/U	C_3	N/U

The DS3 framing bits (F-bits) are not extracted on the overhead port; however, the bit positions for the framing bits (F-bits) are still maintained. The bit positions corresponding to the F-bits in the extracted stream are marked N/U in the above table and should be ignored. The ROH stream for a particular channel is invalid when the DS3 frame alignment is lost for that channel.

For Receive G.751 E3 Overhead extraction, ROHFA is asserted once every 48 bits to mark the RAI bit for each active channel. The RAI and Na bits are always extracted. The justification indication bits (C_{JK}) along with the justification opportunity bits (J_1-J_4) are extracted when they are treated as overhead (PYLD&JUST bit in the E3 FRMR Maintenance Options register set to logic 0). For each G.751 E3 channel, the order of the overhead bit extraction is shown in Table 35, starting from the top left bit, proceeding to the right.

Table 35 G.751 E3 Receive Overhead Bits

Byte	G.751 E3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	RAI	Na	C11	C21	C31	C41	C12	C22
2	C32	C42	C13	C23	C33	C43	J1	J2
3	J3	J4	N/U	N/U	N/U	N/U	N/U	N/U
4	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
5	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
6	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U

The bits in gray in Table 35 may not be valid based on (PYLD&JUST) bit in the E3 FRMR Maintenance Options register; however, the bit position must still be maintained in the overhead sequence. The bit positions marked as N/U in Table 35 must be maintained in the overhead sequence and may be ignored. The ROH stream for a particular channel is invalid when the G.751 E3 frame alignment is lost for that channel.

For G.832 E3 Overhead extraction, ROHFA goes high once every 134 bits to mark the first bit of the FA1 octet for each active channel. For each G.832 channel, the order of the overhead bit extraction is shown in Table 36, starting from the top left FA(1) bit, proceeding to the right, and then to from byte 1 to byte 17 (Note byte 17, is a partial byte).

Table 36 G.832 E3 Receive Overhead Bits

Byte	G.832 E3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	FA1(1)	FA1(2)	FA1(3)	FA1(4)	FA1(5)	FA1(6)	FA1(7)	FA1(8)
2	FA2(1)	FA2(2)	FA2(3)	FA2(4)	FA2(5)	FA2(6)	FA2(7)	FA2(8)
3	EM(1)	EM(2)	EM(3)	EM(4)	EM(5)	EM(6)	EM(7)	EM(8)
4	TR(1)	TR(2)	TR(3)	TR(4)	TR(5)	TR(6)	TR(7)	TR(8)
5	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
6	MA(1)	MA(2)	MA(3)	MA(4)	MA(5)	MA(6)	MA(7)	MA(8)
7	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
8	NR(1)	NR(2)	NR(3)	NR(4)	NR(5)	NR(6)	NR(7)	NR(8)
9	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
10	GC(1)	GC(2)	GC(3)	GC(4)	GC(5)	GC(6)	GC(7)	GC(8)
11-16	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
17	N/U	N/U	N/U	N/U	N/U	N/U		

The bit positions marked as N/U in Table 36 must be maintained in the overhead sequence and may be ignored. The ROH stream for a particular channel is invalid when the G.832 E3 frame alignment is lost for that channel.

For J2 Overhead extraction, ROHFA goes high once every 84 bits to mark the first bit of TS97 in the first frame of each J2 multi-frame. For each J2 channel, the order of the overhead bit extraction is shown in Table 37, starting from the top left TS97 bit 1, proceeding to the right, and then to from frame 1 to frame 4. Shaded out positions in Table 37 are NOT true bit positions but are there to illustrate the frame boundary.

Table 37 J2 Receive Overhead Bits

Fame	J2 Overhead Bits							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	TS97(1)	TS97(2)	TS97(3)	TS97(4)	TS97(5)	TS97(6)	TS97(7)	TS97(8)
	TS98(1)	TS98(2)	TS98(3)	TS98(4)	TS98(5)	TS98(6)	TS98(7)	TS98(8)
	1	1	0	0	m			
2	TS97(1)	TS97(2)	TS97(3)	TS97(4)	TS97(5)	TS97(6)	TS97(7)	TS97(8)
	TS98(1)	TS98(2)	TS98(3)	TS98(4)	TS98(5)	TS98(6)	TS98(7)	TS98(8)
	1	0	1	0	0			
3	TS97(1)	TS97(2)	TS97(3)	TS97(4)	TS97(5)	TS97(6)	TS97(7)	TS97(8)
	TS98(1)	TS98(2)	TS98(3)	TS98(4)	TS98(5)	TS98(6)	TS98(7)	TS98(8)
	x1	x2	x3	a	m			
4	TS97(1)	TS97(2)	TS97(3)	TS97(4)	TS97(5)	TS97(6)	TS97(7)	TS97(8)
	TS98(1)	TS98(2)	TS98(3)	TS98(4)	TS98(5)	TS98(6)	TS98(7)	TS98(8)
	e1	e2	e3	e4	e5			

The ROH stream for a particular channel is invalid when the J2 frame alignment is lost for that channel.

For PLCP Overhead extraction, RPHFA always marks the first bit of the F1 octet and indicates the beginning of the PLCP overhead sequence. The number of growth octets (Zn) in the PLCP frame varies according to the selected PLCP frame format (DS3, DS1, G.751 E3, or E1). For each channel with PLCP framing the order of the bit extraction is shown in Table 38 starting from the top left proceeding to the right and then down.

Table 38 PLCP Receive Overhead Bits

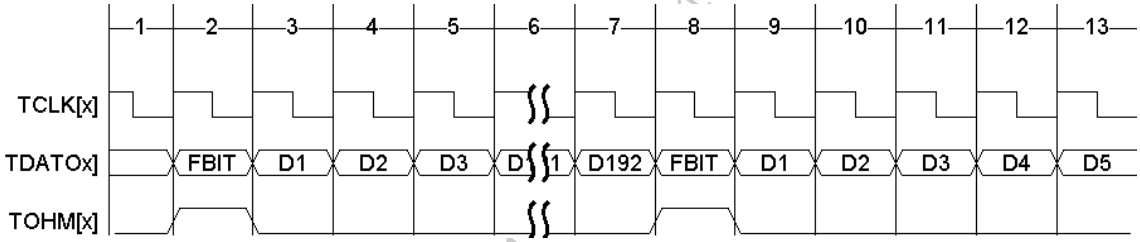
Path Byte	PLCP Overhead Bits							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	F1(1)	F1(2)	F1(3)	F1(4)	F1(5)	F1(6)	F1(7)	F1(8)
2	B1(1)	B1(2)	B1(3)	B1(4)	B1(5)	B1(6)	B1(7)	B1(8)
3	G1(1)	G1(2)	G1(3)	G1(4)	G1(5)	G1(6)	G1(7)	G1(8)
4	M2(1)	M2(2)	M2(3)	M2(4)	M2(5)	M2(6)	M2(7)	M2(8)
5	M1(1)	M1(2)	M1(3)	M1(4)	M1(5)	M1(6)	M1(7)	M1(8)
6	C1(1)	C1(2)	C1(3)	C1(4)	C1(5)	C1(6)	C1(7)	C1(8)

Path Byte	PLCP Overhead Bits							
	1	2	3	4	5	6	7	8
7+(n-x)	Zx(1)	Zx(2)	Zx(3)	Zx(4)	Zx(5)	Zx(6)	Zx(7)	Zx(8)
7+(n-2)	Z2(1)	Z2(2)	Z2(3)	Z2(4)	Z2(5)	Z2(6)	Z2(7)	Zn(8)
7+(n-1)	Z1(1)	Z1(2)	Z1(3)	Z1(4)	Z1(5)	Z1(6)	Z1(7)	Zn(8)

In Table 38, the number of growth octets is defined as n, and the x'th growth octet is Zx. These growth octets are sent out RPH the highest growth octet first. For DS3, there are 6 growth octets; for DS1, there are 4 growth octets; for G.751 E3, there are 3 octets; and for E1, there are 4 growth octets.

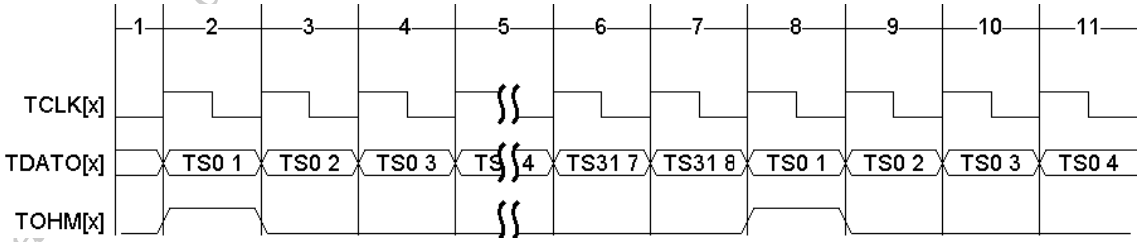
14.3 Transmit Serial Formats

Figure 81 Transmit DS1 Stream



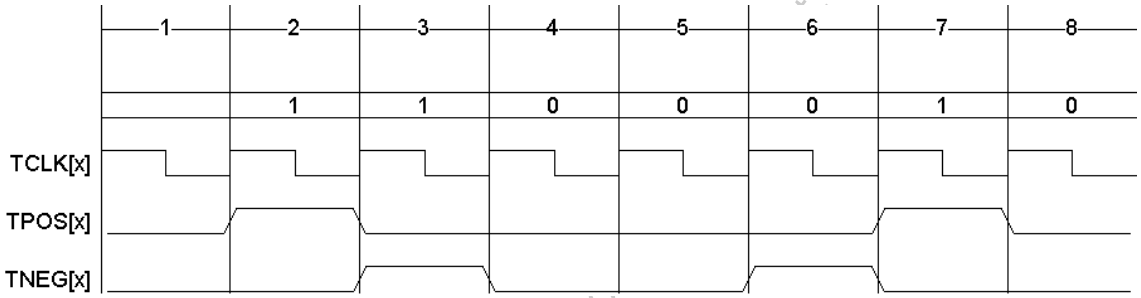
The Transmit DS1 Stream diagram (Figure 81) illustrates the generation of DS1 overhead indicators on TOHM when the S/UNI-12xJET is configured for DS1 PLCP or non-PLCP frame formats. The S/UNI-12xJET flywheels using its internal timeslot counter to generate TOHM. The ATM cell stream is inserted in TDATO, along with a framing bit placeholder every 193 bit periods. An upstream DS1 framer (such as the PM4341A T1XC or PM4344 TQUAD) must be used to insert the appropriate DS1 framing pattern. Note that TCLK is a flow through version of TICLK or RCLK depending on the mode of operation of that channel; a variable propagation delay exists between the source clock and TCLK.

Figure 82 Transmit E1 Stream



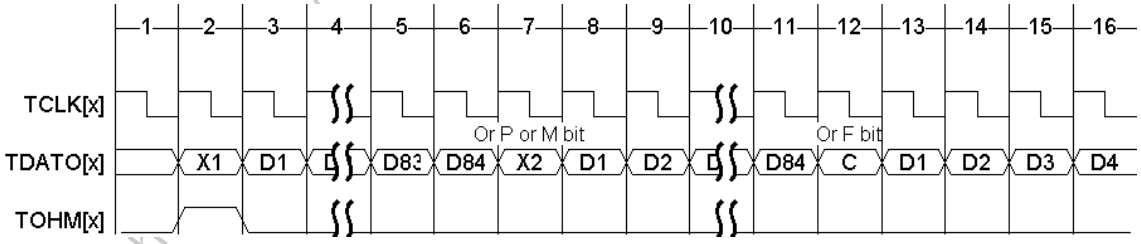
The Transmit E1 Stream diagram (Figure 82) illustrates the generation of E1 frame alignment indicators on TOHM when the S/UNI-12xJET is configured for E1 PLCP or non-PLCP frame formats. The S/UNI-12xJET flywheels using its internal timeslot counter to generate TOHM. The ATM cell stream is inserted in TDATO, along with a framing bit placeholder every 256-bit periods. An upstream E1 framer (such as the PM6341A E1XC or PM6344 EQUAD) must be used to insert the appropriate E1 framing pattern. Note that TCLK is a flow through version of TICLK or RCLK depending on the mode of operation of that channel; a variable propagation delay exists between the source clock and TCLK.

Figure 83 Transmit Bipolar DS3 Stream



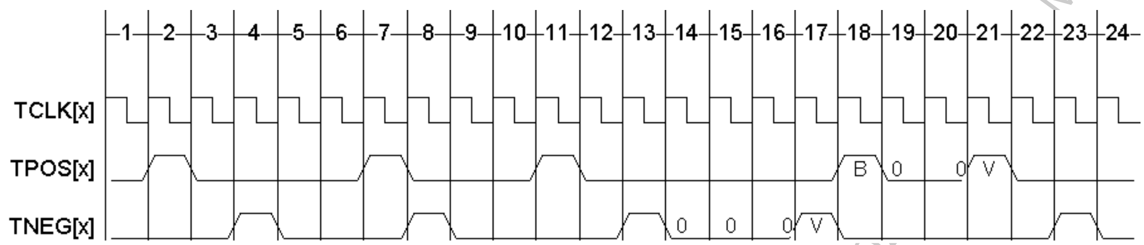
The Transmit Bipolar DS3 Stream diagram (Figure 83) illustrates the generation of a bipolar DS3 stream. The B3ZS encoded DS3 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a DS3 line interface unit. Note that TCLK is a flow through version of TICLK, RCLK, or an internally generated clock from the DS3 de-synchronizer (D3E3MD) depending on the mode of operation of that channel; a variable propagation delay exists between the source clock and TCLK.

Figure 84 Transmit Unipolar DS3 Stream



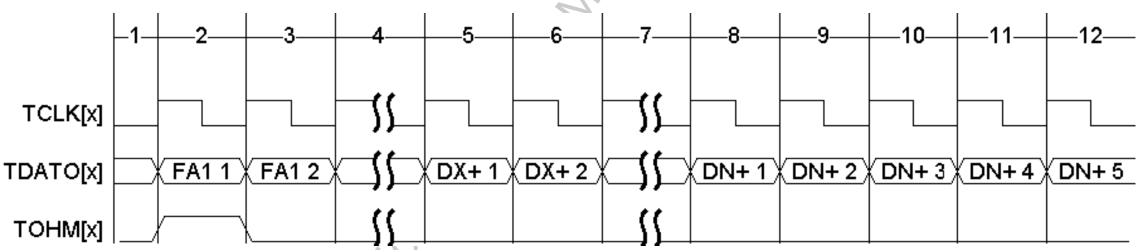
The Transmit Unipolar DS3 Stream diagram (Figure 84) illustrates the unipolar DS3 stream generation. The ATM cell stream, along with valid DS3 overhead bits is contained in TDATO. The TOHM output marks the M-frame boundary (the X1 bit) in the transmit stream. Note that TCLK is a flow through version of TICLK, RCLK, or an internally generated clock from the DS3 de-synchronizer (D3E3MD) depending on the mode of operation of that channel; a variable propagation delay exists between the source clock and TCLK.

Figure 85 Transmit Bipolar E3 Stream



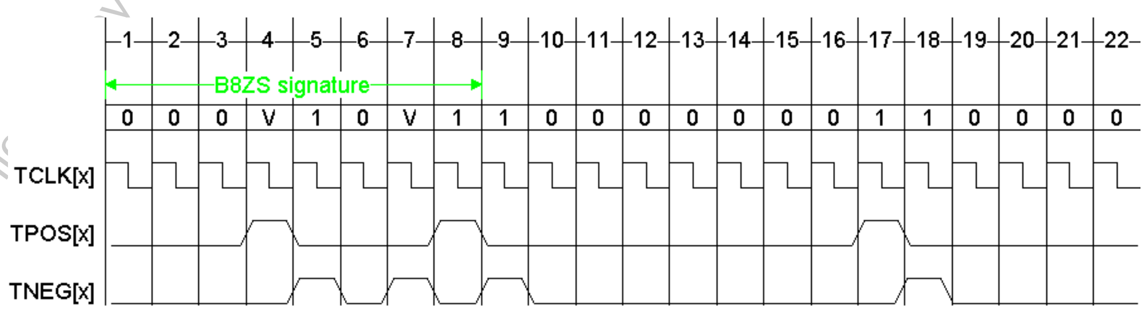
The Transmit Bipolar E3 Stream diagram (Figure 85) illustrates the generation of a bipolar E3 stream. The HDB3 encoded E3 stream is present on TPOS and TNEG (HDB3 Signature Pattern is X00V). These outputs, along with the transmit clock, TCLK, can be directly connected to a E3 line interface unit. Note that TCLK is a flow through version of TICLK, RCLK, or an internally generated clock from the DS3 de-synchronizer (D3E3MD) depending on the mode of operation of that channel; a variable propagation delay exists between the source clock and TCLK.

Figure 86 Transmit Unipolar E3 Stream



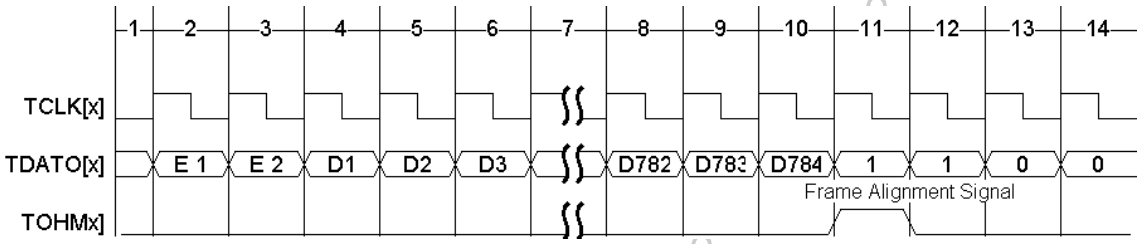
The Transmit Unipolar E3 Stream diagram (Figure 86) illustrates the unipolar E3 stream generation. The ATM cell stream, along with valid E3 overhead bits is contained in TDATO. The TOHM output shown marks the G.832 frame boundary (the first bit of the FA1 frame alignment byte) in the transmit stream. Note that TCLK is a flow through version of TICLK, RCLK, or an internally generated clock from the DS3 de-synchronizer (D3E3MD) depending on the mode of operation of that channel; a variable propagation delay exists between the source clock and TCLK.

Figure 87 Transmit Bipolar J2 Stream



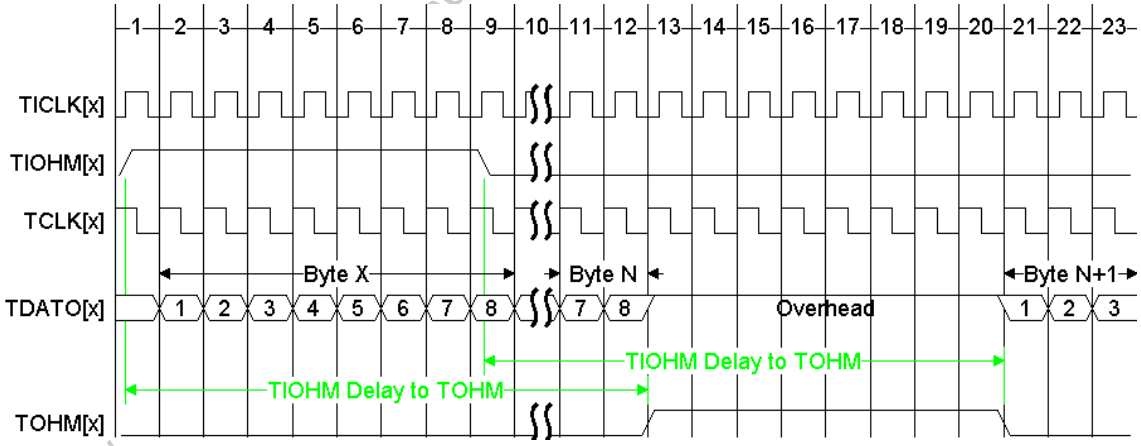
The Transmit Bipolar J2 Stream diagram (Figure 87) illustrates the generation of a bipolar J2 stream. The B8ZS encoded J2 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a J2 line interface unit. Note that TCLK is a flow through version of TICLK or RCLK depending on the mode of operation of that channel; a variable propagation delay exists between the source clock and TCLK.

Figure 88 Transmit Unipolar J2 Stream



The Transmit Unipolar J2 Stream diagram (Figure 88) illustrates the unipolar J2 stream generation. The ATM cell stream, along with valid J2 overhead bits is contained in TDATO. The TOHM output shown marks the J2 multi-frame boundary (the first frame-alignment bit of each J2 multi-frame) in the transmit stream. Note that TCLK is a flow through version of TICLK or RCLK depending on the mode of operation of that channel; a variable propagation delay exists between the source clock and TCLK.

Figure 89 Transmit Arbitrary Framing Stream



The Transmit Arbitrary Framing Stream (Figure 89) illustrates overhead indication positions when interfacing to a non-PLCP based transmission system not supported by the S/UNI-12xJET. The overhead bit placeholder positions are indicated using the TIOHM input. The ATM cells presented in the TDATO transmit stream are held off to include the overhead placeholders. The location of these placeholder positions is indicated by TOHM. A downstream framer inserts the correct overhead information in the placeholder positions.

The delay between TIOHM and TOHM is dependent on the channel used (X) and the specific configuration of that channel. TIOHM is sampled on the rising edge of TICLK. The output TOHM and TDATO are output on the rising edge of TCLK. The cycle-to-cycle based timing relationship between TIOHM and TOHM is maintained. In Figure 89, the byte aligned framing format is shown, meaning when TIOHM is asserted, the resulting TOHM will only take effect on byte boundaries. There are two other arbitrary framing formats :nibble and bit. The byte and nibble framing formats are ideal for ATM cell and Byte-HDLC based data formats, where the bit framing format is used for Bit-HDLC. The framing formats are determined via the SPLT Configuration register FORM[1:0] bits, and Channel Configuration register TOCTA bit. The number of TICLK periods between transmission format overhead bit positions must be divisible by 4 for nibble alignment, 8 for byte alignment, and has no restriction for bit alignment.

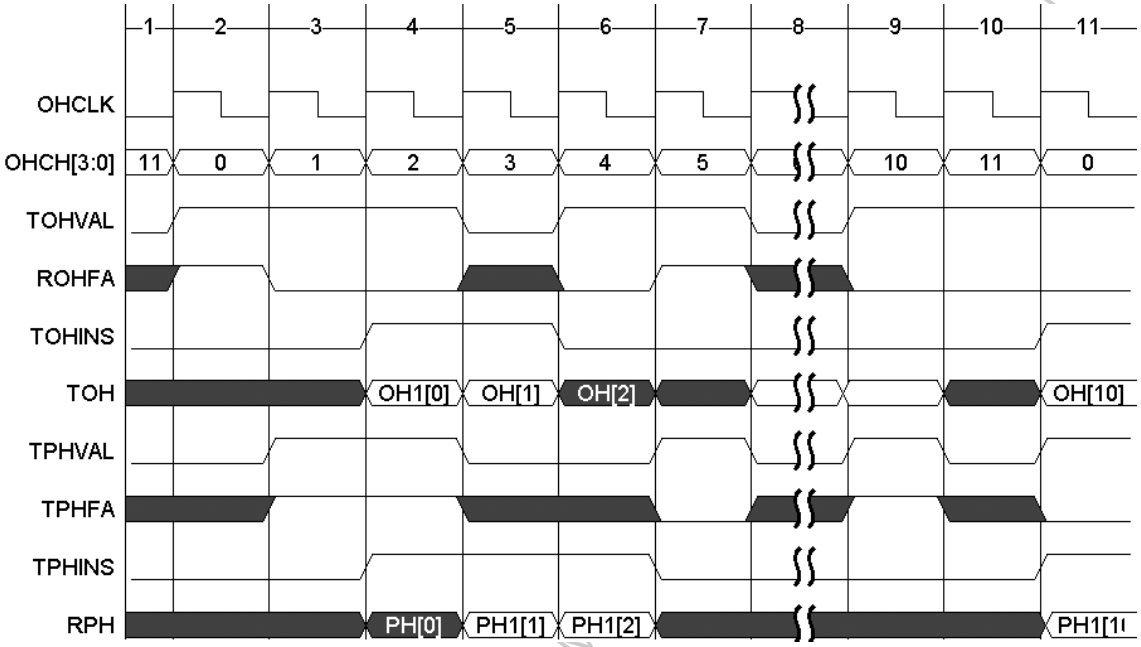
14.4 Transmit Overhead Insertion

On each rising edge of OHCLK, the OHCH[3:0] channel ID increments (and rolls over from 0AH to 00H). If valid data is available for the channel indicated by OHCH[3:0], then the TOHVAL/TPHVAL will be asserted. Otherwise TOHVAL/TPHVAL is low and TOHFA/TPHFA is invalid. For each channel, TOHFA/TPHFA signals the beginning of the frame and overhead sequence for the channel in OHCH[3:0].

As shown in Figure 90, if the internal processor for the channel indicated by OHCH[3:0] is ready to receive an overhead bit, then TOHVAL/TPHVAL will be high for that cycle. The values on TOH/TPH and TOHINS/TPHINS will then be sampled by the S/UNI-12xJET for that channel on the 3rd rising edge of OHCLK after the valid channel cycle began. If the sampled value of TOHINS/TPHINS for that channel is high, then the sampled value of TOH/TPH will be used to overwrite the current overhead bit. If TOHINS/TPHINS is low, the default overhead bit for that position is used. TOHFA/TPHFA signal will be high when the bit being requested is the first bit of that channel's overhead sequence. TOHFA/TPHFA will be low otherwise. When TOHVAL/TPHVAL is low, TOHFA/TPHFA is invalid in the current cycle, and TOH/TPH and TOHINS/TPHINS are not sampled in the 3rd cycle.

DS3 and E3 overhead insertion is input on the TOHINS and TOH pins. External J2 overhead insertion via the Overhead insertion ports is not supported. PLCP overhead insertion is input on TPHINS and TPH pins. Because different channels may be processing different overhead types, Figure 90 depicts the generic operation of the receive overhead extraction interface. In Figure 90, OH1[X], on TOH, depicts the first overhead bit for a given channel [X]. Other overhead bits are shown as OH[X] where X is the channel. The order in which the overhead bits are extracted is discussed below. For TPH, PH1[X], depicts the first overhead bit for a given channel [X], and other overhead bits are shown as PH[X], where X is the channel.

Figure 90 Overhead Insertion



TPHVAL, TPHFA, TPHINS and TPH operate independently from TOHVAL, TOHFA, TPHINS and TOH. There is no functional timing relationship between these two sets of overhead insertion pins.

For each DS3 channel, the order of the overhead bit insertion is as shown in Table 39, starting from the top left X1 bit, proceeding to the right, and then from sub-frame 1 to sub-frame 7. TOHFA is asserted once every 56 bits to mark the X1 bit for each active channel.

Table 39 DS3 Transmit Overhead Bits

M-subframe	DS3 Overhead Bits							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	F_4

For transmit G.751 E3 overhead insertion, TOHFA is asserted once every 48 bits to mark the RAI bit for each active channel. For each G.751 E3 channel, the order of overhead bit insertion is shown in Table 40, starting from the top left bit, proceeding to the right and then down.

Table 40 G.751 E3 Transmit Overhead Bits

Byte	G.751 E3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	RAI	Na	C11	C21	C31	C41	C12	C22
2	C32	C42	C13	C23	C33	C43	J1	J2
3	J3	J4	N/U	N/U	N/U	N/U	N/U	N/U
4	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
5	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
6	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U

The bit positions marked as N/U in Table 40 must be maintained in the overhead sequence and may be ignored. The PYLD&JUST bit in the E3 TRAN Status and Diagnostics Options register has no affect on the insertion of the justification service and the tributary justification bits through the TOH and the TOHINS inputs.

For G.832 E3 overhead insertion, TOHFA is asserted high once every 134 bits to mark the first bit of the FA1 octet for each active channel. For each G.832 channel, the order of the overhead bit insertion is shown in Table 41, starting from the top left FA(1) bit, proceeding to the right, and then to from byte 1 to byte 17 (Note byte 17 is a partial byte).

Table 41 G.832 E3 Transmit Overhead Bits

Byte	G.832 E3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	FA1(1)	FA1(2)	FA1(3)	FA1(4)	FA1(5)	FA1(6)	FA1(7)	FA1(8)
2	FA2(1)	FA2(2)	FA2(3)	FA2(4)	FA2(5)	FA2(6)	FA2(7)	FA2(8)
3	EM(1)	EM(2)	EM(3)	EM(4)	EM(5)	EM(6)	EM(7)	EM(8)
4	TR(1)	TR(2)	TR(3)	TR(4)	TR(5)	TR(6)	TR(7)	TR(8)
5	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
6	MA(1)	MA(2)	MA(3)	MA(4)	MA(5)	MA(6)	MA(7)	MA(8)
7	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
8	NR(1)	NR(2)	NR(3)	NR(4)	NR(5)	NR(6)	NR(7)	NR(8)
9	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
10	GC(1)	GC(2)	GC(3)	GC(4)	GC(5)	GC(6)	GC(7)	GC(8)
11-16	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U
17	N/U	N/U	N/U	N/U	N/U	N/U		

The bit positions marked as N/U in Table 41 must be maintained in the overhead sequence and may be ignored. Also note that the EM byte behaves as an error mask, that is the binary value sampled on TOH in the EM byte location is not inserted directly into the transmit overhead but, rather, the value is XORed with the calculated BIP-8 and inserted in the transmit overhead.

For PLCP overhead insertion, TPHFA always marks the first bit of the F1 octet and indicates the beginning of the PLCP overhead sequence. The number of growth octets (Zn) in the PLCP frame varies according to the selected PLCP frame format (DS3, DS1, G.751 E3, or E1). For each channel with PLCP framing the order of the bit extraction is shown in Table 42 starting from the top left proceeding to the right and then down.

Table 42 PLCP Transmit Overhead Bits

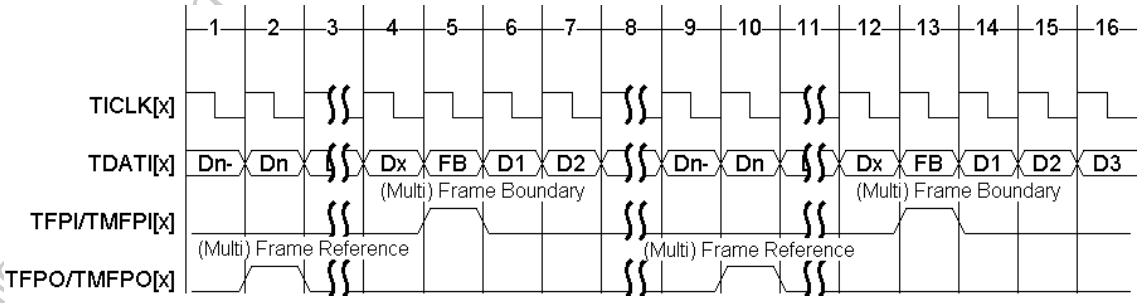
Path Byte	PLCP Overhead Bits							
	1	2	3	4	5	6	7	8
1	F1(1)	F1(2)	F1(3)	F1(4)	F1(5)	F1(6)	F1(7)	F1(8)
2	B1(1)	B1(2)	B1(3)	B1(4)	B1(5)	B1(6)	B1(7)	B1(8)
3	G1(1)	G1(2)	G1(3)	G1(4)	G1(5)	G1(6)	G1(7)	G1(8)
4	M2(1)	M2(2)	M2(3)	M2(4)	M2(5)	M2(6)	M2(7)	M2(8)
5	M1(1)	M1(2)	M1(3)	M1(4)	M1(5)	M1(6)	M1(7)	M1(8)
6	C1(1)	C1(2)	C1(3)	C1(4)	C1(5)	C1(6)	C1(7)	C1(8)
7+(n-x)	Zx(1)	Zx(2)	Zx(3)	Zx(4)	Zx(5)	Zx(6)	Zx(7)	Zx(8)
7+(n-2)	Z2(1)	Z2(2)	Z2(3)	Z2(4)	Z2(5)	Z2(6)	Z2(7)	Zn(8)
7+(n-1)	Z1(1)	Z1(2)	Z1(3)	Z1(4)	Z1(5)	Z1(6)	Z1(7)	Zn(8)

In Table 42, the number of growth octets is defined as n, and the x'th growth octet is Zx. These growth octets are input on TPH the highest growth octet first. For DS3, there are 6 growth octets; for DS1, there are 4 growth octets; for G.751 E3, there are 3 octets; and for E1, there are 4 growth octets.

The bit presented on TPH is only inserted into the path overhead if TPHINS is asserted during the bit in question, or if the appropriate bit is set in the SPLT Control Register. The timing diagram above assumes that the SRCB1 bit in the SPLT Control Register is programmed to logic 0, thereby selecting internal insertion of that octet.

14.5 Transmit Auxiliary Serial Input Format

Figure 91 Transmit Auxiliary Serial Input Stream



The Transmit Auxiliary Serial Input Stream diagram (Figure 91) shows the expected format of the inputs TDATI and TFPI/TMFPI along with TICLK and the output TFPO/TMFPO when the FRMRONLY bit in the S/UNI-12xJET Configuration 1 register is set.

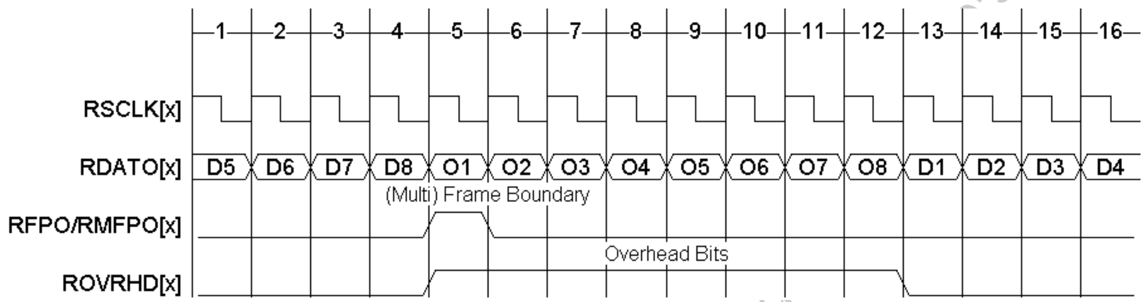
When the S/UNI-12xJET is configured for the DS3 transmit format, the TDATI and TFPI pins must adhere to the DS3 frame format depicted in Figure 54. If the TXMFPI register bit is logic 0, then TFPI is valid, and the S/UNI-12xJET will expect TFPI to pulse for every DS3 overhead bit with alignment to TDATI. If the TXMFPI register bit is logic 1, then TMFPI is valid, and the S/UNI-12xJET will expect TMFPI to pulse once every DS3 M-frame with alignment to TDATI. If the TXMFPO register bit is logic 0, then TFPO is valid, and the S/UNI-12xJET will pulse TFPO once every 85 TICLK cycles, providing upstream equipment with a reference DS3 overhead pulse. If the TXMFPO register bit is logic 1, then TMFPO is valid and the S/UNI-12xJET will pulse TMFPO once every 4760 TICLK cycles, providing upstream equipment with a reference M-frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI.

When the S/UNI-12xJET is configured for the E3 G.751 transmit format, TDATI and TFPI pins must adhere to the E3 G.751 frame format depicted in Figure 55. TFPI or TMFPI pulses high for one TICLK cycle and is aligned to the first bit of the frame alignment signal in the G.751 E3 input data stream on TDATI. TFPO or TMFPO will pulse high for one out of every 1536 TICLK cycles, providing upstream equipment with a reference frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI.

When the S/UNI-12xJET is configured for the J2 transmit format, TDATI and TFPI pins must adhere to the J2 frame format depicted in Figure 57. If the TXMFPI register bit is logic 0, then TFPI is valid (as shown in Figure 91). The S/UNI-12xJET will expect TFPI to pulse once every J2 frame with alignment to the first frame alignment bit on TDATI. If the TXMFPI register bit is logic 1, then TMFPI is valid. The S/UNI-12xJET will expect TMFPI to pulse once every J2 multi-frame with alignment to the first frame alignment bit on TDATI. If the TXMFPO register bit is logic 0, then TFPO is valid. The S/UNI-12xJET will pulse TFPO once every 789 TICLK cycles, providing upstream equipment with a reference frame pulse. If the TXMFPO register bit is logic 1, then TMFPO is valid and the S/UNI-12xJET will pulse TMFPO once every 3156 TICLK cycles, providing upstream equipment with a reference multi-frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI.

14.6 Receive Auxiliary Serial Output Format

Figure 92 Receive Auxiliary Serial Input Stream



The Receive Auxiliary Serial Input Stream diagram (Figure 92) shows the format of the outputs RDATO, RFPO/RMFPO, RSCLK, and ROVRHD when the FRMRONLY bit in the S/UNI-12xJET Configuration 1 register is set. Depending on the mode of operation, ROVRHD may not be available (sub-rate processing), thus the location of overhead bytes must be determined by an external source using the knowledge of the frame format and frame pulse.

When the S/UNI-12xJET is configured for the DS3 receive format, the RDATO, RFPO/RMFPO and ROVRHD outputs adhere to the DS3 framing format shown in Figure 54. If the RXMFPO and 8KREFO register bits are logic 0, RFPO is valid and will pulse high for one RSCLK cycle on first bit of each M-subframe with alignment to the RDATO data stream. If the RXMFPO register bit is a logic 1, and the 8KREFO register bit is logic 0, RMFPO is valid and will pulse high on the X1 bit of the RDATO data output stream. ROVRHD will be high for every overhead bit position on the RDATO data stream.

When the S/UNI-12xJET is configured for the E3 G.751 receive format, the RDATO, RFPO/RMFPO and ROVRHD outputs adhere to the E3 G.751 framing format shown in Figure 55. RFPO or RMFPO pulses high for one RSCLK cycle and is aligned to the first bit of the framing alignment signal in the G.751 E3 output data stream on RDATO. ROVRHD will be high for every overhead bit position on the RDATO data stream. If the PYLD&JUST register bit in the E3 FRMR Maintenance Options register is set to logic 0, the C_{jk} and P_k bits in the RDATO stream will be marked as overhead bits. If the PYLD&JUST register bit is set to logic 1, the C_{jk} and P_k bits in the RDATO stream will be marked as payload.

When the S/UNI-12xJET is configured for the E3 G.832 receive format, the RDATO, RFPO/RMFPO and ROVRHD outputs adhere to the E3 G.832 framing format shown in Figure 56. RFPO or RMFPO pulses high for one RSCLK cycle and is aligned to the first bit of the FA1 byte in the G.832 E3 output data stream on RDATO. ROVRHD will be high for every overhead bit position on the RDATO data stream.

When the S/UNI-12xJET is configured for the J2 receive format, the RDATO, RFPO/RMFPO and ROVRHD outputs adhere to the J2 framing format shown in Figure 57. If the RXMFPO register bit is a logic 0, RFPO is valid and will pulse high for one RSCLK cycle once each J2 frame with alignment to the first frame alignment bit on the RDATO data stream. If the RXMFPO register bit is a logic 1, RMFPO is valid and will pulse high once each J2 multi-frame aligned to the first frame alignment bit on the RDATO data output stream. ROVRHD will be high for every overhead bit position on the RDATO data stream.

14.7 Ingress Flexible Bandwidth Interface

The Ingress Flexible Bandwidth interface is used to insert a serial stream into the Cell/Packet processors to allow for external processing of a serial data stream. The Ingress Flexible Bandwidth Interface functions are described in Section 13.4.

Figure 93 Ingress Flexible Bandwidth Serial Stream

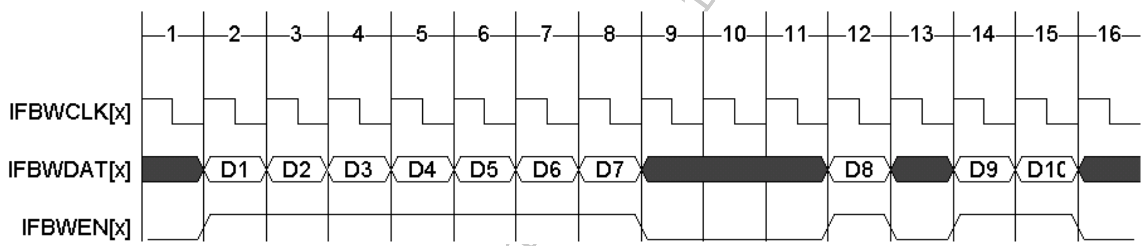


Figure 93 illustrates the functional timing of the Ingress Flexible Bandwidth Interface. IFBWDAT[x] and IFBWEN[x] are sampled on the rising edge of IFBWCLK[x]. When IFBWEN[x] is sampled high, IFBWDAT[x] is considered valid and the sampled value is used inside the S/UNI-12xJET. When IFBWEN[x] is sampled low, IFBWDAT[x] is considered invalid and is ignored. No gapping of the IFBWCLK[x] is allowed since it is used to clock other portions of the chip, while acting as the interface clock to the data processors.

14.8 Egress Flexible Bandwidth Interface

The Egress Flexible Bandwidth interface is used to extract a serial stream out of the Cell/Packet processors to allow for external processing of a serial data stream. The Egress Flexible Bandwidth Interface functions are described in Section 13.4.

Figure 94 Egress Flexible Bandwidth Serial Stream

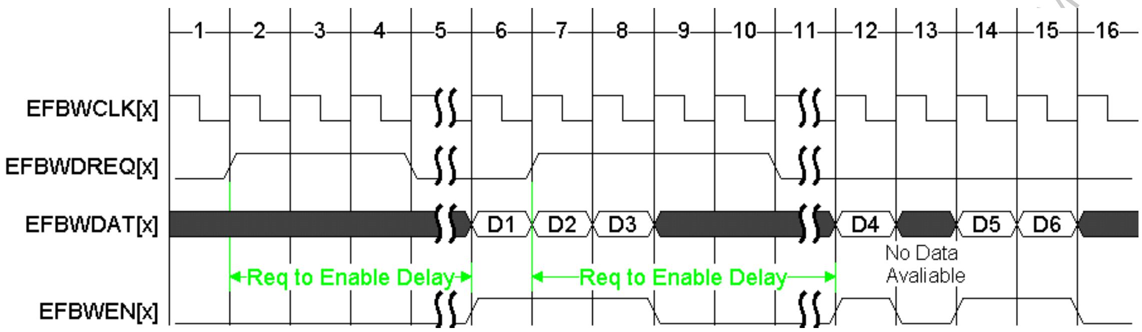


Figure 94 illustrates the functional timing of the Egress Flexible Bandwidth Interface. When EFBWDREQ[x] is asserted, a request is sent to the TXFP/TXCP (Transmit Packet/Cell processors). This invokes a read of data from the processors and the data is presented on EFBWDAT[x] and validated with EFBWEN[x]. When EFBWEN is asserted, EFBWDAT is valid. When EFBWEN is de-asserted, EFBWDAT is invalid and is to be ignored. If a request/acknowledge interface is not required, EFBWDREQ[x] may be tied high, and the value of EFBWEN[x] is used to determine if valid data is present on EFBWDAT[x]. Note that when the receiving data from TXCP and TXFP (when not in non-delineation mode), for every EFBWDREQ[x] there will be an EFBWEN[x]. Another option is to tie EFBWDREQ high, and gap EFBWCLK to control the bandwidth of the egress data stream. The latency between EFBWDREQ[x] and EFBWEN[x] is variable, based on channel (x) and mode of operation; however the maximum latency (Request to Enable Delay in Figure 94) is 16 clock cycles.

14.9 ATM UTOPIA Level 2 System Interface

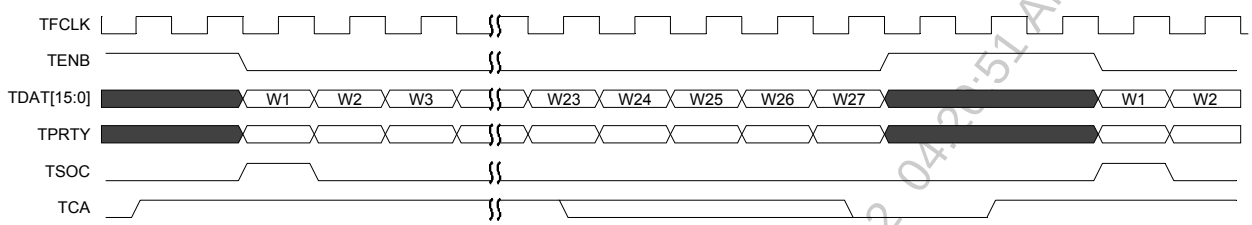
The ATM UTOPIA Level 2 System Interface is compatible with the UTOPIA Level 2 specification (see References). The S/UNI-12xJET only supports the 16-bit mode of operation.

The Transmit UTOPIA Level 2 System Interface Timing diagram Figure 95 illustrates the operation of the system side transmit FIFO interface. Assertion of the transmit cell available output, TCA, indicates that there is space available in the transmit FIFO for at least one ATM cell structure. De-assertion of TCA occurs when the FIFO is filled with the number of ATM cells indicated by the register bits FIFODP[1:0]. If the TCA is configured to de-assert early before the FIFO is truly full, the FIFO will accept additional cells even if TCA is inactive. At any time, if the upstream does not have a word to write, it must de-assert TENB.

As well, the TCA may be configured to de-assert after the last word of a cell is written into the FIFO (FIFO is full) or as the cell is being written into the FIFO (FIFO is near full). In addition, the register bit TCAINV can be used to invert the polarity of TCA.

TSOC must be high during the first word of the ATM cell structure and must be present for the start of each cell. When TSOC is asserted and the previous word transfer was not the end of an ATM cell structure, the system interface realigns itself to the new timing, and the previous partially transferred cell is dropped.

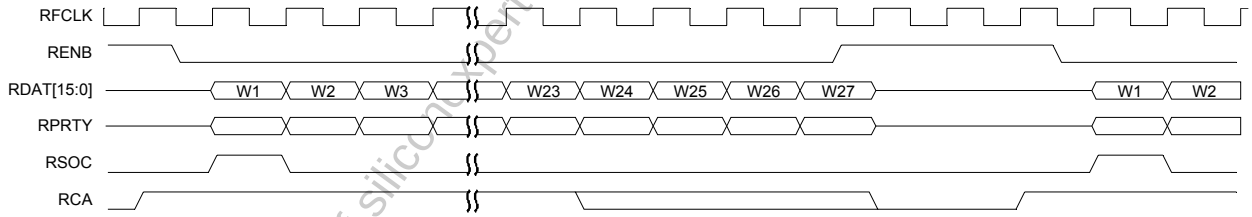
Figure 95 Transmit UTOPIA Level 2 System Interface Timing



The Receive UTOPIA Level 2 System Interface Timing diagram Figure 96 illustrates the operation of the system side receive interface. The RXCP indicates that a cell is available by asserting the receive cell available output RCA. RCA remains high until the receive FIFO is empty. After RCA is de-asserted, it remains low for a minimum of one RFCLK clock cycle and can then reassert to indicate that there are additional cells available in the FIFO.

At any time, the downstream reader can throttle back the reception of words by de-asserting RENB. The RDAT[15:0], RPRTY and RSOC signals tri-state when RENB is sampled de-asserted. RSOC is high during the first word of the cell and is present for each cell.

Figure 96 Receive UTOPIA Level 2 System Interface Timing



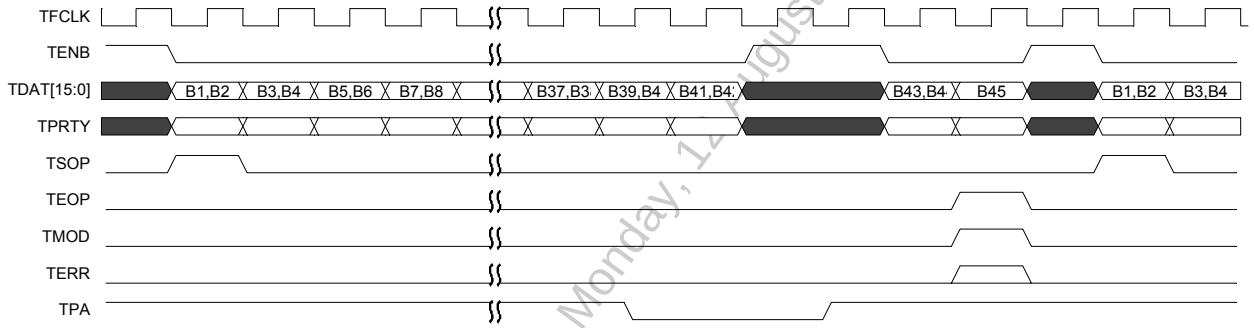
14.10 Packet over SONET/SDH (POS) Level 2 System Interface

The Packet over SONET/SDH (POS) System Interface is compatible with the POS-PHY Level 2 specification (see References). The S/UNI-12xJET supports the byte level and packet level transfer modes of POS-PHY.

The Transmit POS Level 2 System Interface Timing diagram Figure 97 illustrates the operation of the system side transmit FIFO interface. Assertion of the transmit packet available output, TPA, indicates that there is space available in the transmit FIFO. De-assertion of TPA occurs when the FIFO is filled to the depth indicated by the register TPAHWM[7:0]. The exact octet that triggers the de-assertion of TPA depends on the particular timing relationship between the internal SONET/SDH clock and TFCLK, and for that reason is not precise. However the TXFP is always conservative. Thus, when TPA de-asserts with no more than TPAHWM[7:0] bytes in the FIFO remains. If TPA is asserted and the upstream is ready to write a byte, the upstream device should assert TENB. At any time, if the upstream does not have a word to write, it must de-assert TENB. In addition, the register bit TPAINV can be used to invert the meaning of TPA.

TSOP must be high during the first word of the packet and must be present for the start of each packet. TEOP must be high during the last packet word/byte transferred. During a packet transfer, every word must be composed of two bytes and TMOD shall be low. TMOD is used to during the last word of the packet transfer to determine if the word is composed of one or two bytes. It is legal to assert TSOP and TEOP at the same time. This case occurs when a 1-byte or a 2-byte packet is transferred. When TSOP is asserted and the previous word transfer was not marked with TEOP, the system interface realigns itself to the new timing, and the previous packet is aborted.

Figure 97 Transmit POS Level 2 System Interface Timing Diagram



The Receive POS Level 2 System Interface Timing diagram Figure 98 illustrates the operation of the system side receive interface. The RXFP indicates that a packet is available by asserting the receive packet available output RPA. RPA remains high until the receive FIFO is empty. After RPA is de-asserted, it remains low for a minimum of one RFCLK clock cycle and then can assert to indicate that there are additional packets available in the FIFO. At any time, the downstream reader can throttle back the reception of words by de-asserting RENB.

RSOP is high during the first word of the packet. REOP is high during the last packet word. During a packet transfer every word is composed of two bytes. RMOD is used during the last word of the packet transfer to determine if the last word is composed of one or two bytes. It is legal to assert RSOP and REOP at the same time. This case occurs when a 1-byte or a 2-byte packet is transferred. Packets that were subject to an error (aborted, length violation, FIFO overrun, etc) will be marked by RERR high during the last word transfer.

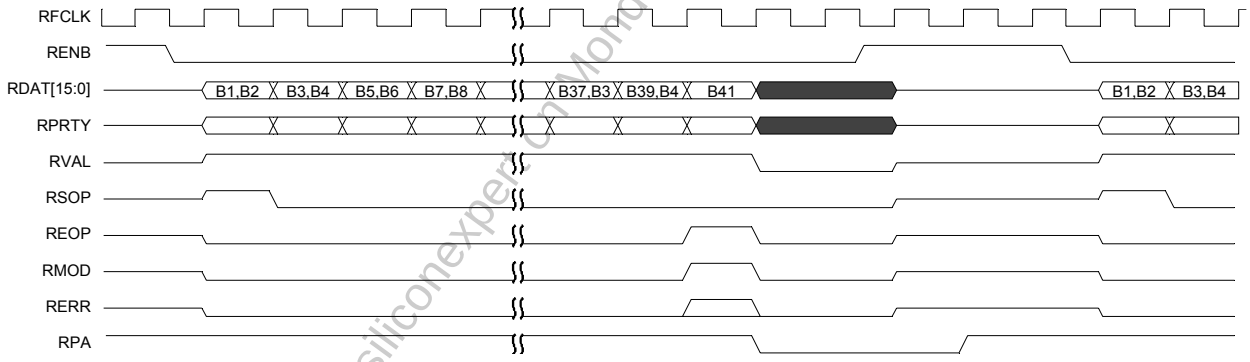
When a packet with less than 6 bytes arrives (from the line side), the receive packet available signal (RPA) may assert before data is available. In this condition, RPA will assert between 1 to 3 RFCLK clock cycles before the data is available and will remain asserted for 1 to 3 RFCLK clock cycles. When the Link Layer device attempts to read the packet by asserting read enable (RENB), it may find that there is no valid data available (receive data valid signal (RVAL) remains de-asserted). RPA will correctly assert again later when data is available. At this time the RVAL signal will be asserted indicating valid data.

With packets greater than 6 bytes, the RPA signal will assert, de-assert and then reassert 1 to 3 RFCLK cycles later (same as the above case with packets less than 6 bytes). However, if the Link layer device attempts to read the packet on the basis of the first occurrence of RPA, it will read valid data (RVAL will be asserted), even if RPA may be de-asserted.

This early assertion of RPA will not cause any data corruption if RVAL is used to qualify the data that is read. It is recommended that RVAL always be used to qualify receive data. The operation of RPA may cause a slight reduction bandwidth on receive side of the POS-PHY interface. However, since there is ample bandwidth on the POS-PHY interface there will be no impact on performance of functionality.

During the transfer of a packet, valid data is marked by RVAL high. If the FIFO under-runs, or if REOP is encountered, the RXFP will de-assert RVAL to halt the transfer, and the link layer device must de-assert RENB. A new transfer may then be started by asserting RENB when RPA indicates that more packet data is available.

Figure 98 Receive POS Level 2 System Interface Timing



The receive POS-PHY Level 2 interface cannot support full bandwidth with arbitrarily small consecutive packets. In general, the minimum consecutive packet size the interface can transfer without overrunning the receive FIFO in the TXFP is a function of how quickly the downstream logic reselects the S/UNI-12xJET after an end of packet is transferred on the bus. If the number of cycles between packet transfers (that is, the number of RFCLK cycles between RVAL going low, RENB de-asserting and then reasserting) is keep small, the minimum full-bandwidth packet size can be as low as 15 to 20 bytes.

14.11 Transmit ATM UTOPIA Level 3 System Interface

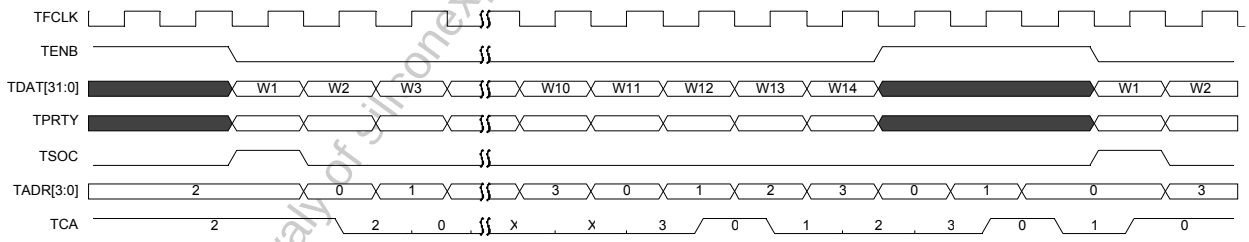
The ATM UTOPIA Level 3 System Interface is compatible with the UTOPIA Level 3 specification (see References). The S/UNI-12xJET only supports the 32-bit mode of operation.

The Transmit UTOPIA Level 3 System Interface Timing diagram Figure 99 illustrates the operation of the system side transmit FIFO interface. Assertion of the transmit cell available output, TCA, indicates that there is space available in the transmit FIFO for at least one ATM cell structure. De-assertion of TCA occurs when the FIFO is filled with the number of ATM cells indicated by the register bits FIFODP[1:0]. TCA will only de-assert one clock cycle after TSOC is sampled high and may assert at any time. If the TCA is configured to de-assert early before the FIFO is truly full, the FIFO will accept additional cells even if TCA is inactive. At any time, if the upstream does not have a cell to write, it must de-assert TENB.

PHY selection occurs by setting the TADR[4:0] bus with the PHY address when TENB changes from a high to a low value. In the example, a 56-byte ATM cell structure written to PHY #2 which reports that the FIFO is full after the start of the cell is written into the FIFO. The PHY channels are polled and PHY #0 reports it can accept at least one ATM cell. A cell is written into PHY #0 which is not full since the transmit cell available TCA does not de-assert after the start of the ATM cell is written into the FIFO.

TSOC must be high during the first byte of the ATM cell structure and must be present for the start of each cell. Thus, TSOC will mark the word with the H1 to H4 bytes. When TSOC is asserted and the previous byte transferred was not the end of an ATM cell structure, the system interface realigns itself to the new timing, and the previous partially transferred cell is dropped. The length of the cell structure can be configured for 52 and 56 bytes using the CELLFORM register in TUL3.

Figure 99 Transmit UTOPIA Level 3 System Interface Timing



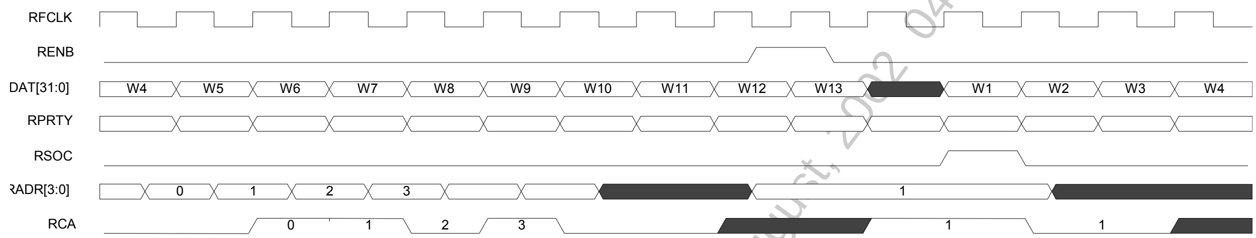
14.12 Receive ATM UTOPIA Level 3 System Interface

The Receive UTOPIA Level 3 System Interface Timing diagram Figure 100 illustrates the operation of the system side receive interface. Assertion of the receive cell available output, RCA, indicates that there is at least one ATM cell structure in the channel FIFO. Internally a channel's RCA status must only de-assert one clock cycle after RSOC has been sampled high by the layer device. A channel's RCA may reassert at any time when a cell is received.

PHY selection occurs by setting the RADR[3:0] bus with the PHY address when RENB changes from a high to a low value. RENB should de-assert when the cell structure of the last cell in the FIFO has finished being transferred. Once the cell transfer has started, the interface cannot be paused. In the example, a 52-byte ATM cell structure read from a PHY. The PHY channels are polled and PHY #0, #1 and #3 report they have at least one ATM cell. A cell is then read from PHY #1.

RSOC is high during the first word of the ATM cell structure and is present for the start of each cell. Thus, RSOC will mark the H1 to H4 bytes in the ATM cell structure. The length of the cell structure can be configured for 52 and 56 bytes using the CELLFORM register in RUL3.

Figure 100 Receive UTOPIA Level 3 System Interface Timing



Note :

- In Figure 100, the value of the selected PHY on RADR[3:0] when RENB is asserted high, only requires one clock cycle. Other PHYs may be polled the following clock-cycle after a PHY selection has occurred.

14.13 Transmit Packet over SONET/SDH (POS) Level 3 System Interface

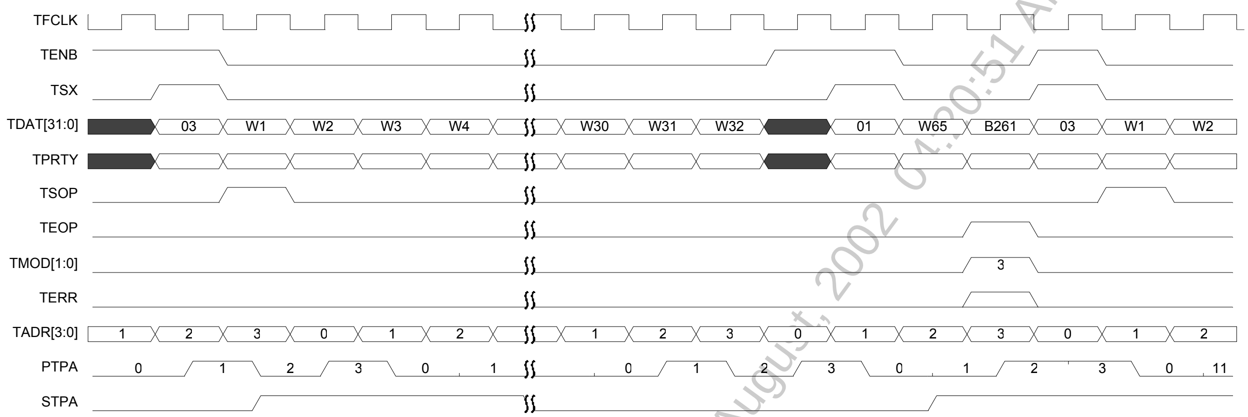
The Packet over SONET/SDH (POS) Level 3 System Interface is compatible with the POS-PHY Level 3 specification (see References). The S/UNI-12xJET only supports the 32-bit mode of operation.

The Transmit POS Level 3 System Interface Timing diagram Figure 101 illustrates the operation of the system side transmit FIFO interface. Assertion of the transmit packet available output, PTPA/STPA, indicates that the FIFO fill level is below the low water mark configured by LWM[7:0]. De-assertion of the transmit packet available output occurs when the FIFO fill level is above the high water mark configured by HWM[7:0]. When a channel is polled with PTPA high and the upstream is ready to write data, the upstream device should select the PHY using TSX and then assert TENB to write data. At any time, if the upstream does not have a byte to write, it must de-assert TENB.

PHY selection is performed by using in-band addressing. The TDAT[7:0] bus contains the PHY address to be selected and is identified by TSX and TENB high. The TADR[4:0] bus is only used for polling the FIFO fill status of the other PHY channels. The PTPA reports the polled FIFO fill status while the STPA reports the FIFO fill status selected by TSX.

TSOP must be high during the first byte of each packet. TEOP must be high during the last byte of the packet. It is legal to assert TSOP and TEOP at the same time. This case occurs when a one, two, three or four byte packet is transferred. When TSOP is asserted and the previous byte transfer was not marked with TEOP, the system interface realigns itself to the new timing, and the previous packet is marked to be aborted.

Figure 101 Transmit POS Level 3 System Interface Timing



When transferring ATM cell structures over the POS-PHY interface, the start of the ATM cell structure must be marked by TSOP and the end of the ATM cell structure must be marked by TEOP. The TMOD[1:0] and TERR signals must be low. The ATM cell structure must be configured by the CELLFORM register in TUL3.

14.14 Receive Packet over SONET/SDH (POS) Level 3 System Interface

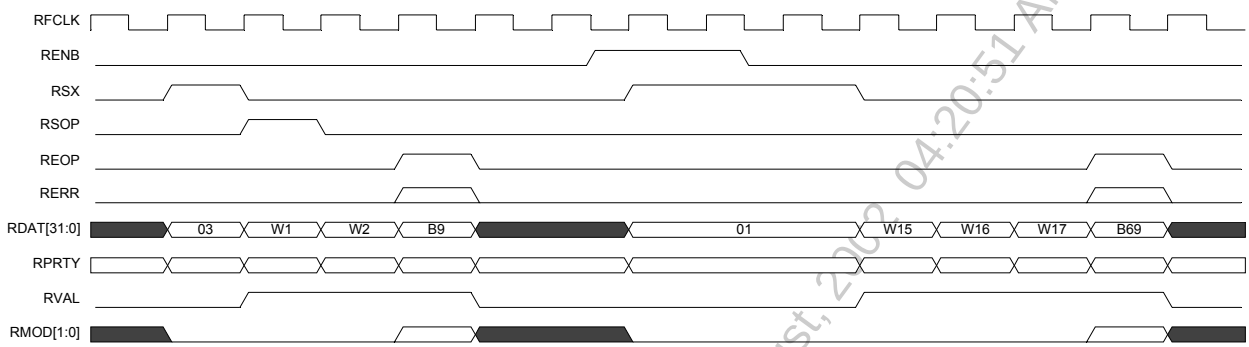
The Receive POS Level 3 System Interface Timing diagram Figure 102 illustrates the operation of the interface. When the channel FIFO has sufficient data to perform a transfer, the RUL3-32 performs an in-band address cycle with RSX set high. During this cycle, the RDAT[7:0] bus contains the PHY address to be selected.

PHY selection is performed by using in-band addressing. The RDAT[7:0] bus contains the PHY address being selected and is identified by RSX high and RVAL low. When RVAL is high, valid packet data is available on the POS-PHY interface. RENB is used by the layer device to pause the interface.

In the example, the RUL3 selects PHY #3 and transfers a nine byte packet. The RUL3-32 then pauses for two clock cycles due to the PAUSE[1:0] registers being configured for the two clock cycles between transfers. This pause allows the layer device to cleanly pause on the in-band address by de-asserting RENB after it samples REOP high. The layer device then reasserts the RENB and the RUL3-32 selects PHY #1. The next packet transferred is the end of a 69 byte packet.

RSOP is high during the first word of each packet. REOP is high during the last word of the packet. It is legal to assert RSOP and REOP at the same time. This case occurs when a 1-byte, 2-byte, 3-byte or 4-byte packet is transferred. The RVAL signal qualifies the data on the bus.

Figure 102 Receive POS Level 3 System Interface Timing



The receive POS-PHY Level 3 interface cannot support full bandwidth with arbitrarily small consecutive packets. In general, the Level 3 interface can carry consecutive 40 byte packets without the RUL3 channel FIFO overflowing.

14.15 Incoming Parallel TelecomBus

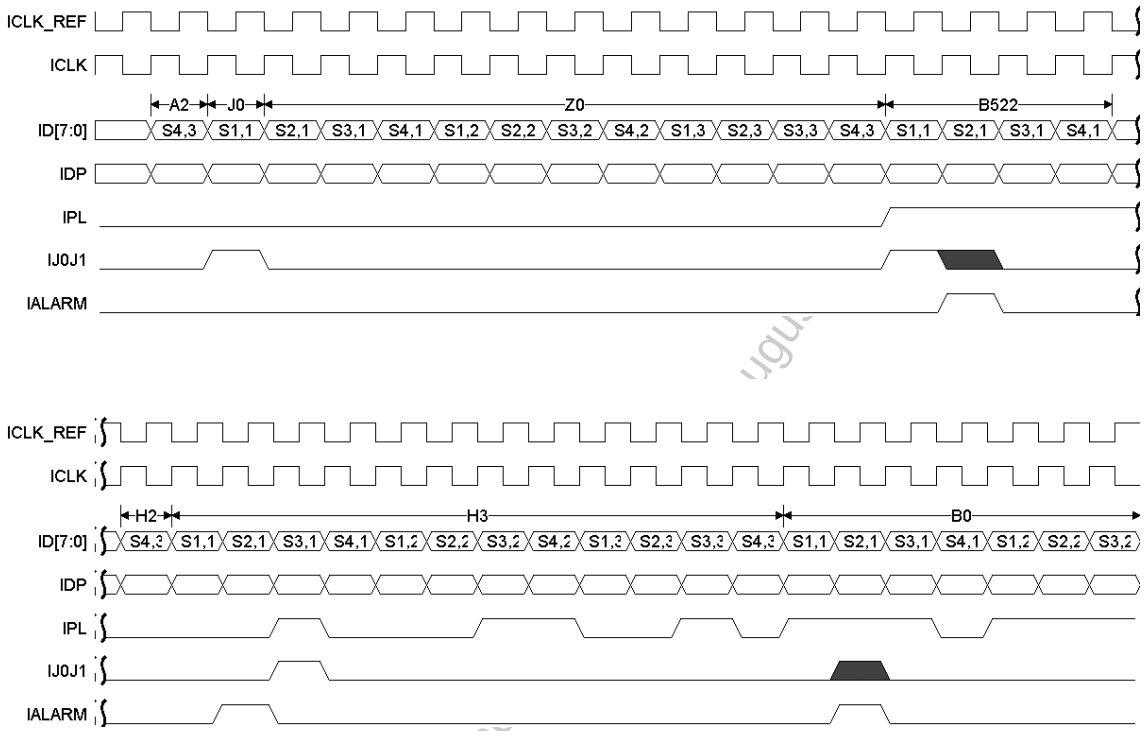
Figure 103 shows the timing of the Incoming TelecomBus interface. Timing is provided by ICLK. SONET/SDH data is carried in the ID[7:0]. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte.

A timeslot naming strategy and assignment on an ID[7:0] bus is shown in Figure 103. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The IPL signal is set high to mark payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal IJ0J1 is set high with IPL set low to mark the J0 byte of a transport frame. IJ0J1 is set high with IPL also set high to mark the J1 byte of all the streams within ID[7:0].

High order streams in AIS alarm are indicated by the IALARM signal. Assertion of the AIS alarm will cause the cell/packet delineation blocks to lose alignment. The ICMP signal selects the active connection memory page in the Ingress Working Time-slot Interchange (IWTI) block. It is only valid at the J0 byte position and is ignored at all other positions within the transport frame. The J0 byte position on all four buses must be aligned.

In Figure 103, timeslots numbers S1,x, S2,y, and S4,z are configured as STS-1/STM-0 operation. Timeslot number S3,n is configured for STS-3c/STM-1 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on IPL and IJ0J1 at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path AIS (IALARM set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is a configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by IJ0J1 being set high at byte S3,1/H3 and IPL being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3.

Figure 103 Incoming Parallel TelecomBus Timing



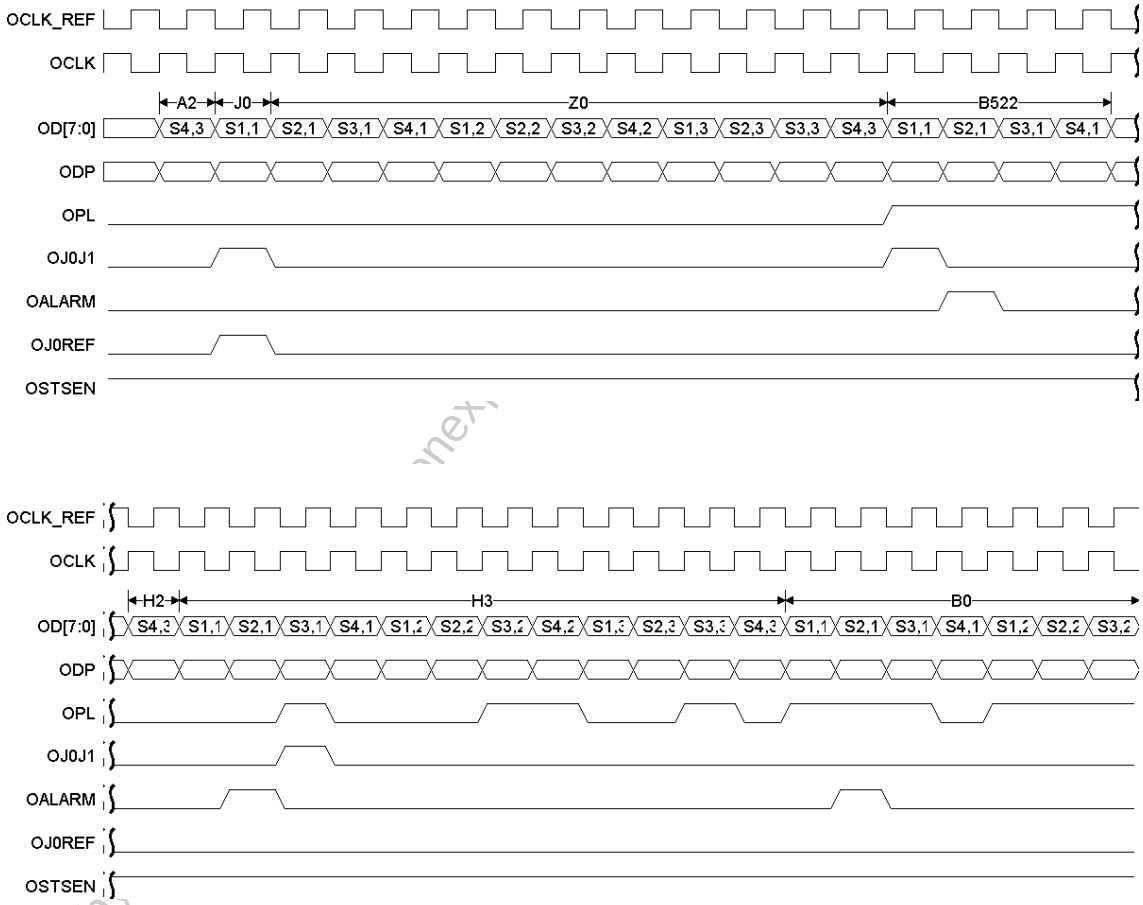
14.16 Outgoing Parallel TelecomBus

Figure 104 shows the timing of the Outgoing TelecomBus interface. Timing is provided by OCLK. SONET/SDH data is carried in the OD[7:0]. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. The OWTI block can be used to rearrange timeslots between the system side and the line side of the S/UNI-12xJET.

The timeslot naming strategy and assignment is shown in Figure 104. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The OPL signal is set high to mark payload bytes and is set low at all other bytes. The OJ0J1 signal is set high with the OPL signal set low to mark the J0 byte of a transport frame. OJ0J1 is set high with OPL also set high to mark the J1 byte of all the streams within OD[7:0]. High order streams in alarm are indicated by the OALARM signal.. For Figure 104 OJ0REFDLY[13:0] is set to all zeros.

In Figure 104, timeslots S1,x, S2,y, and S4,z are configured for STS-1/STM-0 operation. Timeslot S3,n is configured for STS-3c/STM-1 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on OPL and OJ0J1 at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path alarm (OALARM set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is a configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by OJ0J1 being set high at byte S3,1/H3 and OPL being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3. Stream S4,1 is shown to undergo a positive pointer justification event as indicated by the low level on OPL at byte S4,1/B0.

Figure 104 Outgoing Parallel TelecomBus



14.17 Receive Transport Overhead

Figure 105 RTOH output timing

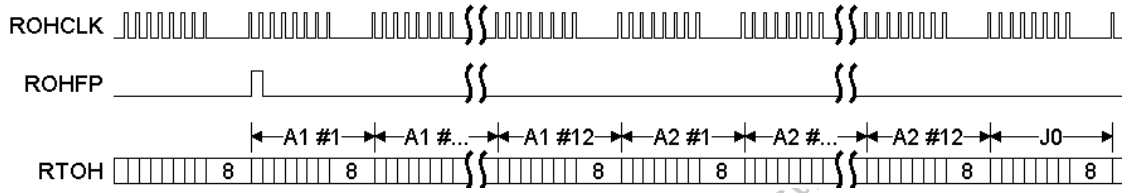


Figure 106 RTOH and ROHFP output timing

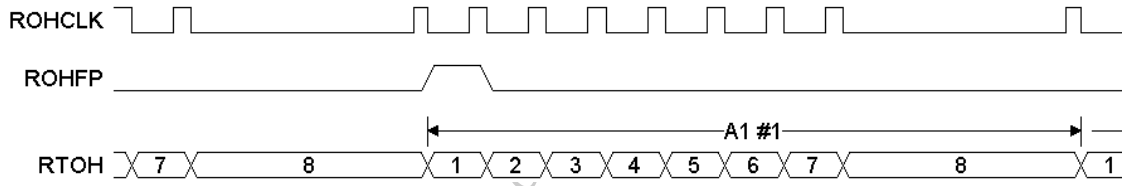


Figure 105 shows the receive transport overhead (RTOH) functional timings. ROHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz clock (33% high duty cycle). 2592 bits (9x3x12 bytes) are output on RTOH between two ROHFP assertions.

Figure 106 shows that RTOH and ROHFP are aligned with the falling edge of ROHCLK. The rising edge of ROHCLK should be used to sample RTOH and ROHFP. Sampling ROHFP high identifies the MSB of the first A1 byte on RTOH.

14.18 Receive Section and Line DCC

Figure 107 ROHFP and RSLD output timing (RSLDSEL = 0)

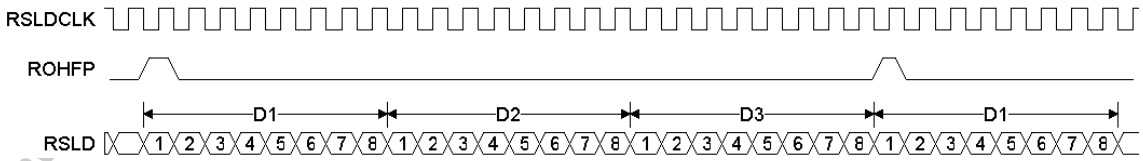


Figure 108 ROHFP and RSLD output timing (RSLDSEL = 1)

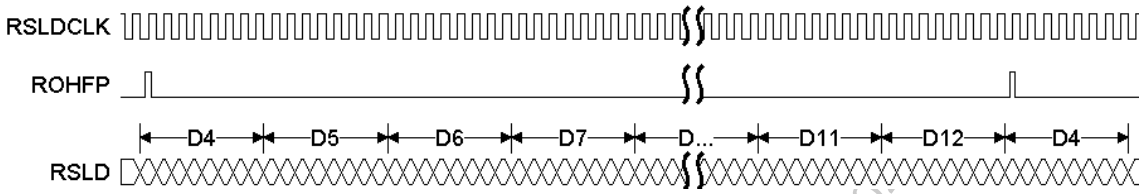


Figure 107 and Figure 108 show the receive section/line DCC (RSLD) functional output timings. When RSLDSEL is set to zero, RSLD and RSLDCLK are carrying the section DCC bytes (D1-D3). When RSLDSEL is set to one, RSLD and RSLDCLK are carrying the line DCC bytes (D4-D12).

RSLDCLK is a 192 kHz clock when carrying the section DCC and a 576 kHz clock when carrying the line DCC. RSLD is aligned with the falling edge of RSLDCLK. The rising edge of RSLDCLK should be used to sample RSLD and ROHFP. Sampling ROHFP high identifies the MSB of the D1 or D4 byte on the RSLD output.

14.19 Receive Path Overhead Port

Figure 109 shows the receive path overhead (RPOH) functional timings. The RPOH port (RPOH, RPOHEN and B3E) is used to output the POH bytes of the STS (VC) payloads and the path BIP-8 errors. The POH bytes are output on RPOH MSB first in the same order that they are received. Since ROHFP is synchronized on the transport frame, zero, one or two path overhead can be output per path per frame. RPOHEN is used to indicate new POH bytes on RPOH. RPOHEN is either asserted or de asserted for the nine POH bytes. The path BIP-8 errors are output on B3E at the same time the path trace byte is output on RPOH. Optionally, block BIP-8 errors can be output on B3E.

Note: RPOHEN will be asserted to validate zero, one or two opportunities per path per frame out of three opportunities. RPOHEN opportunities will alternate from path to path and from frame to frame based on pointer movement.

Figure 109 shows that RPOH and RPOHEN are aligned with the falling edge of ROHCLK. The rising edge of ROHCLK should be used to sample RPOH and RPOHEN. Sampling ROHFP high identifies the MSB of the path trace byte of STS-1/STM-0 #1 on RPOH and the first possible path BIP-8 error of STS-1/STM-0 #1 on B3E.

Figure 109 RPOH output timing

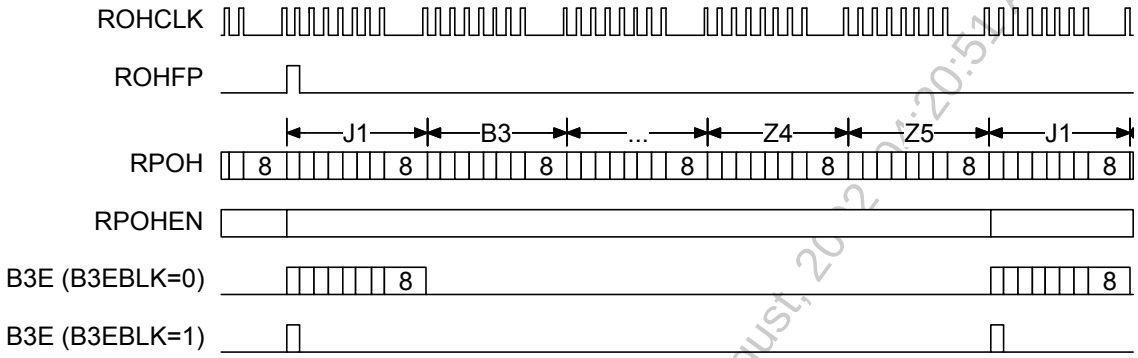
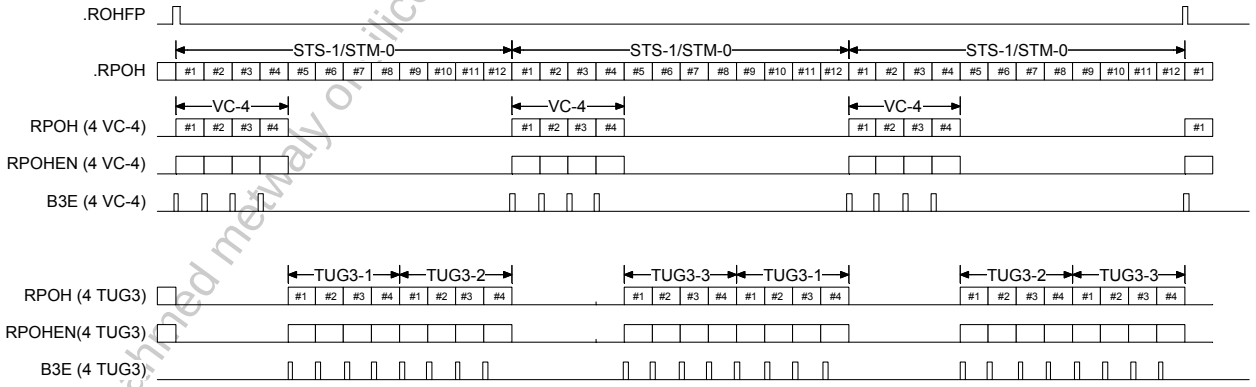


Figure 110 shows the STS-1/STM-0 time slots assignment on RPOH. Since ROHFP is synchronized on the transport frame, zero, one or two path overhead can be output per path per frame. To avoid loosing any POH bytes, three time slots are assigned per path per frame. In STS (AU) mode, the time slots are repeatedly assigned from STS-1/STM-0 #1 to #12. Figure 110 shows the case of a STM-4 data stream carrying four VC-4 payloads. Only the master VC-4 STS-1/STM-0 time slots contain valid POH bytes. Figure 110 shows the case of four VC-4 payloads carrying four TUG3 payloads. Both the master and the slave VC-4 STS-1/STM-0 time slots contain valid POH bytes.

Figure 110 RPOH STS-1/STM-0 time slots output timing



14.20 Transmit Transport Overhead

Figure 111 TTOH and TTOHEN input timing

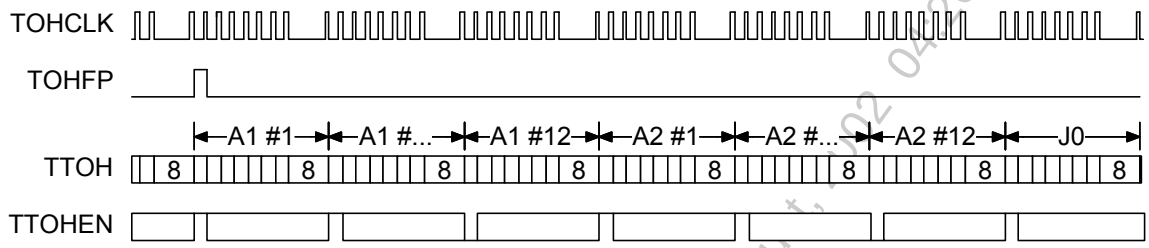


Figure 112 TTOH and TOHFP input timing

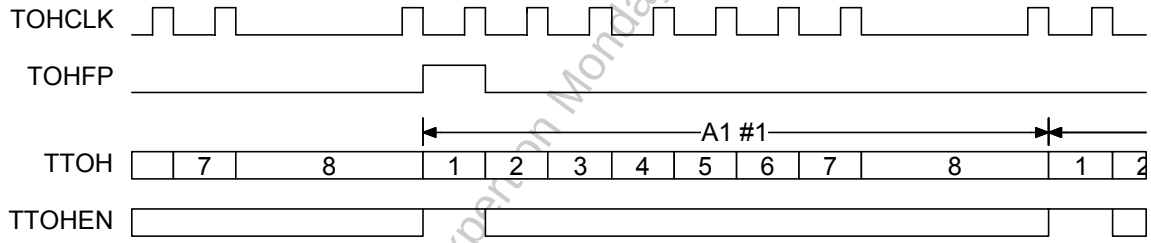


Figure 111 shows the transmit transport overhead (TTOH) functional timings. TOHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz clock (33% high duty cycle). 2592 bits (9x3x12 bytes) are input on TOH between two TOHFP assertions.

TTOHEN is used to validate the insertion of the corresponding byte on TTOH. When TTOHEN is sampled high on the MSB of the byte, the byte will be inserted in the transport overhead. When TTOHEN is sampled low on the MSB of the byte, the byte is not inserted. TTOH and TTOHEN are sampled with the rising edge of TOHCLK. TOHFP is aligned with the falling edge of TOHCLK. The rising edge of TOHCLK should be used to sample TOHFP. Sampling TOHFP high identifies the MSB of the first A1 byte on TTOH.

14.21 Transmit Section and Line DCC

Figure 113 TOHFP and TSLD Output Timing (TSLDSEL = 0)

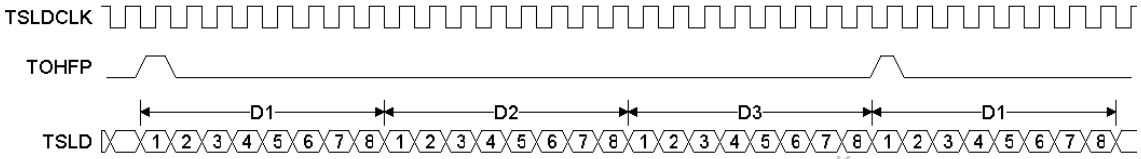


Figure 114 TOHFP and TSLD Output Timing (TSLDSEL = 1)

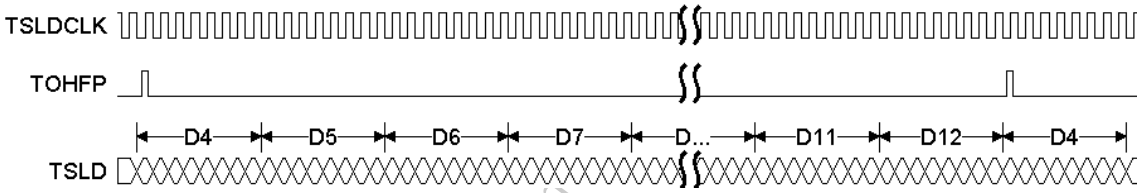


Figure 113 and Figure 114 show the transmit section/line DCC (TSLD) functional input timings. When TSLDSEL is set to zero, TSLD and TSLDCLK are carrying the section DCC bytes (D1-D3). When TSLDSEL is set to one, TSLD and TSLDCLK are carrying the line DCC bytes (D4-D12).

TSLDCLK is a 192 kHz clock when carrying the section DCC and a 576 kHz clock when carrying the line DCC. TSLD is sampled with the rising edge of TSLDCLK. TSLDCLK is generated such that the rising edge of TSLDCLK can be used by external logic to sample TOHFP with proper setup and hold time. Sampling TOHFP high identifies the MSB of the D1 or D4 byte on TSLD.

14.22 Transmit Path Overhead

Figure 115 shows the transmit path overhead (TPOH) functional timings. The TPOH port (TPOH, TPOHEN and TPOHRDY) is used to input the POH bytes of the STS (VC) payloads. The POH bytes are input on TPOH MSB first in the same order that they are transmit. Since TOHFP is synchronized on the transport frame, zero, one or two path overhead can be input per path per frame.

TPOHRDY is asserted to indicate that the S/UNI-12xJET is ready to receive POH bytes. TPOHEN is used to validate the insertion of the corresponding byte on TPOH. If TPOHRDY is logic high and TPOHEN is sampled high on the MSB of the byte, the byte will be inserted in the path overhead. When TPOHEN is sampled low on the MSB of the byte, the byte is not inserted in the output stream. If TPOHRDY is logic low and TPOHEN is sample high on the MSB of the byte, the byte will not be inserted in the path overhead and must be represented at the next opportunity.

TPOH and TPOHEN are sampled with the rising edge of TOHCLK. TPOHRDY is aligned with the falling edge of TOHCLK. The rising edge of TOHCLK should be used to sample TPOHRDY. Sampling TOHFP high identifies the MSB of the path trace byte of STS-1/STM-0 #1 on TPOH.

Figure 115 TPOH Input Timing

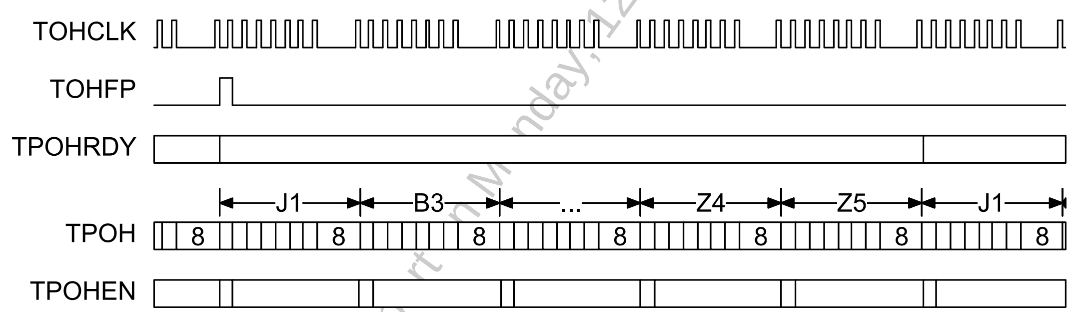
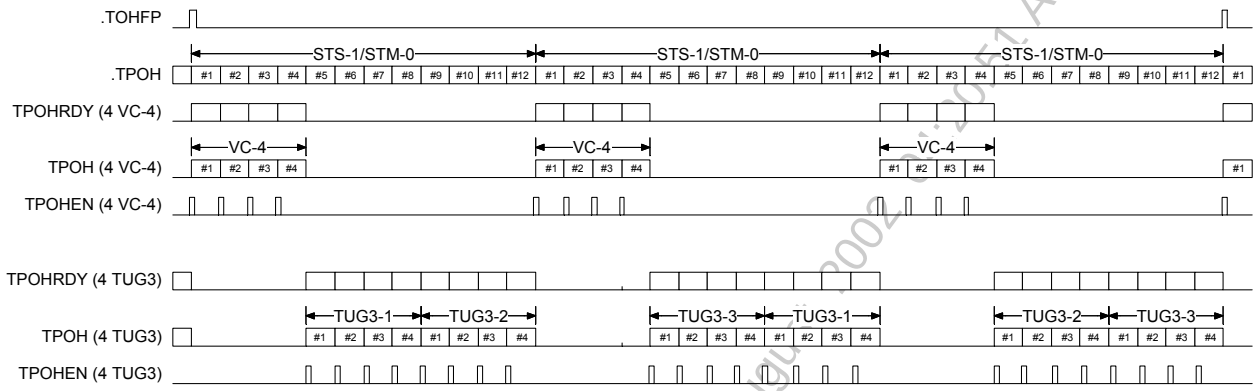


Figure 116 shows the STS-1/STM-0 time slots assignment on TPOH. Since TOHFP is synchronized on the transport frame, zero, one or two path overhead can be input per path per frame. To avoid loosing any POH bytes, three time slots are assigned per path per frame. In STS (AU) mode, the time slots are repeatedly assigned from STS-1/STM-0 #1 to #12. Figure 116 shows the case of a STM-4 data stream carrying four VC-4 payloads. Only the master VC-4 STS-1/STM-0 time slots contain valid POH bytes. Figure 116 shows the case of four VC-4 payloads carrying four TUG3 payloads. Both the master and the slave VC-4 STS-1/STM-0 time slots contain valid POH bytes.

Figure 116 TPOH STS-1/STM-0 Time Slots Input Timing



14.23 Receive SONET/SDH Interface

Figure 117 Receive SONET/SDH Functional Timing

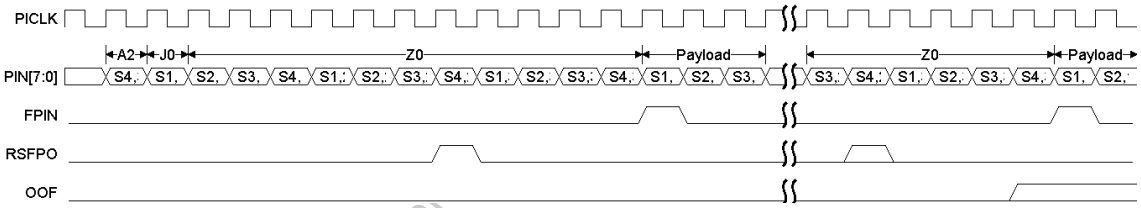


Figure 117 shows the functional timing of the PIN [7:0] input data bus and associated input frame pulse FPIN. When there is no frame realignment, two FPIN assertions or two RSFPO assertions are 125 us apart. When there is a frame realignment, two FPIN assertions or two RSFPO assertions are closer or further apart and then stabilize back to 125 us. OOF is asserted to signal out of frame, and may occur anywhere within the frame.

FPIN may be asserted for one PICLK clock cycle every frame, and is not required to be asserted every frame. When FPIN is not asserted, the internal counters flywheel on the last frame alignment. RSFPO is asserted for one PICLK clock cycle every 125 us as a frame pulse reference. A software programmable delay may used to change the relative delay between the incoming FPIN and the outgoing the RSFPO.

14.24 Transmit SONET/SDH Interface

Figure 118 Transmit SONET/SDH functional timing

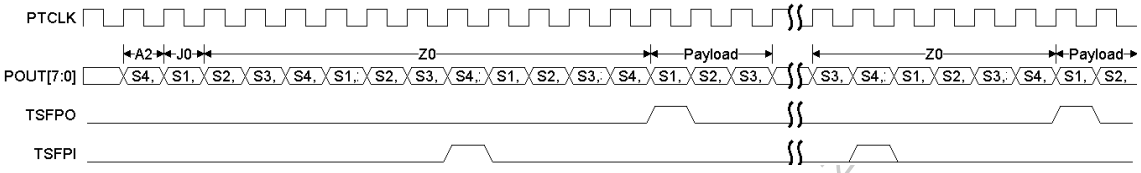


Figure 118 shows the functional timing of the POUT[7:0] output data bus and associated output frame pulse TSFPO. When there is no frame realignment, two TSFPI assertions or two TSFPO assertions are 125 us apart. When there is a frame realignment, two TSFPI assertions or two TSFPO assertions are closer or further apart and then stabilize back to 125 us.

TSFPI may be asserted for one PTCLK clock cycle every frame, and is not required to be asserted every frame. When TSFPI is not asserted, the internal counters flywheel on the last frame alignment. TSFPO is asserted for one PTCLK clock cycle when the first payload byte after the J0/Z0 bytes is available on the POUT[7:0] data bus, and is output every frame. A software programmable delay may used to change the relative delay between the incoming TSFPI and the outgoing the TSFPO.

15 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 43 Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
3.3V (VDDO/VDDQ) Supply Voltage	-0.3V to +4.6V
1.8V (VDDI) Supply Voltage	-0.3V to +2.5V
Input pad tolerance	-2 V < Vpin < VDDO +2 V for 10 ns, 100 mA max
Output pad overshoot limits	-2 V < Vpin < VDDO +2 V for 10 ns, 100 mA max
Voltage on Any Digital Pin	-0.3 V to VVDD+0.3 V
Static Discharge Voltage	±1000 V
Latch-Up Current per Pin	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

16 Normal Operating Conditions

Unless otherwise specified, all DC and AC specifications in this data sheet are valid for the following voltage and temperature ranges. These ranges show the typical IDD per supply, for the major operating modes, with outputs loaded, for vector sets and/or boards functioning normally.

Table 44 Normal Operating Conditions

	Operating Range[1]		Typical[2]
Operating Temperature	T_A = -40 °C to T_J =105 °C		T_J = 60 °C
Supply Voltages	**Minimum (V)**	**Typical (V)**	**Maximum (V)**
1.8V Supply Voltage (VDDI)	1.71	1.8	1.89
3.3V Supply Voltage (VDDO)	3.13	3.3	3.46
3.3V Analog Supply Voltage (AVD)	3.16	3.3	3.46

Notes

1. Power supply, D.C. characteristics, and A.C. timing are characterized across these operating ranges, unless otherwise stated
2. Where typical measurements are given, these parameter values will be used, unless otherwise stated

17 Power Information

17.1 Power Requirements

Table 45 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
Clear Channel PDH Spectra Mode	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
Clear Channel PDH Mach Mode	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
PDH Framer Only	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
Cell/Packet over PDH Utopia/POS-PHY Level 3	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
Cell/Packet over PDH Utopia/POS-PHY Level 2	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
AUX I/F over PDH over SONET Spectra Mode	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
AUX I/F over PDH over SONET Mach Mode	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
Cell/Packet Delineation Only Utopia/POS-PHY Level 3	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
Cell/Packet Delineation Only Utopia/POS-PHY Level 2	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
Cell/Packet over SONET Utopia/POS-PHY Level 3 Spectra Mode	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
Cell/Packet over SONET Utopia/POS-PHY Level 2 Spectra Mode	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A
	Total Power	TBD	TBD	—	W
Cell/Packet over SONET Utopia/POS-PHY Level 3	IDDOP (1.8V)	TBD	—	TBD	A
	IDDOP (3.3 V)	TBD	—	TBD	A

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
Mach Mode	Total Power	TBD	TBD	—	W
Cell/Packet over SONET	IDDOP (1.8V)	TBD	—	TBD	A
Utopia/POS-PHY Level 2	IDDOP (3.3 V)	TBD	—	TBD	A
Mach Mode	Total Power	TBD	TBD	—	W
Cell/Packet over PDH over SONET	IDDOP (1.8V)	TBD	—	TBD	A
Utopia/POS-PHY Level 3	IDDOP (3.3 V)	TBD	—	TBD	A
Spectra Mode	Total Power	TBD	TBD	—	W
Cell/Packet over PDH over SONET	IDDOP (1.8V)	TBD	—	TBD	A
Utopia/POS-PHY Level 2	IDDOP (3.3 V)	TBD	—	TBD	A
Spectra Mode	Total Power	TBD	TBD	—	W
Cell/Packet over PDH over SONET	IDDOP (1.8V)	TBD	—	TBD	A
Utopia/POS-PHY Level 3	IDDOP (3.3 V)	TBD	—	TBD	A
Mach Mode	Total Power	TBD	TBD	—	W
Cell/Packet over PDH over SONET	IDDOP (1.8V)	TBD	—	TBD	A
Utopia/POS-PHY Level 2	IDDOP (3.3 V)	TBD	—	TBD	A
Mach Mode	Total Power	TBD	TBD	—	W

Notes:

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, T_J=60 °C, outputs un-loaded, and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system

2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current.

3. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system

4. High power values are a “normal high power” estimate and are calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: T_J=105° C, outputs un-loaded. These values are suitable for evaluating board and device thermal characteristics

17.2 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

VDD power must be supplied either before VDDI or simultaneously with VDDI.

AVD can be applied either before or after VDD, but must be applied either before or simultaneously with VDDI. In operation, the differential voltage measured between AVD supplies and VDD_DC must be less than 0.5 volt. The relative power sequencing of the multiple AVD power supplies is not important.

I/Os get driven after all the supplies have been powered. Otherwise, the I/Os must be current limited to 20 mA.

Power down the device in the reverse sequence.

17.3 Power Supply Filtering

TBD

Notes:

1. Use a single plane for both digital and analog grounds.
2. Provide separate analog and digital supplies, but otherwise connect the supply voltages together at one point close to the connector where the voltage is brought to the card.
3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

18 D.C. Characteristics

Table 46 DC Characteristics for pins.

Symbol	Parameter	Min (V)	Typ (V)	Max (V)	Conditions
VIL	Input Low Voltage	-0.5	—	0.8	Guaranteed Input LOW Voltage
VIH	Input High Voltage	2.0	—	VDD+0.5	Guaranteed Input HIGH Voltage
VOL	Output or Bi-directional Low Voltage	—	0.1	0.4	VDD = min, IOL = -TBD mA[3]
VOH	Output or Bi-directional High Voltage	2.4	2.7	—	VDD = min, IOH = TBD mA[3]

Table 47 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VT+	Reset Input High Voltage	2.0	—	—	Volts	TTL Schmitt
VT-	Reset Input Low Voltage	—	—	0.8	Volts	TTL Schmitt
VTH	Reset Input Hysteresis Voltage	—	0.5	—	Volts	TTL Schmitt
IILPU	Input Low Current	+20	+83	+200	µA	VIL = GND[1,3]
IIHPU	Input High Current	-10	0	+10	µA	VIH = VDD[1,3]
IIL	Input Low Current	-10	0	+10	µA	VIL = GND[2,3]
IIH	Input High Current	-10	0	+10	µA	VIH = VDD[2,3]
CIN	Input Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF
COUT	Output Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF
CIO	Bi-directional Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF

Notes

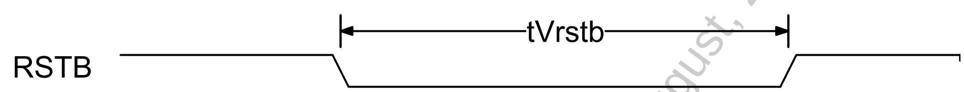
1. Input pin or bi-directional pin with internal pull-up resistor
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing)

19 A.C. Timing Characteristics

Table 48 RSTB Timing (Figure 119)

Symbol	Description	Min	Typical	Max	Units
tVRSTB	RSTB Pulse Width[4]		100		ns

Figure 119 RSTB Timing

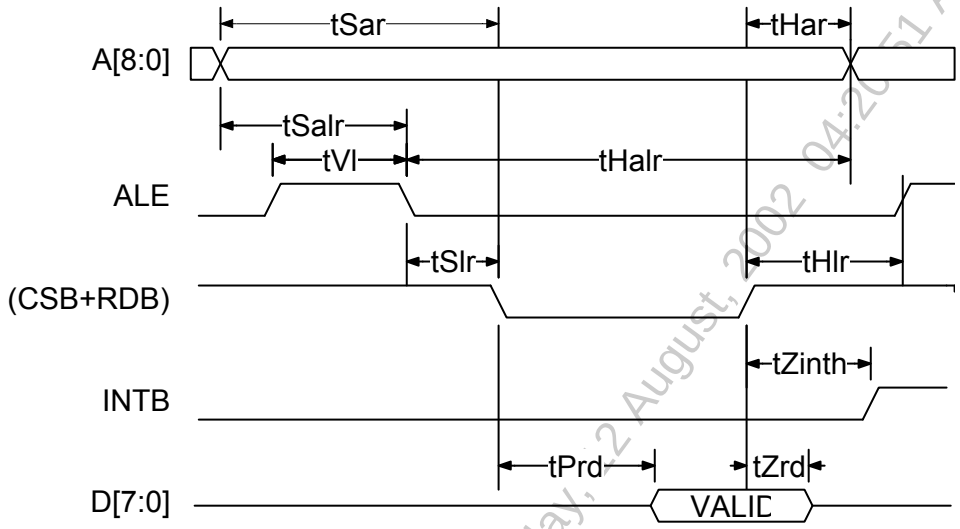


19.1 Microprocessor Interface Timing Characteristics

Table 49 Microprocessor Interface Read Access (Figure 120)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 120 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

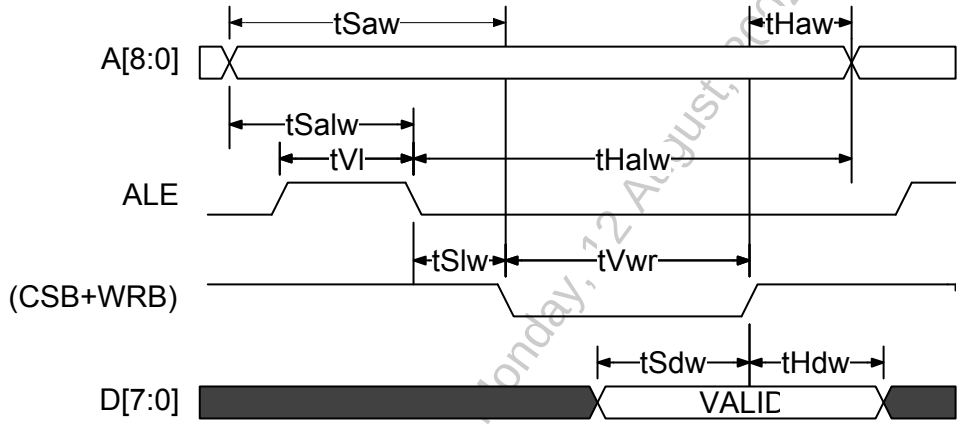
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 50 Microprocessor Interface Write Access (Figure 121)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns

Symbol	Parameter	Min	Max	Units
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 121 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

19.2 PDH Reference Clock Timing

Table 51 PDH Reference Clock Timing

Symbol	Description	Min	Typ	Max	Units
FDS3_REF	DS3_REFCLK Frequency		44.736		MHz
tRise_ DS3_REF	Rise time for DS3_REFCLK			1	ns
tFall_ DS3_REF	Fall Time for DS3_REFCLK			1	ns
DDS3_REF	DS3_REFCLK Duty Cycle	40	50	60	%
JDS3_REF	DS3_REFCLK Jitter 10Hz – 400 kHz			TBD	ps (rms)
	DS3_REFCLK Jitter 30kHz – 400 kHz			TBD	ps (rms)

Symbol	Description	Min	Typ	Max	Units
FE3_REF	E3_REFCLK Frequency		34.368		MHz
tRise_ DS3_REF	Rise time for DS3_REFCLK			1	ns
tFall_ DS3_REF	Fall Time for DS3_REFCLK			1	ns
DE3_REF	E3_REFCLK Duty Cycle	40	50	60	%
JE3_REF	E3_REFCLK Jitter 100Hz – 800kHz			TBD	ps (rms)
	E3_REFCLK Jitter 10kHz – 800kHz			TBD	ps (rms)

19.3 UTOPIA Level 2 System Interface Timing

Table 52 Transmit UTOPIA Level 2 System Interface Timing (Figure 122)

Symbol	Description	Min	Max	Units
FTFCLK	TFCLK Frequency	40	52	MHz
DTFCLK	TFCLK Duty Cycle	40	60	%
JTFCLK	TFCLK Peak to Peak Jitter (> 1 MHz)		1.4	ns
tS_{TADR}	TADR[4:0] Set-up time to TFCLK	3		ns
tH_{TADR}	TADR[4:0] Hold time to TFCLK	0		ns
tS_{TENB}	TENB Set-up time to TFCLK	3		ns
tH_{TENB}	TENB Hold time to TFCLK	0		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	3		ns
tH_{TSOC}	TSOC Hold time to TFCLK	0		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	3		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	0		ns
tS_{TDAT}	TDAT[15:0] Set-up time to TFCLK	3		ns
tH_{TDAT}	TDAT[15:0] Hold time to TFCLK	0		ns
tPTCA	TFCLK High to TCA Valid	1	10	ns

Figure 122 Transmit UTOPIA Level 2 System Interface Timing Diagram

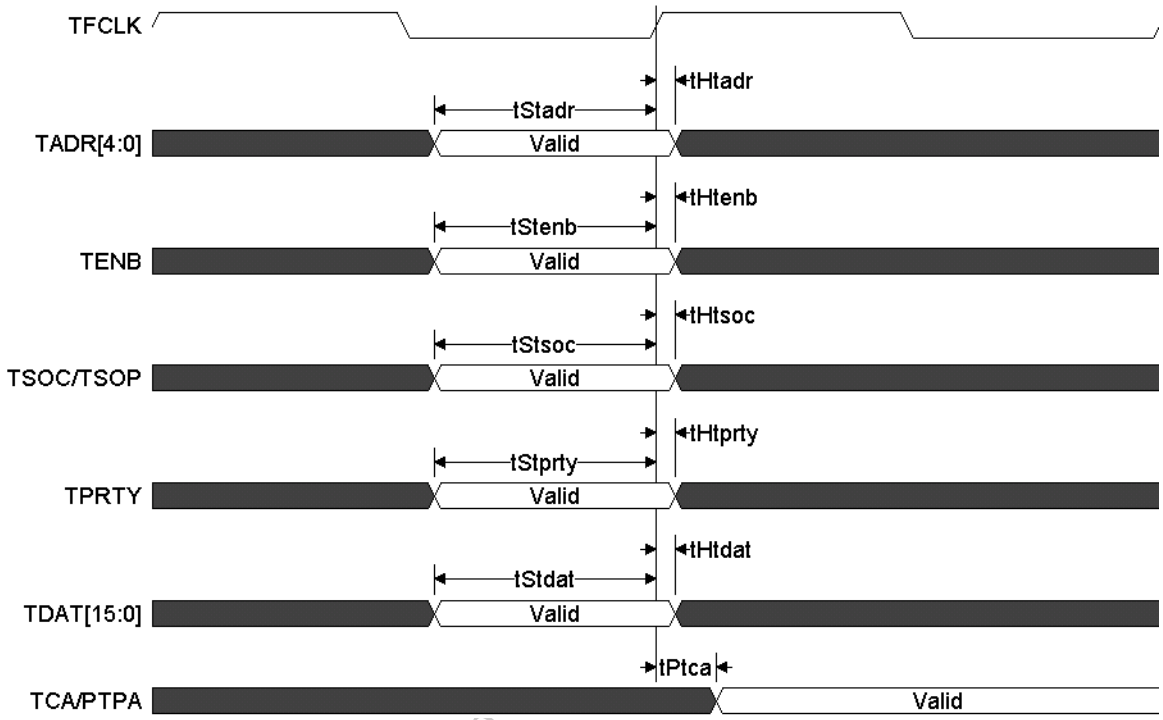
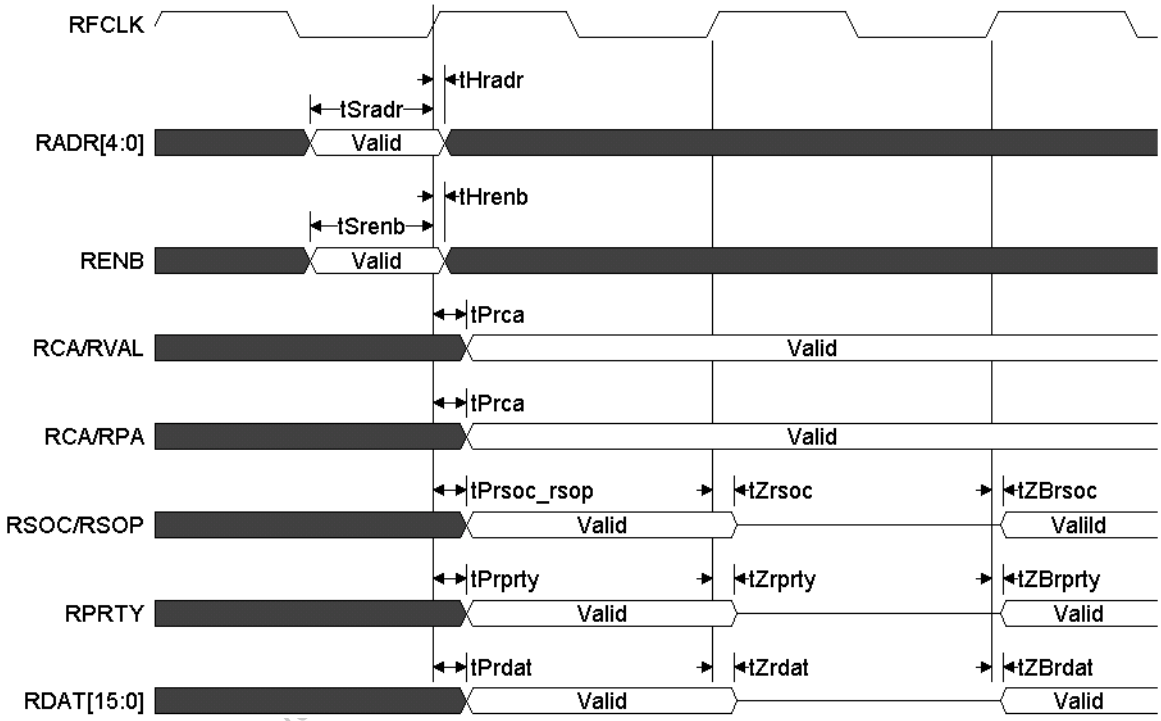


Table 53 Receive UTOPIA Level 2 System Interface Timing (Figure 123)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	40	52	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
J_{RFCLK}	RFCLK Peak to Peak Jitter (> 1 MHz)		1.4	ns
tS_{RADR}	RADR[4:0] Set-up time to RFCLK	3		ns
tH_{RADR}	RADR[4:0] Hold time to RFCLK	0		ns
tS_{RENB}	RENB Set-up time to RFCLK	3		ns
tH_{RENB}	RENB Hold time to RFCLK	0		ns
tP_{RCA}	RFCLK High to RCA Valid	1	10	ns
tP_{RSOC}	RFCLK High to RSOC Valid	1	10	ns
tZ_{RSOC}	RFCLK High to RSOC Tri-state	1	10	ns
tZB_{RSOC}	RFCLK High to RSOC Driven	1		ns
tP_{RPRT}	RFCLK High to RPRTY Valid	1	10	ns
tZ_{RPRTY}	RFCLK High to RPRTY Tri-state	1	10	ns

Symbol	Description	Min	Max	Units
tZB_{RPRTY}	RFCLK High to RPRTY Driven	0		ns
tP_{RDAT}	RFCLK High to RDAT[15:0] Valid	1	10	ns
tZ_{RDAT}	RFCLK High to RDAT[15:0] Tri-state	1	10	ns
tZB_{RDAT}	RFCLK High to RDAT[15:0] Driven	0		ns

Figure 123 Receive UTOPIA Level 2 System Interface Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

19.4 UTOPIA Level 3 System Interface Timing

Table 54 Transmit UTOPIA Level 3 System Interface Timing (Figure 124)

Symbol	Description	Min	Max	Units
f_{TFCLK}	TFCLK Frequency	60	104	MHz
D_{TFCLK}	TFCLK Duty Cycle	40	60	%
J_{TFCLK}	TFCLK Peak to Peak Jitter (> 1 MHz)		1	Ns
tS_{TADR}	TADR[4:0] Set-up time to TFCLK	2		ns
tH_{TADR}	TADR[4:0] Hold time to TFCLK	0.5		ns
tS_{TENB}	TENB Set-up time to TFCLK	2		ns
tH_{TENB}	TENB Hold time to TFCLK	0.5		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	2		ns
tH_{TSOC}	TSOC Hold time to TFCLK	0.5		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	2		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	0.5		ns
tS_{TDAT}	TDAT[31:0] Set-up time to TFCLK	2		ns
tH_{TDAT}	TDAT[31:0] Hold time to TFCLK	0.5		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	2		ns
tP_{TCA}	TFCLK High to TCA Valid	1	6	ns

Figure 124 Transmit UTOPIA Level 3 System Interface Timing

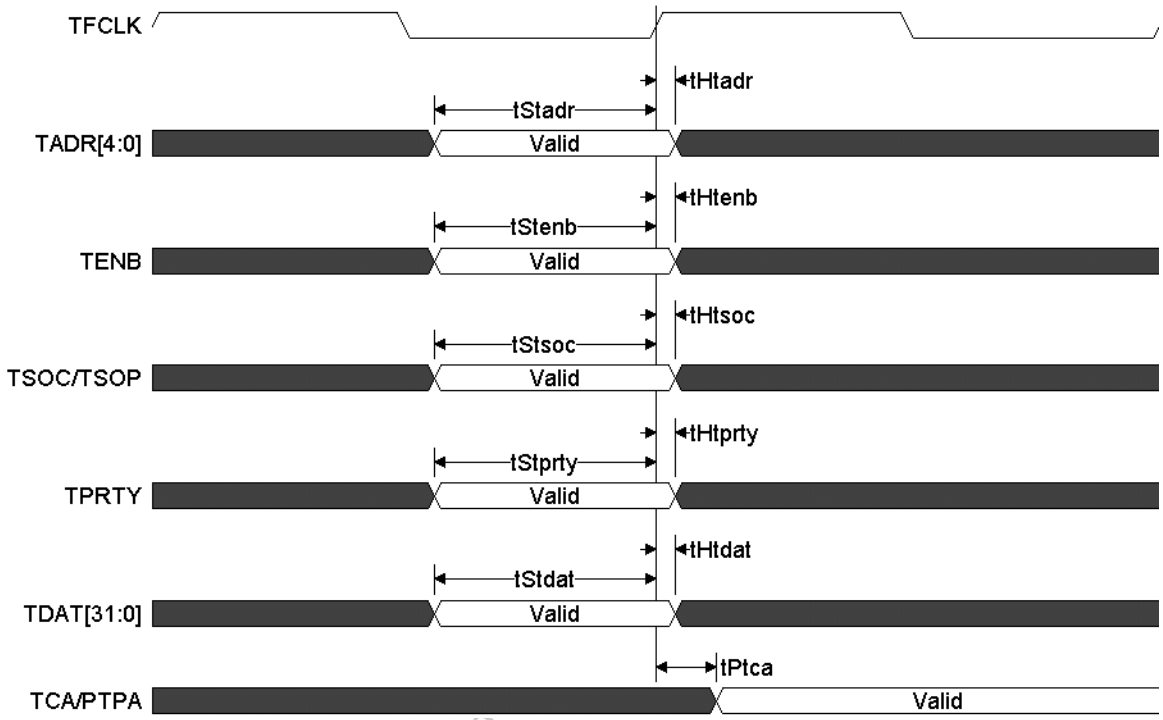
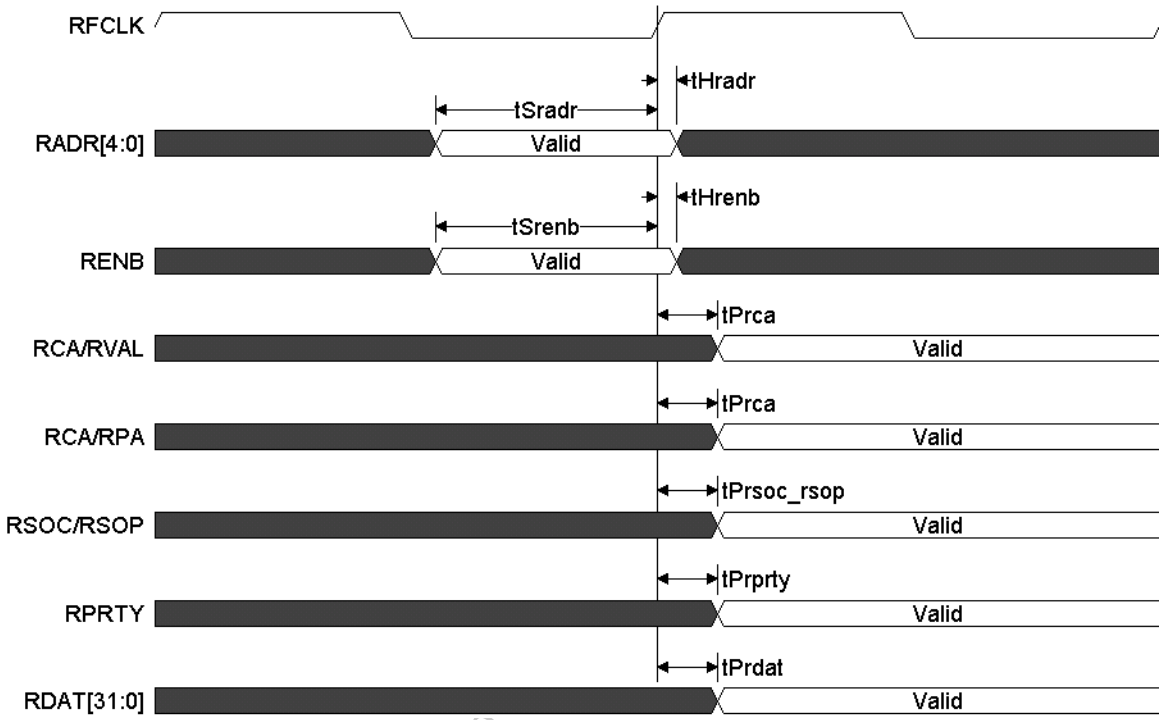


Table 55 Receive UTOPIA Level 3 System Interface Timing (Figure 125)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	60	104	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
J_{RFCLK}	RFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{RADR}	RADR[4:0] Set-up time to RFCLK	2		ns
tH_{RADR}	RADR[4:0] Hold time to RFCLK	0.5		ns
tS_{RENB}	RENB Set-up time to RFCLK	2		ns
tH_{RENB}	RENB Hold time to RFCLK	0.5		ns
tP_{RCA}	RFCLK High to RCA Valid	1	6	ns
tP_{RSOC}	RFCLK High to RSOC Valid	1	6	ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1	6	ns
tP_{RDAT}	RFCLK High to RDAT[31:0] Valid	1	6	ns

Figure 125 Receive UTOPIA Level 3 System Interface Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 30 pF load on the outputs.

19.5 POS Level 2 System Interface Timing

Table 56 Transmit POS-PHY Level 2 System Interface Timing (Figure 126)

Symbol	Description	Min	Max	Units
f_{TFCLK}	TFCLK Frequency	40	52	MHz
D_{TFCLK}	TFCLK Duty Cycle	40	60	%
J_{TFCLK}	TFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{TADR}	TADR[4:0] Set-up time to TFCLK	3		
tH_{TADR}	TADR[4:0] Hold time to TFCLK	0		
tS_{TENB}	TENB Set-up time to TFCLK	3		
tH_{TENB}	TENB Hold time to TFCLK	0		
tS_{TSOP}	TSOP Set-up time to TFCLK	3		ns
tH_{TSOP}	TSOP Hold time to TFCLK	0		ns
tS_{TEOP}	TEOP Set-up time to TFCLK	3		ns
tH_{TEOP}	TEOP Hold time to TFCLK	0		ns
tS_{TERR}	TERR Set-up time to TFCLK	3		ns
tH_{TERR}	TERR Hold time to TFCLK	0		ns
tS_{TMOD}	TMOD[0] Set-up time to TFCLK	3		ns
tH_{TMOD}	TMOD[0] Hold time to TFCLK	0		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	3		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	0		ns
tS_{TDAT}	TDAT[15:0] Set-up time to TFCLK	3		ns
tH_{TDAT}	TDAT[15:0] Hold time to TFCLK	0		ns
tP_{PTPA}	TFCLK High to PTPA Valid	1	10	ns
tP_{STPA}	TFCLK High to STPA Valid	1	10	ns

Figure 126 Transmit POS-PHY Level 2 System Interface Timing

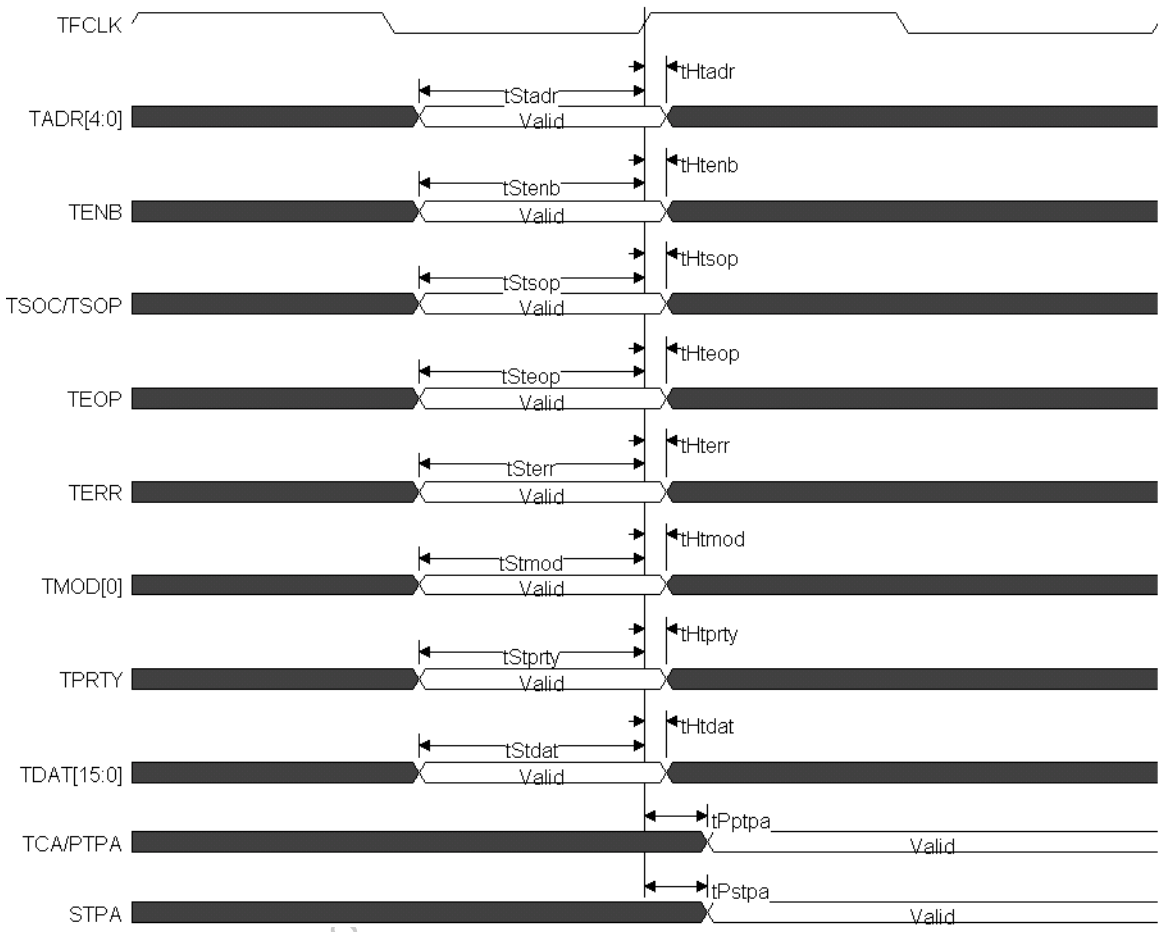
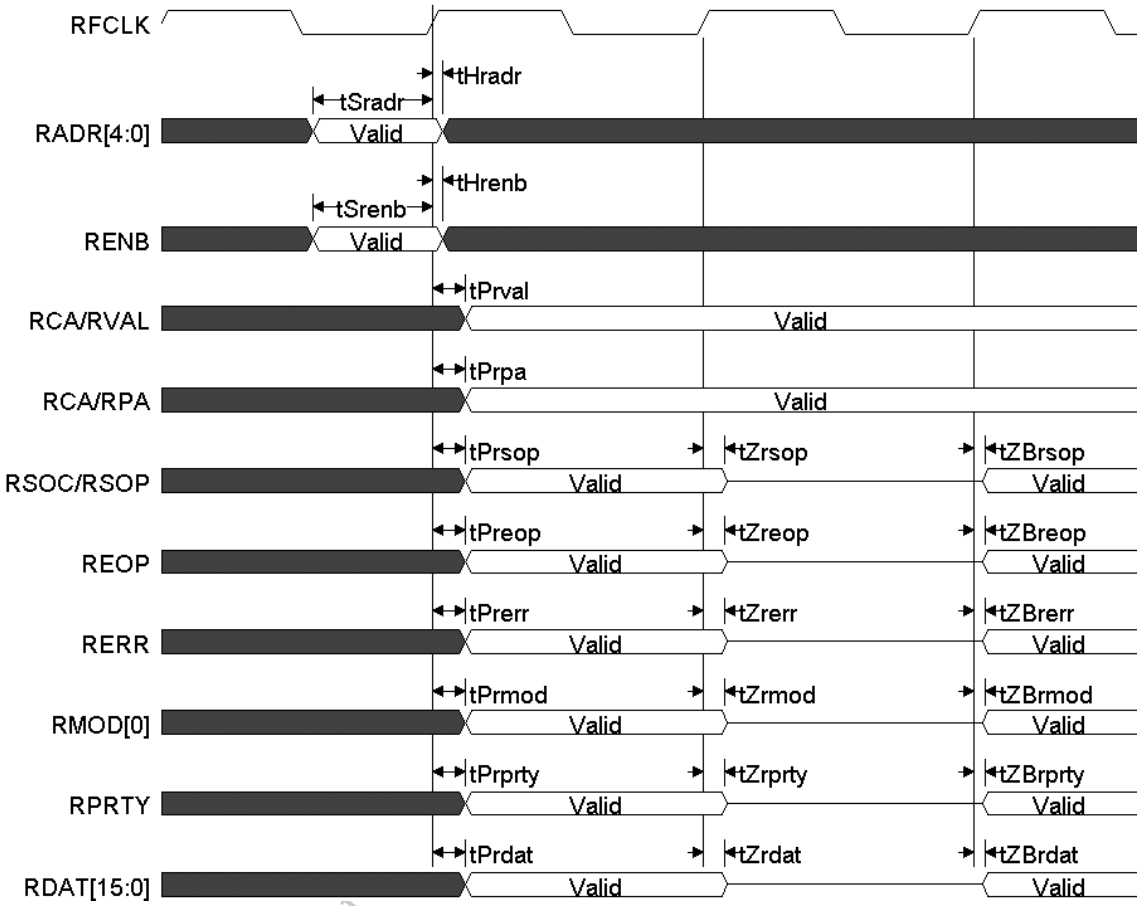


Table 57 Receive POS-PHY Level 2 System Interface Timing (Figure 127)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	40	52	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
J_{RFCLK}	RFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{RADR}	RADR[4:0] Set-up time to RFCLK	3		ns
tH_{RADR}	RADR[4:0] Hold time to RFCLK	0		ns
tS_{RENB}	RENB Set-up time to RFCLK	3		ns
tH_{RENB}	RENB Hold time to RFCLK	0		ns
tP_{RVAL}	RFCLK High to RVAL Valid	1	10	ns
tP_{RPA}	RFCLK High to RPA Valid	1	10	ns

Symbol	Description	Min	Max	Units
tP_{RSOP}	RFCLK High to RSOP Valid	1	10	ns
tZ_{RSOP}	RFCLK High to RSOP Tri-state	1	10	ns
tZB_{RSOP}	RFCLK High to RSOP Driven	0		ns
tP_{REOP}	RFCLK High to REOP Valid	1	10	ns
tZ_{REOP}	RFCLK High to REOP Tri-state	1	10	ns
tZB_{REOP}	RFCLK High to REOP Driven	0		ns
tP_{RERR}	RFCLK High to RERR Valid	1	10	ns
tZ_{RERR}	RFCLK High to RERR Tri-state	1	10	ns
tZB_{RERR}	RFCLK High to RERR Driven	0		ns
tP_{RMOD}	RFCLK High to RMOD[0] Valid	1	10	ns
tZ_{RMOD}	RFCLK High to RMOD[0] Tri-state	1	10	ns
tZB_{RMOD}	RFCLK High to RMOD[0] Driven	0		ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1	10	ns
tZ_{RPRTY}	RFCLK High to RPRTY Tri-state	1	10	ns
tZB_{RPRTY}	RFCLK High to RPRTY Driven	0		ns
tP_{RDAT}	RFCLK High to RDAT[15:0] Valid	1	10	ns
tZ_{RDAT}	RFCLK High to RDAT[15:0] Tri-state	1	10	ns
tZB_{RDAT}	RFCLK High to RDAT[15:0] Driven	0		ns

Figure 127 Receive POS-PHY Level 2 System Interface Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

19.6 POS Level 3 System Interface Timing

Table 58 Transmit POS-PHY Level 3 System Interface Timing (Figure 128)

Symbol	Description	Min	Max	Units
F_{TFCLK}	TFCLK Frequency	60	104	MHz
D_{TFCLK}	TFCLK Duty Cycle	40	60	%
J_{TFCLK}	TFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{TADR}	TADR[3:0] Set-up time to TFCLK	2.5		ns
tH_{TADR}	TADR[3:0] Hold time to TFCLK	0.5		ns
tS_{TENB}	TENB Set-up time to TFCLK	2.5		ns
tH_{TENB}	TENB Hold time to TFCLK	0.5		ns
tS_{TSX}	TSX Set-up time to TFCLK	2.5		ns
tH_{TSX}	TSX Hold time to TFCLK	0.5		ns
tS_{TSOP}	TSOP Set-up time to TFCLK	2.5		ns
tH_{TSOP}	TSOP Hold time to TFCLK	0.5		ns
tS_{TEOP}	TEOP Set-up time to TFCLK	2.5		ns
tH_{TEOP}	TEOP Hold time to TFCLK	0.5		ns
tS_{TERR}	TERR Set-up time to TFCLK	2.5		ns
tH_{TERR}	TERR Hold time to TFCLK	0.5		ns
tS_{TMOD}	TMOD[1:0] Set-up time to TFCLK	2.5		ns
tH_{TMOD}	TMOD[1:0] Hold time to TFCLK	0.5		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	2.5		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	0.5		ns
tS_{TDAT}	TDAT[31:0] Set-up time to TFCLK	2.5		ns
tH_{TDAT}	TDAT[31:0] Hold time to TFCLK	0.5		ns
tP_{PTPA}	TFCLK High to PTPA Valid	1.5	6	ns
tP_{STPA}	TFCLK High to STPA Valid	1.5	6	ns

Figure 128 Transmit POS-PHY Level 3 System Interface Timing

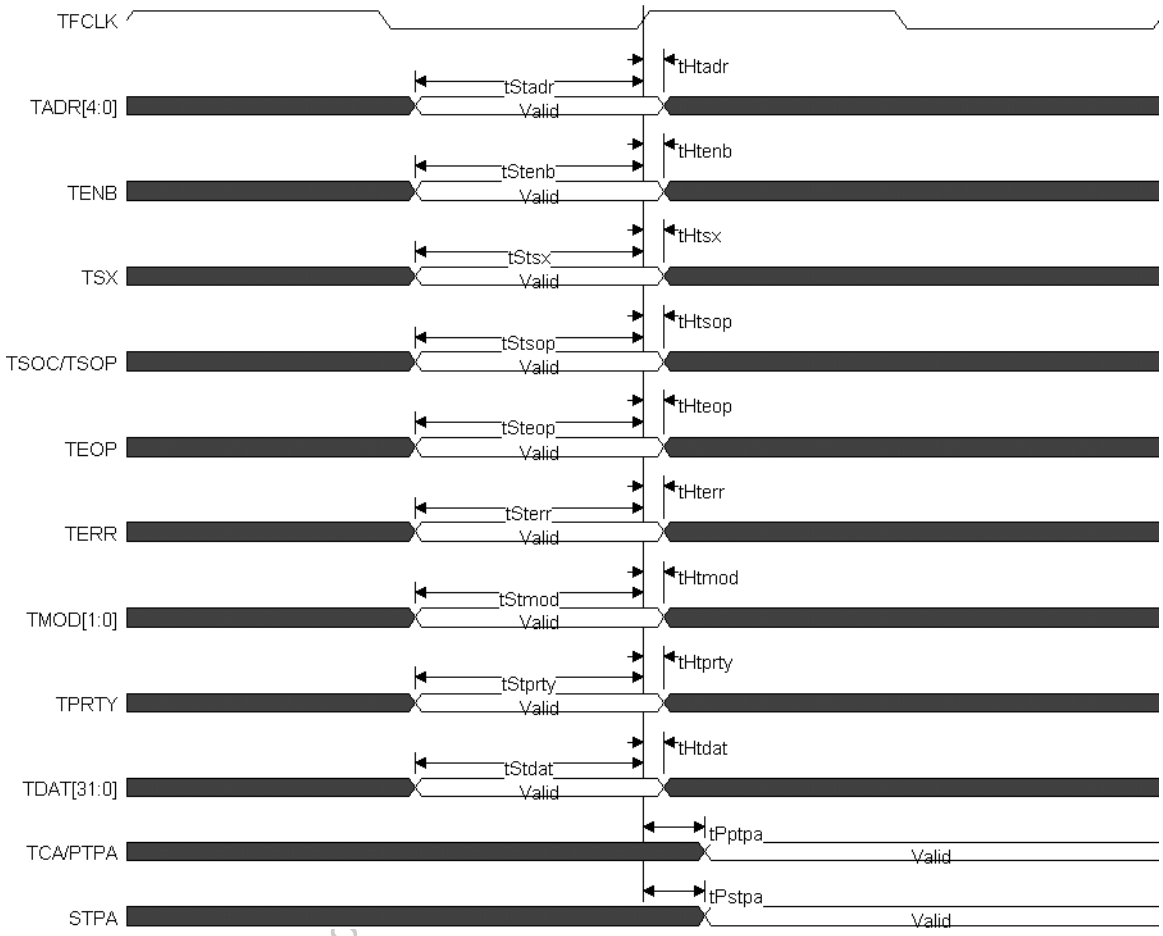
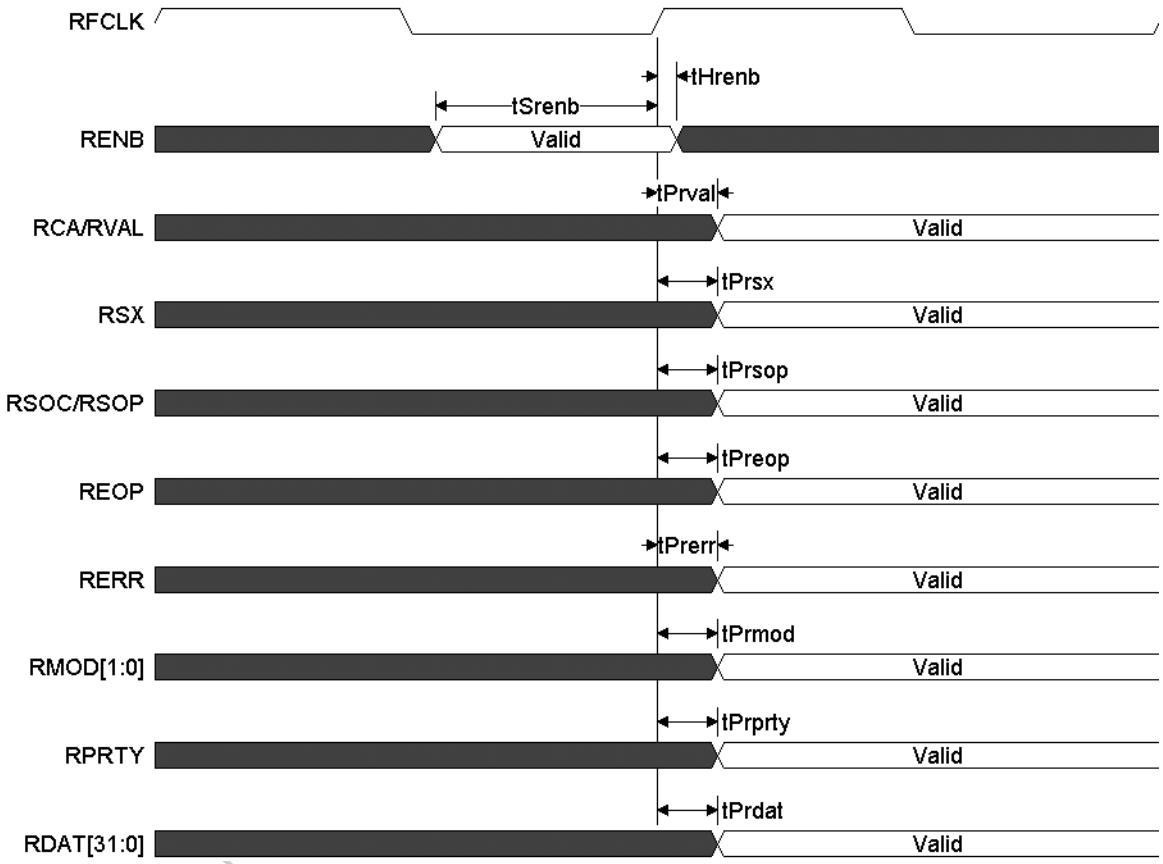


Table 59 Receive POS-PHY Level 3 System Interface Timing (Figure 129)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	60	104	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
J_{RFCLK}	RFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{RENB}	RENB Set-up time to RFCLK	2.5		ns
tH_{RENB}	RENB Hold time to RFCLK	0.5		ns
tP_{RVAL}	RFCLK High to RVAL Valid	1.5	6	ns
tP_{RSX}	RFCLK High to RSX Valid	1.5	6	ns
tP_{RSOP}	RFCLK High to RSOP Valid	1.5	6	ns
tP_{REOP}	RFCLK High to REOP Valid	1.5	6	ns
tP_{RERR}	RFCLK High to RERR Valid	1.5	6	ns

Symbol	Description	Min	Max	Units
tP_{RMOD}	RFCLK High to RMOD[1:0] Valid	1.5	6	ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1.5	6	ns
tP_{RDAT}	RFCLK High to RDAT[31:0] Valid	1.5	6	ns

Figure 129 Receive POS-PHY Level 3 System Interface Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum and minimum output propagation delays are measured with a 30 pF load on the outputs.

19.7 TelecomBus Interface Timing

Table 60 Transmit TelecomBus Interface (Figure 130)

Symbol	Description	Min	Typical	Max	Units
Foclk	OCLK Frequency	77.76	77.76	77.76	MHz
Doclk	OCLK Duty Cycle	40	50	60	%
tSoj0ref	OJ0REF Setup time to OCLK	2.5			ns
tHoj0ref	OJ0REF Hold time to OCLK	0			ns
tPod	OCLK to OD[7:0] Valid	1		5	ns
tPodp	OCLK to ODP Valid	1		5	ns
tPopl	OCLK to OPL Valid	1		5	ns
tPoj0j1	OCLK to OJ0J1 Valid	1		5	ns
tPoalarm	OCLK to OALARM Valid	1		5	ns
tPostsen	OCLK to OSTSEN Valid	1		5	ns

Figure 130 Transmit TelecomBus Interface Timing

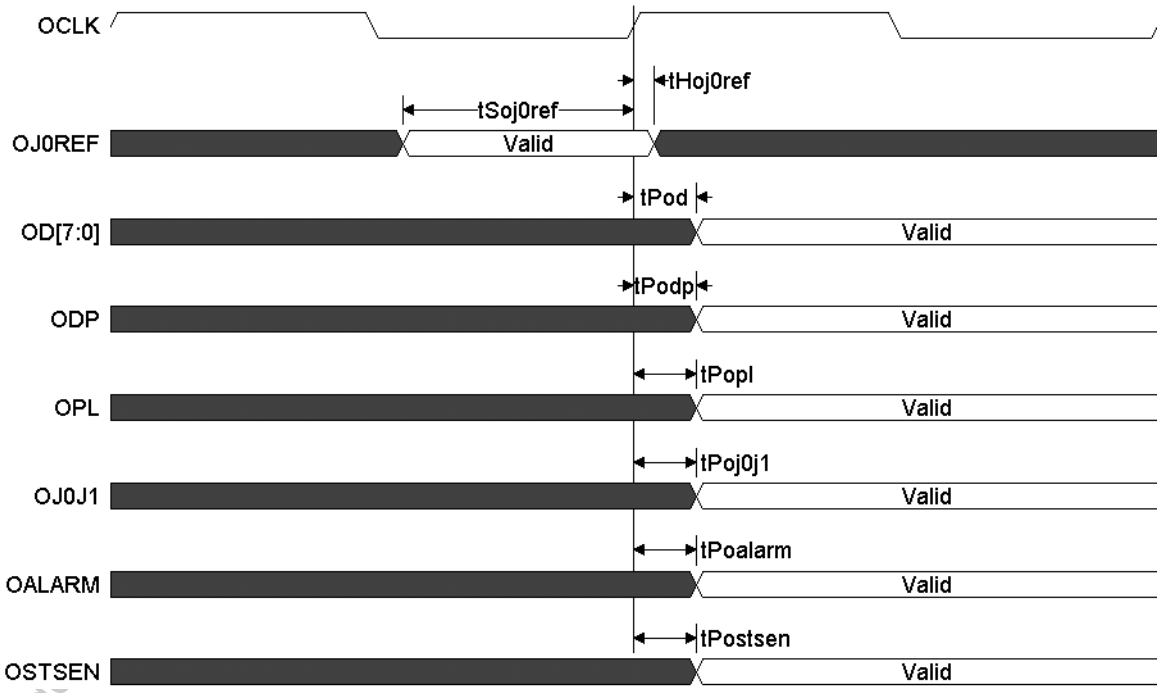
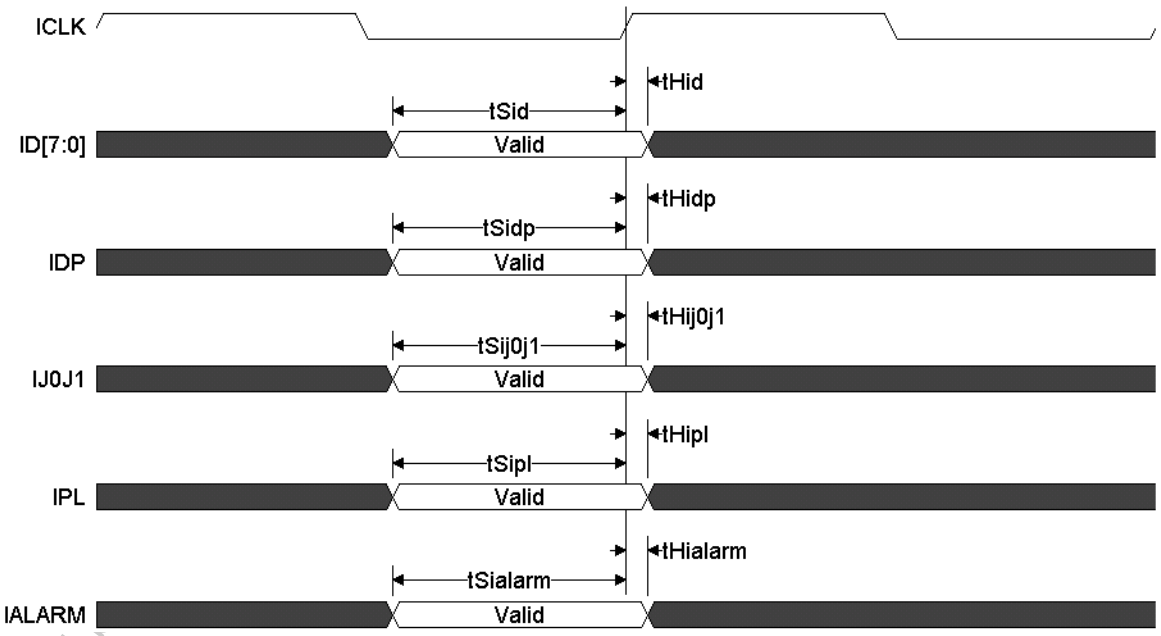


Table 61 Receive TelecomBus Interface (Figure 131)

Symbol	Description	Min	Typical	Max	Units
Ficlk	ICLK Frequency	77.76	77.76	77.76	MHz
Diclk	ICLK Duty Cycle	40	50	60	%
tSid	ID[7:0] Setup time to ICLK	2.5			ns
tHid	ID[7:0] Hold time to ICLK	0			ns
tSidp	IDP Setup time to ICLK	2.5			ns
tHidp	IDP Hold time to ICLK	0			ns
tSij0j1	IJ0J1 Setup time to ICLK	2.5			ns
tHij0j1	IJ0J1 Hold time to ICLK	0			ns
tSipl	IPL Setup time to ICLK	2.5			ns
tHipl	IPL Hold time to ICLK	0			ns
tSialarm	IALARM Setup time to ICLK	2.5			ns
tHialarm	IALARM Hold time to ICLK	0			ns

Figure 131 Receive TelecomBus Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.

4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

19.8 SERDES Interface Timing

Table 62 Transmit SERDES Interface (Figure 132)

Symbol	Description	Min	Typical	Max	Units
Fptclk	PTCLK Frequency	77.76	77.76	77.76	MHz
Dptclk	PTCLK Duty Cycle	40	50	60	%
tStsfpi	TSFPI Setup time to PTCLK	2.5			ns
tHtsfpi	TSFPI Hold time to PTCLK	0			ns
tPpout	PTCLK to POUT[7:0] Valid	1		7	ns
tPtsfpo	PTCLK to TSFPO Valid	1		7	ns

Figure 132 Transmit SERDES Interface Timing

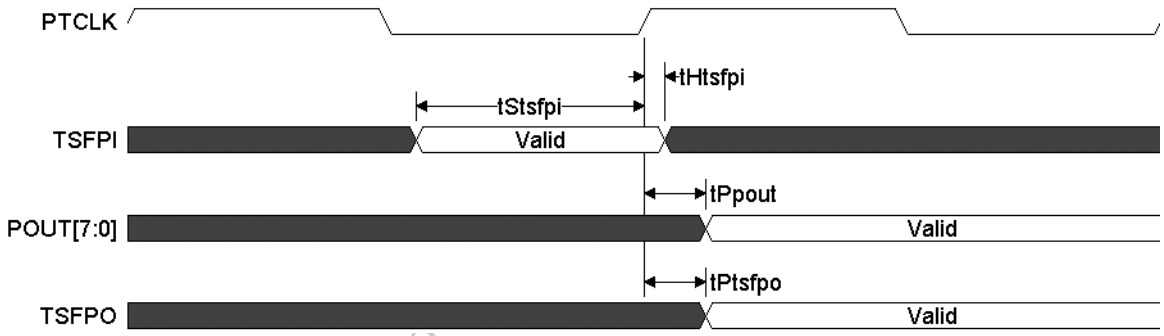
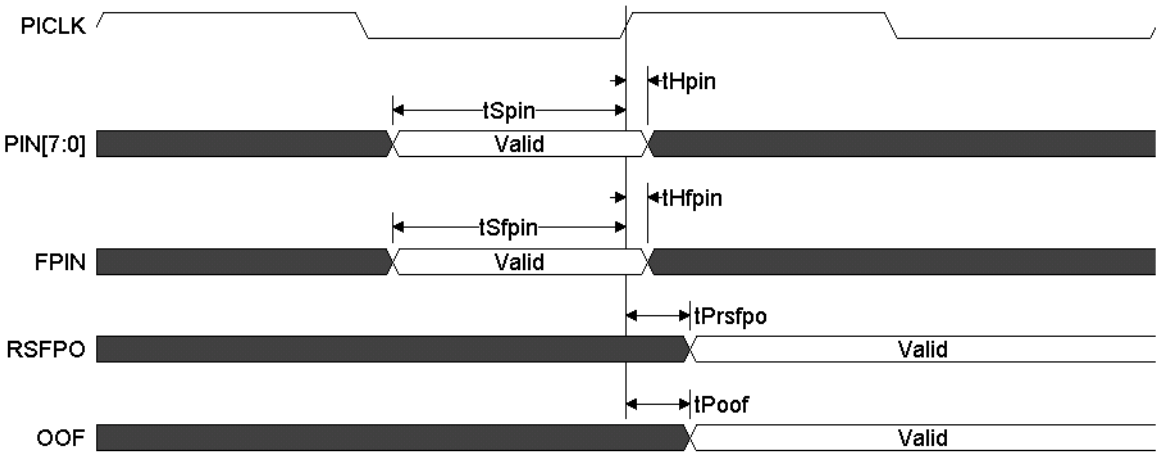


Table 63 Receive SERDES Interface (Figure 133)

Symbol	Description	Min	Typical	Max	Units
Fpiclk	PICLK Frequency	77.76	77.76	77.76	ns
Dpiclk	PICLK Duty Cycle	40	50	60	%
tSpin	PIN[7:0] Setup time to PICLK	2.5			ns
tHpin	PIN[7:0] Hold time to PICLK	0			ns
tSfpin	FPIN Setup time to PICLK	2.5			ns
tHfpin	FPIN Hold time to PICLK	0			ns
tPrsfpo	PICLK to RSFPO Valid	1		7	ns
tPoof	PICLK to OOF Valid	1		7	

Figure 133 Receive SERDES Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

19.9 SONET/SDH Overhead Interface Timing

Table 64 Transmit SONET/SDH Overhead TOHCLK Interface (Figure 134)

Symbol	Description	Min	Typical	Max	Units
tSttoh	TTOH Setup time to TOHCLK rising edge	14			ns
tHttoh	TTOH Hold time to TOHCLK rising edge	0			ns
tSttohen	TTOHEN Setup time to TOHCLK rising edge	14			ns
tHttohen	TTOHEN Hold time to TOHCLK rising edge	0			ns
tStpoh	TPOH Setup time to TOHCLK rising edge	14			ns
tHtpoh	TPOH Hold time to TOHCLK rising edge	0			ns
tPtohfp	TOHCLK falling edge to TOHFP Valid	-7		7	ns
tPtpohen	TOHCLK falling edge to TPOHEN Valid	-7		7	ns
tPtpohrdy	TOHCLK falling edge to TPOHRDY Valid	-7		7	ns

Figure 134 Transmit SONET/SDH Overhead Interface Timing

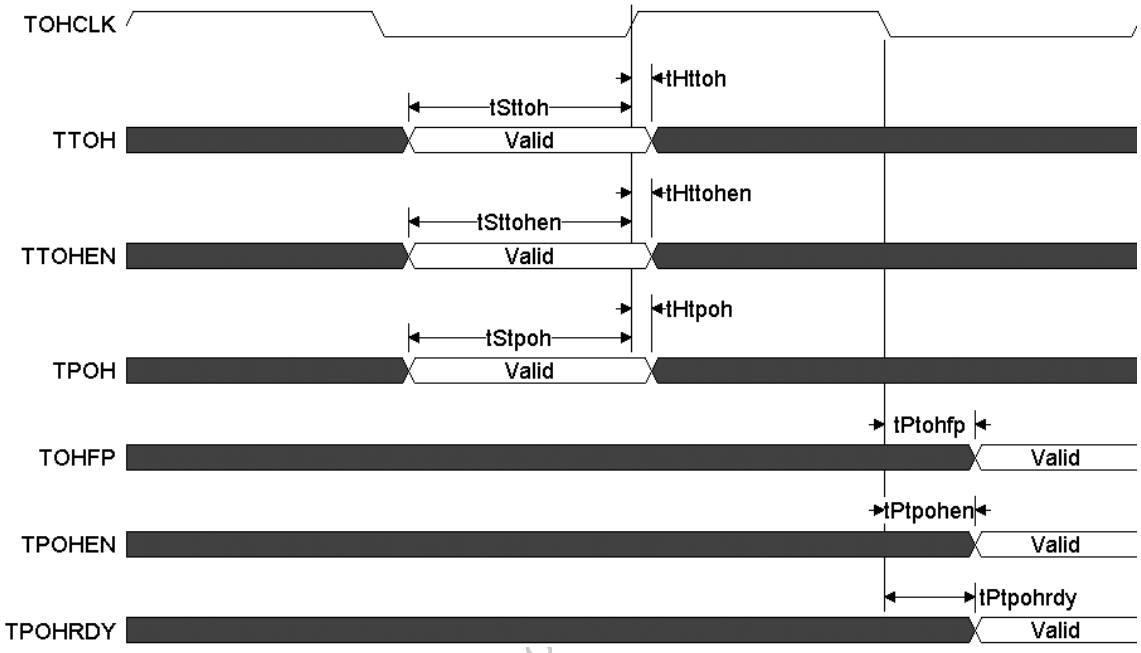


Table 65 Transmit SONET/SDH Overhead TSLDCLK Interface (Figure 135)

Symbol	Description	Min	Typical	Max	Units
tStsld	TSLD Setup time to TSLDCLK rising edge	14			ns
tHtsld	TSLD Hold time to TSLDCLK rising edge	0			ns

Figure 135 Transmit SONET/SDH Overhead Interface Timing

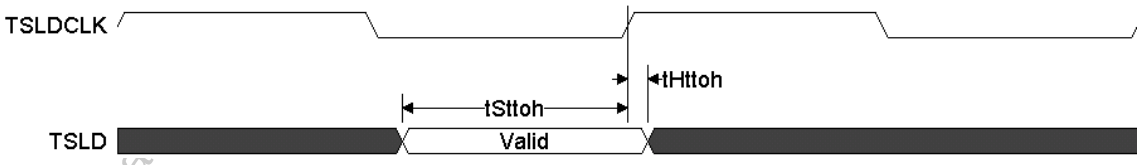


Table 66 Receive SONET/SDH Overhead ROHCLK Interface (Figure 136)

Symbol	Description	Min	Typical	Max	Units
tProhfp	ROHCLK falling edge to ROHFP Valid	-7		7	ns
tPrtoh	ROHCLK falling edge to RTOH Valid	-7		7	ns
tPrpoh	ROHCLK falling edge to RPOH Valid	-7		7	ns
tPrpohen	ROHCLK falling edge to RPOHEN Valid	-7		7	ns

Symbol	Description	Min	Typical	Max	Units
tPsalm	ROHCLK falling edge to SALM Valid	-7		7	ns
tPralm	ROHCLK falling edge to RALM Valid	-7		7	ns
tPb3e	ROHCLK falling edge to B3E Valid	-7		7	ns

Figure 136 Receive SONET/SDH Overhead ROHCLK Interface Timing

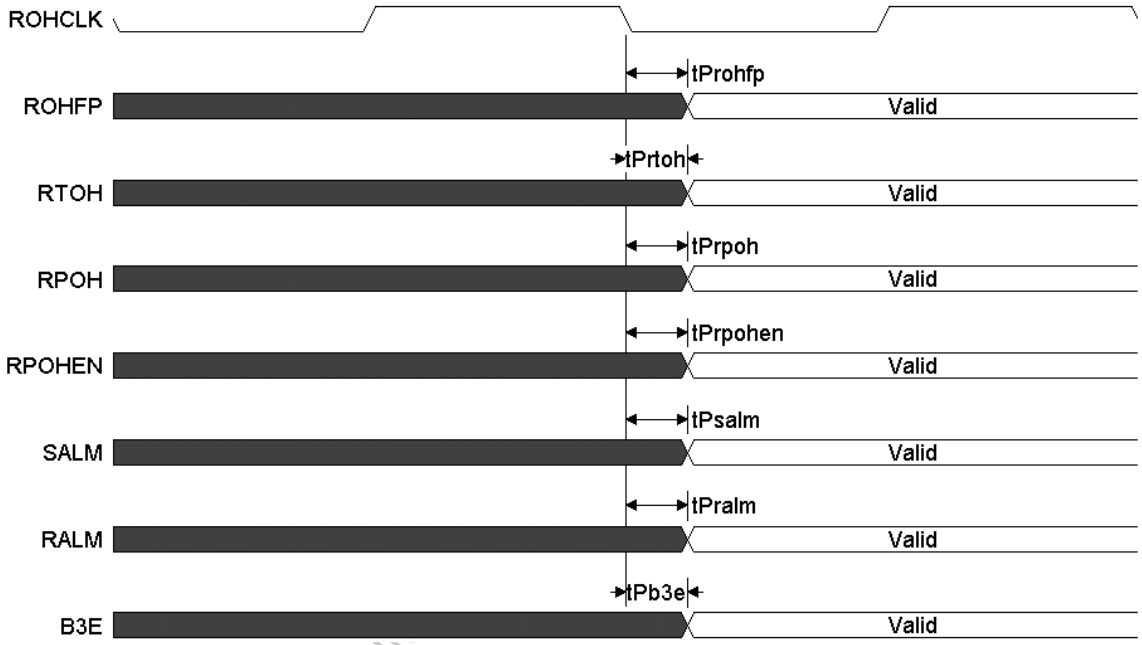
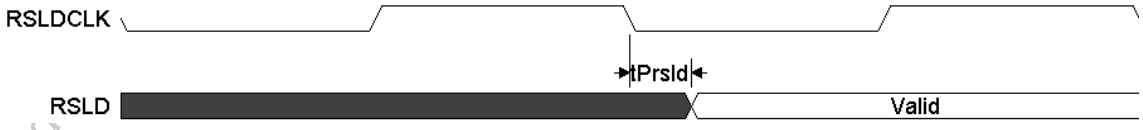


Table 67 Receive SONET/SDH Overhead RSLDCLK Interface (Figure 137)

Symbol	Description	Min	Typical	Max	Units
tPrsld	RSLDCLK falling edge to RSLD Valid	-7		7	ns

Figure 137 Receive SONET/SDH Overhead RSLDCLK Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

19.10 Serial Interface Timing

Table 68 Transmit Serial Interface (Figure 138)

Symbol	Description	Min	Typical	Max	Units
Ftclk	TCLK[n] Frequency (DS3 Operation)		44.736		ns
Ftclk	TCLK[n] Frequency (E3 Operation)		34.368		ns
Dtclk	TCLK[n] Duty Cycle	40	50	60	%
tPtpos	TCLK[n] to TPOS/TDATO[n] Valid	1		10	ns
tPtneg	TCLK[n] to TNEG/TOHM[n] Valid	1		10	ns

Figure 138 Transmit Serial Interface Timing

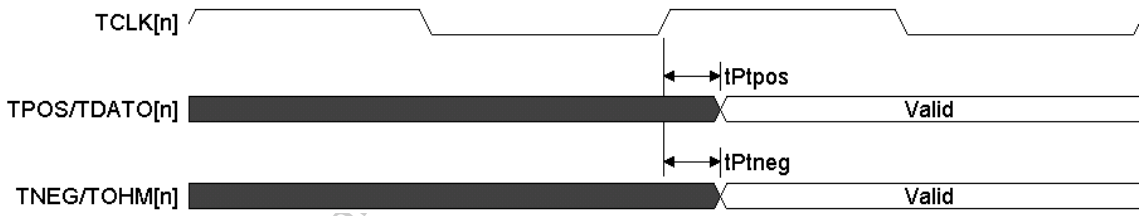
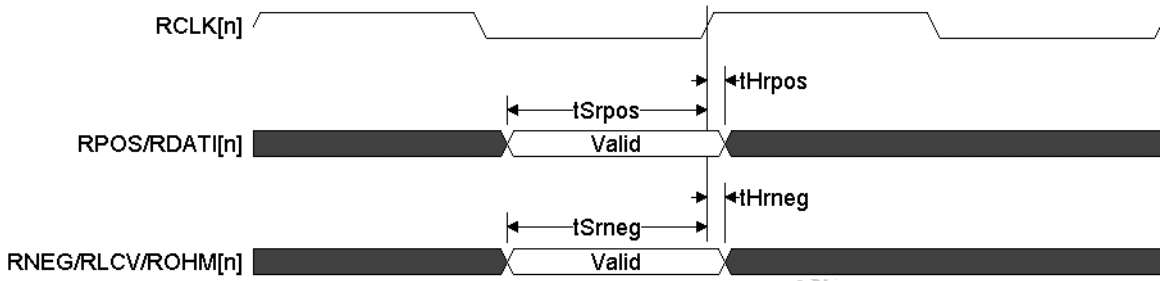


Table 69 Receive Serial Interface (Figure 139)

Symbol	Description	Min	Typical	Max	Units
Frclk	RCLK[n] Frequency (DS3 Operation)		44.736		ns
Frclk	RCLK[n] Frequency (E3 Operation)		34.368		ns
Drclk	RCLK[n] Duty Cycle	40	50	60	%
tSrpos	RPOS/RDATI[n] Setup time to RCLK[n]	3			ns
tHrpos	RPOS/RDATI[n] Hold time to RCLK[n]	1			ns
tSrneg	RNEG/RLCV/ROHMI[n] Setup time to RCLK[n]	3			ns
tHrneg	RNEG/RLCV/ROHMI[n] Hold time to RCLK[n]	1			ns

Figure 139 Receive Serial Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

19.11 DS3/E3 Serial Interface Timing Characteristics

Intrinsic/Mapping Jitter is defined as the sum of the intrinsic payload mapping jitter and the jitter that is generated as a result of the asynchronous mapping. Intrinsic/Mapping Jitter is measured in the absence of pointer movements and input jitter.

Pointer Jitter is defined as the jitter measured due to pointer movements in the SONET/SDH network. Pointer jitter is measured as per ANSI T1.105.3b, ITU G.783, and GR-253 CORE.

Input jitter tolerance is defined as the maximum amplitude sinusoidal jitter that the S/UNI-12xJET can tolerate without error while mapping the DS3/E3 stream into SONET.

Intrinsic/Mapping Wander is defined as the sum of the wander generation of the clocks and the wander that is generated as a result from asynchronous mapping. Intrinsic/Mapping wander is measured in the absence of pointer movements, wander on synchronizing signals, input jitter, and input wander.

Pointer Wander is defined as the wander measured due to pointer movements in the SONET/SDH network. Pointer wander is measured as per ANSI T1.105.3b, ITU G.783, and GR-253 CORE.

Table 70 DS3 Serial Interface Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
JGds3	Peak to peak Intrinsic Jitter in DS3 mode. 10Hz – 400kHz 30kHz – 400kHz		 TBD TBD	 TBD TBD	UIpp
JPds3	Peak to Peak Pointer Jitter in DS3 Mode All 10Hz – 400kHz (unless otherwise specified)				
	Single Pointer Adjustment		TBD	TBD	UIpp
	Burst of 3 Pointer Adjustments		TBD	TBD	UIpp
	Phase Transient Pointer Adjustment Burst		TBD	TBD	UIpp
	Periodic Pointer Adjustments no Add/Cancel		TBD	TBD	UIpp
	Periodic Pointer Adjustments with Add		TBD	TBD	UIpp
	Periodic Pointer Adjustments with Cancel		TBD	TBD	UIpp
JTds3	Peak to peak Jitter Tolerance in DS3 mode.	See Figure 140			
WGds3	MTIE Mapping Wander in DS3 Mode	See Figure 141			
WPds3	MTIE Pointer Wander in DS3 Mode				
	Single Pointer Adjustment	See Figure 142			
	Burst of 3 Pointer Adjustments	See Figure 143			
	Phase Transient Pointer Adjustment Burst	See Figure 144			
	Periodic Pointer Adjustments no Add/Cancel	See Figure 145			
	Periodic Pointer Adjustments with Add	See Figure 146			
	Periodic Pointer Adjustments with Cancel	See Figure 147			

Notes :

1. Typical Pointer Jitter is measured with time constant T = TBD, unless otherwise specified.
2. Maximum Pointer Jitter is measured with a time constant 34ms < T < 1s.
3. Pointer Wander is measured with time constant T = TBD, unless otherwise specified.

Figure 140 DS3 Jitter Tolerance

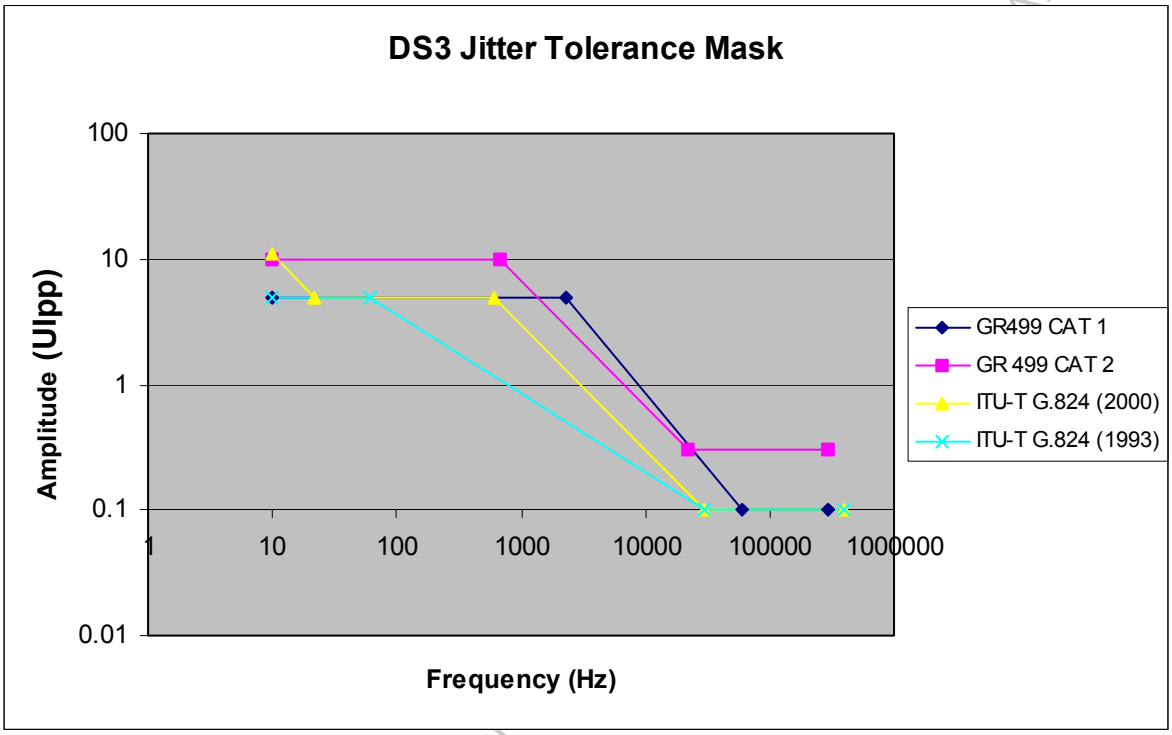


Figure 141 DS3 Mapping Wander MTIE

TBD

Figure 142 DS3 Pointer Wander MTIE (Single Pointer Adjustment)

TBD

Figure 143 DS3 Pointer Wander MTIE (Burst of 3 Pointer Adjustments)

TBD

Figure 144 DS3 Pointer Wander MTIE (Phase Transient Pointer Adjustment Burst)

TBD

Figure 145 DS3 Pointer Wander MTIE (Periodic Pointer Adjustments no Add/Cancel)

TBD

Figure 146 DS3 Pointer Wander MTIE (Periodic Pointer Adjustments with Add)

TBD

Figure 147 DS3 Pointer Wander MTIE (Periodic Pointer Adjustments with Cancel)

TBD

Table 71 E3 Serial Interface Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
JGds3	Peak to peak Intrinsic Jitter in E3 mode. 100Hz – 800kHz 10kHz – 800kHz		 TBD TBD	 TBD TBD	UIpp
JPds3	Peak to Peak Pointer Jitter in E3 Mode				
	Single pointers of opposite polarity 100Hz – 800kHz 10kHz – 800kHz		 TBD TBD	 TBD TBD	UIpp
	Regular Pointers plus one double pointer 100Hz – 800kHz 10kHz – 800kHz		 TBD TBD	 TBD TBD	UIpp
	Regular Pointers with one missing pointer 100Hz – 800kHz 10kHz – 800kHz		 TBD TBD	 TBD TBD	UIpp
	Double pointers of opposite polarity 100Hz – 800kHz		 TBD	 TBD	UIpp
JTds3	Peak to peak Jitter Tolerance in E3 mode.	See Figure 148			
WGds3	MTIE Mapping Wander in E3 Mode	See Figure 149			
WPds3	MTIE Pointer Wander in E3 Mode				
	Single pointers of opposite polarity	See Figure 150			
	Regular Pointers plus one double pointer	See Figure 151			
	Regular Pointers with one missing pointer	See Figure 152			
	Double pointers of opposite polarity	See Figure 153			

Note :

1. Typical Pointer Jitter is measured with time constant T = TBD, unless otherwise specified.
2. Maximum Pointer Jitter is measured with a time constant T = TBD, unless otherwise specified.
3. Pointer Wander is measured with time constant T = TBD, unless otherwise specified.

Figure 148 E3 Jitter Tolerance

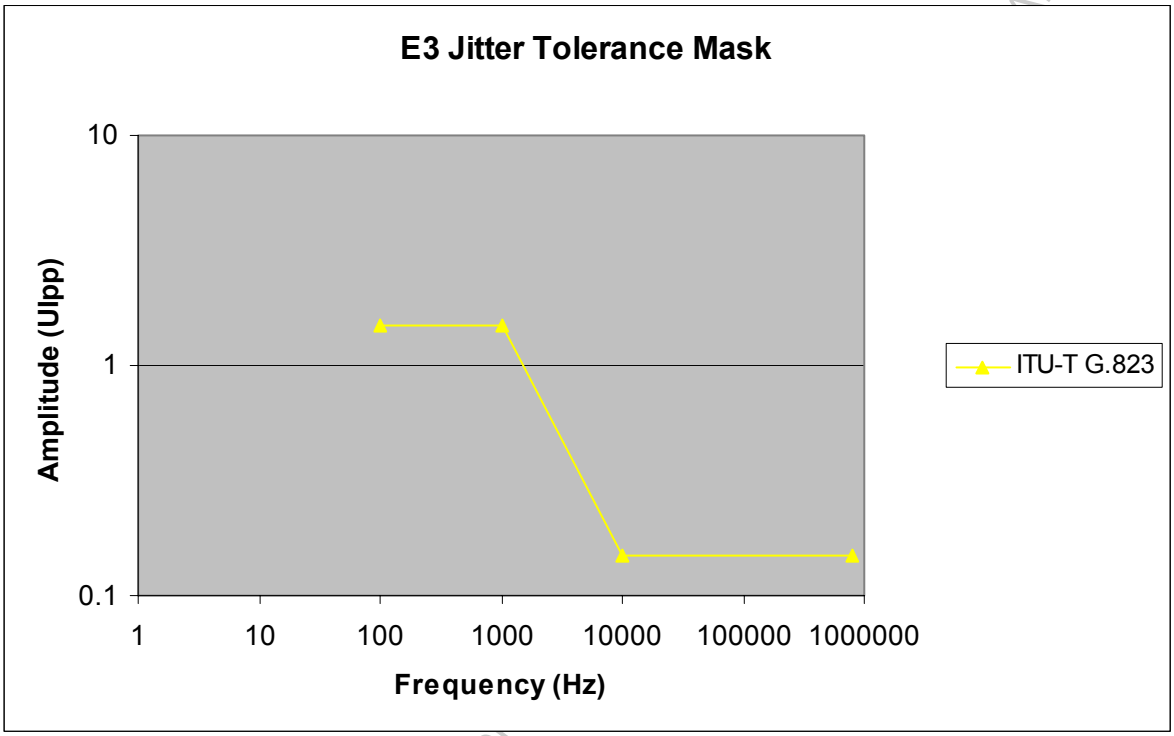


Figure 149 E3 Mapping Wander MTIE

TBD

Figure 150 E3 Pointer Wander MTIE (Single Pointers of opposite polarity)

TBD

Figure 151 E3 Pointer Wander MTIE (Regular Pointers plus one double pointer)

TBD

Figure 152 E3 Pointer Wander MTIE (Regular Pointers with one missing pointer)

TBD

Figure 153 E3 Pointer Wander MTIE (Double pointers of opposite polarity)

TBD

19.12 Auxiliary Serial Interface Timing

Table 72 Transmit Auxiliary Serial Interface (Figure 154)

Symbol	Description	Min	Typical	Max	Units
Fticlk	TICLK[n] Frequency		44.736	52	ns
Dticlk	TICLK[n] Duty Cycle	40	50	60	%
tStdati	TDATI[n] Setup time to TICLK[n]	3			ns
tHtdati	TDATI[n] Hold time to TICLK[n]	1			ns
tStioh	TIOH/TFPI/TMFPI[n] Setup time to TICLK[n]	3			ns
tHtioh	TIOH/TFPI/TMFPI[n] Hold time to TICLK[n]	1			ns
tPtfpo	TICLK[n] to TFPO/TMFPO[n] Valid	1		10	ns

Figure 154 Transmit Auxiliary Serial Interface Timing

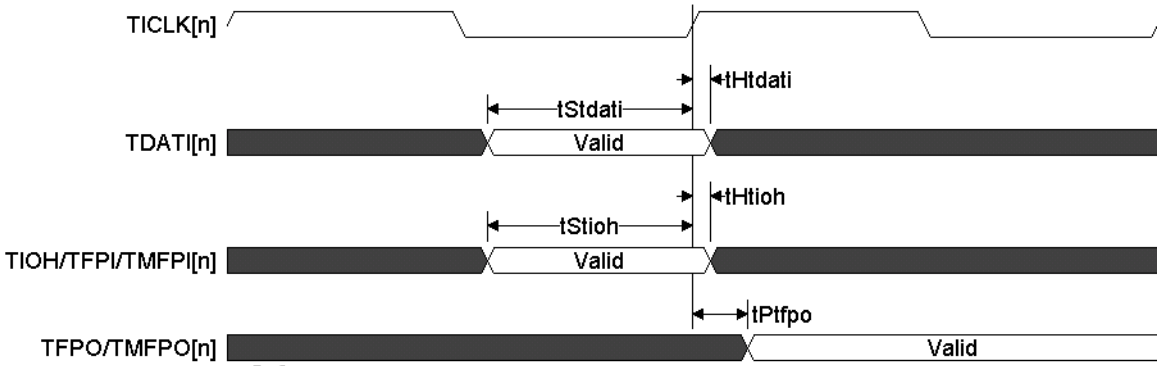
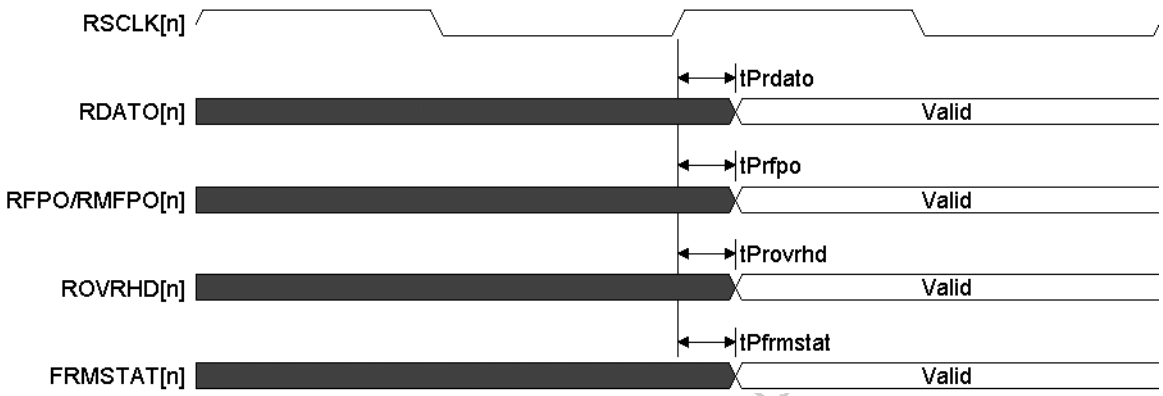


Table 73 Receive Auxiliary Serial Interface (Figure 155)

Symbol	Description	Min	Typical	Max	Units
Frsclk	RSCLK[n] Frequency		44.736	52	ns
Drsclk	RSCLK[n] Duty Cycle	40	50	60	%
tPrdato	RSCLK[n] to RDATO[n] Valid	1		10	ns
tPrfpo	RSCLK[n] to RFPO/RMFPO[n] Valid	1		10	ns
tProvrhd	RSCLK[n] to ROVRHD[n] Valid	1		10	ns
tPfrmstat	RSCLK[n] to FRMSTAT[n] Valid	1		10	ns

Figure 155 Receive Auxiliary Serial Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

19.13 Flexible Bandwidth Interface Timing

Table 74 Egress Flexible Bandwidth Interface (Figure 156)

Symbol	Description	Min	Typical	Max	Units
Fefbwclk	EFBWCLK[n] Frequency		44.736	52	ns
Defbwclk	EFBWCLK[n] Duty Cycle	40	50	60	%
tSefbwdreq	EFBWDREQ[n] Setup time to EFBWCLK[n]	3			ns
tHefbwdreq	EFBWDREQ[n] Hold time to EFBWCLK[n]	1			ns
tPefbwdat	EFBWCLK[n] to EFBWDAT[n] Valid	1		10	ns
tPefbwen	EFBWCLK[n] to EFBWEN[n] Valid	1		10	ns

Figure 156 Egress Flexible Bandwidth Interface Timing

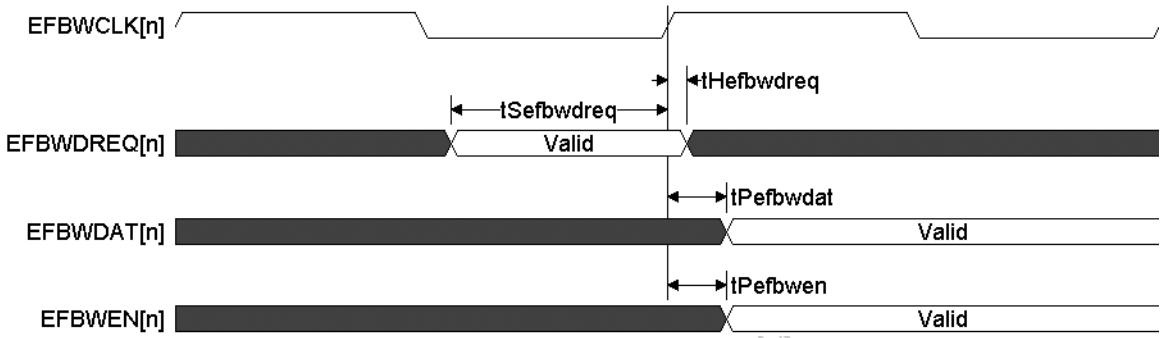
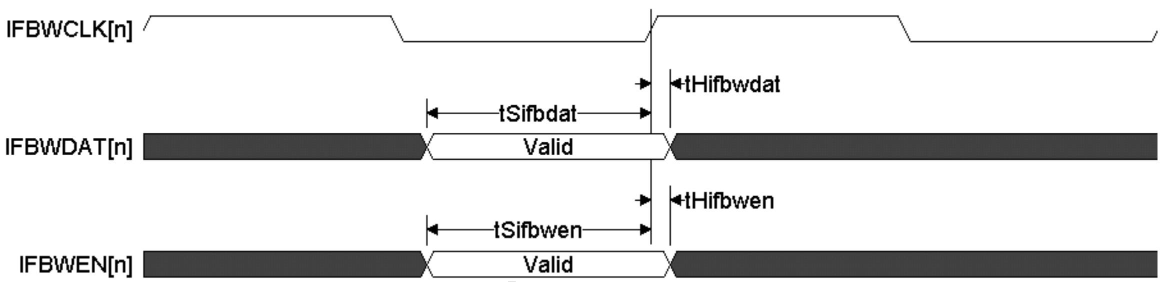


Table 75 Ingress Flexible Bandwidth Interface (Figure 157)

Symbol	Description	Min	Typical	Max	Units
Fifbwclk	IFBWCLK[n] Frequency		44.736	52	ns
Difbwclk	IFBWCLK[n] Duty Cycle	40	50	60	%
tSifbwdat	IFBWDAT[n] Setup time to IFBWCLK[n]	3			ns
tHifbwdat	IFBWDAT[n] Hold time to IFBWCLK[n]	1			ns
tSifbwen	IFBWEN[n] Setup time to IFBWCLK[n]	3			ns
tHifbwen	IFBWEN[n] Hold time to IFBWCLK[n]	1			ns

Figure 157 Ingress Flexible Bandwidth Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

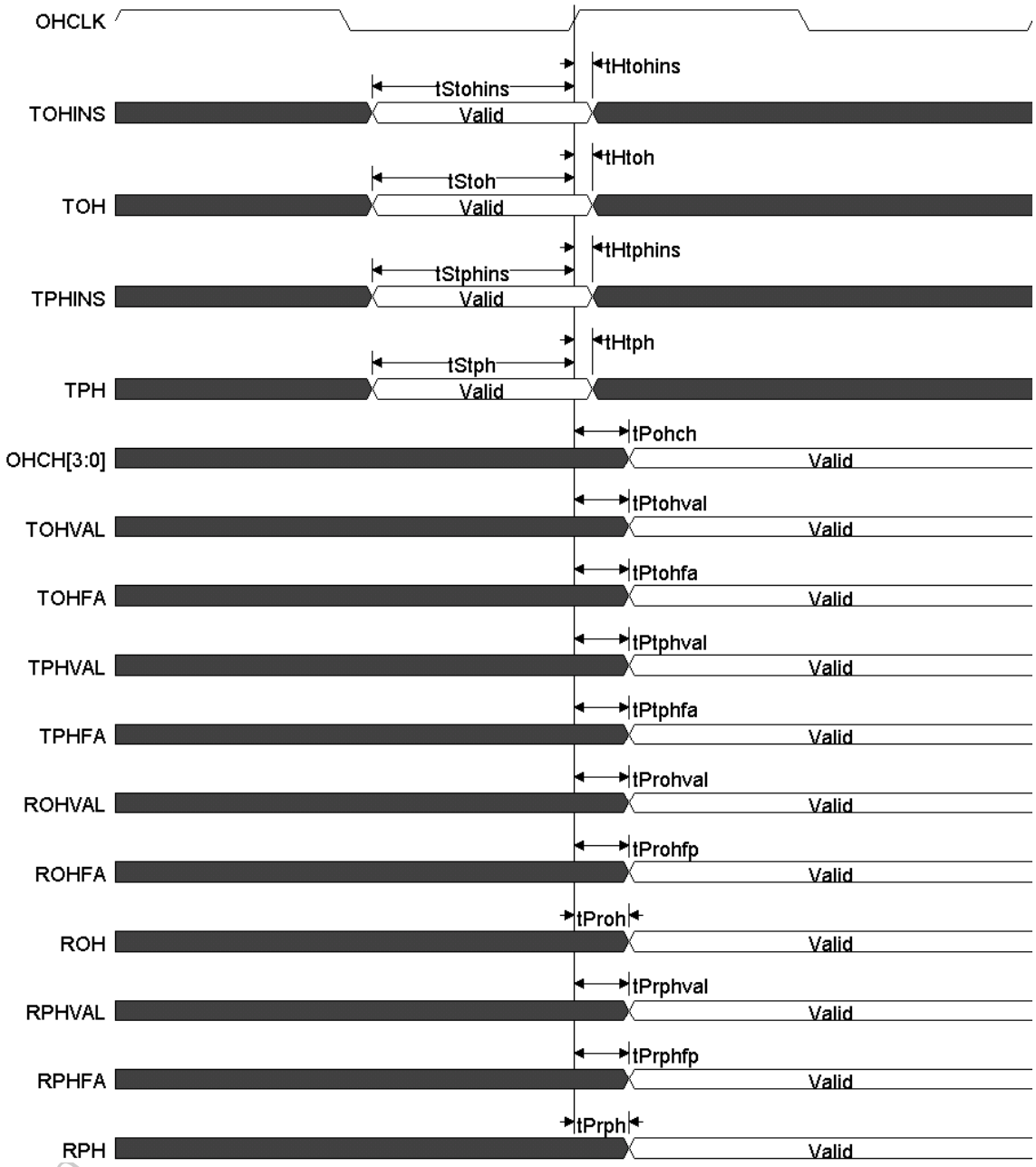
19.14 DS3 & E3 Overhead Interface Timing

Table 76 DS3 & E3 Overhead Insertion & Extraction Interface (Figure 158)

Symbol	Description	Min	Typical	Max	Units
tStohins	TOHINS Setup time to OHCLK	2.5			ns
tHtohins	TOHINS Hold time to OHCLK	0			ns
tStoh	TOH Setup time to OHCLK	2.5			ns
tHtoh	TOH Hold time to OHCLK	0			ns

Symbol	Description	Min	Typical	Max	Units
tStphins	TPHINS Setup time to OHCLK	2.5			ns
tHtphins	TPHINS Hold time to OHCLK	0			ns
tStph	TPH Setup time to OHCLK	2.5			ns
tHtph	TPH Hold time to OHCLK	0			ns
tPohch	OHCLK to OHCH[3:0] Valid	1		8	ns
tPtohval	OHCLK to TOHVAL Valid	1		8	ns
tPtohfa	OHCLK to TOHFA Valid	1		8	ns
tPtphval	OHCLK to TPHVAL Valid	1		8	ns
tPtphfa	OHCLK to TPHFA Valid	1		8	ns
tProhval	OHCLK to ROHVAL Valid	1		8	ns
tProhfa	OHCLK to ROHFA Valid	1		8	ns
tProh	OHCLK to ROH Valid	1		8	ns
tPrphval	OHCLK to RPHVAL Valid	1		8	ns
tPrphfa	OHCLK to RPHFA Valid	1		8	ns
tPrph	OHCLK to RPH Valid	1		8	ns

Figure 158 DS3 & E3 Overhead Insertion & Extraction Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.

4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

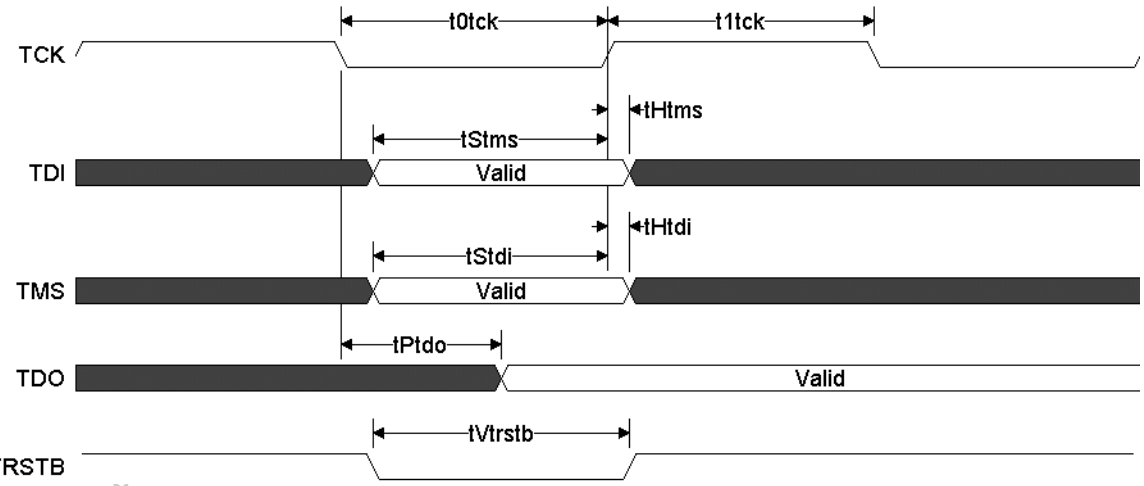
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

19.15 JTAG Interface Timing

Table 77 JTAG Port Interface (Figure 159)

Symbol	Description	Min	Typical	Max	Units
$t1_{TCK}$	TCK high pulse width[5]				ns
$t0_{TCK}$	TCK low pulse width[5]	100			ns
tS_{TMS}, tS_{TDI}	TMS and TDI Set-up time to TCK[1]	50			ns
TH_{TMS}, TH_{TDI}	TMS and TDI Hold time to TCK[2]	50			ns
TP_{TDO}	TCK Low to TDO Valid[6,7]	2		50	ns
TV_{TRSTB}	TRSTB minimum pulse width[4,5]		100		ns

Figure 159 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. This parameter is guaranteed by design. No production tests are done on this parameter.
4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.

20 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment[1].

Table 78 Outside Plant Thermal Information

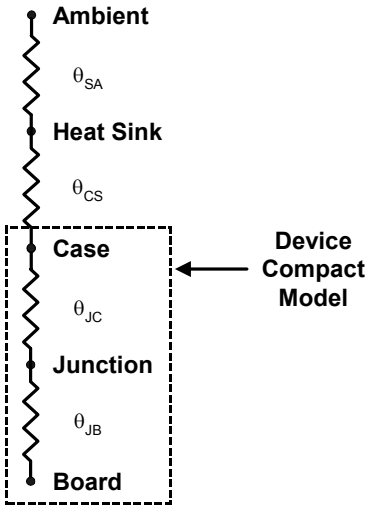
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	95 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 79 Device Compact Model[3]

Junction-to-Case Thermal Resistance, θ_{JC}	0.28 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	TBD °C/W

Table 80 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	The sum of θ_{SA} + θ_{CS} must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}$ °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package
	θ_{SA} and θ_{CS} are required for long-term operation



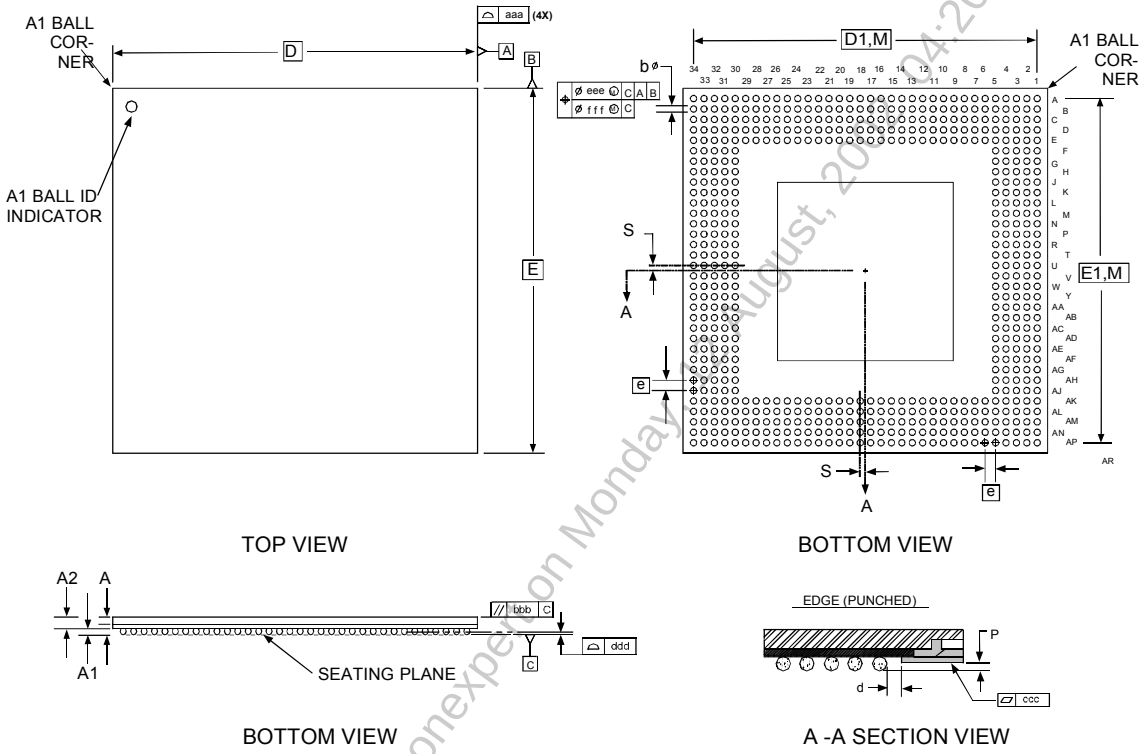
Power depends upon the operating mode. To obtain power information, refer to 'High' power values in section 17.1 Power Requirements.

Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core; for more information about this standard, see Section 4 References
3. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8; for more information about this standard, see Section 4 References
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place

21 Mechanical Information

Figure 160 Mechanical Drawing 580 Pin Tape Super Ball Grid Array (TSBGA)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ccc DENOTES FLATNESS.
5) DIMENSION ddd DENOTES COPLANARITY.
6) DIAMETER OF SOLDER MASK OPENING IS 0.55 +/- 0.050 MM (SMD).

PACKAGE TYPE : 580 TAPE SUPER BALL GRID ARRAY - TSBGA																			
BODY SIZE : 35 x 35 x 1.60 MM																			
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	d	e	aaa	bbb	ccc	ddd	eee	f f f	P	S
Min.	-	0.40	0.80	-	32.90	-	32.90	-	0.50	0.25	-	-	-	-	-	-	-	0.10	-
Nom.	-	0.50	0.91	35.00 BSC	33.00	35.00 BSC	33.00	34x34	0.65	-	1.00 BSC	-	-	-	-	0.30	0.10	-	-
Max.	1.60	0.60	1.00	-	33.10	-	33.10	-	0.80	-	-	0.20	0.25	0.20	0.20	-	-	-	0.50

Notes