PM4354

COMET™ QUAD

COMET-QUAD

FOUR CHANNEL COMBINED E1/T1/J1 TRANSCEIVER/FRAMER

Device Errata

Released

Issue 4: May, 2002

Downloaded by ahmed metwaly of silicon expert on Tuesday, 19 November, 2002 05:55:47 AM

Legal Information

Copyright

© 2002 PMC-Sierra, Inc.

The information is proprietary and confidential to PMC-Sierra, Inc., and for its customers' internal use. In any event, you cannot reproduce any part of this document, in any form, without the express written consent of PMC-Sierra, Inc.

Disclaimer

None of the information contained in this document constitutes an express or implied warranty by PMC-Sierra, Inc. as to the sufficiency, fitness or suitability for a particular purpose of any such information or the fitness, or suitability for a particular purpose, merchantability, performance, compatibility with other parts or systems, of any of the products of PMC-Sierra, Inc., or any portion thereof, referred to in this document. PMC-Sierra, Inc. expressly disclaims all representations and warranties of any kind regarding the contents or use of the information, including, but not limited to, express and implied warranties of accuracy, completeness, merchantability, fitness for a particular use, or non-infringement.

In no event will PMC-Sierra, Inc. be liable for any direct, indirect, special, incidental or consequential damages, including, but not limited to, lost profits, lost business or lost data resulting from any use of or reliance upon the information, whether or not PMC-Sierra, Inc. has been advised of the possibility of such damage.

Trademarks

COMET-QUAD is a trademark of PMC-Sierra, Inc. Other product and company names mentioned herein may be the trademarks of their respective owners.

Patents

The technology discussed is protected by one or more of the following Patents:

U.S. Patent No. 5,973,977

Canadian Patent No. 2,242,152

Relevant patent applications and other patents may also exist.

Downloaded by ahmed metwaly of silicoexpert on Tuesday, 5 September, 2006 05:55:47 AM

Contacting PMC-Sierra

PMC-Sierra
8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000
Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Technical Support: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

Revision History

Issue No.	Issue Date	Details of Change
1	April 2001	Document created.
2	May 2001	Documentation errata incorporated in the latest release of the COMET-QUAD Datasheet, Issue 6.
3	Oct 2001	Added the following documentation errata for the latest release of the COMET-QUAD Datasheet, Issue 6: Sections 3.1, 3.2, 3.3
4	May 2002	Section 3.4: PI to NI package change Section 3.5: Behavior in unframed mode Section 2.4: RLPS RAM initialization

Downloaded by ahmed metwaly of silicon xpert on Monday, 19 November, 2002 05:55:47 AM

Table of Contents

Downloaded by ahmed metwaly of siliconexpert on Tuesday, 19 November, 2002 05:55:47 AM

1 Introduction

In this document:

- Section 2 lists the known functional errata for Revision C of the PM4354 Device.
- Section 3 lists documentation errors found in Issue 6 of the COMET-QUAD Datasheet (PMC-1990315).

1.1 Device Identification

The information contained in Section 2 relates to Revision C of the PM4354 Device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device.

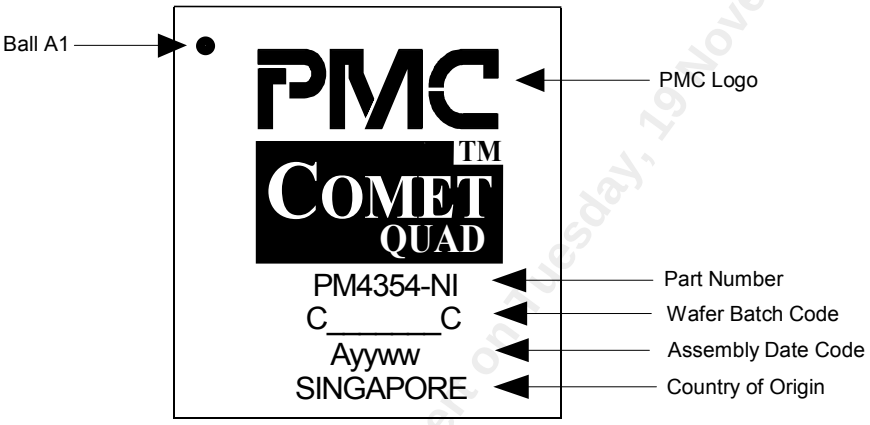


Figure 1 PM4354 COMET-QUAD Branding Format

1.2 References

- Issue 6 of the COMET-QUAD Datasheet (PMC-1990315).

Downloaded by ahmed metwaly of silicoexpert on Tuesday, 19 November 2002 05:15:47 AM

2 Device Functional Deficiency List

This section lists the known functional deficiencies for Revision C of the COMET-QUAD as of the publication date of this document. For each deficiency, the known workaround and the operating constraints, with and without the workaround, are also described.

Please report any functional deficiencies not covered in this errata to PMC-Sierra.

2.1 Internal HDLC Controller and Idle Code Insertion (E1 Mode)

2.1.1 Description:

The two least significant bits of timeslot N, where N is a number between 0 and 31, can be corrupted when any of the below statements are true:

1. Timeslot N+1 is configured for HDLC transmission (via the TDPR) and timeslot N is configured for idle code insertion (via the TPSC).

2. Timeslot N is configured for both HDLC transmission and idle code insertion.

3. Timeslot 31 (N = 31) is configured for idle code insertion and the Si-bit of timeslot 0 is configured for HDLC transmission.

2.1.2 Workarounds:

The following workarounds apply to the above statements respectively:

1. External insertion of idle codes or the use of an external HDLC controller will prevent idle code data corruption. It is recommended to utilize an external HDLC controller should it be necessary to insert idle codes in a timeslot immediately preceding HDLC data.

2. It is recommended to disable idle code insertion for timeslots that are also configured to transmit HDLC data.

3. External insertion of idle codes or the external insertion of HDLC data in the Si-bit position will prevent idle code data corruption.

2.1.3 Performance with workaround:

Normal operation.

2.1.4 Performance without workaround:

The two least significant bits of timeslot N may be corrupted.

NOTE: *This does not impact operation in T1 or J1 modes.*

Downloaded by ahmad.nettey@siliconexpert.com on Tuesday, 13 November, 2012 05:59:47 AM

2.2 Internal HDLC Controller and Timeslot One (E1 Mode)

2.2.1 Description:

If data is inserted into timeslot 1 via the internal HDLC controller and the Sa8-bit is configured to be externally inserted via the backplane, the Sa8-bit can be corrupted.

2.2.2 Workarounds:

The Sa8 bit is not corrupted when insertion is done via COMET's E1-TRAN National Bits Codeword register. The use of the internal HDLC Controller for timeslot one is not recommended.

2.2.3 Performance with workaround:

Normal operation.

2.2.4 Performance without workaround:

Potential corruption of the Sa8 bit.

NOTE: *This does not impact operation in T1 or J1 modes.*

2.3 Internal HDLC Controller and Data in Sa-bit Positions (E1 Mode)

2.3.1 Description:

If the internal HDLC controller is used to insert HDLC data in the Sa8, Sa7, Sa6 or Sa5 bit positions, the more significant bit adjacent to the inserted bit can be corrupted. In other words, HDLC data inserted in Sa8 can corrupt Sa7 and likewise data inserted in Sa5 can corrupt Sa4.

2.3.2 Workarounds:

National Use Bits (Sa-bits) inserted using the internal E1-TRAN block are always inserted correctly. Use of the internal HDLC controller to insert data into the Sa8, Sa7, Sa6, and Sa5 bit positions should be avoided.

2.3.3 Performance with workaround:

Normal operation.

2.3.4 Performance without workaround:

Potential corruption of a National Use (Sa) bit.

NOTE: *This does not impact operation in T1 or J1 modes.*

Downloaded by ahmed nebi of siliconexpert on Tuesday, 19 November, 2002 05:55:47 AM

2.4 Receive Equalizer RAM Initialization

2.4.1 Description:

There is a very rare set of circumstances under which writing to, or reading from, the Receive Line Pulse Slicer (RLPS) Equalization RAM could possibly result in the write or read being performed on a RAM table location other than the one intended.

The data transfer for a read/write from/to the RLPS RAM is initiated by loading the source/target RAM address into one of the RLPS Equalization Indirect Address registers (0FCH, 1FCH, 2FCH, 3FCH). However, since the microprocessor bus and the RLPS RAM operate in different clock domains (the RAM is operating synchronously to the T1 or E1 line), the RAM address latch must have time to synchronize to the microprocessor bus in order to grab the RAM address from the indirect address register. There is a remote possibility that a race condition could occur during this synchronization, and under very specific circumstances, one or more of the eight RAM address bits may not be latched in time for the read/write operation. In this case, the previous value of the address bit will be used to perform the read/write operation. Since any of the eight address bits may be effected, if this race condition occurs it is not possible to predict which location will be written or read.

Two things must happen before the read or write address is latched incorrectly:

1. At the very instant the read or write is initiated by writing to the indirect address register, there must be an exact phase alignment between the active edge of the read/write pulse and the line rate clock. This is a totally random event.

2. If and only if the active edge alignment condition stated above is met, the RAM address latch may not lock in a new address bit value quickly enough, meaning the previous address bit will be latched. The probability of not correctly latching one or more address bits is very sensitive to temperature, voltage, and device process, meaning different devices exhibit different behavior under approximately the same operating conditions, and the same device exhibits different behavior under varying operating conditions.

2.4.2 Workarounds:

PMC-Sierra is <u>not</u> recommending that this workaround be implemented on installed equipment. As discussed in the Performance Without Workaround section below, the rarity and limited scope of impact of this problem does <u>not</u> warrant in-field software upgrades. Only new designs and planned software upgrades to existing designs need implement this workaround.

Prior to an indirect read or write to the RLPS Equalization RAM, a dummy indirect read should be performed to the same address as the intended read or write. This ensures that, in the unlikely event that not all the address bits are latched, the unlatched bits will be identical to those that should have been latched. The contents of the dummy read should be ignored.

Downloaded by [illegible] of [illegible] on Tuesday, [illegible] 2002 05:55:47 AM

The code to perform a write command is shown below:

1. Perform a dummy read to ensure **RLPS Indirect Address** register is initialized

   WRITE nFDH 80H
   WRITE nFCH <RAM Address of the Equalizer RAM table >

2. Pause to ensure address bits are captured by the T1/E1 clock

   PAUSE <wait 3 line rate clock cycles>

3. Write the "Contents" of the Equalizer RAM table to the corresponding **RLPS Indirect Data** register.

   WRITE nD8H <Content[31:24] of the Equalizer RAM table>
   WRITE nD9H <Content[23:16] of the Equalizer RAM table>
   WRITE nDAH <Content[15:8] of the Equalizer RAM table>
   WRITE nDBH <Content[7:0] of the Equalizer RAM table>

4. Identify this operation as an indirect write using the **RLPS RAM Read/WriteB Select** register. (00H corresponds to a write.)

   WRITE nFDH 00H

5. Perform the write operation using the **RLPS Equalization Indirect Address** register.

   WRITE nFCH <RAM Address of the Equalizer RAM table >

6. Pause and then repeat the sequence for the following table entry.

   PAUSE <wait 3 line rate clock cycles>

The above code sequence replaces that found in Section 12.8 on page 373 of the datasheet.

2.4.3 Performance with workaround:

Normal operation.

2.4.4 Performance without workaround:

During a RLPS indirect read cycle this problem may result in an incorrect value being returned to the RLPS Equalization Indirect Data registers. Since there is no operational requirement to ever read the RLPS RAM -- except perhaps to check whether the contents are as previously written -- the impact of an incorrect read is software dependent. For example, if the software driver periodically reads the RLPS RAM values, compares them to what they should be, and re-writes any incorrect values, then the only impact this problem could have would be to erroneously cause a re-write of a value that is actually correct. This would have no impact whatsoever on how the device functions.

Downloaded by [illegible] on Tuesday, 19 November, 2002 05:55:47 AM

Therefore, the only time the performance of the device may be impacted by this problem is if a value in the RLPS RAM table has been written incorrectly during initialization, thereby causing a less than optimal value to be left in that RAM location. However, even if a write error occurs, in the majority of operating conditions the device will simply ignore the incorrect value.

There are three major factors to consider when analyzing the expected performance of the COMET-QUAD without the workaround:

1. What is the expected probability of a write occurring to the wrong location?
2. What is the device, equipment, and service impact should this occur?
3. What recovery mechanisms can be expected, and what is the probability that these recovery mechanisms will cause the RAM table to be re-initialized correctly?

Probability of an Incorrect Write:

To predict the probability of an incorrect write operation one must first determine the probability of the phase alignment condition described above being met, and multiply this by the probability of latching of one or more incorrect address bits. The resultant probability must also be considered over a range of operating conditions. It is difficult to calculate these probabilities precisely, but empirical testing shows that, with nominal devices and operating conditions, an incorrect address could be selected in approximately 1 in 600,000 read/write operations. Under specific conditions and with specific devices this could go as high as 1 in 250,000 operations, or as low as 0 (i.e. never happens). Therefore, across a range of devices and operating conditions, the read/write error rate averages out to better than 1 in 600,000. This is a conservative estimate; tested performance has actually been much better than this.

Impact of a RAM write error:

During the COMET-QUAD startup sequence, the 256 locations of each RAM are initialized with the values found in Section 12.8 of the datasheet. It is possible that an addressing error could occur during each of these series of 256 writes (multiple addressing errors in any RAM are improbable in the extreme). This means that one location could be left uninitialized and another location would be written with the wrong value. There is a 50% probability that the incorrect location being written is a higher address than the target location. If the writes are being done sequentially, then this higher location will be overwritten (i.e. corrected) by a later step in the initialization sequence. This means only the target location is corrupted – it will be left at whatever value was there previously. If a lower address is incorrectly selected, then both the target location and the incorrectly selected location will be corrupted. Therefore, if a write error occurs during the RLPS RAM initialization, there is a 50% chance that only one RAM location will be affected.

Downloaded by ahmed hamed of unexpected on Thursday, 08 November, 2001 05:55:47 AM

Once a receive equalizer is enabled, it hunts sequentially through its RAM table looking for the equalization value that produces the optimal signal recovery. The algorithm that controls this hunt essentially ignores single errors: it will try to use the erroneous value, discover that the signal recovery is poor at that location in the table, and "move on" to the next value. Adjacent table values are typically very near (or identical) in value, so even if the corrupted location is exactly at the desired equalization point the algorithm will simply move over a few locations and function normally. If two RAM locations are corrupted, and the corrupted locations are sufficiently far apart (5 locations or more), the algorithm will not be using them simultaneously, and they will each be treated as above: two occurrences of a single error. As with the single error case, there will be no impact on device performance. However, there is a 2% chance that the two RAM errors are within five locations of each other. Since adjacent values in the table are often identical in value, only the uninitialized value will be significantly different than its intended value. Thus, in approximately half of these cases, only the uninitialized value will be seen as incorrect and will behave exactly like the single error case: it will have no impact.

The remaining case (50% of 2% of 50% = 0.5% of all possible incorrect RLPS indirect writes) could cause the control algorithm to settle at the wrong location in the table and provide less than optimal equalization. This could result in higher bit error rate than expected. Also, the LOS value of the uninitialized location may be incorrect, resulting in incorrect declaration or clearing of the LOS signal.

In summary, the only condition that may cause a performance impact has a probability of occurring that is very small: 0.5% of (1 in 600,000) = 8.3×10^{-9}.

Recovery Mechanisms:

If an equalizer settles at a table location that is off by a significant amount from the desired location, the bit error rate will be high and framing may not lock. A typical operations procedure that an installer might follow is to reset the card in order to begin determining if the problem is with the link, the hardware, or the software. The card reset will cause the RLPS RAM table to be re-initialized, and in all likelihood this second initialization will have no problems. Essentially, there is zero probability that this problem will prevent the installer from getting the link to install after a second or third reset.

The only remaining issue is if the equalizer is only slightly off from its equalization point and this results in a slightly higher than normal bit error rate. Once again, a typical error monitoring procedure would be to reset the card upon discovering the higher than expected bit error rate. As above, this would cause the problem to disappear.

3 Documentation Deficiency List

This section lists the known documentation deficiencies for Issue 6 of the COMET-QUAD Datasheet (PMC-1990315) as of the publication date of this document.

Please report any documentation deficiencies not covered in this errata to PMC-Sierra.

3.1 Timeslot 16 AIS Indication

All references to the Timeslot 16 AIS handling in E1 mode should be removed from the COMET-QUAD Datasheet. This is not a feature of the COMET-QUAD. These references are found here:

1. The “Signaling Frame Alignment” part of Section 9.8, after Table 3, on page 45 of the COMET-QUAD Datasheet. Remove the entire paragraph:

   The E1-FRMR also indicates the reception of TS 16 AIS when timeslot 16 has been received with three or fewer zeros in each of two consecutive multiframe periods. The TS16AIS signal is cleared when each of two consecutive signaling multiframe periods contain four or more zeros OR when the signaling multiframe signal is found.

2. Section 9.8, Paragraph 4

   The E1-FRMR identifies the raw bit values for the Remote (or distant frame) Alarm (bit 3 in timeslot 0 of NFAS frames) and the Remote Signaling Multiframe (or distant multiframe) Alarm (bit 6 of timeslot 16 of frame 0 of the CAS multiframe) via the E1-FRMR International/National Bits Register, and the E1-FRMR Extra Bits Register respectively. Access is also provided to the "debounced" remote alarm and remote signaling multiframe alarm bits which are set when the corresponding signals have been a logic 1 for 2 or 3 consecutive occurrences, as per Recommendation O.162. Detection of AIS **~~and timeslot 16 AIS are~~ is** provided. AIS is also integrated, and an AIS Alarm is indicated if the AIS condition has persisted for at least 100 ms. The out of frame (OOF=1) condition is also integrated, indicating a Red Alarm if the OOF condition has persisted for at least 100 ms.

3. Section 9.8, Paragraph 5

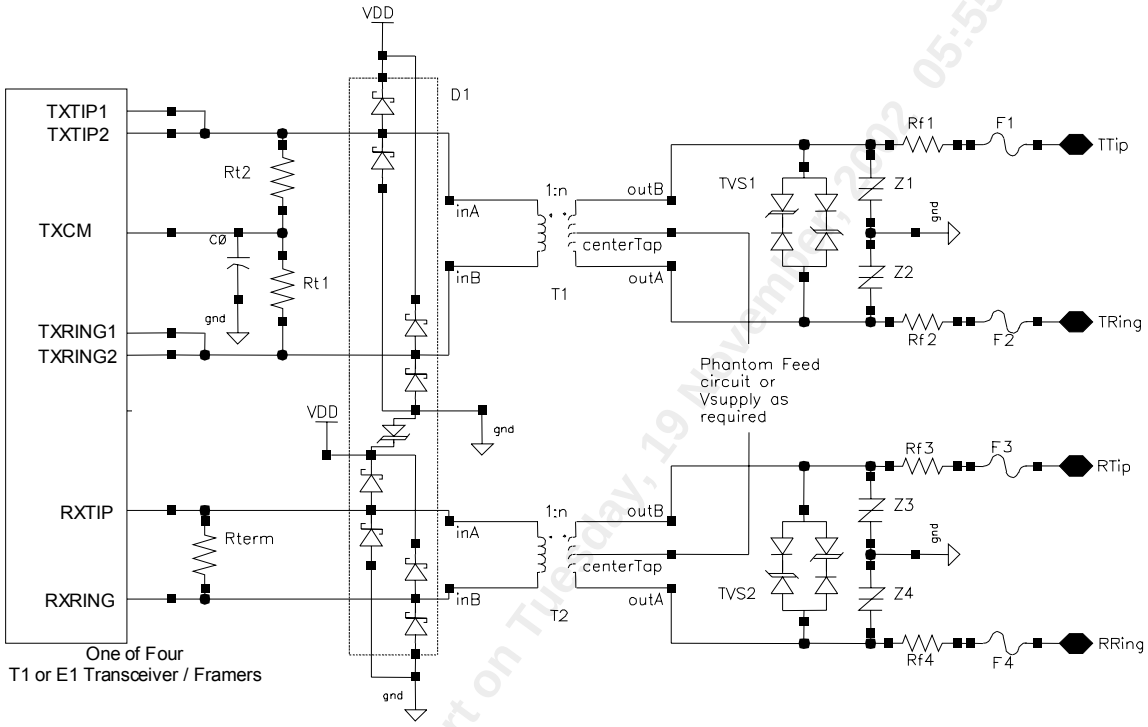
   An interrupt may be generated to signal a change in the state of any status bits (OOF, OOSMF, OOCMF, AIS or RED), and to signal when any event (RAI, RMAI, AISD, **~~TS16AISD,~~** COFA, FER, SMFER, CMFER, CRCE or FEBE) has occurred. Additionally, interrupts may be generated every frame, CRC submultiframe, CRC multiframe or signaling multiframe.

4. Section 9.23, Paragraph 3

   Common Channel Signaling (CCS) is supported in timeslot 16 through the Transmit Channel Insertion (TXCI) block. Support is provided for the transmission of AIS **~~and TS16 AIS~~**, and the transmission of remote alarm (RAI) and remote multiframe alarm signals.

3.2 External Analog Interface Circuit Diagram Missing Lines

Figure 5 on page 34 of the COMET-QUAD Datasheet, "External Analog Interface Circuits," is missing lines. The corrected version is shown below.



3.3 Pins Assigned Twice

In the COMET-QUAD Datasheet, two of the Analog I/O pins have been assigned twice. The D8 and P8 pins have been assigned as Reserved (RES[5:6]) and Analog Test Bus (ATB[1:2]). The ATB[1:2] pin description should be removed from the Datasheet.

3.3.1 Location

This incorrect assignment of D8 and P8 pins to ATB[1:2] is found in Section 8, Pin Descriptions, on page 26 of the COMET-QUAD Datasheet.

Downloaded by ahmed hatwaly @elecomexpert on Tuesday, 19 November 2002 05:55:47 AM

3.4 208 stPBGA Package

The COMET-QUAD package was changed to a 208-pin small thin Plastic Ball Grid Array (stPBGA).

3.4.1 Location

a) Reference to the old package on page 2 in Section 1 of the datasheet

b) The Pin Diagram is on page 14 and 15 in Section 7 of the datasheet

c) Table 110 is on page 445 in Section 18 of the datasheet

d) The Mechanical Information is on page 446 in Section 19 of the datasheet

3.4.2 Original Wording

a) Available in a high density 208-pin fine pitch PBGA (17 mm by 17 mm) package.

b) The COMET-QUAD is packaged in a 208-pin PBGA package having a body size of 17mm by 17mm and a ball pitch of 1.0 mm. The center 16 balls are not used as signal I/Os and are thermal balls.

208 PBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	D (2)	D (1)	TXRING1 (1)	TAVD2 (1)	TAVD3 (1)	TAVD1 (1)	RXRING (1)	RVREF (1	RAVS1 (2)	RAVD2 (2)	TXTIP2 (2	TAVS3 (2)	TXTIP1 (2)	A (1)	A (3)	A (5)	A
B	D (3)	VSS33 (1)	D (0)	TXTIP1 (1	TAVS3 (1)	TXTIP2 (1	RAVD2 (1)	RAVD1 (1)	RAVD1 (2)	RAVS2 (2)	TXRING2 (2)	TAVS2 (2)	A (0)	A (2)	A (4)	A (6)	B
C	D (4)	D (5)	VDD33 (1)	TAVS2 (1)	TXCM (1)	TAVS1 (1)	RXTIP (1)	QAVD (1)	RVREF (2)	RXRING (2)	TAVD1 (2)	TAVD3 (2)	TXRING1 (2)	VSS33 (9)	A (7)	A (8)	C
D	VSS33 (2)	D (6)	D (7)	VDD33 (2)	TXRING2 (1)	RAVS2 (1)	RAVS1 (1)	RES (5)	QAVS (1)	RXTIP (2)	TAVS1 (2)	TXCM (2)	TAVD2 (2)	RDB	A (10)	A (9)	D
E	CASBRD_B RPCM (1)	BRCLK (1)	BRSIG (1)	BRFP (1)									RSTB	ALE	WRB	CSB	E
F	CMVFPC	CMVFPB	BTCLK (1)	CASBTD_B TPCM (1)									BRPCM (2)	VSS33 (5)	INTB	BRCLK (2)	F
G	VDDC25 (1)	VSSC25 (1)	BTSIG (1)	VSSQ33 (1)			GND	GND	GND	GND			VSSC25 (5)	BRFP (2)	BRSIG (2)	VDD33 (5)	G
H	VSSC25 (2)	VDDQ33 (1)	VDDC25 (2)	BTFP (1)			GND	GND	GND	GND			BTPCM (2)	BTFP (2)	VDDC25 (5)	BTCLK (2)	H
J	VDDC25 (3)	VSS33 (3)	VSSC25 (3)	RES[4]			GND	GND	GND	GND			XCLK	BTSIG (2)	RES[3]	VDDC25 (8)	J
K	MVBTD	CCSBTD	CMV8MCLK	VDD33 (3)			GND	GND	GND	GND			VSSQ33 (2)	VDDQ33 (2)	VDDC25 (6)	VSSC25 (6)	K
L	VDDC25 (4)	BTCLK (3)	VSSC25 (4)	MVBRD_CCSBRD									VSS33 (6)	RES[1]	VSSC25 (7)	CTCLK	L
M	BTFP (3)	VSS33 (8)	BTSIG (3)	BTPCM (3)									VDDC25 (7)	BTCLK (4)	BTSIG (4)	BTPCM (4)	M
N	BRCLK (3)	VDD33 (4)	RES[2]	TAVS2 (3)	TXRING2 (3)	RAVS2 (3)	RAVS1 (3)	CAVS	CAVD	RXTIP (4)	TAVS1 (4)	TXCM (4)	BTFP (4)	VDD33 (6)	BRPCM (4)	BRCLK (4)	N
P	BRPCM (3)	BRSIG (3)	TRSTB	TXTIP1 (3	TXCM (3)	TAVS1 (3)	RXTIP (3)	RES (6)	RVREF (4)	RXRING (4)	TAVD1 (4)	TAVD3 (4)	TAVD2 (4)	VSS33 (7)	BRFP (4)	BRSIG (4)	P
R	BRFP (3)	VSS33 (4)	TMS	TXRING1 (3)	TAVS3 (3)	TXTIP2 (3	RAVD2 (3)	RAVD1 (3)	RAVS1 (4)	RAVS2 (4)	TXRING2 (4)	TAVS2 (4)	TXTIP1 (4)	QAVD (2)	PIO	RSYNC	R
T	TDO	TCK	TDI	TAVD2 (3)	TAVD3 (3)	TAVD1 (3)	RXRING (3)	RVREF (3	RAVD1 (4)	RAVD2 (4)	TXTIP2 (4	TAVS3 (4)	TXRING1 (4)	QAVS (2)	RES (8)	RES (7)	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOP VIEW

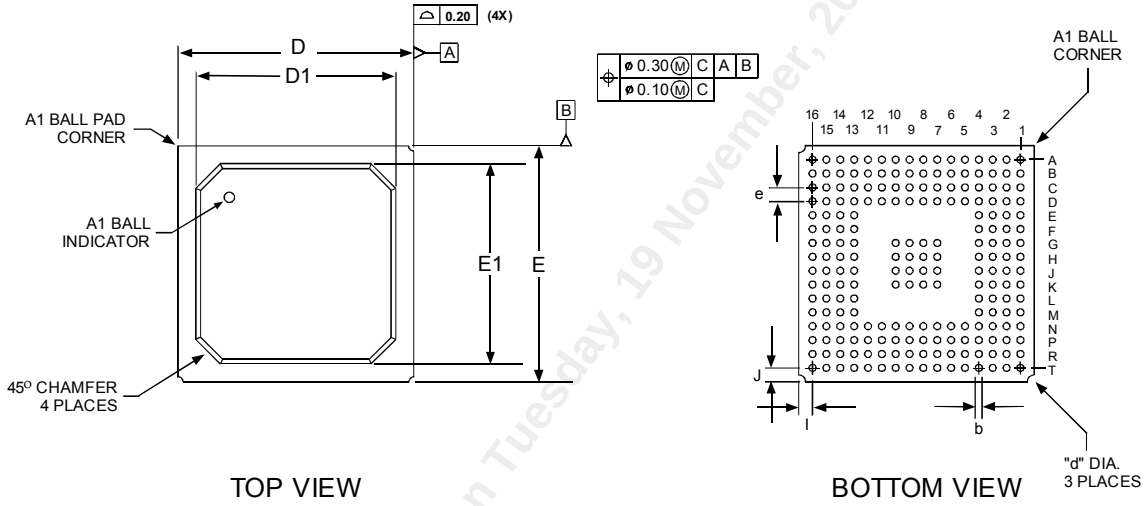
Downloaded by ahmed metwaly of siliconexpert on Tuesday, 19 November, 2002 05:55:47 AM

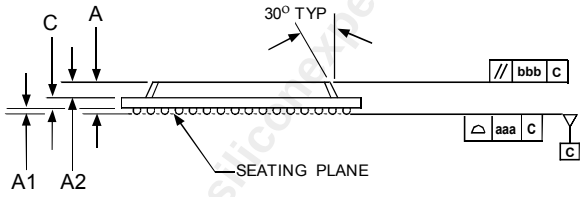
c)

Table 110: - Ordering Information

Part No.	Description
PM4354-PI	208 Plastic Ball Grid Array (PBGA)

d) MECHANICAL INFORMATION





NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES COPLANARITY.
3) DIMENSION bbb DENOTES PARALLEL.

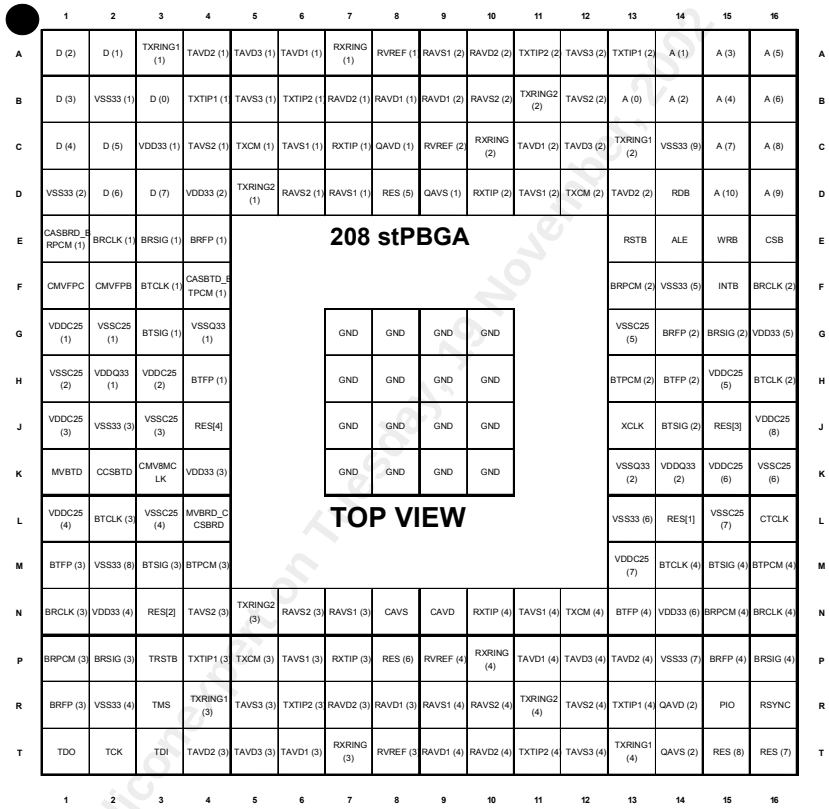
PACKAGE TYPE : 208 PLASTIC BALL GRID ARRAY - PBGA																	
BODY SIZE : 17 x 17 x 1.76 MM (4 layer)																	
Dim.	A (2 layer)	A (4 layer)	A1	A2	D	D1	C (2 layer)	C (4 layer)	E	E1	l	J	b	d	e	aaa	bbb
Min	1.35	1.55	0.30	0.75	-	14.50	0.30	0.50	-	14.50	-	-	0.40	-	-	-	-
Nom.	1.56	1.76	0.40	0.80	17.00	15.00	0.36	0.56	17.00	15.00	1.00	1.00	0.50	1.00	1.00	-	-
Max.	1.75	1.97	0.50	0.85	-	15.70	0.40	0.62	-	15.70	-	-	0.60	-	-	0.15	0.35

Downloaded by and may only be used in accordance with a license agreement on Tuesday, 19 November, 2002 05:55:47 AM

3.4.3 Replacement Wording

a) Available in a high density 208-pin fine pitch stPBGA (17 mm by 17 mm) package

b) The COMET-QUAD is packaged in a 208-pin stPBGA package having a body size of 17mm by 17mm and a ball pitch of 1.0 mm. The center 16 balls are not used as signal I/Os and are thermal balls.



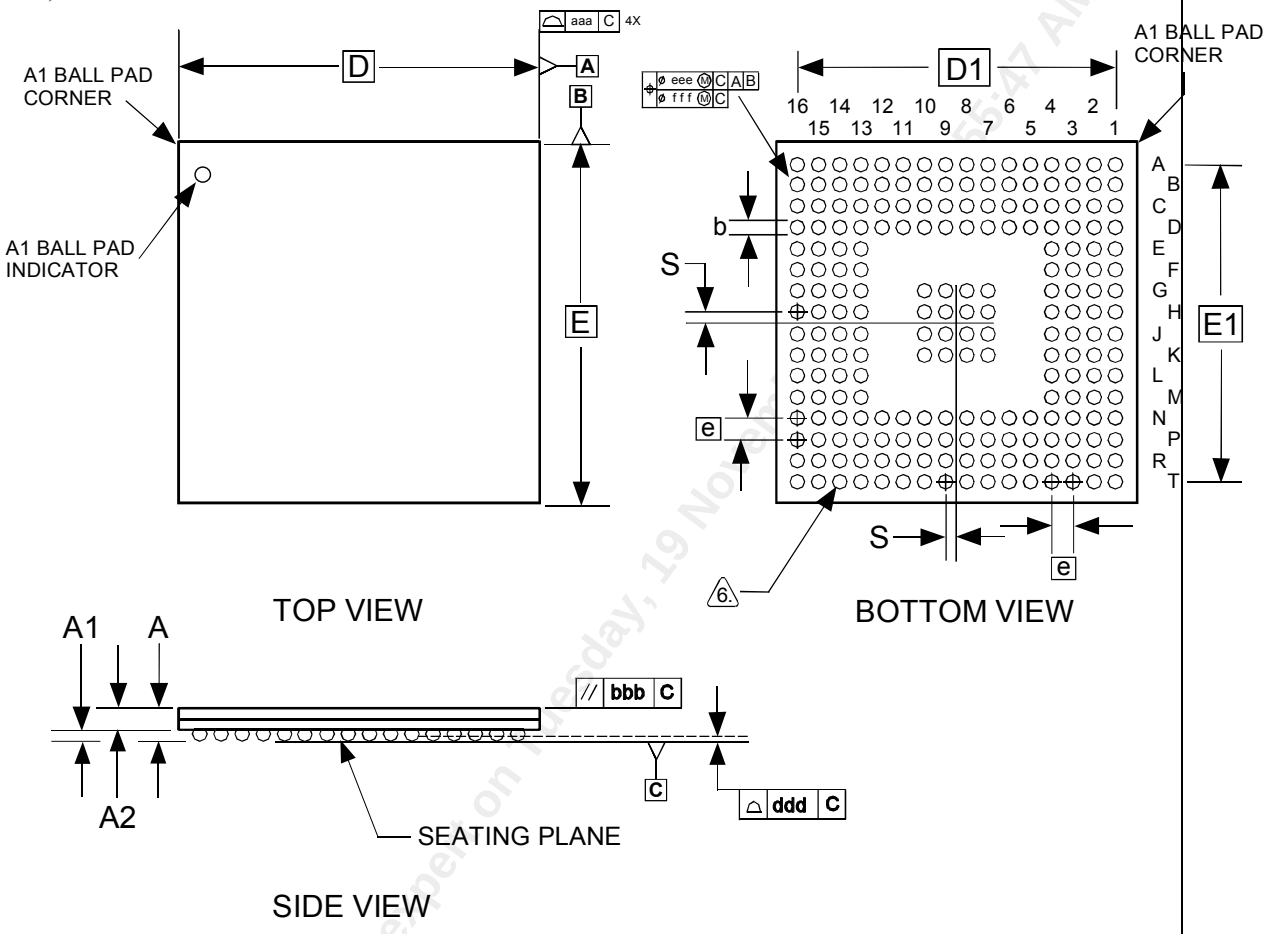
c)

Table 110: - Ordering Information

Part No.	Description
PM4354-NI	208 small thin Plastic Ball Grid Array (stPBGA)

Downloaded by ahmed mostafa of silicon expert on Tuesday, 03 November 2020, 05:35:47 AM

d) MECHANICAL INFORMATION



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ccc DENOTES FLATNESS.
5) DIMENSION ddd DENOTES COPLANARITY.
6) DIAMETER OF SOLDER MASK OPENING IS 0.450 ± 0.05 MM (SMD).

PACKAGE TYPE : 208 SMALL THIN PLASTIC BALL GRID ARRAY - stPBGA																
BODY SIZE : 17 x 17 x 1.70 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	b	e	aaa	bbb	ccc	ddd	eee	f f f	S
Min.	1.40	0.30	1.10	-	-	-	-	0.45	-	-	-	-	-	-	-	-
Nom.	-	-	-	17.00 BSC	15.00 BSC	17.00 BSC	15.00 BSC	0.50	1.00 BSC	-	-	-	-	-	-	0.50
Max.	1.70	-	-	-	-	-	-	0.55	-	0.20	0.25	-	0.20	0.25	0.10	-

Downloaded by ahmed.ibrahim@conexant.com on Tuesday, 19 November 2013, 6:47 AM

3.5 Behavior in Unframed Mode

AIS is not detected while the framer is in unframed mode. Also, it needs to be made clear that the ESF bit of the T1-FRMR Configuration registers (048H, 148H, 248H, 348H) is reset to logic 0 during unframed mode.

3.5.1 Location

Bit 6 (UNF) of the Receive Options registers (002H, 102H, 202H, 302H) is described on page 80 of Section 10.

3.5.2 Original Wording

The UNF bit allows the framer to operate with unframed DS-1 or E1 data. When UNF is set to logic 1, the framer is disabled (both the T1-FRMR and E1-FRMR are held reset) and the recovered data passes through the receiver section of the framer without frame or channel alignment. While UNF is set to logic 1, the Alarm Integrator continues to operate and detects and integrates AIS alarm. When UNF is set to logic 0, the framer operates normally, searching for frame alignment on the incoming data.

3.5.3 Replacement Wording

The UNF bit allows the framer to operate with unframed DS-1 or E1 data. When UNF is set to logic 1, the framer is disabled (both the T1-FRMR and E1-FRMR are held reset) and the recovered data passes through the receiver section of the framer without frame or channel alignment. While UNF is set to logic 1, the Alarm Integrator does not detect or integrate AIS alarm. When UNF is set to logic 0, the framer operates normally, searching for frame alignment on the incoming data. However, after UNF has toggled from logic 1 to logic 0, the framer will have been reset and all of the register bits associated with that framer will have been reset to their default values (for instance: the ESF bit of the T1-FRMR will be set to logic 0).

Downloaded by ahmed metwaly of silicon expert on Tuesday, 13 November, 2012, 05:55:21 AM

Notes

Downloaded by ahmed metwaly of siliconexpert on Tuesday, 19 November, 2002 05:55:47 AM