

DSP56001A

Product Preview 24-BIT DIGITAL SIGNAL PROCESSOR

The DSP56001A is an MPU-style general purpose Digital Signal Processor (DSP) composed of an efficient 24-bit DSP core, program and data memories, various peripherals, and support circuitry. The DSP56000 core is fed by on-chip Program RAM, two independent data RAMs, and two data ROMs containing sine, A-law, and μ -law tables. The DSP56001A contains a Serial Communication Interface (SCI), a Synchronous Serial Interface (SSI), and a parallel Host Interface (HI). This combination of features, illustrated in **Figure 1**, makes the DSP56001A a cost-effective, high-performance solution for high-precision general purpose digital signal processing. The DSP56001A is intended as a replacement for the DSP56001. The DSP56002 should be considered for new designs.

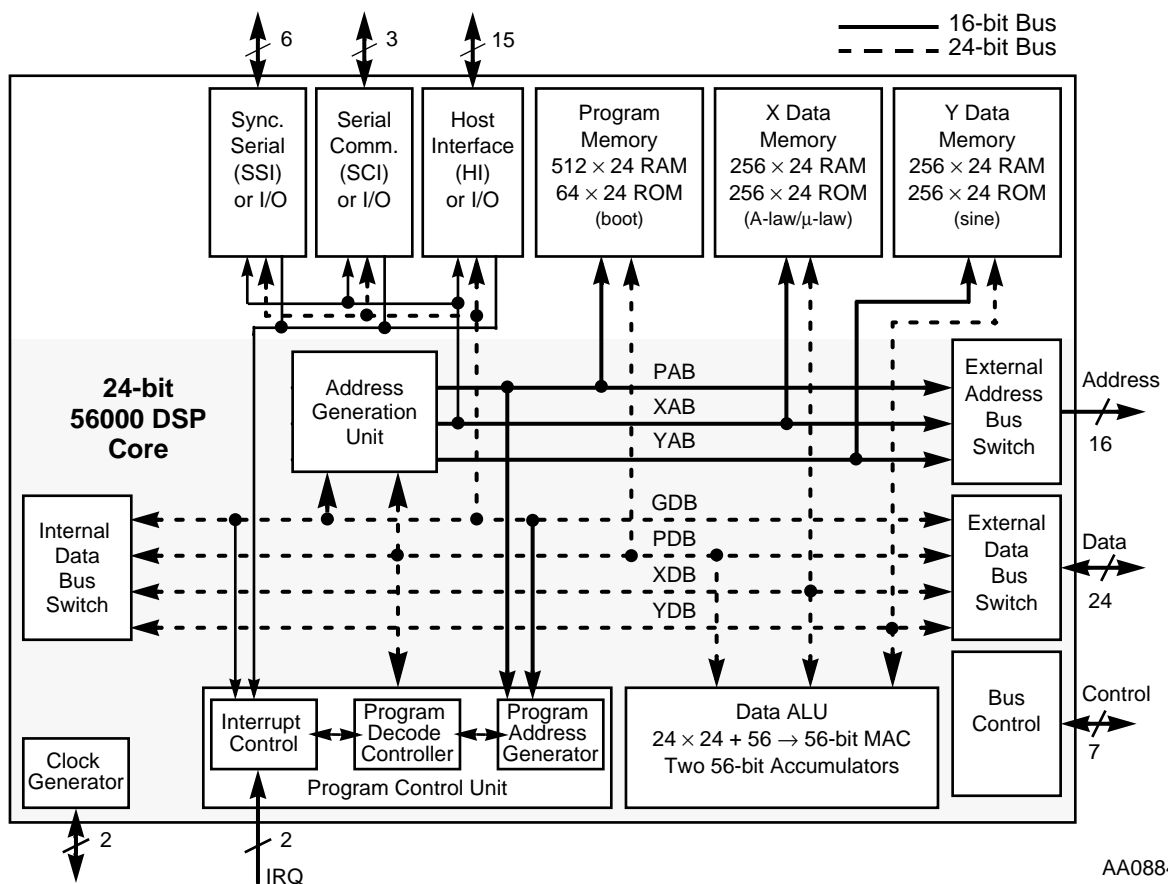


Figure 1 DSP56001A Block Diagram

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Data Sheet Conventions

This data sheet uses the following conventions:

- $\overline{\text{OVERBAR}}$ Used to indicate a signal that is active when pulled low; for example, the $\overline{\text{RESET}}$ pin is active when low
- “asserted” Means that a high true (active high) signal is high or that a low true (active low) signal is low
- “deasserted” Means that a high true (active high) signal is low or that a low true (active low) signal is high

| | | | | |
|-----------|-------------------------|--------------------|---------------------|-------------------------------|
| Examples: | Signal/Symbol | Logic State | Signal State | Voltage |
| | $\overline{\text{PIN}}$ | True | Asserted | $V_{\text{IL}}/V_{\text{OL}}$ |
| | $\overline{\text{PIN}}$ | False | Deasserted | $V_{\text{IH}}/V_{\text{OH}}$ |
| | PIN | True | Asserted | $V_{\text{IH}}/V_{\text{OH}}$ |
| | PIN | False | Deasserted | $V_{\text{IL}}/V_{\text{OL}}$ |

Note: Values for V_{IL} , V_{OL} , V_{IH} , and V_{OH} are defined by individual product specifications.

DSP56001A FEATURES

Digital Signal Processing Core

- Efficient, object code compatible, 24-bit 56000 family DSP engine
- Up to 16.5 Million Instructions Per Second (MIPS)—60.6 ns instruction cycle at 33 MHz
- Up to 99 Million Operations Per Second (MOPS) at 33 MHz
- Executes a 1024-point complex Fast Fourier Transform (FFT) in 59,898 clocks
- Highly parallel instruction set with unique DSP addressing modes
- Two 56-bit accumulators including extension byte
- Parallel 24×24 -bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
- Double precision 48×48 -bit multiply with 96-bit result in 6 instruction cycles
- 56-bit addition/subtraction in 1 instruction cycle
- Fractional arithmetic with support for multiprecision arithmetic
- Hardware support for block-floating point FFT
- Hardware nested DO loops
- Zero-overhead fast interrupts (2 instruction cycles)
- Four 24-bit internal data buses and three 16-bit internal address buses for maximum information transfer on-chip

Memory

- On-chip modified Harvard architecture permitting simultaneous accesses to program and two data memories
- 512×24 -bit on-chip Program RAM and 64×24 -bit bootstrap ROM
- Two 256×24 -bit on-chip data RAMs
- Two 256×24 -bit on-chip data ROMs containing sine, A-law and μ -law tables
- External memory expansion with 16-bit address and 24-bit data buses
- Bootstrap loading from external data bus or Host Interface

Peripheral and Support Circuits

- Byte-wide Host Interface (HI) with Direct Memory Access (DMA) support
- Synchronous Serial Interface (SSI) to communicate with codecs and synchronous serial devices
 - 8-, 12-, 16-, and 24-bit word sizes
 - Up to 32 software-selectable time slots in Network mode
- Serial Communication Interface (SCI) for full-duplex asynchronous communications
- On-chip peripheral registers memory mapped in data memory space
- Double-buffered peripherals
- Up to twenty-four General Purpose I/O (GPIO) pins
- Two external interrupt request pins

Miscellaneous Features

- Power-saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies from 33 MHz down to 4 MHz
- 88-pin Ceramic Pin Grid Array (PGA) package; 13 × 13 array
- 132-pin Plastic Quad Flat Pack (PQFP) surface-mount package; 24 × 24 × 4 mm
- 132-pin Ceramic Quad Flat Pack (CQFP) surface-mount package; 22 × 22 × 4 mm
- 5 V power supply

PRODUCT DOCUMENTATION

The three documents listed in **Table 1** are required for a complete description of the DSP56001A and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

Table 1 DSP56001A Documentation

| Topic | Description | Order Number |
|------------------------|------------------------------------------------------------------------------------------------------|---------------|
| DSP56001 User's Manual | Detailed description of the 56001 architecture, 24-bit DSP, memory, peripherals, and instruction set | DSP56001UM/AD |
| DSP56001A Data Sheet | Pin and package descriptions, and electrical and timing specifications | DSP56001A/D |

Related Documentation

Table 2 lists additional documentation relevant to the DSP56001A.

Table 2 DSP56001A Related Documentation

| Document Name | Description | Order Number |
|-------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|--------------|
| Digital Sine-Wave Synthesis | Application Report; uses the DSP56001 look-up table | APR1/D |
| Digital Stereo 10-band Graphic Equalizer | Application Report; includes code and circuitry; features the DSP56001 | APR2/D |
| Fractional and Integer Arithmetic | Application Report; includes code | APR3/D |
| Implementation of Fast Fourier Transforms | Application Report; comprehensive FFT algorithms and code for DSP56001, DSP56156, and DSP96002 | APR4/D |
| Implementation of PID Controllers | Application Report; PWM using the SCI timer and three phase output using modulo addressing | APR5/D |
| Convolutional Encoding and Viterbi Decoding with a V.32 Modem Trellis Example | Application Report; theory and code; features the DSP56001 | APR6/D |
| Implementing IIR/FIR Filters | Application Report; comprehensive example using the DSP56001 | APR7/D |
| Principles of Sigma-Delta Modulation for A-to-D Converters | Application Report; features the DSP56ADC16; improving resolution with half-band filters | APR8/D |
| Full-Duplex 32-kbit/s CCITT ADPCM Speech Coding | Application Report; features the DSP56001 | APR9/D |
| DSP56001 Interface Techniques and Examples | Application Report; interfaces for pseudo Static RAM, Dynamic RAM, ISA bus, Host Interface | APR11/D |

Table 2 DSP56001A Related Documentation (Continued)

| Document Name | Description | Order Number |
|--------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-----------------------------------------|
| Twin CODEC Expansion Board for the DSP56000 ADS | Application Report; circuit, code, FIR filter design for two voice band codecs connecting to the SSI | APR12/D |
| Conference Bridging in the Digital Telecommunications Environment | Application Report; theory and code; features the DSP56001/002 | APR14/D |
| Implementation of Adaptive Controllers | Application Report; adaptive control using reference models; generalized predictive control; includes code | APR15/D |
| Calculating Timing Requirements of External SRAM | Application Report; determination of SRAM speed for optimum performance | APR16/D |
| Low Cost Controller for DSP56001 | Application Report; circuit and code to connect two DSP56001s to an MC68008 | APR402/D |
| G.722 Audio Processing | Application Report; theory and code using SB-ADPCM | APR404/D |
| Minimal Logic DRAM Interface | Application Report; 1M x 480 ns DRAM, 1 PAL, code | APR405/D |
| Logarithmic/Linear Conversion Routines | Application Report; μ -law and A-law companding routines for PCM mono-circuits | ANE408/D |
| Third Party Compendium | Brochures from companies selling hardware and software that supports Motorola DSPs | DSP3RDPTYPAK/D |
| University Support Program | Flyer; Motorola's program supporting Universities in DSP research and education | BR382/D |
| Technical Training Schedule | Technical Training Schedule | BR348AD/D |
| Audio Course Information | Audio Course Information | BR928/D |
| Real Time Signal Processing Applications with Motorola's DSP56000 Family | Textbook by Mohamed El-Sharkawy; 398+ pages. (This is a charge item.) | Prentice-Hall, 1990; ISBN 0-13-767138-5 |



SECTION 1

SIGNAL/PIN DESCRIPTIONS

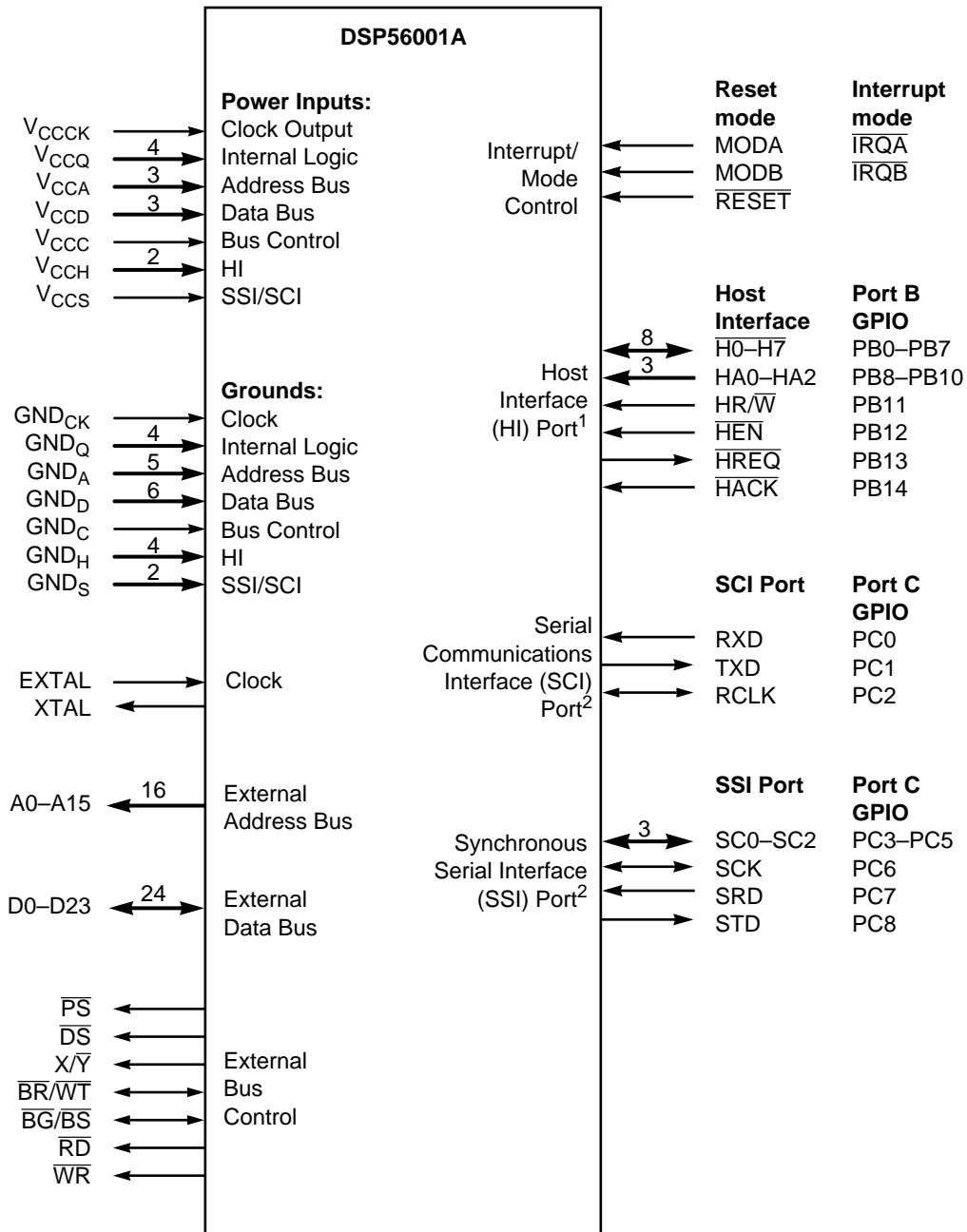
INTRODUCTION

DSP56001A signals are organized into twelve functional groups as summarized in **Table 1-1**.

Table 1-1 Signal Functional Group Allocations

| Functional Group | | Number of Signals | Detailed Description |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-------------------|----------------------|
| Power (V_{CCX}) | | 5 | Table 1-2 |
| Ground (GND_X) | | 7 | Table 1-3 |
| Clock | | 2 | Table 1-4 |
| Address Bus | Port A ¹ | 16 | Table 1-5 |
| Data Bus | | 24 | Table 1-6 |
| Bus Control | | 7 | Table 1-7 |
| Interrupt and Mode Control | | 3 | Table 1-8 |
| Host Interface (HI) Port | Port B ² | 15 | Table 1-9 |
| Serial Communications Interface (SCI) Port | Port C ³ | 3 | Table 1-10 |
| Synchronous Serial Interface (SSI) Port | | 6 | Table 1-11 |
| Note: <ol style="list-style-type: none"> 1. Port A signals define the External Memory Interface port. 2. Port B signals are GPIO signals multiplexed on the external pins also used with the HI signals. 3. Port C signals are GPIO signals multiplexed on the external pins also used by the SCI and SSI ports. | | | |

Figure 1-1 is a diagram of DSP56001A signals by functional group.



- Note:
1. The Host Interface port signals are multiplexed with the Port B GPIO signals (PB0–PB15).
 2. The SCI and SSI signals are multiplexed with the Port C GPIO signals (PC0–PC8).
 3. Power and ground lines are indicated for the 144-pin TQFP package.

AA0885

Figure 1-1 Signals Identified by Functional Group

POWER

Table 1-2 Power Connections

| Power Names | Description |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V _{CCQ} (2) | Internal Logic Power —These lines supply a quiet power source to the oscillator circuits and the mode control and interrupt lines. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V _{CC} power rail. Use a 0.1 μF bypass capacitor located as close as possible to the chip package to connect between the V _{CCQ} lines and the GND _Q lines. |
| V _{CCA} (3) | Address Bus Power —These lines supply power to the address bus. |
| V _{CCD} (3) | Data Bus Power —These lines supply power to the data bus. |
| V _{CC} | Bus Control Power —This line supplies power to the bus control logic. |
| V _{CCH} (2) | Host Interface Power —These lines supply power to the Host Interface logic. |
| V _{CCS} | Serial Interface Power —This line supplies power to the serial interface logic (SCI and SSI). |

GROUND

Table 1-3 Ground Connections

| Ground Names | Description |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GND _Q (2) | Internal Logic Ground —These lines supply a quiet ground connection for the oscillator circuits and the mode control and interrupt lines. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 μF bypass capacitor located as close as possible to the chip package to connect between the V _{CCQ} line and the GND _Q line. |
| GND _A (2) | Address Bus Ground —These lines connect system ground to the address bus. |
| GND _D (2) | Data Bus Ground —These lines connect system ground to the data bus. |
| GND _H (1) | Host Interface Ground —These lines supply ground connections for the Host Interface logic. |

CLOCK

Table 1-4 Clock Signals

| Signal Name | Signal Type | State during Reset | Signal Description |
|-------------|-------------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EXTAL | Input | Input | External Clock/Crystal Input —This input should be connected to an external crystal or to an external oscillator. |
| XTAL | Output | Chip-driven | Crystal Output —This output connects the internal crystal oscillator output to an external crystal. If an external oscillator is used, XTAL should be left unconnected. |

ADDRESS BUS

Table 1-5 Address Bus Signals

| Signal Names | Signal Type | State during Reset | Signal Description |
|--------------|-------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A0–A15 | Output | Tri-stated | Address Bus —These signals specify the address for external program and data memory accesses. If there is no external bus activity, A0–A15 remain at their previous values to reduce power consumption. A0–A15 are tri-stated when the bus grant signal is asserted. |

DATA BUS

Table 1-6 Data Bus Signals

| Signal Names | Signal Type | State during Reset | Signal Description |
|--------------|--------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D0–D23 | Input/Output | Tri-stated | Data Bus —These signals provide the bidirectional data bus for external program and data memory accesses. D0–D23 are tri-stated when the \overline{BG} or \overline{RESET} signal is asserted. |

BUS CONTROL

Table 1-7 Bus Control Signals

| Signal Name | Signal Type | State during Reset | Signal Description |
|----------------------------------------|------------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| \overline{PS} | Output | Tri-stated | Program Memory Select — \overline{PS} is asserted low for external program memory access. \overline{PS} is tri-stated when the \overline{BG} or \overline{RESET} signal is asserted. |
| \overline{DS} | Output | Tri-stated | Data Memory Select — \overline{DS} is asserted low for external data memory access. \overline{DS} is tri-stated when the \overline{BG} or \overline{RESET} signal is asserted. |
| X/\overline{Y} | Output | Tri-stated | X/\overline{Y} External Memory Select —This output is driven low during external Y data memory accesses. It is also driven low during external exception vector fetches when operating in the Development mode. X/\overline{Y} is tri-stated when the \overline{BG} or \overline{RESET} signal is asserted. |
| \overline{BR} \overline{WT} | Input/ Output | Tri-stated | Bus Request/Wait —The bus request input \overline{BR} allows another device such as a processor or DMA controller to become master of the external data bus D0–D23 and external address bus a0–a15. When operating mode register (OMR) bit 7 is clear and \overline{BR} is asserted, the DSP56001A will always release the external data bus D0–D23, address bus A0–A15, and bus control signals \overline{PS} , \overline{DS} , X/\overline{Y} , \overline{RD} , and \overline{WR} (i.e. Port A), by tri-stating these pins after execution of the current instruction has been completed. If OMR bit 7 is set, this pin is an input that allows an external device to force wait states during an external Port A operation for as long as \overline{WT} is asserted. Note: To prevent erroneous operation, pull up the $\overline{BR}/\overline{WT}$ signal when it is not in use. |
| \overline{BG} \overline{BS} | Input/ Output | Tri-stated | Bus Grant/Bus Select —If OMR Bit 7 is clear, this output is asserted to acknowledge an external bus request after Port A has been released. If OMR Bit 7 is set, this signal is bus strobe, and is asserted when the DSP accesses Port A. |
| \overline{WR} | Output | Tri-stated | Write Enable — \overline{WR} is asserted during external memory write cycles. \overline{WR} is tri-stated when the \overline{BG} or \overline{RESET} signal is asserted. |
| \overline{RD} | Output | Tri-stated | Read Enable — \overline{RD} is asserted during external memory read cycles. \overline{RD} is tri-stated when the \overline{BG} or \overline{RESET} signal is asserted. |

INTERRUPT AND MODE CONTROL

Table 1-8 Interrupt and Mode Control Signals

| Signal Name | Signal Type | State during Reset | Signal Description |
|--------------------------------------------------------|-------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>MODA</p> <p>$\overline{\text{IRQA}}$</p> | Input | Input | <p>Mode Select A/External Interrupt Request A—This input has two functions:</p> <ol style="list-style-type: none"> to select the initial chip operating mode, and after synchronization, to allow an external device to request a DSP interrupt. <p>MODA is read and internally latched in the DSP on exit from Reset. MODA and MODB select the initial chip operating mode. After leaving the Reset state, the MODA signal changes to external interrupt request $\overline{\text{IRQA}}$. The chip operating mode can be changed by software after reset. The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request that indicates that an external device is requesting service. It may be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull up resistor is required for wired-OR operation. If the processor is in the Stop state and $\overline{\text{IRQA}}$ is asserted, the processor will exit the Stop state.</p> |
| <p>MODB</p> <p>$\overline{\text{IRQB}}$</p> | Input | Input | <p>Mode Select B/External Interrupt Request B—This input has two functions:</p> <ol style="list-style-type: none"> to select the initial chip operating mode, and after internal synchronization, to allow an external device to request a DSP interrupt. <p>MODB is read and internally latched in the DSP on exit from Reset. MODA and MODB select the initial chip operating mode. After leaving the Reset state, the MODB signal changes to external interrupt request $\overline{\text{IRQB}}$. After reset, the chip operating mode can be changed by software. The $\overline{\text{IRQB}}$ input is an external interrupt request that indicates that an external device is requesting service. It may be programmed to be level sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.</p> |
| <p>$\overline{\text{RESET}}$</p> | Input | Input | <p>Reset—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the DSP is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from MODA and MODB. The internal reset signal is deasserted synchronously with the internal clocks.</p> |

CAUTION

**DO NOT APPLY 10 VOLTS TO ANY PIN OF
THE DSP56001A (including MODB)!
Subjecting any pin of the DSP56001A to
voltages in excess of the specified TTL/CMOS
levels will permanently damage the device.**

HOST INTERFACE (HI) PORT

Table 1-9 HI Signals

| Signal Name | Signal Type | State during Reset | Signal Description |
|-------------------|-----------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H0–H7 | Input/Output | Tri-stated | Host Data Bus (H0–H7) —This data bus transfers data between the host processor and the DSP56001A. When configured as a Host Interface port, the H0–H7 signals are tri-stated as long as \overline{HEN} is deasserted. The signals are inputs unless HR/\overline{W} is high and \overline{HEN} is asserted, in which case H0–H7 become outputs, allowing the host processor to read the DSP56001A data. H0–H7 become outputs when \overline{HACK} is asserted during \overline{HREQ} assertion. |
| PB0–PB7 | Input or Output | | Port B GPIO 0–7 (PB0–PB7) —These signals are GPIO signals (PB0–PB7) when the Host Interface is not selected. After reset, the default state for these signals is GPIO input. |
| HA0–HA2 | Input | Tri-stated | Host Address 0 – Host Address 2 (HA0–HA2) —These inputs provide the address selection for each Host Interface register. |
| PB8–PB10 | Input or Output | | Port B GPIO 8–10 (PB8–PB10) —These signals are GPIO signals (PB8–PB10) when the Host Interface is not selected. After reset, the default state for these signals is GPIO input. |
| HR/\overline{W} | Input | Tri-stated | Host Read/Write —This input selects the direction of data transfer for each host processor access. If HR/\overline{W} is high and \overline{HEN} is asserted, H0–H7 are outputs and DSP data is transferred to the host processor. If HR/\overline{W} is low and \overline{HEN} is asserted, H0–H7 are inputs and host data is transferred to the DSP. HR/\overline{W} must be stable when \overline{HEN} is asserted. |
| PB11 | Input or Output | | Port B GPIO 11 (PB11) —This signal is a GPIO signal called PB11 when the Host Interface is not being used. After reset, the default state for this signal is GPIO input. |

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Table 1-9 HI Signals (Continued)

| Signal Name | Signal Type | State during Reset | Signal Description |
|--------------------------|-------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{\text{HEN}}$ | Input | Tri-stated | Host Enable —This input enables a data transfer on the host data bus. When $\overline{\text{HEN}}$ is asserted and $\text{HR}/\overline{\text{W}}$ is high, H0–H7 become outputs and the host processor may read DSP56001A data. When $\overline{\text{HEN}}$ is asserted and $\text{HR}/\overline{\text{W}}$ is low, H0–H7 become inputs. Host data is latched in the DSP on the rising edge of $\overline{\text{HEN}}$. Normally, a chip select signal derived from host address decoding and an enable strobe are used to generate $\overline{\text{HEN}}$. |
| PB12 | Input or Output | | Port B GPIO 12 (PB12) —This signal is aGPIO signal called PB12 when the Host Interface is not being used. After reset, the default state for this signal is GPIO input. |
| $\overline{\text{HREQ}}$ | Open drain Output | Tri-stated | Host Request —This signal is used by the Host Interface to request service from the host processor, DMA controller, or a simple external controller. Note: $\overline{\text{HREQ}}$ should always be pulled high when it is not in use. |
| PB13 | Input or Output | | Port B GPIO 13 (PB13) —This signal is a GPIO (not open-drain) signal (PB13) when the Host Interface is not selected. After reset, the default state for this signal is GPIO input. |
| $\overline{\text{HACK}}$ | Input | Tri-stated | Host Acknowledge —This input has two functions. It provides a host acknowledge handshake signal for DMA transfers and it receives a host interrupt acknowledge compatible with MC68000 family processors. Note: $\overline{\text{HACK}}$ should always be pulled high when it is not in use. |
| PB14 | Input or Output | | Port B GPIO 14 (PB14) —This signal is a GPIO signal (PB14) when the Host Interface is not selected, and may be programmed as a GPIO signal when the Host Interface is selected. After reset, the default state for this signal is GPIO input. |

SERIAL COMMUNICATIONS INTERFACE PORT

Table 1-10 Serial Communications Interface (SCI) Signals

| Signal Name | Signal Type | State during Reset | Signal Description |
|-------------|-----------------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RXD | Input | Tri-stated | Receive Data (RXD) —This input receives byte-oriented data and transfers the data to the SCI receive shift register. Input data can be sampled on either the positive edge or on the negative edge of the receive clock, depending on how the SCI control register is programmed. |
| PC0 | Input or Output | | Port C GPIO 0 (PC0) —This signal is a GPIO signal called PC0 when the SCI RXD function is not being used. After reset, the default state is GPIO input. |
| TXD | Output | Tri-stated | Transmit Data (TXD) —This output transmits serial data from the SCI transmit shift register. In the default configuration, the data changes on the positive clock edge and is valid on the negative clock edge. The user can reverse this clock polarity by programming the SCI control register appropriately. |
| PC1 | Input or Output | | Port C GPIO 1 (PC1) —This signal is a GPIO signal called PC1 when the SCI TXD function is not being used. After reset, the default state is GPIO input. |
| SCLK | Input/ Output | Tri-stated | SCI Clock (SCLK) —This signal provides an input or output clock from which the transmit/receive baud rate is derived in the Asynchronous mode, and from which data is transferred in the Synchronous mode. The direction and function of the signal is defined by the RCM bit in the SCI Clock Control Register (SCCR). |
| PC2 | Input or Output | | Port C GPIO 2 (PC2) —This signal is a GPIO signal called PC2 when the SCI TCLK function is not being used. After reset, the default state is GPIO input. |

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SYNCHRONOUS SERIAL INTERFACE PORT

Table 1-11 Synchronous Serial Interface (SSI) Signals

| Signal Name | Signal Type | State during Reset | Signal Description |
|-------------|-----------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SC0 | Input or Output | Tri-stated | <p>Serial Clock 0 (SC0)—This signal's function is determined by whether the SCLK is in Synchronous or Asynchronous mode.</p> <ul style="list-style-type: none"> In Synchronous mode, this signal is used as a serial I/O flag. In Asynchronous mode, this signal receives clock I/O. <p>Port C GPIO 3 (PC3)—This signal is GPIO signal PC3 when not configured as SCI signal SC0.</p> <p>After reset, the default state is GPIO input.</p> |
| PC3 | Input or Output | | |
| SC1 | Input or Output | Tri-stated | <p>Serial Clock 1 (SC1)—The SSI uses this bidirectional signal to control flag or frame synchronization. This signal's function is determined by whether the SCLK is in Synchronous or Asynchronous mode.</p> <ul style="list-style-type: none"> In Asynchronous mode, this signal is frame sync I/O. For Synchronous mode with continuous clock, this signal is a serial I/O flag and operates like the SC0. <p>SC0 and SC1 are independent serial I/O flags, but may be used together for multiple serial device selection.</p> <p>Port C GPIO 4 (PC4)—This signal is GPIO signal PC4 when not configured as SSI function SC1.</p> <p>After reset, the default state is GPIO input.</p> |
| PC4 | Input or Output | | |
| SC2 | Input or Output | Tri-stated | <p>Serial Clock 2 (SC2)—The SSI uses this bidirectional signal to control frame synchronization only. As with SC0 and SC1, its function is defined by the SSI operating mode.</p> <p>Port C GPIO 5 (PC5)—This signal is GPIO signal PC5 when not configured as SSI function SC1.</p> <p>After reset, the default state is GPIO input.</p> |
| PC5 | Input or Output | | |
| SCK | Input or Output | Tri-stated | <p>SSI Serial Receive Clock—This bidirectional signal provides the serial bit rate clock for the SSI when only one clock is being used.</p> <p>Port C GPIO 6 (PC6)—This signal is GPIO signal PC6 when the SSI function is not being used.</p> <p>After reset, the default state is GPIO input.</p> |
| PC6 | Input or Output | | |

Table 1-11 Synchronous Serial Interface (SSI) Signals (Continued)

| Signal Name | Signal Type | State during Reset | Signal Description |
|-------------|-----------------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SRD | Input | Tri-stated | SSI Receive Data —This input signal receives serial data and transfers the data to the SSI Receive Shift Register. |
| PC7 | Input or Output | | <p>Port C GPIO 7 (PC7)—This signal is GPIO signal PC7 when the SSI SRD function is not being used.</p> <p>After reset, the default state is GPIO input.</p> |
| STD | Output | Tri-stated | SSI Transmit Data (STD) —This output signal transmits serial data from the SSI Transmitter Shift Register. |
| PC8 | Input or Output | | <p>Port C GPIO 8 (PC8)—This signal is GPIO signal PC8 when the SSI STD function is not being used.</p> <p>After reset, the default state is GPIO input.</p> |



SECTION 2

SPECIFICATIONS

GENERAL CHARACTERISTICS

The DSP56001A is fabricated in high-density HCMOS with TTL compatible inputs and outputs.

Table 2-1 Absolute Maximum Ratings (GND = 0 V)

| Rating | Symbol | Value | Unit |
|--------------------------------------------------|-----------|-----------------------------------|------|
| Supply Voltage | V_{CC} | -0.3 to +7.0 | V |
| All Input Voltages | V_{IN} | (GND - 0.5) to ($V_{CC} + 0.5$) | V |
| Current Drain per Pin excluding V_{CC} and GND | I | 10 | mA |
| Storage Temperature | T_{stg} | -55 to +150 | °C |

Note: This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Table 2-2 Recommended Operating Conditions

| Rating | Symbol | Value | Unit |
|------------------------------------------|----------|-------------|------|
| Supply Voltage | V_{CC} | 4.5 to 5.5 | V |
| Operating Temperature Range (See Note 1) | T_A | -40 to +105 | °C |

Table 2-3 Thermal Characteristics for 88-pin PGA Package

| Thermal Resistance | Symbol | Value | Rating |
|-------------------------------------------|-----------------|-------|--------|
| Junction to Ambient (See Note 2) | $R_{\theta JA}$ | 27 | °C/W |
| Junction to Case (estimated) (See Note 3) | $R_{\theta JC}$ | 6.5 | °C/W |

General Characteristics

Table 2-4 Thermal Characteristics for 132-pin CQFP/PQFP Packages

| Thermal Resistance | Symbol | Value | Rating |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------------|--------|
| Junction to Ambient | $R_{\theta JA}$ | 40 (CQFP) 47 (PQFP) | °C/W |
| Junction to Case (estimated) | $R_{\theta JC}$ | 7.0 (CQFP) 13.0 (PQFP) | °C/W |
| Note: <ol style="list-style-type: none"> 1. See discussion under Design Considerations, Heat Dissipation, page 4-1. 2. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided Printed Circuit Board per SEMI G38-87 in natural convection. SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Road, Mountain View, CA 94043, (415) 964-5111. 3. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88 with the exception that the cold plate temperature is used for the case temperature. | | | |

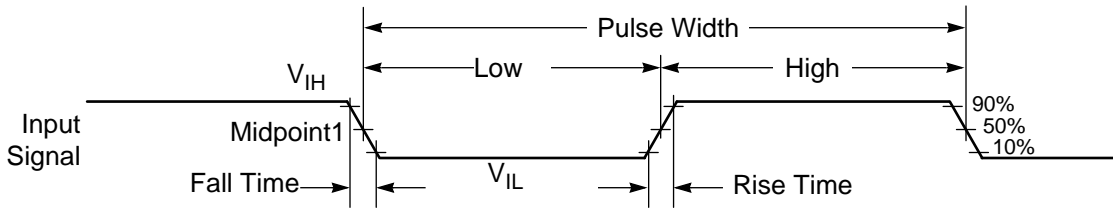
DC ELECTRICAL CHARACTERISTICS

Table 2-5 DC Electrical Characteristics

| Characteristics | Symbol | Min | Typ | Max | Units |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|------------------|----------------------------------------------|---------------------------|
| Supply Voltage 27 MHz 33 MHz | V_{CC} | 4.5 4.75 | 5.0 5.0 | 5.5 5.25 | V V |
| Input High Voltage • EXTAL • $\overline{\text{RESET}}$ • MODA, MODB • All other inputs | V_{IHC} V_{IHR} V_{IHM} V_{IH} | 4.0 2.5 3.5 2.0 | — — — — | V_{CC} V_{CC} V_{CC} V_{CC} | V V V V |
| Input Low Voltage • EXTAL • MODA, MODB • All other inputs | V_{ILC} V_{ILM} V_{IL} | -0.5 -0.5 -0.5 | — — — | 0.6 2.0 0.8 | V V V |
| Input Leakage Current EXTAL, $\overline{\text{RESET}}$, MODA/ $\overline{\text{IRQA}}$, MODB/ $\overline{\text{IRQB}}$, $\overline{\text{DR}}$, $\overline{\text{BR/WT}}$ | I_{IN} | -1 | — | 1 | μA |
| Tri-state (Off-state) Input Current (@ 2.4 V/0.4 V) | I_{TSI} | -10 | — | 10 | μA |
| Output High Voltage ($I_{OH} = -0.4 \text{ mA}$) | V_{OH} | 2.4 | — | — | V |
| Output Low Voltage ($I_{OL} = 1.6 \text{ mA}$) $\overline{\text{HREQ}} I_{OL} = 6.7 \text{ mA}$, TXD $I_{OL} = 6.7 \text{ mA}$ | V_{OL} | — | — | 0.4 | V |
| Internal Supply Current at 33 MHz (Note 1) • In Wait mode (Note 2) • In Stop mode (Note 2) | I_{CCI} I_{CCW} I_{CCS} | — — — | 80 10 2 | 115 25 2000 | mA mA μA |
| Input Capacitance (Note 3) | C_{IN} | — | 10 | — | pF |
| Note: | <ol style="list-style-type: none"> Section 4 Design Considerations describes how to calculate the external supply current. In order to obtain these results all inputs must be terminated (i.e., not allowed to float). Periodically sampled and not 100% tested | | | | |

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, and MODB. These pins are tested using the input levels set forth in the DC electrical characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56001A output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference

INTERNAL CLOCKS

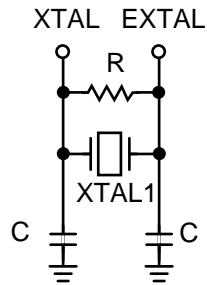
For each occurrence of T_H , T_L , T_C or I_{CYC} , substitute with the numbers in Table 2-6.

Table 2-6 Internal Clocks

| Characteristics | Symbol | Expression |
|------------------------------|-----------|----------------|
| Internal Operation Frequency | f | |
| Internal Clock High Period | T_H | ET_H |
| Internal Clock Low Period | T_L | ET_L |
| Internal Clock Cycle Time | T_C | ET_C |
| Instruction Cycle Time | I_{CYC} | $2 \times T_C$ |

EXTERNAL CLOCK (EXTAL PIN)

The DSP56001A system clock may be derived from the on-chip crystal oscillator as shown in **Figure 2-2**, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, leaving XTAL physically unconnected to the board or socket. The rise and fall times of this external clock should be 4 ns maximum.

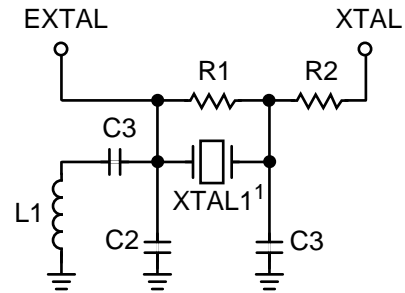


**Fundamental Frequency
Crystal Oscillator**

Suggested Component
Values

R = 680 k Ω \pm 10%
C = 20 pf \pm 20%

- Note:
1. The suggested crystal source is ICM, # 433163 – 4.00 (4 MHz fundamental, 20 pf load) or # 436163 – 30.00 (30 MHz fundamental, 20 pf load)
 2. To reduce system cost, a ceramic resonator may be used instead of the crystal. Suggested source: Murata-Erie #CST4.00MGW040 (4 MHz with built-in load capacitors)



**3rd Overtone
Crystal Oscillator**

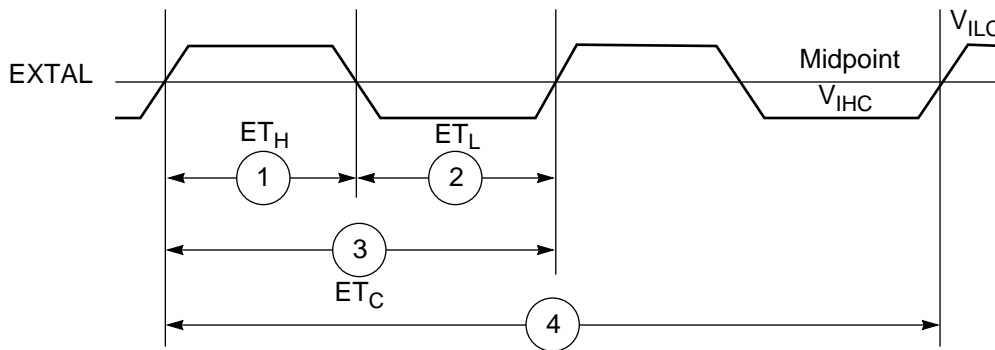
Suggested Component Values

R1 = 470 k Ω \pm 10%
R2 = 330 Ω \pm 10%
C1 = 0.1 μ f \pm 20%
C2 = 26 pf \pm 20%
C3 = 20 pf \pm 10%
L1 = 2.37 μ H \pm 10%
XTAL = 33 MHz, AT cut, 20 pf load,
50 Ω max series resistance

- Note:
1. 3rd overtone crystal
 2. The suggested crystal source is ICM, # 471163 – 33.00 (33 MHz 3rd overtone, 20 pf load)
 3. R2 limits crystal current
 4. Reference Benjamin Parzen, The Design of Crystal and Other Harmonic Oscillators, John Wiley & Sons, 1983

AA0886

Figure 2-2 Crystal Oscillator Circuits



NOTE: The midpoint is $V_{ILC} + 0.5(V_{IHC} - V_{ILC})$.

AA0360

Figure 2-3 External Clock Timing

Table 2-7 Clock Operation

| No | Characteristics | Symbol | 27 MHz | | 33 MHz | | Unit |
|-----------------------------------------------------------------------------------------------------------|---------------------------------------------------|-----------|--------|-----|--------|-----|------|
| | | | Min | Max | Min | Max | |
| | Frequency of Operation (EXTAL Pin) | E_f | 4 | 27 | 4 | 33 | MHz |
| 1 | Clock Input High (46.7% - 53.3% duty cycle) | ET_H | 17 | 150 | 13.5 | 150 | ns |
| 2 | Clock Input Low (46.7% - 53.3% duty cycle) | ET_L | 17 | 150 | 13.5 | 150 | ns |
| 3 | Clock Cycle Time | ET_C | 37 | 250 | 30 | 250 | ns |
| 4 | Instruction Cycle Time = $I_{CYC} = 2 \times T_C$ | I_{CYC} | 74 | 500 | 60 | 500 | ns |
| Note: External Clock Input High and External Clock Input Low are reserved at 50% of the input transition. | | | | | | | |

RESET, STOP, MODE SELECT, AND INTERRUPT TIMING

$V_{CC} = 5.0 \text{ V} \pm 10\%$ for 27 MHz; $V_{CC} = 5.0 \text{ V} \pm 5\%$ for 33 MHz

$T_J = -40$ to $+105 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF} + 1 \text{ TTL loads}$

WS = number of wait states programmed into the external bus access using BCR (WS = 0–15)

Table 2-8 Reset, Stop, Mode Select, and Interrupt Timing (27/33 MHz)

| Num | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------|---------------------|---------------------------------------|---------------------|----------|
| | | Min | Max | Min | Max | |
| 9 | Delay from $\overline{\text{RESET}}$ Assertion to Address High Impedance (periodically sampled and not 100% tested) | — | 38 | — | 31 | ns |
| 10 | Minimum Stabilization Duration <ul style="list-style-type: none"> Internal Oscillator (See Note 1) External clock (See Note 2) | $75000 \times T_C$ $25 \times T_C$ | — — | $75000 \times T_C$ $25 \times T_C$ | — — | ns ns |
| 11 | Delay from Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output (Internal Reset Deassertion) | $8 \times T_C$ | $9 \times T_C + 31$ | $8 \times T_C$ | $9 \times T_C + 25$ | ns |
| 12 | Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to first CKOUT transition | 15 | $T_C - 8$ | 13 | $T_C - 7$ | ns |
| 13 | Synchronous Reset Delay Time from the first CKOUT transition to the First External Address Output | $8 \times T_C + 5$ | $8 \times T_C + 23$ | $8 \times T_C + 5$ | $8 \times T_C + 19$ | ns |
| 14 | Mode Select Setup Time | 77 | — | 62 | — | ns |
| 15 | Mode Select Hold Time | 0 | — | 0 | — | ns |
| 16 | Minimum Edge-Triggered Interrupt Request Assertion Width | 17 | — | 16 | — | ns |
| 16a | Minimum Edge-Triggered Interrupt Request Deassertion Width | 10 | — | 10 | — | ns |

Table 2-8 Reset, Stop, Mode Select, and Interrupt Timing (27/33 MHz) (Continued)

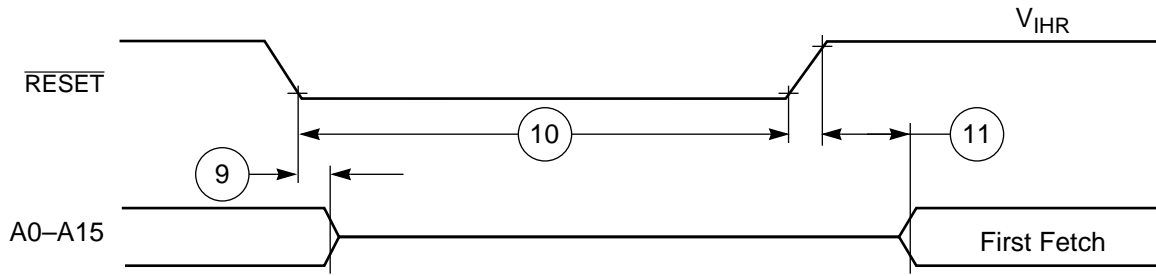
| Num | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|---------------------------------------------|-----------------------|---------------------------------------------|------|
| | | Min | Max | Min | Max | |
| 17 | Delay from \overline{IRQA} , \overline{IRQB} Assertion to External Memory Access Address Out Valid <ul style="list-style-type: none"> • Caused by First Interrupt Instruction Fetch • Caused by First Interrupt Instruction Execution | $5 \times T_C + T_H$ | — | $5 \times T_C + T_H$ | — | ns |
| | | $9 \times T_C + T_H$ | — | $9 \times T_C + T_H$ | — | ns |
| 18 | Delay from \overline{IRQA} , \overline{IRQB} Assertion to General Purpose Transfer Output Valid caused by First Interrupt Instruction Execution | $11 \times T_C + T_H$ | — | $11 \times T_C + T_H$ | — | ns |
| 19 | Delay from Address Output Valid caused by First Interrupt Instruction Execute to Interrupt Request Deassertion for Level-Sensitive Fast Interrupts (See Note 3) | — | $2 \times T_C + T_L + (T_C \times WS) - 34$ | — | $2 \times T_C + T_L + (T_C \times WS) - 27$ | ns |
| 20 | Delay from \overline{RD} Assertion to Interrupt Request Deassertion for Level-Sensitive Fast Interrupts (See Note 3) | — | $2 \times T_C + (T_C \times WS) - 31$ | — | $2 \times T_C + (T_C \times WS) - 25$ | ns |
| 21 | Delay from \overline{WR} Assertion to Interrupt Request Deassertion for Level-Sensitive Fast Interrupts (See Note 3) <ul style="list-style-type: none"> • $WS = 0$ • $WS > 0$ | — | $2 \times T_C - 31$ | — | $2 \times T_C - 25$ | ns |
| | | — | $T_C + T_L + (T_C \times WS) - 31$ | — | $T_C + T_L + (T_C \times WS) - 25$ | ns |

Table 2-8 Reset, Stop, Mode Select, and Interrupt Timing (27/33 MHz) (Continued)

| Num | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|----------------------------|---------------------------|----------------------------|------|
| | | Min | Max | Min | Max | |
| 22 | Delay from General-Purpose Output Valid to Interrupt Request Deassertion for Level-Sensitive Fast Interrupts (See Note 3)—If Second Interrupt Instruction is: <ul style="list-style-type: none"> • Single Cycle • Two Cycles | — | $T_L - 46$ | — | $T_L - 37$ | ns |
| | | — | $2 \times T_C + T_L - 46$ | — | $2 \times T_C + T_L - 37$ | ns |
| 23 | Synchronous Interrupt Setup Time from \overline{IRQA} , \overline{IRQB} Assertion to the second CKOUT transition | 19 | $T_C - 8$ | 16 | $T_C - 6$ | ns |
| 24 | Synchronous Interrupt Delay Time from the second CKOUT transition to the First External Address Output Valid caused by the First Instruction Fetch after coming out of Wait State | $13 \times T_C + T_H + 6$ | $13 \times T_C + T_H + 23$ | $13 \times T_C + T_H + 5$ | $13 \times T_C + T_H + 19$ | ns |
| 25 | Duration for \overline{IRQA} Assertion to Recover from Stop State | 19 | — | 16 | — | ns |
| 26 | Delay from \overline{IRQA} Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop') (See Note 1) <ul style="list-style-type: none"> • Internal Crystal Oscillator Clock, OMR Bit 6 = 0 • Stable External Clock, OMR Bit 6 = 1 | $65548 \times T_C$ | — | $65548 \times T_C$ | — | ns |
| | | $20 \times T_C$ | — | $20 \times T_C$ | — | ns |
| 27 | Duration of Level-Sensitive \overline{IRQA} Assertion to ensure interrupt service (when exiting 'Stop') (See Note 1) <ul style="list-style-type: none"> • Internal Crystal Oscillator Clock, OMR Bit 6 = 0 • Stable External Clock, OMR Bit 6 = 1 | $65534 \times T_C + T_L$ | — | $65534 \times T_C + T_L$ | — | ns |
| | | $6 \times T_C + T_L$ | — | $6 \times T_C + T_L$ | — | ns |

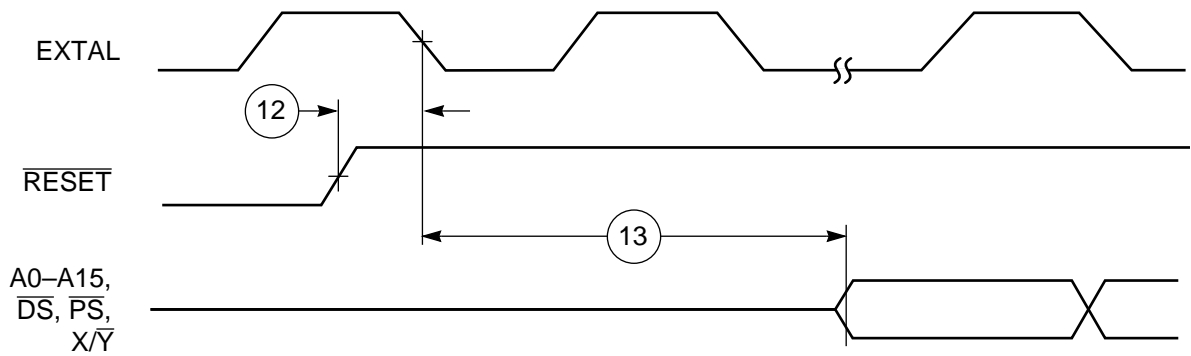
Table 2-8 Reset, Stop, Mode Select, and Interrupt Timing (27/33 MHz) (Continued)

| Num | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|-----|------------------------|-----|------|
| | | Min | Max | Min | Max | |
| 28 | Delay from Level-Sensitive $\overline{\text{IRQA}}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop') (See Note 1) <ul style="list-style-type: none"> • Internal Crystal Oscillator Clock, OMR Bit 6 = 0 • Stable External Clock, OMR Bit 6 = 1 | 65548 × T _C | — | 65548 × T _C | — | ns |
| | | 20 × T _C | — | 20 × T _C | — | ns |
| Note: <ol style="list-style-type: none"> 1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases: <ul style="list-style-type: none"> • after power-on reset, and • when recovering from Stop mode. During this stabilization period, T_C, T_H, and T_L will not be constant. Since this stabilization period varies, a delay of 75,000 × T_C is typically allowed to assure that the oscillator is stable before executing programs. While it is possible to set OMR Bit 6 = 1 when using the internal crystal oscillator, it is not recommended and these specifications do not guarantee timings for that case. 2. Circuit stabilization delay is required during reset when using an external clock in two cases: <ul style="list-style-type: none"> • after power-on reset, and • when recovering from Stop mode. 3. When using fast interrupts and $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ are defined as level-sensitive, then timings 19 through 22 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-Triggered mode is recommended when using fast interrupt. Long interrupts are recommended when using Level-Sensitive mode. | | | | | | |



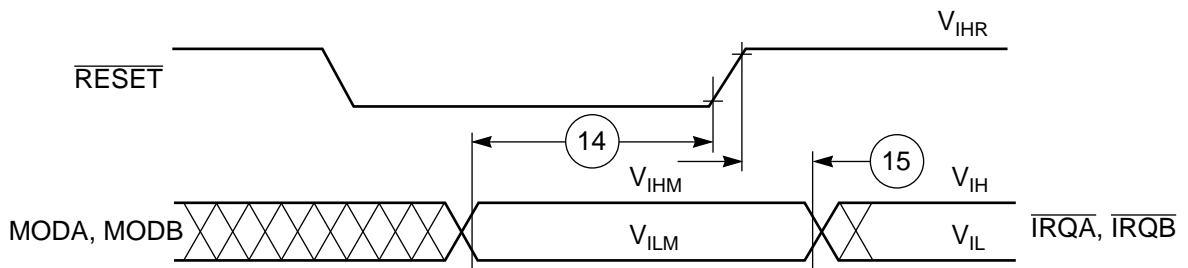
AA0356

Figure 2-4 Reset Timing



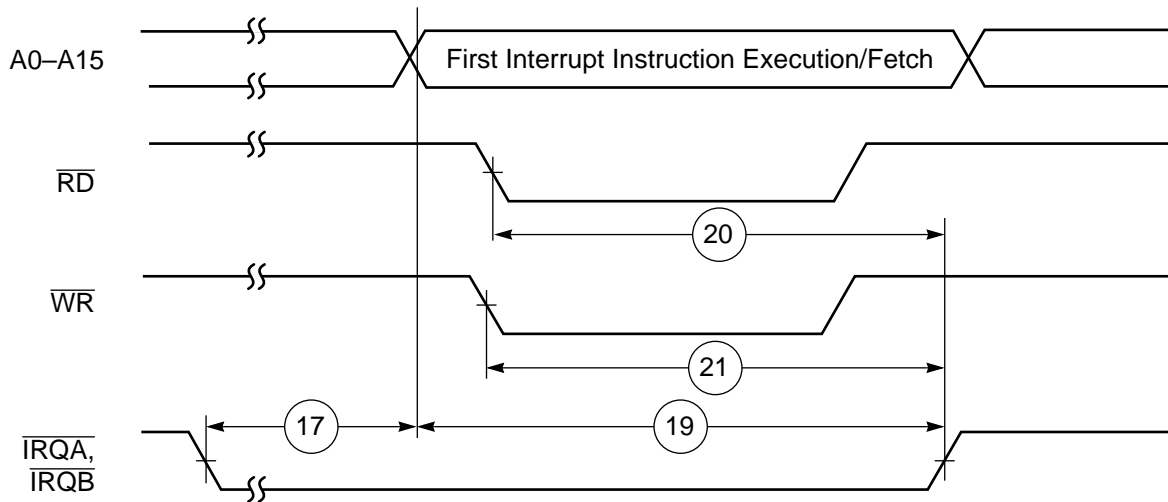
AA0887

Figure 2-5 Synchronous Reset Timing

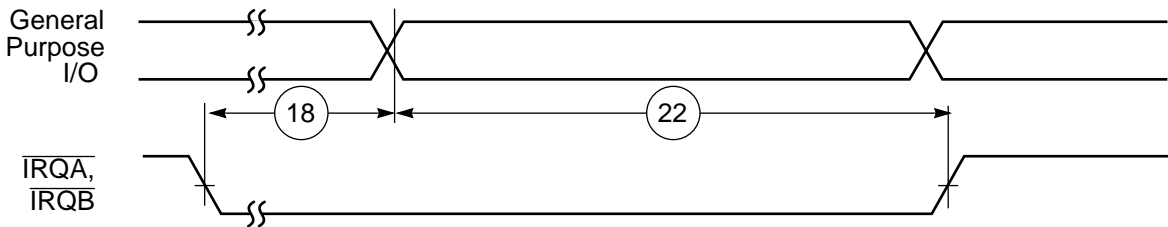


AA0888

Figure 2-6 Operating Mode Select Timing



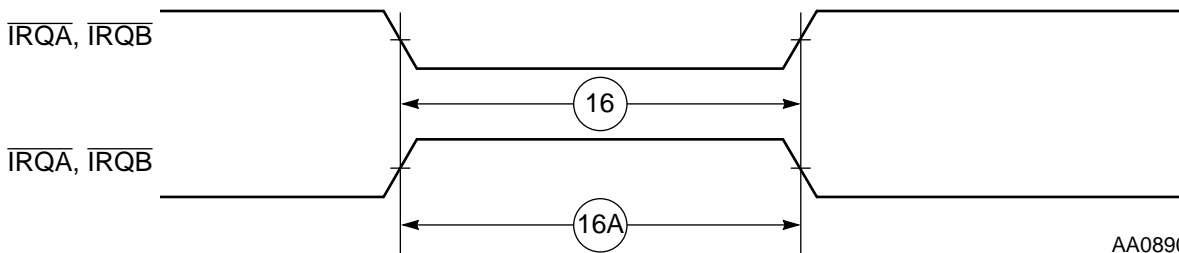
a) First Interrupt Instruction Execution



b) General Purpose I/O

AA0889

Figure 2-7 External Level-Sensitive Fast Interrupt Timing



AA0890

Figure 2-8 External Interrupt Timing (Negative Edge-Triggered)

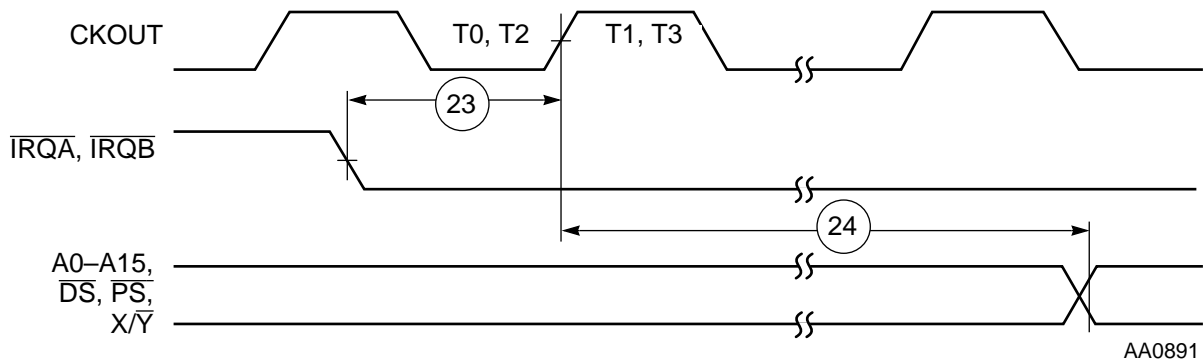


Figure 2-9 Synchronous Interrupt from Wait State Timing

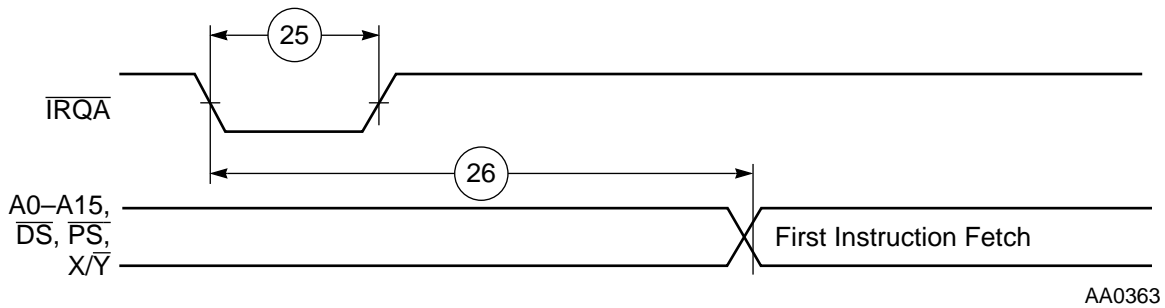


Figure 2-10 Recovery from Stop State Using $\overline{\text{IRQA}}$

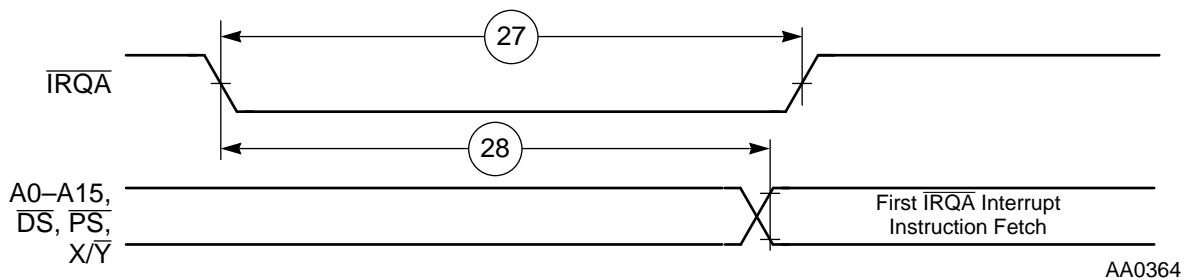


Figure 2-11 Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

HOST I/O (HI) TIMING

$V_{CC} = 5.0\text{ V} \pm 10\%$ for 27 MHz; $5.0\text{ V} \pm 5\%$ for 33 MHz;
 $T_J = -40$ to $105\text{ }^\circ\text{C}$; $C_L = 50\text{ pF} + 1\text{ TTL loads}$

Note: Active low lines should be pulled up in a manner consistent with the AC and DC specifications.

Table 2-9 Host I/O Timing (27/33 MHz)

| Num | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-------------|---------------------|-------------|------|
| | | Min | Max | Min | Max | |
| 30 | Host Synchronization Delay (see Note 1) | T_L | $T_C + T_L$ | T_L | $T_C + T_L$ | ns |
| 31 | $\overline{\text{H}}\overline{\text{E}}\overline{\text{N}}/\overline{\text{H}}\overline{\text{A}}\overline{\text{C}}\overline{\text{K}}$ Assertion Width (See Note 2) <ul style="list-style-type: none"> CVR, ICR, ISR, RXL Read IVR, RXH/M Read Write | $T_C + 46$ | — | $T_C + 37$ | — | ns |
| | | 39 | — | 31 | — | ns |
| | | 19 | — | 16 | — | ns |
| 32 | $\overline{\text{H}}\overline{\text{E}}\overline{\text{N}}/\overline{\text{H}}\overline{\text{A}}\overline{\text{C}}\overline{\text{K}}$ Deassertion Width (See Note 2) <ul style="list-style-type: none"> Between Two TXL Writes (See Note 3) Between Two CVR, ICR, ISR, RXL Reads (See Note 4) | 19 | — | 16 | — | ns |
| | | $2 \times T_C + 46$ | — | $2 \times T_C + 37$ | — | ns |
| | | $2 \times T_C + 46$ | — | $2 \times T_C + 37$ | — | ns |
| 33 | Host Data Input Setup Time Before $\overline{\text{H}}\overline{\text{E}}\overline{\text{N}}/\overline{\text{H}}\overline{\text{A}}\overline{\text{C}}\overline{\text{K}}$ Deassertion | 4 | — | 4 | — | ns |
| 34 | Host Data Input Hold Time After $\overline{\text{H}}\overline{\text{E}}\overline{\text{N}}/\overline{\text{H}}\overline{\text{A}}\overline{\text{C}}\overline{\text{K}}$ Deassertion | 4 | — | 4 | — | ns |
| 35 | $\overline{\text{H}}\overline{\text{E}}\overline{\text{N}}/\overline{\text{H}}\overline{\text{A}}\overline{\text{C}}\overline{\text{K}}$ Assertion to Output Data Active from High Impedance | 0 | — | 0 | — | ns |
| 36 | $\overline{\text{H}}\overline{\text{E}}\overline{\text{N}}/\overline{\text{H}}\overline{\text{A}}\overline{\text{C}}\overline{\text{K}}$ Assertion to Output Data Valid | — | 39 | — | 31 | ns |
| 37 | $\overline{\text{H}}\overline{\text{E}}\overline{\text{N}}/\overline{\text{H}}\overline{\text{A}}\overline{\text{C}}\overline{\text{K}}$ Deassertion to Output Data High Impedance (See Note 6) | — | 27 | — | 22 | ns |
| 38 | Output Data Hold Time After $\overline{\text{H}}\overline{\text{E}}\overline{\text{N}}/\overline{\text{H}}\overline{\text{A}}\overline{\text{C}}\overline{\text{K}}$ Deassertion (See Note 7) | 4 | — | 4 | — | ns |

Table 2-9 Host I/O Timing (Continued)(27/33 MHz) (Continued)

| Num | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-----|----------------------------|-----|------|
| | | Min | Max | Min | Max | |
| 39 | HR/ \overline{W} Low Setup Time Before \overline{HEN} Assertion | 0 | — | 0 | — | ns |
| 40 | HR/ \overline{W} Low Hold Time After \overline{HEN} Deassertion | 4 | — | 4 | — | ns |
| 41 | HR/ \overline{W} High Setup Time to \overline{HEN} Assertion | 0 | — | 0 | — | ns |
| 42 | HR/ \overline{W} High Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion | 4 | — | 4 | — | ns |
| 43 | HA0-HA2 Setup Time Before \overline{HEN} Assertion | 0 | — | 0 | — | ns |
| 44 | HA0-HA2 Hold Time After \overline{HEN} Deassertion | 4 | — | 4 | — | ns |
| 45 | DMA \overline{HACK} Assertion to \overline{HREQ} Deassertion (See Note 5) | 4 | 46 | 4 | 46 | ns |
| 46 | DMA \overline{HACK} Deassertion to \overline{HREQ} Assertion (See Notes 5, 6) | | | | | |
| | • for DMA RXL Read | $t_{HSDL} + T_C + T_H + 4$ | — | $t_{HSDL} + T_C + T_H + 4$ | — | ns |
| | • for DMA TXL Write | $t_{HSDL} + T_C + 4$ | — | $t_{HSDL} + T_C + 4$ | — | ns |
| | • all other cases | 4 | — | 4 | — | ns |
| 47 | Delay from \overline{HEN} Deassertion to \overline{HREQ} Assertion for RXL Read (See Notes 5, 6) | $t_{HSDL} + T_C + T_H + 4$ | — | $t_{HSDL} + T_C + T_H + 4$ | — | ns |
| 48 | Delay from \overline{HEN} Deassertion to \overline{HREQ} Assertion for TXL Write (See Notes 5, 6) | $t_{HSDL} + T_C + 4$ | — | $t_{HSDL} + T_C + 4$ | — | ns |
| 49 | Delay from \overline{HEN} Assertion to \overline{HREQ} Deassertion for RXL Read, TXL Write (See Notes 5, 6) | 4 | 70 | 4 | 65 | ns |
| Note: | <ol style="list-style-type: none"> Host synchronization delay (t_{HSDL}) is the time period required for the DSP56001 to sample any external asynchronous input signal, determine whether it is high or low, and synchronize it to the DSP56001 internal clock. See Host Port Considerations in the section on Design Considerations. This timing must be adhered to only if two consecutive writes to the TXL are executed without polling TXDE or \overline{HREQ}. This timing must be adhered to only if two consecutive reads from one of these registers are executed without polling the corresponding status bits or \overline{HREQ}. \overline{HREQ} is pulled up by a 1 kΩ resistor. Specifications are periodically sampled and not 100% tested. May decrease to 0 ns for future versions. | | | | | |

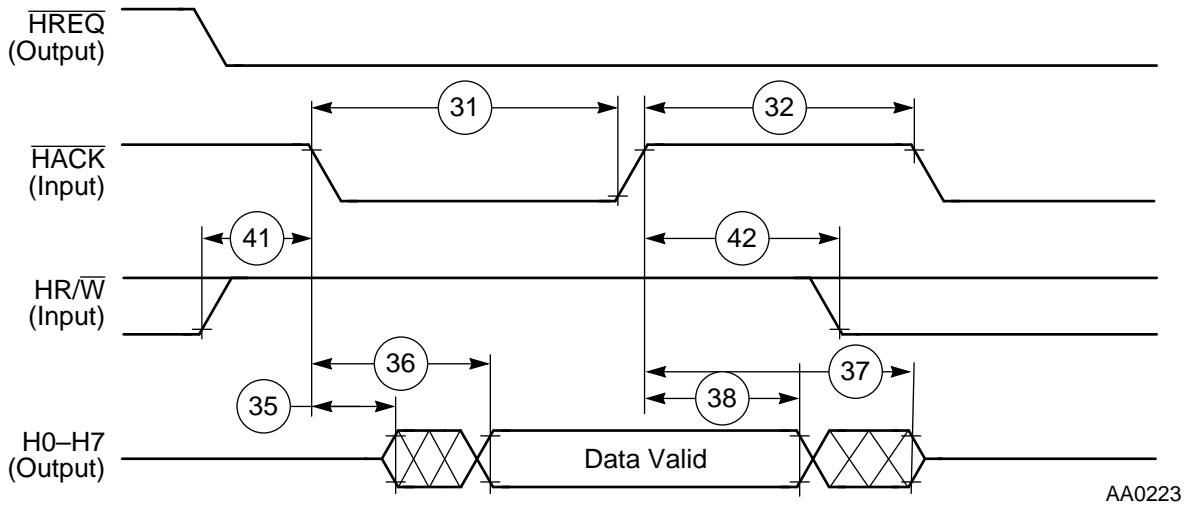


Figure 2-12 Host Interrupt Vector Register (IVR) Read

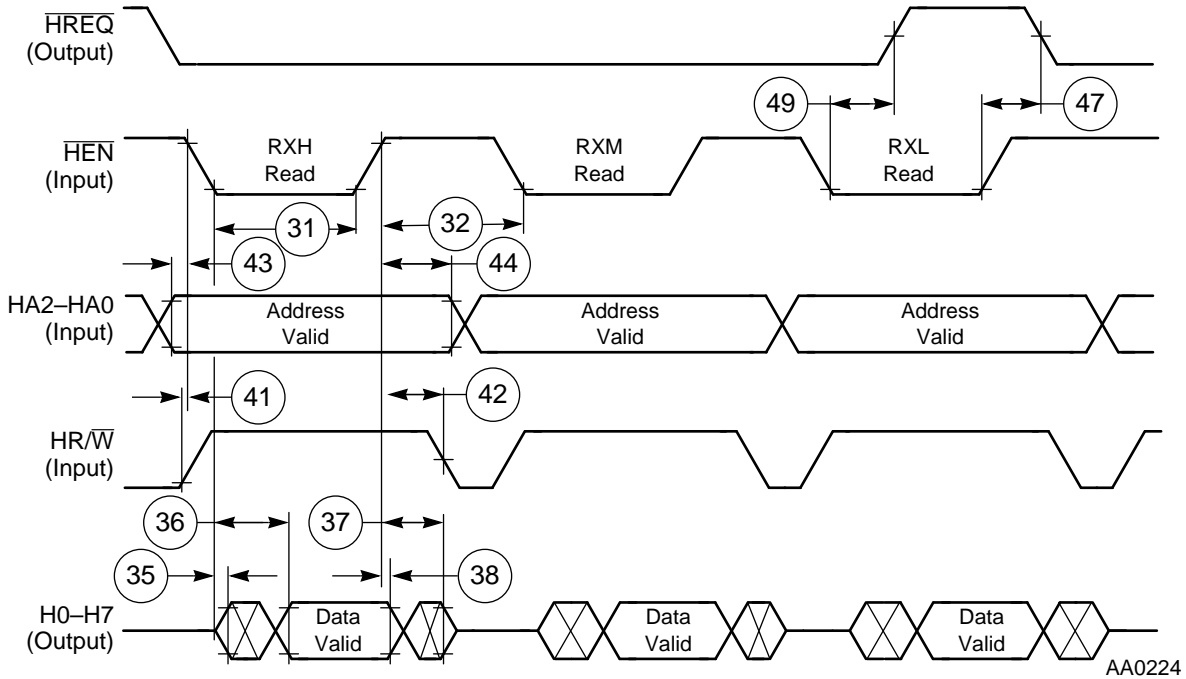
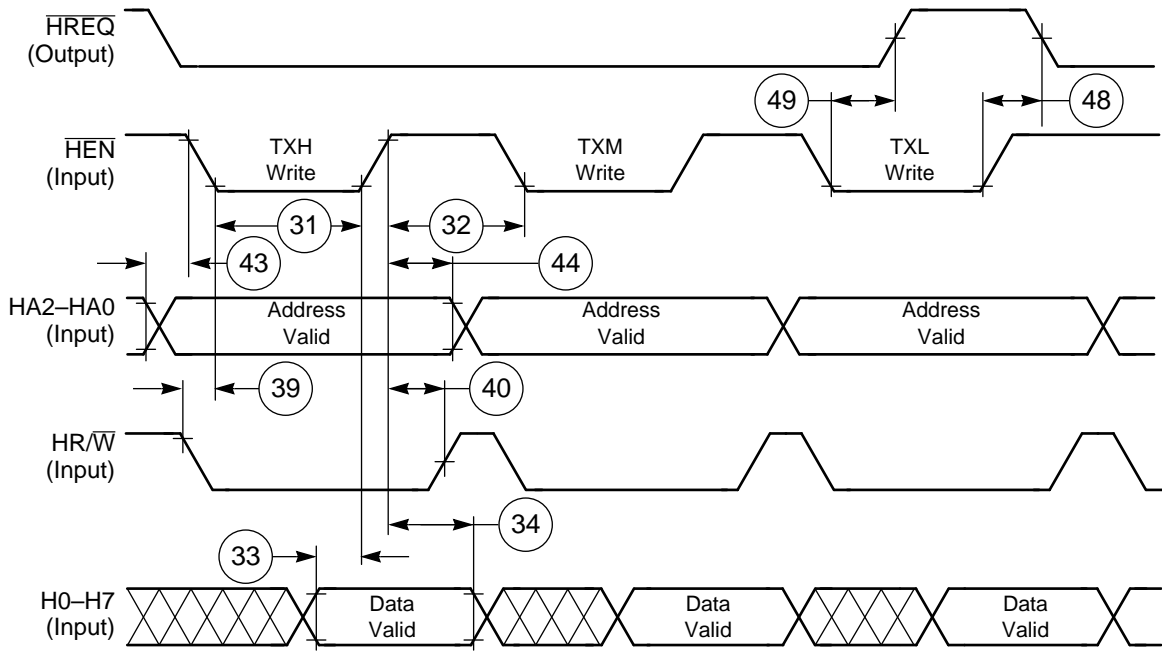
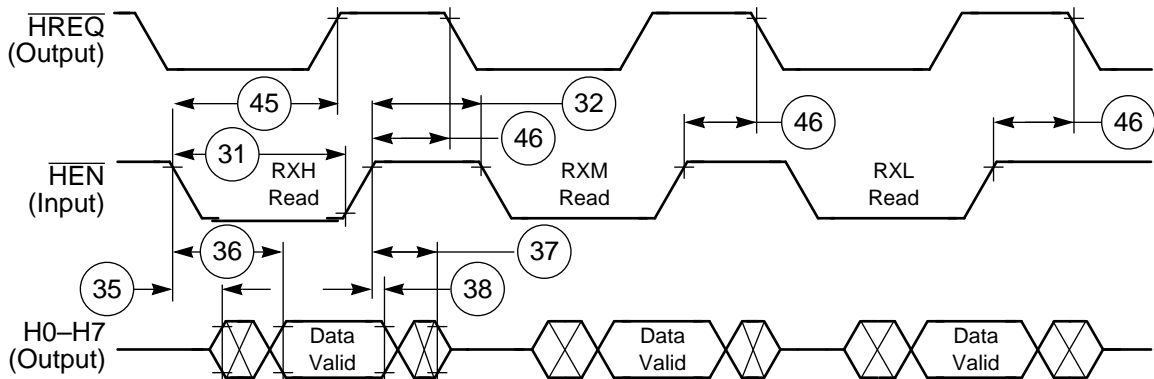


Figure 2-13 Host Read Cycle (Non-DMA Mode)



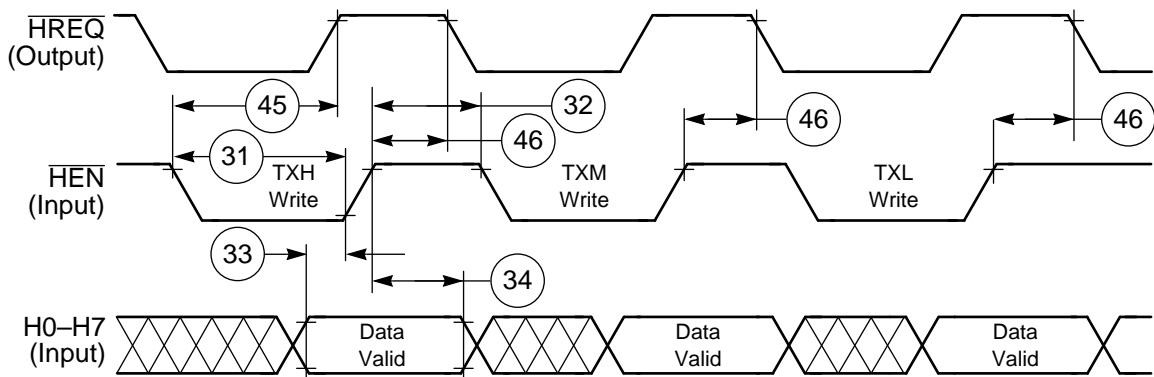
AA0225

Figure 2-14 Host Write Cycle (Non-DMA Mode)



AA0230

Figure 2-15 Host DMA Read Cycle



AA0231

Figure 2-16 Host DMA Write Cycle

SERIAL COMMUNICATION INTERFACE (SCI) TIMING

$V_{CC} = 5.0\text{ V} \pm 10\%$ for 27 MHz; $5.0\text{ V} \pm 5\%$ for 33 MHz;

$T_J = -40$ to $105\text{ }^\circ\text{C}$; $C_L = 50\text{ pF} + 1\text{ TTL loads}$

t_{SCC} = Synchronous Clock Cycle Time (For internal clock, t_{SCC} is determined by the SCI Clock Control Register and T_C .) The minimum t_{SCC} value is $8 \times T_C$.

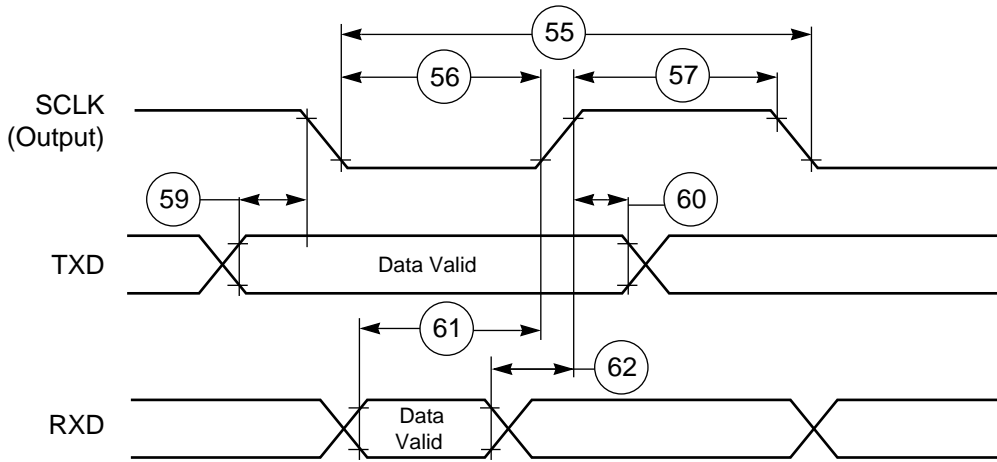
Table 2-10 SCI Synchronous Mode Timing (27/33 MHz)

| Num | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|-----------------------------------------------------------------|---------------------------|--------------------------|---------------------------|--------------------------|------|
| | | Min | Max | Min | Max | |
| 55 | Synchronous Clock Cycle— t_{SCC} | $8 \times T_C$ | — | $8 \times T_C$ | — | ns |
| 56 | Clock Low Period | $4 \times T_C - 15$ | — | $4 \times T_C - 13$ | — | ns |
| 57 | Clock High Period | $4 \times T_C - 15$ | — | $4 \times T_C - 13$ | — | ns |
| 58 | < intentionally blank > | — | — | — | — | — |
| 59 | Output Data Setup to Clock Falling Edge (Internal Clock) | $2 \times T_C + T_L - 39$ | — | $2 \times T_C + T_L - 31$ | — | ns |
| 60 | Output Data Hold After Clock Rising Edge (Internal Clock) | $2 \times T_C - T_L - 11$ | — | $2 \times T_C - T_L - 9$ | — | ns |
| 61 | Input Data Setup Time Before Clock Rising Edge (Internal Clock) | $2 \times T_C + T_L + 35$ | — | $2 \times T_C + T_L + 28$ | — | ns |
| 62 | Input Data Not Valid Before Clock Rising Edge (Internal Clock) | — | $2 \times T_C + T_L - 8$ | — | $2 \times T_C + T_L - 6$ | ns |
| 63 | Clock Falling Edge to Output Data Valid (External Clock) | — | 48 | — | 39 | ns |
| 64 | Output Data Hold After Clock Rising Edge (External Clock) | $T_C + 9$ | — | $T_C + 8$ | — | ns |
| 65 | Input Data Setup Time Before Clock Rising Edge (External Clock) | 23 | — | 19 | — | ns |
| 66 | Input Data Hold Time After Clock Rising Edge (External Clock) | 31 | — | 25 | — | ns |

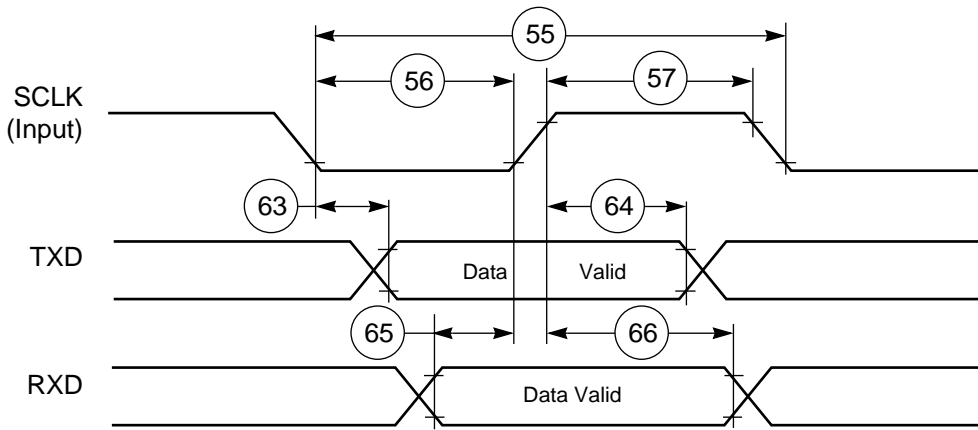
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Table 2-11 SCI Asynchronous Mode Timing — 1X Clock

| Num | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|--------------------------------------------------------------|----------------------|-----|----------------------|-----|------|
| | | Min | Max | Min | Max | |
| 67 | Asynchronous Clock Cycle— t_{ACC} | $64 \times T_C$ | — | $64 \times T_C$ | — | ns |
| 68 | Clock Low Period | $32 \times T_C - 15$ | — | $32 \times T_C - 13$ | — | ns |
| 69 | Clock High Period | $32 \times T_C - 15$ | — | $32 \times T_C - 13$ | — | ns |
| 70 | < intentionally blank > | — | — | — | — | — |
| 71 | Output Data Setup to Clock Rising Edge (Internal Clock) | $32 \times T_C - 77$ | — | $32 \times T_C - 61$ | — | ns |
| 72 | Output Data Hold After Clock Rising Edge (Internal Clock) | $32 \times T_C - 77$ | — | $32 \times T_C - 61$ | — | ns |



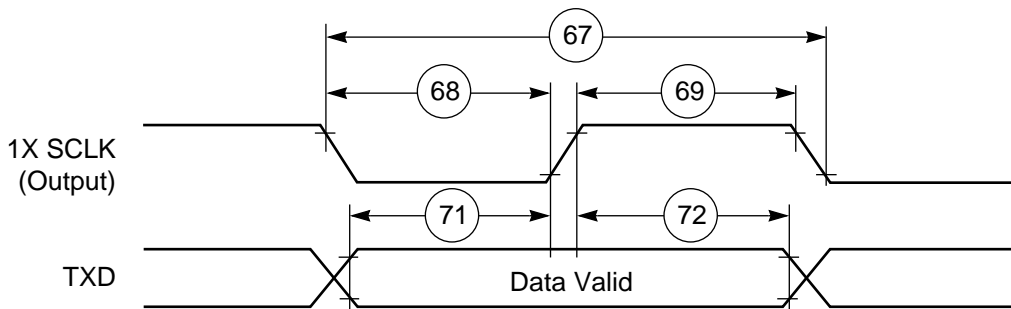
a) Internal Clock



b) External Clock

AA0892

Figure 2-17 SCI Synchronous Mode Timing



Note: In the Wired-OR mode, TXD can be pulled up by 1 kΩ.

AA0893

Figure 2-18 SCI Asynchronous Mode Timing

SYNCHRONOUS SERIAL INTERFACE (SSI) TIMING

$V_{CC} = 5.0\text{ V} \pm 10\%$ for 27 MHz; $V_{CC} = 5.0\text{ V} \pm 5\%$ for 33 MHz;
 $T_J = -40\text{ to }105^\circ\text{ C}$; $C_L = 50\text{ pF} + 2\text{ TTL loads}$

- t_{SSICC} = SSI clock cycle time
- TXC (SCK Pin) = Transmit Clock
- RXC (SC0 or SCK Pin) = Receive Clock
- FST (SC2 Pin) = Transmit Frame Sync
- FSR (SC1 or SC2 Pin) = Receive Frame Sync
- i ck = Internal Clock
- x ck = External Clock
- g ck = Gated Clock
- i ck a = Internal Clock, Asynchronous mode (Asynchronous implies that STD and SRD are two different clocks)
- i ck s = Internal Clock, Synchronous mode (Synchronous implies that STD and SRD are the same clock)
- bl = bit length
- wl = word length

Table 2-12 SSI Timing

| Num | Characteristics | 27 MHz | | 33 MHz | | Case | Unit |
|-----|---------------------------------------------------------|---------------------|-----|---------------------|-----|----------------|------|
| | | Min | Max | Min | Max | | |
| 80 | Clock Cycle— t_{SSICC} (See Note 1) | $4 \times T_C$ | — | $4 \times T_C$ | — | — | ns |
| 81 | Clock High Period | $4 \times T_C - 15$ | — | $4 \times T_C - 13$ | — | — | ns |
| 82 | Clock Low Period | $4 \times T_C - 15$ | — | $4 \times T_C - 13$ | — | — | ns |
| 84 | SRD Rising Edge to FSR Out (bl) High | — | 61 | — | 48 | x ck i ck a | ns |
| | | — | 38 | — | 31 | | ns |
| 85 | SRD Rising Edge to FSR Out (bl) Low | — | 54 | — | 43 | xck i ck a | ns |
| | | — | 31 | — | 25 | | ns |
| 86 | SRD Rising Edge to FSR Out (wl) High | — | 54 | — | 43 | x ck i ck a | ns |
| | | — | 31 | — | 25 | | ns |
| 87 | RXC Rising Edge to FSR Out (wl) Low | — | 54 | — | 43 | x ck i ck a | ns |
| | | — | 31 | — | 25 | | ns |
| 88 | Data In Setup Time Before RXC (SCK in Synchronous Mode) | 12 | — | 10 | — | x ck i ck a | ns |
| | | 27 | — | 22 | — | | ns |
| | Falling Edge | 19 | — | 16 | — | i ck s | ns |

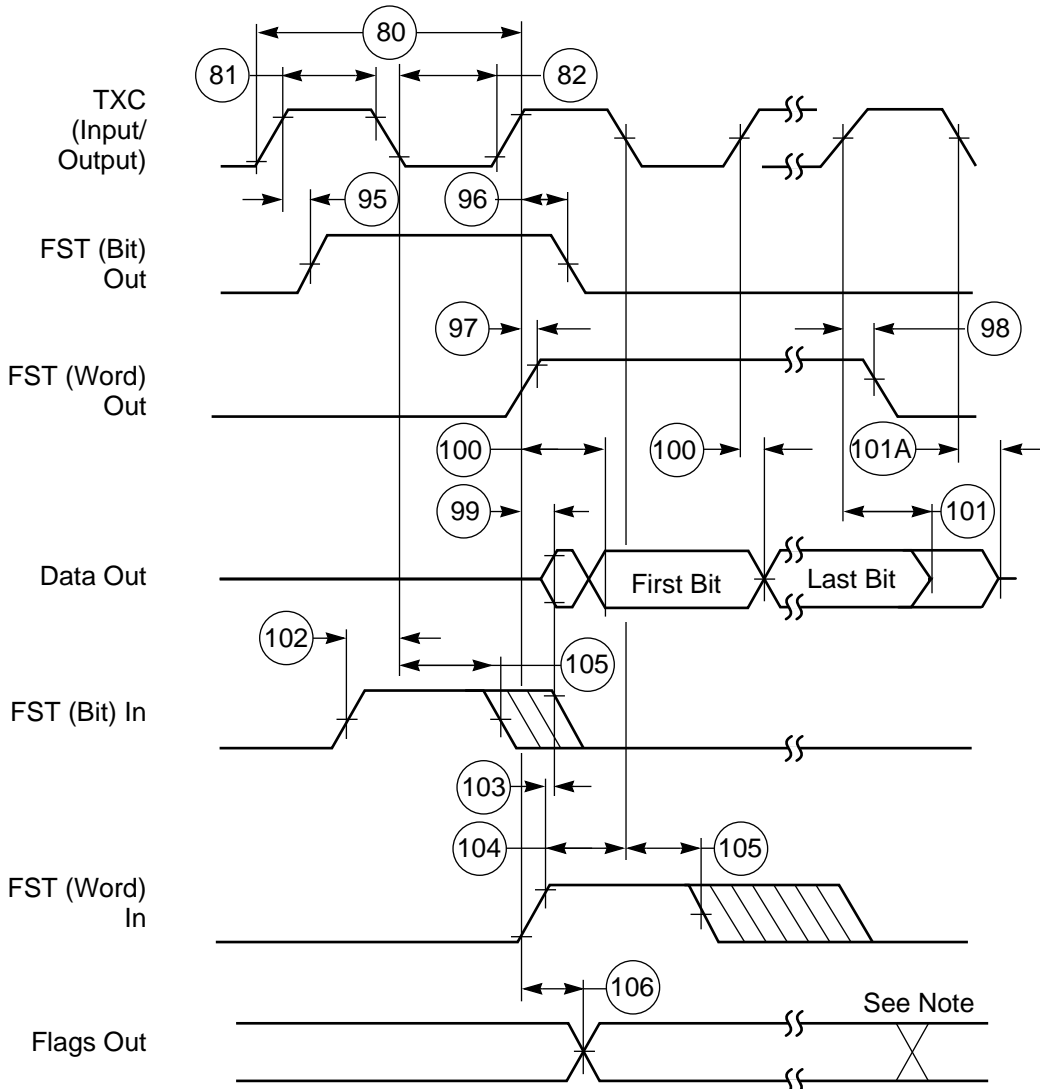
Table 2-12 SSI Timing (Continued)

| Num | Characteristics | 27 MHz | | 33 MHz | | Case | Unit |
|------|----------------------------------------------------------|----------|-------------|----------|-------------|----------------|----------|
| | | Min | Max | Min | Max | | |
| 89 | Data In Hold Time After RXC Falling Edge | 27 4 | — — | 22 4 | — — | x ck i ck | ns ns |
| 90 | FSR Input (bl) High Before RXC Falling Edge | 12 27 | — — | 10 23 | — — | x ck i ck a | ns ns |
| 91 | FSR Input (wl) High Before RXC Falling Edge | 15 42 | — — | 13 34 | — — | x ck i ck a | ns ns |
| 92 | FSR Input Hold Time After RXC Falling Edge | 27 4 | — — | 22 4 | — — | x ck i ck | ns ns |
| 93 | Flags Input Setup Before RXC Falling Edge | 23 39 | — — | 19 31 | — — | x ck i ck s | ns ns |
| 94 | Flags Input Hold Time After RXC Falling Edge | 27 4 | — — | 22 4 | — — | x ck i ck s | ns ns |
| 95 | TXC Rising Edge to FST Out (bl) High | — — | 54 23 | — — | 43 19 | x ck i ck | ns ns |
| 96 | TXC Rising Edge to FST Out (bl) Low | — — | 50 27 | — — | 40 22 | x ck i ck | ns ns |
| 97 | TXC Rising Edge to FST Out (wl) High | — — | 50 27 | — — | 40 22 | x ck i ck | ns ns |
| 98 | TXC Rising Edge to FST Out (wl) Low | — — | 50 27 | — — | 40 22 | x ck i ck | ns ns |
| 99 | TXC Rising Edge to Data Out Enable from High Impedance | — | 50 31 | — | 40 25 | x ck i ck | ns ns |
| 100 | TXC Rising Edge to Data Out Valid | — | 50 31 | — | 40 25 | x ck i ck | ns ns |
| 101 | TXC Rising Edge to Data Out High Impedance (See Note 2) | — — | 54 31 | — — | 43 25 | x ck i ck | ns ns |
| 101A | TXC Falling Edge to Data Out High Impedance (See Note 2) | — | $T_C + T_H$ | — | $T_C + T_H$ | g ck | ns |

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Table 2-12 SSI Timing (Continued)

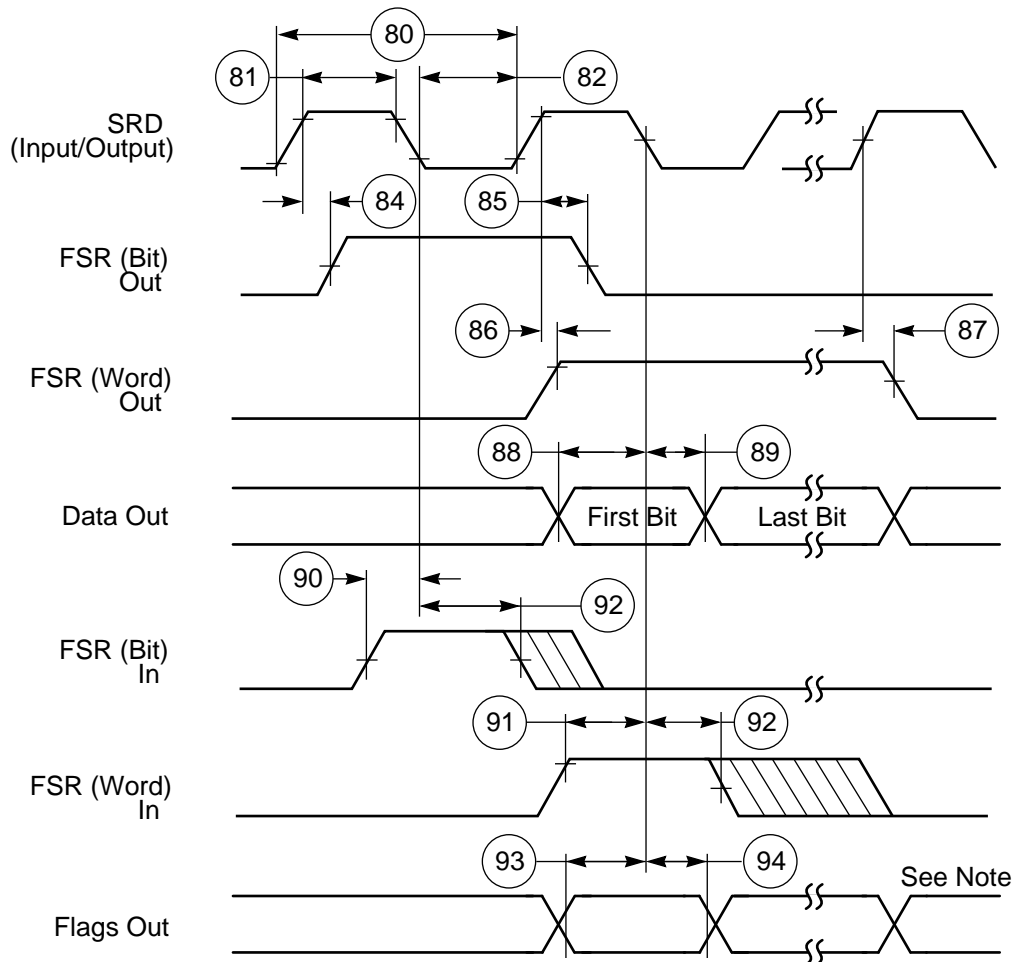
| Num | Characteristics | 27 MHz | | 33 MHz | | Case | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|----------|----------|----------|----------|--------------|----------|
| | | Min | Max | Min | Max | | |
| 102 | FST Input (bl) Setup Time Before TXC Falling Edge | 12 27 | — | 10 23 | — | x ck i ck | ns ns |
| 103 | FST Input (wl) to Data Out Enable from High Impedance | — | 46 | — | 37 | | ns |
| 104 | FST Input (wl) Setup Time Before TXC Falling Edge | 15 42 | — — | 13 34 | — — | x ck i ck | ns ns |
| 105 | FST Input Hold Time After TXC Falling Edge | 27 4 | — — | 22 4 | — — | x ck i ck | ns ns |
| 106 | Flag Output Valid After TXC Rising Edge | — — | 54 31 | — — | 43 25 | x ck i ck | ns ns |
| Note: 1. For internal clock, External Clock Cycle is defined by I_{cyc} and SSI control register. 2. Periodically sampled and not 100% tested | | | | | | | |



Note: In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

AA0894

Figure 2-19 SSI Transmitter Timing



Note: In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

AA0895

Figure 2-20 SSI Receiver Timing

EXTERNAL BUS ASYNCHRONOUS TIMING

$V_{CC} = 5.0\text{ V} \pm 10\%$ for 27 MHz; $V_{CC} = 5.0\text{ V} \pm 5\%$ for 33 MHz;

$T_J = -40\text{ to }105\text{ }^\circ\text{C}$; $C_L = 50\text{ pF} + 1\text{ TTL loads}$

WS = Number of Wait States, as determined by BCR (WS = 0 to 15)

Capacitance Derating: The DSP56001A external bus timing specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the external bus pins (A0-A15, D0-D23, \overline{PS} , \overline{DS} , \overline{RD} , \overline{WR} , X/Y) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins (HI, SCI, SSI) derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active low lines should be pulled up in a manner consistent with the AC and DC specifications.

Table 2-13 External Bus Asynchronous Timing

| No. | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|------------------------------------------------------------------------------------------|--------------------------|----------------------------------------------------|--------------------------|----------------------------------------------------|------|
| | | Min | Max | Min | Max | |
| 115 | Delay from \overline{BR} Assertion to \overline{BG} Assertion | | | | | |
| | • With no external access from the DSP | $2 \times T_C + T_H$ | $4 \times T_C + T_H + 15$ | $2 \times T_C + T_H$ | $4 \times T_C + T_H + 13$ | ns |
| | • During external read or write access | $T_C + T_H$ | $4 \times T_C + T_H + T_C \times WS + 15$ | $T_C + T_H$ | $4 \times T_C + T_H + T_C \times WS + 13$ | ns |
| | • During external read-modify-write access | $T_C + T_H$ | $6 \times T_C + T_H + 2 \times T_C \times WS + 15$ | $T_C + T_H$ | $6 \times T_C + T_H + 2 \times T_C \times WS + 13$ | ns |
| | • During Stop mode—external bus will not be released and \overline{BG} will not go low | — | — | — | — | ns |
| | • During Wait mode | $T_H + 3$ | $T_C + T_H + 23$ | $T_H + 3$ | $T_C + T_H + 19$ | ns |
| 116 | Delay from \overline{BR} Deassertion to \overline{BG} Deassertion | $2 \times T_C$ | $4 \times T_C + 15$ | $2 \times T_C$ | $4 \times T_C + 13$ | ns |
| 117 | \overline{BG} Deassertion Duration | $2 \times T_C + T_H - 8$ | — | $2 \times T_C + T_H - 6$ | — | ns |
| 118 | Delay from Address, Data, and Control Bus High Impedance to \overline{BG} Assertion | 0 | — | 0 | — | ns |

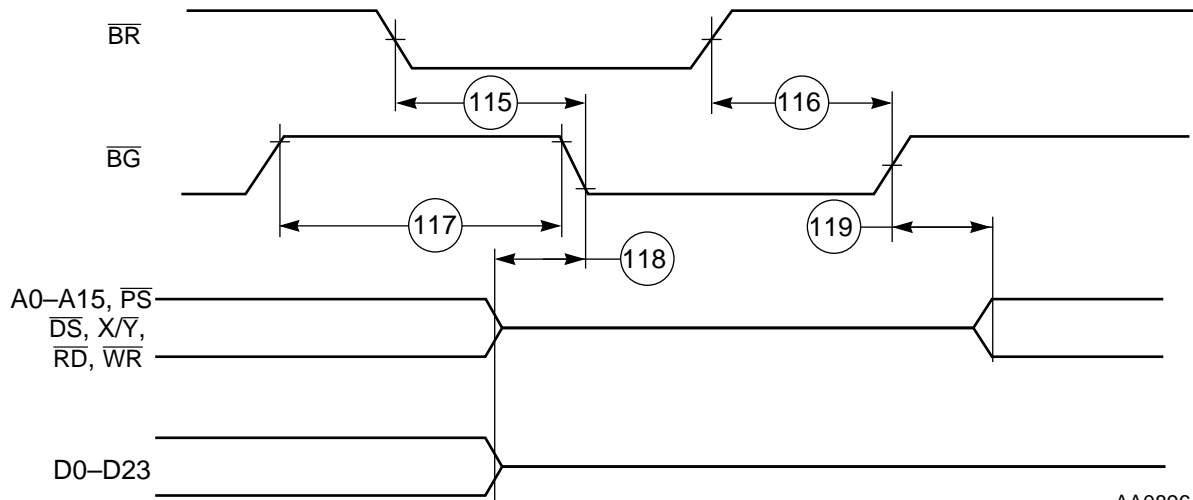
Table 2-13 External Bus Asynchronous Timing (Continued)

| No. | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|------------------------------------------------------------------------------------------------------------------------------|---------------------------------|-----------|---------------------------------|-------------|------|
| | | Min | Max | Min | Max | |
| 119 | Delay from \overline{BG} Deassertion to Address and Control Bus Enabled | 0 | T_{H-8} | 0 | T_{H-6} | ns |
| 120 | Address Valid to \overline{WR} Assertion • $WS = 0$ • $WS > 0$ | $T_L - 7$ | $T_L + 5$ | $T_L - 5.5$ | $T_L + 5$ | ns |
| | | $T_C - 7$ | $T_C + 5$ | $T_C - 5.5$ | $T_C + 5$ | ns |
| 121 | \overline{WR} Assertion Width • $WS = 0$ • $WS > 0$ | $T_C - 7$ | — | $T_C - 5$ | — | ns |
| | | $WS \times T_C + T_L - 7$ | — | $WS \times T_C + T_L - 5$ | — | ns |
| 122 | \overline{WR} Deassertion to Address Not Valid | $T_H - 9$ | — | $T_H - 7.5$ | — | ns |
| 123 | \overline{WR} Assertion to Data Out Active From High Impedance • $WS = 0$ • $WS > 0$ | $T_H - 7$ | $T_H + 8$ | $T_H - 5.5$ | $T_H + 6.5$ | ns |
| | | 0 | 8 | 0 | 6.5 | ns |
| 124 | Data Out Hold Time from \overline{WR} Deassertion (the maximum specification is periodically sampled, and not 100% tested) | $T_H - 7$ | $T_H + 6$ | $T_H - 5.5$ | $T_H + 4.5$ | ns |
| 125 | Data Out Setup Time to \overline{WR} Deassertion • $WS = 0$ • $WS > 0$ | $T_L - 5$ | — | $T_L - 5$ | — | ns |
| | | $WS \times T_C + T_L - 5$ | — | $WS \times T_C + T_L - 5$ | — | ns |
| 126 | \overline{RD} Deassertion to Address Not Valid | $T_H - 7$ | — | $T_H - 5.5$ | — | ns |
| 127 | Address Valid to \overline{RD} Deassertion • $WS = 0$ • $WS > 0$ | $T_C + T_L - 6$ | — | $T_C + T_L - 6$ | — | ns |
| | | $(WS + 1) \times T_C + T_L - 6$ | — | $(WS + 1) \times T_C + T_L - 6$ | — | ns |

Table 2-13 External Bus Asynchronous Timing (Continued)

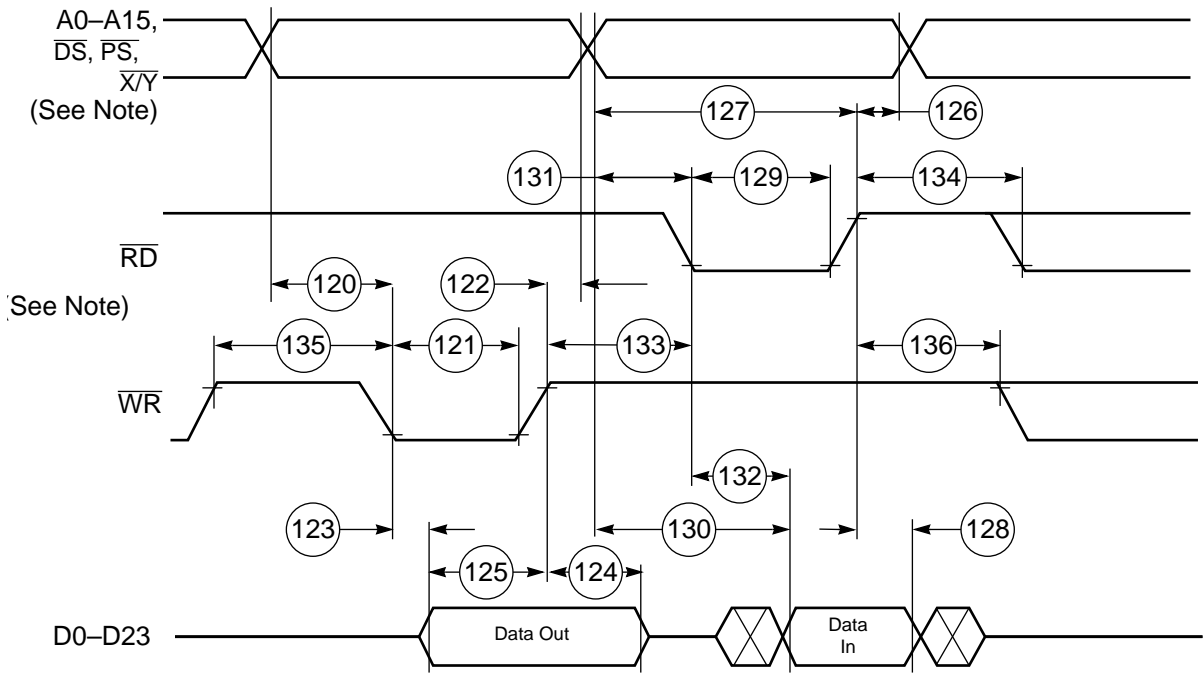
| No. | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|----------------------------------------------------------|---------------------------|----------------------------------|-----------------------------|----------------------------------|------|
| | | Min | Max | Min | Max | |
| 128 | Input Data Hold Time to \overline{RD} Deassertion | 0 | — | 0 | — | ns |
| 129 | \overline{RD} Assertion Width | | | | | |
| | • WS = 0 | $T_C - 7$ | — | $T_C - 5.5$ | — | ns |
| | • WS > 0 | $(WS + 1) \times T_C - 7$ | — | $(WS + 1) \times T_C - 5.5$ | — | ns |
| 130 | Address Valid to Input Data Valid | | | | | |
| | • WS = 0 | — | $T_C + T_L - 14$ | — | $T_C + T_L - 11$ | ns |
| | • WS > 0 | — | $(WS + 1) \times T_C + T_L - 14$ | — | $(WS + 1) \times T_C + T_L - 11$ | ns |
| 131 | Address Valid to \overline{RD} Assertion | $T_L - 7$ | $T_L + 5$ | $T_L - 5.5$ | $T_L + 5$ | ns |
| 132 | \overline{RD} Assertion to Input Data Valid | | | | | |
| | • WS = 0 | — | $T_C - 11$ | — | $T_C - 9$ | ns |
| | • WS > 0 | — | $(WS + 1) \times T_C - 11$ | — | $(WS + 1) \times T_C - 9$ | ns |
| 133 | \overline{WR} Deassertion to \overline{RD} Assertion | $T_C - 12$ | — | $T_C - 10$ | — | ns |
| 134 | \overline{RD} Deassertion to \overline{RD} Assertion | $T_C - 8$ | — | $T_C - 6.5$ | — | ns |
| 135 | \overline{WR} Deassertion to \overline{WR} Assertion | | | | | |
| | • WS = 0 | $T_C - 12$ | — | $T_C - 10$ | — | ns |
| | • WS > 0 | $T_C + T_H - 12$ | — | $T_C + T_H - 10$ | — | ns |
| 136 | \overline{RD} Deassertion to \overline{WR} Assertion | | | | | |
| | • WS = 0 | $T_C - 8$ | — | $T_C - 6.5$ | — | ns |
| | • WS > 0 | $T_C + T_H - 8$ | — | $T_C + T_H - 6.5$ | — | ns |

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Figure 2-21 Bus Request / Bus Grant Timing



Note: During Read-Modify-Write instructions, the address lines do not change state.

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Figure 2-22 External Bus Asynchronous Timing

EXTERNAL BUS SYNCHRONOUS TIMING

$V_{CC} = 5.0\text{ V} \pm 10\%$ for 27 MHz, $V_{CC} = 5.0\text{ Vdc} \pm 5\%$ for 33 MHz,
 $T_j = -40^\circ$ to $+105^\circ\text{ C}$, $C_L = 50\text{ pF} + 1\text{ TTL loads}$

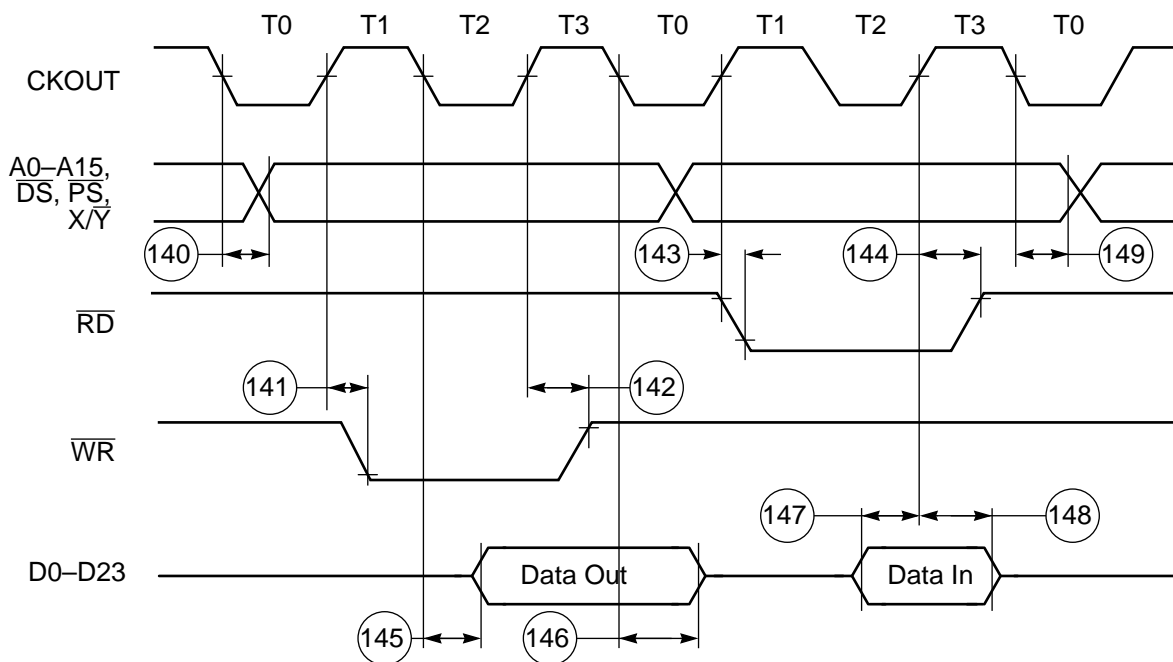
Capacitance Derating: The DSP56001A external bus timing specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the external bus pins (A0–A15, D0–D23, \overline{PS} , \overline{DS} , \overline{RD} , \overline{WR} , X/ \overline{Y}) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins (HI, SCI, SSI) derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active-low lines should be pulled up in a manner consistent with the AC and DC specifications.

Table 2-14 External Bus Synchronous Timing

| Num | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------|--------|------------|------|
| | | Min | Max | Min | Max | |
| 140 | Clk Low transition to Address Valid | — | 19 | — | 19 | ns |
| 141 | Clk High transition to \overline{WR} Assertion(See Note 1, 2) <ul style="list-style-type: none"> • WS=0 • WS>0 | 0 | 17 | 0 | 17 | ns |
| | | 0 | $T_H + 17$ | 0 | $T_H + 17$ | ns |
| 142 | Clk High transition to \overline{WR} Deassertion | 5 | 16 | 5 | 13 | ns |
| 143 | Clk High transition to \overline{RD} Assertion | 0 | 16 | 0 | 16 | ns |
| 144 | Clk High transition to \overline{RD} Deassertion | 3 | 13 | 3 | 10.5 | ns |
| 145 | Clk Low transition to Data-Out Valid | — | 19 | — | 19 | ns |
| 146 | Clk Low transition to Data-Out Invalid (See Note 3) | 4 | — | 3.5 | — | ns |
| 147 | Data-In Valid to Clk High transition (Setup) | 4 | — | 4 | — | ns |
| 148 | Clk High transition to Data-In Invalid (Hold) | 12 | — | 12 | — | ns |
| 149 | Clk Low transition to Address Invalid (See Note 3) | 2 | — | 2 | — | ns |

Table 2-14 External Bus Synchronous Timing (Continued)

| Num | Characteristics | 27 MHz | | 33 MHz | | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--------|-----|--------|-----|------|
| | | Min | Max | Min | Max | |
| Note: 1. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. 2. WS are wait state values specified in the BCR. 3. Clk Low transition to data-out invalid (specification # T146) and Clk Low transition to address invalid (specification # T149) indicate the time after which data/address are no longer guaranteed to be valid. 4. Timings are given from Clk midpoint to V_{OL} or V_{OH} of the corresponding signal(s). | | | | | | |



Note: During Read-Modify-Write Instructions, the address lines do not change states. AA0395

Figure 2-23 Synchronous Bus Timing

BUS STROBE / WAIT TIMING

$V_{CC} = 5.0\text{ V} \pm 10\%$ for 27 MHz; $V_{CC} = 5.0\text{ V} \pm 5\%$ for 33 MHz;
 $T_J = -40\text{ to }105^\circ\text{ C}$; $C_L = 50\text{ pF} + 2\text{ TTL loads}$

Table 2-15 Bus Strobe / Wait Timing

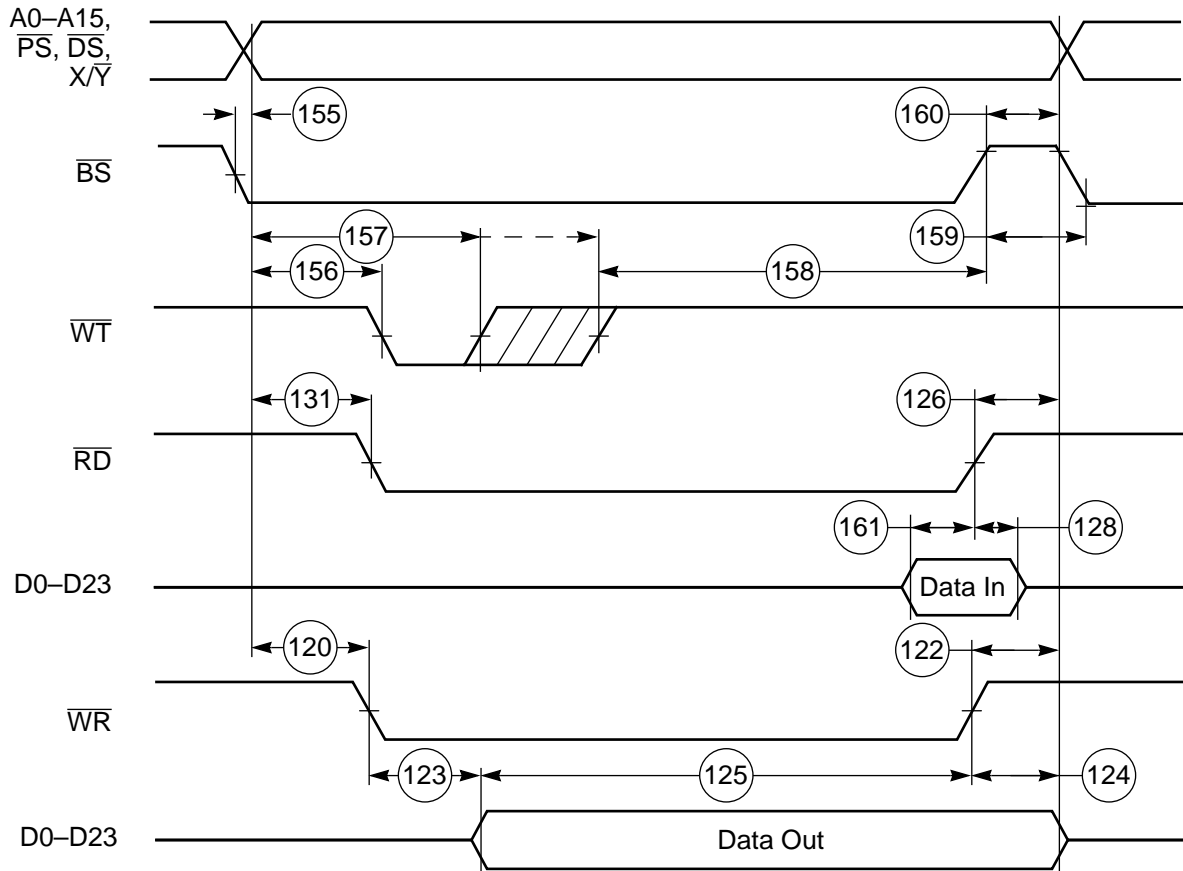
| No. | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|---------------------------|---------------------------|---------------------------|------|
| | | Min | Max | Min | Max | |
| 150 | First CKOUT transition to \overline{BS} Assertion | 3 | 19 | 2.5 | 19 | ns |
| 151 | \overline{WT} Assertion to first CKOUT transition (setup time) | 3 | — | 2.5 | — | ns |
| 152 | First CKOUT transition to \overline{WT} Deassertion for Minimum Timing | 11 | $T_C - 6$ | 12 | $T_C - 5$ | ns |
| 153 | \overline{WT} Deassertion to first CKOUT transition for Maximum Timing (2 wait states) | 6 | — | 5 | — | ns |
| 154 | Second CKOUT transition to \overline{BS} Deassertion | 3 | 20 | 3 | 19 | ns |
| 155 | \overline{BS} Assertion to Address Valid | -2 | 8 | -2 | 6.5 | ns |
| 156 | \overline{BS} Assertion to \overline{WT} Assertion (See Note 1) | 0 | $T_C - 11$ | 0 | $T_C - 10$ | ns |
| 157 | \overline{BS} Assertion to \overline{WT} Deassertion (See Note 1 and Note 3) <ul style="list-style-type: none"> • $WS \leq 2$ • $WS \geq 2$ | T_C | $2 \times T_C - 11$ | $T_C + 4$ | $2 \times T_C - 10$ | ns |
| | | $(WS - 1) \times T_C$ | $WS \times T_C - 11$ | $(WS - 1) \times T_C + 4$ | $WS \times T_C - 10$ | ns |
| 158 | \overline{WT} Deassertion to \overline{BS} Deassertion | $T_C + T_L$ | $2 \times T_C + T_L + 17$ | $T_C + T_L$ | $2 \times T_C + T_L + 15$ | ns |
| 159 | Minimum \overline{BS} Deassertion Width for Consecutive External Accesses | $T_H - 6$ | — | $T_H - 4.5$ | — | ns |
| 160 | \overline{BS} Deassertion to Address Invalid (See Note 2) | $T_H - 8$ | — | $T_H - 6.5$ | — | ns |

Table 2-15 Bus Strobe / Wait Timing (Continued)

| No. | Characteristics | 27 MHz | | 33 MHz | | Unit |
|-----|-------------------------------------------------------|--------|-----|--------|-----|------|
| | | Min | Max | Min | Max | |
| 161 | Data-In Valid to \overline{RD} Deassertion (Set Up) | 12 | — | 10 | — | ns |

Note:

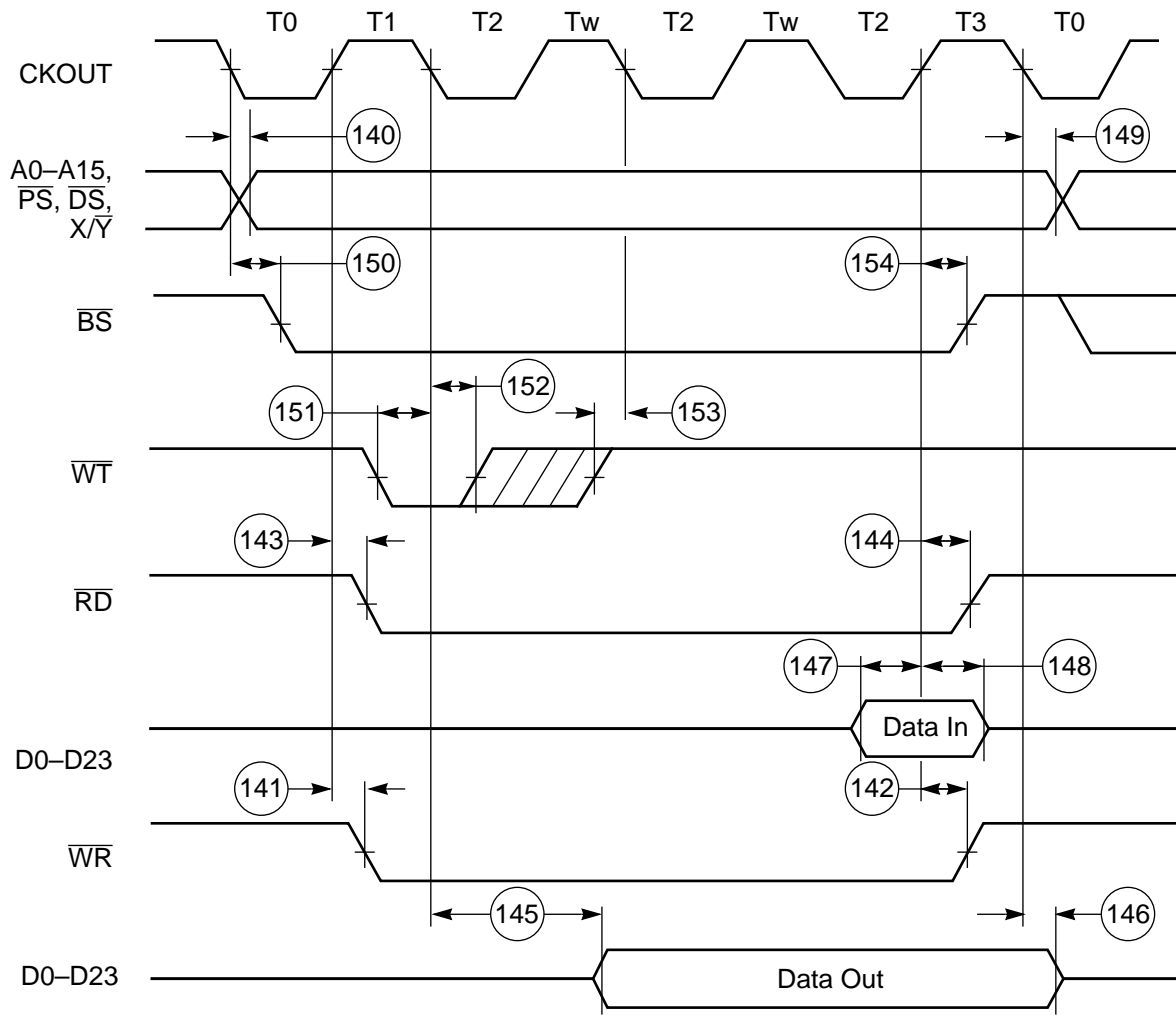
1. If wait states are also inserted using the BCR and if the number of wait states is greater than two, then specification numbers T156 and T157 can be increased accordingly.
2. \overline{BS} deassertion to address invalid indicates the time after which the address are no longer guaranteed to be valid.
3. The minimum number of wait states when using $\overline{BS}/\overline{WT}$ is two (2).
4. For read-modify-write instructions, the address lines will not change states between the read and the write cycle. However, \overline{BS} will deassert before asserting again for the write cycle. If wait states are desired for each of the read and write cycle, the \overline{WT} pin must be asserted once for each cycle.



Note: During Read-Modify-Write instructions, the address lines do not change state. However, \overline{BS} will deassert before asserting again for the write cycle.

AA0398

Figure 2-24 Asynchronous $\overline{BS} / \overline{WT}$ Timings



Note: During Read-Modify-Write Instructions, the address lines do not change state. However, \overline{BS} will deassert before asserting again for the write cycle.

AA0397

Figure 2-25 Synchronous \overline{BS} / \overline{WT} Timings



SECTION 3

PACKAGING

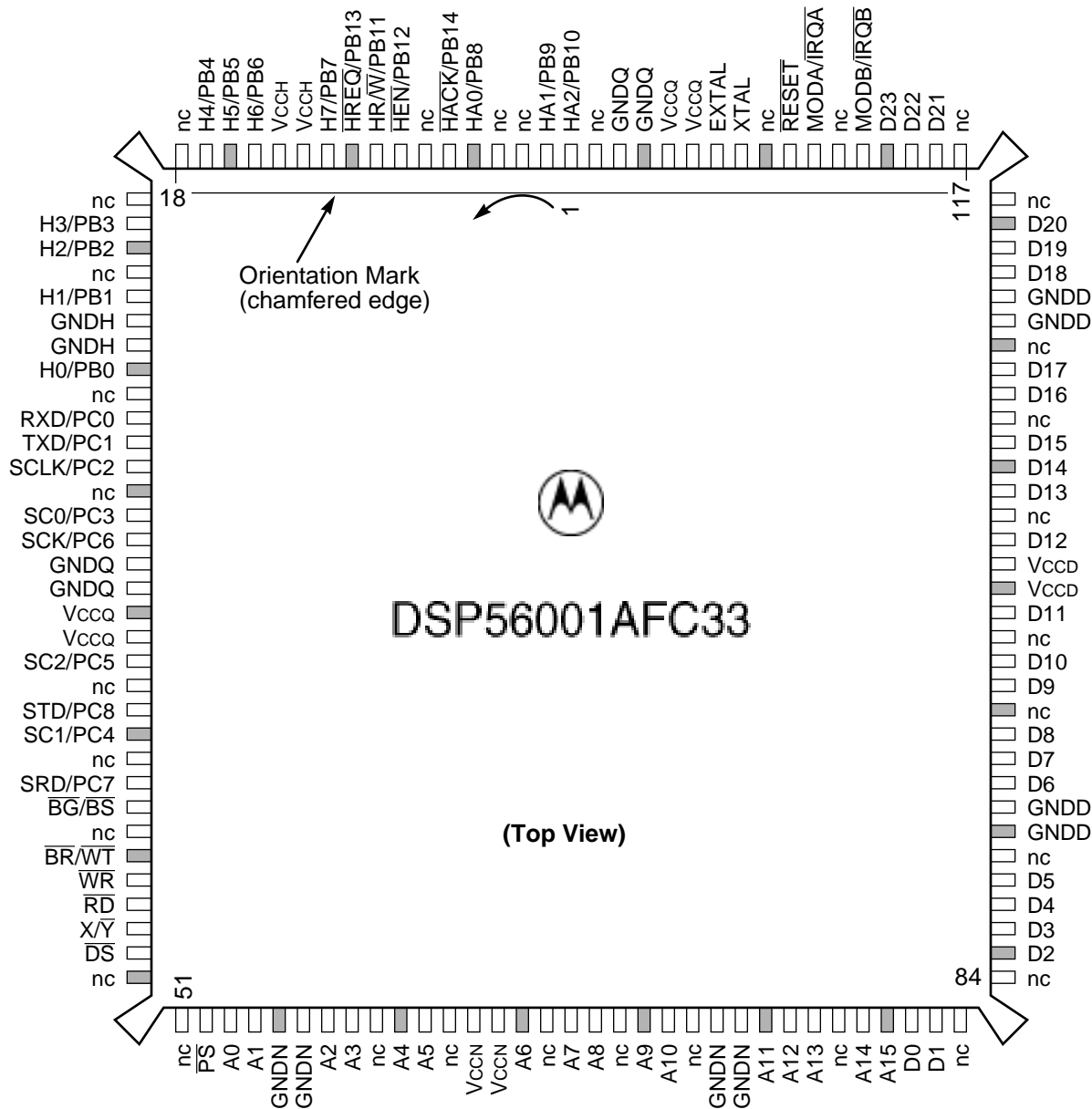
PIN-OUT AND PACKAGE INFORMATION

This section supplies information about the packages which are available for this product. Diagrams of the pinouts of each package are included, and tables describing the pins allocated to each of the signals described in **Table 3-1** through **Table 3-5**.

The DSP56001A is available in 3 packages:

- 132-pin plastic quad flat pack (PQFP), type 'FC'
- 132-pin ceramic quad flat pack (CQFP), type 'FE'
- 88-pin Pin Grid Array (PGA), type 'RC'

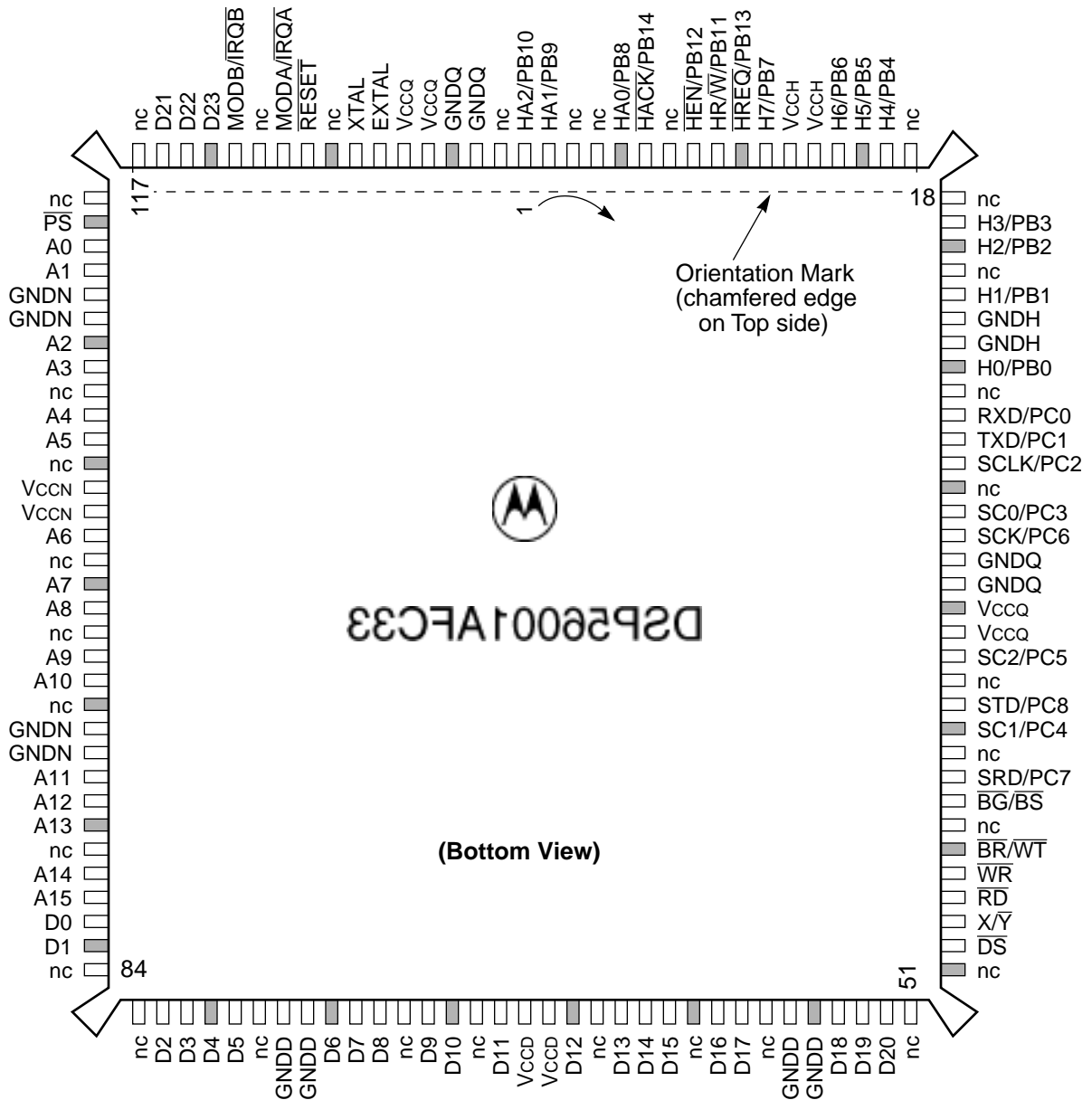
Top and bottom views of the each package are shown, together with their pin-outs.



- Note:
1. "nc" are no connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
 2. An $\overline{\text{O}}$ VERBAR indicates the signal is asserted when the voltage = ground (active low).
 3. To simplify locating the pins, each fifth pin is shaded in the illustration.

AA0898

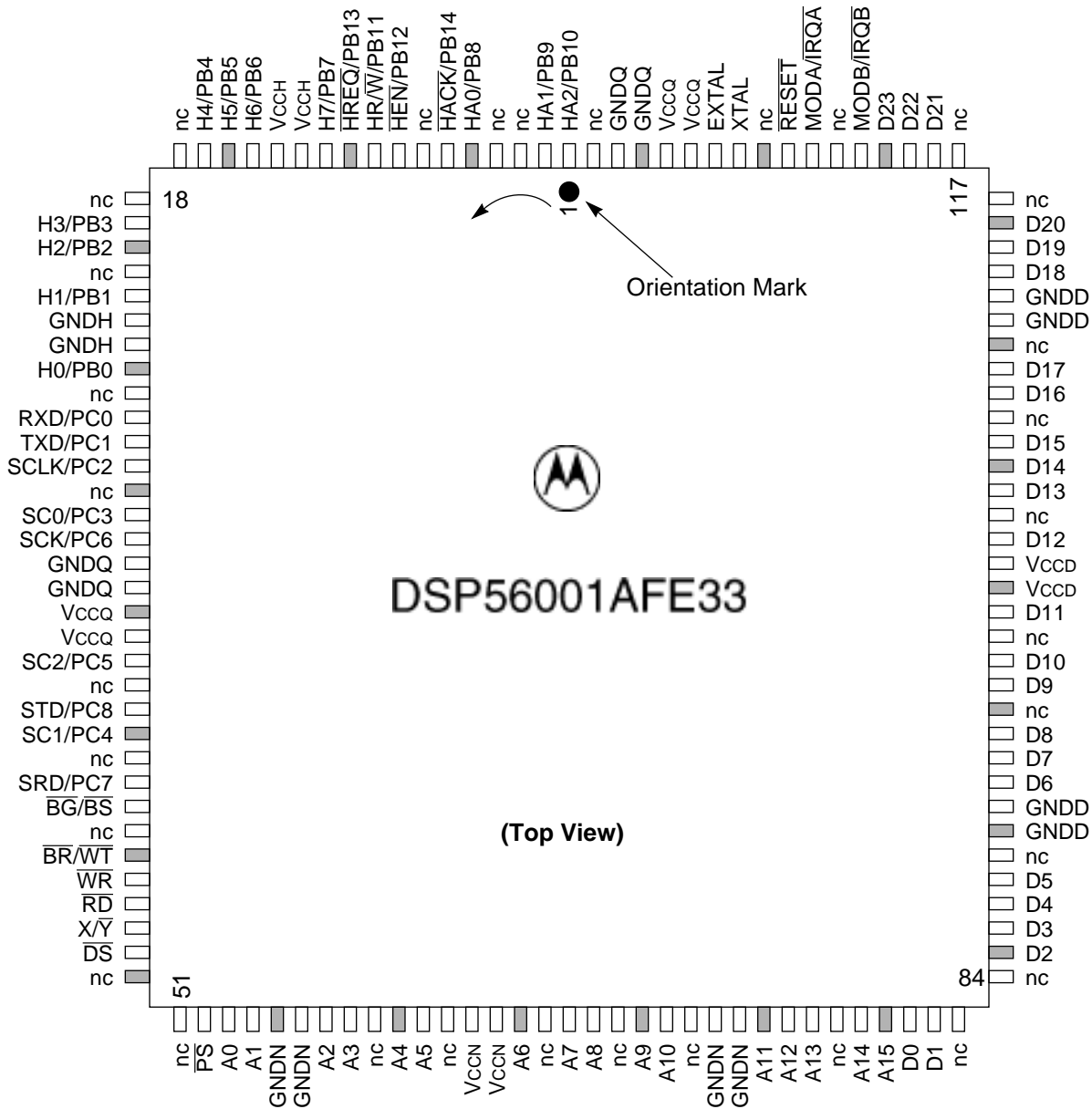
Figure 3-1 Top View of the 132-pin Plastic (FC) Quad Flat Package



- Note:
1. "nc" are no connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
 2. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).
 3. To simplify locating the pins, each fifth pin is shaded in the illustration.

AA0899

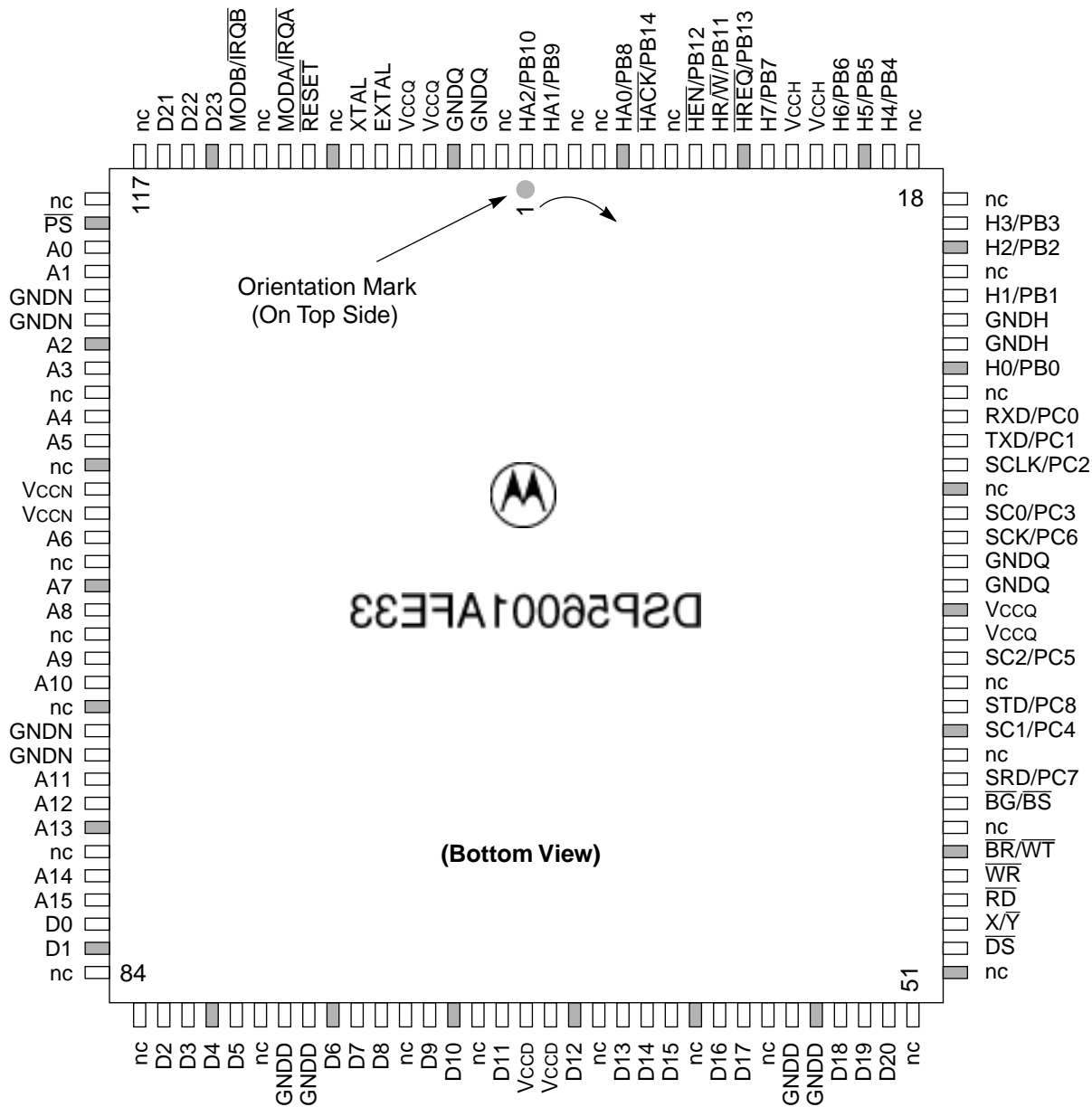
Figure 3-2 Bottom View of the 132-pin Plastic (FC) Quad Flat Package



- Note: 1. "nc" are no connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
 2. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).
 3. To simplify locating the pins, each fifth pin is shaded in the illustration.

AA0900

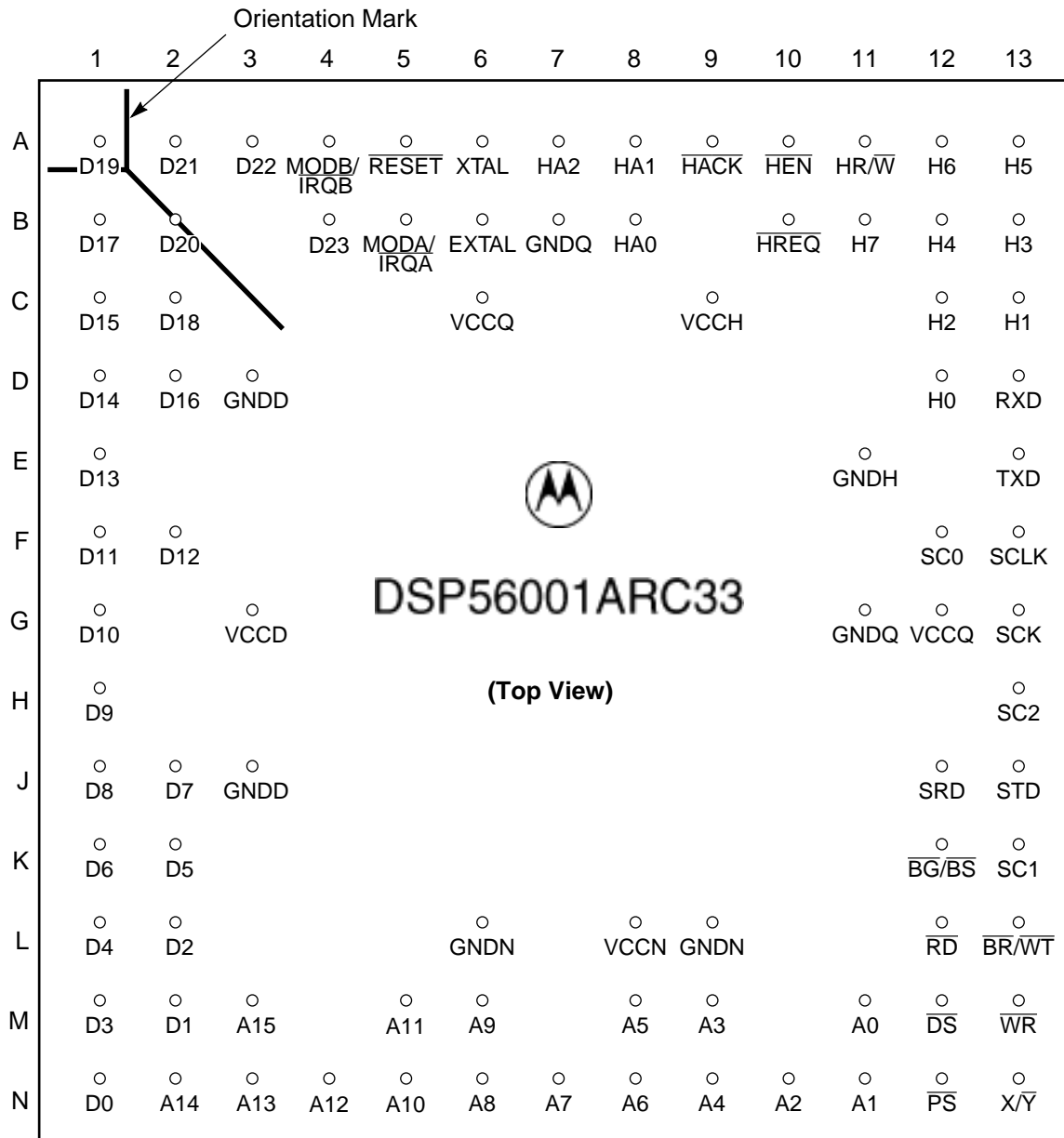
Figure 3-3 Top View of the 132-pin Ceramic (FE) Quad Flat Package



- Note:
1. "nc" are no connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
 2. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).
 3. To simplify locating the pins, each fifth pin is shaded in the illustration.

AA0901

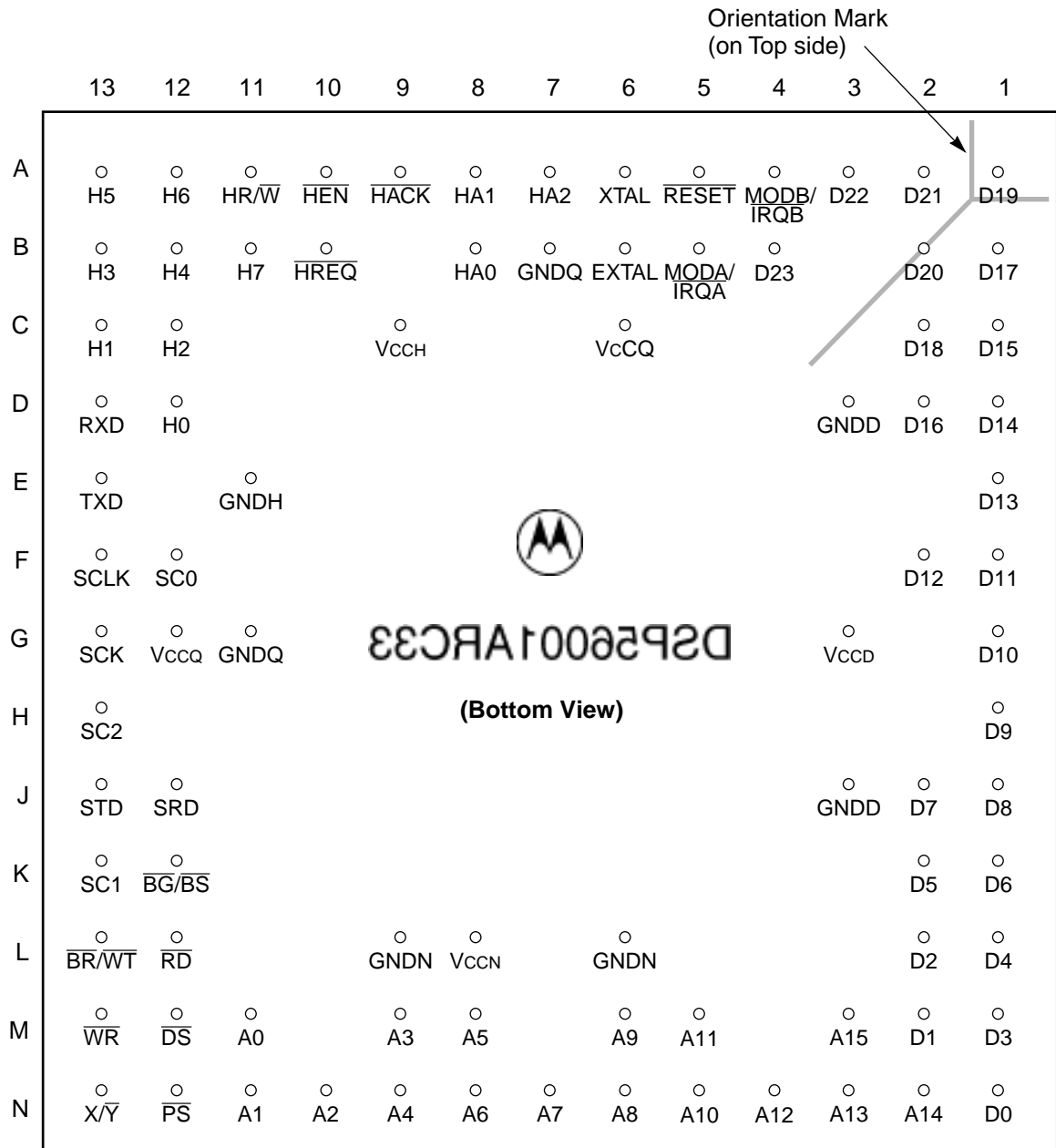
Figure 3-4 Bottom View of the 132-pin Ceramic (FE) Quad Flat Package



- Note:
1. "nc" are no connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
 2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).
 3. To simplify locating the pins, each fifth pin is shaded in the illustration.

AA0902

Figure 3-5 Top View of the 88-pin Ceramic (RC) Pin Grid Array Package



- Note:
1. "nc" are no connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
 2. An $\overline{\text{O}}$ VERBAR indicates the signal is asserted when the voltage = ground (active low).
 3. To simplify locating the pins, each fifth pin is shaded in the illustration.
- AA0903

Figure 3-6 Bottom View of the 88-pin Ceramic (RC) Pin Grid Array Package

The DSP56001A signals that may be programmed as General Purpose I/O are listed with their primary function in **Table 3-1**.

Table 3-1 DSP56001A General Purpose I/O Pin Identification

| Pin Number 132 pin "FC" PQFP "FE" CQFP | Pin Number 88 pin "RC" PGA | Primary Function | Port | GPIO ID |
|-------------------------------------------------|----------------------------------|---------------------|------|---------|
| 25 | D12 | H0 | B | PB0 |
| 22 | C13 | H1 | | PB1 |
| 20 | C12 | H2 | | PB2 |
| 19 | B13 | H3 | | PB3 |
| 16 | B12 | H4 | | PB4 |
| 15 | A13 | H5 | | PB5 |
| 14 | A12 | H6 | | PB6 |
| 11 | B11 | H7 | | PB7 |
| 5 | B8 | HA0 | | PB8 |
| 2 | A8 | HA1 | | PB9 |
| 1 | A7 | HA2 | | PB10 |
| 9 | A11 | HR/ \overline{W} | | PB11 |
| 8 | A10 | \overline{HEN} | | PB12 |
| 10 | B10 | \overline{HREQ} | | PB13 |
| 6 | A9 | HACK | PB14 | |

Table 3-1 DSP56001A General Purpose I/O Pin Identification

| Pin Number 132 pin "FC" PQFP "FE" CQFP | Pin Number 88 pin "RC" PGA | Primary Function | Port | GPIO ID |
|-------------------------------------------------|----------------------------------|---------------------|------|---------|
| 27 | D13 | RXD | C | PC0 |
| 28 | E13 | TXD | | PC1 |
| 29 | F13 | SCLK | | PC2 |
| 31 | F12 | SC0 | | PC3 |
| 40 | K13 | SC1 | | PC4 |
| 37 | H13 | SC2 | | PC5 |
| 32 | G13 | SCK | | PC6 |
| 42 | J12 | SRD | | PC7 |
| 39 | J13 | STD | | PC8 |

Table 3-2 DSP56001A Signal Identification by Pin Number — PGA

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---------|---------------------------------|---------|-------------|---------|---------------------------|
| A1 | D19 | D1 | D14 | L6 | GNDN |
| A2 | D21 | D2 | D16 | L8 | VCCN |
| A3 | D22 | D3 | GNDD | L9 | GNDN |
| A4 | MODB/ $\overline{\text{IRQB}}$ | D12 | H0/PB0 | L12 | $\overline{\text{RD}}$ |
| A5 | $\overline{\text{RESET}}$ | D13 | RXD/PC0 | L13 | $\overline{\text{BR/WT}}$ |
| A6 | XTAL | E1 | D13 | M1 | D3 |
| A7 | HA2/PB10 | E11 | GNDH | M2 | D1 |
| A8 | HA1/PB9 | E13 | TXD/PC1 | M3 | A15 |
| A9 | $\overline{\text{HACK}}$ /PB14 | F1 | D11 | M5 | A11 |
| A10 | $\overline{\text{HEN}}$ /PB12 | F2 | D12 | M6 | A9 |
| A11 | HR/ $\overline{\text{W}}$ /PB11 | F12 | SC0/PC3 | M8 | A5 |

Table 3-2 DSP56001A Signal Identification by Pin Number — PGA

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---------|-------------------------|---------|-------------------------------|---------|-------------------|
| A12 | H6/PB6 | F13 | SCLK/PC2 | M9 | A3 |
| A13 | H5/PB5 | G1 | D10 | M11 | A0 |
| B1 | D17 | G3 | VCCD | M12 | \overline{DS} |
| B2 | D20 | G11 | GNDQ | M13 | \overline{WR} |
| B4 | D23 | G12 | VCCQ | N1 | D0 |
| B5 | MODA/ \overline{IRQA} | G13 | SCK/PC6 | N2 | A14 |
| B6 | EXTAL | H1 | D9 | N3 | A13 |
| B7 | GNDQ | H13 | SC2/PC5 | N4 | A12 |
| B8 | HA0/PB8 | J1 | D8 | N5 | A10 |
| B10 | \overline{HREQ} /PB13 | J2 | D7 | N6 | A8 |
| B11 | H7/PB7 | J3 | GNDD | N7 | A7 |
| B12 | H4/PB4 | J12 | SRD/PC7 | N8 | A6 |
| B13 | H3/PB3 | J13 | STD/PC8 | N9 | A4 |
| C1 | D15 | K1 | D6 | N10 | A2 |
| C2 | D18 | K2 | D5 | N11 | A1 |
| C6 | VCCQ | K12 | $\overline{BG}/\overline{BS}$ | N12 | \overline{PS} |
| C9 | VcCH | K13 | SC1/PC4 | N13 | X/ \overline{Y} |
| C12 | H2/PB2 | L1 | D4 | — | — |
| C13 | H1/PB1 | L2 | D2 | — | — |

Table 3-3 DSP56001A Signal Identification by Pin Number —PQFP & CQFP

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---------|--------------------------|---------|-------------------------------|---------|-----------------|
| 1 | HA2/PB10 | 26 | nc | 51 | nc |
| 2 | HA1/PB9 | 27 | RXD/PC0 | 52 | \overline{PS} |
| 3 | nc | 28 | TXD/PC1 | 53 | A0 |
| 4 | nc | 29 | SCLK/PC2 | 54 | A1 |
| 5 | HA0/PB8 | 30 | nc | 55 | GNDN |
| 6 | \overline{HACK} /PB14 | 31 | SC0/PC3 | 56 | GNDN |
| 7 | nc | 32 | SCK/PC6 | 57 | A2 |
| 8 | \overline{HEN} /PB12 | 33 | GNDQ | 58 | A3 |
| 9 | HR/ \overline{W} /PB11 | 34 | GNDQ | 59 | nc |
| 10 | \overline{HREQ} /PB13 | 35 | VCCQ | 60 | A4 |
| 11 | H7/PB7 | 36 | VCCQ | 61 | A5 |
| 12 | VcCH | 37 | SC2/PC5 | 62 | nc |
| 13 | VcCH | 38 | nc | 63 | VCCN |
| 14 | H6/PB6 | 39 | STD/PC8 | 64 | VCCN |
| 15 | H5/PB5 | 40 | SC1/PC4 | 65 | A6 |
| 16 | H4/PB4 | 41 | nc | 66 | nc |
| 17 | nc | 42 | SRD/PC7 | 67 | A7 |
| 18 | nc | 43 | $\overline{BG}/\overline{BS}$ | 68 | A8 |
| 19 | H3/PB3 | 44 | nc | 69 | nc |
| 20 | H2/PB2 | 45 | $\overline{BR}/\overline{WT}$ | 70 | A9 |
| 21 | nc | 46 | \overline{WR} | 71 | A10 |
| 22 | H1/PB1 | 47 | \overline{RD} | 72 | nc |
| 23 | GNDH | 48 | X/ \overline{Y} | 73 | GNDN |
| 24 | GNDH | 49 | \overline{DS} | 74 | GNDN |
| 25 | H0/PB0 | 50 | nc | 75 | A11 |

Table 3-3 DSP56001A Signal Identification by Pin Number —PQFP & CQFP

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------|-------------|---------|--------------------------------|
| 76 | A12 | 95 | nc | 114 | D19 |
| 77 | A13 | 96 | D9 | 115 | D20 |
| 78 | nc | 97 | D10 | 116 | nc |
| 79 | A14 | 98 | nc | 117 | nc |
| 80 | A15 | 99 | D11 | 118 | D21 |
| 81 | D0 | 100 | VCCD | 119 | D22 |
| 82 | D1 | 101 | VCCD | 120 | D23 |
| 83 | nc | 102 | D12 | 121 | MODB/ $\overline{\text{IRQB}}$ |
| 84 | nc | 103 | nc | 122 | nc |
| 85 | D2 | 104 | D13 | 123 | MODA/ $\overline{\text{IRQA}}$ |
| 86 | D3 | 105 | D14 | 124 | $\overline{\text{RESET}}$ |
| 87 | D4 | 106 | D15 | 125 | nc |
| 88 | D5 | 107 | nc | 126 | XTAL |
| 89 | nc | 108 | D16 | 127 | EXTAL |
| 90 | GNDD | 109 | D17 | 128 | Vccq |
| 91 | GNDD | 110 | nc | 129 | Vccq |
| 92 | D6 | 111 | GNDD | 130 | GNDQ |
| 93 | D7 | 112 | GNDD | 131 | GNDQ |
| 94 | D8 | 113 | D18 | 132 | nc |
| <p>Note: 1. "nc" are no connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias. 2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).</p> | | | | | |

Freescale Semiconductor, Inc.

Table 3-4 DSP56001A Identification by Signal Name

| Signal Name | 132 pin "FC" PQFP or "FE" CQFP Pin No. | 88 pin "RC" PGA Pin No. | Signal Name | 132 pin "FC" PQFP or "FE" CQFP Pin No. | 88 pin "RC" PGA Pin No. |
|-----------------|-------------------------------------------------|-------------------------------|-----------------|-------------------------------------------------|-------------------------------|
| A0 | 53 | M11 | D8 | 94 | J1 |
| A1 | 54 | N11 | D9 | 96 | H1 |
| A2 | 57 | N10 | D10 | 97 | G1 |
| A3 | 58 | M9 | D11 | 99 | F1 |
| A4 | 60 | N9 | D12 | 102 | F2 |
| A5 | 61 | M8 | D13 | 104 | E1 |
| A6 | 65 | N8 | D14 | 105 | D1 |
| A7 | 67 | N7 | D15 | 106 | C1 |
| A8 | 68 | N6 | D16 | 108 | D2 |
| A9 | 70 | M6 | D17 | 109 | B1 |
| A10 | 71 | N5 | D18 | 113 | C2 |
| A11 | 75 | M5 | D19 | 114 | A1 |
| A12 | 76 | N4 | D20 | 115 | B2 |
| A13 | 77 | N3 | D21 | 118 | A2 |
| A14 | 79 | N2 | D22 | 119 | A3 |
| A15 | 80 | M3 | D23 | 120 | B4 |
| \overline{BG} | 43 | K12 | \overline{DS} | 49 | M12 |
| \overline{BR} | 45 | L13 | EXTAL | 127 | B6 |
| \overline{BS} | 43 | K12 | GNDD | 90 | D3 |
| D0 | 81 | N1 | GNDD | 91 | J3 |
| D1 | 82 | M2 | GNDD | 111 | |
| D2 | 85 | L2 | GNDD | 112 | |
| D3 | 86 | M1 | GNDH | 23 | E11 |
| D4 | 87 | L1 | GNDH | 24 | |

Table 3-4 DSP56001A Identification by Signal Name (Continued)

| Signal Name | 132 pin "FC" PQFP or "FE" CQFP Pin No. | 88 pin "RC" PGA Pin No. | Signal Name | 132 pin "FC" PQFP or "FE" CQFP Pin No. | 88 pin "RC" PGA Pin No. |
|-------------|-------------------------------------------------|-------------------------------|-------------|-------------------------------------------------|-------------------------------|
| D5 | 88 | K2 | GNDN | 55 | L6 |
| D6 | 92 | K1 | GNDN | 56 | L9 |
| D7 | 93 | J2 | GNDN | 73 | |
| GNDN | 74 | | PB2 | 20 | C12 |
| GNDQ | 33 | B7 | PB3 | 19 | B13 |
| GNDQ | 34 | G11 | PB4 | 16 | B12 |
| GNDQ | 130 | | PB5 | 15 | A13 |
| GNDQ | 131 | | PB6 | 14 | A12 |
| H0 | 25 | D12 | PB7 | 11 | B11 |
| H1 | 22 | C13 | PB8 | 5 | B8 |
| H2 | 20 | C12 | PB9 | 2 | A8 |
| H3 | 19 | B13 | PB10 | 1 | A7 |
| H4 | 16 | B12 | PB11 | 9 | A11 |
| H5 | 15 | A13 | PB12 | 8 | A10 |
| H6 | 14 | A12 | PB13 | 10 | B10 |
| H7 | 11 | B11 | PB14 | 6 | A9 |
| HA0 | 5 | B8 | PC0 | 27 | D13 |
| HA1 | 2 | A8 | PC1 | 28 | E13 |
| HA2 | 1 | A7 | PC2 | 29 | F13 |
| HACK | 6 | A9 | PC3 | 31 | F12 |
| HEN | 8 | A10 | PC4 | 40 | K13 |
| HR/W | 9 | A11 | PC5 | 37 | H13 |
| HREQ | 10 | B10 | PC6 | 32 | G13 |
| IRQA | 123 | B5 | PC7 | 42 | J12 |

Table 3-4 DSP56001A Identification by Signal Name (Continued)

| Signal Name | 132 pin "FC" PQFP or "FE" CQFP Pin No. | 88 pin "RC" PGA Pin No. | Signal Name | 132 pin "FC" PQFP or "FE" CQFP Pin No. | 88 pin "RC" PGA Pin No. |
|--------------------------|-------------------------------------------------|-------------------------------|---------------------------|-------------------------------------------------|-------------------------------|
| $\overline{\text{IRQB}}$ | 121 | A4 | PC8 | 39 | J13 |
| MODA | 123 | B5 | $\overline{\text{PS}}$ | 52 | N12 |
| MODB | 121 | A4 | $\overline{\text{RD}}$ | 47 | L12 |
| $\overline{\text{NMI}}$ | none | none | $\overline{\text{RESET}}$ | 124 | A5 |
| PB0 | 25 | D12 | RXD | 27 | D13 |
| PB1 | 22 | C13 | SC0 | 31 | F12 |
| SC1 | 40 | K13 | nc | 26 | |
| SC2 | 37 | H13 | nc | 30 | |
| SCK | 32 | G13 | nc | 38 | |
| SCLK | 29 | F13 | nc | 41 | |
| SRD | 42 | J12 | nc | 44 | |
| STD | 39 | J13 | nc | 50 | |
| TXD | 28 | E13 | nc | 51 | |
| VCCD | 100 | G3 | nc | 59 | |
| VCCD | 101 | | nc | 62 | |
| VCCH | 12 | C9 | nc | 66 | |
| VCCH | 13 | | nc | 69 | |
| VCCN | 63 | L8 | nc | 72 | |
| VCCN | 64 | | nc | 78 | |
| VCCQ | 35 | C6 | nc | 83 | |
| VCCQ | 36 | G12 | nc | 84 | |
| VCCQ | 128 | | nc | 89 | |
| VCCQ | 129 | | nc | 95 | |
| $\overline{\text{WR}}$ | 46 | M13 | nc | 98 | |

Pin-out and Package Information

Table 3-4 DSP56001A Identification by Signal Name (Continued)

| Signal Name | 132 pin "FC" PQFP or "FE" CQFP Pin No. | 88 pin "RC" PGA Pin No. | Signal Name | 132 pin "FC" PQFP or "FE" CQFP Pin No. | 88 pin "RC" PGA Pin No. |
|------------------|-------------------------------------------------|-------------------------------|-------------|-------------------------------------------------|-------------------------------|
| \overline{WT} | 45 | L13 | nc | 103 | |
| X/\overline{Y} | 48 | N13 | nc | 107 | |
| XTAL | 126 | A6 | nc | 110 | |
| nc | 3 | | nc | 116 | |
| nc | 4 | | nc | 117 | |
| nc | 7 | | nc | 122 | |
| nc | 17 | | nc | 125 | |
| nc | 18 | | nc | 132 | |
| nc | 21 | | | | |

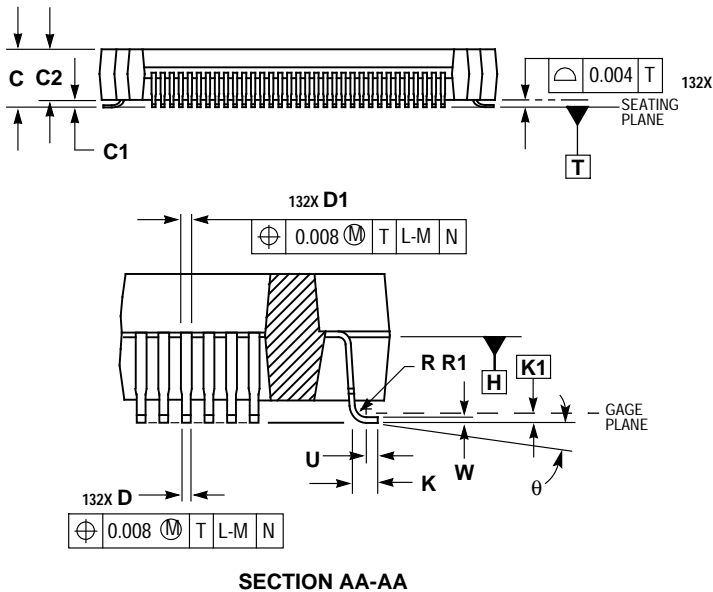
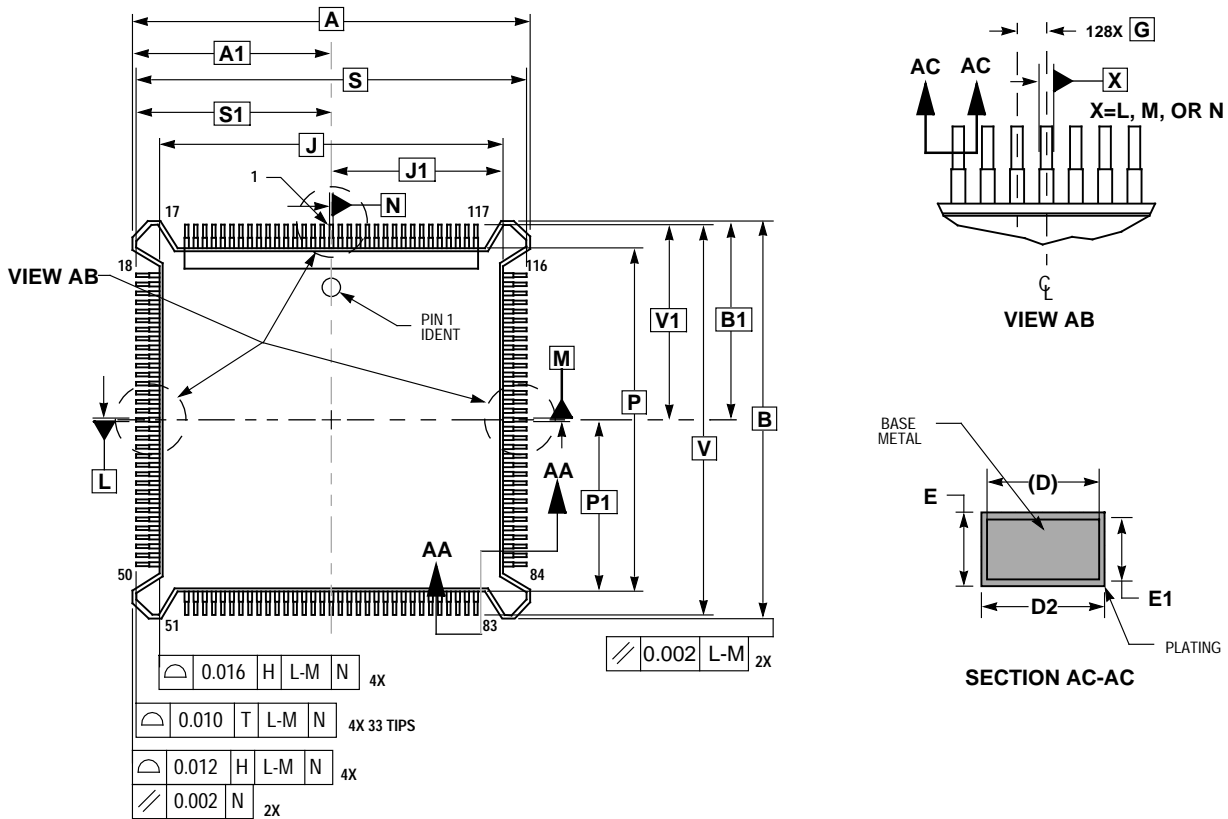
Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-5 DSP56001A Power Supply Pins

| 132 pin "FC" PQFP or "FE" CQFP Pin No. | 88 pin "RC" PGA Pin No. | Power Supply | Circuit Supplied |
|----------------------------------------------|-------------------------------|--------------|---------------------------|
| 63 | L8 | VCCN | Address Bus Buffers |
| 64 | | | |
| 55 | L6 | GNDN | |
| 56 | L9 | | |
| 73 | | | |
| 74 | | | |

Table 3-5 DSP56001A Power Supply Pins (Continued)

| 132 pin "FC" PQFP or "FE" CQFP Pin No. | 88 pin "RC" PGA Pin No. | Power Supply | Circuit Supplied | |
|----------------------------------------------|-------------------------------|--------------|------------------------|-------------|
| 100 | G3 | VCCD | Data Bus Buffers | |
| 101 | | | | |
| 90 | D3 | GNDD | | |
| 91 | J3 | | | |
| 111 | | | | |
| 112 | | | | |
| 35 | C6 | VCCQ | Internal Logic | |
| 36 | G12 | | | |
| 128 | | | | |
| 129 | | | | |
| 33 | B7 | GNDQ | | |
| 34 | G11 | | | |
| 130 | | | | |
| 131 | | | | |
| 12 | C9 | | | VCCH |
| 13 | | GNDH | | Peripherals |
| 23 | E11 | | | |
| 24 | | | | |



- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
 - DIMENSIONS IN INCHES.
 - DIMENSIONS A, B, J, AND P DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION FOR DIMENSIONS A AND B IS 0.007, FOR DIMENSIONS J AND P IS 0.010.
 - DATUM PLANE H IS LOCATED AT THE UNDERSIDE OF LEADS WHERE LEADS EXIT PACKAGE BODY.
 - DATUMS L, M, AND N TO BE DETERMINED WHERE CENTER LEADS EXIT PACKAGE BODY AT DATUM H.
 - DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
 - DIMENSIONS A, B, J, AND P TO BE DETERMINED AT DATUM PLANE H.
 - DIMENSION F DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.019.

| DIM | INCHES | |
|-----|--------|-------|
| | MIN | MAX |
| A | 1.100 | BSC |
| A1 | 0.550 | BSC |
| B | 1.100 | BSC |
| B1 | 0.550 | BSC |
| C | 0.160 | 0.180 |
| C1 | 0.020 | 0.040 |
| C2 | 0.135 | 0.145 |
| D | 0.008 | 0.012 |
| D1 | 0.012 | 0.016 |
| D2 | 0.008 | 0.011 |
| E | 0.006 | 0.008 |
| E1 | 0.005 | 0.007 |
| F | 0.014 | 0.014 |
| G | 0.025 | BSC |
| J | 0.950 | BSC |
| J1 | 0.475 | BSC |
| K | 0.034 | 0.044 |
| K1 | 0.010 | BSC |
| P | 0.950 | BSC |
| P1 | 0.475 | BSC |
| R1 | 0.013 | REF |
| S | 1.080 | BSC |
| S1 | 0.540 | BSC |
| U | 0.025 | REF |
| V | 1.080 | BSC |
| V1 | 0.540 | BSC |
| W | 0.006 | 0.008 |
| θ | 0° | 8° |

Figure 3-7 132-pin Plastic Quad Flat Pack (PQFP) Mechanical Information

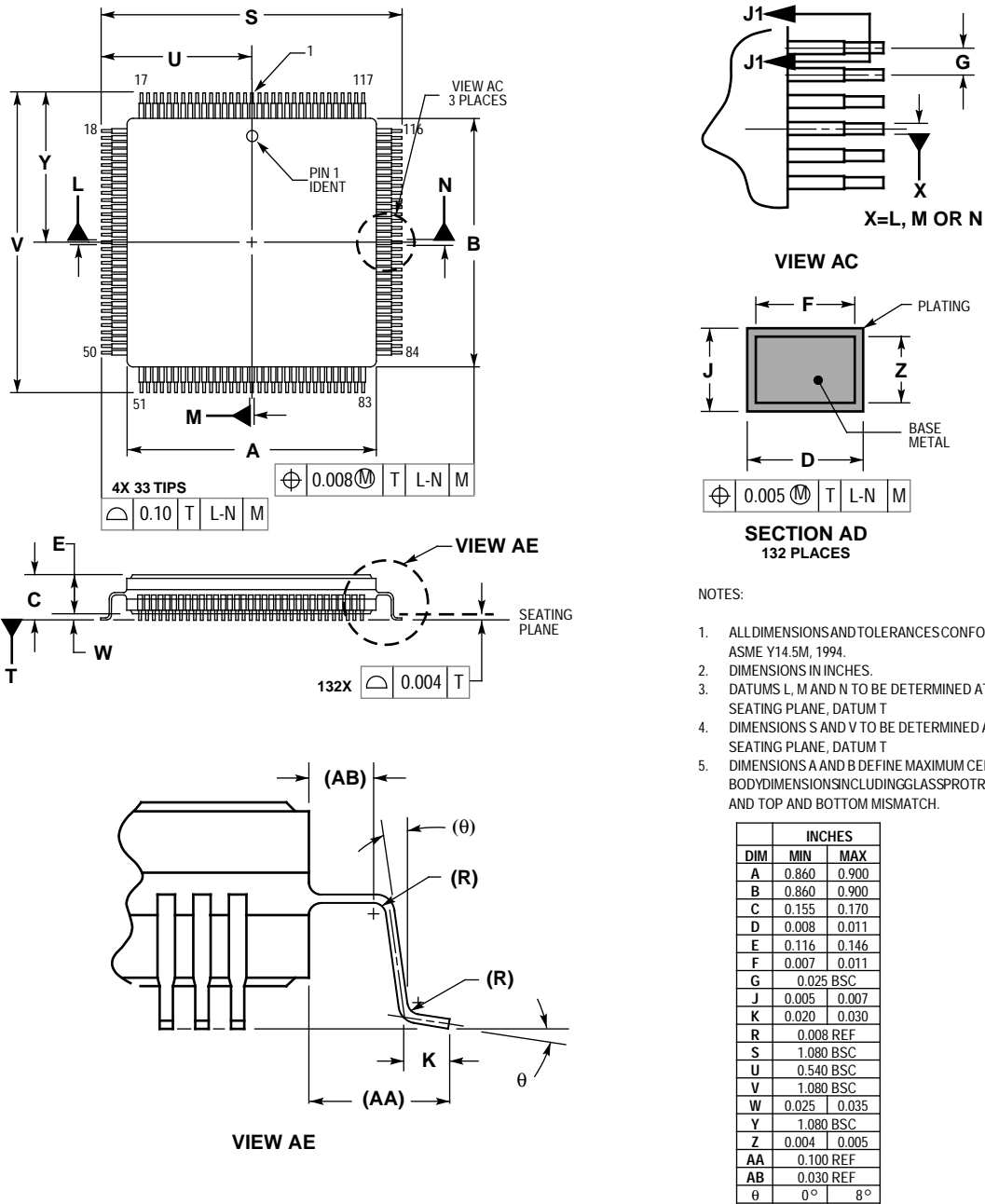


Figure 3-8 132-pin Ceramic Quad Flat Pack (CQFP) Mechanical Information

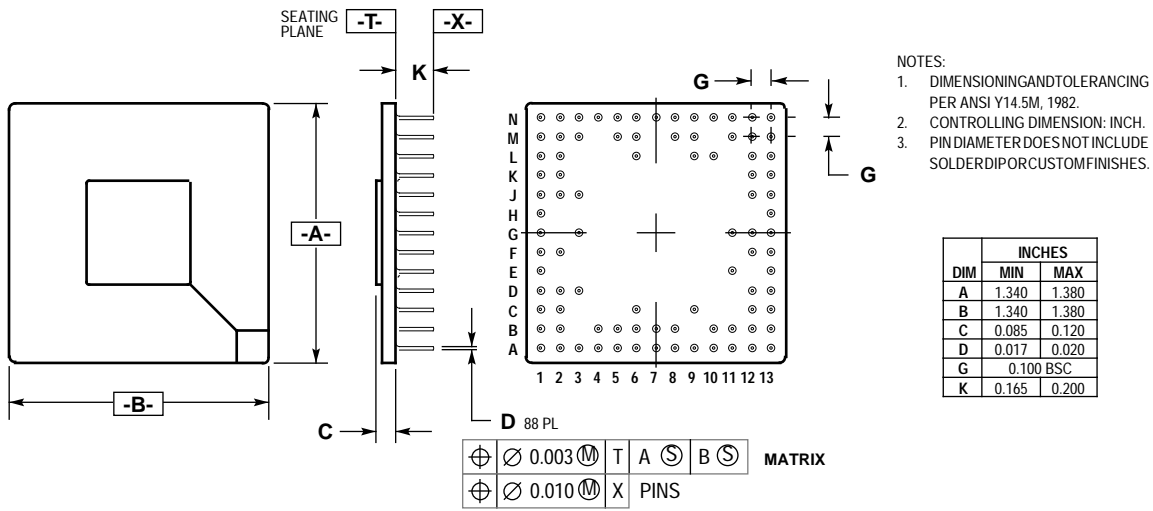
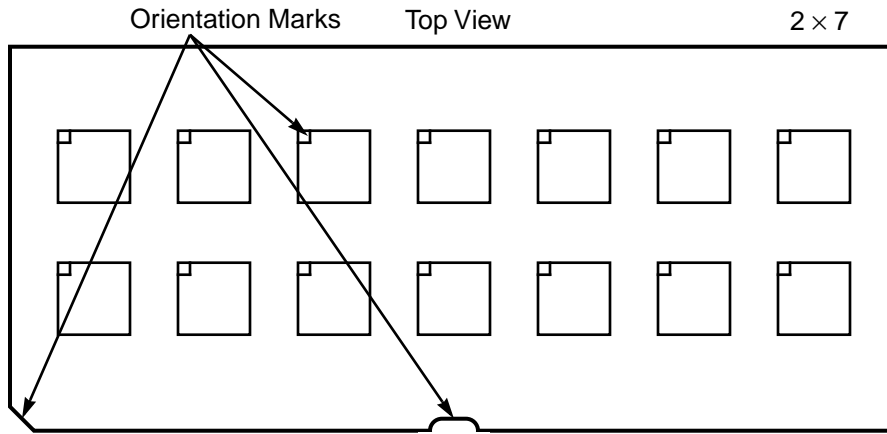
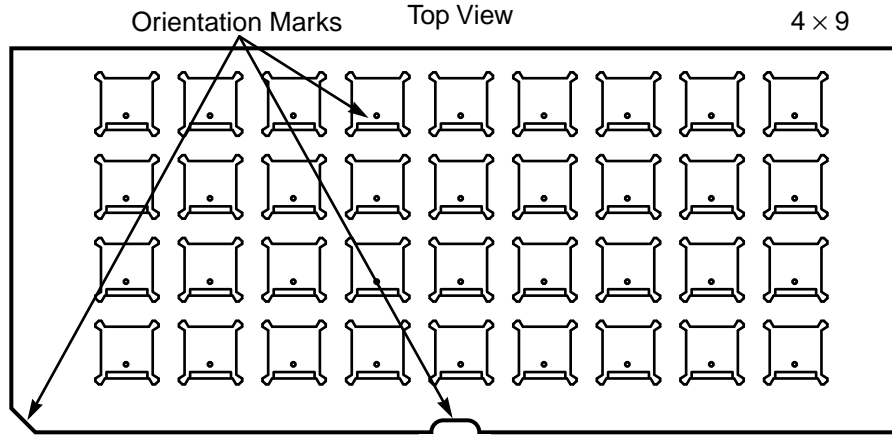


Figure 3-9 88-pin Pin Grid Array (PGA) Mechanical Information



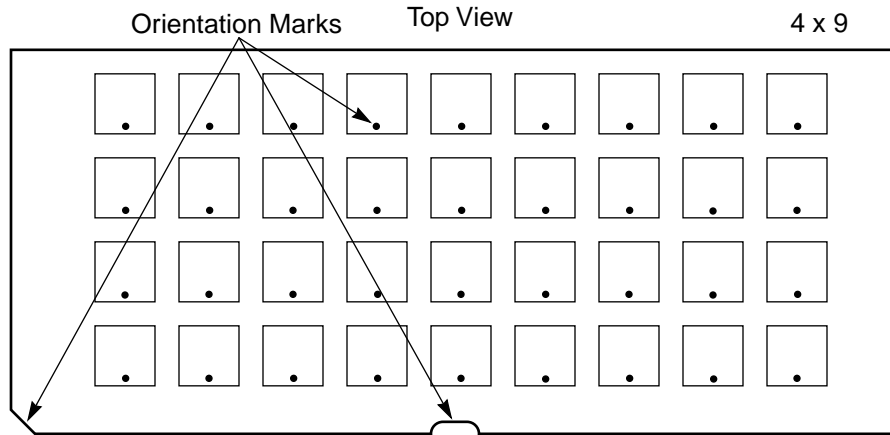
AA0617

Figure 3-10 PGA Shipping Tray



AA1132

Figure 3-11 PQFP Shipping Tray



AA0897

Figure 3-12 CQFP Shipping Tray



SECTION 4

DESIGN CONSIDERATIONS

SUBSTITUTING THE DSP56001A FOR THE DSP56001

This section highlights the differences between the DSP56001 and DSP56001A that need to be taken into consideration when substituting the DSP56001A for the DSP56001. New designs should use the DSP56002 due to its enhanced features and speed.

Hardware Considerations

NON-MASKABLE INTERRUPT (NMI)

A Non-Maskable Interrupt (NMI) function was previously accessible on the DSP56001 by applying 10 volts to the MODB/ $\overline{\text{IRQB}}$ pin. The DSP56001A does not support a non-maskable interrupt (NMI).

CAUTION

DO NOT APPLY 10 VOLTS TO ANY PIN OF THE DSP56001A (including MODB)! Subjecting any pin of the DSP56001A to voltages in excess of the specified TTL/CMOS levels will permanently damage the device.

AC ELECTRICAL CHARACTERISTICS

The DSP56001A die utilizes a faster technology than the DSP56001. As a result, many DSP56001A signals exhibit faster rise and fall times than the same signals on the DSP56001. These faster edges may generate more radiated noise and EMI, and may require more attention to these issues (e.g., the DSP56001A based circuit may require better decoupling).

Software/Application Considerations

Software written for the DSP56001 will generally run unmodified on the DSP56001A. There are, however, certain differences which should be noted. Users should consider the impact these differences may have on each application.

AGU MODIFY REGISTERS

Numbers between \$8000 and \$FFFE (inclusive) are not valid values for loading into the modify registers (M0–M7) of the address generation unit on the DSP56001. Certain values within this range, however, enable wrap-around addressing modes on the DSP56001A that are not supported, and inadvertent enabling of these addressing modes may yield unexpected results. Do **not** load the modify registers of the DSP56001A with values from \$8000 to \$FFFE.

RESERVED MEMORY LOCATIONS

Certain memory locations are designated as reserved on the DSP56001. Accesses to these memory locations on the DSP56001A will result in unpredictable processor behavior **including the possibility of halting the processor completely**. In particular, writes to the following X memory locations should be avoided on the DSP56001A:

X:\$FFDE, X:\$FFDF, X:\$FFFC, X:\$FFFD

MOVEP TO RN/NN/MN REGISTERS

On the DSP56001 there is a pipeline delay when using the MOVEP instruction to change the contents of an address register (Mn, Nn, or Rn). The new contents of the destination address register will not be available for use during the following instruction (i.e, there is a single instruction cycle delay).

On the DSP56001A this pipeline delay has been removed. If an address register (Mn, Nn, or Rn) is directly changed with a MOVEP instruction, the updated contents will be available for use during the following instruction. DSP56001 software that depends on this pipeline delay must be modified when moved onto the DSP56001A.

MOVEP TO/FROM DATA ALU REGISTERS

MOVEP instructions to/from Data ALU registers take 2 instruction cycles on the DSP56001. On the DSP56001A, these instructions take only 1 instruction cycle. DSP56001 software which is dependent on the timing of this form of the MOVEP instruction must be modified when ported to the DSP56001A.

Table 4-1 Illegal Instructions

| Instruction Symbol | Instruction Name |
|---------------------------------|------------------------------------------------|
| DEBUG—DO NOT USE | Enter Debug mode |
| DEBUG _{cc} —DO NOT USE | Enter Debug mode conditionally |
| DEC | Decrement by one |
| INC | Increment by one |
| MAC #iiii | Signed multiply-accumulate immediate |
| MPY #iiii | Signed multiply immediate |
| MACR #iiii | Signed multiply-accumulate and round immediate |
| MPYR #iiii | Signed multiply and round immediate |

MOVEP IMMEDIATE

MOVEP Immediate instructions take 3 instruction cycles on the DSP56001. On the DSP56001A, these instructions take only 2 instruction cycles. DSP56001 software that is dependent on the timing of this form of the MOVEP instruction must be modified when ported to the DSP56001A.

ILLEGAL INSTRUCTIONS

The instructions listed in Table 4-1 will *not* generate an illegal instruction interrupt on the DSP56001A. None of these instructions are tested on the DSP56001A and should *not* be used.

Note: The DEBUG and DEBUG_{cc} instructions are microcoded on the DSP56001A, but the peripherals necessary to make use of this instruction are not available. Any use of the DEBUG or DEBUG_{cc} instructions will completely halt the processor. The processor will exit this state only on reset.

STOP/WAIT TIMING

Wake-up from the Stop and Wait operating modes with \overline{IRQA} and \overline{IRQB} is longer on the DSP56001A by one T_c period.

SCI/SSI INITIALIZATION TIMING

On the DSP56001A, the SCI and SSI clocks are stopped when the peripherals are not enabled in order to save power. As a result, the initialization time of the SCI and SSI is longer on the DSP56001A than on the DSP56001.

CONTROL REGISTERS

The OMR and the Status Register on the DSP56001A have been altered from those on the DSP56001. Refer to **Table 4-2** for details of these alterations.

Table 4-2 Summary of Control Register Differences

| REGISTER | BIT | DSP56001 DEFINITION | DSP56001A DEFINITION | EXPLANATION OF DIFFERENCE |
|-------------------------|-----|------------------------------------|------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Status Register | 7 | Reserved— Read/Written as zero. | Reserved— Read as don't care. | On the 001A this bit may be read as 0 or 1. The user should not rely on this bit being a given value. |
| | 14 | Reserved— Read/Written as zero. | Reserved— Write as zero only, read as don't care. | If this bit is set on the 56001A, the operations performed by the Data ALU change, and 56001 code will yield erroneous results. Write this bit only as zero. |
| Operating Mode Register | 3 | Reserved— Read/.Written as zero | Reserved— Write as zero only, read as don't care. | If this bit is set, memory reads may be from incorrect locations. Write this bit only as zero. |
| Port B Control Register | 1 | Reserved— Written as zero. | Reserved— Written as zero. | Writing this bit as a 1 will result in behavior differences between the 001 and the 001A. |

HOST COMMAND VECTOR REGISTER

The DSP56001A's Host Command Vector Register (CVR) also differs from that of the DSP56001 (see **Table 4-3**).

Table 4-3 Summary of Host Command Vector Register Differences

| REGISTER | BIT | DSP56001 DEFINITION | DSP56001A DEFINITION | EXPLANATION OF DIFFERENCE |
|------------------------------------|-----|----------------------------|------------------------------|------------------------------------------------------------|
| Host Command Vector Register (CVR) | 5 | Reserved— Read as zero. | Reserved—Read as don't care. | This bit should be written with only a zero on the 56001A. |

HEAT DISSIPATION

The average chip junction temperature, T_J , in °C, can be obtained from:

$$\text{Equation 1: } T_J = T_A + (P_D \times \Theta_{JA})$$

Where:

T_A = ambient temperature, °C

Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{CC} \times V_{CC}$ watt—chip internal power

$P_{I/O}$ = power dissipation on input and output pins—user determined

For most applications $P_{I/O} < P_{INT}$ and $P_{I/O}$ can be neglected. An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$\text{Equation 2: } P_D = K / (T_J + 273)$$

Solving equations (1) and (2) for K gives:

$$\text{Equation 3: } K = P_D \times (T_A + 273) + P_D \times \Theta_{JA}$$

Where: K is a constant pertaining to the particular package

K can be determined from equation (2) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A . The total thermal resistance of a package (Θ_{JA}) can be separated into two components, Θ_{JC} and Θ_{CA} , representing the barrier to heat flow from the semiconductor junction to the package (case) surface (Θ_{JC}) and from the case to the outside ambient (Θ_{CA}). These terms are related by the equation:

$$\text{Equation 4: } \Theta_{JA} = \Theta_{JC} + \Theta_{CA}$$

Θ_{JC} is device-related and cannot be influenced by the user. However, Θ_{CA} is user-dependent and can be minimized by thermal management techniques such as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management can significantly reduce Θ_{CA} so that Θ_{JA} approximately equals Θ_{JC} . Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, "Thermal Resistance Measurement Method for MC68XX Microcomponent Devices", and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

ELECTRICAL DESIGN CONSIDERATIONS**CAUTION**

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP, and from the board ground to each GND pin.
- Use at least four 0.1 μ F bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the \overline{RD} , \overline{WR} , \overline{IRQA} , \overline{IRQB} , \overline{NMI} , \overline{HEN} , and \overline{HACK} pins.
- Consider all device loads, as well as parasitic capacitance due to PCB traces, when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.

POWER CONSUMPTION

Power dissipation is a key issue in portable DSP applications. The following describes some factors that affect current consumption. Current consumption is described by the formula:

$$\text{Equation 5: } I = C \times V \times f$$

where :

- C = node/pin capacitance
- V = voltage swing
- f = frequency of node/pin toggle

For example, for an address pin loaded with a 50 pF capacitance and operating at 5.5V with a 33 MHz clock, toggling at its maximum possible rate (which is 8.25 MHz), the current consumption is:

$$\text{Equation 6: } I = 50 \times 10^{-12} \times 5.5 \times 8.25 \times 10^6 = 227 \text{ mA}$$

The maximum internal current value ($I_{CCI} - \text{max}$), reflects the maximum possible switching of the internal buses, which is not necessarily a real application case. The typical internal current value ($I_{CCI} - \text{typ}$) reflects the average switching of the internal buses.

The following steps are recommended for applications requiring very low current consumption:

1. Minimize external memory accesses; use internal memory accesses instead.
2. Minimize the number of pins that are switching.
3. Minimize the capacitive load on the pins.
4. Connect the unused inputs to pull-up or pull-down resistors.

HOST PORT CONSIDERATIONS

Careful synchronization is required when reading multi-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected. The situation exists in the Host Interface. The following paragraphs present considerations for proper operation.

Host Programming Considerations

UNSYNCHRONIZED READING OF RECEIVE BYTE REGISTERS

When reading receive byte registers, RXH or RXL, the host program should use interrupts or poll the RXDF flag, which indicates that data is available. This assures that the data in the receive byte registers will be stable.

OVERWRITING TRANSMIT BYTE REGISTERS

The host program should not write to the transmit byte registers, TXH or TXL, unless the TXDE bit is set, indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the HRX register.

SYNCHRONIZATION OF STATUS BITS FROM DSP TO HOST

HC, HREQ, DMA, HF3, HF2, TRDY, TXDE, and RXDF status bits are set or cleared from inside the DSP and read by the host processor (refer to the *User's Manual* for descriptions of these status bits). The host can read these status bits very quickly without regard to the clock rate used by the DSP, but the state of the bit could be changing during the read operation. Generally, this is not a system problem, since the bit will be read correctly in the next pass of any host polling routine. However, if the host asserts $\overline{\text{HEN}}$ for more than timing number 31, with a minimum cycle time of timing number 31 + 32, then these status bits are guaranteed to be stable. Exercise care when reading status bits HF3 and HF2 as an encoded pair. If the DSP changes HF3 and HF2 from 00 to 11, there is a small probability that the host could read the bits during the transition and receive 01 or 10 instead of 11. If the combination of HF3 and HF2 has significance, the host could read the wrong combination. Therefore, read the bits twice and check for consensus.

OVERWRITING THE HOST VECTOR

The host program should change the Host Vector register only when the Host Command bit (HC) is clear. This change will guarantee that the DSP interrupt control logic will receive a stable vector.

CANCELLING A PENDING HOST COMMAND EXCEPTION

The host processor may elect to clear the HC bit to cancel the host command exception request at any time before it is recognized by the DSP. Because the host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the host command exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time that the HC bit is cleared.

VARIANCE IN THE HOST INTERFACE TIMING

The Host Interface (HI) may vary. Therefore, a host which attempts to load (bootstrap) the DSP should first make sure that the part has completed its HI port programming (e.g., by setting the INIT bit in ICR then polling it and waiting it to be cleared, then reading the ISR or by writing the TREQ/RREQ together with the INIT and then polling INIT, ISR, and the $\overline{\text{HREQ}}$ pin).

DSP Programming Considerations

SYNCHRONIZATION OF STATUS BITS FROM HOST TO DSP

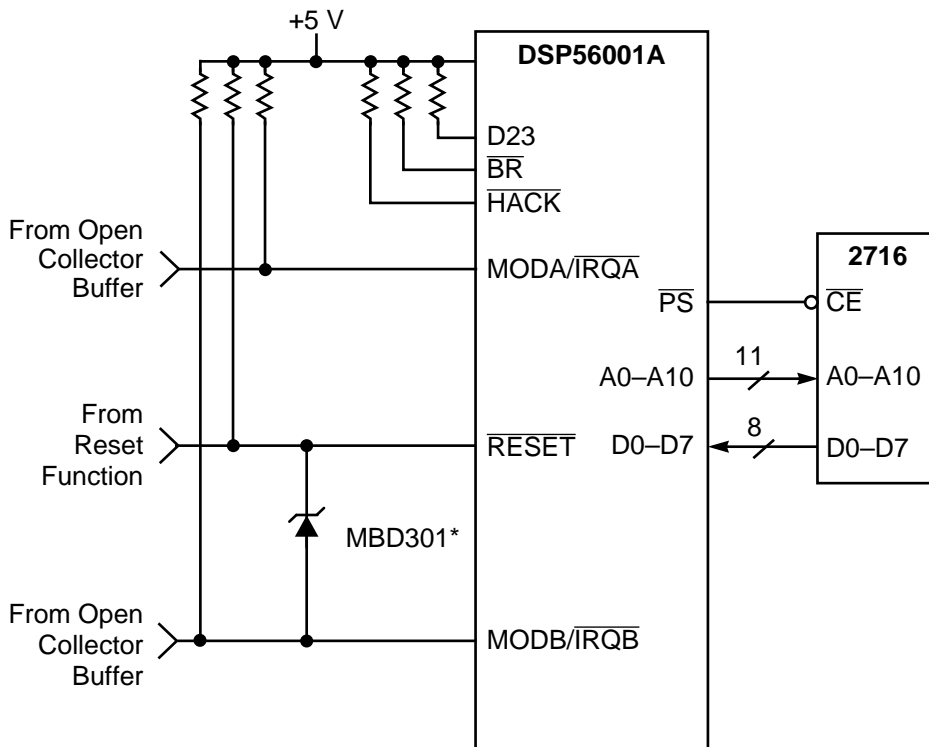
DMA, HF1, HF0, and HCP, HTDE, and HRDF status bits are set or cleared by the host processor side of the interface. These bits are individually synchronized to the DSP clock. (Refer to the *User's Manual* for descriptions of these status bits.)

READING HF0 AND HF1 AS AN ENCODED PAIR

Care must be exercised when reading status bits HF0 and HF1 as an encoded pair, because the four combinations (00, 01, 10, and 11) each have significance. A very small probability exists that the DSP will read the status bits during transition. Therefore, HF0 and HF1 should be read twice and checked for consensus.

APPLICATION EXAMPLES

The lowest cost DSP56001A-based system is shown in **Figure 4-1**. It uses no run time external memory and requires only two chips, the DSP56001A and a low cost EPROM. The EPROM read access time should be less than 780 nanoseconds when the DSP56001A is operating at a clock rate of 20.5 MHz.

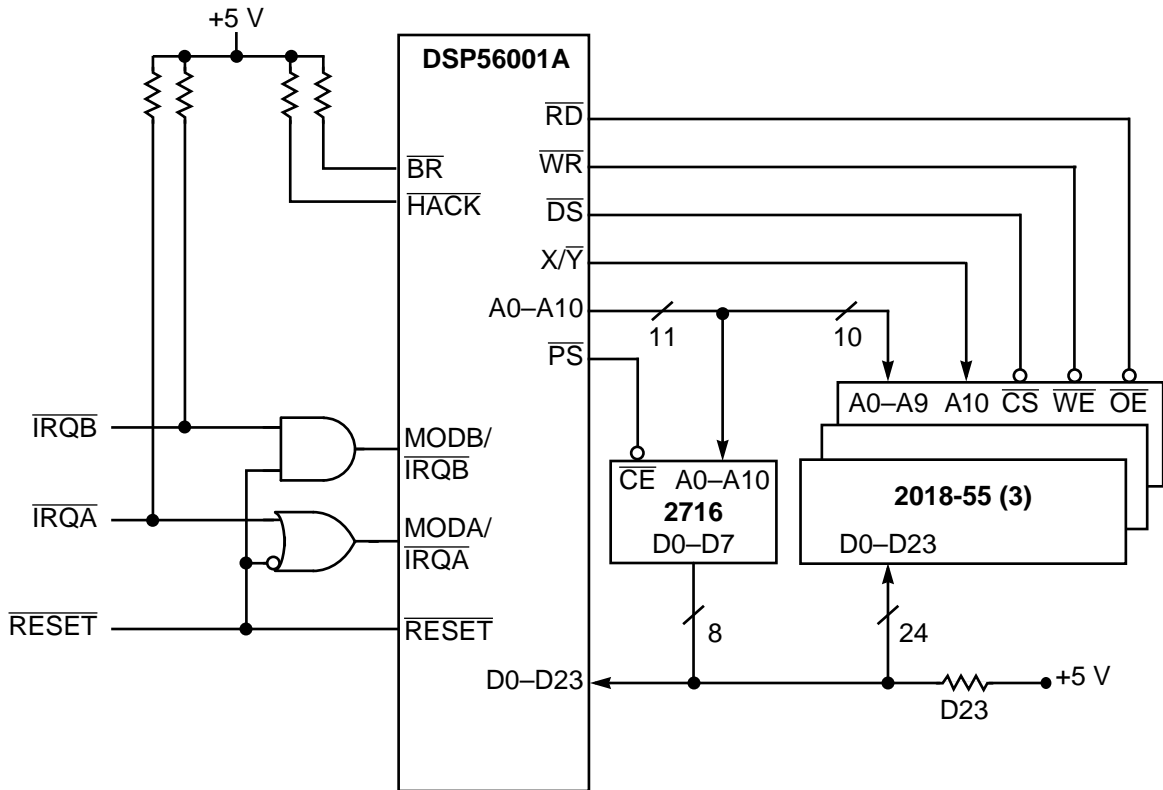


- Note:
1. *These diodes **must** be Schottky diodes.
 2. All resistors are 15 K Ω unless noted otherwise.
 3. When in Reset, \overline{IRQA} and \overline{IRQB} must be deasserted by external peripherals.

AA0904

Figure 4-1 No Glue Logic, Low Cost Memory Port Bootstrap—Mode 1

A system with external data RAM memory requires no glue logic to select the external EPROM from Bootstrap mode. \overline{PS} is used to enable the EPROM and \overline{DS} is used to enable the high speed data memories, as shown in Figure 4-2.

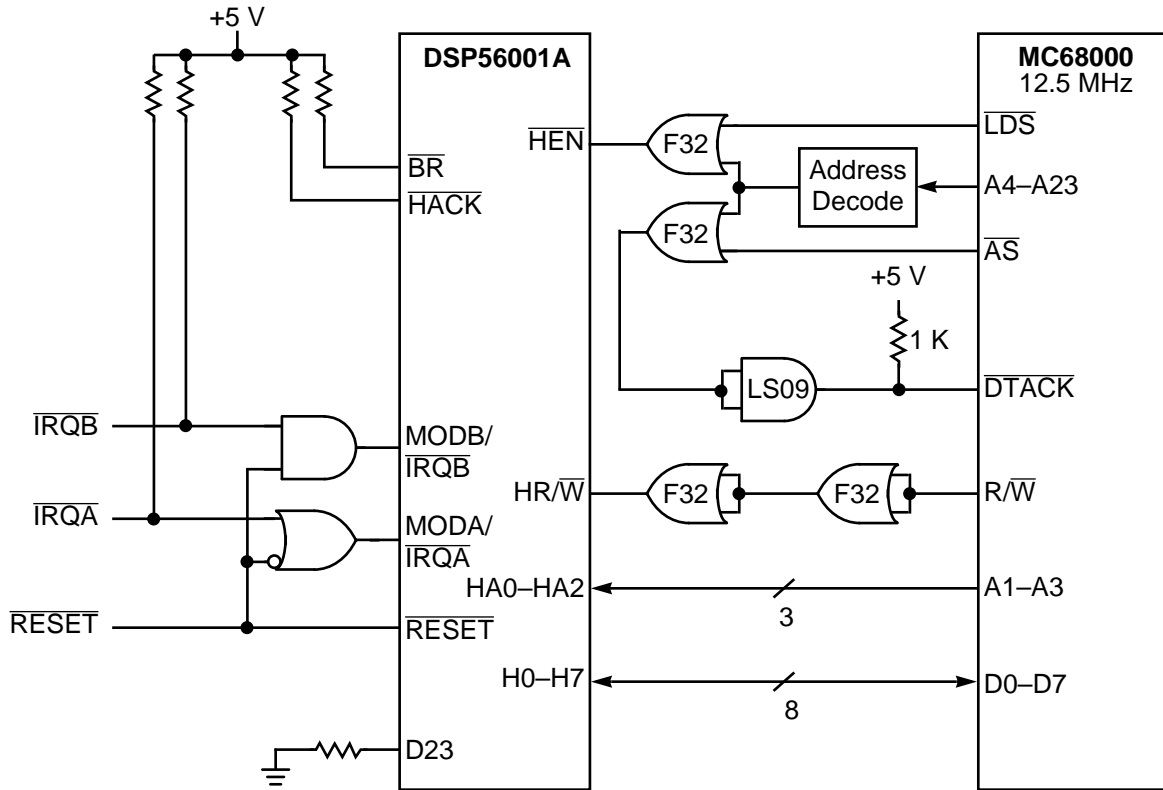


- Note:
1. All resistors are 15 KΩ unless noted otherwise.
 2. When in Reset, \overline{IRQA} and \overline{IRQB} must be deasserted by external peripherals.

AA0905

Figure 4-2 Port A Bootstrap with External Data RAM—Mode 1

Figure 4-3 shows the DSP56001A bootstrapping via the Host Port from an MC68000.

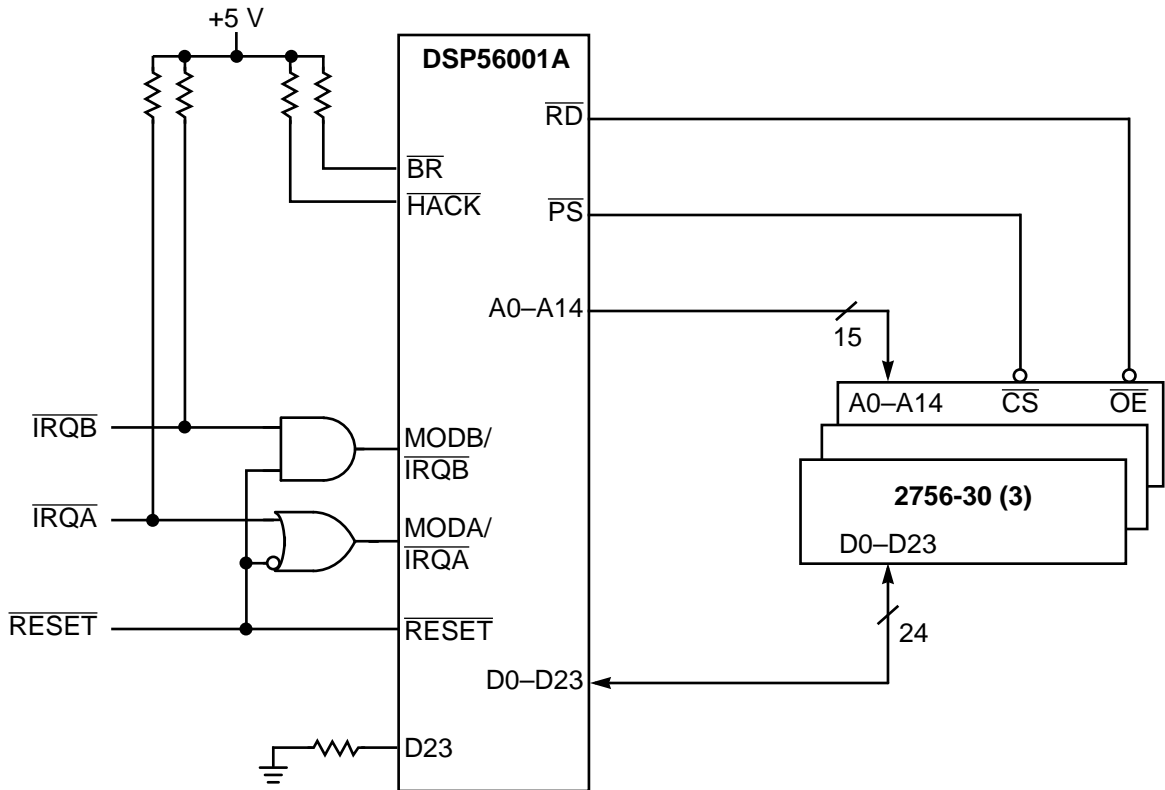


- Note: 1. All resistors are 15 K Ω unless noted otherwise.
 2. When in Reset, \overline{IRQA} and \overline{IRQB} must be deasserted by external peripherals.

AA0906

Figure 4-3 DSP56001A Host Bootstrap Example—Mode 5

In **Figure 4-4**, the DSP56001A is operated in Mode 3 with external program memory and the reset vector at location \$0000. The programmer can overlay the high-speed on-chip Program RAM with DSP algorithms by using the MOVEM instruction.

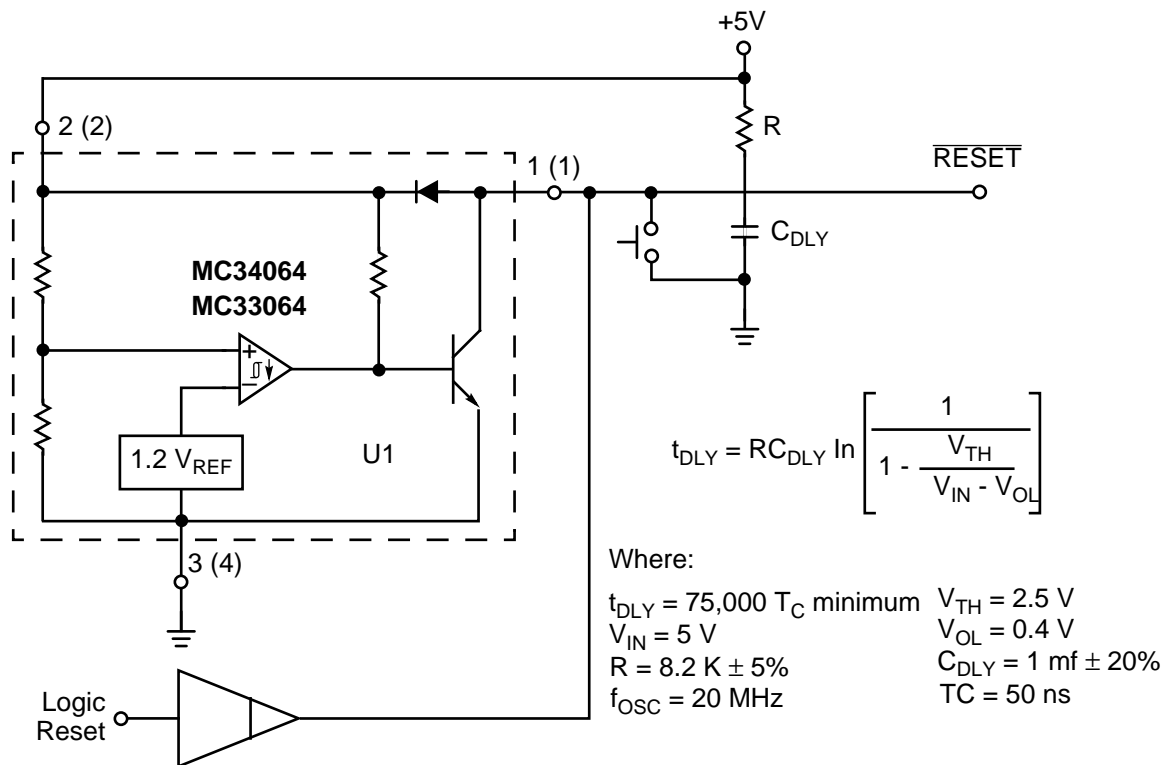


- Note:
1. All resistors are 15 K Ω unless noted otherwise.
 2. When in Reset, \overline{IRQA} and \overline{IRQB} must be deasserted by external peripherals.

AA0907

Figure 4-4 32K Words of External Program ROM—Mode 3

Figure 4-5 shows a circuit that waits until V_{CC} on the DSP56001A is at least 4.5 V before initiating a $75,000 \times T_C$ oscillator stabilization delay required for the on-chip oscillator (only $25 \times T_C$ is required for an external oscillator). This insures that the DSP is operational and stable before releasing the reset signal.

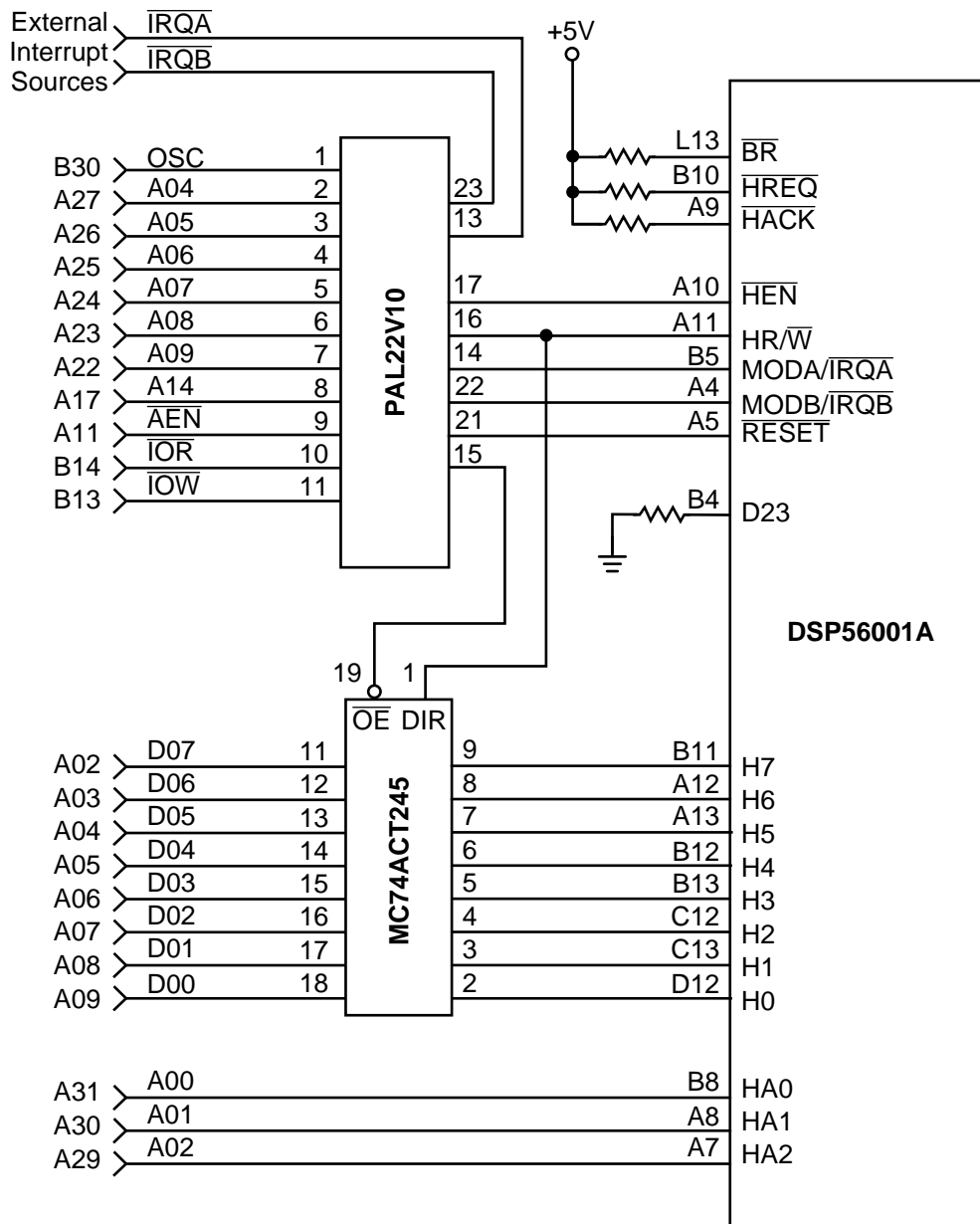


- Note:
1. \overline{IRQA} , and \overline{IRQB} must be driven to the logic levels appropriate for the application.
 2. MODA and MODB must be driven to the logic levels appropriate for the application.

AA0908

Figure 4-5 Reset Circuit Using MC34064/MC33064

Figure 4-6 shows the DSP56001A connected to the bus of an IBM-PC computer. This circuit is complete and does not require external ROM or RAM to load and execute code from the PC. The PAL equations and other details of this circuit are available in the application report entitled "DSP56001 Interface Techniques and Examples" (APR11/D).



- Note: 1. Connector is J1 of ISA Bus.
 2. All series resistors are 15 KΩ.

AA0909

Figure 4-6 DSP56001A-to-ISA Bus Interface Schematic

SECTION 5

ORDERING INFORMATION

Table 5-1 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 5-1 DSP56001A Ordering Information

| Part | Package Type | Pin Count | Frequency (MHz) | Order Number |
|-------------|-------------------------------|------------------|------------------------|---------------------|
| DSP56001A | Ceramic Pin-Grid Array (PGA) | 88 | 27 | DSP56001ARC27 |
| | | | 33 | DSP56001ARC33 |
| | Plastic Quad Flat Pack (PQFP) | 132 | 27 | DSP56001AFC27 |
| | | | 33 | DSP56001AFC33 |
| | Ceramic Quad Flat Pack (CQFP) | 132 | 27 | DSP56001AFE27 |
| | | | 33 | DSP56001AFE33 |



APPENDIX A

ROM TABLE LISTINGS

The data ROM in the 56001A contains numeric tables.

Table A-1 contains the μ -law and A-law expansion table, stored in X-ROM from address X:\$100.

Table A-2 contains the sine wave table, stored in Y-ROM from address Y:\$100.

MU-LAW / A-LAW EXPANSION TABLES

Table A-1 μ -Law / A-law Expansion Table

| | | | | | | | |
|------|-----|----------|--------|------|----|----------|--------|
| | ORG | X:\$100 | | M_16 | DC | \$327C00 | ; 3231 |
| | | | | M_17 | DC | \$307C00 | ; 3103 |
| | | | | M_18 | DC | \$2E7C00 | ; 2975 |
| M_00 | DC | \$7D7C00 | ; 8031 | M_19 | DC | \$2C7C00 | ; 2847 |
| M_01 | DC | \$797C00 | ; 7775 | M_1A | DC | \$2A7C00 | ; 2719 |
| M_02 | DC | \$757C00 | ; 7519 | M_1B | DC | \$287C00 | ; 2591 |
| M_03 | DC | \$717C00 | ; 7263 | M_1C | DC | \$267C00 | ; 2463 |
| M_04 | DC | \$6D7C00 | ; 7007 | M_1D | DC | \$247C00 | ; 2335 |
| M_05 | DC | \$697C00 | ; 6751 | M_1E | DC | \$227C00 | ; 2207 |
| M_06 | DC | \$657C00 | ; 6495 | M_1F | DC | \$207C00 | ; 2079 |
| M_07 | DC | \$617C00 | ; 6239 | M_20 | DC | \$1EFC00 | ; 1983 |
| M_08 | DC | \$5D7C00 | ; 5983 | M_21 | DC | \$1DFC00 | ; 1919 |
| M_09 | DC | \$597C00 | ; 5727 | M_22 | DC | \$1CFC00 | ; 1855 |
| M_0A | DC | \$557C00 | ; 5471 | M_23 | DC | \$1BFC00 | ; 1791 |
| M_0B | DC | \$517C00 | ; 5215 | M_24 | DC | \$1AFC00 | ; 1727 |
| M_0C | DC | \$4D7C00 | ; 4959 | M_25 | DC | \$19FC00 | ; 1663 |
| M_0D | DC | \$497C00 | ; 4703 | M_26 | DC | \$18FC00 | ; 1599 |
| M_0E | DC | \$457C00 | ; 4447 | M_27 | DC | \$17FC00 | ; 1535 |
| M_0F | DC | \$417C00 | ; 4191 | M_28 | DC | \$16FC00 | ; 1471 |
| M_10 | DC | \$3E7C00 | ; 3999 | M_29 | DC | \$15FC00 | ; 1407 |
| M_11 | DC | \$3C7C00 | ; 3871 | M_2A | DC | \$14FC00 | ; 1343 |
| M_12 | DC | \$3A7C00 | ; 3743 | M_2B | DC | \$13FC00 | ; 1279 |
| M_13 | DC | \$387C00 | ; 3615 | M_2C | DC | \$12FC00 | ; 1215 |
| M_14 | DC | \$367C00 | ; 3487 | M_2D | DC | \$11FC00 | ; 1151 |
| M_15 | DC | \$347C00 | ; 3359 | | | | |

Freescale Semiconductor, Inc.

ROM Table Listings

mu-Law / A-Law Expansion Tables

| | | | | | | | | | |
|------|----|----------|---|------|------|----|----------|---|-----|
| M_2E | DC | \$10FC00 | ; | 1087 | M_57 | DC | \$028C00 | ; | 163 |
| M_2F | DC | \$0FFC00 | ; | 1023 | M_58 | DC | \$026C00 | ; | 155 |
| M_30 | DC | \$0F3C00 | ; | 975 | M_59 | DC | \$024C00 | ; | 147 |
| M_31 | DC | \$0EBC00 | ; | 943 | M_5A | DC | \$022C00 | ; | 139 |
| M_32 | DC | \$0E3C00 | ; | 911 | M_5B | DC | \$020C00 | ; | 131 |
| M_33 | DC | \$0DBC00 | ; | 879 | M_5C | DC | \$01EC00 | ; | 123 |
| M_34 | DC | \$0D3C00 | ; | 847 | M_5D | DC | \$01CC00 | ; | 115 |
| M_35 | DC | \$0CBC00 | ; | 815 | M_5E | DC | \$01AC00 | ; | 107 |
| M_36 | DC | \$0C3C00 | ; | 783 | M_5F | DC | \$018C00 | ; | 99 |
| M_37 | DC | \$0BBC00 | ; | 751 | M_60 | DC | \$017400 | ; | 93 |
| M_38 | DC | \$0B3C00 | ; | 719 | M_61 | DC | \$016400 | ; | 89 |
| M_39 | DC | \$0ABC00 | ; | 687 | M_62 | DC | \$015400 | ; | 85 |
| M_3A | DC | \$0A3C00 | ; | 655 | M_63 | DC | \$014400 | ; | 81 |
| M_3B | DC | \$09BC00 | ; | 623 | M_64 | DC | \$013400 | ; | 77 |
| M_3C | DC | \$093C00 | ; | 591 | M_65 | DC | \$012400 | ; | 73 |
| M_3D | DC | \$08BC00 | ; | 559 | M_66 | DC | \$011400 | ; | 69 |
| M_3E | DC | \$083C00 | ; | 527 | M_67 | DC | \$010400 | ; | 65 |
| M_3F | DC | \$07BC00 | ; | 495 | M_68 | DC | \$00F400 | ; | 61 |
| M_40 | DC | \$075C00 | ; | 471 | M_69 | DC | \$00E400 | ; | 57 |
| M_41 | DC | \$071C00 | ; | 455 | M_6A | DC | \$00D400 | ; | 53 |
| M_42 | DC | \$06DC00 | ; | 439 | M_6B | DC | \$00C400 | ; | 49 |
| M_43 | DC | \$069C00 | ; | 423 | M_6C | DC | \$00B400 | ; | 45 |
| M_44 | DC | \$065C00 | ; | 407 | M_6D | DC | \$00A400 | ; | 41 |
| M_45 | DC | \$061C00 | ; | 391 | M_6E | DC | \$009400 | ; | 37 |
| M_46 | DC | \$05DC00 | ; | 375 | M_6F | DC | \$008400 | ; | 33 |
| M_47 | DC | \$059C00 | ; | 359 | M_70 | DC | \$007800 | ; | 30 |
| M_48 | DC | \$055C00 | ; | 343 | M_71 | DC | \$007000 | ; | 28 |
| M_49 | DC | \$051C00 | ; | 327 | M_72 | DC | \$006800 | ; | 26 |
| M_4A | DC | \$04DC00 | ; | 311 | M_73 | DC | \$006000 | ; | 24 |
| M_4B | DC | \$049C00 | ; | 295 | M_74 | DC | \$005800 | ; | 22 |
| M_4C | DC | \$045C00 | ; | 279 | M_75 | DC | \$005000 | ; | 20 |
| M_4D | DC | \$041C00 | ; | 263 | M_76 | DC | \$004800 | ; | 18 |
| M_4E | DC | \$03DC00 | ; | 247 | M_77 | DC | \$004000 | ; | 16 |
| M_4F | DC | \$039C00 | ; | 231 | M_78 | DC | \$003800 | ; | 14 |
| M_50 | DC | \$036C00 | ; | 219 | M_79 | DC | \$003000 | ; | 12 |
| M_51 | DC | \$034C00 | ; | 211 | M_7A | DC | \$002800 | ; | 10 |
| M_52 | DC | \$032C00 | ; | 203 | M_7B | DC | \$002000 | ; | 8 |
| M_53 | DC | \$030C00 | ; | 195 | M_7C | DC | \$001800 | ; | 6 |
| M_54 | DC | \$02EC00 | ; | 187 | M_7D | DC | \$001000 | ; | 4 |
| M_55 | DC | \$02CC00 | ; | 179 | M_7E | DC | \$000800 | ; | 2 |
| M_56 | DC | \$02AC00 | ; | 171 | M_7F | DC | \$000000 | ; | 0 |

| | | | | | | | | | |
|------|----|----------|---|------|------|----|----------|---|------|
| A_80 | DC | \$158000 | ; | 688 | A_A9 | DC | \$720000 | ; | 3648 |
| A_81 | DC | \$148000 | ; | 656 | A_AA | DC | \$7E0000 | ; | 4032 |
| A_82 | DC | \$178000 | ; | 752 | A_AB | DC | \$7A0000 | ; | 3904 |
| A_83 | DC | \$168000 | ; | 720 | A_AC | DC | \$660000 | ; | 3264 |
| A_84 | DC | \$118000 | ; | 560 | A_AD | DC | \$620000 | ; | 3136 |
| A_85 | DC | \$108000 | ; | 528 | A_AE | DC | \$6E0000 | ; | 3520 |
| A_86 | DC | \$138000 | ; | 624 | A_AF | DC | \$6A0000 | ; | 3392 |
| A_87 | DC | \$128000 | ; | 592 | A_B0 | DC | \$2B0000 | ; | 1376 |
| A_88 | DC | \$1D8000 | ; | 944 | A_B1 | DC | \$290000 | ; | 1312 |
| A_89 | DC | \$1C8000 | ; | 912 | A_B2 | DC | \$2F0000 | ; | 1504 |
| A_8A | DC | \$1F8000 | ; | 1008 | A_B3 | DC | \$2D0000 | ; | 1440 |
| A_8B | DC | \$1E8000 | ; | 976 | A_B4 | DC | \$230000 | ; | 1120 |
| A_8C | DC | \$198000 | ; | 816 | A_B5 | DC | \$210000 | ; | 1056 |
| A_8D | DC | \$188000 | ; | 784 | A_B6 | DC | \$270000 | ; | 1248 |
| A_8E | DC | \$1B8000 | ; | 880 | A_B7 | DC | \$250000 | ; | 1184 |
| A_8F | DC | \$1A8000 | ; | 848 | A_B8 | DC | \$3B0000 | ; | 1888 |
| A_90 | DC | \$0AC000 | ; | 344 | A_B9 | DC | \$390000 | ; | 1824 |
| A_91 | DC | \$0A4000 | ; | 328 | A_BA | DC | \$3F0000 | ; | 2016 |
| A_92 | DC | \$0BC000 | ; | 376 | A_BB | DC | \$3D0000 | ; | 1952 |
| A_93 | DC | \$0B4000 | ; | 360 | A_BC | DC | \$330000 | ; | 1632 |
| A_94 | DC | \$08C000 | ; | 280 | A_BD | DC | \$310000 | ; | 1568 |
| A_95 | DC | \$084000 | ; | 264 | A_BE | DC | \$370000 | ; | 1760 |
| A_96 | DC | \$09C000 | ; | 312 | A_BF | DC | \$350000 | ; | 1696 |
| A_97 | DC | \$094000 | ; | 296 | A_C0 | DC | \$015800 | ; | 43 |
| A_98 | DC | \$0EC000 | ; | 472 | A_C1 | DC | \$014800 | ; | 41 |
| A_99 | DC | \$0E4000 | ; | 456 | A_C2 | DC | \$017800 | ; | 47 |
| A_9A | DC | \$0FC000 | ; | 504 | A_C3 | DC | \$016800 | ; | 45 |
| A_9B | DC | \$0F4000 | ; | 488 | A_C4 | DC | \$011800 | ; | 35 |
| A_9C | DC | \$0CC000 | ; | 408 | A_C5 | DC | \$010800 | ; | 33 |
| A_9D | DC | \$0C4000 | ; | 392 | A_C6 | DC | \$013800 | ; | 39 |
| A_9E | DC | \$0DC000 | ; | 440 | A_C7 | DC | \$012800 | ; | 37 |
| A_9F | DC | \$0D4000 | ; | 424 | A_C8 | DC | \$01D800 | ; | 59 |
| A_A0 | DC | \$560000 | ; | 2752 | A_C9 | DC | \$01C800 | ; | 57 |
| A_A1 | DC | \$520000 | ; | 2624 | A_CA | DC | \$01F800 | ; | 63 |
| A_A2 | DC | \$5E0000 | ; | 3008 | A_CB | DC | \$01E800 | ; | 61 |
| A_A3 | DC | \$5A0000 | ; | 2880 | A_CC | DC | \$019800 | ; | 51 |
| A_A4 | DC | \$460000 | ; | 2240 | A_CD | DC | \$018800 | ; | 49 |
| A_A5 | DC | \$420000 | ; | 2112 | A_CE | DC | \$01B800 | ; | 55 |
| A_A6 | DC | \$4E0000 | ; | 2496 | A_CF | DC | \$01A800 | ; | 53 |
| A_A7 | DC | \$4A0000 | ; | 2368 | A_D0 | DC | \$005800 | ; | 11 |
| A_A8 | DC | \$760000 | ; | 3776 | A_D1 | DC | \$004800 | ; | 9 |

Freescale Semiconductor, Inc.

ROM Table Listings

mu-Law / A-Law Expansion Tables

| | | | | | | | | | |
|------|----|----------|---|-----|------|----|----------|---|-----|
| A_D2 | DC | \$007800 | ; | 15 | A_FB | DC | \$03D000 | ; | 122 |
| A_D3 | DC | \$006800 | ; | 13 | A_FC | DC | \$033000 | ; | 102 |
| A_D4 | DC | \$001800 | ; | 3 | A_FD | DC | \$031000 | ; | 98 |
| A_D5 | DC | \$000800 | ; | 1 | A_FE | DC | \$037000 | ; | 110 |
| A_D6 | DC | \$003800 | ; | 7 | A_FF | DC | \$035000 | ; | 106 |
| A_D7 | DC | \$002800 | ; | 5 | | | | | |
| A_D8 | DC | \$00D800 | ; | 27 | | | | | |
| A_D9 | DC | \$00C800 | ; | 25 | | | | | |
| A_DA | DC | \$00F800 | ; | 31 | | | | | |
| A_DB | DC | \$00E800 | ; | 29 | | | | | |
| A_DC | DC | \$009800 | ; | 19 | | | | | |
| A_DD | DC | \$008800 | ; | 17 | | | | | |
| A_DE | DC | \$00B800 | ; | 23 | | | | | |
| A_DF | DC | \$00A800 | ; | 21 | | | | | |
| A_E0 | DC | \$056000 | ; | 172 | | | | | |
| A_E1 | DC | \$052000 | ; | 164 | | | | | |
| A_E2 | DC | \$05E000 | ; | 188 | | | | | |
| A_E3 | DC | \$05A000 | ; | 180 | | | | | |
| A_E4 | DC | \$046000 | ; | 140 | | | | | |
| A_E5 | DC | \$042000 | ; | 132 | | | | | |
| A_E6 | DC | \$04E000 | ; | 156 | | | | | |
| A_E7 | DC | \$04A000 | ; | 148 | | | | | |
| A_E8 | DC | \$076000 | ; | 236 | | | | | |
| A_E9 | DC | \$072000 | ; | 228 | | | | | |
| A_EA | DC | \$07E000 | ; | 252 | | | | | |
| A_EB | DC | \$07A000 | ; | 244 | | | | | |
| A_EC | DC | \$066000 | ; | 204 | | | | | |
| A_ED | DC | \$062000 | ; | 196 | | | | | |
| A_EE | DC | \$06E000 | ; | 220 | | | | | |
| A_EF | DC | \$06A000 | ; | 212 | | | | | |
| A_F0 | DC | \$02B000 | ; | 86 | | | | | |
| A_F1 | DC | \$029000 | ; | 82 | | | | | |
| A_F2 | DC | \$02F000 | ; | 94 | | | | | |
| A_F3 | DC | \$02D000 | ; | 90 | | | | | |
| A_F4 | DC | \$023000 | ; | 70 | | | | | |
| A_F5 | DC | \$021000 | ; | 66 | | | | | |
| A_F6 | DC | \$027000 | ; | 78 | | | | | |
| A_F7 | DC | \$025000 | ; | 74 | | | | | |
| A_F8 | DC | \$03B000 | ; | 118 | | | | | |
| A_F9 | DC | \$039000 | ; | 114 | | | | | |
| A_FA | DC | \$03F000 | ; | 126 | | | | | |

SINE WAVE TABLE

This sine wave table is normally used by FFT routines that use bit-reversed address pointers. This table can be used as it is for up to 512 point FFTs; however, for larger FFTs, the table must be copied to a different memory location to allow the Reverse-carry addressing mode to be used (see REVERSE-CARRY MODIFIER (Mn = \$0000) in the *DSP56001 User's Manual* for additional information).

Table A-2 Sine Wave Table

| | | | | | |
|---------|----------|-----------------|---------|----------|-----------------|
| ORG | Y:\$100 | | S_1A DC | \$4C3FE0 | ; +0.5956993103 |
| | | | S_1B DC | \$4EBFE9 | ; +0.6152315736 |
| | | | S_1C DC | \$5133CD | ; +0.6343932748 |
| S_00 DC | \$000000 | ; +0.0000000000 | S_1D DC | \$539B2B | ; +0.6531729102 |
| S_01 DC | \$03242B | ; +0.0245412998 | S_1E DC | \$55F5A5 | ; +0.6715589762 |
| S_02 DC | \$0647D9 | ; +0.0490676016 | S_1F DC | \$5842DD | ; +0.6895405054 |
| S_03 DC | \$096A90 | ; +0.0735644996 | S_20 DC | \$5A827A | ; +0.7071068287 |
| S_04 DC | \$0C8BD3 | ; +0.0980170965 | S_21 DC | \$5CB421 | ; +0.7242470980 |
| S_05 DC | \$0FAB27 | ; +0.1224106997 | S_22 DC | \$5ED77D | ; +0.7409511805 |
| S_06 DC | \$12C810 | ; +0.1467303932 | S_23 DC | \$60EC38 | ; +0.7572088242 |
| S_07 DC | \$15E214 | ; +0.1709619015 | S_24 DC | \$62F202 | ; +0.7730104923 |
| S_08 DC | \$18F8B8 | ; +0.1950902939 | S_25 DC | \$64E889 | ; +0.7883464098 |
| S_09 DC | \$1C0B82 | ; +0.2191012055 | S_26 DC | \$66CF81 | ; +0.8032075167 |
| S_0A DC | \$1F19F9 | ; +0.2429800928 | S_27 DC | \$68A69F | ; +0.8175848722 |
| S_0B DC | \$2223A5 | ; +0.2667128146 | S_28 DC | \$6A6D99 | ; +0.8314697146 |
| S_0C DC | \$25280C | ; +0.2902846038 | S_29 DC | \$6C2429 | ; +0.8448535204 |
| S_0D DC | \$2826B9 | ; +0.3136816919 | S_2A DC | \$6DCA0D | ; +0.8577286005 |
| S_0E DC | \$2B1F35 | ; +0.3368898928 | S_2B DC | \$6F5F03 | ; +0.8700870275 |
| S_0F DC | \$2E110A | ; +0.3598949909 | S_2C DC | \$70E2CC | ; +0.8819212914 |
| S_10 DC | \$30FBC5 | ; +0.3826833963 | S_2D DC | \$72552D | ; +0.8932244182 |
| S_11 DC | \$33DEF3 | ; +0.4052414000 | S_2E DC | \$73B5EC | ; +0.9039893150 |
| S_12 DC | \$36BA20 | ; +0.4275551140 | S_2F DC | \$7504D3 | ; +0.9142097235 |
| S_13 DC | \$398CDD | ; +0.4496113062 | S_30 DC | \$7641AF | ; +0.9238795042 |
| S_14 DC | \$3C56BA | ; +0.4713967144 | S_31 DC | \$776C4F | ; +0.9329928160 |
| S_15 DC | \$3F174A | ; +0.4928981960 | S_32 DC | \$788484 | ; +0.9415441155 |
| S_16 DC | \$41CE1E | ; +0.5141026974 | S_33 DC | \$798A24 | ; +0.9495282173 |
| S_17 DC | \$447ACD | ; +0.5349975824 | S_34 DC | \$7A7D05 | ; +0.9569402933 |
| S_18 DC | \$471CED | ; +0.5555701852 | S_35 DC | \$7B5D04 | ; +0.9637761116 |
| S_19 DC | \$49B415 | ; +0.5758082271 | | | |

Freescale Semiconductor, Inc.

ROM Table Listings

Sine Wave Table

| | | | | | |
|---------|-----------|-----------------|---------|----------|-----------------|
| S_36 DC | \$7C29FC | ; +0.9700313210 | S_5F DC | \$5CB421 | ; +0.7242470980 |
| S_37 DC | \$7CE3CF | ; +0.9757022262 | S_60 DC | \$5A827A | ; +0.7071068287 |
| S_38 DC | \$7D8A5F | ; +0.9807853103 | S_61 DC | \$5842DD | ; +0.6895405054 |
| S_39 DC | \$7E1D94 | ; +0.9852777123 | S_62 DC | \$55F5A5 | ; +0.6715589762 |
| S_3A DC | \$7E9D56 | ; +0.9891765118 | S_63 DC | \$539B2B | ; +0.6531729102 |
| S_3B DC | \$7F0992 | ; +0.9924796224 | S_64 DC | \$5133CD | ; +0.6343932748 |
| S_3C DC | \$7F6237 | ; +0.9951847792 | S_65 DC | \$4EBFE9 | ; +0.6152315736 |
| S_3D DC | \$7FA737 | ; +0.9972904921 | S_66 DC | \$4C3FE0 | ; +0.5956993103 |
| S_3E DC | \$7FD888 | ; +0.9987955093 | S_67 DC | \$49B415 | ; +0.5758082271 |
| S_3F DC | \$7FF622 | ; +0.9996988773 | S_68 DC | \$471CED | ; +0.5555701852 |
| S_40 DC | \$7FFFFFF | ; +0.9999998808 | S_69 DC | \$447ACD | ; +0.5349975824 |
| S_41 DC | \$7FF622 | ; +0.9996988773 | S_6A DC | \$41CE1E | ; +0.5141026974 |
| S_42 DC | \$7FD888 | ; +0.9987955093 | S_6B DC | \$3F174A | ; +0.4928981960 |
| S_43 DC | \$7FA737 | ; +0.9972904921 | S_6C DC | \$3C56BA | ; +0.4713967144 |
| S_44 DC | \$7F6237 | ; +0.9951847792 | S_6D DC | \$398CDD | ; +0.4496113062 |
| S_45 DC | \$7F0992 | ; +0.9924796224 | S_6E DC | \$36BA20 | ; +0.4275551140 |
| S_46 DC | \$7E9D56 | ; +0.9891765118 | S_6F DC | \$33DEF3 | ; +0.4052414000 |
| S_47 DC | \$7E1D94 | ; +0.9852777123 | S_70 DC | \$30FBC5 | ; +0.3826833963 |
| S_48 DC | \$7D8A5F | ; +0.9807853103 | S_71 DC | \$2E110A | ; +0.3598949909 |
| S_49 DC | \$7CE3CF | ; +0.9757022262 | S_72 DC | \$2B1F35 | ; +0.3368898928 |
| S_4A DC | \$7C29FC | ; +0.9700313210 | S_73 DC | \$2826B9 | ; +0.3136816919 |
| S_4B DC | \$7B5D04 | ; +0.9637761116 | S_74 DC | \$25280C | ; +0.2902846038 |
| S_4C DC | \$7A7D05 | ; +0.9569402933 | S_75 DC | \$2223A5 | ; +0.2667128146 |
| S_4D DC | \$798A24 | ; +0.9495282173 | S_76 DC | \$1F19F9 | ; +0.2429800928 |
| S_4E DC | \$788484 | ; +0.9415441155 | S_77 DC | \$1C0B82 | ; +0.2191012055 |
| S_4F DC | \$776C4F | ; +0.9329928160 | S_78 DC | \$18F8B8 | ; +0.1950902939 |
| S_50 DC | \$7641AF | ; +0.9238795042 | S_79 DC | \$15E214 | ; +0.1709619015 |
| S_51 DC | \$7504D3 | ; +0.9142097235 | S_7A DC | \$12C810 | ; +0.1467303932 |
| S_52 DC | \$73B5EC | ; +0.9039893150 | S_7B DC | \$0FAB27 | ; +0.1224106997 |
| S_53 DC | \$72552D | ; +0.8932244182 | S_7C DC | \$0C8BD3 | ; +0.0980170965 |
| S_54 DC | \$70E2CC | ; +0.8819212914 | S_7D DC | \$096A90 | ; +0.0735644996 |
| S_55 DC | \$6F5F03 | ; +0.8700870275 | S_7E DC | \$0647D9 | ; +0.0490676016 |
| S_56 DC | \$6DCA0D | ; +0.8577286005 | S_7F DC | \$03242B | ; +0.0245412998 |
| S_57 DC | \$6C2429 | ; +0.8448535204 | S_80 DC | \$000000 | ; +0.0000000000 |
| S_58 DC | \$6A6D99 | ; +0.8314697146 | S_81 DC | \$FCDBD5 | ; -0.0245412998 |
| S_59 DC | \$68A69F | ; +0.8175848722 | S_82 DC | \$F9B827 | ; -0.0490676016 |
| S_5A DC | \$66CF81 | ; +0.8032075167 | S_83 DC | \$F69570 | ; -0.0735644996 |
| S_5B DC | \$64E889 | ; +0.7883464098 | S_84 DC | \$F3742D | ; -0.0980170965 |
| S_5C DC | \$62F202 | ; +0.7730104923 | S_85 DC | \$F054D9 | ; -0.1224106997 |
| S_5D DC | \$60EC38 | ; +0.7572088242 | S_86 DC | \$ED37F0 | ; -0.1467303932 |
| S_5E DC | \$5ED77D | ; +0.7409511805 | S_87 DC | \$EA1DEC | ; -0.1709619015 |

| | | | | | | | |
|---------|----------|---|---------------|---------|----------|---|---------------|
| S_88 DC | \$E70748 | ; | -0.1950902939 | S_B1 DC | \$8893B1 | ; | -0.9329928160 |
| S_89 DC | \$E3F47E | ; | -0.2191012055 | S_B2 DC | \$877B7C | ; | -0.9415441155 |
| S_8A DC | \$E0E607 | ; | -0.2429800928 | S_B3 DC | \$8675DC | ; | -0.9495282173 |
| S_8B DC | \$DDDC5B | ; | -0.2667128146 | S_B4 DC | \$8582FB | ; | -0.9569402933 |
| S_8C DC | \$DAD7F4 | ; | -0.2902846038 | S_B5 DC | \$84A2FC | ; | -0.9637761116 |
| S_8D DC | \$D7D947 | ; | -0.3136816919 | S_B6 DC | \$83D604 | ; | -0.9700313210 |
| S_8E DC | \$D4E0CB | ; | -0.3368898928 | S_B7 DC | \$831C31 | ; | -0.9757022262 |
| S_8F DC | \$D1EEF6 | ; | -0.3598949909 | S_B8 DC | \$8275A1 | ; | -0.9807853103 |
| S_90 DC | \$CF043B | ; | -0.3826833963 | S_B9 DC | \$81E26C | ; | -0.9852777123 |
| S_91 DC | \$CC210D | ; | -0.4052414000 | S_BA DC | \$8162AA | ; | -0.9891765118 |
| S_92 DC | \$C945E0 | ; | -0.4275551140 | S_BB DC | \$80F66E | ; | -0.9924796224 |
| S_93 DC | \$C67323 | ; | -0.4496113062 | S_BC DC | \$809DC9 | ; | -0.9951847792 |
| S_94 DC | \$C3A946 | ; | -0.4713967144 | S_BD DC | \$8058C9 | ; | -0.9972904921 |
| S_95 DC | \$C0E8B6 | ; | -0.4928981960 | S_BE DC | \$802778 | ; | -0.9987955093 |
| S_96 DC | \$BE31E2 | ; | -0.5141026974 | S_BF DC | \$8009DE | ; | -0.9996988773 |
| S_97 DC | \$BB8533 | ; | -0.5349975824 | S_C0 DC | \$800000 | ; | -1.0000000000 |
| S_98 DC | \$B8E313 | ; | -0.5555701852 | S_C1 DC | \$8009DE | ; | -0.9996988773 |
| S_99 DC | \$B64BEB | ; | -0.5758082271 | S_C2 DC | \$802778 | ; | -0.9987955093 |
| S_9A DC | \$B3C020 | ; | -0.5956993103 | S_C3 DC | \$8058C9 | ; | -0.9972904921 |
| S_9B DC | \$B14017 | ; | -0.6152315736 | S_C4 DC | \$809DC9 | ; | -0.9951847792 |
| S_9C DC | \$AECC33 | ; | -0.6343932748 | S_C5 DC | \$80F66E | ; | -0.9924796224 |
| S_9D DC | \$AC64D5 | ; | -0.6531729102 | S_C6 DC | \$8162AA | ; | -0.9891765118 |
| S_9E DC | \$AA0A5B | ; | -0.6715589762 | S_C7 DC | \$81E26C | ; | -0.9852777123 |
| S_9F DC | \$A7BD23 | ; | -0.6895405054 | S_C8 DC | \$8275A1 | ; | -0.9807853103 |
| S_A0 DC | \$A57D86 | ; | -0.7071068287 | S_C9 DC | \$831C31 | ; | -0.9757022262 |
| S_A1 DC | \$A34BDF | ; | -0.7242470980 | S_CA DC | \$83D604 | ; | -0.9700313210 |
| S_A2 DC | \$A12883 | ; | -0.7409511805 | S_CB DC | \$84A2FC | ; | -0.9637761116 |
| S_A3 DC | \$9F13C8 | ; | -0.7572088242 | S_CC DC | \$8582FB | ; | -0.9569402933 |
| S_A4 DC | \$9D0DFE | ; | -0.7730104923 | S_CD DC | \$8675DC | ; | -0.9495282173 |
| S_A5 DC | \$9B1777 | ; | -0.7883464098 | S_CE DC | \$877B7C | ; | -0.9415441155 |
| S_A6 DC | \$99307F | ; | -0.8032075167 | S_CF DC | \$8893B1 | ; | -0.9329928160 |
| S_A7 DC | \$975961 | ; | -0.8175848722 | S_D0 DC | \$89BE51 | ; | -0.9238795042 |
| S_A8 DC | \$959267 | ; | -0.8314697146 | S_D1 DC | \$8AFB2D | ; | -0.9142097235 |
| S_A9 DC | \$93DBD7 | ; | -0.8448535204 | S_D2 DC | \$8C4A14 | ; | -0.9039893150 |
| S_AA DC | \$9235F3 | ; | -0.8577286005 | S_D3 DC | \$8DAAD3 | ; | -0.8932244182 |
| S_AB DC | \$90A0FD | ; | -0.8700870275 | S_D4 DC | \$8F1D34 | ; | -0.8819212914 |
| S_AC DC | \$8F1D34 | ; | -0.8819212914 | S_D5 DC | \$90A0FD | ; | -0.8700870275 |
| S_AD DC | \$8DAAD3 | ; | -0.8932244182 | S_D6 DC | \$9235F3 | ; | -0.8577286005 |
| S_AE DC | \$8C4A14 | ; | -0.9039893150 | S_D7 DC | \$93DBD7 | ; | -0.8448535204 |
| S_AF DC | \$8AFB2D | ; | -0.9142097235 | S_D8 DC | \$959267 | ; | -0.8314697146 |
| S_B0 DC | \$89BE51 | ; | -0.9238795042 | S_D9 DC | \$975961 | ; | -0.8175848722 |

ROM Table Listings

Sine Wave Table

| | | | | |
|------|----|----------|---|---------------|
| S_DA | DC | \$99307F | ; | -0.8032075167 |
| S_DB | DC | \$9B1777 | ; | -0.7883464098 |
| S_DC | DC | \$9D0DFE | ; | -0.7730104923 |
| S_DD | DC | \$9F13C8 | ; | -0.7572088242 |
| S_DE | DC | \$A12883 | ; | -0.7409511805 |
| S_DF | DC | \$A34BDF | ; | -0.7242470980 |
| S_E0 | DC | \$A57D86 | ; | -0.7071068287 |
| S_E1 | DC | \$A7BD23 | ; | -0.6895405054 |
| S_E2 | DC | \$AA0A5B | ; | -0.6715589762 |
| S_E3 | DC | \$AC64D5 | ; | -0.6531729102 |
| S_E4 | DC | \$AECC33 | ; | -0.6343932748 |
| S_E5 | DC | \$B14017 | ; | -0.6152315736 |
| S_E6 | DC | \$B3C020 | ; | -0.5956993103 |
| S_E7 | DC | \$B64BEB | ; | -0.5758082271 |
| S_E8 | DC | \$B8E313 | ; | -0.5555701852 |
| S_E9 | DC | \$BB8533 | ; | -0.5349975824 |
| S_EA | DC | \$BE31E2 | ; | -0.5141026974 |
| S_EB | DC | \$C0E8B6 | ; | -0.4928981960 |
| S_EC | DC | \$C3A946 | ; | -0.4713967144 |
| S_ED | DC | \$C67323 | ; | -0.4496113062 |
| S_EE | DC | \$C945E0 | ; | -0.4275551140 |
| S_EF | DC | \$CC210D | ; | -0.4052414000 |
| S_F0 | DC | \$CF043B | ; | -0.3826833963 |
| S_F1 | DC | \$D1EEF6 | ; | -0.3598949909 |
| S_F2 | DC | \$D4E0CB | ; | -0.3368898928 |
| S_F3 | DC | \$D7D947 | ; | -0.3136816919 |
| S_F4 | DC | \$DAD7F4 | ; | -0.2902846038 |
| S_F5 | DC | \$DDDC5B | ; | -0.2667128146 |
| S_F6 | DC | \$E0E607 | ; | -0.2429800928 |
| S_F7 | DC | \$E3F47E | ; | -0.2191012055 |
| S_F8 | DC | \$E70748 | ; | -0.1950902939 |
| S_F9 | DC | \$EA1DEC | ; | -0.1709619015 |
| S_FA | DC | \$ED37F0 | ; | -0.1467303932 |
| S_FB | DC | \$F054D9 | ; | -0.1224106997 |
| S_FC | DC | \$F3742D | ; | -0.0980170965 |
| S_FD | DC | \$F69570 | ; | -0.0735644996 |
| S_FE | DC | \$F9B827 | ; | -0.0490676016 |
| S_FF | DC | \$FCDBD5 | ; | -0.0245412998 |




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