GD4066B

QUAD BILATERAL SWITCHES

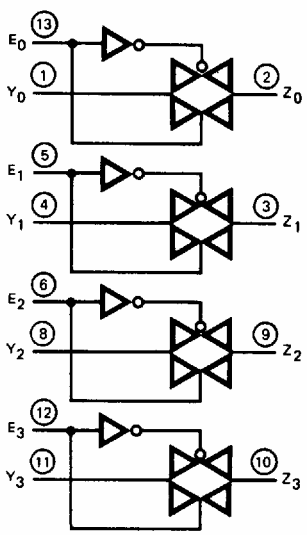
DESCRIPTION – The 4066B has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch; high impedance between Y_n and Z_n (OFF condition).

- **DIGITAL OR ANALOG SIGNAL SWITCHING**
- **INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)**

PIN NAMES

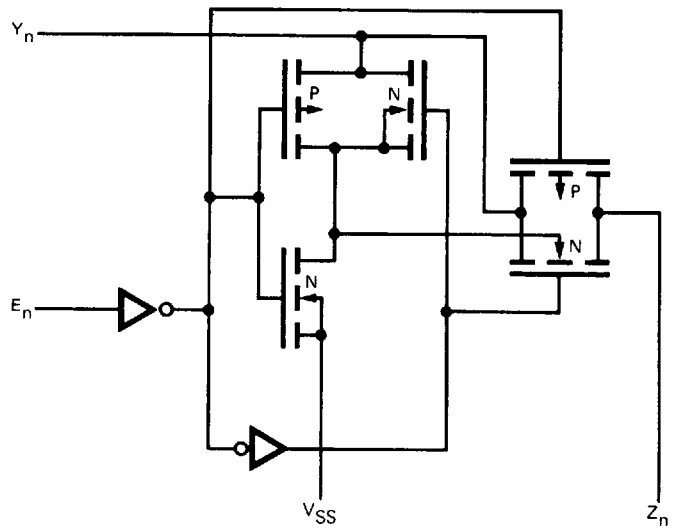
E_0–E_3	Enable Inputs
Y_0–Y_3	Input/Output Terminals
Z_0–Z_3	Input/Output Terminals

LOGIC SYMBOL

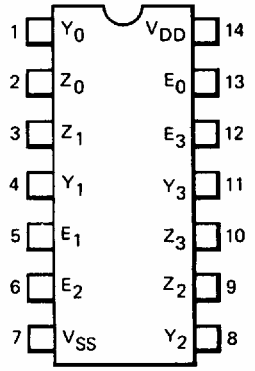


V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Numbers

LOGIC DIAGRAM (1/4 OF A 4066B)



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE.
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		190	900		100	450		80	250	Ω	MIN	$E_n = V_{DD}$ R_L = 10 kΩ to $V_{DD}/2$ $V_{is} = V_{DD}$ to V_{SS}
				270	1000		120	500		80	280		25°C	
				330	1090		170	520		130	300		MAX	
		XM		160	850		85	400		60	220	Ω	MIN.	
				270	1000		120	500		80	280		25°C	
				360	1150		190	550		145	320		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	$E_n = V_{DD}$ R_L = 10 kΩ to $V_{DD}/2$ $V_{is} = V_{DD}$ or V_{SS}
I_Z	OFF State Leakage Current	XC									±300	nA	MIN, 25°C	$E_n = V_{SS}$ $V_{is} = V_{DD}$ or V_{SS} $V_{os} = V_{SS}$ or V_{DD}
											±1000		MAX	
		XM									±100		MIN, 25°C	
											±1000		MAX	
I_{DD}	Quiescent Power Supply Dissipation	XC			1			2			4	μA	MIN, 25°C	All inputs at V_{DD} or V_{SS}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		8 8	45 45		3 4	30 30		2 2	20 20	ns	C_L = 50 pF, R_L = 200 Ω to V_{SS} Input Transition Times ≤ 20 ns E_n = V_{DD} V_{is} = V_{DD} (square wave)
t_{PZL} t_{PZH}	Output Enable Time		32 32	125 125		16 16	60 60		13 13	50 50	ns	C_L = 50 pF, R_L = 1 kΩ to V_{SS} or V_{DD} E_n = V_{DD} (square wave) Input Transition Times ≤ 20 ns V_{is} = V_{DD} or V_{SS}
t_{PLZ} t_{PHZ}	Output Disable Time		380 380			380 380			400 400		ns	
	Distortion, Sine Wave Response		0.4			0.4			0.4		%	R_L = 10 kΩ Input Frequency = 1 kHz E_n = V_{DD} V_{is} = V_{DD}/2 (sine wave) p-p
	Crosstalk Between Any Two Switches					0.9					MHz	R_L = 1 kΩ E_A = V_{DD}, E_B = V_{SS} V_{is} = V_{DD}/2 (sine wave) p-p 20 Log_{10} [V_{os} (B)/V_{is} (A)] = -50 dB
	Crosstalk, Enable Input to Output					50					mV	Input Transition Times ≤ 20 ns $R_{L(OUT)}$ = 1 kΩ $R_{L(IN)}$ = 50 Ω E_n = V_{DD} (square wave)
	OFF State Feedthrough					1.25					MHz	R_L = 1 kΩ, E_n = V_{SS} V_{is} = V_{DD}/2 (sine wave) p-p 20 Log_{10} (V_{os}/V_{is}) = -50 dB
	ON State Frequency Response					40					MHz	R_L = 1 kΩ V_{is} = V_{DD}/2 (sine wave) p-p E_n = V_{DD}, 20 Log_{10} (V_{os}/V_{os} @ 1 kHz) = -3 dB
f_{MAX}	Enable Input Frequency (Note 4)					10					MHz	C_L = 50 pF, R_L = 1 kΩ Input Transition Times ≤ 20 ns E_n = V_{DD} (square wave) V_{os} = V_{is}/2 at DC V_{is} = V_{DD}
C_{is}	Input Switch Capacitance					4					pF	V_{DD} = 10 V E_n = V_{SS} V_{is} = Open 100 kHz or 1 MHz Bridge
C_{os}	Output Switch Capacitance					4					pF	
C_{ios}	Feedthrough Switch Capacitance					0.2					pF	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11 the voltage drop across the bidirectional switch must not exceed 0.5 V at $T_A \leq 25°C$, or 0.3 V at $T_A > 25°C$. No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.