LSI/CSI

LS7066

24 BIT MULTIMODE COUNTER

FEATURES:

- Microprocessor Compatible Three State I/O Bus.
- Programmable modes are: Binary, BCD, 24 hour clock up, down, ÷ N, x4 quadrature and single cycle. These modes can co-exist in different combinations.
- DC to 4 MHz
- 24-Bit comparator for pre-set count comparsion.
- Readable status register.
- Input/Output TTL compatible.
- Single +5VDC power supply.
- 20 pin Plastic Dip.

GENERAL DESCRIPTION

The LS7066 is a monolithic, ion implanted MOS 24-bit counter that can be programmed to operate in several different modes. The operating mode is set up by writing control words into internal control registers (see figure 8). There are three 6-bit and one 2-bit control registers for setting up the circuit functional characteristics. In addition to the control registers, there is a 5-bit output status register (OSR) that indicates the current counter status. The LS7066 communicates with external circuits through an 8-bit three state I/O bus. Control and data words are written into the LS7066 through the bus. In addition to the I/O bus, there are a number of discrete inputs and outputs to facilitate instantaneous hardware based control functions and instantaneous status indication.

REGISTER DESCRIPTION

The following hardware registers are addressable through the I/O bus. The addressing modes of these registers are listed in Table 1.

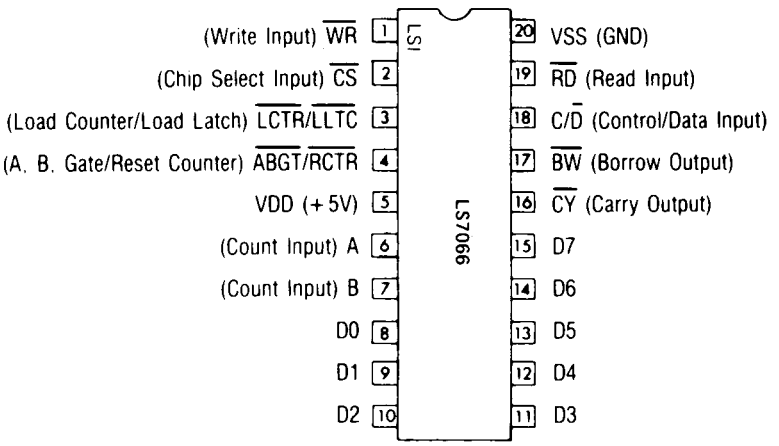
Output Status Register (OSR). The OSR is a 5-bit read only register that holds the counter status information at any given time. When read, the OSR bit 0 through 4 are placed on the I/O bus, D0 through D4 respectively. The OSR bits contain the status information as follows:

Bit 0: Borrow toggle flip-flop (BWT). This flip-flop changes state every time the counter (CNTR) underflows.

Bit 1: Carry toggle flip-flop (CYT). This flip-flop changes state every time the CNTR overflows.

Bit 2: Compare toggle flip-flop (COMPT). This flip-flop changes state every time CNTR equals to preset register (PR0-PR2).

CONNECTION DIAGRAM — TOP VIEW
STANDARD 20 PIN PLASTIC DIP



Bit 3: Sign register. The sign register is set to "1" whenever CNTR underflows indicating that a borrow has taken place. It resets to "0" when CNTR overflows indicating a carry. This register is also reset whenever CNTR is reset.

Bit 4: UP/DN Indicator. In quadrature mode, when set to "1," this bit indicates that the counter is operating in the UP count mode. When reset to "0," it indicates that the counter is in DOWN count mode. When not in quadrature mode this bit is forced to a "1."

Preset Register (PR). The preset register is made of three 8-bit registers, PR0, PR1 and PR2, in concatenation to make one 24-bit register. Data is written into the 3 individual registers with one register being addressed at a time. The 24-bit data can then be transferred into the CNTR all at once.

Output Latch (OL). The output latch is a 24-bit register made of three 8-bit registers OL0, OL1 and OL2. Data from the CNTR can be transferred all at once into the OL. OL0, OL1 and OL2 can then be individually addressed to be read on the I/O bus.

Master Control Register (MCR). The MCR is a 6-bit write only register. A control word written into the MCR sets up the chip characteristics in the following manner:

D0 = 1: Resets the PR/OL address counter.
D1 = 1: Loads the OL with the CNTR value.
D2 = 1: Resets the CNTR borrow toggle flip-flop, the carry toggle flip-flop and the sign register.
D3 = 1: Loads the CNTR with the PR value.
D4 = 1: Resets the compare toggle flip-flop.
D5 = 1: Master reset. The master reset presets the PR to all "1's" and resets the following: the CNTR, all control registers (excepting the MCR), the OL and the OSR. Note that a master reset overrides D1 and D3.

Input Control Register (ICR). The ICR is a 6-bit write only register that controls the operating modes of the 4 discrete inputs called A, B, $\overline{ABGT}/\overline{RCTR}$ and $\overline{LCTR}/\overline{LLTC}$. A counter decrement or increment may also be caused by writing the proper control word into the ICR. The functions of the different bits of the control word are as follows:

D0 = 0: Sets up A as up count input and B as down count input.
D0 = 1: Sets up A as the count input and B as the count up/down direction control input. (See note 1)
D1 = 1: Increments CNTR once. (See note 2)
D2 = 1: Decrements CNTR once.(See note 2)
D3 = 0: Disables inputs A and B.
D3 = 1: Enables inputs A and B.
D4 = 0: $\overline{ABGT}/\overline{RCTR}$ input is set up as the counter external reset input.
D4 = 1: $\overline{ABGT}/\overline{RCTR}$ input is set up as the A and B enable/disable gate.
D5 = 0: $\overline{LCTR}/\overline{LLTC}$ input is set up as the external load command input for the CNTR.
D5 = 1: $\overline{LCTR}/\overline{LLTC}$ input is set up as the external load command input for the OL.

NOTE 1: When B is Setup as UP/DN control input, B may switch only when A is high.

NOTE 2: When incrementing or decrementing the CNTR by writing into the ICR, inputs A and B, if enabled, must be held high.

Output/Counter Control Register (OCCR). The OCCR is a 6-bit write only register. A control word written into the OCCR sets up the counter and the output characteristics in the following manner:

D0 = 0: Sets counter to binary mode.
D0 = 1: Sets counter to BCD mode.
D1 = 1: Sets counter to non-recycle mode. In this mode, the counter counts for only one cycle beginning with a counter "reset" or "load" command and ending with the generation of a carry or a borrow. Following that, the counter is inhibited until a new reset or load command is applied.
D2 = 1: Sets counter to divide by N mode.
D3 = 1: Sets counter to 24 hour clock mode.(See note 3)
D4, D5: These two bits control the $\overline{CY}$ and $\overline{BW}$ output lines as follows:

D5	D4	
0	0	Enables active low carry and borrow on $\overline{CY}$ and $\overline{BW}$ respectively.
0	1	Enables the carry and borrow toggle flip-flops on $\overline{CY}$ and $\overline{BW}$ respectively.
1	0	Enables active high carry and borrow on $\overline{CY}$ and $\overline{BW}$ respectively.
1	1	Enables comparator output on $\overline{CY}$ and compare toggle flip-flop on $\overline{BW}$ respectively.

NOTE 3: 24 hour mode overrides binary or BCD mode.

Quadrature Register (QR). The QR is a 2-bit register that enables inputs A and B to count in the X4 quadrature mode. In this mode, "A clocks" leading "B clocks," generate internal up clocks whereas "B clocks" leading "A clocks" generate internal down clocks.

An internal clock is generated for every transition of either A or B clock. The QR Control word assignment is as follows:

D0 = 0: Disables quadrature mode
D0, D1=1 Enables quadrature mode

TABLE 1 - Register Addressing Modes

D7	D6	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	COMMENT
X	X	X	X	X	1	Disable Chip.
0	0	1	1	⊓	0	Write to Master Control Register (MCR).
0	1	1	1	⊓	0	Write to input control register (ICR).
1	0	1	1	⊓	0	Write to output/counter control register (OCCR).
1	1	1	1	⊓	0	Write to quadrature register (QR).
X	X	0	1	⊓	0	Write to preset register (PR) and increment register address counter. (See note 4)
X	X	0	⊓	1	0	Read output latch (OL) and increment register address counter. (See note 4)
X	X	1	⊓	1	0	Read output status register (OSR).

X = irrelevant

⊓ = Negative Pulse

NOTE 4: Following any control read/write operation a data Read/Write sequence must be preceded by an "Address Counter" reset instruction.

I/O Description: (See register description for I/O Programming.)

DataBus (D0-D7) (Pin 8-Pin 15). The 8-line data bus is a three-state I/O bus for interfacing with the system bus.

$\overline{CS}$ (Chip Select Input) (Pin 2). A logical "0" at this input enables the chip for Read and Write.

$\overline{RD}$ (Read Input) (Pin 19). A logical "0" at this input enables the OSR and the OL to be read on the data bus.

$\overline{WR}$ (Write Input) (Pin 1) A logical "0" at this input enables the data bus to be written into the control and data registers.

C/$\overline{D}$ (Control/Data Input) (Pin 18). A logical "1" at this input enables a control word to be written into one of the four control registers or, the OSR to be read on the I/O bus. A logical "0" on the other hand enables a data word to be written into the PR, or the OL to be read on the I/O bus.

A (Pin 6). Input A is a programmable count input capable of functioning in three different modes, such as, up count input, down count input and quadrature input.

B (Pin 7). Input B is also a programmable count input that can be programmed to function either as down count input, or count direction control gate for input A, or quadrature input. When B is programmed as count direction control gate, B = 0 enables A as the UP Count input and B = 1 enables A as the DN Count input.

$\overline{ABGT}$/$\overline{RCTR}$ (Pin 4) This input may be programmed to function as either inputs A and B enable gate or as external counter reset input. A logical "0" is the active level on this input.

$\overline{LCTR}$/$\overline{LLTC}$ (Pin 3) This input can be programmed to function as the external load command input for either the counter or the OL. When programmed as counter load input, the counter is loaded with the data contained in the PR. When programmed as the OL load input, the OL is loaded with the data contained in the counter. A logical "0" is the active level on this input.

$\overline{CY}$ (Pin 16). This output pin can be programmed to serve as one of the following:

A. $\overline{CY}$. True carry out (active "0").
B. CY. Complemented carry out (active "1").
C. CYT. Carry toggle flip-flip out.
D. $\overline{COMP}$. Comparator out (active "0").

$\overline{BW}$ (Pin 17). This output can be programmed to serve as one of the following:

A. $\overline{BW}$. True Borrow out (active "0").
B. BW. Complemented borrow out (active "1").
C. BWT. Borrow toggle flip-flop out.
D. COMPT. Compare toggle flip-flop out.

VDD (Pin 5). Supply voltage positive terminal.

VSS (Pin 20). Supply voltage negative terminal.

Absolute Maximum Ratings:

Parameter	Value	Units
Voltage at any pin with respect to VSS	−0.5 to 12	Volts
Operating Temperature	0 to +70	°C
Storage Temperature	−65 to +150	°C

DC Electrical Characteristics. (All voltages referenced to VSS. Unless otherwise specified, VDD = 5V.)

Parameter	Symbol	Min. Value	Max. Value	Unit	Remarks
Supply Voltage	VDD	4.75	5.5	Volts	–
Supply Current	IDD	20	35	mA	–
Input Low Voltage	V_{IL}	–	0.8	Volts	–
Input High Voltage	V_{IH}	2.0	–	Volts	–
Output Low Voltage	V_{OL}	–	0.4	Volts	@ 4mA Sink
Output High Voltage	V_{OH}	2.5	–	Volts	@ 200ua Source
Input Current	–	–	15	nA	Leakage Current
Output Source Current	I_{SRC}	200	–	uA	@V_{OH} = 2.5 V
Output Sink Current	I_{SNK}	4	–	mA	@ V_{OL} = 0.4 V
Data Bus Off-State Leakage Current	–	–	15	nA	

TRANSIENT CHARACTERISTICS. (See timing Diagrams in Fig. 2 through Fig. 7.)

Parameter	Symbol	Min. Value	Max. Value	Unit
Clock A/B "Low"	Tcl	125	–	ns
Clock A/B "High"	Tch	125	–	ns
Clock A/B Frequency (see note 5)	fc	–	4	MHz
Clock UP/DN Reversal Delay	Tudd	125	–	ns
$\overline{LCTR}$ Positive edge to the next A/B positive OR negative edge delay	T_{LC}	125	–	ns
Clock A/B to $\overline{CY}$/$\overline{BW}$/$\overline{COMP}$ "low" propagation delay	T_{CBL}		160	ns
Clock A/B to $\overline{CY}$/$\overline{BW}$/$\overline{COMP}$ "high" propagation delay	T_{CBH}		350	ns
$\overline{LCTR}$ and $\overline{LLTC}$ pulse width	T_{LCW}	70	–	ns
Clock A/B to CYT, BWT and COMPT "high" propagation delay	T_{TFH}		300	ns
Clock A/B to CYT, BWT and COMP "low" propagation delay	T_{TFL}		300	ns
$\overline{WR}$ pulse width	T_{WW}	400	–	ns
$\overline{RD}$ to data out delay	T_{RD}		400	ns
$\overline{WR}$ to $\overline{WR}$/$\overline{RD}$ Delay (See note 6)	T_{WD}	800	—	ns
Data set-up time for $\overline{WR}$	T_{DS}	0	–	–
Data hold time for $\overline{WR}$	T_{DH}	10	–	ns
$\overline{CS}$, C/$\overline{D}$ set-up time for $\overline{RD}$	T_{CRS}	0	–	ns
$\overline{CS}$, C/$\overline{D}$ hold time for $\overline{RD}$	T_{CRH}	10	–	ns
$\overline{CS}$, C/$\overline{D}$ set-up time for $\overline{WR}$	T_{CWS}	0	–	ns
$\overline{CS}$, hold time for $\overline{WR}$	T_{CWH}	10	–	ns
Quadrature Clock				
Clock A/B "low"	T_{CLQ}	1500	–	ns
Clock A/B "high"	T_{CHQ}	1500	–	ns
A and B phase delay	T_{PH}	750	–	ns
Clock A/B frequency	f_{CQ}	–	333	KHz

NOTE 5: In divide by N mode, the maximum clock frequency is 3MHZ.

NOTE 6: If a write to the LS7066 is followed by a RD/WR with TWD < 800 ns, erroneous data could be written into the LS7066 even if the second RD/WR was not directed to the LS7066. For systems with TWD < 800ns, the LS7066 RD/WR inputs must be gated with $\overline{CS}$ input as shown in fig. 9.

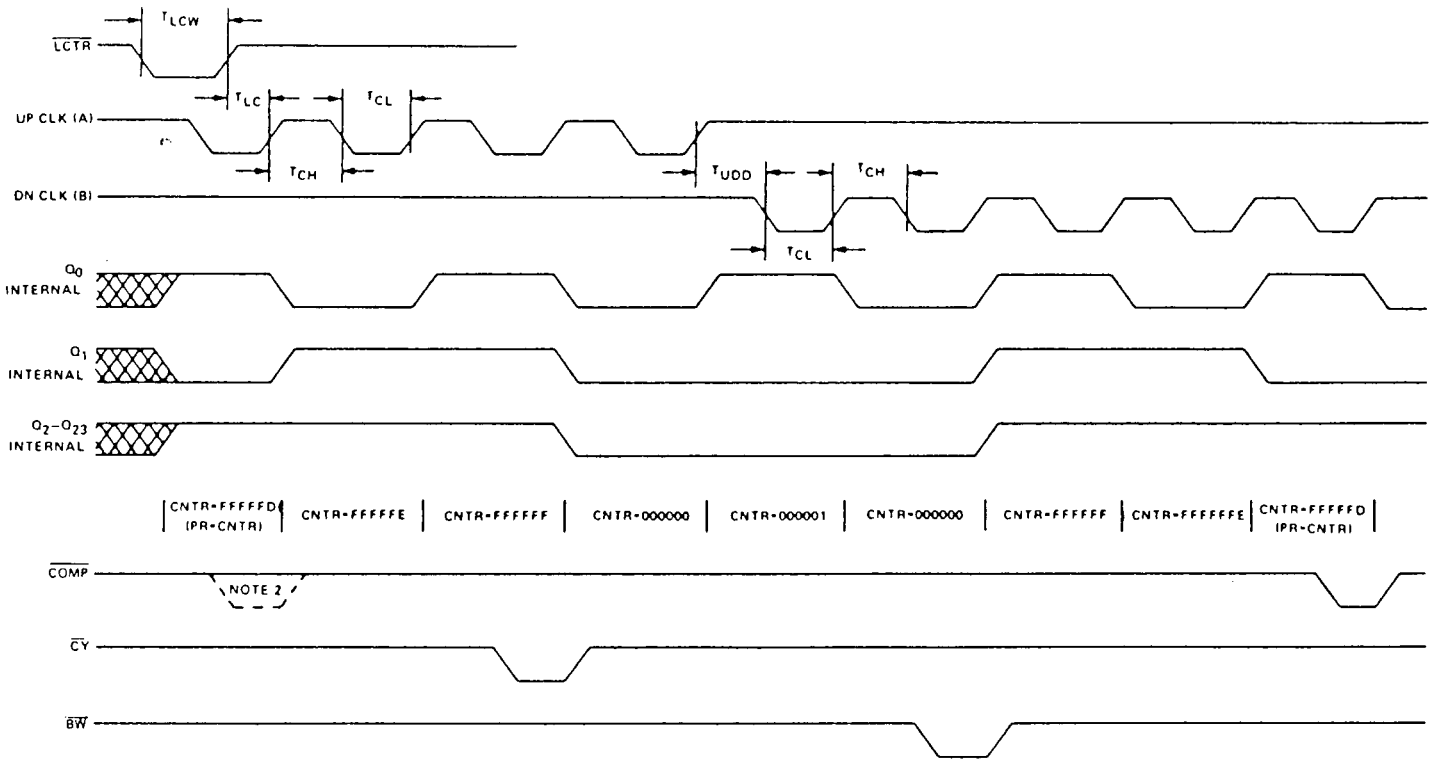


FIGURE 2 - LOAD COUNTER, UP CLOCK, DOWN CLOCK, COMPARE OUT, CARRY, BORROW

Note 1: The counter in this example, is assumed to be operating in the binary mode.

Note 2: No COMP output is generated here, although PR=CNTR. COMP output is disabled with a counter load command and enabled with the rising edge of the next clock, thus eliminating invalid COMP outputs whenever the CNTR is loaded from the PR.

Note 3: When up Clock is active, the DN clock should be held "HIGH" and vice verse.

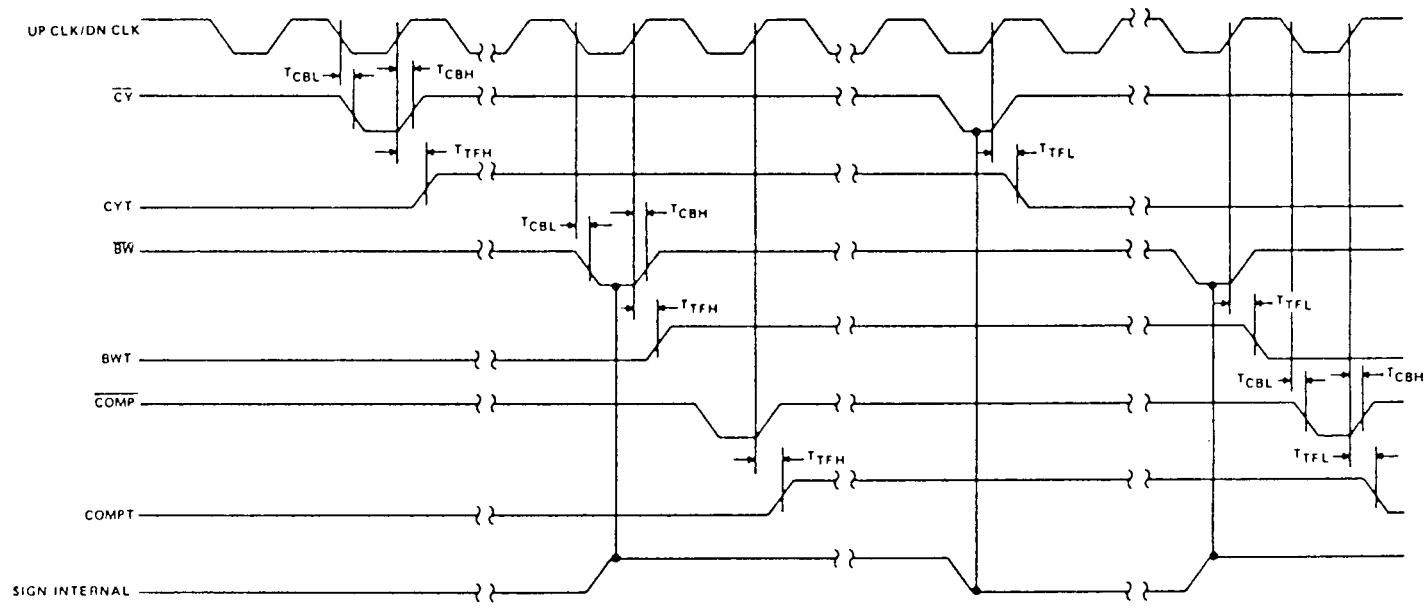


FIGURE 3 — CLOCK TO $\overline{CY}$/$\overline{BW}$ OUTPUT PROPAGATION DELAYS

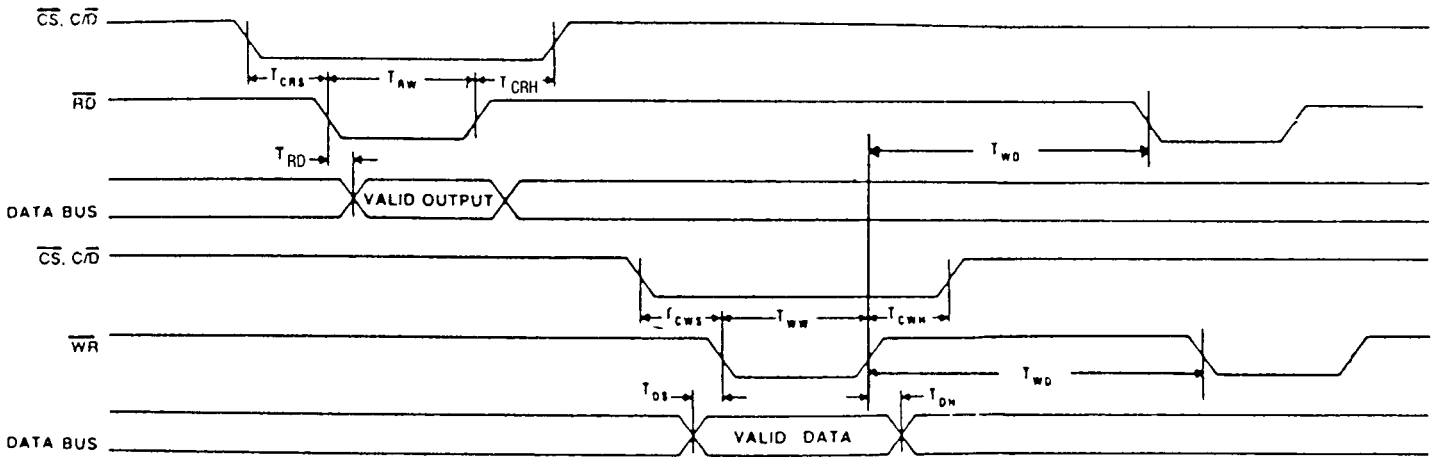
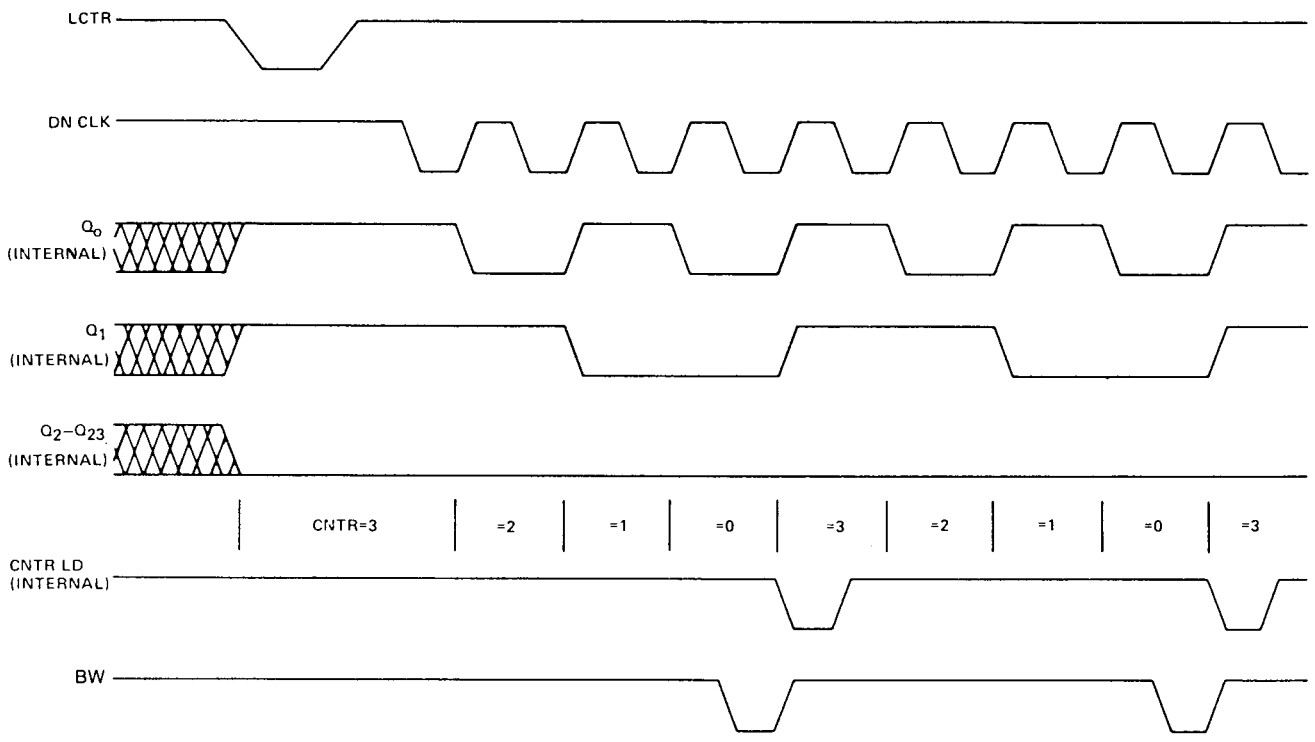


FIGURE 4 — READ/WRITE CYCLES



NOTE: EXAMPLE OF DIVIDE BY 4 IN DOWN COUNT MODE.

FIGURE 5 - DIVIDE BY N MODE

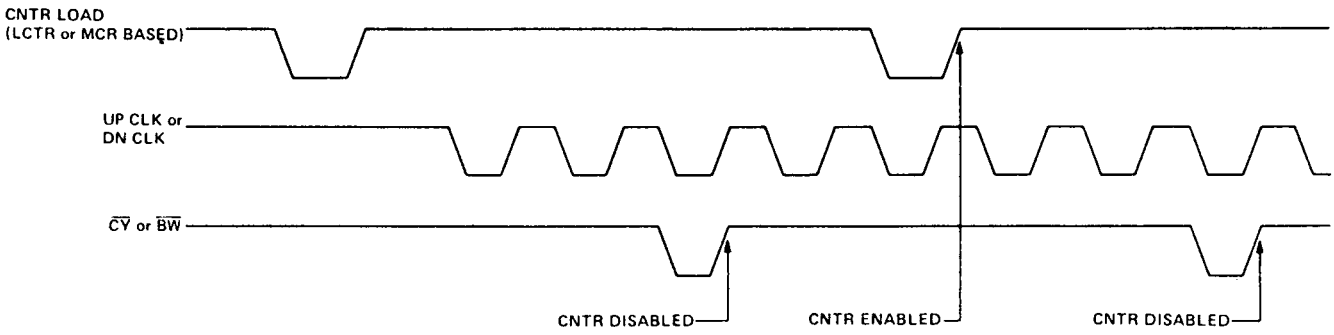


FIGURE 6 - CYCLE ONCE MODE

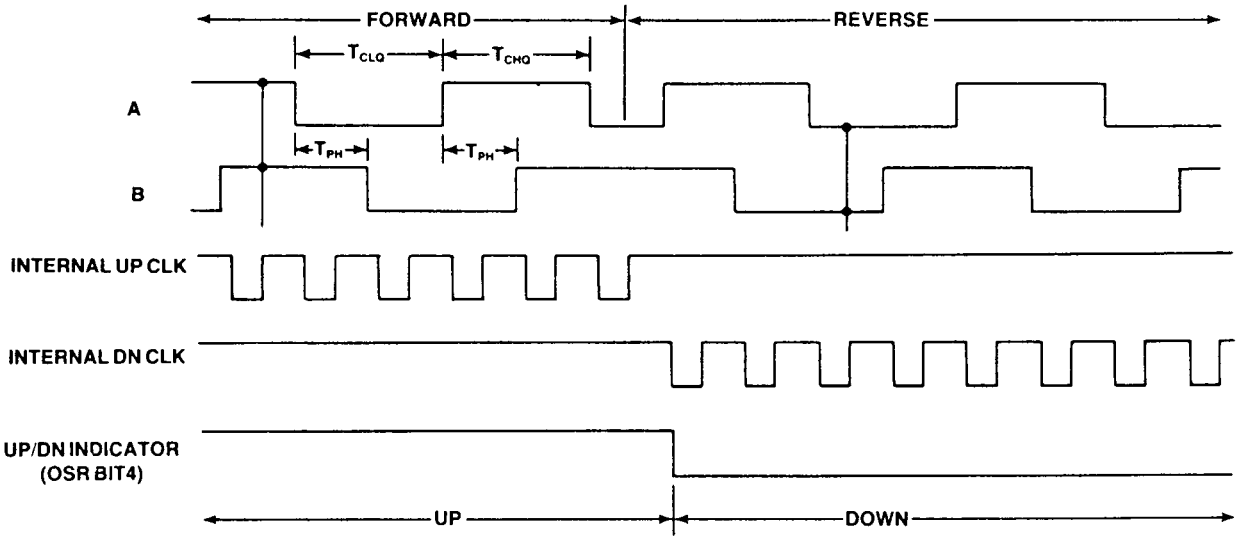


FIGURE 7 – QUADRATURE MODE

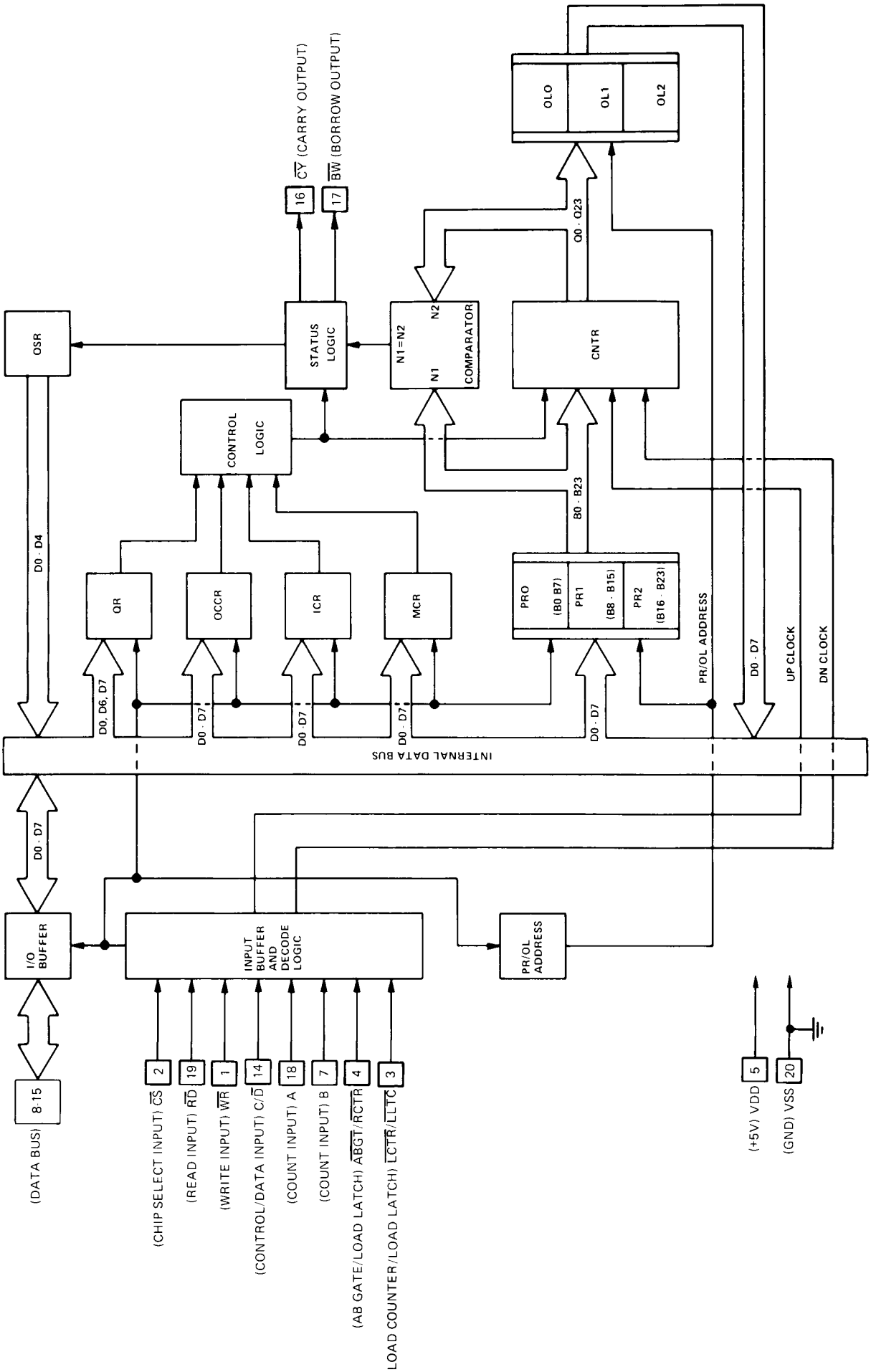


FIGURE 8 – LS7066 BLOCK DIAGRAM

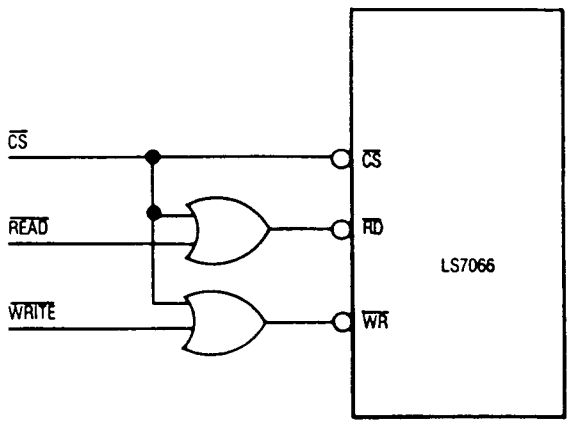


FIGURE 9