FEATURES

- 3.3V and 5V power supply options
- Typical 30ps output-to-output skew
- Max. 50ps output-to-output skew
- Synchronous enable/disable
- Multiplexed clock input
- 75KΩ internal input pull-down resistors
- Available in 20-pin SOIC package

DESCRIPTION

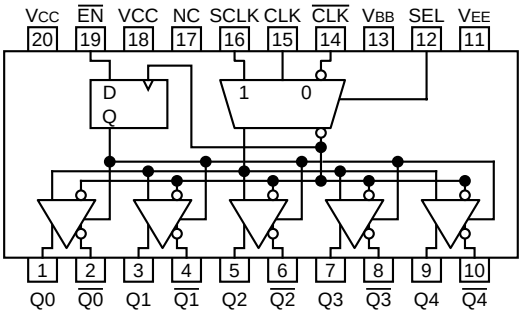
The SY100EL14V is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The EL14V is suitable for operation in systems operating from 3.3V to 5.0V supplies. If a single-ended input is to be used the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL14V under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

The EL14V features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pull-down resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

When both differential inputs are left open, CLK input will pull down to V_{EE} and $\overline{CLK}$ input will bias around $V_{CC}/2$.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
SCLK	Scan Clock Input
$\overline{EN}$	Synchronous Enable
SEL	Clock Select Input
V_{BB}	Reference Output
Q_{0-4}	Differential Clock Outputs

TRUTH TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK or SCLK

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	-8.0 to 0	VDC
V_I(3)	Input Voltage (V_{CC} = 0V)	0 to -6.0	VDC
I_{OUT}	Output Current - Continuous - Surge	 50 100	mA
T_A	Operating Temperature Range	-40 to +85	°C
V_{EE}	Operating Range(1),(2)	-5.7 to -3.0	V

NOTES:

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 100EL14V Series: -3.0V to -5.5V.
3. In PECL mode operation, V_I(Max) = V_{CC}.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min) to V_{EE} (Max); V_{CC} = GND(1)

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage(2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage(2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{OHA}	Output HIGH Voltage(2)	-1095	—	—	-1035	—	—	-1035	—	—	-1035	—	—	mV
V_{OLA}	Output LOW Voltage(2)	—	—	-1555	—	—	-1610	—	—	-1610	—	—	-1610	mV
V_{IH}	Input HIGH Voltage	-1165	—	-880	-1165	—	-880	-1165	—	-880	-1165	—	-880	mV
V_{IL}	Input LOW Voltage	-1810	—	-1475	-1810	—	-1475	-1810	—	-1475	-1810	—	-1475	mV
I_{IL}	Input LOW Current(3) $\overline{CLK}$	0.5 -300	— —	— —	0.5 -300	— —	— —	0.5 -300	— —	— —	0.5 -300	— —	— —	µA
I_{IH}	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{EE}	Power Supply Current	—	32	40	—	32	40	—	32	40	—	34	42	mA
V_{BB}	Output Reference Voltage	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	V

NOTES:

1. This table replaces the three traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = -4.5V now apply across the full V_{EE} range of -3.0V to -5.5V. Outputs are terminated through a 50Ω resistor to -2.0V except where otherwise specified on the individual data sheets.
2. V_{IN} = V_{IH}(Max) or V_{IL}(Min).
3. V_{IN} = V_{IL}(Max).

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min) to V_{EE} (Max); V_{CC} = GND

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	 520 470 470	 720 770 770	 550 500 500	 750 800 800	 580 530 530	 680 680 680	 780 830 830	 630 580 580	 830 880 880	ps
t_{skew}	Part-to-Part Skew[1] Within-Device Skew	— —	200 50	— —	200 50	— —	— —	200 50	— —	200 50	ps
t_S	Setup Time $\overline{EN}$	150	—	150	—	150	—	—	150	—	ps
t_H	Hold Time $\overline{EN}$	200	—	200	—	200	—	—	200	—	ps
V_{PP}	Minimum Input CLK Swing	150	—	150	—	150	—	—	150	—	mV
V_{CMR}	Common Mode Range[2] V_{PP} < 500mV V_{PP} ≥ 500mV	 -2.0 -1.8	 -0.4 -0.4	 -2.1 -1.9	 -0.4 -0.4	 -2.1 -1.9	 — —	 -0.4 -0.4	 -2.1 -1.9	 -0.4 -0.4	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230	500	230	500	230	360	500	230	500	ps

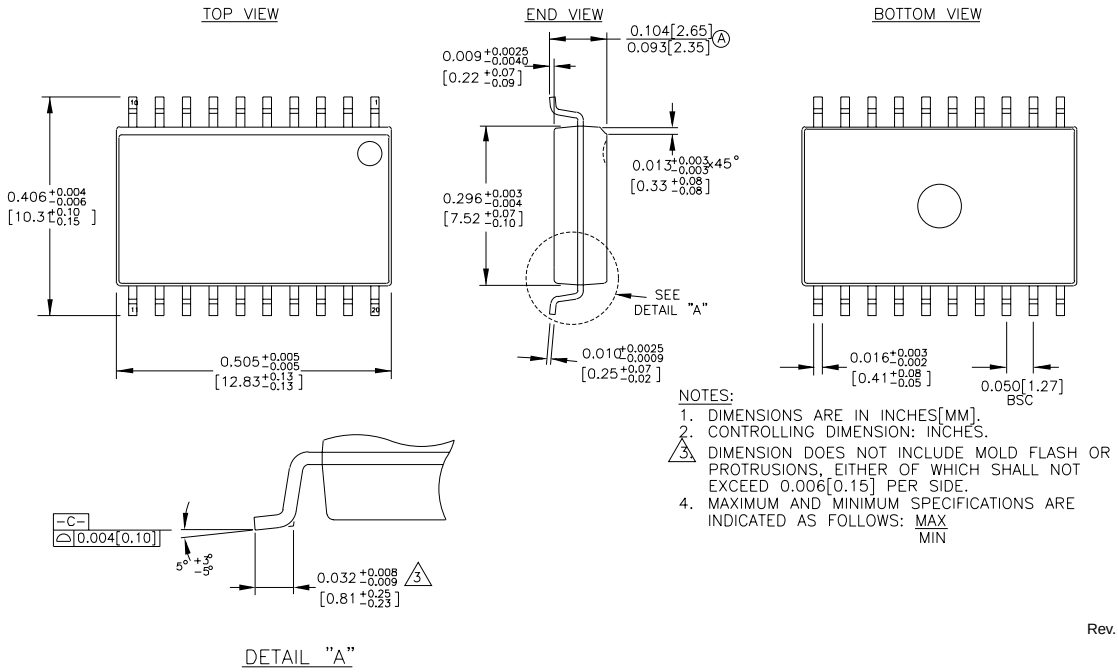
NOTES:

1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
2. The V_{CMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}(Min) and 1V. The lower end of the V_{CMR} range varies 1:1 with V_{EE}. The numbers in the specification table assume a nominal V_{EE} = -3.3V. For PECL operation, the V_{CMR}(Min) will be fixed at 3.3V – |V_{CMR}(Min)|.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100EL14VZC	Z20-1	Commercial
SY100EL14VZCTR	Z20-1	Commercial

20 LEAD SOIC .300" WIDE (Z20-1)



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