CONEXANT™

Endstation ServiceSAR Controller

RS8235

Endstation ATM xBR Service Segmentation and Reassembly Controller (ServiceSAR)

Conexant's RS8235 offers endstations all of the xBR service categories in a highly integrated 3.3V CMOS package. The RS8235 architecture complements the RS8234 edge SAR feature set, so that software reuse is maximized. The RS8235 directly connects to Conexant's RS8251 PHY device for a total NIC solution.

The RS8235 supports a similar feature set to the RS8234 edge SAR, but in a reduced footprint. System designers can therefore offer a common traffic control and host interface to a new market segment.

Integrated Management

The RS8235 complies with ATM Forum specifications UNI 3.1, T.M. 4.1 and all other relevent standards. The RS8235 provides integrated traffic management for all service categories, including constant bit rate (CBR), variable bit rate (VBR1, VBR2, and VBR3), real-time VBR, unspecified bit rate (UBR), available bit rate (ABR), guaranteed frame rate (GFR) (guaranteed MCR on UBR VCCs), and generic flow control (GFC). The xBR traffic management block automatically schedules each VCC according to user-assigned parameters to maximize line utilization.

Distinguishing Features

- Fully T.M. 4.1-compliant
- 3.3V/5V low power utilization (< 1 watt)
- 208-pin PQFP
- Commercial temperature
- 4K VCCs
- Software compatible with RS8234

Endstation ServiceSAR Controller

RS8235

Endstation Architecture

The RS8235's architecture is designed to minimize and control host traffic congestion. The host manages the RS8235 terminal using write-only control and status queues. The host submits data for transmit by writing buffer descriptor pointers to one of four transmit queues. These entries may be thought of as task lists for the Endstation SAR to perform. In addition, the RS8235 can perform ATM server functions for up to four clients. The device's architecture lessens the control burden on the host system while minimizing PCI bus utilization, by eliminating reads across the PCI bus from host control activities. It also provides control points to manage congestion, which is critical for ABR.

The RS8235 System

The RS8235 consists of five separate coprocessors (incoming and outgoing DMA, segmentation, reassembly and xBR traffic manager), each of which maintains state information in shared, off-chip memory. This memory is controlled by the SAR through the local bus interface, which arbitrates access to the bus between the various coprocessors. These coprocessors, though they run off the same system clock, operate asynchronously from each other. Communication between the coprocessors takes place through on-chip FIFOs or through queues in local memory.

The RS8235's on-chip coprocessor blocks are surrounded by high-performance PCI and UTOPIA ports for glueless interface to a variety of system components with full line-rate throughput and low bus occupancy. Figure 1 illustrates these functional blocks.

xBR Cell Scheduler

The cell scheduler rate-shapes all segmentation traffic according to per-channel parameters. The RS8235 supports eight user-assigned scheduling priorities in addition to CBR. The user assigns a priority to each channel and sets the range of available transmission rates for the scheduler by setting the size of the dynamic schedule table and the duration of each scheduling slot in the table. The user can further control consumption of bandwidth by assigning peak cell-rate limits to four of those scheduling priorities.

ABR Traffic Management

The ABR flow control manager dynamically rate-shapes ABR traffic independently per VCC, based upon network feedback. One or more ABR templates are used to govern the behavior of traffic. Both relative rate (RR) and explicit rate (ER) algorithms are employed when computing a rate adjustment on an ABR VCC. Programmable ABR templates allow rate-shaping policies on groups of VCCs to be tuned for different network applications. The RS8235 automatically generates and processes all resource management (RM) cells. The on-chip hardware, coupled with the user-defined ABR templates, implements all required source and destination behaviors as defined in TM4.0. Optional behaviors such as use-it-or-lose-it, out-of-rate RM cells, host congestion and allowed cell rate (ACR) monitoring are also supported.

IP Interworking

The VBR-3, CLP0+1 category includes rate-shaping via the dual leaky bucket GCRA algorithm based on the CLP bit, which is recommended by the IETF for use with IP.

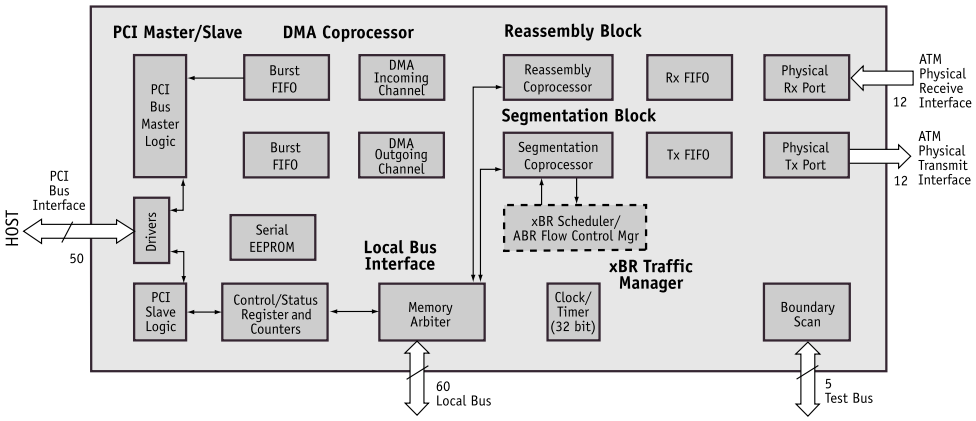


Figure 1. RS8235 functional block diagram

Virtual Path Networking

The RS8235 can interleave segmentation of numerous VCCs (i.e., separate VC channels) as members of one VP. VP-based traffic shaping is supported. The entire VP is scheduled according to one set of traffic parameters.

CBR Tunneling

The user can designate up to four CBR pipes (or tunnels) in which to transmit multiple CBR channels. This allows proprietary traffic management schemes to operate under a pre-allocated CBR bandwidth.

RS8235/8251EVM ATM Evaluation Module

The RS8235 ATM Evaluation Module (EVM) provides complete evaluation capability for the RS8235 segmentation and reassembly controller. The EVM serves as a hardware and software reference design for development of customer-specific ATM applications. The RS8235/8251EVM was designed to provide a rapid prototyping environment to assist and speed customer development of new ATM products, thereby reducing product time to market.

Figure 2 shows a block diagram of the hardware for the RS8235/8251EVM. The software is described on the following page.

The RS8235/8251EVM PCI card is specifically designed to be a full-featured ATM controller based on Conexant's RS8251 ATM receiver/transmitter and the RS8235 Endstation SAR. The PHY interface comes configured with an optical OC-3 connection for testing at 155 Mbps.

The PCI interface between the host processor and the local system is controlled by the RS8235 Hardware Programming Interface (RS8235HPI), a software driver for the RS8235, on top of which a system designer can develop and place proprietary driver software. This interface allows users to easily port their applications to the RS8235/8251EVM. This software is written in C, and source code is available under a no-cost license agreement.

The RS8235/8251EVM also includes documentation, a full set of design schematics and artwork for the RS8235/8251EVM PCI card.

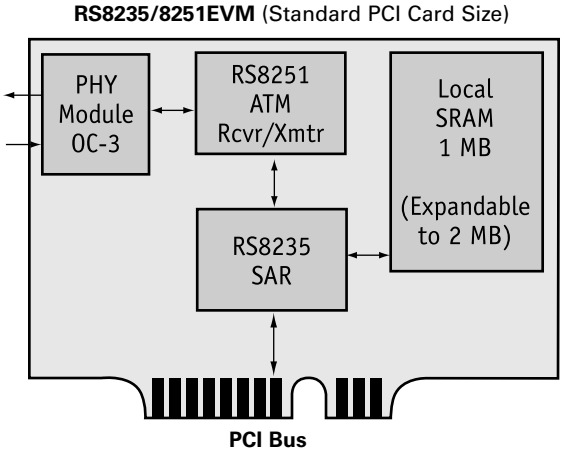
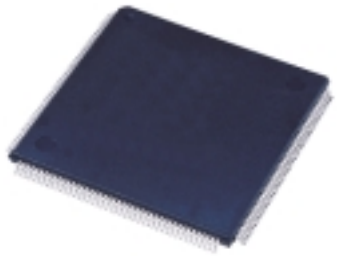


Figure 2. RS8235/8251EVM hardware block diagram



RS8235/8251EVM Features	Benefits
Hardware interface fully compliant with PCI	Provides an easy, high-performance hardware interface to other off-the-shelf PCI products, such as Ethernet cards or multimedia accelerators.
Hardware reference design	Full-featured RS8235/8251EVM reference design provided as a complete ATM UNI which implements the full functionality of the RS8235 Endstation SAR.
Software reference design	Greatly speeds development of new applications. Allows the user to develop and port proprietary software applications atop the software driver provided with the RS8235/8251EVM.
Traffic generation and checking capability	Assists in product debug state as an ATM load generator and checker.
Optical OC-3 interface	Enables high-performance testing.

RS8235HPI Features	Benefits
Software reference design	Shortens development time of customer system-specific ATM applications.
Modular software design	Allows users to utilize only those functions they want and to incorporate those functions into their own applications.
Dynamic rate control per virtual channel	Users can establish ABR, CBR, UBR or VBR connections at VCC setup on each of over 32,000 channels.
SAR initialization and VCC control	Provides detailed examples for control and management of the RS8235. Significantly shortens design time.
Well-defined, robust RS8235HPI interface	Enables users to easily port their application to the RS8235/8251EVM.
Well-documented C source code	Gives users a clear description of how the software and hardware function.
RS8235HPI Macro Layer software	Offers a layer of abstraction for ease-of-use of the RS8235HPI primitives. Reference device driver for VxWorks.

What is ATM?

Asynchronous Transfer Mode (ATM) has emerged as the primary networking technology for next-generation, multi-service communication networks. ATM-enabled services benefit the Internet as well as emerging applications in science, telemedicine and distance learning. Just as the Internet revolutionized worldwide communications, ATM brings new meaning to high-speed networking.

ATM, which uses a fixed-size packet, or cell, is a transport protocol capable of providing a homogeneous network for all traffic types, whether the application is to carry conventional telephony, video entertainment, or data traffic over LANs, MANs or WANs.

The ITU-T and ANSI selected ATM for Broadband-ISDN. SONET/SDH, as specified by the ITU, is intended as the primary transport mechanism for ATM cells in WAN applications. ATM also plays a key role in next-generation consumer applications for high-speed Internet access and wireless access. The ADSL Forum and the Universal ADSL Working Group chose ATM as the network layer protocol for G.lite and G.DMT ADSL.

ATM physical-layer (ATM-PHY) IC devices adapt ATM cells to and from transmission rates ranging from 1.544 Mbps to 2.4 Gbps via a standard system interface called UTOPIA. ATM-PHY devices perform ATM cell functions (transmission convergence) such as cell scrambling/descrambling, cell delineation (HEC), cell header processing, and cell-rate decoupling as well as rate-specific functions for frame generation/recovery frame adaptation and clock/data recovery.

RS8235HPI Hardware Programming Interface

The RS8235 Hardware Programming Interface (HPI) provides a set of fully-defined software primitives to interface with an ATM UNI port based on the RS8235 SAR. It serves as an interface point for system software designed to configure and manage the RS8235-based UNI without the need for detailed manipulation of hardware-related structures. It thus provides a layer of abstraction from the hardware for the system designer and user.

RS8235HPI primitives are used by higher-level application software (such as network management and device drivers) to obtain ATM services as required by their upper protocol layers. These primitives handle SAR resource, control and status management. The RS8235HPI performs functions in the following categories:

- RS8235 SAR device initialization
- Memory resource allocation
- Resource management
- Connection management (including VCC setup and teardown, and processing status)
- Segmentation/data transmission
- Data reception/reassembly
- Statistics gathering/error reporting
- Diagnostic testing

The RS8235HPI provides a reference implementation of these critical functions in order to shorten the development of a production-quality, customer system specific ATM application.

The RS8235HPI is implemented in well-documented C source code, specifically written to be highly portable across a multiplicity of processors, compilers and development environments.

RS8235 Endstation SAR

Special Features:

xBR Traffic Management

- **TM 4.0 Service Classes**
  - CBR
  - VBR (single, dual and CLP 0+1 leaky buckets)
  - Real-time VBR
  - ABR
  - UBR
  - GFC (controlled and uncontrolled flows)
  - Guaranteed frame rate (GFR) (guaranteed MCR on UBR VCCs)
- **8 Levels of priorities (8 + CBR)**
- **Dynamic per-VCC scheduling**
- **Multiple programmable ABR templates (supplied by Conexant or user)**
- **Scheduler driven by local clock for low-jitter CBR**
- **Internal RM OAM cell feedback path**
- **Virtual FIFO rate matching**
- **Per-VCC MCR and ICR**
- **Tunneling**
  - VP tunnels (VCI interleaving on PDU boundaries)
  - CBR tunnels (cells interleaved on UBR with an aggregate CBR limit)

Multi-Queue Segmentation Processing

- **4 Transmit queues with optional priority levels**
- **4K VCCs maximum ****
- **AAL5 CPCS generation**
- **AAL0 Null CPCS (optional use of PTI for PDU demarcation)**
- **ATM cell header generation**
- **Raw cell mode (52 octet)**
- **200 Mbps half duplex**
- **155 Mbps full duplex (with 2-cell PDUs)**
- **Message and streaming status modes**
- **Variable-length transmit FIFO-CDV-host latency matching (1 to 9 cells)**
- **Symmetric Tx and Rx architecture**
  - Buffer descriptors
  - Queues
- **User-defined field circulates back to host (32 bits)**
- **Distributed host or SAR-shared memory segmentation**
- **Simultaneous segmentation and reassembly**
- **Per-PDU control of CLP/PTI (UBR)**
- **Per-PDU control of AAL5 UU field**
- **Virtual Tx FIFO (PCI host)**

Multi-Queue Reassembly Processing

- **4 reassembly queues**
- **4K VCCs maximum ****
- **AAL5 CPCS checking**
- **AAL0**
  - PTI termination
  - Cell count termination
- **Early packet discard, based on:**
  - Receive buffer underflow
  - Receive status overflow
  - CLP with priority threshold
  - AAL5 max PDU length
  - Rx FIFO full
  - Frame Relay DE with priority threshold
  - LECID filtering for echo suppression
  - Per-VCC firewalls
- **Dynamic channel lookup (NNI or UNI addressing)**
  - Supports full address space
  - Deterministic
  - Flexible VCI count per VPI
  - Optimized for signaling address assignment
- **Message and streaming status modes**
- **Raw cell mode (52 octet)**
- **200 Mbps half duplex**
- **155 Mbps full duplex (with 2-cell PDUs)**
- **Distributed host or SAR-shared memory reassembly**
- **8 programmable reassembly hardware time-outs (assignable per VCC)**
- **Global max PDU length for AAL5**
- **Per-VCC buffer firewall (memory usage limit)**
- **Simultaneous reassembly and segmentation**
- **Idle cell filtering**

High-Performance Host Architecture with Buffer Isolation

- **Write-only control and status**
- **Read multiple command for data transfer**
- **Up to 4 host clients control and status queues**
- **Physical or logical clients**
  - Enables peer-to-peer architecture
- **Descriptor-based buffer chaining**
- **Scatter/gather DMA**
- **Endian neutral**
- **Non-word (byte) aligned host buffer addresses**
- **Automatically detects presence of Tx data or Rx free buffers**
- **Virtual FIFOs (PCI bursts treated as single address)**
- **Hardware indication of BOM**
- **Allows isolation of system resources**
- **Status queue interrupt delay**

Designer Toolkit

- **Evaluation module (RS8235/8251EVM)**
- **Reference schematics**
- **Hardware Programming Interface – RS8235HPI reference source code (C)**

Standards-Based I/O

- **33 MHz PCI 2.1**
- **Serial EEPROM to store PCI configuration information**
- **PHY interfaces**
  - UTOPIA master (Level 1)
  - UTOPIA slave (Level 1)
- **Flexible local memory architecture**
- **Optional local control interface**
- **Boundary scan for board-level testing**
- **Source loopback, for diagnostics**
- **Glueless connection to Conexant's RS8250 ATM PHY device**

Electrical/Mechanical

- **208-pin QFP package**
- **3.3V power supply**
- **5V tolerant I/O pads**
- **5V – 3.3V PCI pads**
- **Low power (<1W) at full rate**
- **Industrial temperature range**
- **TTL level inputs**
- **CMOS level outputs**

Standards Compliance

- **UNI/NNI 3.1**
- **T.M. 4.1**
- **Bellcore GR-1248**
- **ATM Forum B-ICI V 2.0**
- **I.363**
- **I.610 /GR-1248**
- **AToM MIB (RFC1695)**
- **ILMI MIB**
- **ANSI T1.635**
- **GFC per I.361**
- **SNMP**
- **I^2C Protocol**
- **PCI Revision 2.1**
- **IEEE 1149.1-1990**
- **IEEE 1149.1 supplement B, 1994**

Statistics and Counters

- **Global register counter of # of cells transmitted**
- **Global register counter of # of cells received on active channels**
- **Global register counter of # of cells received on inactive channels**
- **Global register counter of # of AAL5 CPCS-PDUs discarded due to per-channel firewall, etc.**
- **RSM per VCC service discard counters (Frame Relay and LANE)**
- **1 programmable interval timer (32 bits with interrupt)**

** Depends on local memory size and device configuration; 4K VCCs typically.

Product Features

- **AAL0, AAL5**
- **Factory supplied ABR templates (user may configure)**
- **xBR Traffic Manager**
  - CBR
  - VBR (single bucket)
  - VBR (dual bucket)
  - VBR (CLP 0+1)
  - rt-VBR
  - ABR (TM4.0)
  - UBR
  - GFC
  - GFR
- **PCI 2.1**
- **UTOPIA Level 1**
- **Glueless interface to Conexant's RS8251 PHY device**
- **Reference design available**
- **RS8235 evaluation module available**
- **Reference software available (RS8235HPI)**

Applications

- **ATM NICs**
- **ATM Uplinks**
  - Ethernet switches
- **ATM Servers**
  - File servers

Ordering Information

Part Number	Description
RS8235KHFD	ATM Endstation SAR
RS8235/8251EVM	RS8235 and RS8251 PCI Evaluation Module

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