

SYNCHRONOUS DRAM

MT48LC32M8A2 – 8 MEG x 8 x 4 BANKS
MT48LC16M16A2 – 4 MEG x 16 x 4 BANKS

For the latest data sheet, please refer to the Micron Web site: www.micron.com/dramds

Features

- Supports PC100 and PC133 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE, and auto refresh modes
- Self refresh mode; standard and low power
- LVTTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- 64ms, 8,192-cycle refresh

OPTION

- | | MARKING |
|--|----------------|
| • Configuration | |
| 16 Meg x 16 (4 Meg x 16 x 4 banks) | 16M16 |
| 32 Meg x 8 (8 Meg x 8 x 4 banks) | 32M8 |
| WRITE Recovery (^t WR) | A2 |
| ^t WR = "2 CLK" ¹ | |
| • Package | |
| Plastic Package – OCPL ² | |
| 54-pin TSOP II (400 mil) | TG |
| 54-pin TSOP II (400 mil) Lead-free | P |
| • Timing (Cycle Time) | |
| 6.0ns @ CL = 3 | -6A |
| • Self Refresh | |
| Standard | None |
| • Operating Temperature Range | |
| Commercial (0°C to +70°C) | None |

NOTE:

1. Refer to Micron Technical Note: TN-48-05.
2. Off-center parting line.

Part Number:

MT48LC16M16A2TG-6A

Addendum Changes

The standard 256Mb SDRAM data sheets also pertain to the x8 and x16 device and should be referenced for a complete description of SDRAM functionality and operating modes. However, to meet the faster speed grades, some of the AC timing parameters are slightly different. This addendum data sheet will concentrate on the key differences required to support the enhanced speeds.

The Micron 256Mb data sheet provides full specifications and functionality unless specified herein.

Table 1: Address Table

	16 MEG x 16	32 MEG x 8
Configuration	4 Meg x 16 x 4 banks	8 Meg x 8 x 4 banks
Refresh Count	8K	8K
Row Addressing	8K (A0–A12)	8K (A0–A12)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	512 (A0–A8)	1K (A0–A9)

Table 2: Key Timing Parameters

CL = CAS (READ) latency

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME CL = 3	SETUP TIME	HOLD TIME
-6A	167 MHz	5.4ns	1.5ns	0.8ns

Table 3: I_{DD} SPECIFICATIONS AND CONDITIONS

 Notes: 1, 5, 6, 11, 13; notes appear in the standard data sheet; V_{DD}/V_{DDQ} = +3.3V ±0.3V

PARAMETER/CONDITION		SYMBOL	-6A	UNITS	NOTES
Operating Current: active mode; burst = 2; READ or WRITE; t _{RC} = t _{RC} (MIN)		I _{DD1}	135	mA	3, 18, 19, 32
Standby Current: power-down mode; all banks idle; CKE = LOW		I _{DD2}	2	mA	32
Standby Current: active mode; CKE = HIGH; CS# = HIGH; all banks active after t _{RCD} met; no accesses in progress		I _{DD3}	40	mA	3, 12, 19, 32
Operating Current: burst mode; continuous burst; READ or WRITE; all banks active		I _{DD4}	135	mA	3, 18, 19, 32
Auto Refresh Current CKE = HIGH; CS# = HIGH	t _{RFC} = t _{RFC} (MIN)	I _{DD5}	285	mA	3, 12, 18, 19, 32, 33
	t _{RFC} = 8.125μs	I _{DD6}	3.5	mA	
Self Refresh Current: CKE ≤ 0.2V	Standard	I _{DD7}	2.5	mA	4

Table 4: Electrical Characteristics and Recommended AC Operating Conditions

Notes 5, 6, 8, 9, 11; Notes appear in the standard data sheet

AC CHARACTERISTICS		SYMBOL	-6A		UNITS	STD DATA SHEET NOTES
PARAMETER			MIN	MAX		
Access time from CLK (pos. edge)	CL = 3	$t_{AC} (3)$		5.4	ns	27
Address hold time		t_{AH}	0.8		ns	
Address setup time		t_{AS}	1.5		ns	
CLK high-level width		t_{CH}	2.5		ns	
CLK low-level width		t_{CL}	2.5		ns	
Clock cycle time	CL = 3	$t_{CK} (3)$	6		ns	23
CKE hold time		t_{CKH}	0.8		ns	
CKE setup time		t_{CKS}	1.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		t_{CMH}	0.8		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		t_{CMS}	1.5		ns	
Data-in hold time		t_{DH}	0.8		ns	
Data-in setup time		t_{DS}	1.5		ns	
Data-out high-impedance time	CL = 3	$t_{HZ} (3)$		5.4	ns	10
Data-out low-impedance time		t_{LZ}	1		ns	
Data-out hold time (load)		t_{OH}	3		ns	
Data-out hold time (no load)		t_{OH_N}	1.8		ns	28
ACTIVE to PRECHARGE command		t_{RAS}	42	120,000	ns	
ACTIVE to ACTIVE command period		t_{RC}	60		ns	
ACTIVE to READ or WRITE delay		t_{RCD}	18		ns	
Refresh period (8,192 rows)		t_{REF}		64	ms	
AUTO REFRESH period		t_{RFC}	60		ns	
PRECHARGE command period		t_{RP}	18		ns	
ACTIVE bank a to ACTIVE bank b command		t_{RRD}	12		ns	7
Transition time		t_T	0.3	1.2	ns	
WRITE recovery time ¹		t_{WR}	1 CLK + 6ns		ns	
			12		ns	25
Exit SELF REFRESH to ACTIVE command		t_{XSR}	67		ns	20

NOTE:

- Auto precharge mode only. The precharge timing budget (t_{RP}) begins 6ns for -6A after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.

Table 5: AC Functional Characteristics

Notes appear in the standard data sheet.

PARAMETER	SYMBOL	-6A SPEED	UNITS	STD DATA SHEET NOTES
READ/WRITE command to READ/WRITE command	t_{CCD}	1	t_{CK}	17
CKE to clock disable or power-down entry mode	t_{CKED}	1	t_{CK}	14
CKE to clock enable or power-down exit setup mode	t_{PED}	1	t_{CK}	14
DQM to input data delay	t_{DQD}	0	t_{CK}	17
DQM to data mask during WRITES	t_{DQM}	0	t_{CK}	17
DQM to data high-impedance during READs	t_{DQZ}	2	t_{CK}	17
WRITE command to input data delay	t_{DWD}	0	t_{CK}	17
Data-in to ACTIVE command	t_{DAL}	5	t_{CK}	15, 21 ¹
Data-in to PRECHARGE command	t_{DPL}	2	t_{CK}	16, 21
Last data-in to burst STOP command	t_{BDL}	1	t_{CK}	17
Last data-in to new READ/WRITE command	t_{CDL}	1	t_{CK}	17
Last data-in to PRECHARGE command	t_{RDL}	2	t_{CK}	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command	t_{MRD}	2	t_{CK}	26
Data-out to high-impedance from PRECHARGE command (CL = 3)	t_{ROH} (3)	3	t_{CK}	17

NOTE:

1. The Note 21 in the standard data sheet does not apply for this speed grade and should read "Based on $t_{CK} = 6ns$ "

Data Sheet Designation:

Production: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.



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