VSC7302
Data Sheet

Heathrow-III™ – 16-Port Gigabit Ethernet Switch-on-a-Chip

FEATURES

- 16 Gigabit Ethernet ports with nonblocking wire-speed performance
- Tri-speed (10/100/1000 Mb/s) operation via RGMII or RTBI interface
- Support for both wire-speed automatic learning, and CPU-based learning
- 272 kB on-chip frame buffer
- Jumbo frame support
- Programmable classifier for QoS (Layer 4/ Multimedia)
- 8 k MAC addresses and 4 k VLAN support (IEEE802.1Q)
- Per-port shaping, policing, and Broadcast Storm Control
- IEEE802.1Q-in-Q nested VLAN support
- Full duplex flow control (IEEE802.3x) and half duplex back pressure
- Flexible link aggregation compliant with IEEE802.3ad
- Spanning Tree Protocol support (IEEE802.1D)
- Multiple Spanning Tree support (IEEE802.1s)
- Port-based Access Control (IEEE802.1X)
- IGMP, GARP, GMRP, and GVRP support
- Cost effective 4 pin serial CPU interface
- Performance optimized 8/16 bit interface for SNMP and Web-based management

GENERAL DESCRIPTION

Heathrow-III is a full-featured, 16-port, Gigabit Ethernet switch-on-a-chip with several integrated management interfaces and support for both copper and optical PHYs.

Heathrow-III provides nonblocking, wire-speed gigabit performance on all ports. It enables managed operation through a generic 8- or 16-bit CPU interface, supporting several important routing protocols, thus making Web-based and SNMP management possible.

In addition, less processor intensive managed operation is obtainable using a simple 4-wire serial interface.

Heathrow-III has been optimized for desktop and workgroup market segments, and does not require additional external memory.

Each port is equipped with a Policer for ingress traffic control and a Shaper for egress traffic rate management.

The chip also supports programmable higher layer classification and prioritization to enable enhanced Quality of Service (QoS) support for real time applications such as VoIP.

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FUNCTIONAL OVERVIEW

Heathrow-III can operate as either a VLAN aware switch or a VLAN unaware switch. It forwards frames at Layer 2 based on information up to and including Layer 4.

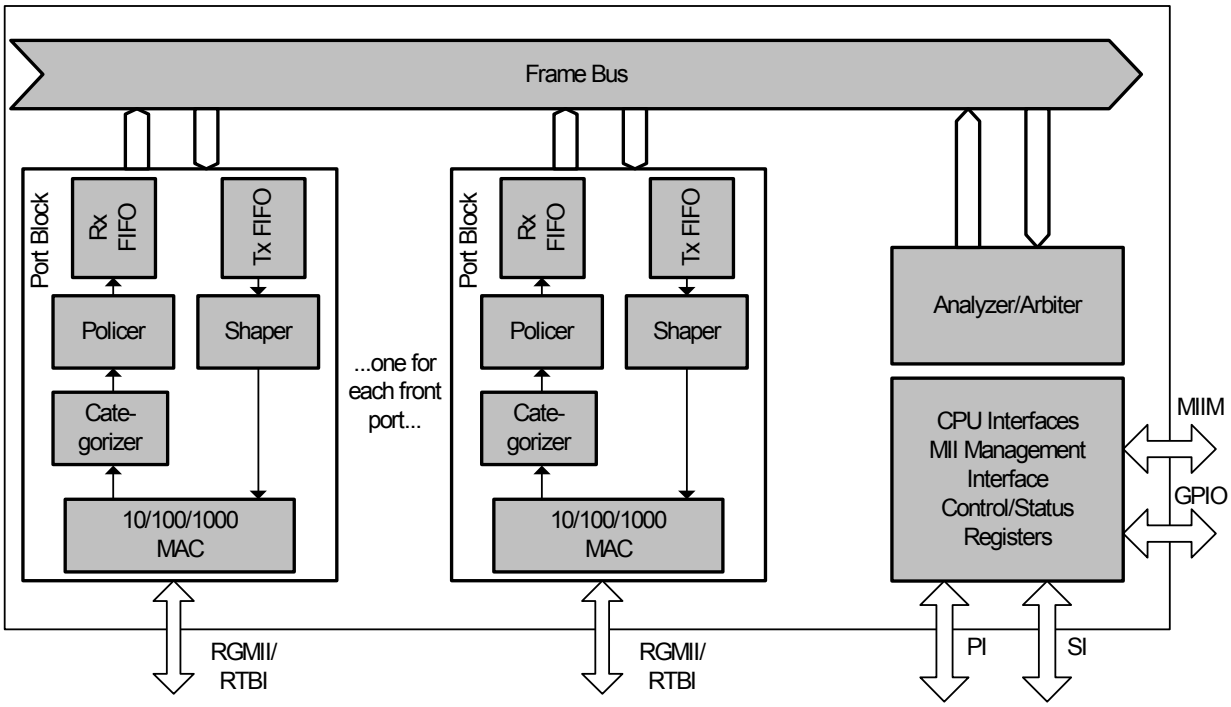


Figure 1. Block Diagram

Tri-Speed Gigabit MACs

Heathrow-III implements 16 separate tri-speed Ethernet MACs designed to comply with IEEE Std 802.3-2002. The tri-speed MACs provide support for full duplex operation at 10/100/1000 Mb/s and half duplex operation at 10/100 Mb/s.

Gigabit Ethernet PCS

In each MAC, Heathrow-III implements the Physical Coding Sublayer (PCS) functionality required to conform to RTBI/SERDES. It is also designed to comply with IEEE Std 802.3-2002 (clauses 36 and 37). In addition, it provides the CPU register interface for implementing the Auto Negotiation Process.

Register Access

The control block receives commands via the CPU interfaces from an off-chip controller/processor and interprets these commands. The commands can be divided into four categories:

- MII Management reads and writes for PHY control
- Configuration
- Status or statistics gathering
- Capture and transmission of packets

Link Aggregation

Heathrow-III supports ingress and egress port aggregation. Up to 8 ports can be aggregated, with a frame distribution function based on the Source MAC address, the Destination MAC address, or a combination of both.

VLAN Support

Heathrow-III can be configured as either VLAN unaware (behaving transparently against VLAN tagged frames) or as VLAN aware.

When VLAN is enabled, frames that are received without a VLAN tag on a given port get tagged with a port specific, configurable VLAN number. Frames that already have a VLAN tag when they are received have no additional tag added.

VLAN awareness (and thus tagging/untagging of frames) can be configured on a per-port basis, which is a very powerful feature for advanced applications.

Heathrow-III can set up and maintain 4096 VLANs.

Furthermore, each port can be configured to a set of ports it can forward to, thereby facilitating port-based VLANs. Per default, all ports can forward to all others.

802.1Q-in-Q Support

Q-in-Q is an efficient method for enabling Subscriber Aggregation. This is very useful in, but is not limited to, the MAN. Q-in-Q is, in effect, the use of double VLAN tags.

In Heathrow-III, Q-in-Q is supported in three ways:

1. Each port can add or strip a VLAN tag (independently configurable for ingress and egress per port)
2. Frame priority can be determined based on information in the second VLAN tag
3. The frame can be forwarded based on information in the second VLAN tag

If several Heathrow-IIIs are used to aggregate a number of subscribers towards the edge of the network, the Q-in-Q support can be used to store prioritization information and the source port number of each frame for use by subsequent Heathrow-IIIs. In this way, prioritization need only be done once, and the network edge router easily stores the route back to the subscriber from where the frame originated.

The effective maximum frames size will be 1526 bytes throughout the Q-in-Q network, as the standard end-station MTU of 1518 bytes gets append two VLAN tags.

Quality Of Service

Heathrow-III has two priority queues on each port, and the enhanced classifier/categorizer can assign priorities based on information taken from Layer 2 to Layer 4.

The Categorizer analyzes all received frames. It can determine the priority of each frame based on:

1. Priority in the IEEE802.1Q (VLAN) tag
2. Differentiated Services Code Point from the IP-header
3. TCP/UDP port
4. DSAP Value
5. EtherType field
6. Priority in a Q-in-Q tag

Based on the priority determined by the Categorizer, high and low priority traffic are kept separate to ensure that high priority traffic will never be blocked by low priority traffic.

Flow Control

All ports can be independently configured to use nondropping flow control, also enabling the use of Asymmetric Flow Control. The programmer can set up individual high and low thresholds for each FIFO. These thresholds control the start and stop of pause signaling. The internal FIFOs have enough memory to handle flow control on short-haul full duplex lines without using excessive pause signaling.

The switch generates flow control when necessary to ensure frames are never dropped, or it can be programmed to discard low priority traffic first in case of congestion.

Packet Forwarding

The advanced filtering and forwarding capabilities of Heathrow-III are a result of the work carried out by the Analyzer.

The Analyzer maintains and uses three tables for packet forwarding: A source port table, a VLAN table, and a destination address table.

When frame header information has been extracted from an incoming packet, the Analyzer uses these tables to look up the following information:

- A 16-bit Source Port Mask (one bit per port)
- A 16-bit VLAN Mask
- A 16-bit Destination Port Mask (if the DMAC address is known, otherwise a programmable mask)

These three masks are then combined by a bit-by-bit AND operation, and finally the results are adjusted to reflect any active link aggregations. The resulting bit mask is forwarded to the Arbiter as the next forwarding decision for the given source port.

By default, the three masks are set up such that:

- Packets received on a given port cannot be forwarded to that same port
- There is no VLAN present (all ports are members of all VLANs, frame tags are not examined)
- Packets to a given destination address are forwarded only to the port where the destination was learned

MAC Address Learning

When a packet is received, the source MAC address is looked up in the destination address table (see the ”Packet Forwarding” on page 16). If it is not presently registered and it is not a multicast address, a new entry is created. If necessary, an entry is discarded to make room for the new one based on a “least recently used” algorithm.

Because Heathrow-III is capable of looking up or adding all incoming entries to the MAC table at maximum load, the process is referred to as “wire-speed learning”.

In addition, addresses can be locked using an off-chip controller or CPU by writing into the table. Locked entries are never discarded.

Shaping and Policing

Heathrow-III provides per-port policing as well as per-port shaping. Policing can be used to limit incoming subscriber streams according to a traffic contract, while shaping can be used to protect a receiving device against high bandwidth bursts.

Based on a leaky bucket algorithm, Shaper as well as Policer support a bit rate granularity of 244 kb/s for 1G, 48.8 kb/s for 100M, and 4.88 kb/s for 10M. Spanning Tree and IGMP control frames are to be forwarded to the CPU capture facility only and will not be policed from the stream.

The ingress Policer is able to initiate the generation of flow control messages, enabling dropless policing.

An additional leaky-bucket system handles Heathrow-III’s Broadcast and Multicast Storm Control.

CPU Interfaces

Heathrow-III has two different CPU interfaces: a serial, SPI-style, 4-pin serial CPU interface and a generic, 16-bit, 37-wire parallel interface (PI). The SI allows interfacing to a vast amount of micro controllers, including the popular 8051 controller. The PI provides interfacing to many well-known processors, like the PowerPC and ARM CPUs.

The interfaces enable monitoring and configuration of the switch. They also give access to the capture and transmission of packets for STP and the GxRP protocols (GARP, GVRP, and so forth), as well as direct access to the output queues.

The SI is capable of transferring approximately 2.5 MB/s, whereas the PI can handle about 25 MB/s.

The PI interface can be configured to run in 8-bit mode, allowing it to work with an 8-bit CPU system.

MII Management Interface

Set up and status monitoring of connected PHYs is done through the two built-in MII Management controllers. Each of the two identical controllers is capable of connecting to up to 32 PHYs. Two interfaces rather than one primarily has electrical advantages (less load on the bus) and enables the use of more than one PHY per port (for example: 10/100 PHY and a 1000 PHY).

The controllers are suitable for direct connection to standard RGMII/RTBI PHYs and are accessed via the CPU interfaces.

General Purpose I/Os

Heathrow-III features four general purpose I/Os (GPIO). These pins are freely configurable as either inputs or outputs and are accessed via either CPU interface.

FUNCTIONAL DESCRIPTION

In this section, the different aspects of the Heathrow-III chip are explained. In many instances, references to the register set are made.

NOTE: *This section deals with overall Heathrow-III functionality. However, many smaller features and settings are available, which are not mentioned here. To learn about these, carefully read through the Configuration section, including the Register Description.*

Introduction – A Packet's Life In Heathrow-III

In the following topics, several blocks of Heathrow-III, as shown in Figure 1, are explained through the investigation of a packet's life in the chip. To better understand how the blocks interact, refer to Figure 2.

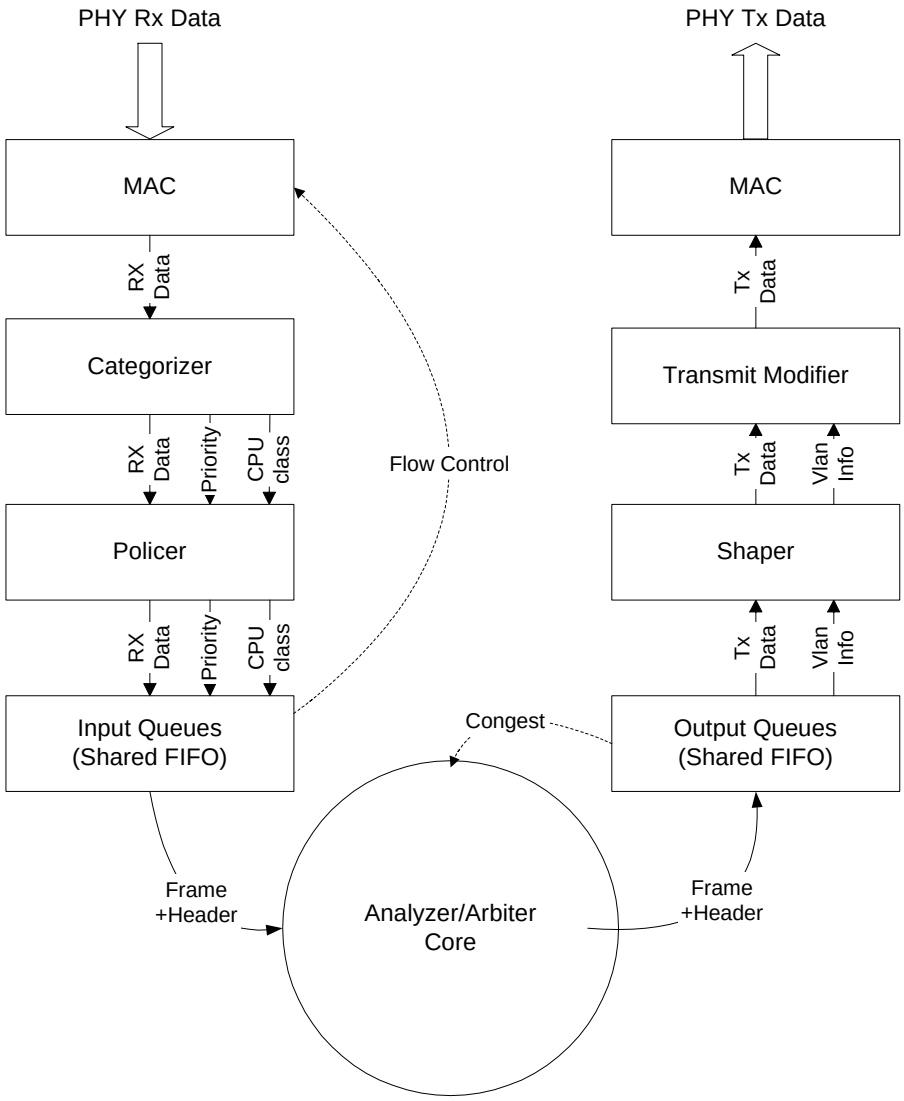


Figure 2. The Life of a Packet

The PHY Rx Data is received by the MAC, which sends the realigned data further through the Categorizer and the Policer to the port's Input Queues. After frame analysis and bus arbitration by the core, the frame is transferred to the determined set of Tx ports. It is cleared from the Input Queue when the last Tx port has stored it in its FIFO. The Tx port now sends the packet through the Shaper (which could drop the incoming frame if the bandwidth is violated), then the Modifier (which may insert a VLAN tag in the data stream and/or modify the CRC field in the frame). Finally, the frame enters the MAC, which handles the actual transmission. After transmission, the frame is cleared from the output queue.

MAC Features

Each of the 16 ports of Heathrow-III are equipped with a MAC, which can operate in various modes. The modes are mainly set up in the MACCONF register, where selections of speed, duplex mode, and so forth are made. When changing mode, the port must be reset. This is done by writing the configuration word twice: First with the reset bits set, and then with the reset bits cleared.

The more advanced features of the MAC are configured in the ADVPORTM register, where the transmit clock can be inverted, halted, and so forth. It is also here that the RTBI mode is enabled for fiber PHYs. Finally, in the MACHDXGAP register, important half duplex settings such as the Frame Gap values are configured.

The MAC supports frame lengths of up to 12.2 kB. The maximum length accepted by the MAC is configurable in the MAXLEN register.

VLAN Features

The VLAN influence on frame analysis is described in the ”Frame Analysis” on page 27. However, because the way each port handles tagged and untagged frames is controlled separately in each Port Controller, this is described here.

For ingress (Rx) frames, the processing of tagged and untagged frames can be configured in these aspects:

- For determining the priority of ingress frames:
  - If TAG prioritization is in use, the priority field within a tagged frame will be used for internal prioritization.
  - If TAG prioritization is in use, all untagged frames will get a configurable internal priority.
  - If TAG prioritization is *not* in use, the internal prioritization will be based on the contents following the tag.
- For determining the VLAN membership:
  - The tag can be ignored, and the VLAN membership will be based solely on the priority determined based on the payload. This is used when using Heathrow-III as a VLAN unaware switch.
  - The tag can be used for VLAN membership allocation. Priority tagged frames (VID = 0) in this respect will not be handled as VLAN tagged, and thus will be treated as an untagged frame.
  - Untagged frames will be allocated to a VLAN determined by the internal prioritization.

Egress (Tx) frame handling can be configured as follows:

- Do not tag frames. This is used when using Heathrow-III as a VLAN unaware switch or when the port is VLAN-wise configured as an ACCESS port.
- Tag all frames. This is used when the port is VLAN-wise configured as a trunk port.
- Tag all frames except those with a specific VID. This is used when the port is VLAN-wise setup as a hybrid port.

These parameters are configured for each individual port in the CATCONF, CATPVID, and TXUPDCFG registers.

Congestion Control

Each port of Heathrow-III can be programmed to handle congestion, either by dropping frames when specific limits are reached, or by reporting Flow Control Condition to the sources of additional packets. The required type of congestion control for a switch based on Heathrow-III is up to the network administrator.

Each port in Heathrow-III has two registers for configuring congestion control. In the POOLCFG register, the flow control mechanism is programmed, and in the DROPCFG register the conditions for dropping frames are set. Each port has a pool of memory for storing frames, and this pool is shared between the ingress and egress queues. By the use of the watermarks found in these registers, it can be assured that all queues receive a fair amount of memory. The memory unit is 256 bytes, and each port has its own 64 units of memory — which equals 16 kB in total per port. The current memory allocation can be read in the FREEPOOL register.

The following examples show three basic modes of congestion control for which a port can be configured.

Drop Mode

In drop mode, dropping incoming frames according to watermarks solves memory depletion. The POOLCFG watermarks must be set so that no flow control mechanisms are activated at any time, which is through values 63 (never reached).

Ingress

A low priority packet is dropped if the amount of ingress data exceeds DROPCFG (Ingress Drop Low), and a high priority packet is dropped if the amount exceeds DROPCFG (Ingress Drop All). By default, the thresholds are 10 and 50 (2.5 kB and 12.5 kB).

Egress

A low priority packet is dropped if the amount of egress data exceeds DROPCFG (Egress Drop Low), and a high priority packet is dropped if the amount exceeds DROPCFG (Egress Drop All). By default, the thresholds are 10 and 50 (2.5 kB and 12.5 kB).

Advanced Drop Mode

The drop mode setup can run with better performance if ports with oversubscribed egress queues (like when many ingress ports are forwarding to the same egress port) can signal their overloaded condition back to the ingress ports. This is called internal flow control. The mode is an extended version of the drop mode setup, and is set by enabling egress flow control in the pool system, through the POOLCFG register. The effects for the two frame directions are:

Egress

When the amount of egress data exceeds POOLCFG (Egress High) the ingress ports are stopped from forwarding more data, and the depletion is feed back to the ingress queues. This is by default 48 (12 kB).

Ingress

If an egress port has blocked further transfers, the forwarding will stop until the POOLCFG (Ingress High) watermark has been reached. This is by default 44 (11 kB). This is only enabled when POOLCFG (Ingress Protection Method) is set to “disobey egress status” (0).

The advanced drop mode configuration is the chip default setup, with the default values as described here.

Flow Control Mode

When running a port in flow control mode, no packet drop is allowed on the port, and memory depletion must be handled by flow controlling the source of additional data. In this mode, the DROPCFG register must be set to not drop any packets at all. This is accomplished by setting all watermarks to 63, as the theoretical maximum consumption from either ingress or egress is 61 memory units. The flow control mechanism is handled through the POOLCFG register.

Ingress Flow Control

When ingress flow control is used, packets are only dropped if no more room exists in the memory pool. With correct threshold settings and correct flow control behavior of transmission sources, dropping will never occur.

The MAC handles the flow control situation in both Full Duplex Mode and Half Duplex Mode. In FDX, the MAC sends flow control frames (pause frames) to the source of the packets telling the source to hold any further traffic. In HDX, the MAC performs Back Pressure to halt the transmitting party by colliding incoming frames.

Transmitted pause frames are filled with the pause time value set in the FCCONF register. If “zero pause enable” is set in the FCCONF register, the MAC will deassert flow control by sending a pause frame with a zero pause time. The source can then reinitiate transmission of packets immediately.

The POOLCFG (Ingress High) watermark determines when flow control is activated towards the incoming stream.

Egress Flow Control

If egress flow control is enabled in the FCCONF register, the MAC will obey received pause frames by pausing the egress traffic for the time given in the pause time.

Additionally, the egress device will report congestion to the ingress ports (by informing the ingress ports of a lack of memory for further egress frames). This is controlled by the POOLCFG (Egress High/Low) watermarks.

Asymmetric flow control, where only ingress or egress has flow control enabled, is supported in Heathrow-III by enabling flow control in the desired direction only.

Flow Control Thresholds

Thresholds must be set with care to avoid packet loss in all cases (provided that no pause frames are lost). The amount of data that can possibly be received from the moment the MAC is asked to send a pause frame until the last byte from the remote partner has been received is:

2 x (maximum frame size) +	[media occupied]
2 x (cable length) x 5 bits x (speed / 1000) +	[data on cable]
250 bytes	[various reaction times]

This value varies for different speeds and cable lengths, as shown in Table 1. Standard Ethernet frame sizes are assumed, with sizes up to 1526 bytes (see the ”Jumbo Frames” on page 36).

Table 1. Flow Control Data Receivable After Pause Frame

Speed	Length			
	10 m	100 m	550 m	2000 m
10	3.1 kB	3.1 kB		
100	3.1 kB	3.1 kB		
1000	3.1 kB	3.2 kB	3.8 kB	5.8 kB

When setting the thresholds, it is beneficial to have as large a part of the pool memory allocated for egress data as possible. This can be accomplished by setting the thresholds using the values from Table 1 in place of the “X” in Table 2.

Table 2. Flow Control Thresholds To Avoid Packet Loss

Threshold	Value
Ingress High	4 kB [at least two max size frames]
Egress High	15 kB – (Ingress High + XTable 1)
Egress Low	15 kB – (Ingress High + XTable 1)

The ingress thresholds can, according to desired operation, be set to other values than the ones suggested. The 15 kB offset used for calculating the egress thresholds is derived from the 16 kB available memory minus the maximum overhead for each queue.

As an example, the configuration for a 1G port on a 550 m media results in thresholds:

- Ingress High = 4 kB – register value 0x10 (256 bytes slices)
- Egress High = 15 kB – (4 kB + 3.8 kB) = 7.2 kB – register value 0x1d
- Egress Low = Egress High – register value 0x1d

Frame Categorization

Each port has a Frame Categorizer, whose main purpose is to determine the priority of ingress frames. This priority can be either high or low, and is based on information in Layer 2–4 within the frame. A number of registers, found in the Categorizer Block Registers, are available for configuring this.

Frame Priority Determination

The priority determination is based on a set of parameters that can be configured in each port. The parameters are mainly targeted at recognizing specific IP frame types, but also other specific frames specified by Layer 2 header fields can be recognized. The set of configurable parameters are listed in Table 3, and are shown in order of execution in Figure 3 (register values shown in the flow chart are default values). Each FSx value in the table is actually a bit in the CATPRIO register, which can be programmed to either 1 (high priority) or 0 (low priority).

When classifying IP frames, only frames of type IPv4 are recognized as of IP type (IP header version field equals 4). A frame is recognized as an 802.2 frame if the Type/Length field is less than 0x600.

Table 3. Frame Priority Parameters

Parameter	Description
Tag Only	Priority is always taken from the IEEE802.1D TCI field. Untagged frames are given the priority FS2. If this option is NOT set, tag information is disregarded, except if CFI in the frame is set. In this case, the priority will be set to FS1.
CATDSAP	IEEE802.2 frames with SNAP encapsulated data will be classified as what is found in the encapsulated data. IEEE802.2 frames with DSAP matching this register, will get priority FS4. All other IEEE802.2 frames will get priority FS5.
CATETHT	Frames with matching Ethernet type (except IP frames) get priority FS6. IP packets are categorized based on the parameters below. All other frame types are assigned priority FS8.
CATPORTx	For TCP/UDP Frames: If their source or destination ports match one of these parameters, their priority is based on the IP DS field found in frame. Nonmatching port numbers result in priority FS7.
CATIPPRT	IP frames (non TCP/UDP) with matching protocol number get their priority based on the IP DS field found in the frame. All other IP frames get priority FS7.

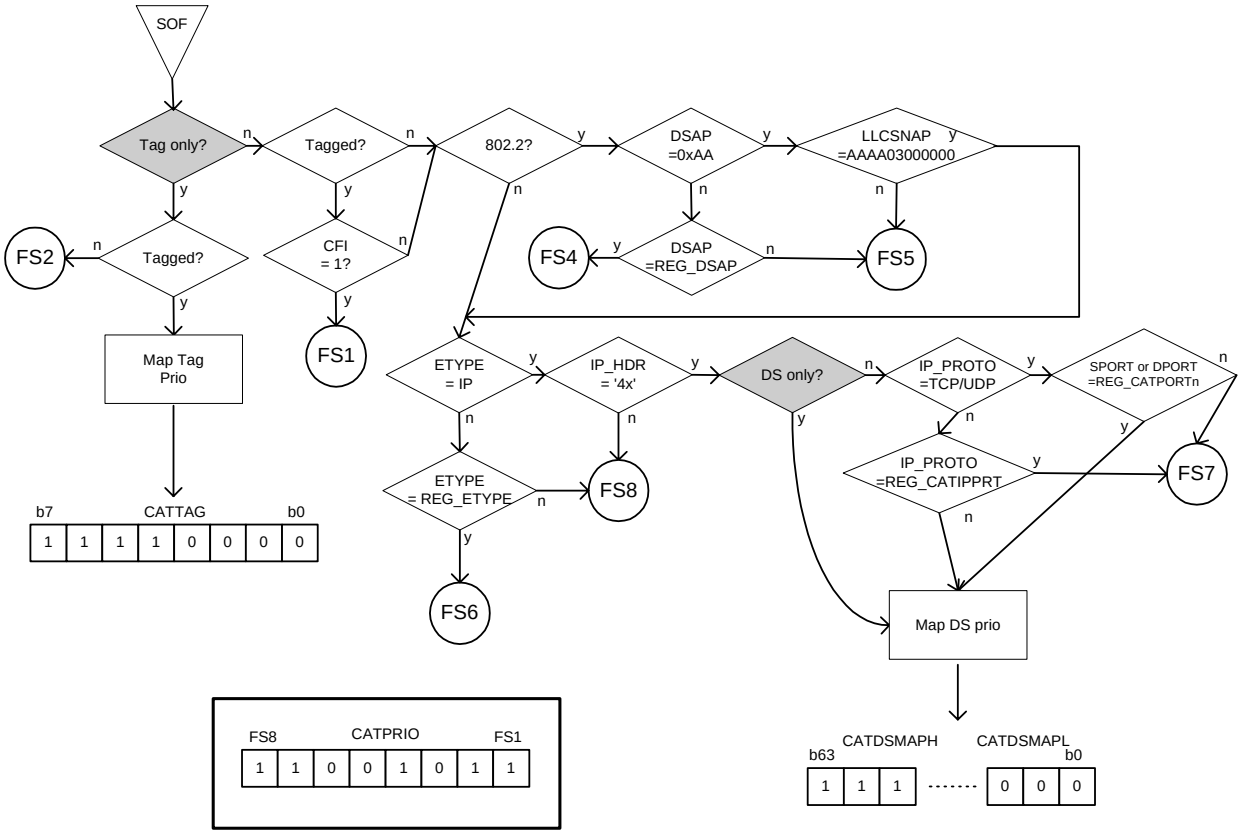


Figure 3. Categorizer Priority Assignment Flow Chart

Example:

All frames with Ethernet type 09A1h are to be prioritized “high”. To do this, set CATETHT = 9A1h, FS6 = 1, and all other FSs = 0.

When the Tag priority is used to prioritize, the CATTAG register is used to translate the 8 tag priority values into low or high priority. When IP packets' DS fields are to be used for priority calculation (according to the table above), the CATDSMAPL/CATDSMAPH registers are used. DS will be used either when an IP port or protocol match is found, or when the DS-only flag is set in the CATCONF register. Refer to the register list for further information.

Frame Class Determination

Another task for the Categorizer is to determine a class for each packet. This class is used in the frame analysis process to decide where to send the packet. The classes recognized by the Categorizer and the codes given to the Analyzer are shown in Table 4.

Table 4. Frame Classes

Frame Type	Condition	Class To Analyzer
Reserved Addresses (IEEE802.1D 7.12.6)	DMAC = 0180C200000x (STP, BPDU)	FORCECPUONLY (MAC control frames will be filtered by the MAC)
IP/ARP MAC broadcast	DMAC = BC, Type = IP/ARP	FORCECPU
IGMP	DMAC = 01005Exxxxxx, Type = IP, IP type IGMP	FORCECPUONLY
IP Multicast Data	DMAC = 01005Exxxxxx, Type = IP, non IGMP, DIP outside 224.0.0.x	MUSTBEKNOWN
IP Multicast Ctrl	DMAC = 01005Exxxxxx, Type = IP, non IGMP, DIP inside 224.0.0.x	FORCECPU
Others	Others	NORMAL

For a class to be recognized, it must be enabled in the CATCONF register. The class is transferred to the Analyzer module, which uses it in the process of determining the set of egress ports to which each packet should be forwarded. Refer to Table 11.

Policing

The policing feature of Heathrow-III provides per-port data rate control at a granularity of less than 256 kb/s and operates on all frame types. There is also a separate Policer dedicated to broadcast and multicast traffic; this enables Broadcast Storm Control.

None of the two Policers will affect packets destined for the CPU queue only.

General Policer

The POLICECONF register is used to set up the Policer:

- Bit 24:16: “Bucket Threshold”: The bucket threshold, measured in units of 512 bytes
- Bit 11:0: “Data Rate”: The bucket is emptied with this rate. Rate unit is speed dependent:
  - 1G: 244 kb/s
  - 100M: 48.8 kb/s
  - 10M: 4.88 kb/s

Each incoming packet causes the bucket level to be increased by a number equal to the packet size (without preamble and IFG) measured in bytes. The bucket level is decreased at a steady rate corresponding to the value of the Data Rate bit field.

Policer behavior depends on the two bits Drop Mode and Flow Control Mode:

- Bit 31: “Drop mode”: Dropping of packets in case the bucket threshold is reached

If the bucket level reaches the Policer threshold, packets are discarded and the bucket level is not increased. Over time, the bucket level will drop below the threshold. At this time, packets will be allowed to enter the switch again.

- Bit 30: “Flow control mode”: Generation of flow control in case the bucket threshold is reached

If the bucket level reaches the Policer threshold, flow control frames are generated. Packets are not discarded. Over time, the bucket level will drop below the threshold. At this time, the flow control condition is cleared again.

The Policer is completely disabled if both bits are disabled (0).

Broadcast/Multicast Policer

The Policer used for Broadcast and Multicast Storm Control is set up with the MCSTORMCONF register. Rate parameters are set up like the general Policer.

Shaping

The shaping feature of Heathrow-III provides per port data rate management at a granularity of less than 256 kb/s.

The SHAPECONF register is used to set up the shaper:

- Bit 24:16: “Bucket Threshold”: The bucket threshold, measured in units of 512 bytes
- Bit 11:0: “Data Rate”: The bucket is emptied with this rate. Rate unit is speed dependent:
  - 1G: 244 kb/s
  - 100M: 48.8 kb/s
  - 10M: 4.88 kb/s

Each packet leaving the switch causes the bucket level to be increased by a number equal to the packet size (without preamble and IFG) measured in bytes. The bucket level is decreased at a steady rate corresponding to the value of the Data Rate bit field.

Shaper behavior depends on the two bits Drop Mode and Hold Mode:

- Bit 31: “Drop mode”: Dropping of packets in case the bucket threshold is reached

If the bucket level reaches the shaper threshold, packets are discarded and the bucket level is not increased. Over time, the bucket level will drop below the threshold. At this time, packets will be transmitted again.

- Bit 30: “Hold mode”: Holding back packets in case the bucket threshold is reached

If the bucket level reaches the Shaper threshold, packets are kept in the egress queue. As no packets are leaving the transmit queues, the bucket level is not increased. Over time, the bucket level will drop below the threshold. At this time, packets will be allowed to leave the switch again.

The shaper is completely disabled if both bits are disabled (0).

Frame Analysis

Tables in the Analyzer

The central Heathrow-III Analyzer module maintains a number of tables and masks. Table 5 lists the most important ones. Refer to the register list for more details.

Table 5. Basic Frame Analysis Data

Table/Register	Description
MAC Table	8192 stations learned by CPU or auto learned; each entry in the table is a MAC record

Table 5. Basic Frame Analysis Data (cont'd)

Table/Register	Description
VLAN Table	4096 masks with allowed egress ports for each VID, and a flag – SourceChk - for checking the ingress port as being a member of the VLAN in which frames are received
Source Port Masks	16 port masks with allowed egress ports for each ingress port
Destination Port Masks	64 port masks with translation of logical port indexes to port masks
Aggregation Port Masks	16 port masks with allowed egress ports for each Aggregation Key
Unicast Flooding Mask	A port mask indicating where to send unicast packets with unknown destination addresses
Multicast Flooding Mask	A port mask indicating where to send multicast packets with unknown destination addresses; this mask also covers the broadcast address

Analysis Overview

The end result of a frame analysis is the Forwarding Mask containing the set of egress ports to which the analyzed frame is to be forwarded.

The forwarding decision is based on header information from the incoming packets, user configured tables, auto learned information, and the CPU class reported by the Categorizer (see the "Frame Class Determination" on page 25).

The general flow is as shown in the Figure 4. Special cases (analysis exceptions) are not shown, but are described in the "Exception Flags" on page 35.

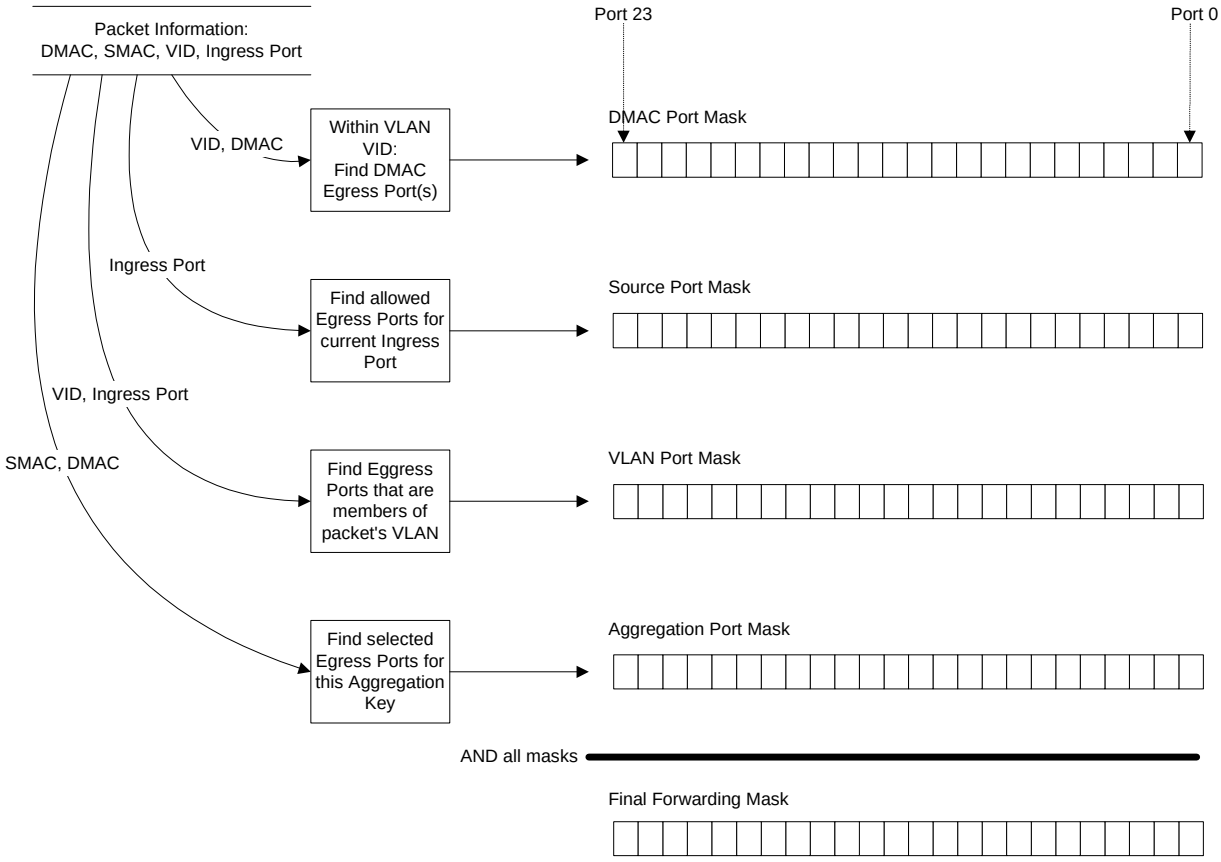


Figure 4. Frame Analysis

The Final Forwarding Mask is the set of egress ports that will each get a copy of the packet - basically that is the ports which all passed the four subanalysis steps shown in Figure 4.

The MAC Table

Heathrow-III keeps track of which Destination MAC address belongs to which port, by writing and reading an internal MAC address table. This table is used in the DMAC Analysis Block where it is checked if the DMAC address in the packet has been previously used as an SMAC address.

The MAC table consists of 8192 records with the contents described in Table 6.

Table 6. MAC Address Table

MAC Record Field	Description
MAC Address	The 48-bit Mac address (matched at lookup)
VLAN ID	The 12-bit VLAN ID (matched at lookup)
Destination Index	Destination Mask number

Table 6. MAC Address Table (cont'd)

MAC Record Field	Description
Aged Flag	Flag: ageing has run since last learn of this address
Locked Flag	Flag: entry is locked. It will not be aged out nor overwritten
Valid	Flag: entry is valid
CPUCopy	Exception Flag: copy frames destined for this DMAC to the CPU buffer
FwdKill	Exception Flag: do not forward packets with this DMAC to any ports
Ignore	VLAN Exception Flag: do not apply VLAN port mask for packets with this DMAC

The table is automatically updated by an auto learning process, a CPU based learning process, or by direct manipulation from the CPU through register accesses (see "Direct MAC Table Access" on page 30). The MAC address and VLAN ID are the identification of the station, the three flags hold the status of the entry, and the three exception flags are for special purposes, as explained later.

For auto-learned ports, the Destination Index number is the port number it was learned from plus 4 (port+4). It is used as a pointer into a table of 64 Destination Port Masks, each translating this logical index number into a set of egress ports. In standard setups, only Destination Port Mask 4-19 are used, and per default they are all configured to have only the port bit corresponding to their index set. So, if a station is learned on port 4, its record will have '8' (4+4) in the destination index, and when packets are sent to the station, Destination Port Mask number 8 will be used—which is a port mask with only bit 8 set.

Direct MAC Table Access

As mentioned, apart from the more automated learning processes, it is also possible to directly access the table in order to dump the contents or to write specific data at specific locations. This happens via the register interface.

The MAC table is organized as a 2048x4 entry hash table. When directly accessing the table, the MACTINDX is first written with the desired record table position, and a Read Entry or Write Entry command is hereafter issued through the MACACCES register. Each operation will auto increment the index to ease dumping or updating the whole table.

Table 7. MAC Table Layout

Hash Key	0	1	2	3
0	MAC Record	MAC Record	MAC Record	MAC Record
1	MAC Record	MAC Record	(empty)	(empty)
2	MAC Record	(empty)	(empty)	(empty)
3	(empty)	(empty)	(empty)	(empty)
4	MAC Record	MAC Record	MAC Record	MAC Record
. . .	. . .	. . .	. . .	. . .
2047	MAC Record	MAC record	(empty)	(empty)

A MAC entry MUST be written into the correct hash chain, in order to be found by the search engines. Therefore, when accessing the table for specific addresses, the table index must comply with the hash key formula, which basically is an XOR operation on most of the station identification (VLAN,MAC).

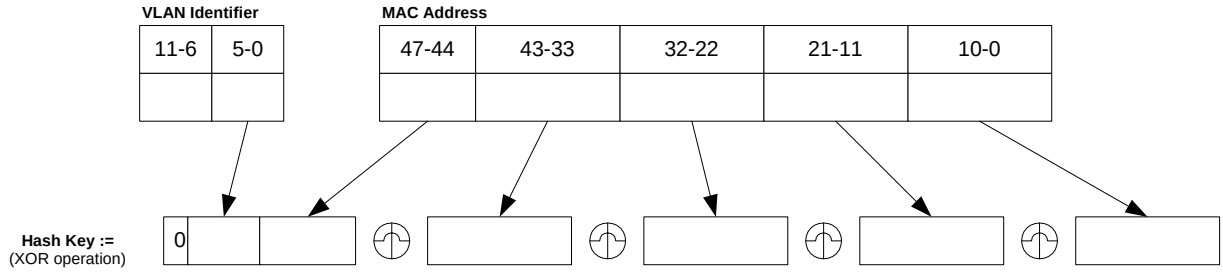


Figure 5. Hash Key Calculation

Example:

MAC address 00-00-12-34-56-78, in VLANID 15 has the hash key = xor (0F0h,000h,048h,68Ah,678h) = 4Ah = 74 decimal.

Every time the search engines are looking up this address, hash chain 74 will be searched.

The frame analysis process reorders each of the chains internally. To be able to read out all four entries of a chain while the analysis engine is operating, a chain shadow register can be enabled through the MACTINDX register. When using this, only reading bucket 0 will make a physical read from the table, and buckets 1–3 will be stored in a shadow chain. Refer to the register description.

Automatic Learning From Incoming Packets

Learning of stations is done automatically if enabled for the ingress port. The learning process inserts an entry into the MAC table where:

- MAC = source MAC address from packet
- VID = Source VID from packet (or PVID if untagged)
- Destination Index = ingress port number
- Flags aged = locked = false, valid = true
- Flags Ignore VLAN, CPUCopy, FwdKill as configured in the AGENCNTL register

The learning occurs at wire speed on every packet received. Regardless of a station already being present in the table, the learning mechanism is still activated. In this aspect, a station is learned every time it is seen as a source address.

The learning can be made dependant on the port being a member of the VLAN which the frame is received in by setting the VlanCheck flag in the ADVLEARN register.

Manually Manipulating MAC Table Entries Via The CPU

MAC table entries can also be manually manipulated via the CPU Interface. Here, the CPU has full control over the flags and Destination Index inserted. This can be used for setting up permanent stations or multicast groups, where

the locked flag must be set. In addition, it is used for CPU Based Learning (see the ”CPU Based Learning” on page 42).

When setting up a permanent station on a port, the CPU can write an entry with the Destination Index pointing to the port where the station is permanently attached, and the locked and valid bits are set.

When setting up a multicast group, an unused Destination Port Mask is first allocated. It is used to remember the set of egress ports that belong to the group. After that, an entry is created in the MAC Table with the Destination Port Index pointing to the allocated Destination Port Mask, and the locked and valid bits are set.

Unlearning/ageing

By writing an AGE command to the MAC Table Command register (MACACCES) which subsequently causes the Analyzer to run through all entries, ageing is performed. In such an ageing pass, one of two things happens to each entry: If the aged flag is set, the entry will be cleared, else if the aged flag is clear, the flag will be set. The only exceptions to this procedure are locked entries, which won't be modified. In this way, all nonlocked entries that haven't been relearned between two ageing passes are removed.

Immediate unlearning of single MAC addresses is done by issuing a FORGET to the MACACCES register.

Frame Forwarding Decision

The analysis of where to send a packet is done in four separate steps (see Figure 4). Each of these steps takes different conditions into account, as explained in the following sections.

DMAC Processing

This block finds the possible egress ports based on the DMAC and VID found in the packet. The MAC table is searched for an entry with matching VID and DMAC, and the output mask from this step is the Destination Port Mask pointed to by the Destination Index found in the record. If the entry could not be found, one of the globally configured Flooding Masks is instead returned causing the packet to be forwarded to all the ports that have their corresponding bit set to 1 in the Flooding Mask.

VLAN Processing

The VLAN processing part looks up the allowed set of egress ports for the reported VID. The mask containing this information is taken from a configured table of records (VLAN Table). By default, this table is set to all 1s in all records meaning that all ports are members of all VLANs. Each VLAN in the table can also be marked with the requirement that the ingress port must be a member of the VLAN if ingress packets are to be forwarded from this port. If this flag (“Source Check”) is set and the ingress port's bit is not set in the given VLAN Table entry, the resulting mask from this step will be all 0s, that is, the packet will not be forwarded to any port.

Source Port Processing

A packet must never be forwarded to its ingress port, as this results in network loops. This step ensures that this cannot happen. The ingress port number is used as an index into a table of 16 port masks, each containing the set of egress ports to which a packet from any of the ingress ports may be forwarded. By default, every port bit in every mask of this table is set to 1, except the bit corresponding to each port's number. The source port masks can also be used to facilitate VLANs only defined by the switch port on which the packets are received (port grouping or port based VLANs).

Aggregation Processing

Link aggregation is a method of logically grouping a set of ports, so that two network stations can be interconnected using multiple links. All stations learned in a group of ports must be able to receive packets from all connections in the group. Also, the stations learned on any port in the group must be able to correctly forward frames to any other port in the group – like station B in Figure 6. This method is used to create larger bandwidths between network nodes.

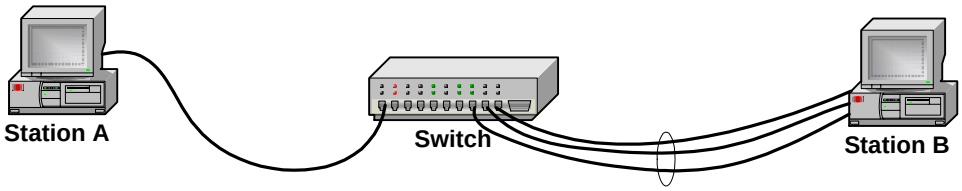


Figure 6. Aggregation Example

Some of the port masks mentioned previously must be set to reflect the groups:

The Source Port Masks (SRCMASKS): For each port, this mask must be set so an ingress port in a group can't forward to any of the other ports in the same group

The Destination Port Masks (DSTMASKS) must be set so that a station learned on a port in a group can receive frames from all ports in that group.

When using link aggregation, the Aggregation Port Masks (AGGRMSKS) are used to guarantee that any one frame is transmitted only on one port within a group. To achieve this, Heathrow-III calculates an Aggregation Key with a value between 0 and 15 for every packet received. The value is calculated in one of three ways, determined by the AGGRCNTL register, to be:

- The four LSBs of the Source MAC Address (SMAC)
- The four LSBs of Destination MAC Address (DMAC)
- The four LSBs of (SMAC XOR DMAC)

When calculated, the Aggregation Key is then used as an index into a table of 16 Aggregation Port Masks. In a nonaggregated setup, these masks are set to all 1s (the default value), but when setting up one or more aggregated groups, the masks must be configured such that only one port bit is set in each group.

In short, aggregation works like this:

1. SMAC/DMAC is calculated into an Aggregation Key
2. The Aggregation Key points to one of sixteen Aggregation Port Masks
3. The selected Aggregation Port Mask shows which port in the group should get the packet

Example:

Two aggregated groups are to be established. They consist of

Ports 2, 6, and 7

Ports 12, 13, 14, and 15

The Port Masks must be set as shown in Table 8, Table 9, and Table 10. In the tables, read the rows as flags for port 15 (leftmost) to 0 (rightmost).

Table 8. Source Port Masks

Port	Source Port Masks															
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
2,6,7	1	1	1	1	1	1	1	1	0	0	1	1	1	0	1	1
12,13,14,15	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Others	All 1 except the bit corresponding to the port_number+4															

Table 9. Destination Port Mask

Port	Destination Port Mask															
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
2,6,7	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0
12,13,14,15	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Others	All 0 except the bit corresponding to the port_number+4															

Table 10. Aggregation Port Mask

Aggregation Key	Aggregation Port Mask															
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
0	0	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	0	1	1	1	1	0	1	1
2	0	1	0	0	1	1	1	1	1	0	1	1	1	0	1	1
3	1	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1
4	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1
5	0	0	1	0	1	1	1	1	1	0	1	1	1	0	1	1
6	0	1	0	0	1	1	1	1	0	0	1	1	1	1	1	1
7	1	0	0	0	1	1	1	1	0	1	1	1	1	0	1	1
8	0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1
9	0	0	1	0	1	1	1	1	0	0	1	1	1	1	1	1
10	0	1	0	0	1	1	1	1	0	1	1	1	1	0	1	1
11	1	0	0	0	1	1	1	1	1	0	1	1	1	0	1	1
12	0	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1
13	0	0	1	0	1	1	1	1	0	1	1	1	1	0	1	1

Table 10. Aggregation Port Mask (cont'd)

Aggregation Key	Aggregation Port Mask															
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
14	0	1	0	0	1	1	1	1	1	0	1	1	1	0	1	1
15	1	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1

Exception Flags

In the preceding, only the most simple analysis cases have been explained. As mentioned in ”The MAC Table” on page 29, some exception flags exist. Together with the class reported by the Categorizer on the ingress port, the exception flags can alter the way the masks are ANDed together.

Each entry in the MAC table has 3 exception flags:

- Ignore VLAN flag: The VLAN port mask will NOT be ANDed with the forward mask
- FwdKill: The Destination Port Mask will be set to all 0s
- CPUCopy: Frames for this address will be copied to the CPU capture buffer

Entries, which have been auto learned, have their exception flags set to the configured learn flags, found in the AGENCNTL register. CPU learned entries have their exception flags set individually at the insert operation. During analysis, the flags found in the MAC record are used, if the lookup succeeded. Otherwise, flooding flags (also found in the AGENCNTL register) are used.

Examples of the use of these exceptions are:

- GVRP frames are to be sent to the CPU buffer, and not be forwarded elsewhere
- Packets are to be held back for a specific station
- Packets destined for a reserved management MAC address are to be sent to the CPU, and not elsewhere

In the first case, an entry from the CPU with DMAC = 0180C2000021 (GVRP), valid = locked = 1, FwdKill = 1, CPUCopy = 1, is inserted. An entry must be inserted for each VLAN the frame can be received in. As GVRP frames are untagged, this means that the possible VLANs are the set of PVIDs on the ports where GVRP frames can be received.

In the second case, a permanent entry with DMAC = the station, VID = the VLAN in which the station was found, valid = locked = 1, FwdKill = 1, CPUCopy = 0, is inserted.

The third case is handled like the first one.

Categorizer Class

The final special case of the analysis flow is the Categorizer Class reported by the Categorizer block on the ingress port. As mentioned in the ”Frame Class Determination” on page 25, four different classes exist. The default class is NORMAL. When this is reported, no change is made to the analysis flow as it has been described above. But if enabled in the CATCONF register, the other classes will be reported. The meaning of these is explained in Table 11.

Basically, all the masks are ANDed. As previously mentioned, the flags reported by the DMAC process, the VLAN process, or the received Categorizer Classification can change this.

Table 11. Categorizer Classes

Categorizer Class	Meaning
MUSTBEKNOWN	If the DMAC was not found in the MAC table, FwdKill flag is forced. This is reported for IP Multicast DMACs and when running IGMP Snooping - in which case unknown multicast addresses should not be forwarded.
FORCECPU	The CPUCopy flag will be forced. This is used for IP/ARP MAC broadcast frames and for capturing ARP broadcasts. This is necessary when operating an IP end station through Heathrow-III.
FORCECPUONLY	Both the CPUCopy and the FwdKill flags are forced. This is used for all BPDU type frames. BPDUs must never be forwarded to any port according to IEEE802.1D.
NORMAL	The CPUCopy and FwdKill flags are as reported from the DMAC process.

Port Mirroring

The frame analysis engine has an option to mirror all packets either

- Belonging to a specific VLAN, or
- Received on specific ports

The target port number is configured in the AGENCNTL register, and the source number (VLAN or port) is set in the VLAN table and source port masks. The CPU capture can also be mirrored in the sense that all frames destined for the CPU can be forwarded to the mirror port also. This is also set in the AGENCNTL register.

Jumbo Frames

Heathrow-III supports jumbo frames of up to 12.2 kB. The default chip configuration is set to a maximum length of 1518 bytes, but this can be changed through the MAXLEN register.

Because the shared pool for frames in each device is 16 kB, the thresholds must be carefully chosen to allowing flows of relatively large frames. Otherwise, the pool control system drops frames before they are fully stored. This is handled through the POOLCFG register.

Jumbo frames are best supported on 1G links running drop mode, but can also be used for other port modes. The aspects are described below.

QoS And Jumbo Frames

Because the memory for storing frames is limited to 16 kB, it is not possible to have both high and low priority jumbo frames. Either all frames must be classified for high priority, or only high priority frames can be allowed to have jumbo size (by setting the low priority thresholds much lower than the high thresholds). For smaller sizes of jumbo frames, like 4 kB, some degree of QoS would be possible.

Flow Control And Jumbo Frames

The use of flow control while simultaneously allowing jumbo frames has limitations. This is because the amount of excess data that can arrive between the time a pause frame is required to be transmitted and the time at which the remote partner stops transferring more data can be as much as two maximum sized frames. The sequence is:

1. The MAC starts transmission of a maximum size frame
2. Shortly after, the thresholds trigger a pause frame transmission
3. The MAC finalizes the (1) transmission, and initiates the (2) pause frame
4. The remote link partner initiates a maximum size frame transmission
5. Shortly after, the remote partner receives the (3) pause frame
6. The remote partner finalizes the (4) maximum size frame
7. The remote partner suspends transmission due to (5)

The delay from (2) to (7) is more than two maximum sized frames, which, in the case of jumbo frames, is more than the available memory. It is therefore not immediately possible to utilize flow control and bidirectional jumbo frames on the same ports. If, however, the jumbo frames are flowing only in one direction, it is possible to configure the ports for proper flow control.

Early Transmission

Because the pool memory is smaller than two jumbo frames, it is not immediately possible to have a bidirectional stream of jumbo frames between two ports, as this would require pool memory for at least two jumbo frames: one ingress and one egress (store & forward both on ingress and egress). To enable this, an early transmit mechanism is available in the ports, allowing the MACs to initiate transmission before the egress frame is fully stored. This is configured in POOLCFG through the early transmit level. This level is per default disabling early transmission. To avoid malfunction in the device, it is a requirement that an entire frame, which has been initiated for transmission, can be stored in the egress pool. Therefore, the early transmit level must be set correctly, taking the ingress to egress transfer speed into account, which is 30% larger than the MAC-TX speed at 1G. This requirement is best described through examples. The examples here assume that the ports operate in drop mode. Furthermore, jumbo frames cannot be multicast with the examples described below, because they cannot be early initiated. For details about multicast forwarding jumbo frames, refer to the Heathrow-III API.

Example 1: Jumbo frames of 9 kB required, on 1G ports

MAXLEN = 9 kB

ingress high threshold = 9.5 kB

egress high threshold = 6.5 kB

When an egress frame is MAC initiated and n kB have already been received from the ingress port, the maximum amount of data to be stored during the MAC transmission is $n + (1.3 – 1.0) \times (9 – n) = 2.7 + 0.7 \times n$. This must not exceed 6.5 kB (egress threshold), and therefore $2.7 + 0.7 \times n < 6.5$, which requires $n < 5.4$. Early transmit level must be set to 4 kB.

Example 2: Jumbo frames of 12 kB required, on 1G ports

MAXLEN = 12 kB

Ingress high threshold = 12.5 kB

Egress high threshold = 3.5 kB

When an egress frame is MAC initiated and n kB have already been received from the ingress port, the maximum amount of data to be stored during the MAC transmission is n + (1.3 – 1.0) x (12 – n) = 3.6 + 0.7 x n. This must not exceed 3.5 kB (egress threshold), and therefore 3.6 + 0.7 x n < 3.5, which requires n < 0. Early transmit is therefore *not* possible for frames of 12 kB. Both ingress and egress thresholds must be set to 12.5 kB, and frame drops are inevitable when both directions are active with jumbo frames.

Example 3: Jumbo frames of size 4 kB required, on 1G ports

MAXLEN = 4 kB

Ingress high threshold = 8 kB

Egress high threshold = 8 kB

When an egress frame is MAC initiated and n kB have already been received from the ingress port, the maximum amount of data to be stored during the MAC transmission is n + (1.3 – 1.0) x (4 – n) = 1.2 + 0.7 x n. This must not exceed 8 kB (egress threshold), and therefore 1.2 + 0.7 x n < 8, which requires n < 9.7. This is much higher than the maximum frame size, so early transmission is not required, but still has some memory utilization advantages.

Jumbo Frames on 10/100 Ports

When transmitting jumbo frames on 10/100 ports, early transmission is not applicable, as almost all of the frame will be received from the ingress ports while the egress transmission is in progress due to the much higher ingress to egress transfer rate. Because having a fully stored ingress packet in memory is required, there is not sufficient room for a full egress frame. This can be solved by the use of egress flow control.

Example: Jumbo frames of size 9 kB required, on 10M ports

MAXLEN = 9 kB

Ingress high threshold = 9.5 kB

Enable egress flow control, with High Threshold = 5.5 kB (suspend), Low Threshold = 5.0 kB (resume)

This way, the switch will effectively be input buffered, which may result in lower head-of-line performance.

CPU Packet Transmit and Receive

It is possible to send and receive frames to and from any port via the CPU interfaces. This is useful for implementing traffic control protocols such as Spanning Tree Protocol, GVRP, IGMP snooping, and so forth for letting the CPU act as an end station on the network, or when using CPU based learning. The packet injection/readout is done through the register interface.

CPU Packet Transmission

The transmission of packets is done by injecting packets into the transmit queues of the ports that should transmit them. This is accomplished by writing certain registers in the shared FIFO block of the ports. The sequence is:

1. Write the frame length shifted 16 bits left, to the CPUTXDAT register (length is in bytes, including CRC)
2. Write a fixed signature – 0x00000254 to CPUTXDAT
3. Write the frame data including CRC field to CPUTXDAT

4. If an odd number of writes occurred, write an extra word to CPUTXDAT
5. Set the CPU Tx bit of the MISCFIFO register

A write operation to the CPUTXDAT queue can internally take more time than the delay before the next operation. Therefore, the CPU must check that the queues are ready for additional data, which can be done in two ways:

- By checking the “CPU Tx Data Pending” bit in the MISCSTAT register for the port after each two words written
- By checking the “CPU Tx Data Overflow” bit in the MISCSTAT register for the port after the whole frame is written, but before the “CPU Tx” bit (step 5) is applied. If this bit is set, a rewind operation must be issued to the MISCFIFO register, and the frame must be rewritten to the queue. This can be done by either the “pending” or the “overflow” method as desired

NOTE: *It is the responsibility of the switch control software to ensure a minimum frame size of 64 bytes, as Heathrow-III does not pad automatically.*

Heathrow-III can replace the CRC value set in the frame, by the use of the TXUPDCFG register. This saves the CPU from having to calculate the correct CRC value.

CPU Packet Reception

As explained previously, it is possible to copy or redirect frames to the 16 kB CPU buffer. Through the register interface these packets can be read out and released from the buffer again, so more frames can be stored. If the buffer space is depleted, additional frames targeted for the capture buffer will be dropped.

The frame availability status of the buffer can be read in the CPUCTRL register. Through this register it is also possible to have an interrupt generated when packets are ready to be read.

By writing to the CAPREADP register, the first frame in the receive buffer is released, and the status bit of the CPUCTRL register is updated. The capture RAM is mapped into the register space as shown in Figure 7.

The address space for the capture buffer is always aligned so that the next nonreleased packet is read from the beginning of the buffer. The most significant byte in this address is the first byte of the frame header. When the packet is released, the address space is realigned to the next frame.

The CPU capture buffer is 16 kB, but only 4 kB can be seen at a time through the register interface. The first 1 kB is accessed in Subblock 0, the second in Subblock 1, the third in Subblock 2, and the fourth in Subblock 3. For a single normal frame (which only have sizes of below 2 kB [1526 bytes, in fact]), only the first two subblocks are needed. For further details about the register space, refer to the ”Spanning Tree Protocol” on page 43. If jumbo frames are forwarded to the capture buffer, with sizes larger than 4 kB, they can only be read out by means of some manipulations with the stored headers. If this is needed, refer to the software API provided.

The frame header is shown in Figure 7. For a detailed description of each field, refer to Table 12.

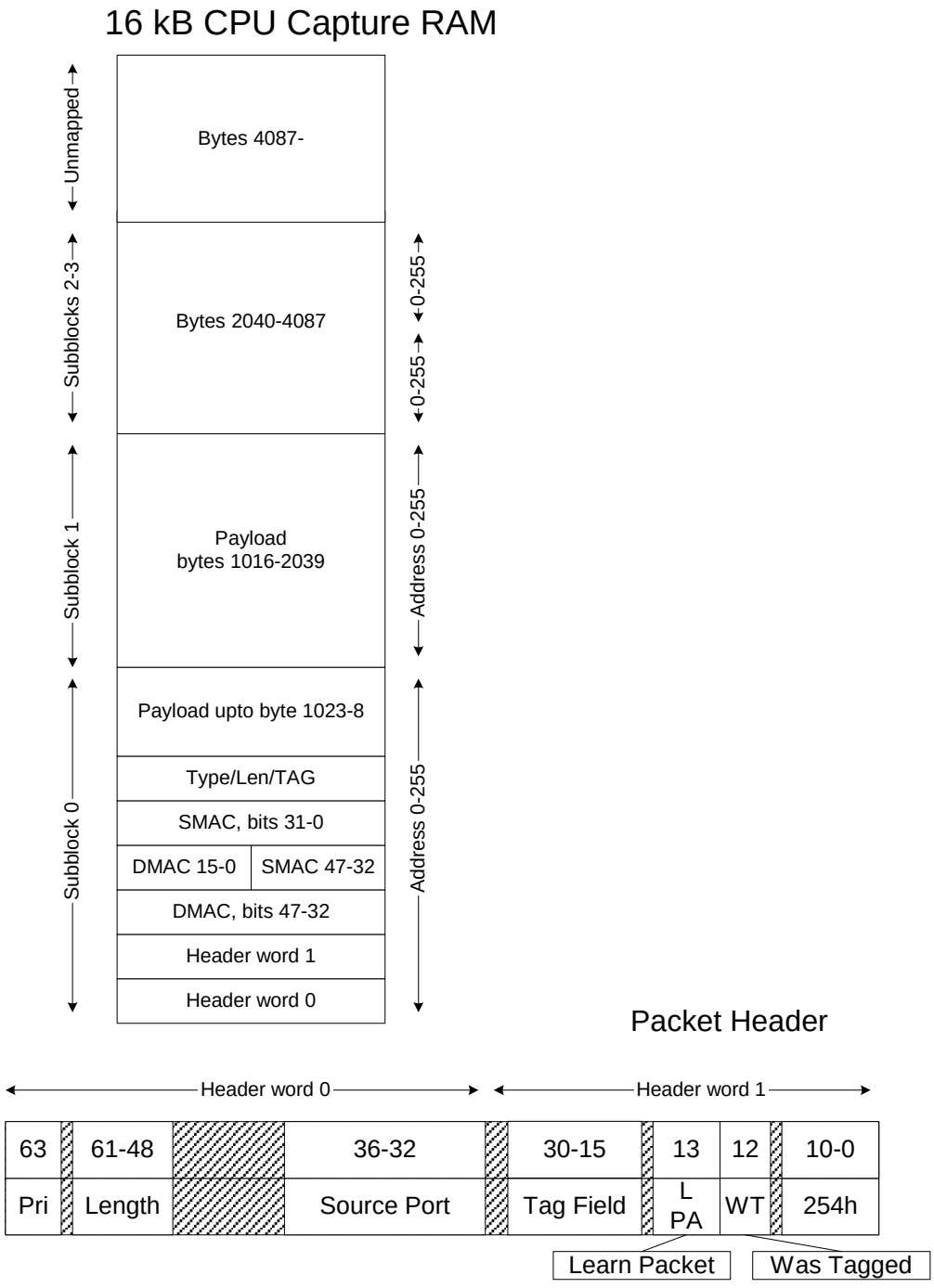


Figure 7. CPU Capture Buffer

Table 12. Packet Header Format

Header Field	Description
Pri	The priority decided by the Categorizer (1 = high)
Length	The frame length excluding this header, including CRC
Source Port	The source port of the frame (4–19, where 4 = port 0, and 19 = port 15)
TagField	The tag field found in the frame. If frame was untagged, this field is set to the CATPVID register value
LPA	Learn Packet. Packet forwarded to CPU as a learn request
WT	Was Tagged. Packet was tagged when arriving at the ingress port
254h	This is a fixed signature checked by the internal queue system

Example:

An interrupt routine for reading out frame from the CPU Capture Buffer. (Notation for registers: block. subblock. Address. Further information about register addressing is found in the ”Spanning Tree Protocol” on page 43).

```
Interrupt(
     If read(SYSTEM.0.CPUCTRL).CPU Rx_Frame_Ready = 1 then
         Hmsw = read(CAPTURE.0.0); Hlsw = read(CAPTURE.0.1)
         If NOT ((Hlsw and 0x7ff) = 0x254) then -- Unexpected error
         Pri:=(Hmsw >> 31) AND 0x1
         Len:=(Hmsw >> 16) AND 0x3FFF
         SrcPort:=Hmsw AND 0x1F
         Tag:=(Hlsw >> 15) AND 0xFFFF
         WasTagged:=(Hlsw >> 12) AND 0x1
         Learn:=(Hlsw >> 13) AND 0x1
         For x=0 to (len-1)/4 loop
             ofs=x+2 -- First two words are the buffer header!
             Pktdata(x)= read(CAPTURE.(ofs/256).ofs MOD 256)
         End loop
         If Learn AND (read(SYSTEM.0.CPUCTRL).Learn_Truncate = 1) then
             LenCaptured:=64
         Else
             LenCaptured:=Len
         End If
         Enqueue (pktdata,src,len,...)
         Write(CAPTURE.4.CAPREADP)
     End if
)
```

CPU Based Learning

As default operation, Heathrow-III will auto learn all SMAC addresses into the MAC table. When more advanced learning policies are required, the CPU capture function can instead be used to allow CPU based learning (see the ”Manually Manipulating MAC Table Entries Via The CPU” on page 31). The learning method is configured through the ADVLEARN register, where it is possible to disable the auto learning mode and to request that all packets subject to learning or station move to be forwarded to the capture queue. It is also possible to have all learn packets forwarded to specific ports. This can be used for NPU attachment or for debugging purposes.

If packets from unlearned stations are to be discarded for security reasons, learn drop mode can be enabled (also through the ADVLEARN register).

Through the CPUCTRL register, it is possible to truncate all learn frames forwarded to the CPU so that only the first 64 bytes are stored. The length field in the packet header holds the original packet length (see coding example above).

MII Management Bus

In Heathrow-III, two identical, independent MII Management controllers exist for accessing PHY registers.

The controllers are programmed with target PHY address, register index, and write data. A status register indicates when the operation is complete.

As each MIIM controller can address 32 PHYs, Heathrow-III can manage a total of 64 PHYs.

The operation is set up in the MIIMCMD register, status is read from the MIIMSTAT register, and the read result can be found in the MIIMDATA register.

The two controllers are selected by using either Subblock 0 or Subblock 1.

Scan Operation

The controllers also have the ability to scan a range of PHYs, mainly for automatic polling of link status from the PHYs' status registers. The scan feature is programmed with:

- The range of PHY addresses to be read
- The index of the register to be read from each PHY
- A value mask (PhyRegMask) used to mask out the bit(s) that are to be checked

Heathrow-III continuously reads the specified register bit(s) in the PHYs within the specified PHY range. When the register value is available, a scan result register (MIIMSRES) has the bit position corresponding to the PHY address read, updated. This bit value will be set to 1 if all the bits set in the valuemask is also set in the read reply.

To handle multiple changes in the response from a PHY between two CPU reads of the MIIMSRES register, only the first change in each PHY’s scan result is saved, until the CPU has read the result register.

Example:

How to continuously update the Link Status for PHY numbers 10-17.

- Set MIIMSCAN to PhyAddrLow = 10, PhyAddrHigh = 17, PhyRegMask = 0x0004.
- Set MIIMCMD to SCAN, READ, PhyAddr = 10, PhyReg = 1.

Bit 10-17 in the MIIMSRES register now reflects the link status of PHYs 10-17.

In the above example, it is presumed that the link status of the PHYs is found in register 1, bit 2 (common position in most PHYs).

Spanning Tree Protocol

This section describes how the various Spanning Tree Protocol states are supported in Heathrow-III. The states include listening, learning, forwarding, blocking, and disabled. According to the IEEE802.1D standard, the Spanning Tree Protocol states have the properties listed in Table 13.

Table 13. Spanning Tree Protocol Port State Properties.

State	BPDU reception	BPDU generation	Frame forwarding	SMAC learning
Disabled	No	No	No	No
Blocking	Yes	No	No	No
Listening	Yes	Yes	No	No
Learning	Yes	Yes	No	Yes
Forwarding	Yes	Yes	Yes	Yes

These states can all be configured in Heathrow-III through the CATCONF, SRCMASKS, and LERNMASK registers. Table 14 lists how a port ‘portId’ is configured to the different states.

Table 14. Spanning Tree Protocol Port State Configuration of Heathrow-III

State	’BPDU Capture’ in CATCONF, port ‘portId’	SRCMASKS, mask ‘portId’	LERNMASK, bit ‘portId’
Disabled	0	0	0
Blocking	1	0	0
Listening	1	0	0
Learning	1	0	1
Forwarding	1	1 except for bit ‘portId’	1

In terms of Heathrow-III configuration, there is no difference between the Blocking and the Listening state. It is simply up to the CPU to throw away BPDU in the Blocking state.

CONFIGURATION

Command Interfaces

Through a CPU attached to Heathrow-III, it is possible to configure, monitor, and collect statistics from different parts of the switching engine.

In Heathrow-III, there are two buses attached to the internal register interface. The set of registers and their functionality is not dependent on the CPU interface chosen. The choice of interface is up to the system designer and should be made as a trade-off between board layout and speed requirements.

The two interfaces provided are a 4-pin serial interface (SI) and a 37-pin parallel interface (PI).

Register Space

Heathrow-III consists of several functional blocks. Some of these blocks (the ports and the MII Management Systems) are further divided into subblocks. All subblocks within a given block are clones with equal sets of registers.

Within each (sub) block an 8-bit address space exists, where each address accesses 32 bits of register data.

The blocks are identified with block IDs as listed in Table 15.

Table 15. Heathrow-III Blocks

Block ID	Subblocks	Slow	Functional Block	Short Name
1	4–15	Yes	Low Port	LPORT
2	0	Yes	Analyzer	ANALYZER
3	0-1	Yes	MII Management	MIIM
3	2	Yes	Memory initialization	MEMINIT
4	0–3, 4, 7	No	CPU Capture Buffer	CAPTURE
5	0	Yes	Frame Arbiter	ARBITER
6	0–3	Yes	High Port	HPORT
7	0	No	System Registers	SYSTEM

The Slow column shows a property of the block that will be explained in the ”Reading Slow Registers” on page 49.

For the ports, the subblock number maps to the ports such that subblock numbers 4–15 (Block 1) represents ports 0–11, and subblock numbers 0–3 (Block 6) represents ports 12–15. For MII Management, the subblock is either 0 or 1. The subblock number also applies to the CPU capture buffer, but not as a selector between sub modules, rather as an extension to the 8-bit address space. Refer to the ”CPU Packet Reception” on page 39.

The entire set of registers is listed in the ”Register Overview” on page 53.

The Serial Interface

The Serial Interface (SI) is a simple interface that operates as described in the “Serial Peripheral Interface” or “SPI” specification by Motorola (not to be confused with “SPI4” which is a high speed interface), running in mode CPHA = 0 and CPOL = 0. It consists of 4 signal lines: an input clock (SI_CLK), an enable signal (SI_nEN), and a data signal in each direction (SI_DI and SI_DO).

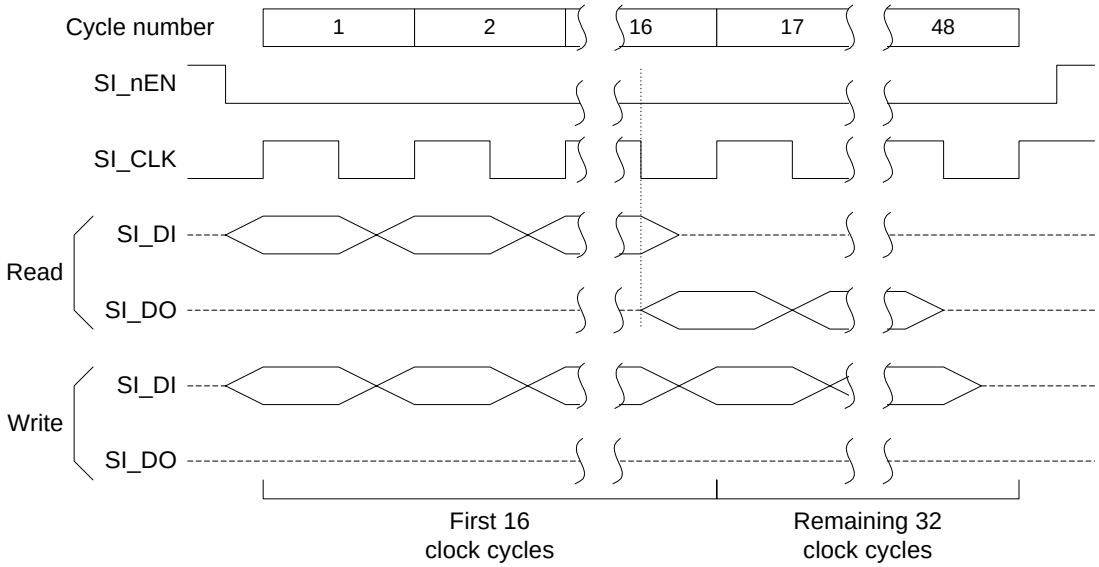


Figure 8. SI Communication

An external clock at a speed between 0 and 25 MHz clocks the interface. SI_nEN low starts an operation consisting of 48 clock cycles: 8 for command/block/subblock, 8 for address, and 32 for data. In case of a read operation, SI_DO is driven; otherwise it is kept tri-stated.

Table 16. Block Address Structure Format

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Block ID			Write	Subblock Number			
1	Address							
2	Data							
3	Data							
4	Data							
5	Data							

SI Clock Select

The internal timing of Heathrow-III means that the SI user must ensure at least a 600 ns delay from when the last bit of a read address is transmitted to when SI_CLK goes low again. This can be done in three ways:

1. Let the SI clock run at about 0.8 MHz or below (see Figure 9 and Figure 10)
2. Let the SI clock pause (at HIGH) after the last address is clocked out (see Figure 11)
3. Ask Heathrow-III to insert idle byte periods before the read data (see Figure 12)

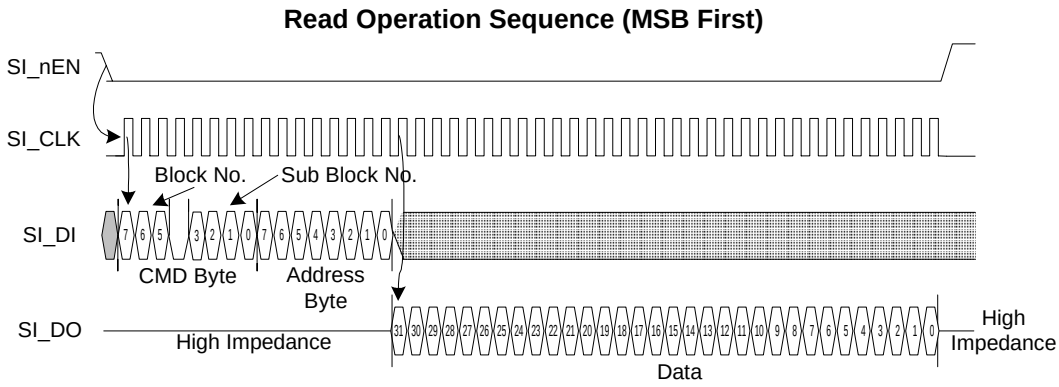


Figure 9. SI Read Operation Sequence (Low Clock)

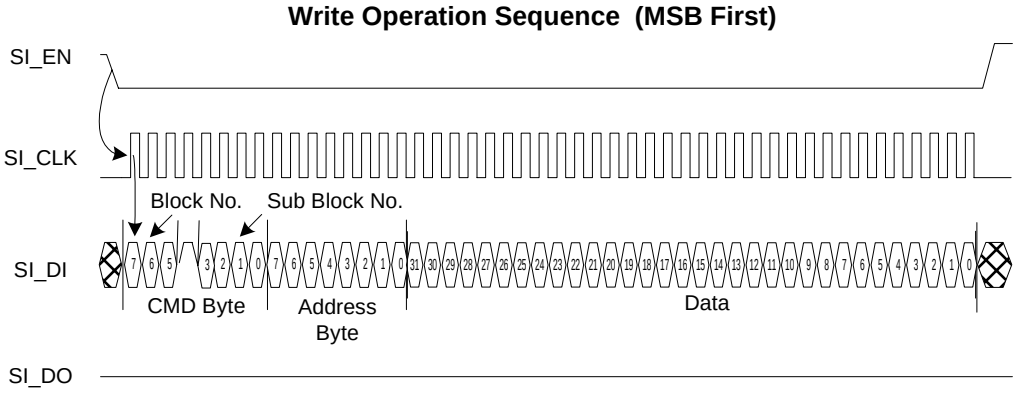


Figure 10. SI Write Operation Sequence (Low Clock)

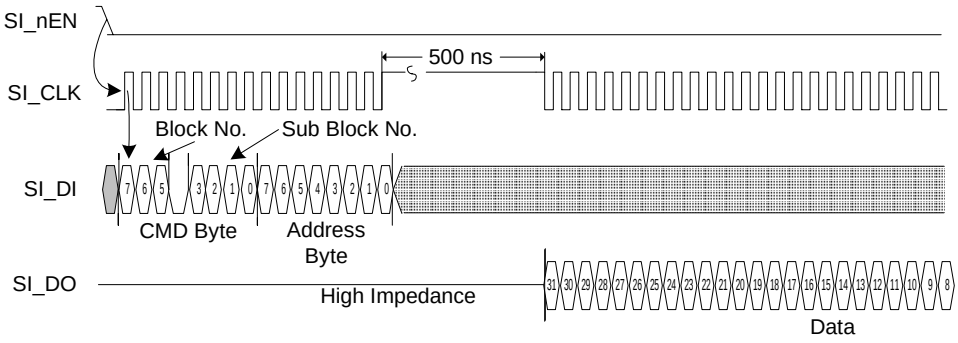


Figure 11. Figure 11: SI Read Operation With Clock Pause

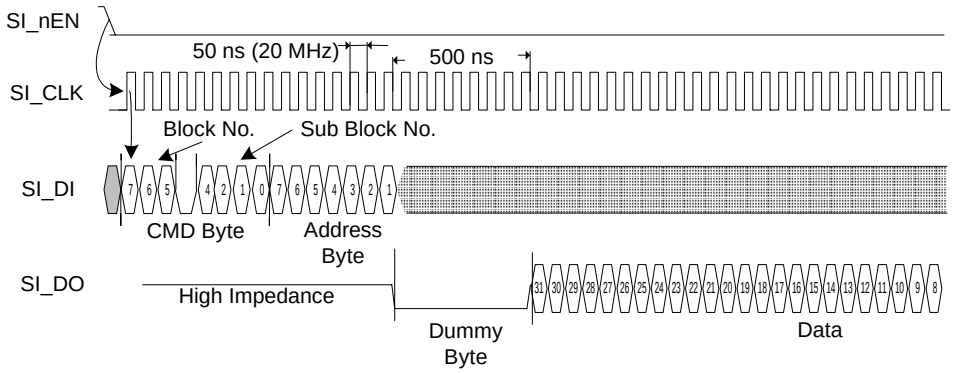


Figure 12. SI Read Operation With Dummy Byte

As an example of the third option, assume the SI clock is running at 10 MHz. This gives a clock cycle of 100 ns, so to ensure a 600 ns delay before data is read out, Heathrow-III must add padding bytes so that (8 x #pads + 1/2) x ClkCycle ≥ 600 ns. Hence, to run a 10 MHz SI, 1 byte of extra dummy data must be inserted in the read protocol sequence between command/address and data. Table 17 lists the clock limits for each configuration of dummy bytes.

Table 17. Number Of Dummy Bytes Versus Clock

Max. SI Clock	No. of Dummy Bytes
0.8 MHz	0
14 MHz	1
27 MHz	2
40 MHz	3

Write operations do not contain any padding bytes no matter what padding configuration has been chosen. Thus, no special care need be taken during the initial set-up of Heathrow-III for pad insertion; this can be done at full speed.

SI Configuration

By the use of certain system registers, it is possible to configure the SI protocol sequence. These possibilities exist:

- To select the byte order for the interface when sending 32 bit data words (endian selection)
- To select whether to transfer the most or the least significant bit within each byte first
- To select insertion of idle bytes before read data are transmitted

Table 18. SI Configuration Register

System Register	Description
CPUMODE	Selects endian mode and bit transfer order
SIPAD	Selects number of padding bytes

The Parallel Interface

For faster access to the registers, the Parallel Interface (PI) can be used. It consists of 16 address lines, 16 bidirectional data lines, and 5 control signals.

Table 19. PI Interface Signals

PI Signal	Direction	Width	Description
PI_Addr	I	16	Selects the block, sub_block and address (Refer to 3.4.3)
PI_Data	I/O	16	Driven by CPU at write, Heathrow-III at read
PI_nWR	I	1	Selects read (1) or write (0)
PI_nOE	I	1	Enable drive of the data bus from Heathrow-III
PI_nCS	I	1	Start a CPU operation
PI_nDone	OZ	1	Acknowledges an operations
PI_IRQ	O	1	A configurable interrupt signal for various events

The operations of the interface can be seen in Figure 13. To use the interface, do the following:

1. Lower nCS signal
2. Within 120 ns, Set up address, R/W select and data in case of write operation.
3. Wait until at least 140 ns from when nCS was lowered, or wait for nDone to fall
4. Store data from data bus in case of read operation
5. Raise nCS signal

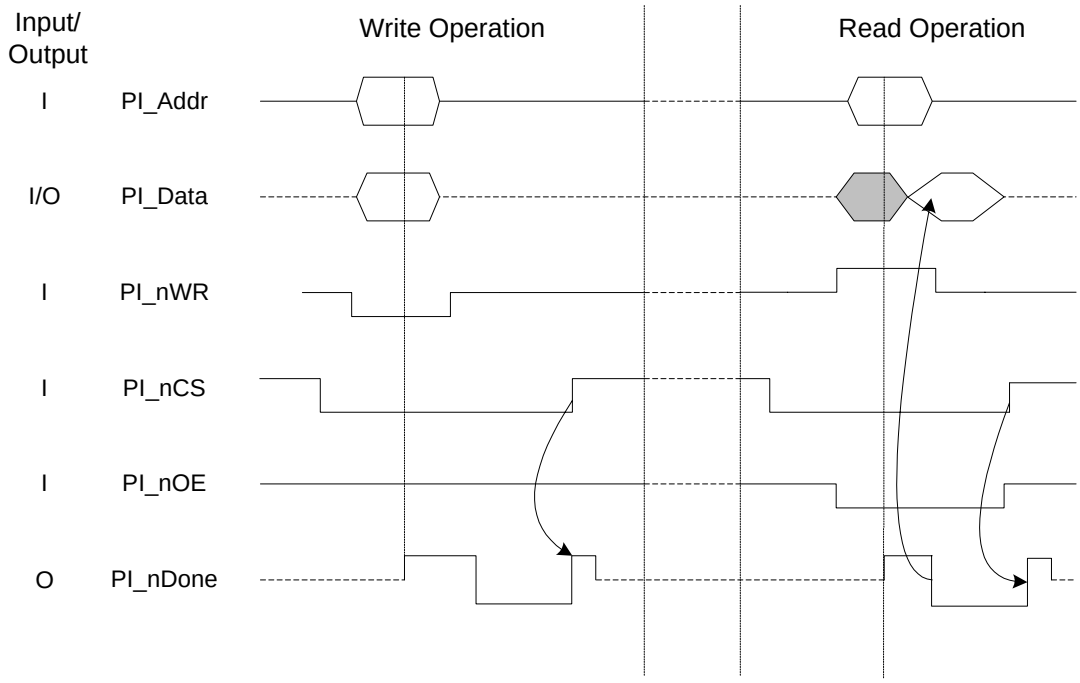


Figure 13. PI Communication

All inputs are latched a configurable amount of time after nCS falling. The delay is set in the CPUCTRL register, and is configurable from 10 to 130 ns with the default being 130 ns. nDone acknowledges the operation around 10 ns later. For precise timing information, refer to the AC specifications for the PI interface.

The nOE signal along with nCS directly control the output driver of the data bus.

As the registers internally in Heathrow-III are 32-bit organized, every register access must be performed in two consecutive CPU cycles. In a write operation, Heathrow-III does not update any target inside the chip until both 16-bit half words have been written, and in a read operation, Heathrow-III only accesses the internal 32-bit source when the first half word of a register is read.

Reading Slow Registers

Most of the registers in Heathrow-III have a larger access time than acceptable for a CPU bus cycle. The access time can be up to 500 ns, and therefore special action must be taken to read these.

Using the SLOWDATA Postponed Result

A way to cope with the slow read result is to make a dummy read of one of the half words from the target register, and then read the result from the SLOWDATA register. This feature must be enabled through the CPUCTRL register.

Example:

1. Read one of the half words of the register
2. Poll the SlowDone bit of CPUCTRL, or wait for SlowDone interrupt
3. Read one of the half words of the SLOWDATA register
4. Read the other half word of the SLOWDATA register

Extended Bus Cycle

It is also possible to extend the bus cycle, thereby postponing the nDone handshake until slow data is available. All registers are in this mode read like fast registers, but the nDone signal will not be activated until up to 600 ns after falling nCS. The extended bus cycle is default behavior, and can be disabled through the CPUCTRL register. Only the first half word of a slow register will have a long access time.

Interrupt Control

The PI_IRQ pin of Heathrow-III can be used to signal when a CPU should take action on two different events: When the SLOWDATA register has been filled, or when a packet is ready in the CPU packet receive buffer. The interrupt signal is of level type, and is cleared when the source condition inside Heathrow-III is removed by reading the SLOWDATA register, or by acknowledging a CPU packet.

Register Addressing

The Heathrow-III registers are mapped into the 16-bit address space of the PI as shown in Table 20.

Table 20. Register Mapping in PI Address Space

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Block ID			Subblock Number				Register address								WS

The WS bit selects the most or least significant 16 bits of the 32-bit word. In big endian mode, WS = 1 selects the least significant. In little endian mode, WS = 1 selects the most significant. For proper use, the first reading/writing of the 32-bit word must have WS = 0, and the second reading/writing must have WS = 1.

8-Bit Data Bus Width

The parallel interface also supports CPUs equipped with only an 8-bit interface. This is configured through the PIWIDTH register, which has the Heathrow-III address 0xe002. In this mode, all register accesses are split into four byte accesses. The byte select is not added to the address bus, so in effect a register is read through multiple accesses to the same address, and an 8-bit CPU should thus have its address lines 1..16 attached to Heathrow-III.

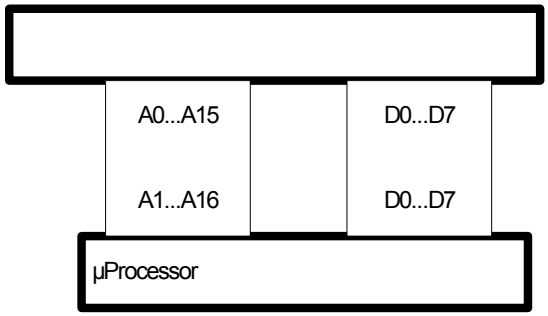


Figure 14. 8-Bit Data Bus Width

As an example, system register 0 is read (Big endian mode) as shown in Table 21.

Table 21. PI Bus 8-Bit Data Width Example

Access No.	Heathrow-III Address	CPU Bus address	Data
0	0xe000	0x1C000	Most significant byte
1	0xe000	0x1C001	Second most significant byte
2	0xe001	0x1C002	Second least significant byte
3	0xe001	0x1C003	Least significant byte

Minimum Software Requirements

The Heathrow-III device is almost fully working with its chip default configuration, and the minimum set of registers to setup for basic operation is listed in Table 22. For using TBI modes, statistics, aggregation, VLAN, flow control, MAC ageing, and so forth, refer to the ”Register Overview” on page 53 and the Heathrow-III software API.

Table 22. Minimum Register Set to Set Up

Register Name	Use For
MEMINIT	Initializing memories
MEMRES	Reading result from memory initialization
MACACCESS	Formatting MAC table
VLANACCESS	Formatting VLAN table
MACCONF	Setting the port mode according to PHY status
RECVMASK	Enabling frame forwarding from ports
MIIMCMD	Performing a MII management operation
MIIMDATA	Reading PHY read results from MII management operation

The mandatory operation for the software is split into an initialization sequence and a PHY polling operation. If the PHYs are running with fixed speed and duplex mode, the poll operation could be ignored, and the Heathrow-III ports can be set up to the desired mode as a part of the initialization sequence.

The very simple routines below are only for showing the minimum requirements, and cannot be used as the basis for a final software system. They are added here for introducing the use of the chip registers. The register accesses are notated in the format block.subblock.address.

Initialization Sequence

The following initialization sequence is REQUIRED to ensure proper operation of the switch.

```
/* Initialize memories */
for memid in (0..5,10..25){
     Write(MEMINIT.2.MEMINIT, 0x1010400 + memId);
     Sleep 1 ms;
}
Sleep 30 ms;
/* Read result from memory initialization */
for (memId=0; memId<=23; memId++){
     /* Initiate reading */
     Write(MEMINIT.2.MEMINIT, 0x20000 + memId);
     Sleep 1 ms;
     /* Read the result */
     result=Read(MEMINIT.2.MEMRES);
     if ((result&0x3)!=0x3){
         /* Memory initialization failed for Memory memId */
     }
}
/* Format memories */
Write(ANALYZER.0.MACACCESS, 5); /* CLEAR MAC TABLE command */
Write(ANALYZER.0.VLANACCESS, 3); /* CLEAR VLAN TABLE command */
Sleep 40 ms;
```

Port Mode Procedure

Execute this procedure on a regular basis, for updating the port mode according to the PHY state. This example is made for illustrating the basic requirements only, but must be expanded for a real software control program. Refer to the API for a fully detailed procedure.

```
for (portId=0; portId<=15; portId++) {
     /*Use MIIMCMD and MIIMDATA to retrieve current speed
       and link status from PHY attached to port <portId>
       Put the status into the <mode>
     */

  /* enable forwarding from a port, only if the port link is up */
  If (mode==DOWN) then
      Write(ANALYZER.0.RECVMASK, Read(ANALYZER.0.RECVMASK) &
~(1<<(portId+4)));
  else
      Write(ANALYZER.0.RECVMASK, Read(ANALYZER.0.RECVMASK) | (1<<(portId+4)));

  /* Set the port MAC to the current mode */
  Switch (mode) {
        Case DOWN: Write(PORT.portId.MACCONF, 0x20000030); break;
        Case 1GFULL: Write(PORT.portId.MACCONF, 0x100701C1); break;
        Case 100MFULL: Write(PORT.portId.MACCONF, 0x100504C2); break;
        Case 10MFULL: Write(PORT.portId.MACCONF, 0x100504C3); break;
        Case 100MHALF: Write(PORT.portId.MACCONF, 0x100104C2); break;
        Case 10MHALF: Write(PORT.portId.MACCONF, 0x100104C3); break;
        }
}
```

Register Overview

Table 23. System Block Registers (Block 7

Address	Register Name	Short Name
00h	CPU Transfer Mode	CPUMODE
01h	SI Padding	SIPAD
02h	PI BusWidth	PIWIDTH
13h	Semaphore Register	HWSEM
14h	Global Reset	GLORESET
18h	Chip Identification	CHIPID
24h	Time Compare Value	TIMECMP
2Ch	SlowData	SLOWDATA
30h	CPU Control	CPUCTRL
34h	General Purpose IO	GPIO

Table 24. MAC Block Registers (Block 1/6)

Address	Register Name	Short Name
00h	MAC Config	MACCONF
02h	Half Duplex Gaps	MACHDXGAP
04h	Flow Control Setup	FCCONF
08h	Flow Control SMAC High	FCMACHI
0Ch	Flow Control SMAC Low	FCMACLO
10h	Max Length	MAXLEN
11h	Shaper Setup	SHAPECONF
12h	Policer Setup	POLICECONF
13h	Multicast Storm Setup	MCSTORMCONF
14h	TBI Status Register	TBISTAT
18h	TBI Control Register	TBICTRL
19h	Advanced Port Mode Setup	ADVPORTM
24h	Transmit Modify Setup	TXMODIFY
25h	CFI Drop Counter	CFIDROP

Table 25. Shared FIFO Block Registers (Block 1/6)

Address	Register Name	Short Name
C0h	CPU Transmit DATA	CPUTXDAT
C4h	MISC Control Register	MISCFIFO
CCh	Pool Control Register	POOLCFG
DCh	Drop Control Register	DROPCFG
C8h	Misc Status	MISCSTAT
D8h	Free RAM Counter	FREEPOOL

Table 26. Categorizer Block Registers (Block 1/6)

Address	Register Name	Short Name
60h	Categorizer Config	CATCONF
64h	Categorizer Map Tag	CATTAG
68h	EtherType Register	CATETHT
6Ch	DSAP Register	CATDSAP
70h	IP Protocol Register	CATIPPRT
74h	Categorizer Priorities	CATPRIO

Table 26. Categorizer Block Registers (Block 1/6) (cont'd)

Address	Register Name	Short Name
78h	DS Mapping Register High	CATDSMAPH
79h	DS Mapping Register Low	CATDSMAPL
7Ch	PVID Register	CATPVID
80h	TCP/UDP Port Register 1	CATPORT1
84h	TCP/UDP Port Register 2	CATPORT2
88h	TCP/UDP Port Register 3	CATPORT3
8Ch	TCP/UDP Port Register 4	CATPORT4
90h	TCP/UDP Port Register 5	CATPORT5

Table 27. Statistics Block Registers (Block 1/6)

Address	Register Name	Short Name
37h	Rx Total Bad Packets	RXBADPKT
39h	Rx Control Packets	RXCTRL
44h	Tx Total Error Packets	TXERR

Table 28. Detailed Counters Block Registers (Block 1/6)

Address	Register Name	Short Name
50h	Rx Octets	C_RXOCT
51h	Tx Octets	C_TXOCT
A0h	Rx Drops	C_RXDROP
A1h	Rx Packets	C_RXPKT
A2h	Rx Broadcasts	C_RXBC
A3h	Rx Multicasts	C_RXMC
A4h	Rx CRC/ALIGN	C_RXCRC
A5h	Rx Undersize	C_RXSHT
A6h	Rx Oversize	C_RXLONG
A7h	Rx Fragments	C_RXFRAG
A8h	Rx Jabbers	C_RXJAB
A9h	Rx 64 Bytes	C_RX64
AAh	Rx 65-127 Bytes	C_RX65
ABh	Rx 128-255 Bytes	C_RX128
ACh	Rx 256-511 Bytes	C_RX256

Table 28. Detailed Counters Block Registers (Block 1/6) (cont'd)

Address	Register Name	Short Name
ADh	Rx 512-1023 Bytes	C_RX512
AEh	Rx 1024-long Bytes	C_RX1024
AFh	Tx Drops	C_TXDROP
B0h	Tx Packets	C_TXPKT
B1h	Tx Broadcasts	C_TXBC
B2h	Tx Multicasts	C_TXMC
B3h	Tx Collisions	C_TXCOL
B4h	Tx 64 Bytes	C_TX64
B5h	Tx 65-127 Bytes	C_TX65
B6h	Tx 128-255 Bytes	C_TX128
B7h	Tx 256-511 Bytes	C_TX256
B8h	Tx 512-1023 Bytes	C_TX512
B9h	Tx 1024-long Bytes	C_TX1024
BAh	Tx FIFO Drops	C_TXOVFL
BBh	Rx High Priority Frames	C_RXHP
BCh	Rx Low Priority Frames	C_RXLP
BDh	Tx High Priority Frames	C_TXHP
BEh	Tx Low Priority Frames	C_TXLP

Table 29. MII Management Bus Block Registers (Block 3)

Address	Register Name	Short Name
00h	MII-M Status	MIIMSTAT
01h	MII-M Command	MIIMCMD
02h	MII-M Return Data	MIIMDATA
03h	MII-M Prescaler	MIIMPRES
04h	MII-M Scan setup	MIIMSCAN
05h	MII-M Scan Results	MIIMSRES

Table 30. Memory Initialization Block Registers (Block 3)

Address	Register Name	Short Name
00h	Initialize	MEMINIT
01h	Read Result	MEMRES

Table 31. Frame Arbiter Block Registers (Block 5)

Address	Register Name	Short Name
0Ch	Arbiter Empty	ARBEMPTY
0Eh	Arbiter Discard	ARBDISC

Table 32. CPU Capture Block Registers (Block 4)

Address	Register Name	Short Name
00h	Read Pointer	CAPREADP
03h	Write Pointer	CAPWRP
FFh	Full Reset	CAPRST

Table 33. Frame Analyzer Block Registers (Block 2)

Address	Register Name	Short
03h	Advanced Learning Setup	ADVLEARN
04h	IP Multicast Flood Mask	IFLODMSK
05h	VLAN Source Port Mask	VLANMASK
08h	Station Move Logger	ANMOVED
09h	Ageing Filter	ANAGEFIL
0Ah	Event Sticky Bits	ANEVENTS
0Bh	Event Sticky Mask	ANCNTMSK
0Ch	Event Sticky Counter	ANCNTVAL
0Dh	Learn Mask	LERNMASK
0Eh	Unicast Flood Mask	UFLODMSK
0Fh	Multicast Flood Mask	MFLODMSK
10h	Receive Mask	RECVMASK
20h	Aggregation Mode	AGGRCNTL
30h - 3Fh	Aggregation Masks	AGGRMSKS
40h - 7Fh	Destination Port Masks	DSTMASKS
80h - 97h	Source Port Masks	SRCMASKS
B0h	Mac Table Command	MACACCES
C0h	Mac Table Index	MACTINDX
06h	Mac Address High	MACHDATA
07h	Mac Address Low	MACLDATA

Table 33. Frame Analyzer Block Registers (Block 2) (cont'd)

Address	Register Name	Short
D0h	VLAN Table Command	VLANACES
E0h	VLAN Table Index	VLANTINDX
F0h	Analyzer Config Register	AGENCNTL

Register Description

Unspecified fields in the registers must be written zero, and can be ignored on read. The mode column in the register tables in the following sections shows the access for the register:

R/W Read and write

R/O Read only

W/O Write only (read dummy)

C/R Clear on read (Sticky status bit)

System Block Registers (Block 7)

Table 34. CPU Transfer Mode - CPUMODE (Address 00h)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
3	Endian	R/W	Configures the byte order mode on CPU interface: SI = MSByte first PI = MSHalfword first (A0=0)	1
0	BitDone	R/W	Configures the SI and PI interface as: SI = MSBit first in each byte PI = nDONE active LOW	1
Note: Controls the data transfer mode for the CPU interfaces. In order for the write to work independently of the current transfer mode, BitDone must be mirrored to bits 7, 8, 15, 16, 23, 24, and 31 - and Endian must be mirrored to bits 4, 11, 12, 19, 20, 27, and 28. In this respect, the possible values for this register are: 0x00000000 Little endian, LSB first / nDONE active HIGH 0x18181818 Big endian, LSB first / nDONE active HIGH 0x81818181 Little endian, MSB first / nDONE active LOW 0x99999999 Big endian, MSB first / nDONE active LOW				

Table 35. SI Padding - SIPAD (Address 01h)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
2:0	SI Padding	R/W	Cycle count	0
Note: Number of byte cycles (0–7) during SI read between command and the first byte read. Used to assure 600 ns delay, and must be set according to the SI clock frequency.				

Table 36. PI BusWidth - PIWIDTH (Address 02h)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
0	HalfWidth mode	W/O	Selects bus width: 0 = Bus width is 16-bit 1 = Bus width is 8-bit	0
Note: Regardless of the current bus width, a single 8 or 16 bit access to this register will be effective. This register is accessible only through the PI interface itself.				

Table 37. Semaphore Register - HWSEM (Address 13h)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
0	Semaphore Register	R/W	This field behaves as a semaphore. Only the first read will return 1. Any further reads will return 0. When written 1, the next read will return 1.	0
Note: The semaphore can be useful when using more the one CPU interface (PI and SI in the same design).				

Table 38. Global Reset - GLORESET (Address 14h)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31:0	Global Reset	W/O	Do full reset	0
Note: This register is used to fully reset Heathrow-III as if reset externally. Only value 0xffffffff applies and should be followed by a delay of at least 125 µs, before any access is made to the chip.				

Table 39. Chip Identification - CHIPID (Address 18h)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31:28	REVISION_NUMBER	R/O	Revision ID: 0000 = First revision 0001 = Second revision	0
27:12	PART_NUMBER	R/O	BCD Encoded Part Number for this device	7302h
11:1	MANUFACTURER_ID	R/O	The unique identifier for the chip vendor	74h
0	RESERVED	R/O	Always read 1	1
Note: This register returns the same value as the JTAG Identifier				

Table 40. Time Compare Value - TIMECMP (Address 24h)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
25:0	Time Compare Value	R/W	Time value for frame age calculation	3B9ACA0h
Note: Sets the time determining how long a frame can be queued in Heathrow-III before it is regarded as being too old, and dropped. ageing occurs after 32 ns times the value of this register. Default value equals 2 seconds.				

Table 41. SlowData - SLOWDATA (Address 2Ch)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31:0	SlowData	R/O	This is the read data from slow registers	0
Note: When read, the SlowDone bit in Interrupt Control Register is cleared.				

Table 42. CPU Control - CPUCTRL (Address 30h)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
11:8	PI Wait	R/W	Number of clock cycles to wait after nCS seen low, before other inputs are latched. The unit is 8 ns, thereby allowing the input signals to be unstable for up to 120 ns more than the maximum speed for the interface. The field should be lowered to match what the PI master can deliver.	Fh
7	Learn Truncate	R/W	Captured frames for learning will be truncated to 64 bytes.	0

Table 42. CPU Control - CPUCTRL (Address 30h)
Block 7 Subblock 0 (cont'd)

Bit	Name	Mode	Description	Default
5	ExtCpu Use Slow	R/W	1 = Use slow mode for slow registers when accessed through PI, splitting a read operation into two phases. 0 = Use extended bus cycle, where the nDone signal will be kept high until read data is ready.	0
4	SlowDone	R/O	Set when a slow register operation is complete internally. Cleared when the SLOWDATA register is read, or when a new slow data operation is initiated.	0
3	CPU Rx Frame Ready	R/O	Set as long as a packet is ready in the CPU capture buffer. This bit is a mirror of the Frame Ready bit in the CAPWRP register.	0
2	Inverse INTR Polarity	R/W	Set the interrupt signal to be active low.	0
1	Int Enable Packet	R/W	Enables interrupt when a CPU Rx frame is ready.	0
0	Int Enable Slow	R/W	Enables interrupt when a slow register read or write is complete.	0

Table 43. General Purpose IO - GPIO (Address 34h)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
9	Output Enable 1	R/W	GPIO1 will be of type output	0
8	Output Enable 2	R/W	GPIO2 will be of type output	0
7	Output Enable 3	R/W	GPIO3 will be of type output	0
6	Output Enable 4	R/W	GPIO4 will be of type output	0
4	Data Value 1	R/W	The value seen on the GPIO1 pins when read, and the value to drive when written	1
3	Data Value 2	R/W	The value seen on the GPIO2 pins when read, and the value to drive when written	1
2	Data Value 3	R/W	The value seen on the GPIO3 pins when read, and the value to drive when written	1
1	Data Value 4	R/W	The value seen on the GPIO4 pins when read, and the value to drive when written	1
Note: When the GPIO pins are set into output mode, the value read will match the value written.				

MAC Block Registers (Block 1/6)

Table 44. MAC Config - MACCONF (Address 00h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
29	Port Reset	R/W	The port is held reset while this bit is set. Only the Shared FIFO block registers and the Shared FIFO drop counters (C_RXDROP and C_TXOVFL) will be reset. All other port configurations will be kept	1
28	Tx_en	R/W	Enable frame transmission.	0
27	Seed Load	R/W	Load seed for back off algorithm.	0
26:19	Back Off Seed	R/W	Value used to seed the randomizer used for the back off algorithm. To load a seed into the randomizer, a transmit clock must be present, and the transmitter must be idle. The Seed Load must be asserted for at least 1 µs, and the Back Off Seed field must not be changed simultaneously with deassertion of Seed Load.	0
18	Full Duplex	R/W	Enable full duplex mode.	1
17	Giga Mode	R/W	Set MAC to gigabit mode.	0
16	Rx_en	R/W	Enable frame receive.	0
15	RESERVED	R/W	Must be 0.	0
14	VLAN Awareness	R/W	Allow tagged frames to be max_length+4 bytes long.	0
10:6	Tx IPG	R/W	The interframe gap between two consecutive transmitted frames. The unit is line clock cycle, and an offset of 5 cycles is added to value of this register. Recommended: 10/100 = 19 1G/TBI = 7	0
5	Rx Reset	R/W	The receive domain is held reset while this bit is set.	1
4	Tx Reset	R/W	The transmit domain is held reset while this bit is set.	1
3	Local Rx Clock	R/W	If set - use transmitter clock for rx domain. Used in loopback tests only.	0
2:0	Transmit Clock Select	R/W	000 = No transmit clock 001 = 125 MHz (RGMII-1000/TBI) 010 = 25 MHz (RGMII-100) 011 = 2.5 MHz (RGMII-10) 100 = External MII RxClk (Test only)	0
Notes: This register configures most MAC functions. When changing the clock or duplex select fields, the register must be written twice. Once with all three reset flags asserted, once without.				

Table 45. Half Duplex Gaps - MACHDXGAP (Address 02h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
11:8	LCOLPOS	R/W	Late Collision Position. Adjust the border between a collision and a late collision in steps of 1 byte. According to IEEE 802.3 section 21.3 this border is allowed to be on data byte 56 (counting frame data from 1), that is, a frame experiencing a collision on data byte 55 will always be retransmitted, and on byte 57 will never be retransmitted. Using LCOLPOS = 2, the border will be in this range. For each higher LCOLPOS value, the border is moved 1 byte higher. The range of the field is 0–15.	2
7:4	IFG2	R/W	Second part of half duplex RX to TX Inter Frame Gap. On RGMII, RX-to-TX_IFG = 4.5 + (IFG1 + IFG2) / 2 byte. Within IFG2, transitions on CRS are ignored. The unit is one line clock cycle.	Ah
3:0	IFG1	R/W	First part of half duplex RX to TX Inter Frame Gap. The sum of IFG1 and IFG2 times the RX to TX IFG. Within IFG1, this timing will be restarted if CRS has multiple high-low transitions, that is, is noisy. The unit is one line clock cycle.	7

Table 46. Flow Control Setup - FCCONF (Address 04h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
17	Zero Pause Enable	R/W	If set, a zero delay pause frame is transmitted when pause condition is left	0
16	Flow Control Obey	R/W	Obey pause control frames	0
15:0	Pause Value	R/W	This value is inserted into the generated pause frames	0
Note: This register controls the flow control setup. The frames will be generated by the conditions set up in POOLCFG and/or POLICECONF.				

Table 47. Flow Control SMAC High - FCMACHI (Address 08h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Flow Control SMAC High	R/W	These are the upper 3 bytes inserted in the generated flow control frames	0

Table 48. Flow Control SMAC Low - FCMACLO (Address 0Ch)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Flow Control SMAC Low	R/W	These are the lower 3 bytes inserted in the generated flow control frames	0

Table 49. Max Length - MAXLEN (Address 10h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
16	Type/Len Check	R/W	Enable check of valid type/length field. If enabled, ingress frames can be dropped due to inrange/outrange errors.	0
15:0	Max Length	R/W	Frame will be ”long” (dropped and counted in “longs” counter) if frame length exceeds this limit. The internal limit is 12.2 kbytes. See VLAN Awareness in MACCONF for tagged length check.	5EEh

Table 50. Shaper Setup - SHAPECONF (Address 11h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31	Drop Mode	R/W	Drop egress frames when the bucket is full.	0
30	Hold Mode	R/W	Hold back frame transmission when bucket is full.	0
29	Reset	R/W	Reset filling in shaper. Filling is kept reset while this bit is set.	0
24:16	Bucket Threshold	R/W	Bucket is filled when the fill level is above this number of 512 byte slices.	0
11:0	Data Rate	R/W	The bucket is emptied at this rate. Rate unit is speed dependent: 1G = 244 kb/s 100M = 48.8 kb/s 10M = 4.88 kb/s	0
Note: The C_TXOVFL counter is counting the number of frames dropped due to this feature. If neither bit 30 nor 31 is set, the shaper has no effect on the flow				

Table 51. Policer Setup - POLICECONF (Address 12h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31	Drop Mode	R/W	Drop ingress frames when the bucket is full.	0
30	Flow Control Mode	R/W	Generate flow control frames when bucket is full.	0
29	Reset	R/W	Reset filling in policer. Filling is kept reset while this bit is set.	0
24:16	Bucket Threshold	R/W	Bucket is filled when the fill level is above this number of 512 byte slices.	0
11:0	Data Rate	R/W	The bucket is emptied at this rate. Rate unit is speed dependent: 1G = 244 kb/s 100M = 48.8 kb/s 10M = 4.88 kb/s	0
Note: The flow control frames are generated as configured in the flow control configuration registers, and the dropped frames are counted by the C_RXDROP counter. If neither bit 30 nor 31 is set, the policer has no effect on the flow.				

Table 52. Multicast Storm Setup - MCSTORMCONF (Address 13h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31	Enable	R/W	Drop ingress frames when the bucket is full.	0
29	Reset	R/W	Reset filling in multicast storm bucket. Filling is kept reset while this bit is set.	0
24:16	Bucket Threshold	R/W	Bucket is filled when the fill level is above this number of 512 byte slices.	0
11:0	Data Rate	R/W	The bucket is emptied at this rate. Rate unit is speed dependent: 1G = 244 kb/s 100M = 48.8 kb/s 10M = 4.88 kb/s	0
Note: The dropped frames are counted by the C_RXDROP counter. If bit 31 is zero, storm control has no effect on the flow.				

Table 53. TBI Status Register - TBISTAT (Address 14h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:24	Link down counter	C/R	Counts number of link down events (until 255)	0

Table 53. TBI Status Register - TBISTAT (Address 14h)
Block 1/6 Subblock 4-15/0-3 (cont'd)

Bit	Name	Mode	Description	Default
20	Link Status	R/O	Zero if link has been down since last read	0
19:18	PCS State	R/O	Current state of the PCS: 00 = IDLE 01 = CONFIG 11 = DATA	0
17	ANEG Priority Resolution	R/O	This flag will be set one link timer tick before the auto negotiation process is complete. It can be used for validating the negotiated abilities after ANEG to close down the data path in case of mismatch. The data path must be disabled through the RX/TX enable flags in MACCONF.	0
16	ANEG Complete	R/O	The auto negotiation process has completed.	0
15:0	Ability	R/O	ANEG Partner advertisement word.	0
Note: This register must be polled to ensure proper auto negotiation operation for TBI ports. Within 10 ms after ANEG Complete is asserted, the ability word must be matched against own abilities, or the line must be closed. Refer to the Heathrow-III software API for further details.				

Table 54. TBI Control Register - TBICTRL (Address 18h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31	Write Strobe	R/W	This bit must be set to activate the configuration in this register	0
23	Signal Detect Polarity	R/W	The level of the CRS pin when the link is valid	0
22	Enable signal detect	R/W	When enabled, the CRS is used to validate the link	0
19	Debug Link Timer	R/W	Enable 2 µs timer instead of normal 10 ms	0
18	Internal Loop Back	R/W	If enabled TBI Tx data will be looped back into TBI receive	0
17	ANEG Enable	R/W	Enable the auto negotiation process in TBI	0
16	ANEG Restart	R/W	Restart the auto negotiation process. It is not necessary to clear the flag after it has been set	0
15:0	Advertisement Word	R/W	The auto negotiation advertised	0
Note: This register must be written twice to activate a new configuration. Once with the strobe bit cleared, once with it asserted.				

Table 55. Advanced Port Mode Setup - ADVPORTM (Address 19h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
6	Loopback	R/W	Enable internal loopback. All egress frames will be echoed through the ingress path.	0
5	Skip ERR XOR	R/W	In RGMII, the error signal will *not* be XORed with TXEN/ RXDV. Use only for older RGMII PHYs.	0
4	Invert GTX	R/W	Set if GTX clock is to be inverted. Try toggling this bit when having problems with PHY Transmit.	0
3	Halt GTX	R/W	Set if GTX is to be kept silent. Use this in MII modes for power save.	0
0	TBI Enable	R/W	Enable the TBI layer for this port.	0

Table 56. Transmit Modify Setup - TXMODIFY (Address 24h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
15:4	Untagged vID	R/W	Frames with this vID will be transmitted untagged	0
3	Untagged vID Enable	R/W	If set, frame in a specific VLAN will not be tagged, even if port is set up for tagging	0
2	Update CRC Tag	R/W	Recalculate CRC after tag insertion/removal	1
1	Update CRC CPU	R/W	Recalculate CRC for CPU transmit frames	0
0	Insert TAG	R/W	If set, frames will be transmitted with VLAN tags	0

Table 57. CFI Drop Counter - CFIDROP (Address 25h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:0	CFI Drops Counter	R/O	Counts the number of CFI marked frames dropped before transmit on this port	0
Note: If a port is set up to transmit untagged frames, CFI marked frames will be dropped.				

Shared FIFO Block Registers (Block 1/6)

Table 58. CPU Transmit DATA - CPUTXDAT (Address C0h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:0	CPU Transmit DATA	W/O	Write 4 bytes of Tx Data. An even number of writes MUST be performed.	0
Note: This register is used by the CPU to transmit frames. The first two words must hold a header for the frame, which is: word1 = length in upper 16 bit, zero in lower word2 = 0x00000254 (mandatory signature)				

Table 59. MISC Control Register - MISCFIFO (Address C4h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
1	Rewind CPU Tx	W/O	Cancel the CPU Tx Data that have been written through the Transmit Data register	0
0	CPU Tx	W/O	Transmit the frame data written through the Transmit Data register	0

Table 60. Pool Control Register - POOLCFG (Address CCh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31	Use Total Count	R/W	If set, the total size (ingress + egress) of allocated memory will be used when referencing threshold limits. This feature is only added for special applications, and should in general not be used.	0
30	Track Pool Usage	R/W	When set, the freepool register will report the largest memory usage since last read instead of current.	0
29:24	Egress Low	R/W	Stop internal flow control towards ingress ports when below this watermark.	30h
21:16	Egress High	R/W	Start internal flow control towards ingress ports when above this watermark.	30h
14	Ingress Protection Method	R/W	Protection for overflow in ingress queues. 0 = by disobeying egress status 1 = by issuing pause frames to the MAC	0
13:8	Ingress Low	R/W	Stop pause generation or resume obeying egress status when below this watermark.	2Ch

Table 60. Pool Control Register - POOLCFG (Address CCh)
Block 1/6 Subblock 4-15/0-3 (cont'd)

Bit	Name	Mode	Description	Default
5:0	Ingress High	R/W	Start pause generation or stop obeying egress status when above this watermark.	2Ch
Note: All the values are in 256-byte slices.				

Table 61. Drop Control Register - DROPCFG (Address DCh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:30	Early Transmit Level	R/W	Allow MAC to initiate transmit before the whole packet has been received from the ingress device, if the amount of egress data is less than this level. The unit is 2 kB.	0
29:24	Egress Drop Low	R/W	Drop low priority egress frames when above this watermark.	Ah
21:16	Egress Drop All	R/W	Drop all egress frames when above this watermark.	32h
13:8	Ingress Drop Low	R/W	Drop low priority ingress frames when above this watermark.	Ah
5:0	Ingress Drop All	R/W	Drop all ingress frames from MAC when above this watermark.	32h
Note: All the values are in 256-byte slices.				

Table 62. Misc Status - MISCSTAT (Address C8h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
8	CPU Tx Data Pending	R/O	Indicates that Tx data recently written to CPUTXDAT have not yet been transferred to the Tx queue. No further writes to CPUTXDAT must take place before this bit is clear.	0
7	CPU Tx Data Overflow	R/O	Indicates that additional TX data was written by the CPU before the "data pending" bit above was clear. When this flag is detected, the rewind command must be issued.	0

Table 63. Free RAM Counter - FREEPOOL (Address D8h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
21:16	FreeCount	R/O	Number of free 256-byte slices of RAM in shared FIFO	3Bh
13:8	Ingress Used	R/O	Number of 256-byte slices used for ingress data	3

**Table 63. Free RAM Counter - FREEPOOL (Address D8h)
Block 1/6 Subblock 4-15/0-3 (cont'd)**

Bit	Name	Mode	Description	Default
5:0	Egress Used	R/O	Number of 256-byte slices used for egress data	2
Note: The default values for the use counters are above zero, due to a minimum allocation for each queue of 1 slice. None of the three fields in this register can therefore hit more the 63.				

Categorizer Block Registers (Block 1/6)

The registers in this section mainly control the prioritization of incoming frames. The function of each of the registers cannot be disabled, so a network-unused value must be applied to a field if the function is not wanted.

**Table 64. Categorizer Config - CATCONF (Address 60h)
Block 1/6 Subblock 4-15/0-3**

Bit	Name	Mode	Description	Default
31	Tag Only	R/W	If set, the priority of the tagged frames will be calculated from the TCI priority within the frame, and any higher layer information will be disregarded. Untagged frames will get the priority FS2.	0
30	Ignore TCI	R/W	Always report the PvID for incoming frames instead of taking it from the tag field within frame.	1
29	Ignore CTRL	R/W	Forward MAC Control frames. Through an entry in the MAC table, they can also be redirected to the capture buffer.	0
26	DS Only	R/W	If set, the priority will be based on the DS field for all IP frames. If cleared, only IP frames with protocol and port match will be based on DS. If DS field is not used, the priority will be FS7.	0
25	Keep Tag	R/W	The frame tag will not be removed from the frame when forwarding. This bit must be set when operating as a VLAN unaware switch, so that a tag field will be left untouched.	1
23	Drop Untagged	R/W	If set, all untagged or priority-tagged frames received on this port will be dropped (except BPDUs).	0
22	IGMP Capture	R/W	Recognize IGMP frames and redirect them to CPU.	0
21	BPDU Capture	R/W	Recognize BPDUs and redirect them to CPU. If this flag is not set, BPDU's will be forwarded as any other multicast frame.	1
20	Enable IPMC Flood Mask	R/W	When set, IP multicast frames outside 224.0.0.x (the data block) with unknown DMAC will be forwarded based on the IP multicast flooding mask.	0
19	ARP BC Capture	R/W	Recognize ARP broadcasts and copy them to CPU.	0
18	Drop NullMac	R/W	Drop packets with zero source or destination MAC address.	0

Table 64. Categorizer Config - CATCONF (Address 60h)
Block 1/6 Subblock 4-15/0-3 (cont'd)

Bit	Name	Mode	Description	Default
17	IPMC Ctrl snoop	R/W	Recognize IP multicast frames in DIP range 224.0.0.x, and copy them to the CPU capture buffer.	0
15	IP BC Capture	R/W	Recognize IP broadcasts and copy them to CPU.	0

Table 65. Categorizer Map Tag - CATTAG (Address 64h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
7	Categorizer Map Tag	R/W	Internal priority for tag priority no. 7	1
6	Categorizer Map Tag	R/W	Internal priority for tag priority no. 6	1
5	Categorizer Map Tag	R/W	Internal priority for tag priority no. 5	1
4	Categorizer Map Tag	R/W	Internal priority for tag priority no. 4	1
3	Categorizer Map Tag	R/W	Internal priority for tag priority no. 3	1
2	Categorizer Map Tag	R/W	Internal priority for tag priority no. 2	1
1	Categorizer Map Tag	R/W	Internal priority for tag priority no. 1	1
0	Categorizer Map Tag	R/W	Internal priority for tag priority no. 0	1
Note: If the priority is to be based on the tag field, this register maps the 8 possible priorities to the internal low/high queues.				

Table 66. EtherType Register - CATETHT (Address 68h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
15:0	EtherType Register	R/W	EtherType value for prioritization	800h
Note: Refer to the Frame Priority Determination in the Functional Description section.				

Table 67. DSAP Register - CATDSAP (Address 6Ch)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
7:0	DSAP Register	R/W	A DSAP value for prioritization	AAh
Note: Refer to the Frame Priority Determination in the Functional Description section.				

Table 68. IP Protocol Register - CATIPPRT (Address 70h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
7:0	IP Protocol Register	R/W	An IP protocol for prioritization	6
Note: Refer to the Frame Priority Determination in the Functional Description section.				

Table 69. Categorizer Priorities - CATPRIO (Address 74h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
7	FS8	R/W	Non-IP frame priority	1
6	FS7	R/W	TCP/UDP frames with unconfigured port number in the Categorizer	1
5	FS6	R/W	Non-IP frames with configured EtherType	1
4	FS5	R/W	802.2 frames, non-SNAP and non-DSAP match	1
3	FS4	R/W	802.2 frames, non-SNAP with DSAP match	1
2	---	R/W	Unused	1
1	FS2	R/W	Untagged frames when only using priority field in tag ID	1
0	FS1	R/W	Tagged frames with CFI field =1	1
Note: This register maps all the frame classifications into high or low priority. Refer to the flowchart in the Frame Priority Diagram, found in the Functional Description section.				

Table 70. DS Mapping Register High - CATDSMAPH (Address 78h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:0	DS Mapping Register High	R/W	This mask defined the priority for DSCP 63,62,...32	FFFFFF FFh

Table 71. DS Mapping Register Low - CATDSMAPL (Address 79h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:0	DS Mapping Register Low	R/W	This mask defined the priority for DSCP 31,30,...,0	FFFFFF FFh

Table 72. PVID Register - CATPVID (Address 7Ch)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:20	Port vID	R/W	Default vID for untagged frames, classified as low priority	0
19	Port CFI Field	R/W	Default CFI bit for untagged frames, classified as low priority	0
18:16	Port VLAN Priority	R/W	Default priority for untagged frames, classified as low priority	0
15:4	Port vID	R/W	Default vID for untagged frames, classified as high priority	0
3	Port CFI Field	R/W	Default CFI bit for untagged frames, classified as high priority	0
2:0	Port VLAN Priority	R/W	Default priority for untagged frames, classified as high priority	0
Note: If bit 30 of CATCONF is set, all frames will get the PvID VLAN info as forwarding info.				

Table 73. TCP/UDP Port Register 1 - CATPORT1 (Address 80h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:16	Port 1	R/W	When this port number is matched in an incoming frame, priority can optionally be based on the frame's DS code point	50h
15:0	Port 2	R/W	When this port number is matched in an incoming frame, priority can optionally be based on the frame's DS code point	14h

Table 74. TCP/UDP Port Register 2 - CATPORT2 (Address 84h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:16	Port 3	R/W	When this port number is matched in an incoming frame, priority can optionally be based on the frame's DS code point	50h
15:0	Port 4	R/W	When this port number is matched in an incoming frame, priority can optionally be based on the frame's DS code point	14h

Table 75. TCP/UDP Port Register 3 - CATPORT3 (Address 88h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:16	Port 5	R/W	When this port number is matched in an incoming frame, priority can optionally be based on the frame's DS code point	50h
15:0	Port 6	R/W	When this port number is matched in an incoming frame, priority can optionally be based on the frame's DS code point	14h

Table 76. TCP/UDP Port Register 4 - CATPORT4 (Address 8Ch)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:16	Port 7	R/W	When this port number is matched in an incoming frame, priority can optionally be based on the frame's DS code point	50h
15:0	Port 8	R/W	When this port number is matched in an incoming frame, priority can optionally be based on the frame's DS code point	14h

Table 77. TCP/UDP Port Register 5 - CATPORT5 (Address 90h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:16	Port 9	R/W	When this port number is matched in an incoming frame, priority can optionally be based on the frame's DS code point	50h
15:0	Port 10	R/W	When this port number is matched in an incoming frame, priority can optionally be based on the frame's DS code point	14h

Statistics Block Registers (Block 1/6)

Table 78. Rx Total Bad Packets - RXBADPKT (Address 37h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx Total Bad Packets	R/O	Bad packets only	0

Table 79. Rx Control Packets - RXCTRL (Address 39h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx Control Packets	R/O	Number of MAC control frames received	0

Table 80. Tx Total Error Packets - TXERR (Address 44h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx Total Error Packets	R/O	Number of bad packets transmitted	0

Detailed Counters Block Registers (Block 1/6)

The counters in this block are for RMON-II counter support. They are cleared by writing the C_RXDROP register with any value. All counters will wrap around at their maximum values. For 1G-operation, 24-bit counters can wrap around every 10 seconds whereas 32-bit counters can wrap around every 30 seconds depending on the traffic load. For 100M and 10M operations, these values must be scaled by a factor of 10 and 100, respectively.

Table 81. Rx Octets - C_RXOCT (Address 50h)
Block 1/6 Subblock 4-15/0-3

it	Name	Mode	Description	Default
31:0	Rx Octets	R/O	Received octets in good and bad packets	0

Table 82. Tx Octets - C_TXOCT (Address 51h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
31:0	Tx Octets	R/O	Transmitted octets in good and bad packets	0

Table 83. Rx Drops - C_RXDROP (Address A0h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
15:0	Rx Drops	R/W	Frames dropped due to lack of receive buffer	0
Note: Any write to this register will clear all counters.				

Table 84. Rx Packets - C_RXPKT (Address A1h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx Packets	R/O	Number of good and bad packets	0
Note: For counting only good RX packets, the sum of high and low priority packets must be used (C_RXHP+C_RXLP).				

Table 85. Rx Broadcasts - C_RXBC (Address A2h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx Broadcasts	R/O	Number of good broadcasts	0

Table 86. Rx Multicasts - C_RXMC (Address A3h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx Multicasts	R/O	Number of good multicasts	0

Table 87. Rx CRC/ALIGN - C_RXCRC (Address A4h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Number of CRC errors	R/O	Alignment errors and RX_ER events	0

Table 88. Rx Undersize - C_RXSHT (Address A5h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx Undersize	R/O	Number of short frames with valid CRC (<64 Bytes)	0

Table 89. Rx Oversize - C_RXLONG (Address A6h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx Oversize	R/O	Number of long frames with valid CRC (according to max_length register)	0

Table 90. Rx Fragments - C_RXFRAG (Address A7h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx Fragments	R/O	Number of short frames with invalid CRC (< 64 bytes)	0

Table 91. Rx Jabbers - C_RXJAB (Address A8h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx Jabbers	R/O	Number of long frames with invalid CRC (according to max_length register)	0

Table 92. Rx 64 Bytes - C_RX64 (Address A9h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx 64 Bytes	R/O	Number of 64-byte frames in good and bad packets	0

Table 93. Rx 65-127 Bytes - C_RX65 (Address AAh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx 65-127 Bytes	R/O	Number of 65–127-byte frames in good and bad packets	0

Table 94. Rx 128-255 Bytes - C_RX128 (Address ABh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx 128-255 Bytes	R/O	Number of 128–255-byte frames in good and bad packets	0

Table 95. Rx 256-511 Bytes - C_RX256 (Address ACh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx 256-511 Bytes	R/O	Number of 256–511-byte frames in good and bad packets	0

Table 96. Rx 512-1023 Bytes - C_RX512 (Address ADh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx 512-1023 Bytes	R/O	Number of 512–1023-byte frames in good and bad packets	0

Table 97. Rx 1024-long Bytes - C_RX1024 (Address AEh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx 1024-long Bytes	R/O	Number of 1024-max_length-byte frames in good and bad packets	0
Note: The maximum frame length is set in the MAXLEN register.				

Table 98. Tx Drops - C_TXDROP (Address AFh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx Drops	R/O	Number of frames dropped due to excessive collision, late collision, or frame ageing	0

Table 99. Tx Packets - C_TXPKT (Address B0h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx Packets	R/O	Number of good packets	0

Table 100. Tx Broadcasts - C_TXBC (Address B1h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx Broadcasts	R/O	Number of good broadcasts	0

Table 101. Tx Multicasts - C_TXMC (Address B2h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx Multicasts	R/O	Number of good multicasts	0

Table 102. Tx Collisions - C_TXCOL (Address B3h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx Collisions	R/O	Number of collisions transmitting frames experience. An excessive collided frame gives 16 counts.	0

Table 103. Tx 64 Bytes - C_TX64 (Address B4h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx 64 Bytes	R/O	Number of 64-byte frames in good and bad packets	0

Table 104. Tx 65-127 Bytes - C_TX65 (Address B5h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx 65-127 Bytes	R/O	Number of 65–127-byte frames in good and bad packets	0

Table 105. Tx 128-255 Bytes - C_TX128 (Address B6h)
Block 1/6 Subblock 4-15/0-3

it	Name	Mode	Description	Default
23:0	Tx 128-255 Bytes	R/O	Number of 128–255-byte frames in good and bad packets	0

Table 106. Tx 256-511 Bytes - C_TX256 (Address B7h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx 256-511 Bytes	R/O	Number of 256–511-byte frames in good and bad packets	0

Table 107. Tx 512-1023 Bytes - C_TX512 (Address B8h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx 512-1023 Bytes	R/O	Number of 512–1023-byte frames in good and bad packets	0

Table 108. Tx 1024-long Bytes - C_TX1024 (Address B9h)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx 1024-long Bytes	R/O	Number of 1024-max_length-byte frames in good and bad packets	0
Note: The maximum frame length is set in the MAXLEN register.				

Table 109. Tx FIFO Drops - C_TXOVFL (Address BAh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
15:0	Tx FIFO Drops	R/O	Number of frames dropped due to lack of transmit buffer	0

Table 110. Rx High Priority Frames - C_RXHP (Address BBh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx High Priority Frames	R/O	Number of Rx frames classified as high priority	0

Table 111. Rx Low Priority Frames - C_RXLP (Address BCh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Rx Low Priority Frames	R/O	Number of Rx frames classified as low priority	0

Table 112. Tx High Priority Frames - C_TXHP (Address BDh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx High Priority Frames	R/O	Number of Tx frames classified as high priority	0

Table 113. Tx Low Priority Frames - C_TXLP (Address BEh)
Block 1/6 Subblock 4-15/0-3

Bit	Name	Mode	Description	Default
23:0	Tx Low Priority Frames	R/O	Number of Tx frames classified as low priority	0

MII Management Bus Block Registers (Block 3)

Table 114. MII-M Status - MIIMSTAT (Address 00h)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
3	Busy	R/O	The bus is currently active	0
1	Reading	R/O	A Read operation is in progress	0
0	Writing	R/O	A Write operation is in progress	0
Note: This register provides the status of the management bus.				

Table 115. MII-M Command - MIIMCMD (Address 01h)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
27	Scan	R/W	Enable SCAN mode	0
26	Operation	R/W	Set MII-M operation to read (1) or write (0)	0
25:21	PHY Address	R/W	Address of PHY to operate on	0
20:16	PHY Register	R/W	Register number for operation	0
15:0	Write Data	R/W	Data to write in write operations	0
Note: An operation will commence when this register is written.				

Table 116. MII-M Return Data - MIIMDATA (Address 02h)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
16	Failure	R/O	Operation failed - no PHY read reply	0
15:0	MII-M Return Data	R/O	Read Data	0

Table 117. MII-M Prescaler - MIIMPRES (Address 03h)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
5:0	Prescale Value	R/W	The divisor for the MIIM clock. A 62.5 MHz clock will be divided by this value. Default clock with default value at approximately 2 MHz. The register must not be configured to anything less than 5.	20h

Table 118. MII-M Scan setup - MIIMSCAN (Address 04h)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
25:21	PhyAddress HIGH	R/W	This is the upper limit for the PHY addresses to be scanned	0
20:16	PhyAddress LOW	R/W	This is the low limit for the PHY addresses to be scanned	0
15:0	PhyRegMask	R/W	The MASK with target bits in the PHY replies	0
Note: When the SCAN bit is set in the command register, the operation set up will be repeated infinitely until the bit is reset by a register write. The PHY address will be looping between the lower and upper limits of the address. In case of a read operation, the scan results register bit (phy addr) will get the value 1 if (phy_reply and phy_mask) = phy_mask, otherwise 0. By this mechanism, it is possible to have an updated link state vector for all 32 PHYs attached to the MII-M bus.				

Table 119. MII-M Scan Results - MIIMSRES (Address 05h)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
31:0	MII-M Scan Results	R/O	The scan results as explained above	0

Memory Initialization Block Registers (Block 3)

Table 120. Initialize - MEMINIT (Address 00h)
Block 3 Subblock 2

Bit	Name	Mode	Description	Default
24:8	Memory Operation	R/W	For proper initialization of RAM, this field MUST be written 10104h. For initiating reading of result of RAM initialization, the field must be written 200h.	0
7:0	Memory Id	R/W	The identifier for the RAM to initialize or to initiate reading of result from. Range is 4-19.	0

Table 121. Read Result - MEMRES (Address 01h)
Block 3 Subblock 2

Bit	Name	Mode	Description	Default
31:2	Reserved	R/O	Contains garbage.	0
1:0	Memory Result	R/O	This field contains the result of the memory initialization. For proper initialization of RAM, this field MUST read 3h.	0

Frame Arbiter Block Registers (Block 5)

Table 122. Arbiter Empty - ARBEMPTY (Address 0Ch)
Block 5 Subblock 0

Bit	Name	Mode	Description	Default
19:4	Arbiter Empty	R/O	Status per source port. No frame is pending from this source	FFFFh

This register is to be used when reseting a port to stop interaction with other ports before shutting the port down. A correct reset sequence is:
- Set DROPCFG to 0x00000000 (drop all frames)
- Set POOLCFG to 0x00000000 (ignore backpressure)
- Clear RX_EN bit in MACCONF
- Wait until arbiter empty bit is set for the port
- If time out from above operation:
  - Set DROPCFG, POOLCFG and RX_EN=0 on all ports
  - Wait until arbiter empty bit is set for all ports
  - If time out from above operation:
    - Make a full core reset.
    - Reconfigure everything according to mode
  - else
    - Reset the target port
    - Reconfigure all ports according to mode
  - endif
- else
  - Reset the target port
  - Reconfigure port according to mode
- endif

The timeout period should be set to 500 ms, but is not critical.
For further information on the reset procedure, refer to the Heathrow-III Reference Board Software Manual.

Table 123. Arbiter Discard - ARBDISC (Address 0Eh)
Block 5 Subblock 0

Bit	Name	Mode	Description	Default
19:4	Arbiter Discard	R/W	Config bit per port. All frames from a source will be discarded if the source corresponding bit is set in this register	0

CPU Capture Block Registers (Block 4)

Table 124. Read Pointer - CAPREADP (Address 00h)
Block 4 Subblock 4

Bit	Name	Mode	Description	Default
10:0	Read Pointer	R/W	The physical address of the first frame for reading. The RAM cells are 8 bytes wide (2048 x 8 = 16 kB buffer).	0

Table 124. Read Pointer - CAPREADP (Address 00h)
Block 4 Subblock 4

Bit	Name	Mode	Description	Default
Note: Write anything to this register and the read pointer will be advanced to the next frame for readout. This register is only present in Subblock 4. Subblocks 0–3 are for frame readout.				

Table 125. Write Pointer - CAPWRP (Address 03h)
Block 4 Subblock 4

Bit	Name	Mode	Description	Default
17	Frame Ready	R/O	A frame is ready for readout. Note that buffer address 0 is always pointing to the next frame available	0
16	Frame Dropped	R/W	A frame for the CPU buffer is dropped due to lack of buffer space	0
10:0	Write Pointer	R/O	The physical address of the start of the next incoming frame	0
Note: The Frame Dropped status bit is cleared by writing anything to this register. This register is only present in Subblock 4. Subblocks 0–3 are for frame readout.				

Table 126. Full Reset - CAPRST (Address FFh)
Block 4 Subblock 7

Bit	Name	Mode	Description	Default
31:0	Full Reset	W/O	Writing anything to this register reset the CPU receive block fully	0
Note: This register is only present in Subblock 7.				

Frame Analyzer Block Registers (Block 2)

Table 127. Advanced Learning Setup - ADVLEARN (Address 03h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
31	Automode	R/W	Unicast source addresses will automatically be inserted into the MAC table	1
30	Dropmode	R/W	Frames subject to learning or station port move will not be forwarded based on destination address	0
29	VlanCheck	R/W	If a frame is discarded because of the VLAN Source Check flag in the VLAN table (see VLANACES register), the source address will not be learned	0
24	CpuLearn	R/W	Learn frames will be forwarded to the CPU Capture module	0

Table 127. Advanced Learning Setup - ADVLEARN (Address 03h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
19:4	LearnMirror	R/W	Learn frames will also be forwarded to ports marked in this mask	0

Table 128. IP Multicast Flood Mask - IFLODMSK (Address 04h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
19:4	IP Multicast Flood Mask	R/W	Port mask with allowed ports for unknown IP multicast flooding. Will be overruled if Flood FwdKill flag is set. The mask only applies if the Enable IPMC Flood Mask field in CATCONF register is set.	0

Table 129. VLAN Source Port Mask - VLANMASK (Address 05h)
Block 2 Subblock 0

it	Name	Mode	Description	Default
19:4	VLAN Source Port Mask	R/W	Mask for requiring VLAN Source Check on Ingress port. If bit<port> is set, the <port> must be marked in the ingress frame's VLAN Port Mask, otherwise the frame is dropped	0

Table 130. Station Move Logger - ANMOVED (Address 08h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
19:4	Station Move Logger	R/W	Sticky bit set when a station has been learned on a port while already learned on another port	0
Note: The register is cleared by writing the bits to be cleared. This mask can be used to detect topology problems in the network, where stations are learned on multiple ports repeatedly. If some bits in this register get asserted repeatedly, the ports can be shut down, or management warnings can be issued.				

Table 131. Ageing Filter - ANAGEFIL (Address 09h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
31	PID Enab	R/W	If set only entries with matching destination are aged	0
20:16	PID Value	R/W	Destination port for ageing only the part of table with entries on specific ports	0

Table 131. Ageing Filter - ANAGEFIL (Address 09h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
15	vID Enab	R/W	If set only entries with matching VLAN membership are aged	0
11:0	vID Value	R/W	VLAN Identifier for ageing only the parts of the MAC table that contain entries belonging to specific VLAN(s)	0
Note: This register sets up which entries should be touched by an ageing operation. This way it is possible to have different ageing periods in each VLAN, and to have quick removal of entries on specific ports.				

Table 132. Event Sticky Bits - ANEVENTS (Address 0Ah)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
21	Learn Drop	R/W	A frame was dropped as it was subject to learning, and the DropMode flag was set in ADVLEARN	0
20	Aged Entry	R/W	An entry was removed at CPU Learn, or CPU requested an ageing process	0
19	CPU Learn Failed	R/W	An learn failed due to hash table depletion	0
18	AUTO Learn Failed	R/W	A learn of incoming source MAC address failed due to hash table depletion	0
17	Learn Remove	R/W	An entry was removed when learning a new source MAC address	0
16	AUTO Learned	R/W	An entry was learned from an incoming frame	0
15	AUTO Moved	R/W	A station was moved to another port	0
14	Dropped	R/W	A packet was not transmitted to any ports	0
13	Classified Drop	R/W	A packet was not forwarded due to classification (like BPDUs)	0
12	Classified Copy	R/W	A packet was copied to the CPU due to classification	0
11	VLAN Discard	R/W	A packet was discarded due to lack of VLAN membership on source port	0
10	FWD Discard	R/W	A packet was discarded due to missing forwarding state on source port	0
9	Multicast Flood	R/W	A packet was flooded with multicast flooding mask	0
8	Unicast Flood	R/W	A packet was flooded with unicast flooding mask	0
7	Destination Known	R/W	A packet was forwarded with known destination MAC address	0
6	Bucket3 Match	R/W	A destination was found in hash table bucket 3	0
5	Bucket2 Match	R/W	A destination was found in hash table bucket 2	0
4	Bucket1 Match	R/W	A destination was found in hash table bucket 1	0
3	Bucket0 Match	R/W	A destination was found in hash table bucket 0	0

Table 132. Event Sticky Bits - ANEVENTS (Address 0Ah)
Block 2 Subblock 0 (cont'd)

Bit	Name	Mode	Description	Default
2	CPU Operation	R/W	A CPU initiated operation has been processed	1
1	DMAC Lookup	R/W	A destination address has been looked up in the MAC table	0
0	SMAC Lookup	R/W	A source address has been looked up in the MAC table	0
Note: This register contains various debug event logs. A sticky bit is cleared by writing it.				

Table 133. Event Sticky Mask - ANCNTMSK (Address 0Bh)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
21:0	Sticky Mask	R/W	This mask determines which events are to be counted by the ANCNTVAL register	0
Note: Refer to the flag list in the ANEVENTS register. For proper operation, only one bit should be set in the mask. Otherwise - if two events occur simultaneously, they might be mistaken as one event only.				

Table 134. Event Sticky Counter - ANCNTVAL (Address 0Ch)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
27:0	Event Sticky Counter	R/W	This counter counts the number of events seen as specified in the Event Sticky Mask	0

Table 135. Learn Mask - LERNMASK (Address 0Dh)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
19:4	Learn Mask	R/W	If bit<port> is set in this mask, incoming frames are subject to auto learning on that port	FFFFh

Table 136. Unicast Flood Mask - UFLODMSK (Address 0Eh)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
19:4	Unicast Flood Mask	R/W	Port mask with allowed ports for unknown unicast flooding	FFFFh

Table 137. Multicast Flood Mask - MFLODMSK (Address 0Fh)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
19:4	Multicast Flood Mask	R/W	Port mask with allowed ports for unknown multicast flooding, and for broadcast flooding	FFFFh

Table 138. Receive Mask - RECVMASK (Address 10h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
19:4	Receive Mask	R/W	If a port is not marked in this mask, incoming frames will be discarded	0

Table 139. Aggregation Mode - AGGRCNTL (Address 20h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
1:0	Aggregation Mode	R/W	Mode of aggregation 00 = Reserved 01 = SMAC 10 = DMAC 11 = SMAC xor DMAC	1h

Table 140. Aggregation Masks - AGGRMSKS (Address 30h - 3Fh)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
19:4	Mask	R/W	Mask used to select only one port within each aggregation group	FFFFh
Note: These 16 masks select a single port in each aggregated port group. If no aggregation is configured, these masks will be all 1s.				

Table 141. Destination Port Masks - DSTMASKS (Address 40h - 7Fh)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
19:4	Destination Port Mask	R/W	Mask used to translate a logical port number from a destination lookup into a set of ports.	See below

Table 141. Destination Port Masks - DSTMASKS (Address 40h - 7Fh)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
Note: By default, Destination Port Masks 4-19 have the bit corresponding to their number set only. The remaining masks are cleared to 0 for multicasts. In normal situations it doesn't make sense to change the first 16 masks from the default, except in aggregation setups. Otherwise frames to a station would be transmitted on another port than the port it was auto learned on.				

Table 142. Source Port Masks - SRCMASKS (Address 84h - 93h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
25	CPU Copy	R/W	All frames from this port will be copied to the CPU capture buffer	0
24	Mirror	R/W	All frames from this port will be mirrored to the port set in the Analyzer Config register	0
19:4	Ports	R/W	Mask used to disallow frames from being forward from specific source port.	See below
Note: These masks are used to prevent frames from being looped back to the ports on which they were received, and must be updated according to the aggregation configuration. A frame received on port n, will use register 0x80+n as a mask to filter out transmit ports to avoid loop back, or to facilitate port grouping (port based VLANs). The default values are that all bits are set except for the index number. Ex. srcmask 5 has default value 11111111111111111011111b, or FFFFDFh.				

Table 143. Mac Table Command - MACACCES (Address B0h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
14	CPUCopy	R/W	Frames for this destination will be copied to the CPU capture buffer.	0
13	FwdKill	R/W	Frames for this destination are dropped.	0
12	Ignore VLAN	R/W	The VLAN mask is ignored for this destination.	0
11	Aged Flag	R/W	This flag is set on every ageing run. Entry is removed if set already. The flag is cleared when the entry is target for a source address lookup.	0
10	Valid	R/W	Entry is valid.	0
9	Locked	R/W	Entry is locked and will not be removed by ageing or auto learn pushout. Port move events are only registered in ANMOVE if a MAC address is learned with the lock flag cleared.	0
8:3	Destination Index	R/W	Index into the destination mask table. For unicasts a number from 0-15.	0

Table 143. Mac Table Command - MACACCES (Address B0h)
Block 2 Subblock 0 (cont'd)

Bit	Name	Mode	Description	Default
2:0	Mac Table Command	R/W	Mac Table Command.	0
Note: This register is used for updating or reading the MAC table from the CPU. The command selects between different operations, and takes the following values: 000 = idle (the previous operation is complete) 001 = learn (the MAC data is learned into the table) 010 = forget (the MAC data is removed from the table) 011 = age table (the ageing procedure is performed on the table) 100 = flush table (all nonlocked entries is removed from the table) 101 = clear table (table is completely cleared) 110 = read entry (the entry pointed to by the MAC Table Index register is read) 111 = write entry (the entry pointed to by the MAC Table Index register is written)				

Table 144. Mac Table Index - MACTINDX (Address C0h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
13	Shadow	R/W	Enable MAC table shadow register. With this register set, when reading from bucket 0, the remaining three buckets will be latched into a register for future access.	0
12:11	Bucket	R/W	The bucket selects one of the 4 entries per table line.	0
10:0	Index	R/W	The index selects one of the 2048 MAC table lines.	0
Note: Used in MAC table read and write operations, where this register selects the entry to read or write.				

Table 145. Mac Address High - MACHDATA (Address 06h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
27:16	vID	R/W	vID to be used in MAC CPU write operations. Additionally, vID is returned in read operations.	0
15:0	MAC Address High	R/W	Upper 16 MAC address bits for CPU write operations. Additionally, MAC Address High is returned in read operations.	0

Table 146. Mac Address Low - MACLDATA (Address 07h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
31:0	Mac Address Low	R/W	Lower 32 MAC address bits for CPU operations	0

Table 147. VLAN Table Command - VLANACES (Address D0h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
27	VLAN Mirror	R/W	Set if all frames in this VLAN are to be mirrored onto the port specified in the Analyzer Config register	0
26	VLAN Source Check	R/W	Set if frames in this VLAN must be marked in the VLAN Port Mask	0
25:2	VLAN Port Mask	R/W	Frames in this VLAN can only be sent to ports in this mask	FFFFh
1:0	VLAN Table Command	R/W	VLAN Table Command	0
Note: This register is used for updating and reading the VLAN table from the CPU. The command selects between various operations, and takes on the following values: 00 = idle (the previous operation is complete) 01 = read entry (the entry set in VLAN Index is read out into this register) 10 = write entry (the entry set in VLAN Index is written) 11 = clear table (the VLAN table is initialized to default values) The Command bits must read as Idle before a new command can be issued.				

Table 148. VLAN Table Index - VLANTINDX (Address E0h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
11:0	Index	R/W	The index selects one of the 4096 VLAN table lines	0
Note: Used in VLAN table read and write operations, where this register selects the entry to read or write.				

Table 149. Analyzer Config Register - AGENCNTL (Address F0h)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
11	Flood CPUCopy	R/W	Flooded frames will be copied to the CPU	0
10	Flood FwdKill	R/W	Flooded frames will not be sent to any ports	0
9	Flood Ignore VLAN	R/W	Flooded frames will not be sensitive to the VLAN masks	0

**Table 149. Analyzer Config Register - AGENCNTL (Address F0h)
Block 2 Subblock 0 (cont'd)**

Bit	Name	Mode	Description	Default
8	Mirror CPU	R/W	Frames destined for the CPU capture buffer will also be forwarded to the configured mirror port.	0
7	Learn CPUCopy	R/W	Auto learned stations will get the CPUCopy flag set in their entry in the MAC table	0
6	Learn FwdKill	R/W	Auto Learned stations will get the FwdKill flag set in their entry in the MAC table	0
5	Learn Ignore VLAN	R/W	Auto Learned stations will get the Ignore VLAN flag set in their entry in the MAC table	0
4:0	Mirror Port	R/W	Frames mirrored will be sent to this port	0

SIGNAL DESCRIPTION

To make it easier to distinguish the signals from each other and which interface each belongs to, most of the signals have the interface name appended as prefix. Additionally, an active low signal is denoted with a lower case 'n' as prefix on the actual 'name', not interface name (for example: PI_nOE).

Signal List By Function

The following notation has been used to define the pin types.

Table 150. Pin Type Definitions

Pin Type	Definition
I	Input only
O	Output only
I/O	Bidirectional
OZ	3-state output
A	Analog
Power	Power
GND	Ground
NC	No connection, do not connect
3V	3.3 V tolerant
5V	5 V tolerant

Clock Circuits

Table 151. Clk Interface

Signal Name	Type	Description
PLL_Cap0 PLL_Cap1	A	PLL Loop filter capacitor, connect 100 nF capacitor between the pins
Clk	I, 3V	System reference clock, LVTTL input. It can be either 25 MHz or 125 MHz selectable by Clk125_En signal.
Clk125_En	I, 3V	0 = 25 MHz clock select 1 = 125 MHz clock select
PLL_En	I, 3V	Internal test, pull up to VDD_IN

Combined RGMII/RTBI Interface

Table 31 contains a complete description of port 0, when used in the different modes. The signal name used is the default RGMII name, if the signal has a different name in another mode, this name is listed under the signal description for this mode.

Table 152. RGMII Ports

Signal Name	Type	Description
RGMII[0:15]_RD0 RGMII[0:15]_RD1 RGMII[0:15_RD2 RGMII[0:15]_RD3	I	RGMII mode (10/100 Mbit): Receive data input. Contains bit [3:0] on the rising edge of the Rx_Clk. Data is only sampled on the rising edge not on the falling. RGMII mode (1000 Mbit): Multiplexed receive data input. Contains bit [3:0] on the rising edge of the Rx_Clk and bit [7:4] on the falling edge. RTBI mode: Multiplexed receive data input. Contains bit [3:0] on the rising edge of the Rx_Clk and bit [8:5] on the falling edge.
RGMII[0:15]_Rx_Clk	I	Receive Clock. This clock is used to synchronize the receive data and control.
RGMII[0:15]_Rx_Ctrl	I	RGMII mode: Data valid and receive error input. On rising edge of the Rx_Clk, this input serves as data valid signaling valid data from the PHY is available on RD[3:0]. On the falling edge of Rx_Clk it contains a logical derivative of data valid and receive error from the PHY (see RGMII standard). RTBI mode: Becomes RTBI_RD4, contains bit 4 on the rising edge of the Rx_Clk and bit 9 on the falling edge.
RGMII[0:15]_TD0 RGMII[0:15]_TD1 RGMII[0:15]_TD2 RGMII[0:15]_TD3	O	RGMII mode (10/100 Mbit): Transmit data output. Contains bit [3:0] on the rising edge of the Tx_Clk. No data change occur on the falling edge of Tx_Clk. RGMII mode (1000 Mbit): Multiplexed transmit data output. Contains bit [3:0] on the rising edge of the Tx_Clk and bit [7:4] on the falling edge. RTBI mode: Multiplexed transmit data output. Contains bit [3:0] on the rising edge of the Tx_Clk and bit [8:5] on the falling edge.
RGMII[0:15]_Tx_Clk	O	Transmit Clock. This clock is continuously driven from the MAC, and transmit data and control are synchronized to it.

Table 152. RGMII Ports (cont'd)

Signal Name	Type	Description
RGMII[0:15]_Tx_Ctrl	O	RGMII mode: Transmit control. On the rising edge of Tx_Clk it serves as transmit enable indicating valid data on TD[3:0]. On the falling edge it contains a logical derivative based on transmit enable and error from the MAC (see RGMII standard). RTBI mode: Becomes RTBI_TD4, contains bit 4 on the rising edge of the Tx_Clk and bit 9 on the falling edge.
RTBI[0:15]_SigDet	I	RGMII: Unused, pull high or low. RTBI: Signal detect, active high. Indicates valid RTBI receive data. The SigDet pins usage and polarity is controlled by the TBI control register (TBICTRL).

Power Supply and Ground Pins

Table 153. Power and Ground

Signal Name	Type	Description
VDD	Power	1.8 V core supply
VDD_OUT25	Power	2.5 V output supply
VDD_OUT33	Power	3.3 V output supply
VDD_IN	Power	2.5 V input supply
VSS	GND	Common ground
VDD_PLL	Power	2.5 V supply to internal PLL
VSS_PLL	GND	Internal PLL ground

JTAG Interface

Table 154. JTAG Interface

Signal Name	Type	Description
JTAG_nTRST	I, 5V	JTAG Test Reset, active low. For normal operation JTAG_nTRST should be pulled low.
JTAG_TCK	I, 5V	JTAG Clock.
JTAG_TDI	I, 5V	JTAG Test Data In.
JTAG_TDO	OZ, 3V	JTAG Test Data Out.
JTAG_TMS	I, 5V	JTAG Test Mode Select.

Parallel CPU Interface (PI)

Table 155. PI Interface

Signal Name	Type	Description
PI_Addr0 PI_Addr1 PI_Addr2 PI_Addr3 PI_Addr4 PI_Addr5 PI_Addr6 PI_Addr7 PI_Addr8 PI_Addr9 PI_Addr10 PI_Addr11 PI_Addr12 PI_Addr13 PI_Addr14 PI_Addr15	I, 3V	LSB Parallel CPU interface address bus Selects the block, subblock and address Refer to ”Interrupt Control” on page 50 for a description of the address space MSB
PI_Data0 PI_Data1 PI_Data2 PI_Data3 PI_Data4 PI_Data5 PI_Data6 PI_Data7 PI_Data8 PI_Data9 PI_Data10 PI_Data11 PI_Data12 PI_Data13 PI_Data14 PI_Data15	I/O, 3V	LSB Parallel CPU interface data bus Driven by CPU at write, Heathrow-III at read MSB
PI_IRQ	O	A configurable interrupt signal for various events. The interrupt signal's polarity can be programmed. The Interrupt pin is not an open drain output and should not be wire-ORed to other pins.
PI_nCS	I, 3V	Start a CPU operation.
PI_nDone	OZ, 3V	Acknowledges an operation. Programmable polarity.
PI_nOE	I, 3V	Enable drive of the data bus from Heathrow-III.
PI_nWR	I, 3V	Selects read (1) or write (0).

Serial Interface

Table 156. SI Interface

Signal Name	Type	Description
SI_Clk	I, 3V	SI clock from the master.
SI_DI	I, 3V	Serial input from the master.
SI_DO	OZ, 3V	Serial output to the master.
SI_nEn	I, 3V	0 = enable SI interface. 1 = disable SI interface.

MII Management Interface

Table 157. MII Management Interface

Signal Name	Type	Description
MDIO_0	I/O, 5V	Management data input/output – interface 0. MDIO is a bidirectional signal between the PHY and Heathrow-III, used to transfer control and status information. Control information is driven by Heathrow-III synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by Heathrow-III.
MDC_0	O	Management data clock – interface 0. MDC is sourced by the Station Management entity (Heathrow-III) to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal.
MDIO_1	I/O, 5V	Management data input/output – interface 1. Refer to MDIO_0 for a description.
MDC_1	O	Management data clock – interface 1. Refer to MDC_0 for a description.

General Purpose I/Os

Table 158. GPIO Signals

Signal Name	Type	Description
GPIO1 GPIO2 GPIO3 GPIO4	I, 3V	General purpose I/O. If unused, pull high to VDD_IN or low to VSS.

Miscellaneous

Table 159. Miscellaneous Signals

Signal Name	Type	Description
nReset	I, 3V	Global chip reset, active low
Test_Mode	I, 3V	Internal test, pull low to VSS
VDD_Probe	A	Internal test, leave floating
Reserved_0	NC	Leave floating
Reserved_1	I, 3V	Internal test, pull low to VSS

Signal List By Ball Number

Table 160 lists the signals by ball number.

Table 160. Signal List by Ball Number

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
A1	VSS_77	A35	PI_Data10	B30	PI_Addr2
A2	VSS_75	A36	PI_Data9	B31	PI_nOE
A3	VSS_74	A37	VSS_44	B32	PI_IRQ
A4	Reserved_94	A38	VSS_45	B33	PI_Data13
A5	VSS_70	A39	VSS_46	B34	VDD_IN_1
A6	Reserved_88	B1	VSS_78	B35	VSS_40
A7	VSS_68	B2	Reserved_95	B36	VSS_41
A8	VDD_OUT25_6	B3	VSS_73	B37	VSS_42
A9	Reserved_78	B4	VSS_71	B38	VDD_OUT33_0
A10	Reserved_75	B5	Reserved_92	B39	VSS_43
A11	VSS_66	B6	Reserved_89	C1	VSS_81
A12	Reserved_69	B7	Reserved_85	C2	VSS_80
A13	Reserved_67	B8	Reserved_82	C3	VSS_79
A14	VSS_63	B9	Reserved_79	C4	VDD_OUT25_8
A15	Reserved_61	B10	Reserved_76	C5	VSS_69
A16	VDD_OUT25_2	B11	Reserved_72	C6	VDD_IN_6
A17	VSS_60	B12	Reserved_70	C7	Reserved_86
A18	MDC_1	B13	Reserved_68	C8	Reserved_83
A19	MDIO_1	B14	Reserved_64	C9	Reserved_80
A20	VSS_58	B15	Reserved_62	C10	VSS_67
A21	GPIO2	B16	Reserved_59	C11	Reserved_73
A22	VDD_OUT33_4	B17	Reserved_56	C12	Reserved_71
A23	VSS_56	B18	Reserved_54	C13	VSS_64
A24	JTAG_TDI	B19	VDD_OUT25_0	C14	Reserved_65
A25	Clk125_En	B20	MDIO_0	C15	Reserved_63
A26	VSS_53	B21	VDD_IN_3	C16	VSS_61
A27	PI_Addr12	B22	SI_DO	C17	Reserved_57
A28	PI_Addr9	B23	JTAG_TDO	C18	Reserved_55
A29	VSS_50	B24	JTAG_TCK	C19	VSS_59
A30	PI_Addr3	B25	Test_Mode	C20	Reserved_1
A31	PI_Addr0	B26	PI_Addr15	C21	VSS_57
A32	VSS_48	B27	PI_Addr11	C22	SI_DI
A33	PI_Data14	B28	VDD_IN_2	C23	JTAG_TMS
A34	PI_Data11	B29	PI_Addr6	C24	VSS_55

Table 160. Signal List by Ball Number (cont'd)

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
C25	nReset	D20	GPIO4	E15	VSS_62
C26	PI_Addr14	D21	GPIO1	E16	VDD_27
C27	VSS_52	D22	SI_nEn	E17	VDD_26
C28	PI_Addr8	D23	JTAG_nTRST	E18	VDD_25
C29	PI_Addr5	D24	VDD_Probe	E19	VDD_24
C30	VSS_49	D25	PLL_En	E20	GPIO3
C31	PI_nCS	D26	PI_Addr13	E21	VDD_23
C32	PI_nDone	D27	PI_Addr10	E22	SI_Clk
C33	VSS_47	D28	PI_Addr7	E23	VDD_22
C34	VDD_OUT33_2	D29	PI_Addr4	E24	VDD_21
C35	VSS_36	D30	PI_Addr1	E25	VSS_54
C36	PI_Data7	D31	PI_nWR	E26	VDD_20
C37	VSS_37	D32	PI_Data15	E27	VDD_19
C38	VSS_38	D33	PI_Data12	E28	VSS_51
C39	VSS_39	D34	PI_Data8	E29	VDD_18
D1	Reserved_97	D35	PI_Data6	E30	VDD_17
D2	VSS_83	D36	VSS_34	E31	VDD_16
D3	Reserved_96	D37	PI_Data4	E32	VDD_OUT33_3
D4	VSS_82	D38	VSS_35	E33	VDD_15
D5	Reserved_93	D39	PI_Data3	E34	PI_Data5
D6	Reserved_90	E1	VSS_76	E35	VDD_14
D7	Reserved_87	E2	Reserved_99	E36	VDD_OUT33_1
D8	Reserved_84	E3	VSS_72	E37	VSS_32
D9	Reserved_81	E4	Reserved_98	E38	PI_Data2
D10	VDD_IN_5	E5	VDD_33	E39	VSS_33
D11	Reserved_74	E6	Reserved_91	F1	VDD_IN_7
D12	VDD_OUT25_4	E7	VDD_32	F2	Reserved_102
D13	VDD_OUT25_3	E8	VDD_OUT25_5	F3	Reserved_101
D14	Reserved_66	E9	VDD_31	F4	Reserved_100
D15	VDD_IN_4	E10	Reserved_77	F5	VDD_OUT25_7
D16	Reserved_60	E11	VSS_65	F35	VSS_31
D17	Reserved_58	E12	VDD_30	F36	Reserved_52
D18	VDD_OUT25_1	E13	VDD_29	F37	Reserved_53
D19	MDC_0	E14	VDD_28	F38	PI_Data0

Table 160. Signal List by Ball Number (cont'd)

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
F39	PI_Data1	K4	RGMII0_Tx_Clk	N37	VSS_25
G1	Reserved_105	K5	VDD_36	N38	Reserved_33
G2	Reserved_104	K35	Reserved_41	N39	Reserved_34
G3	VSS_84	K36	Reserved_42	P1	VSS_91
G4	Reserved_103	K37	VSS_28	P2	RGMII1_TD2
G5	VDD_34	K38	VDD_OUT25_47	P3	RGMII1_TD3
G35	VDD_13	K39	Reserved_43	P4	RGMII1_Tx_Ctrl
G36	Reserved_50	L1	VSS_88	P5	VDD_OUT25_12
G37	VSS_30	L2	RGMII0_RD2	P35	VDD_OUT25_45
G38	VDD_IN_0	L3	RGMII0_RD1	P36	Reserved_30
G39	Reserved_51	L4	VDD_37	P37	Reserved_31
H1	VSS_86	L5	VDD_38	P38	Reserved_32
H2	VDD_OUT25_9	L35	VDD_10	P39	VSS_24
H3	RGMII0_TD1	L36	Reserved_38	R1	RGMII1_RD0
H4	RGMII0_TD0	L37	Reserved_39	R2	RTBI1_SigDet
H05	VSS_85	L38	Reserved_40	R3	RGMII1_Tx_Clk
H35	VDD_12	L39	VSS_27	R4	VDD_40
H36	Reserved_47	M1	RGMII0_Rx_Clk	R5	VDD_41
H37	Reserved_48	M2	RGMII0_Rx_Ctrl	R35	VDD_8
H38	Reserved_49	M3	RGMII0_RD3	R36	Reserved_26
H39	VSS_29	M4	VDD_IN_8	R37	Reserved_27
J1	VDD_OUT25_10	M5	VSS_89	R38	Reserved_28
J2	RGMII0_Tx_Ctrl	M35	VSS_26	R39	Reserved_29
J3	RGMII0_TD3	M36	Reserved_35	T1	RGMII1_RD1
J4	RGMII0_TD2	M37	Reserved_36	T2	RGMII1_RD2
J5	VDD_35	M38	Reserved_37	T3	VSS_92
J35	VDD_11	M39	VDD_IN_27	T4	RGMII1_RD3
J36	Reserved_44	N1	RGMII1_TD0	T5	VDD_IN_9
J37	Reserved_45	N2	RGMII1_TD1	T35	Reserved_23
J38	VDD_OUT25_48	N3	VSS_90	T36	VDD_IN_26
J39	Reserved_46	N4	VDD_OUT25_11	T37	VSS_23
K1	RGMII0_RD0	N5	VDD_39	T38	Reserved_24
K2	RTBI0_SigDet	N35	VDD_9	T39	Reserved_25
K3	VSS_87	N36	VDD_OUT25_46	U1	VSS_93

Table 160. Signal List by Ball Number (cont'd)

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
U2	RGMII1_Rx_Ctrl	Y35	VSS_19	AC39	VSS_17
U3	RGMII1_Rx_Clk	Y36	VDD_PLL	AD1	RGMII3_Tx_Clk
U4	RGMII2_TD0	Y37	Clk	AD2	RTBI3_SigDet
U5	VDD_42	Y38	Reserved_0	AD3	VSS_99
U35	VDD_7	Y39	VSS_20	AD4	RGMII3_RD0
U36	Reserved_20	AA1	VDD_IN_10	AD5	RGMII3_RD1
U37	Reserved_21	AA2	RGMII2_RD3	AD35	Reserved_5
U38	Reserved_22	AA3	VSS_97	AD36	Reserved_6
U39	VSS_22	AA4	RGMII2_Rx_Ctrl	AD37	VSS_16
V1	RGMII2_TD1	AA5	VDD_44	AD38	VDD_OUT25_42
V2	VDD_OUT25_13	AA35	VDD_5	AD39	Reserved_7
V3	RGMII2_TD2	AA36	VSS_PLL	AE1	RGMII3_RD2
V4	RGMII2_TD3	AA37	VSS_18	AE2	VDD_IN_11
V5	RGMII2_Tx_Ctrl	AA38	PLL_Cap0	AE3	RGMII3_RD3
V35	VDD_OUT25_43	AA39	PLL_Cap1	AE4	RGMII3_Rx_Ctrl
V36	Reserved_17	AB1	RGMII2_Rx_Clk	AE5	VDD_46
V37	Reserved_18	AB2	RGMII3_TD0	AE35	VDD_3
V38	Reserved_19	AB3	RGMII3_TD1	AE36	Reserved_2
V39	VDD_OUT25_44	AB4	VDD_OUT25_15	AE37	Reserved_3
W1	VDD_OUT25_14	AB5	RGMII3_TD2	AE38	VDD_OUT25_41
W2	RGMII2_Tx_Clk	AB35	Reserved_11	AE39	Reserved_4
W3	VSS_94	AB36	VDD_IN_24	AF1	VSS_100
W4	RTBI2_SigDet	AB37	Reserved_12	AF2	RGMII3_Rx_Clk
W5	VDD_43	AB38	Reserved_13	AF3	RGMII4_TD0
W35	VDD_6	AB39	Reserved_14	AF4	RGMII4_TD1
W36	VDD_IN_25	AC1	VSS_98	AF5	VDD_OUT25_17
W37	VSS_21	AC2	RGMII3_TD3	AF35	VDD_IN_23
W38	Reserved_15	AC3	RGMII3_Tx_Ctrl	AF36	RGMII15_RD3
W39	Reserved_16	AC4	VDD_OUT25_16	AF37	RGMII15_Rx_Ctrl
Y1	VSS_96	AC5	VDD_45	AF38	RGMII15_Rx_Clk
Y2	RGMII2_RD0	AC35	VDD_4	AF39	VSS_15
Y3	RGMII2_RD1	AC36	Reserved_8	AG1	RGMII4_TD2
Y4	RGMII2_RD2	AC37	Reserved_9	AG2	RGMII4_TD3
Y5	VSS_95	AC38	Reserved_10	AG3	VSS_101

Table 160. Signal List by Ball Number (cont'd)

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
AG4	RGMII4_Tx_Ctrl	AK37	VSS_12	AP2	VDD_IN_13
AG5	VDD_47	AK38	RGMII14_Rx_Clk	AP3	RGMII5_Rx_Ctrl
AG35	VDD_2	AK39	RGMII15_TD0	AP4	RGMII5_Rx_Clk
AG36	RGMII15_RD0	AL1	RGMII5_TD1	AP5	RGMII6_TD0
AG37	VSS_14	AL2	VDD_OUT25_19	AP35	VDD_67
AG38	RGMII15_RD1	AL3	RGMII5_TD2	AP36	RGMII13_Rx_Clk
AG39	RGMII15_RD2	AL4	RGMII5_TD3	AP37	RGMII14_TD0
AH1	VDD_OUT25_18	AL5	VSS_105	AP38	RGMII14_TD1
AH2	RGMII4_Tx_Clk	AL35	VSS_11	AP39	VDD_OUT25_37
AH3	RTBI4_SigDet	AL36	RGMII14_RD1	AR1	VSS_110
AH4	RGMII4_RD0	AL37	RGMII14_RD2	AR2	RGMII5_RD3
AH5	VSS_102	AL38	RGMII14_RD3	AR3	VSS_109
AH35	RGMII15_TD3	AL39	RGMII14_Rx_Ctrl	AR4	RGMII6_TD1
AH36	RGMII15_Tx_Ctrl	AM1	VSS_106	AR5	VSS_108
AH37	VDD_OUT25_40	AM2	RGMII5_Tx_Ctrl	AR6	RTBI6_SigDet
AH38	RGMII15_Tx_Clk	AM3	VDD_OUT25_20	AR7	VDD_51
AH39	RTBI15_SigDet	AM4	RGMII5_Tx_Clk	AR8	RGMII6_Rx_Ctrl
AJ1	VSS_103	AM5	VDD_49	AR9	RGMII7_TD3
AJ2	RGMII4_RD1	AM35	RGMII14_TD2	AR10	VDD_52
AJ3	RGMII4_RD2	AM36	RGMII14_Tx_Clk	AR11	VSS_127
AJ4	VDD_IN_12	AM37	RTBI14_SigDet	AR12	VDD_53
AJ5	VDD_48	AM38	RGMII14_RD0	AR13	VDD_54
AJ35	VDD_1	AM39	VSS_10	AR14	RGMII8_Tx_Clk
AJ36	RGMII15_TD1	AN1	RTBI5_SigDet	AR15	VDD_55
AJ37	VDD_OUT25_39	AN2	RGMII5_RD0	AR16	RGMII8_Rx_Clk
AJ38	RGMII15_TD2	AN3	VSS_107	AR17	VDD_56
AJ39	VSS_13	AN4	RGMII5_RD1	AR18	VDD_OUT25_28
AK1	RGMII4_RD3	AN5	VDD_50	AR19	VDD_57
AK2	RGMII4_Rx_Ctrl	AN35	VDD_66	AR20	RGMII9_Rx_Ctrl
AK3	VSS_104	AN36	RGMII14_TD3	AR21	VDD_58
AK4	RGMII4_Rx_Clk	AN37	VSS_9	AR22	RGMII10_Tx_Clk
AK5	RGMII5_TD0	AN38	RGMII14_Tx_Ctrl	AR23	VDD_59
AK35	VDD_0	AN39	VDD_OUT25_38	AR24	VDD_60
AK36	VDD_IN_22	AP1	RGMII5_RD2	AR25	VSS_138

Table 160. Signal List by Ball Number (cont'd)

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
AR26	RGMII11_Tx_Clk	AT21	VDD_OUT25_29	AU16	VSS_131
AR27	VDD_61	AT22	VDD_OUT25_30	AU17	RGMII9_TD3
AR28	VSS_141	AT23	RGMII10_RD2	AU18	RTBI9_SigDet
AR29	VDD_62	AT24	RGMII10_Rx_Clk	AU19	VSS_133
AR30	RGMII12_Tx_Ctrl	AT25	RGMII11_TD1	AU20	RGMII10_TD0
AR31	VDD_63	AT26	VDD_OUT25_32	AU21	VSS_135
AR32	RGMII12_RD3	AT27	RGMII11_RD1	AU22	RGMII10_Tx_Ctrl
AR33	VDD_64	AT28	RGMII11_Rx_Ctrl	AU23	VDD_IN_18
AR34	VDD_65	AT29	RGMII12_TD1	AU24	VSS_137
AR35	RGMII13_RD0	AT30	RGMII12_TD3	AU25	RGMII11_TD0
AR36	RGMII13_RD3	AT31	RGMII12_RD0	AU26	RGMII11_Tx_Ctrl
AR37	VSS_7	AT32	VDD_IN_20	AU27	VSS_140
AR38	VSS_8	AT33	RGMII13_TD0	AU28	RGMII11_RD3
AR39	RGMII13_Rx_Ctrl	AT34	RGMII13_TD3	AU29	RGMII12_TD0
AT1	VDD_OUT25_21	AT35	RGMII13_Tx_Clk	AU30	VSS_143
AT2	VSS_112	AT36	VSS_6	AU31	RTBI12_SigDet
AT3	RGMII6_TD2	AT37	RGMII13_RD2	AU32	RGMII12_RD2
AT4	VSS_111	AT38	VSS_5	AU33	VSS_145
AT5	RGMII6_Tx_Ctrl	AT39	VDD_IN_21	AU34	RGMII13_TD2
AT6	RGMII6_RD1	AU1	VSS_116	AU35	VSS_146
AT7	RGMII6_Rx_Clk	AU2	VSS_115	AU36	RTBI13_SigDet
AT8	VDD_OUT25_24	AU3	VSS_114	AU37	VSS_4
AT9	RGMII7_Tx_Ctrl	AU4	VDD_OUT25_22	AU38	VSS_3
AT10	RGMII7_RD0	AU5	VSS_113	AU39	VSS_2
AT11	RGMII7_RD3	AU6	RGMII6_RD2	AV1	VSS_120
AT12	RGMII8_TD0	AU7	VSS_124	AV2	RGMII6_TD3
AT13	RGMII8_TD3	AU8	RGMII7_TD2	AV3	VSS_119
AT14	RTBI8_SigDet	AU9	RGMII7_Tx_Clk	AV4	VSS_118
AT15	RGMII8_RD2	AU10	VSS_126	AV5	VSS_117
AT16	RGMII9_TD0	AU11	RGMII7_Rx_Ctrl	AV6	VDD_IN_14
AT17	RGMII9_TD2	AU12	RGMII8_TD1	AV7	RGMII7_TD0
AT18	RGMII9_Tx_Clk	AU13	VSS_129	AV8	VDD_OUT25_23
AT19	RGMII9_RD2	AU14	RGMII8_RD0	AV9	RTBI7_SigDet
AT20	RGMII9_Rx_Clk	AU15	VDD_IN_16	AV10	RGMII7_RD2

Table 160. Signal List by Ball Number (cont'd)

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
AV11	RGMII7_Rx_Clk	AV34	VDD_OUT25_35	AW18	RGMII9_RD1
AV12	VDD_OUT25_25	AV35	RGMII13_Tx_Ctrl	AW19	RGMII9_RD3
AV13	RGMII8_Tx_Ctrl	AV36	VSS_148	AW20	VSS_134
AV14	RGMII8_RD1	AV37	VSS_149	AW21	RGMII10_TD3
AV15	RGMII8_RD3	AV38	RGMII13_RD1	AW22	RGMII10_RD0
AV16	RGMII9_TD1	AV39	VSS_1	AW23	VSS_136
AV17	RGMII9_Tx_Ctrl	AW1	VSS_121	AW24	RGMII10_RD3
AV18	RGMII9_RD0	AW2	VSS_122	AW25	RGMII11_TD2
AV19	VDD_IN_17	AW3	VSS_123	AW26	VSS_139
AV20	RGMII10_TD1	AW4	RGMII6_Tx_Clk	AW27	RTBI11_SigDet
AV21	RGMII10_TD2	AW5	RGMII6_RD0	AW28	RGMII11_RD2
AV22	RTBI10_SigDet	AW6	RGMII6_RD3	AW29	VSS_142
AV23	RGMII10_RD1	AW7	RGMII7_TD1	AW30	VDD_OUT25_33
AV24	RGMII10_Rx_Ctrl	AW8	VSS_125	AW31	VDD_OUT25_34
AV25	VDD_OUT25_31	AW9	RGMII7_RD1	AW32	VSS_144
AV26	RGMII11_TD3	AW10	VDD_IN_15	AW33	RGMII12_Rx_Ctrl
AV27	RGMII11_RD0	AW11	VSS_128	AW34	RGMII13_TD1
AV28	VDD_IN_19	AW12	RGMII8_TD2	AW35	VSS_147
AV29	RGMII11_Rx_Clk	AW13	VDD_OUT25_26	AW36	VDD_OUT25_36
AV30	RGMII12_TD2	AW14	VSS_130	AW37	VSS_150
AV31	RGMII12_Tx_Clk	AW15	RGMII8_Rx_Ctrl	AW38	VSS_151
AV32	RGMII12_RD1	AW16	VDD_OUT25_27	AW39	VSS_0
AV33	RGMII12_Rx_Clk	AW17	VSS_132		

Signal List By Signal Name

Table 161 lists the signals by signal name.

Table 161. Signal List by Signal Name

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
Clk	Y37	PI_Data2	E38	Reserved_12	AB37
Clk125_En	A25	PI_Data3	D39	Reserved_13	AB38
GPIO1	D21	PI_Data4	D37	Reserved_14	AB39
GPIO2	A21	PI_Data5	E34	Reserved_15	W38
GPIO3	E20	PI_Data6	D35	Reserved_16	W39
GPIO4	D20	PI_Data7	C36	Reserved_17	V36
JTAG_nTRST	D23	PI_Data8	D34	Reserved_18	V37
JTAG_TCK	B24	PI_Data9	A36	Reserved_19	V38
JTAG_TDI	A24	PI_Data10	A35	Reserved_20	U36
JTAG_TDO	B23	PI_Data11	A34	Reserved_21	U37
JTAG_TMS	C23	PI_Data12	D33	Reserved_22	U38
MDC_0	D19	PI_Data13	B33	Reserved_23	T35
MDC_1	A18	PI_Data14	A33	Reserved_24	T38
MDIO_0	B20	PI_Data15	D32	Reserved_25	T39
MDIO_1	A19	PI_IRQ	B32	Reserved_26	R36
nReset	C25	PI_nCS	C31	Reserved_27	R37
PI_Addr0	A31	PI_nDone	C32	Reserved_28	R38
PI_Addr1	D30	PI_nOE	B31	Reserved_29	R39
PI_Addr2	B30	PI_nWR	D31	Reserved_30	P36
PI_Addr3	A30	PLL_Cap0	AA38	Reserved_31	P37
PI_Addr4	D29	PLL_Cap1	AA39	Reserved_32	P38
PI_Addr5	C29	PLL_En	D25	Reserved_33	N38
PI_Addr6	B29	Reserved_0	Y38	Reserved_34	N39
PI_Addr7	D28	Reserved_1	C20	Reserved_35	M36
PI_Addr8	C28	Reserved_2	AE36	Reserved_36	M37
PI_Addr9	A28	Reserved_3	AE37	Reserved_37	M38
PI_Addr10	D27	Reserved_4	AE39	Reserved_38	L36
PI_Addr11	B27	Reserved_5	AD35	Reserved_39	L37
PI_Addr12	A27	Reserved_6	AD36	Reserved_40	L38
PI_Addr13	D26	Reserved_7	AD39	Reserved_41	K35
PI_Addr14	C26	Reserved_8	AC36	Reserved_42	K36
PI_Addr15	B26	Reserved_9	AC37	Reserved_43	K39
PI_Data0	F38	Reserved_10	AC38	Reserved_44	J36
PI_Data1	F39	Reserved_11	AB35	Reserved_45	J37

Table 161. Signal List by Signal Name (cont'd)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
Reserved_46	J39	Reserved_80	C9	RGMII0_TD2	J4
Reserved_47	H36	Reserved_81	D9	RGMII0_TD3	J3
Reserved_48	H37	Reserved_82	B8	RGMII0_Tx_Clk	K4
Reserved_49	H38	Reserved_83	C8	RGMII0_Tx_Ctrl	J2
Reserved_50	G36	Reserved_84	D8	RGMII1_RD0	R1
Reserved_51	G39	Reserved_85	B7	RGMII1_RD1	T1
Reserved_52	F36	Reserved_86	C7	RGMII1_RD2	T2
Reserved_53	F37	Reserved_87	D7	RGMII1_RD3	T4
Reserved_54	B18	Reserved_88	A6	RGMII1_Rx_Clk	U3
Reserved_55	C18	Reserved_89	B6	RGMII1_Rx_Ctrl	U2
Reserved_56	B17	Reserved_90	D6	RGMII1_TD0	N1
Reserved_57	C17	Reserved_91	E6	RGMII1_TD1	N2
Reserved_58	D17	Reserved_92	B5	RGMII1_TD2	P2
Reserved_59	B16	Reserved_93	D5	RGMII1_TD3	P3
Reserved_60	D16	Reserved_94	A4	RGMII1_Tx_Clk	R3
Reserved_61	A15	Reserved_95	B2	RGMII1_Tx_Ctrl	P4
Reserved_62	B15	Reserved_96	D3	RGMII10_RD0	AW22
Reserved_63	C15	Reserved_97	D1	RGMII10_RD1	AV23
Reserved_64	B14	Reserved_98	E4	RGMII10_RD2	AT23
Reserved_65	C14	Reserved_99	E2	RGMII10_RD3	AW24
Reserved_66	D14	Reserved_100	F4	RGMII10_Rx_Clk	AT24
Reserved_67	A13	Reserved_101	F3	RGMII10_Rx_Ctrl	AV24
Reserved_68	B13	Reserved_102	F2	RGMII10_TD0	AU20
Reserved_69	A12	Reserved_103	G4	RGMII10_TD1	AV20
Reserved_70	B12	Reserved_104	G2	RGMII10_TD2	AV21
Reserved_71	C12	Reserved_105	G1	RGMII10_TD3	AW21
Reserved_72	B11	RGMII0_RD0	K1	RGMII10_Tx_Clk	AR22
Reserved_73	C11	RGMII0_RD1	L3	RGMII10_Tx_Ctrl	AU22
Reserved_74	D11	RGMII0_RD2	L2	RGMII11_RD0	AV27
Reserved_75	A10	RGMII0_RD3	M3	RGMII11_RD1	AT27
Reserved_76	B10	RGMII0_Rx_Clk	M1	RGMII11_RD2	AW28
Reserved_77	E10	RGMII0_Rx_Ctrl	M2	RGMII11_RD3	AU28
Reserved_78	A9	RGMII0_TD0	H4	RGMII11_Rx_Clk	AV29
Reserved_79	B9	RGMII0_TD1	H3	RGMII11_Rx_Ctrl	AT28

Table 161. Signal List by Signal Name (cont'd)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
RGMII11_TD0	AU25	RGMII14_Rx_Clk	AK38	RGMII3_RD2	AE1
RGMII11_TD1	AT25	RGMII14_Rx_Ctrl	AL39	RGMII3_RD3	AE3
RGMII11_TD2	AW25	RGMII14_TD0	AP37	RGMII3_Rx_Clk	AF2
RGMII11_TD3	AV26	RGMII14_TD1	AP38	RGMII3_Rx_Ctrl	AE4
RGMII11_Tx_Clk	AR26	RGMII14_TD2	AM35	RGMII3_TD0	AB2
RGMII11_Tx_Ctrl	AU26	RGMII14_TD3	AN36	RGMII3_TD1	AB3
RGMII12_RD0	AT31	RGMII14_Tx_Clk	AM36	RGMII3_TD2	AB5
RGMII12_RD1	AV32	RGMII14_Tx_Ctrl	AN38	RGMII3_TD3	AC2
RGMII12_RD2	AU32	RGMII15_RD0	AG36	RGMII3_Tx_Clk	AD1
RGMII12_RD3	AR32	RGMII15_RD1	AG38	RGMII3_Tx_Ctrl	AC3
RGMII12_Rx_Clk	AV33	RGMII15_RD2	AG39	RGMII4_RD0	AH4
RGMII12_Rx_Ctrl	AW33	RGMII15_RD3	AF36	RGMII4_RD1	AJ2
RGMII12_TD0	AU29	RGMII15_Rx_Clk	AF38	RGMII4_RD2	AJ3
RGMII12_TD1	AT29	RGMII15_Rx_Ctrl	AF37	RGMII4_RD3	AK1
RGMII12_TD2	AV30	RGMII15_TD0	AK39	RGMII4_Rx_Clk	AK4
RGMII12_TD3	AT30	RGMII15_TD1	AJ36	RGMII4_Rx_Ctrl	AK2
RGMII12_Tx_Clk	AV31	RGMII15_TD2	AJ38	RGMII4_TD0	AF3
RGMII12_Tx_Ctrl	AR30	RGMII15_TD3	AH35	RGMII4_TD1	AF4
RGMII13_RD0	AR35	RGMII15_Tx_Clk	AH38	RGMII4_TD2	AG1
RGMII13_RD1	AV38	RGMII15_Tx_Ctrl	AH36	RGMII4_TD3	AG2
RGMII13_RD2	AT37	RGMII2_RD0	Y2	RGMII4_Tx_Clk	AH2
RGMII13_RD3	AR36	RGMII2_RD1	Y3	RGMII4_Tx_Ctrl	AG4
RGMII13_Rx_Clk	AP36	RGMII2_RD2	Y4	RGMII5_RD0	AN2
RGMII13_Rx_Ctrl	AR39	RGMII2_RD3	AA2	RGMII5_RD1	AN4
RGMII13_TD0	AT33	RGMII2_Rx_Clk	AB1	RGMII5_RD2	AP1
RGMII13_TD1	AW34	RGMII2_Rx_Ctrl	AA4	RGMII5_RD3	AR2
RGMII13_TD2	AU34	RGMII2_TD0	U4	RGMII5_Rx_Clk	AP4
RGMII13_TD3	AT34	RGMII2_TD1	V1	RGMII5_Rx_Ctrl	AP3
RGMII13_Tx_Clk	AT35	RGMII2_TD2	V3	RGMII5_TD0	AK5
RGMII13_Tx_Ctrl	AV35	RGMII2_TD3	V4	RGMII5_TD1	AL1
RGMII14_RD0	AM38	RGMII2_Tx_Clk	W2	RGMII5_TD2	AL3
RGMII14_RD1	AL36	RGMII2_Tx_Ctrl	V5	RGMII5_TD3	AL4
RGMII14_RD2	AL37	RGMII3_RD0	AD4	RGMII5_Tx_Clk	AM4
RGMII14_RD3	AL38	RGMII3_RD1	AD5	RGMII5_Tx_Ctrl	AM2

Table 161. Signal List by Signal Name (cont'd)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
RGMII6_RD0	AW5	RGMII8_Tx_Clk	AR14	Test_Mode	B25
RGMII6_RD1	AT6	RGMII8_Tx_Ctrl	AV13	VDD_0	AK35
RGMII6_RD2	AU6	RGMII9_RD0	AV18	VDD_1	AJ35
RGMII6_RD3	AW6	RGMII9_RD1	AW18	VDD_2	AG35
RGMII6_Rx_Clk	AT7	RGMII9_RD2	AT19	VDD_3	AE35
RGMII6_Rx_Ctrl	AR8	RGMII9_RD3	AW19	VDD_4	AC35
RGMII6_TD0	AP5	RGMII9_Rx_Clk	AT20	VDD_5	AA35
RGMII6_TD1	AR4	RGMII9_Rx_Ctrl	AR20	VDD_6	W35
RGMII6_TD2	AT3	RGMII9_TD0	AT16	VDD_7	U35
RGMII6_TD3	AV2	RGMII9_TD1	AV16	VDD_8	R35
RGMII6_Tx_Clk	AW4	RGMII9_TD2	AT17	VDD_9	N35
RGMII6_Tx_Ctrl	AT5	RGMII9_TD3	AU17	VDD_10	L35
RGMII7_RD0	AT10	RGMII9_Tx_Clk	AT18	VDD_11	J35
RGMII7_RD1	AW9	RGMII9_Tx_Ctrl	AV17	VDD_12	H35
RGMII7_RD2	AV10	RTBI0_SigDet	K2	VDD_13	G35
RGMII7_RD3	AT11	RTBI1_SigDet	R2	VDD_14	E35
RGMII7_Rx_Clk	AV11	RTBI10_SigDet	AV22	VDD_15	E33
RGMII7_Rx_Ctrl	AU11	RTBI11_SigDet	AW27	VDD_16	E31
RGMII7_TD0	AV7	RTBI12_SigDet	AU31	VDD_17	E30
RGMII7_TD1	AW7	RTBI13_SigDet	AU36	VDD_18	E29
RGMII7_TD2	AU8	RTBI14_SigDet	AM37	VDD_19	E27
RGMII7_TD3	AR9	RTBI15_SigDet	AH39	VDD_20	E26
RGMII7_Tx_Clk	AU9	RTBI2_SigDet	W4	VDD_21	E24
RGMII7_Tx_Ctrl	AT9	RTBI3_SigDet	AD2	VDD_22	E23
RGMII8_RD0	AU14	RTBI4_SigDet	AH3	VDD_23	E21
RGMII8_RD1	AV14	RTBI5_SigDet	AN1	VDD_24	E19
RGMII8_RD2	AT15	RTBI6_SigDet	AR6	VDD_25	E18
RGMII8_RD3	AV15	RTBI7_SigDet	AV9	VDD_26	E17
RGMII8_Rx_Clk	AR16	RTBI8_SigDet	AT14	VDD_27	E16
RGMII8_Rx_Ctrl	AW15	RTBI9_SigDet	AU18	VDD_28	E14
RGMII8_TD0	AT12	SI_Clk	E22	VDD_29	E13
RGMII8_TD1	AU12	SI_DI	C22	VDD_30	E12
RGMII8_TD2	AW12	SI_DO	B22	VDD_31	E9
RGMII8_TD3	AT13	SI_nEn	D22	VDD_32	E7

Table 161. Signal List by Signal Name (cont'd)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
VDD_33	E5	VDD_67	AP35	VDD_OUT25_5	E8
VDD_34	G5	VDD_IN_0	G38	VDD_OUT25_6	A8
VDD_35	J5	VDD_IN_1	B34	VDD_OUT25_7	F5
VDD_36	K5	VDD_IN_2	B28	VDD_OUT25_8	C4
VDD_37	L4	VDD_IN_3	B21	VDD_OUT25_9	H2
VDD_38	L5	VDD_IN_4	D15	VDD_OUT25_10	J1
VDD_39	N5	VDD_IN_5	D10	VDD_OUT25_11	N4
VDD_40	R4	VDD_IN_6	C6	VDD_OUT25_12	P5
VDD_41	R5	VDD_IN_7	F1	VDD_OUT25_13	V2
VDD_42	U5	VDD_IN_8	M4	VDD_OUT25_14	W1
VDD_43	W5	VDD_IN_9	T5	VDD_OUT25_15	AB4
VDD_44	AA5	VDD_IN_10	AA1	VDD_OUT25_16	AC4
VDD_45	AC5	VDD_IN_11	AE2	VDD_OUT25_17	AF5
VDD_46	AE5	VDD_IN_12	AJ4	VDD_OUT25_18	AH1
VDD_47	AG5	VDD_IN_13	AP2	VDD_OUT25_19	AL2
VDD_48	AJ5	VDD_IN_14	AV6	VDD_OUT25_20	AM3
VDD_49	AM5	VDD_IN_15	AW10	VDD_OUT25_21	AT1
VDD_50	AN5	VDD_IN_16	AU15	VDD_OUT25_22	AU4
VDD_51	AR7	VDD_IN_17	AV19	VDD_OUT25_23	AV8
VDD_52	AR10	VDD_IN_18	AU23	VDD_OUT25_24	AT8
VDD_53	AR12	VDD_IN_19	AV28	VDD_OUT25_25	AV12
VDD_54	AR13	VDD_IN_20	AT32	VDD_OUT25_26	AW13
VDD_55	AR15	VDD_IN_21	AT39	VDD_OUT25_27	AW16
VDD_56	AR17	VDD_IN_22	AK36	VDD_OUT25_28	AR18
VDD_57	AR19	VDD_IN_23	AF35	VDD_OUT25_29	AT21
VDD_58	AR21	VDD_IN_24	AB36	VDD_OUT25_30	AT22
VDD_59	AR23	VDD_IN_25	W36	VDD_OUT25_31	AV25
VDD_60	AR24	VDD_IN_26	T36	VDD_OUT25_32	AT26
VDD_61	AR27	VDD_IN_27	M39	VDD_OUT25_33	AW30
VDD_62	AR29	VDD_OUT25_0	B19	VDD_OUT25_34	AW31
VDD_63	AR31	VDD_OUT25_1	D18	VDD_OUT25_35	AV34
VDD_64	AR33	VDD_OUT25_2	A16	VDD_OUT25_36	AW36
VDD_65	AR34	VDD_OUT25_3	D13	VDD_OUT25_37	AP39
VDD_66	AN35	VDD_OUT25_4	D12	VDD_OUT25_38	AN39

Table 161. Signal List by Signal Name (cont'd)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
VDD_OUT25_39	AJ37	VSS_17	AC39	VSS_51	E28
VDD_OUT25_40	AH37	VSS_18	AA37	VSS_52	C27
VDD_OUT25_41	AE38	VSS_19	Y35	VSS_53	A26
VDD_OUT25_42	AD38	VSS_20	Y39	VSS_54	E25
VDD_OUT25_43	V35	VSS_21	W37	VSS_55	C24
VDD_OUT25_44	V39	VSS_22	U39	VSS_56	A23
VDD_OUT25_45	P35	VSS_23	T37	VSS_57	C21
VDD_OUT25_46	N36	VSS_24	P39	VSS_58	A20
VDD_OUT25_47	K38	VSS_25	N37	VSS_59	C19
VDD_OUT25_48	J38	VSS_26	M35	VSS_60	A17
VDD_OUT33_0	B38	VSS_27	L39	VSS_61	C16
VDD_OUT33_1	E36	VSS_28	K37	VSS_62	E15
VDD_OUT33_2	C34	VSS_29	H39	VSS_63	A14
VDD_OUT33_3	E32	VSS_30	G37	VSS_64	C13
VDD_OUT33_4	A22	VSS_31	F35	VSS_65	E11
VDD_PLL	Y36	VSS_32	E37	VSS_66	A11
VDD_Probe	D24	VSS_33	E39	VSS_67	C10
VSS_0	AW39	VSS_34	D36	VSS_68	A7
VSS_1	AV39	VSS_35	D38	VSS_69	C5
VSS_2	AU39	VSS_36	C35	VSS_70	A5
VSS_3	AU38	VSS_37	C37	VSS_71	B4
VSS_4	AU37	VSS_38	C38	VSS_72	E3
VSS_5	AT38	VSS_39	C39	VSS_73	B3
VSS_6	AT36	VSS_40	B35	VSS_74	A3
VSS_7	AR37	VSS_41	B36	VSS_75	A2
VSS_8	AR38	VSS_42	B37	VSS_76	E1
VSS_9	AN37	VSS_43	B39	VSS_77	A1
VSS_10	AM39	VSS_44	A37	VSS_78	B1
VSS_11	AL35	VSS_45	A38	VSS_79	C3
VSS_12	AK37	VSS_46	A39	VSS_80	C2
VSS_13	AJ39	VSS_47	C33	VSS_81	C1
VSS_14	AG37	VSS_48	A32	VSS_82	D4
VSS_15	AF39	VSS_49	C30	VSS_83	D2
VSS_16	AD37	VSS_50	A29	VSS_84	G3

Table 161. Signal List by Signal Name (cont'd)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
VSS_85	H5	VSS_108	AR5	VSS_131	AU16
VSS_86	H1	VSS_109	AR3	VSS_132	AW17
VSS_87	K3	VSS_110	AR1	VSS_133	AU19
VSS_88	L1	VSS_111	AT4	VSS_134	AW20
VSS_89	M5	VSS_112	AT2	VSS_135	AU21
VSS_90	N3	VSS_113	AU5	VSS_136	AW23
VSS_91	P1	VSS_114	AU3	VSS_137	AU24
VSS_92	T3	VSS_115	AU2	VSS_138	AR25
VSS_93	U1	VSS_116	AU1	VSS_139	AW26
VSS_94	W3	VSS_117	AV5	VSS_140	AU27
VSS_95	Y5	VSS_118	AV4	VSS_141	AR28
VSS_96	Y1	VSS_119	AV3	VSS_142	AW29
VSS_97	AA3	VSS_120	AV1	VSS_143	AU30
VSS_98	AC1	VSS_121	AW1	VSS_144	AW32
VSS_99	AD3	VSS_122	AW2	VSS_145	AU33
VSS_100	AF1	VSS_123	AW3	VSS_146	AU35
VSS_101	AG3	VSS_124	AU7	VSS_147	AW35
VSS_102	AH5	VSS_125	AW8	VSS_148	AV36
VSS_103	AJ1	VSS_126	AU10	VSS_149	AV37
VSS_104	AK3	VSS_127	AR11	VSS_150	AW37
VSS_105	AL5	VSS_128	AW11	VSS_151	AW38
VSS_106	AM1	VSS_129	AU13	VSS_PLL	AA36
VSS_107	AN3	VSS_130	AW14		

ELECTRICAL SPECIFICATIONS

Unless otherwise noted, the DC and AC electrical specifications in this section are guaranteed over process, recommended supply voltage.

General Electrical Specifications

The recommended operating conditions are listed in Table 162, and the absolute maximum ratings are listed in Table 163.

Table 162. Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit
Supply Voltage:				
V_{DD}	+1.70	+1.80	+1.90	V
V_{DD_OUT33}	+3.13	+3.30	+3.47	V
V_{DD_OUT25}	+2.37	+2.50	+2.63	V
V_{DD_IN}	+2.37	+2.50	+2.63	V
V_{DD_PLL}	+2.37	+2.50	+2.63	V
Operating Temperature [1]	0	—	TBD	°C
Note 1: Lower limit of specification is ambient temperature and upper limit is case temperature.				

Table 163. Absolute Maximum Ratings

Parameter	Min	Typical	Max	Unit
Supply Voltage:				
V_{DD}	–0.5	—	TBD	V
V_{DD_OUT33}	–0.5	—	TBD	V
V_{DD_OUT25}	–0.5	—	TBD	V
V_{DD_IN}	–0.5	—	TBD	V
V_{DD_PLL}	–0.5	—	TBD	V
DC Input Voltage:				
5 V Tolerant I/Os	–0.5	—	TBD	V
Non 5 V Tolerant I/Os	–0.5	—	TBD	V
Voltage Applied to an Output in High-Impedance State	–0.5	—	TBD	V
Power Dissipation	—	3.2	TBD	W
Temperature:				
Storage	–65	—	+150	°C

Table 163. Absolute Maximum Ratings (cont'd)

Parameter	Min	Typical	Max	Unit
ESD (Human Body Model)	—	—	±500	V
Note: Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.				

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

Power Sequencing

The following must be observed at all times including power up and down.

VDD_OUT25 < VDD_IN + 1.35 V

VDD_OUT33 < VDD_IN + 1.35 V

VDD_PLL < VDD_IN + 0.5 V

The nReset input should be held low until all power supply voltages have reached their recommended operating condition values.

DC Electrical Characteristics

DC Specifications for Clk Signal

The reference clk is a single ended LVTTL input.

Table 164. DC Specifications for Clk

Symbol	Parameter	Conditions		Min	Max	Unit
		Supply	Input/Output			
V_{IH}	Input high voltage	—	—	2.0	3.6	V
V_{IL}	Input low voltage	—	—	–0.3	0.80	V
I_{IH}	Input high current	V_{DD_IN} = min	V_I = 3.3 V	—	280	µA
I_{IL}	Input low current	V_{DD_IN} = max	V_I = 0.0 V	–210	—	µA

DC Specifications for RGMII and RTBI

The outputs and inputs of the RGMII and RTBI interfaces meet or exceed the requirements in the JEDEC JESD8-5 2.5V CMOS interface except for the input leakage current in low state. All RGMII and RTBI and outputs and inputs comply with the specifications in Table 165.

Table 165. DC Specifications for RGMII and RTBI

Symbol	Parameter	Conditions		Min	Max	Unit
		Supply	Input/Output			
V_{OH}	Output high voltage	V_{DD_OUT25} = min	I_{OH} = –1.0 mA	2.0	—	V
V_{OL}	Output low voltage	V_{DD_OUT25} = min	I_{OL} = 1.0 mA	—	0.40	V
V_{IH}	Input high voltage	—	—	1.70	3.0	V
V_{IL}	Input low voltage	—	—	–0.3	0.70	V
I_{IH}	Input current	V_{DD_IN} = max	VI = V_{DD_IN}	—	5	µA
I_{IL}	Input low current	V_{DD_IN} = max	VI = 0.0 V	–75	—	µA

DC Specifications for MII Management

The outputs and inputs of the MII Management interfaces meet or exceed the requirements in the JEDEC JESD8-5 2.5V CMOS interface with the added benefit of 5 V input tolerance. All MIIM outputs and inputs comply with the specifications in Table 166.

Table 166. DC Specifications for MII Management

Symbol	Parameter	Conditions		Min	Max	Unit
		Supply	Input/Output			
V_{OH}	Output high voltage	V_{DD_OUT25} = min	I_{OH} = –1.0 mA	2.0	—	V
V_{OL}	Output low voltage	V_{DD_OUT25} = min	I_{OL} = 1.0 mA	—	0.40	V
V_{IH}	Input high voltage	—	—	1.70	5.5	V
V_{IL}	Input low voltage	—	—	–0.3	0.70	V
I_{IH}	Input current	V_{DD_IN} = max	V_I = V_{DD_IN}	—	5	µA
I_{IL}	Input low current	V_{DD_IN} = max	V_I = 0.0 V	TBD	—	µA

DC Specifications for PI, SI, JTAG, and Other Control Signals

The outputs and inputs meet or exceed the requirements of the LVTTL and LVCMOS standard, JEDEC JESD8-B (September 1999) standard except for the input leakage current in low state. All outputs and inputs comply with the specifications in Table 167.

Table 167. DC Specifications for PI, SI, JTAG, and Other Control Signals

Symbol	Parameter	Conditions		Min	Max	Unit
		Supply	Input/Output			
V_{OH}	Output high voltage	V_{DD_OUT33} = min	I_{OH} = –100 µA	V_{DD_OUT33} – 0.2	—	V
			I_{OH} = –2 mA	2.4	—	V
V_{OL}	Output low voltage	V_{DD_OUT33} = min	I_{OL} = 100 µA	—	0.20	V
			I_{OL} = 2 mA	—	0.40	V
V_{IH} [1]	Input high voltage	—	—	2.0	3.6 [1]	V
V_{IL}	Input low voltage	—	—	–0.3	0.8	V
I_{IH}	Input high current	V_{DD_IN} = min	V_I = 3.3 V	—	5	µA
I_{IL}	Input low current	V_{DD_IN} = max	V_I = 0.0 V	–75	—	µA
Note 1. V_{IH}(max) = 5.5 V for JTAG input signals.						

The following I/O signals comply with the specifications in Table 167:

Clk125_En	Test_Mode	PI_nWR	SI_Clk	JTAG_nTRST
GPIOx	PI_Addr[15:0]	PI_nOE	SI_DI	JTAG_TCK
nReset	PI_Data[15:0]	PI_nDone	SI_DO	JTAG_TDI
PLL_En	PI_nCS	PI_IRQ	SI_nEn	JTAG_TDO
JTAG_TMS				

Current Consumption

The table below shows the absolute maximum operating current for Heathrow-III, which is found at worst case silicon, minimum operating temperature and maximum power supply.

Table 168. Maximum Operating Current

Symbol	Parameter	Conditions	Max	Unit
I_{DD}	Average active operating current for core	@ V_{DD} = 1.9 V	TBD	mA
I_{DD_OUT25}	Average active operating current for 2.5 V outputs	@ V_{DD_IO25} = 2.63 V	TBD	mA
I_{DD_OUT33}	Average active operating current for 3.3 V outputs	@ V_{DD_IO33} = 3.47 V	TBD	mA
I_{DD_IN}	Average active operating current for inputs	@ V_{DD_IN} = 2.63 V	TBD	mA

Table 168. Maximum Operating Current (cont'd)

Symbol	Parameter	Conditions	Max	Unit
I_{DD_PLL}	Average active operating current for PLL	@ V_{DD_PLL} = 2.63 V	25	mA
Note: All power consumption figures assume 100% TX activity.				

Typical Current Consumption

Table 169 shows typical figures for current consumption for the Heathrow-III chip in various situations. The numbers are measured under typical conditions (process, temperature, and supply voltage).

Table 169. Typical Current Consumption

Supply	Idle [1]	1 Gb/s [2] One Port	Full [3]	Unit
V_{DD} (1.8 V)	TBD	TBD	TBD	mA
V_{DD_OUT25} (2.5 V)	TBD	TBD	TBD	mA
V_{DD_OUT33} (3.3 V)	TBD	TBD	TBD	mA
V_{DD_IN} (2.5 V)	TBD	TBD	TBD	mA
V_{DD_PLL} (2.5 V)	TBD	TBD	TBD	mA

Notes:
1. Idle after reset.
2. Full traffic on one 1 Gb/s port (condition TBD).
3. Full traffic on 16 1 Gb/s ports and the parallel CPU interface.
4. All power consumption figures assume 100% TX activity on the specified ports.

AC Electrical Characteristics

All AC electrical characteristics are guaranteed over worst case to best case silicon, recommended operating temperature, recommended power supply voltages and under the individual load condition given in the following sections.

Clock Timing

The signal applied to the Clk input should comply with the requirements in Table 170 at the pin of the chip.

Table 170. System Clock AC Specifications

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f_{clk}	Nominal Clk frequency	25 MHz input clk	—	25	—	MHz
		125 MHz input clk	—	125	—	MHz
—	Clk frequency tolerance [2]	—	–50	—	+50	ppm
—	Clk duty cycle	@ 0.5 V_{DD_IO33}	30	—	70	%

Table 170. System Clock AC Specifications (cont'd)

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
t_r, t_f	Clk rise/fall time	—	—	—	5	ns

Notes:
1. Typical values are at 25°C.
2. The frequency tolerance of the output clocks of the ports is directly connected to the frequency tolerance on the input clk.

The frequency tolerance of the output clocks of the ports is directly connected to the frequency tolerance on the input clk.

The internal PLL uses the positive going edge; hence this edge has to be clean (for example: free of excess jitter). Any jitter on this edge will be passed to the output clocks.

Reset Timing

Figure 15 shows the nReset signal waveform and required measurement points for the timing specification.

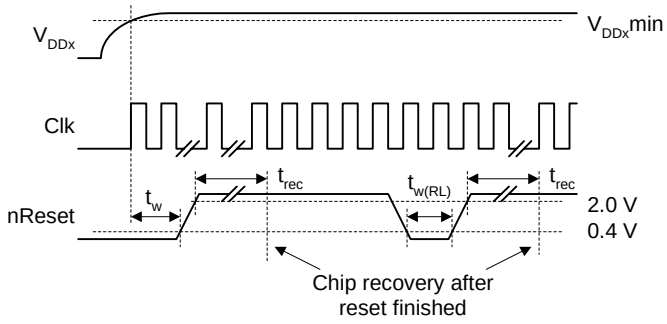


Figure 15. nReset Signal Timing Parameters

The nReset assertion time during power up is measured from when the last of the following happens (all power supplies has reached within valid levels plus Clk signal is stable) to when the nReset signal enters the transition region.

The signal applied to the nReset input should comply with the requirements in Table 171 at the pin of the chip.

Table 171. nReset AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit
t_w	nReset assertion time after all power supplies and clk stable	See Figure 14	10	—	ms
t_{rec}	Recovery time from reset inactive to chip fully active	See Figure 14	—	60	ns
t_w(RL)	Reset pulse width	See Figure 14	20	—	ns

Table 171. nReset AC Specifications (cont'd)

Symbol	Parameter	Conditions	Min	Max	Unit
t_r, t_f	Rise and fall time of nReset	0.8 V to 2.0 V	—	10 [1]	ns
Note 1. Guaranteed by design.					

RGMII (10/100/1000 Mb/s) And RTBI (1000 Mb/s)

All AC specifications for the RGMII and RTBI interfaces meet or exceed the requirements of the HP RGMII/RTBI draft 1.3.

The RGMII and RTBI timing parameters are defined in Figure 16 and Figure 17.

The skew between the clock and the other signals (both Tx and Rx) are defined as the time period between when the signals and when the clock reach the threshold value of 1.25 V. This is a double data rate interface, so both the rising and falling edge of the clock is used.

Figure 16 and Figure 17 show the RGMII and RTBI transmit and receive waveforms and required measurement points for the different signals. All AC timing requirements are specified relative to 1.25 V.

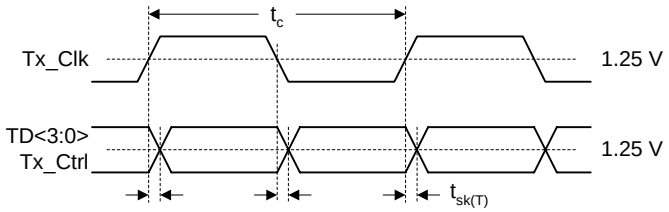


Figure 16. RGMII and RTBI Transmit Waveforms

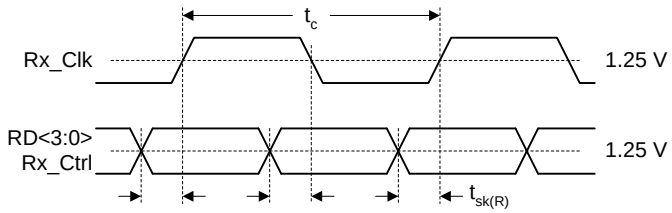


Figure 17. RGMII and RTBI Receive Waveforms

Note: As measured at 'measurement point' in Figure 18.

In RTBI mode, the Rx_Ctrl and Tx_Ctrl becomes respectively RD4 and TD4.

Additionally, in 10/100 RGMII mode, data is duplicated on the falling edge of the clk (no data transitions on the falling clock).

All RGMII and RTBI transmit signals comply with the specifications in Table 172 and Table 173 when measured using the test circuit in Figure 18. All RGMII and RTBI receive signal requirements are requested at the chip pins.

Table 172. RGMII and RTBI 1000 Mb/s AC Specifications

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f	Clk frequency	1000 Mb/s	—	125	—	MHz
—	Clk frequency stability	—	–50	—	+50	ppm
t_c	Clk cycle time	@ 1.25 V	7.2	8	8.8	ns
—	Clk duty cycle	@ 1.25 V	45	50	55	%
t_r	RGMII signal rise time	20 to 80%	—	—	0.75	ns
t_f	RGMII signal fall time	80 to 20%	—	—	0.75	ns
$t_{sk(T)}$ [2]	Data to Clock output skew	@ 1.25 V	–500	0	500	ps
$t_{sk(R)}$	Data to Clock input skew	@ 1.25 V	1	—	2.6	ns

Notes:
1. Typical values are at 25°C.
2. Guaranteed by design.

Table 173. RGMII 10/100 Mb/s AC Specifications

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f	Clk frequency	100 Mb/s	—	25	—	MHz
		10 Mb/s	—	2.5	—	MHz
—	Clk frequency stability	—	–50	—	+50	ppm
t_c	Clk cycle time	100 Mb/s	36	40	44	ns
		10 Mb/s	360	400	440	ns
—	Clk duty cycle	@ 1.25 V	40	50	60	%
t_r	RGMII signal rise time	20 to 80%	—	—	0.75	ns
t_f	RGMII signal fall time	80 to 20%	—	—	0.75	ns
$t_{sk(T)}$ [2]	Data to Clock output skew	@ 1.25 V	–500	0	500	ps
$t_{sk(R)}$	Data to Clock input skew	@ 1.25 V	1	—	—	ns

Notes:
1. Typical values are at 25°C.
2. Guaranteed by design.

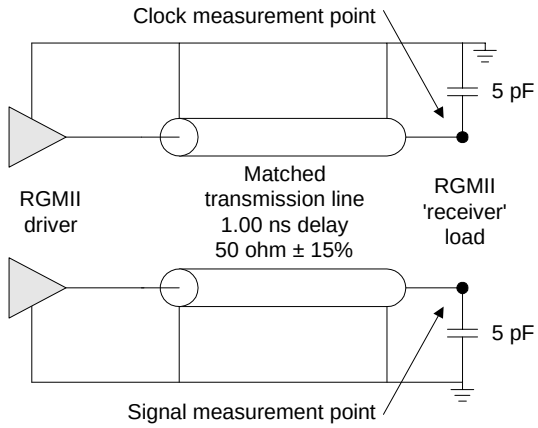


Figure 18. RGMII and RTBI Test Circuit

MII Management

All ac specifications for the MII Management interface has been designed to meet or exceed the requirements of IEEE Std 802.3-2002 (clause 22.2-4).

Figure 19 shows the MII management waveforms and required measurement points for the signals.

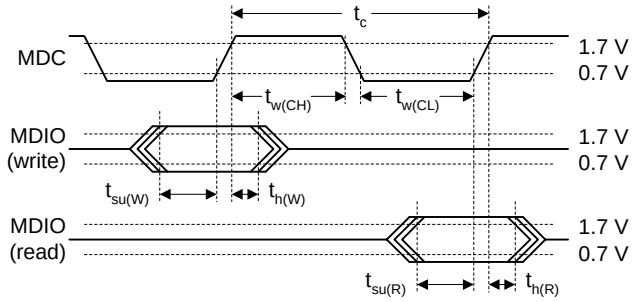


Figure 19. MII Management Waveforms

The setup time of MDIO relative to the rising edge of MDC is defined as the length of time between when the MDIO exits and remains out of the switching region and when MDC enters the switching region. The hold time of MDIO relative to the rising edge of MDC is defined as the length of time between when MDC exits the switching region and when MDIO enters the switching region.

All MII management transmit signals comply with the specifications in Table 174. The MDIO signal requirements are requested at the chip pin.

Table 174. MII Management AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	MDC frequency	—	1	2.5	MHz
t_c	MDC cycle time	—	400	—	ns
$t_{w(CH)}$	MDC time high	C_{load} = 50 pF	160	—	ns
$t_{w(CL)}$	MDC time low	C_{load} = 50 pF	160	—	ns
$t_{su(W)}$	MDIO setup to MDC on write	C_{load} = 50 pF	10	—	ns
$t_{h(W)}$	MDIO hold from MDC on write	C_{load} = 50 pF	10	—	ns
$t_{su(R)}$	MDIO setup to MDC on read	C_{load} = 50 pF on MDC	15	—	ns
$t_{h(R)}$	MDIO hold from MDC on read	See Figure 18	0	—	ns

SI (Serial CPU Interface)

All SI AC timing requirements are specified relative to respectively the input low and high threshold level (0.8 V and 2.0 V).

The SI timing parameters and required measurement points are defined in Figure 20 and Figure 21.

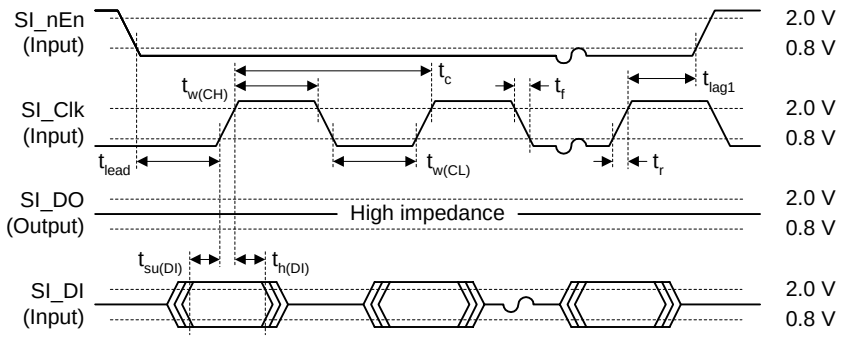


Figure 20. SI Input Data Waveform

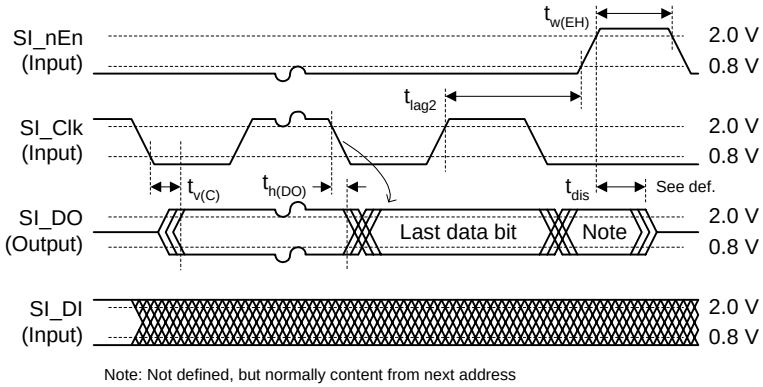


Figure 21. SI Output Data Waveform

All SI signals complies with the specifications in Table 175, and the SI receive signal requirements are requested at the chip pins.

Table 175. SI Interface AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	Clk frequency	—	—	25 [1]	MHz
t_c	Clk cycle time	—	40 [1]	—	ns
$t_{w(CH)}$	Clk time high	—	16	—	ns
$t_{w(CL)}$	Clk time low	—	16	—	ns
t_r, t_f	Clk rise and fall time	Between V_{IL} and V_{IH}	—	10 [2]	ns
$t_{su(DI)}$	DI setup to Clk	—	4	—	ns
$t_{h(DI)}$	DI hold from Clk	—	2	—	ns
t_{lead}	Enable active before first Clk	—	10	—	ns
t_{lag1} [3]	Enable inactive after clk (input cycle)	—	32	—	ns
t_{lag2}	Enable inactive after clk (output cycle)	—	See note[4]	—	ns
$t_{w(EH)}$	Enable inactive width	—	16	—	ns
$t_{v(C)}$	DO valid after Clk	C_L = 30 pF	—	12	ns
$t_{h(DO)}$	DO hold from Clk	C_L = 0 pF	0	—	ns

Table 175. SI Interface AC Specifications (cont'd)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{dis} [5]	DO disable time	See Figure 22	—	15 [5]	ns

Notes:
1. The SI clock frequency may be up to 25 MHz, but if it exceeds 0.5 MHz, dummy bytes must be inserted.
2. Guaranteed by design.
3. t_{lag1} is only defined for write operations to the chip, not read.
4. The last rising edge on the clk is necessary for the master to be able to read in the data. The lag time depend on the necessary hold time on the master data input.
5. The pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

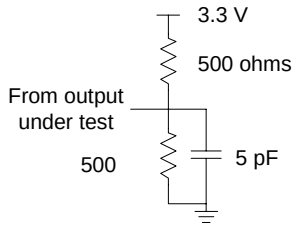
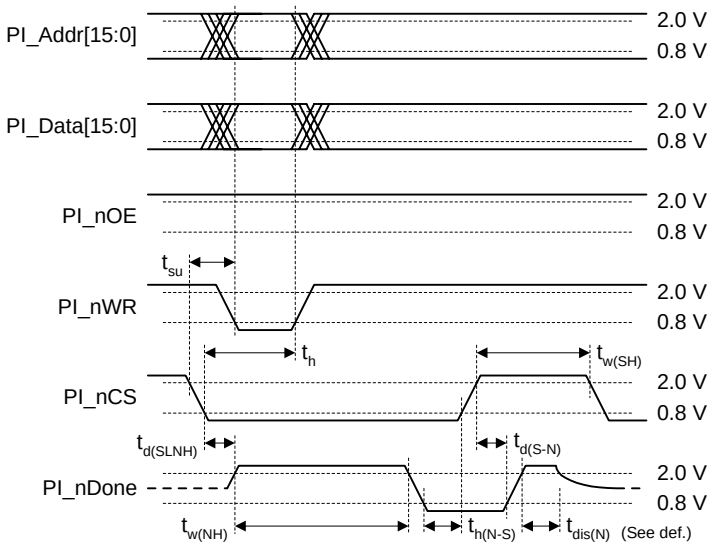


Figure 22. Test Circuit for Signal Disable Test

PI (Parallel CPU Interface)

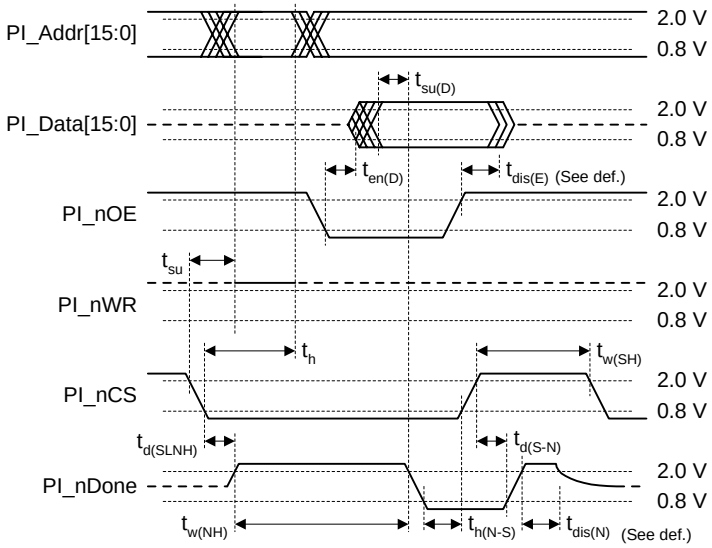
All PI AC timing requirements are specified relative to respectively the input low and high threshold level (0.8 V and 2.0 V).

The PI timing parameters and required measurement points are defined in Figure 23 and Figure 24.



PI_nDone's polarity is programmable, here shown as active low.

Figure 23. PI Write Cycle (Input to Chip)



PI_nDone's polarity is programmable, here shown as active low.

Figure 24. PI Read Cycle Waveforms

All PI signals complies with the specification in Table 176, and the PI receive signal requirements are requested at the chip pins.

Table 176. PI Interface AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit
t_{su}	PI_Addr, PI_Data, PI_nWR setup to PI_nCS falling	PI_Data only on write	–10 [1]	—	ns
t_h	PI_Addr, PI_Data, PI_nWR hold from PI_nCS falling	PI_Data only on write	30 [1]	—	ns
$t_{d(SLNH)}$	Delay from low PI_nCS to rising PI_nDone	—	—	20	ns
$t_{w(NH)}$	Width of PI_nDone high	—	—	30 [1, 2]	ns
$t_{h(N-S)}$	PI_nCS hold from PI_nDone falling	—	0	—	ns
$t_{d(S-N)}$	Delay from PI_nCS rising to PI_nDone rising	—	—	10	ns
$t_{dis(N)}$ [3]	PI_nDone disable time from PI_nDone pulled inactive	See Figure 25	—	12	ns
$t_{w(SH)}$	Width of PI_nCS high	—	15	—	ns
$t_{en(D)}$ [4]	PI_nOE and PI_nCS low to PI_Data enabled	C_L = 50 pF	—	15	ns
$t_{su(D)}$	PI_Data setup to PI_nDone falling on read	—	2	—	ns
$t_{dis(E)}$ [3, 4]	PI_Data disable time from either PI_nCS or PI_nOE high	See Figure 25	—	12	ns

Notes:
1. An initial delay can be added before input data/conditions is sampled. It can be added in steps of 8 ns from 0 ns to 120 ns. Default is 120 ns to ensure operation with slow CPUs, but it is recommended to change this value. Timing in this table is shown with 0 ns delay.
2. When using extended bus cycles, the response time can be up to 550 ns.
3. The pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occur.
4. Internal data output enable requires both PI_nOE and PI_nCS active.

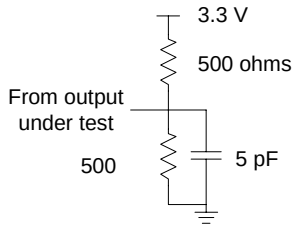


Figure 25. Test Circuit for Signal Disable Test

A reset of the interrupt status signal (PI_IRQ) caused by a read or write will occur simultaneously with the falling edge of PI_nDone, as shown in Figure 26 and Figure 27.

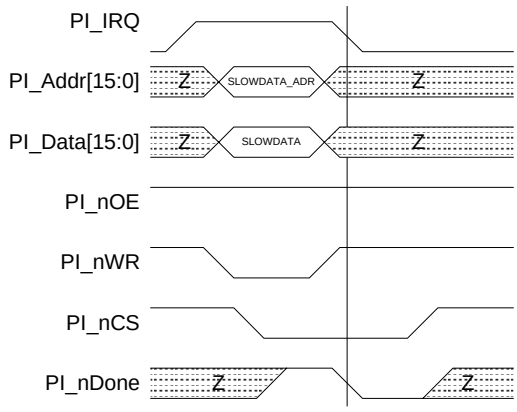


Figure 26. PI Interrupt Write Cycle

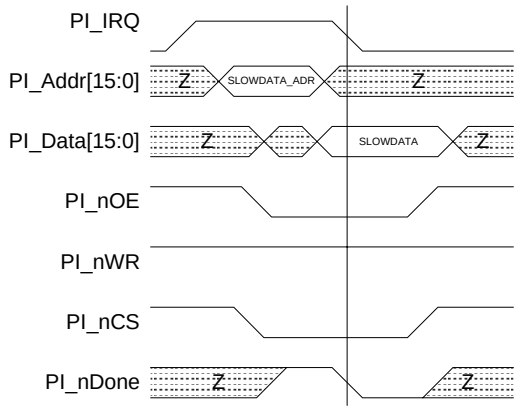


Figure 27. PI Interrupt Read Cycle

JTAG

All AC specifications for the JTAG interface have been designed to meet or exceed the requirements of IEEE Std 1149.1-2001.

Figure 28 shows the JTAG transmit and receive waveforms and required measurement points for the different signals.

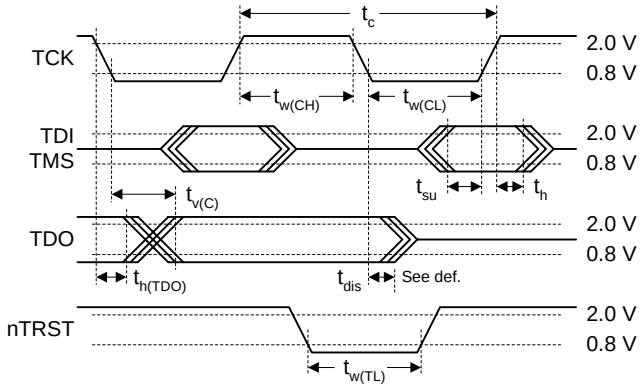


Figure 28. JTAG Interface Timing Definitions

All JTAG signals comply with the specifications in Table 177, and the JTAG receive signal requirements are requested at the chip pin.

Table 177. JTAG AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	TCK frequency	—	—	10	MHz
t_c	TCK cycle time	—	100	—	ns
$t_{w(CH)}$	TCK time high	—	40	—	ns
$t_{w(CL)}$	TCK time low	—	40	—	ns
t_{su}	Setup to TCK rising	See Figure 28	0	—	ns
t_h	Hold from TCK rising	See Figure 28	30	—	ns
$t_{v(C)}$	TDO valid after TCK falling	C_L = 10 pF	—	28	ns
$t_{h(DO)}$	TDO hold from TCK falling	C_L = 0 pF	0	—	ns
t_{dis} [1]	DO disable time	See Figure 29	—	30 [1]	ns
$t_{w(TL)}$	nTRST time low	—	30	—	ns
Note 1: The pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.					

The JTAG_nTRST signal is asynchronous to the clock and consequently does not have a setup and hold time requirement.

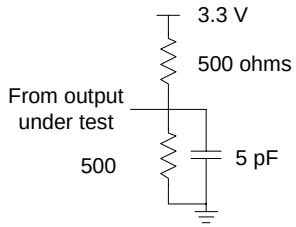


Figure 29. Test Circuit for Signal Disable Test

DESIGN GUIDE

Power Supplies

Power Supply Decoupling

It is important to have the power supplies very well decoupled, because Heathrow-III's signals have short fall/rise times. To make good power supply decoupling, it is recommended that power and ground planes be included in the PCB. The capacitance between the power and ground planes is comparable to that of a capacitor with very low ESR and ESL.

It is recommended that the PCB have at least one solid plane for each power supply: VSS, VDD_OUT25, and VDD. VDD_OUT33 does not need a power plane.

Additionally, make sure that at least the ground plane is not slotted.

In addition to power planes, it is recommended that unused board areas on signal planes be filled with copper and connected to the proper power source to increase the capacitance between the power supplies.

NOTE: *The dielectric material of some capacitors is not well suited for decoupling, because the capacity decreases significantly with increasing DC offset and increasing temperature.*

The following are recommended:

- For each three VDD_OUTx pins, there should be at least one 100 nF decoupling capacitor
- For each ten VDD_OUTx pins, there should be at least one 1 uF decoupling capacitor
- On VDD_OUTx and VDD, there should be at least one 10 uF decoupling capacitor very near Heathrow-III
- For each three VDD pins, there should be at least one 100 nF decoupling capacitor
- For each ten VDD pins, there should be at least one 1 uF decoupling capacitor
- VDD_IN can be made as a plane but this is not required. Because the current flowing in VDD_IN is small, five 100 nF capacitors evenly spread around Heathrow-III are recommended. The VDD_IN supply can be connected to the VDD_OUT25 plane.

The tracks from the power supply pins to the power planes' vias should be as short as possible. Less than 40 mil (1 mm) is recommended.

Core 1.8 V (VDD)

This supply should be made as a plane where all VDD pins are connected.

3.3 V Output Supply (VDD_OUT33)

All VDD_OUT33 pins must be connected to the same power supply.

2.5 V Output Supply (VDD_OUT25)

All VDD_OUT25 pins must be connected to the same power supply.

Input Power Supply (VDD_IN)

All VDD_IN pins must be connected to the same power supply. Normally this plane can be shared with VDD_OUT25.

PLL

PLL Supply Filtering

It is recommended that the two PLL power pins (VDD_PLL, VSS_PLL) be connected to a “quiet” supply. This can be done by low-pass filtering the digital VDD_IN. Remember to connect the VSS_PLL to the filter capacitor first, then to the digital VSS power plane.

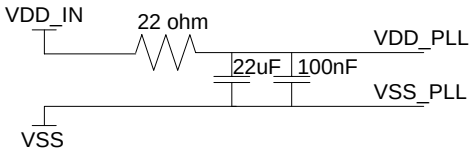


Figure 30. PLL Supply Filtering

PLL Loop Filter Capacitor

The on-chip PLL uses an external 0.1 µF capacitor connected between its Cap0 and Cap1 terminals to control the Loop Filter. This capacitor should be a multilayer ceramic dielectric, or better, with at least a 5 V working voltage rating and a good temperature coefficient. This capacitor is used to minimize the impact of common-mode noise on the Clock Multiplier Unit (especially power supply noise). Higher value capacitors provide better robustness in systems. NPO is preferred but X7R may be acceptable. NPO is preferred over X7R because the power supply noise sensitivity varies with temperature.

For best noise immunity, the designer may choose to use a 3-capacitor circuit with one differential capacitor between Cap0 and Cap1 (C1), a capacitor from Cap0 to ground (C2), and a capacitor from Cap1 to ground (C3). Larger values are better but 0.1 µF is adequate. However, if the designer cannot use a 3-capacitor circuit, a single differential capacitor (C1) is adequate. These components should be isolated from noisy traces.

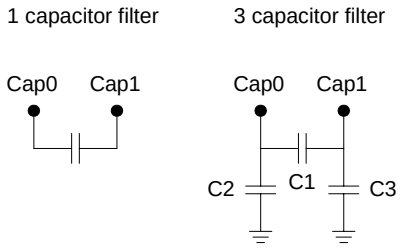


Figure 31. PLL Loop Filter Capacitor

PLL Inputs

The reference clock to Heathrow-III can be either a 25 MHz or a 125 MHz clock. The function is:

CLK125_EN selects 125 MHz clock if high or 25 MHz clock if low.

CLK must be a 25 MHz LVTTL clock when CLK125_EN is low, else a 125 MHz LVTTL clock when CLK125_EN is high. Refer to the ”Termination Considerations” on page 133 for layout recommendations on clock layout. The clock can be supplied from a 2.5 V or 3.3V oscillator/driver.

PLL_EN must be high for normal operation.

Logic high can be supplied from 2.5 V to 3.3 V sources, VDD_0UT25 or VDD_OUT33.

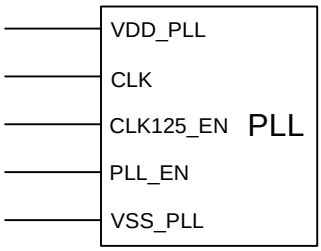


Figure 32. PLL Power and Control Signals

External Pull Resistors

All single ended inputs on Heathrow-III that are unused must have a pull resistor to maintain a stable level. The following signals may need a pull resistor:

Clk125_En	JTAG_TMS	PI_nOE	RGMIIx_Rx_Clk	SI_DI
JTAG_nTRST	nReset	PI_nWR	RGMIIx_Rx_Ctrl	SI_nEn
JTAG_TCK	PI_Addr[15:0]	PLL_En	RTBIx_SigDet	Test_Mode
JTAG_TDI	PI_nCS	RGMIIx_RD[3:0]	SI_Clk	

Interfaces

MII Management

Heathrow-III includes two identical management busses. It is recommended that they are equally loaded and the layout is done very carefully.

It is recommend that the clock signal (MDCx) is routed from Heathrow-III to PHY 1 then PHY 2 then PHY n and then terminated with 120 Ω to ground and 75 Ω to VDD_OUT25. It is also recommended that the PCB trace is routed with as high impedance as possible and at least 68 Ω

MDIOx should have 1.5 kΩ pull-up resistor to 2.5 V, and the trace should follow the MDCx trace. See Figure 33.

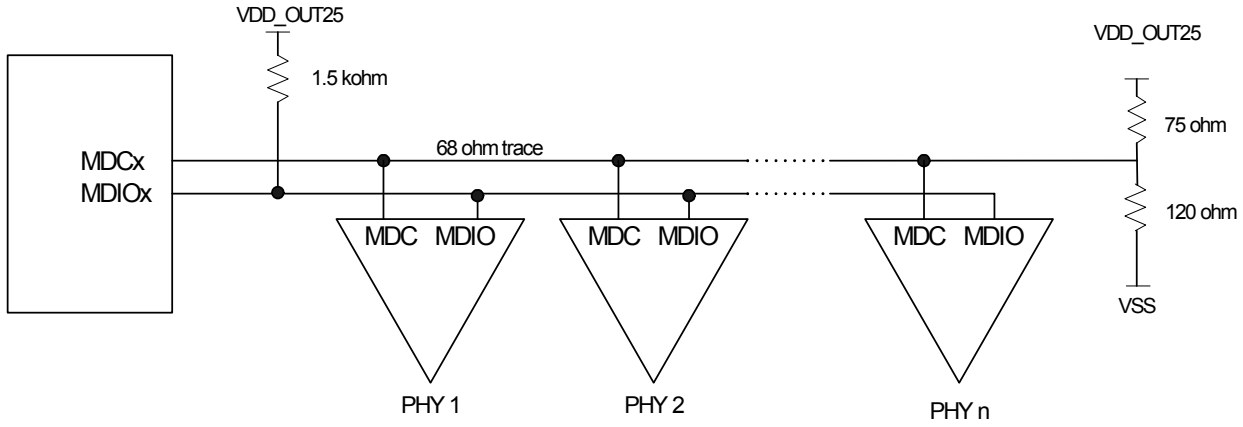


Figure 33. MDC/MDIO Layout Scheme

Care should be taken with respect to the layout guidelines described in the ”Termination Considerations” on page 133.

If it is desired to route the PCB-trace with 50 Ω, it is recommend that a clock driver be used. This driver should be placed close to Heathrow-III. It must be verified against the data sheet that this driver is capable of driving 35 Ω traces. This is because the impedance is lowered when the trace is loaded capacitive-wise by the PHYs. Routing guidelines will be the same as above, and the termination should be equal to the loaded trace impedance (typically 35 Ω).

It also is possible to use individual clock drivers for each PHY, routed in a star configuration.

Parallel CPU Interface (PI)

This interface consists of PI_Addr[15:0], PI_Data[15:0], PI_nCS, PI_nDone, PI_nOE, PI_nWR, and PI_IRQ. If this interface is not used, all signals except PI_IRQ need to be pulled high. PI_Addr[15:0] can be pulled high with a single resistor; PI_Data[15:0] can be pulled high with a single resistor; and the four control signals should have single resistors. When using an 8 bit interface, the unused data bits PI_data[8:15] must individually be pulled high or low with 15 to 20 kΩ resistors.

This interface can be configured either as an 8-bit or a 16-bit interface. If configured as an 8-bit interface, PI_Data[7..0] carries data information and PI_Data[15..8] needs to be pulled (high is preferred). For address mapping using an 8-bit interface, see the ”8-Bit Data Bus Width” on page 50. When using the parallel interface, please note the timing in Table 176: the time $t_{d(SLNH)}$ indicates when an issued command is sampled by Heathrow-III.

If the host CPU is not located close to Heathrow-III, it is recommended that the address and (at least) the control signals are series terminated close to the CPU to avoid crosstalk or malfunction of the interface. For specific values, refer to data for the CPU output driver.

To ensure that the PI_nDone signal is driven inactive properly, add a 4.7 kΩ pull-up resistor to this signal.

Serial CPU Interface (SI)

This interface consists of 4 signals: SI_DO, SI_DI, SI_Clk, and SI_nEn. SI_DO, SI_DI, and SI_Clk can be shared by multiple devices and there must be one SI_nEN separate for each device on the bus. Care should be taken when routing SI_Clk to avoid reflections, or noise from other traces, that causes double clocking of one or more devices on the bus (see the ”Termination Considerations” on page 133 for recommendations).

If this interface not is used, the inputs should be pulled high or low (SI_nEN must be pulled high). For the other three signals, high is recommended.

JTAG Interface

If the JTAG interface is not used, the input pins must be pulled high (inactive) except JTAG_nTRST, which should be pulled to ground. It can either be tied to ground or if JTAG chain is used, a pull down resistor of 2 kΩ maximum should be used. If other JTAG resets must be pulled low in the JTAG chain, a smaller value of the resistor should be used. Consult specific devices for their internal pull resistors.

MAC Interface

The Heathrow-III MAC interfaces can be configured for two modes:

1. RGMII
2. RTBI

The interfaces of all 16 ports can be configured individually for one of the two modes, but the input supply (VDD_IN) and output supply (VDD_OUT25) voltages are shared.

When the RTBI interface is used, it may be a requirement that the reference clock to Heathrow-III is frequency locked to the RTBI PHY’s reference clock. Check with the RTBI PHY’s data sheet.

To reduce the crosstalk between signal and clock (Tx_CLK and Rx_CLK) PCB lines, it is recommended that the spacing on each side of the clock lines be larger than twice the track width. The RGMII/RTBI traces should be kept shorter than 1.8 ns.

If a port is not used, then pull RGMII_Rx_Ctrl low and RGMII_RD[3:0] plus RGMII_Rx_Clk high (or low).

Termination Considerations

MAC Interfaces

All signals in the MAC interface and the reference Clk input (both on VSC7302 and the PHYs), require termination considerations.

All RGMII/RTBI outputs were designed to drive one load and they have built-in series termination optimized for 50 Ω transmission lines.

If any additional termination is added to the RGMII/RTBI output signals, it is recommended that all signals within each port be terminated equally.

All RGMII/RTBI traces should be impedance controlled. The recommended value is 50 Ωto ground plane, but this is not a strict requirement, and the board designer can experiment with different values if needed.

Summary:

- Place series termination resistors, if needed, as close to the output pins as possible
- Keep output traces, between Heathrow-III and one PHY, approximately the same length. Notice the special clk track requirement in RGMII and RTBI mode, if the PHY does not include the clock delay.
- Keep input traces, between one PHY and Heathrow-III, approximately the same length. Notice the special clk track requirement in RGMII and RTBI mode, if the PHY does not include the clock delay.

Other Outputs from Heathrow-III

All other outputs do not have a built-in series termination, and they should be terminated appropriately on board if required.

Other Inputs to Heathrow-III

For recommendations on the termination of input signals to Heathrow-III, refer to the data sheet of the specific devices.

Other Design Information

Signal Reference Plane

In the package, all signals are referenced to the common ground plane (VSS). Therefore, it is recommended that all high-speed signals are referenced to ground or have a low impedance ac return path to ground if referenced to another power supply.

Reference Clock

The reference clock for the VSC7302 and PHYs can be taken from the same oscillator. The reference clock for PHYs must be a low-jitter type and must come from a non-PLL based clock source (including oscillator, buffer, and so forth). A PLL base source clock will disturb the built-in PLL in the PHYs.

PRELIMINARY PACKAGE INFORMATION

Package Outline

All Measurements are in mm
Body Size: 40.00 x 40.00 TSBGA Package
No. of Balls: 680
Ball Pitch: 1.00
Ball Footprint: 38 x 38
A1 Ball Corner Location Indication on Top of Package

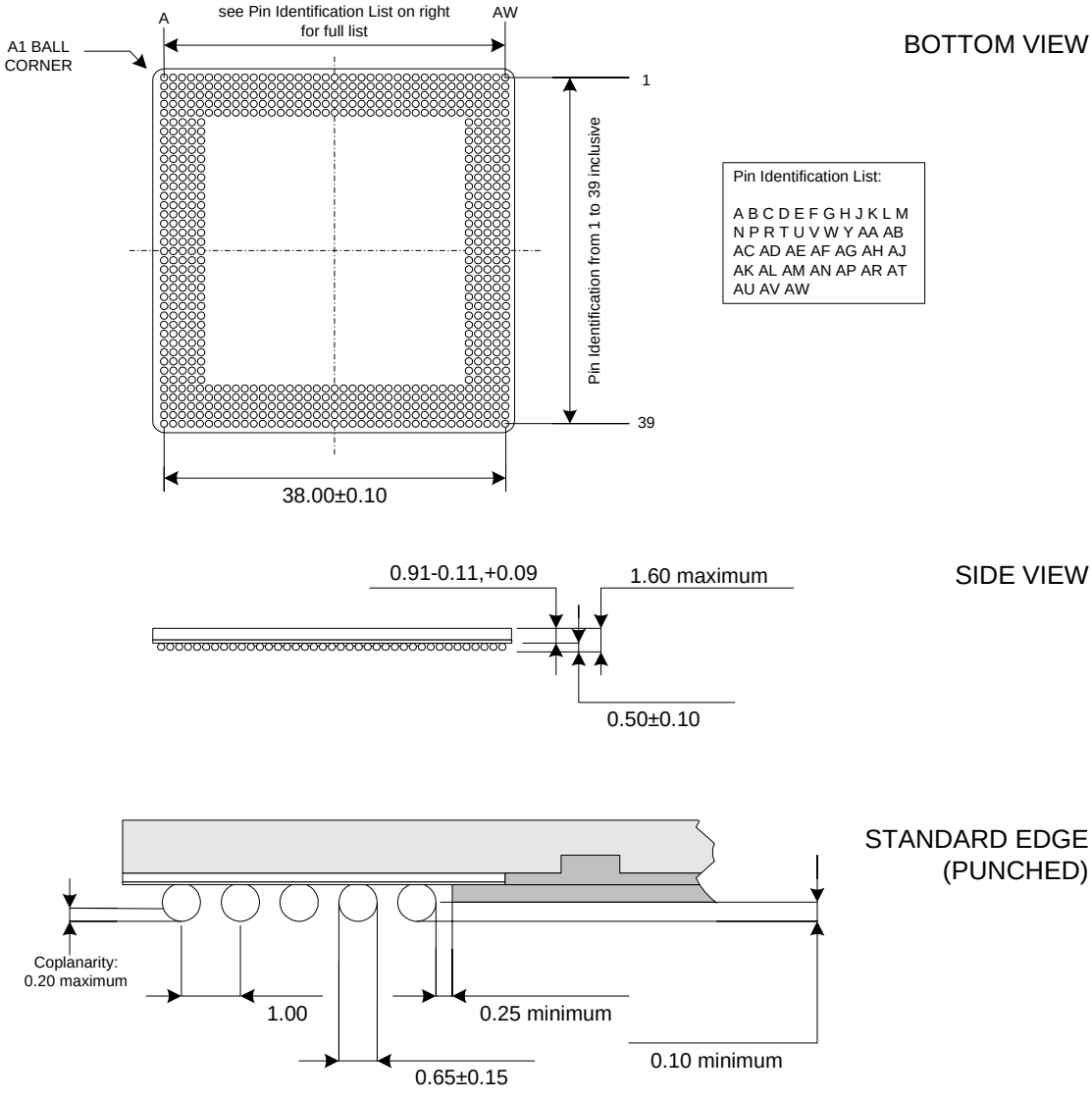


Figure 34. 680-Pin TSBGA Package Information

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 178. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC7302VF	0.1	9.8	8.6	7.2

Moisture Sensitivity Level

This device is rated moisture sensitivity level 3 or better as specified in the JEDEC standard IPC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

ERRATA

Customers should pay particular attention to the layout to ensure that the timing requirements for the RGMII interface are met. Vitesse's field application engineers (FAEs) have extensive experience with optimizing board layouts. Contact Vitesse's FAEs for layout recommendations. They can also review schematics and gerber files to ensure a robust, manufacturable design.

VSC7302 has been released to initial production. 1000 hours of high temperature operating life testing, nominal characterization, the release of a production-level automated test equipment (ATE) test program, and system level validation have been performed. The device will achieve full production release upon completion of full characterization.

The Advance Product Information data sheet is based on simulation and nominal characterization results. The final data sheet will be updated when the device is released to full production.

Item #1: 10/100 Mb/s Full Duplex Flow Control Pause Frames are not Sent on Egress Overloaded Link (2146)

Issue

A port cannot generate pause frames when the egress port is transmitting data at wire speed.

The observation only applies for Ethernet and Fast Ethernet (10/100 Mb/s) operation in Full Duplex with Flow Control enabled.

Implications

Ingress traffic can be lost because the link partner is not paused. This will only occur for ports heavily loaded with traffic in both directions.

Workaround

To make room for pause frames, it is necessary to limit the egress data stream by use of the built-in shaper to ensure loss-free operation. By the use of the shaper, a port can be configured so that transmission of pause frames can be guaranteed. Three different workarounds exist—each one applicable depending on the application:

1) Leave it as it is, which means the shaper is disabled:

All speeds: Device register 0x11: 0x0 (shaper disabled)

Ingress drop is possible in congested scenarios, but throughput in uncongested scenarios will be as high as 100%.

2) A static shaping of the egress ports running 10/100 Mb/s flow control. It is recommended to shape down to ~67% to achieve 0% packet loss. The register settings are:

1Gbps FDX: Device register 0x11: 0x0 (shaper disabled)

10/100Mbps FDX:Device register 0x11: 0x40010550 (shaper bandwidth = 66,4%)

The advantage is zero loss under all circumstances but throughput can never exceed the 67% even in uncongested scenarios.

3) A dynamic adaptive shaper optimization that adjusts the shaper according to traffic by polling registers and counters. In this case, a software routine must monitor the ingress drop counter and upon drops it must shape the egress rate down to ~67%. Hereafter, it can increase the rate until new drops are seen. Then it should maintain the level reached just before drops or decrease the rate until no more drops are seen. When traffic stops (the ingress and egress buffers are empty for a period of time), it must release the shaper.

This workaround combines the benefits of the two previous ones: Traffic will only be shaped when necessary, and throughput will be up to 100% if possible. The disadvantage is that a small momentary ingress drop is inevitable when the shaper kicks in.

If a small initial drop is acceptable, then workaround 3 is superior to the others in terms of performance.

Item #2: The Utilization of a Flow Controlled Link can Drop to Zero (2154)

Issue

The utilization of a link interconnecting two VSC7302 Heathrow-III-based switches can drop to zero in certain traffic scenarios where multicast frames (broadcast, multicast, flooding) are present and flow control is enabled.

For a multicast frame, multiple egress ports can receive the same frame from an ingress port at the same time. However, if one of the egress ports congests, then all egress ports will be blocked. Because this can happen instantly and possibly in the middle of frame, all the egress devices in the multicast group will be waiting for the one congested port.

If the above behavior is triggered simultaneously in two interconnected switches, then both switches will receive pause frames and will thus cease to transmit data frames on the interconnected link. As a result, traffic in both directions will be stopped until external action is taken.

Implications

A SW polling routine is required to detect and solve this situation. This will cause frames to be lost in specific scenarios.

Workaround

A SW polling routine must monitor the fill level by observing the queue pointers in each of the port FIFOs. If these pointers have remained unchanged and there is data present for a period of more than two seconds, the routine will assume that this issue has occurred on the link. To loosen up for this situation, the SW routine will momentarily disable egress congestion notification for the port in question. As a consequence, some frames will be lost due to aging and FIFO drop, but the link will begin to carry traffic again.

ORDERING INFORMATION

Part Number	Description
VSC7302VF	Heathrow-III 16 x 1 Gb/s Ethernet Switch Package type VF: 680-pin Tape Super BGA with grounded heat spreader

STANDARD REFERENCES

Ports

The Ethernet ports have been designed to meet or exceed the requirements found in the following standards:

- IEEE Std 802.3-2002 Edition for Ethernet, Fast Ethernet and Gigabit Ethernet
- Hewlett Packard RGMII specification v1.3; Reduced Gigabit Media Independent Interface

ABBREVIATIONS

Table 179. Abbreviations

Abbreviation	Explanation
CFI	canonical format indicator
CMD	command
CPU	central processing unit
CRC	cyclic redundancy check
DS	differentiated services
DSAP	destination service access point
DMAC	destination media access controller address
FIFO	first in first out
GARP	generic/group attributes registration protocol
GbE	Gigabit Ethernet
Gb/s	gigabits per second
GMRP	generic/group multicast registration protocol
GVRP	generic/group VLAN registration protocol
Id	identification
IEEE	Institute of Electrical and Electronic Engineers
IGMP	internet group management protocol
IP	internet protocol
kB	1024 bytes
LAN	local area network
LSB	least significant bit/byte
MAC	media access controller
Mb/s	megabit per second
MDIO	management data input output
MII	medium independent interface
MIIM	medium independent interface management

Table 179. Abbreviations (cont'd)

Abbreviation	Explanation
Mpackets/s	million packets per second
MSB	most significant bit/byte
PCS	physical coding sublayer
PHY	physical layer device
QoS	quality of service
Rbc	receive bit clock
RFC	request for comments
RGMII	reduced gigabit medium independent interface
RMON	remote monitoring
RST	reset
RW	read/write
SFD	start of frame delimiter
SMAC	source media access controller
SNMP	simple networking management protocol
SI	serial CPU interface
SoC	system-on-a-chip
STP	spanning tree protocol
TBD	to be decided
TCP	transmission control protocol
UDP	user data protocol
VLAN	virtual local area network
VID	virtual local area network identifier
VoIP	voice over internet protocol
WAN	wide area network

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