FSAC20SH60

FSAC20SH60

Smart Power Integrated Module (SPIM)

General Description

FSAC20SH60 is an advanced smart power integrated module (SPIM) that Fairchild has newly developed and designed to provide very compact and high performance ac motor drives mainly targeting high speed low-power inverter-driven application like servo drive system. It combines optimized circuit protection and drive matched to low-loss IGBTs. Highly effective short-circuit current detection/protection is realized through the use of advanced current sensing IGBT chips that allow continuous monitoring of the IGBTs current. System reliability is further enhanced by the built-in over-temperature and integrated under-voltage lock-out protection. The high speed built-in HVIC provides opto-coupler-less IGBT gate driving capability that further reduce the overall size of the inverter system design. In addition the incorporated HVIC facilitates the use of single-supply drive topology enabling the FSAC20SH60 to be driven by only one drive supply voltage without opto-couplers. Inverter current sensing application can be achieved due to devided negative dc terminals.

Features

- UL Certified No. E209204
- Three-phase IGBT inverter bridge including control ICs for gate driving and protection
- Converter bridge for one-phase AC-to-DC power conversion
- Circuit for dynamic braking of motor regeneration energy
- Divided negative dc-link terminals for inverter current sensing applications
- Single-grounded power supply due to built-in HVIC
- Typical switching frequency of 15kHz
- Built-in thermistor for over-temperature monitoring
- Inverter power rating of 1.5kW / 100~253 Vac
- Very low thermal resistance due to using DBC substrate
- Isolation rating of 2500Vrms/min.
- Adjustable current protection level by varying series resistor value with sense-IGBTs

Applications

- AC 100V ~ 253V three-phase inverter drive for small power ac motor drives
- Industrial applications requiring high switching frequency operation like servo drive system
- Application ratings:
  - Power : 1.5 kW / 100~253 Vac
  - Switching frequency : Typical 15kHz (PWM Control)
  - 100% load current : 7A (Irms)
  - 150% load current : 10.5A (Irms) for 1 minute

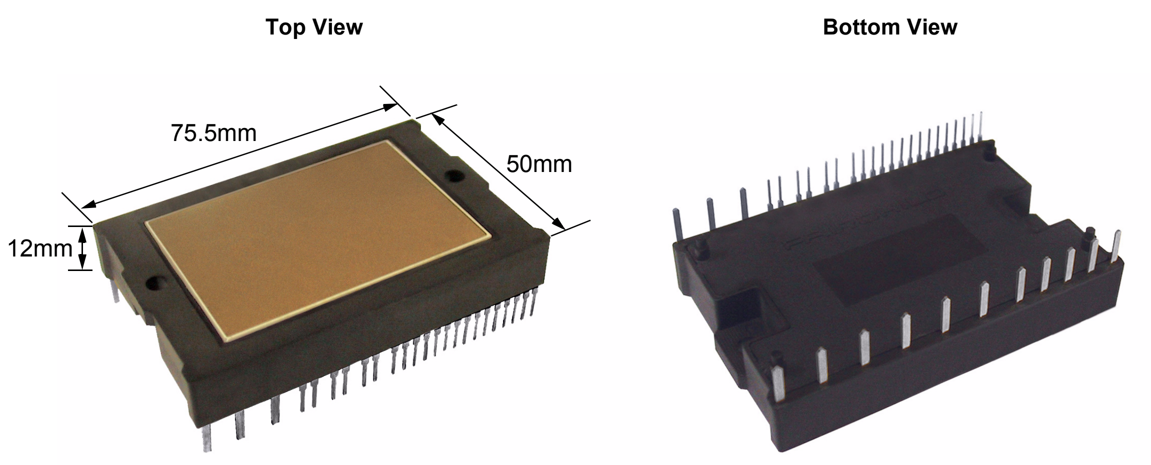


Fig. 1. External View

Integrated Power Functions

- IGBT inverter for three-phase DC/AC power conversion (Please refer to Fig. 3)
- Diode converter for one-phase AC/DC power conversion (Please refer to Fig. 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting,
  Control circuit under-voltage (UV) protection
  Note) Available bootstrap circuit example is given in Figs. 13 and 14.
- For inverter low-side IGBTs: Gate drive circuit, Short circuit protection (SC),
  Control supply circuit under-voltage (UV) protection
- For Brake circuit IGBT : Drive circuit
- Temperature Monitoring: System over-temperature monitoring using built-in thermistor
  Note) Available temperature monitoring circuit is given in Fig. 14.
- Fault signaling: Corresponding to a SC fault (Low-side IGBTs) or a UV fault (Low-side supply)
- Input interface: 5V CMOS/LSTTL compatible, Schmitt trigger input

Bottom View

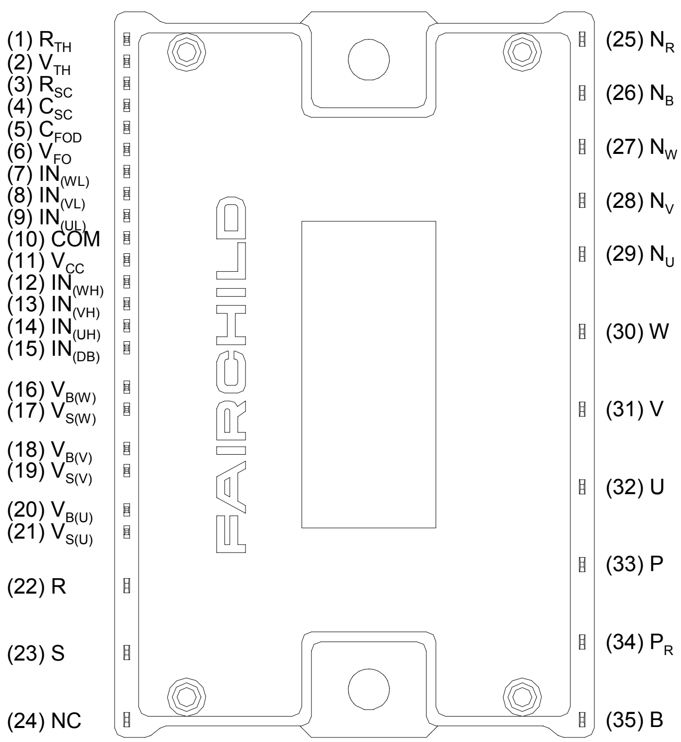
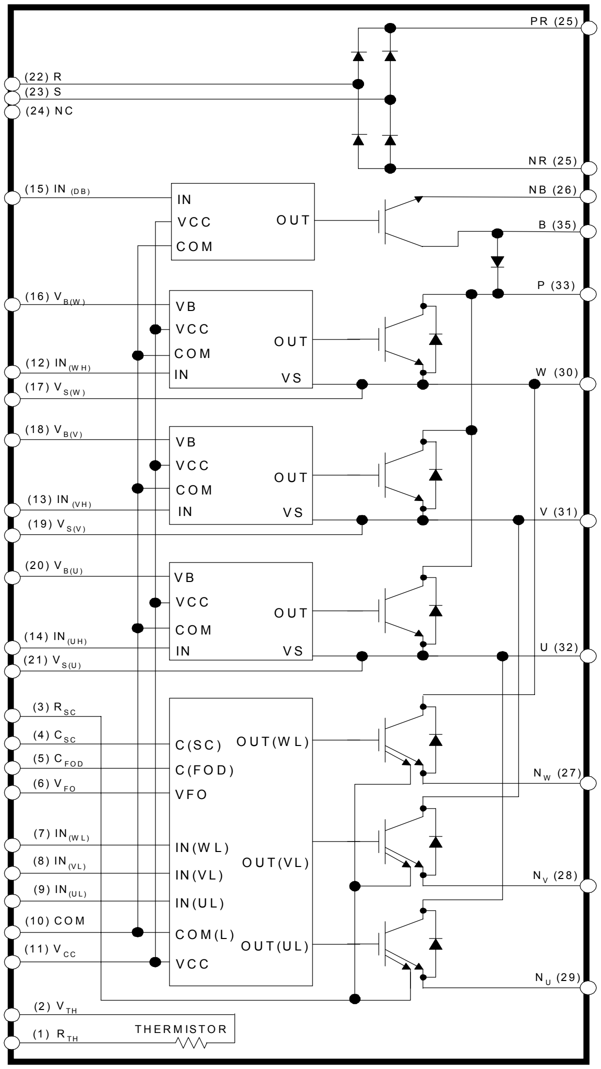


Fig. 2. Pin Configuration

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
2	V_{TH}	Thermistor Bias Voltage
3	R_{SC}	Resistor for Short-Circuit Current Detection
4	C_{SC}	Capacitor (Low-pass Filter) for Short-Circuit Current Detection Input
5	C_{FOD}	Capacitor for Fault Output Duration Time Selection
6	V_{FO}	Fault Output
7	$IN_{(WL)}$	Signal Input for Low-side W Phase
8	$IN_{(VL)}$	Signal Input for Low-side V Phase
9	$IN_{(UL)}$	Signal Input for Low-side U Phase
10	COM	Common Supply Ground
11	V_{CC}	Common Bias Voltage for IC and IGBTs Driving
12	$IN_{(WH)}$	Signal Input for High-side W Phase
13	$IN_{(VH)}$	Signal Input for High-side V Phase
14	$IN_{(UH)}$	Signal Input for High-side U Phase
15	$IN_{(DB)}$	Signal Input for Dynamic Braking
16	$V_{B(W)}$	High-side Bias Voltage for W Phase IGBT Driving
17	$V_{S(W)}$	High-side Bias Voltage Ground for W Phase IGBT Driving
18	$V_{B(V)}$	High-side Bias Voltage for V Phase IGBT Driving
19	$V_{S(V)}$	High-side Bias Voltage Ground for V Phase IGBT Driving
20	$V_{B(U)}$	High-side Bias Voltage for U Phase IGBT Driving
21	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase IGBT Driving
22	R	AC Input for R phase
23	S	AC Input for S phase
24	NC	No Connection
25	N_R	Negative DC-Link Output
26	N_B	Emitter of Brake IGBT
27	N_W	Negative DC-Link Input for W phase
28	N_V	Negative DC-Link Input for V phase
29	N_U	Negative DC-Link Input for U phase
30	W	Output for W Phase
31	V	Output for V Phase
32	U	Output for U Phase
33	P	Positive DC-Link Input
34	P_R	Positive DC-Link Output
35	B	Collector of Brake IGBT



Note:
1) Inverter low-side is composed of three sense-IGBTs including freewheeling diodes for each IGBT and one control IC which has gate driving and protection functions.
2) Inverter high-side is composed of three normal-IGBTs including freewheeling diodes and three drive ICs for each IGBT.

Fig. 3. Internal Equivalent Circuit and Input/Output Pins

Absolute Maximum Ratings (T_J = 25°C, Unless Otherwise Specified)

Inverter Part (Including Brake Part)

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{PN}	Applied between P-N_U, N_V, N_W	450	V
Supply Voltage (Surge)	$V_{PN(Surge)}$	Applied between N_U, N_V, N_W, Surge Value	500	V
Collector-Emitter Voltage	V_{CES}		600	V
Each IGBT Collector Current	$\pm I_C$	T_C = 25°C	20	A
Each IGBT Collector Current (Peak)	$\pm I_{CP}$	T_C = 25°C, Instantaeous Value (Under 1ms)	40	A
Brake IGBT Collector Current	I_C	T_C = 25°C	20	A
Brake IGBT Collector Current (Peak)	I_{CP}	T_C = 25°C	40	A
Brake Diode Anode Current	I_F	T_C = 25°C	20	A
Brake Diode Anode Current (Peak)	I_{FP}	T_C = 25°C	40	A
Collector Dissipation	P_C	Per One Chip	66	W
Operating Junction Temperature	T_J	(Note 1)	-20 ~ +125	℃

Note:
1. It would be recommended that the average junction temperature should be limited to T_J≤125 (T_C≤100) in order to guarantee safe operation.

Converter Part

Item	Symbol	Condition	Rating	Unit
Repetitive Peak Reverse Voltage	V_{RRM}		900	V
Recommended AC Input Voltage	E_a		220	V
DC Output Current	I_O	1-Phase Rectifying Circuit	18	A
Surge (non-repetitive) Forward Current	I_{FSM}	1 Cycle at 60Hz, Peak Value Non-repetitive	300	A
I^2t for Fusing	I^2t	Value for One Cycle of Surge Current	370	A^2s

Control Part

Item	Symbol	Condition	Rating	Unit
Control Supply Voltage	V_{CC}	Applied between V_{CC} - COM	20	V
High-side Control Bias Voltage	V_{BS}	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	20	V
Input Signal Voltage	V_{IN}	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(DB)}$ - COM	-0.3 ~ V_{CC}+0.3	V
Fault Output Supply Voltage	V_{FO}	Applied between V_{FO} - COM	-0.3~V_{CC}+0.3	V
Fault Output Current	I_{FO}	Sink Current at V_{FO} Pin	5	mA
Current Sensing Input Voltage	V_{SC}	Applied between C_{SC} - COM	-0.3~V_{CC}+0.3	V

Total System

Item	Symbol	Condition	Rating	Unit
Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{PN(PROT)}$	V_{CC} = V_{BS} = 13.5 ~ 16.5V T_J = 125°C, Non-repetitive, less than 6µs	400	V
Module Case Operation Temperature	T_C	Center of DBC Plate	-20 ~ +100	°C
Storage Temperature	T_{STG}		-20 ~ +125	°C
Isolation Voltage	V_{ISO}	60Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat-sink Plate	2500	V_{rms}

Thermal Resistance

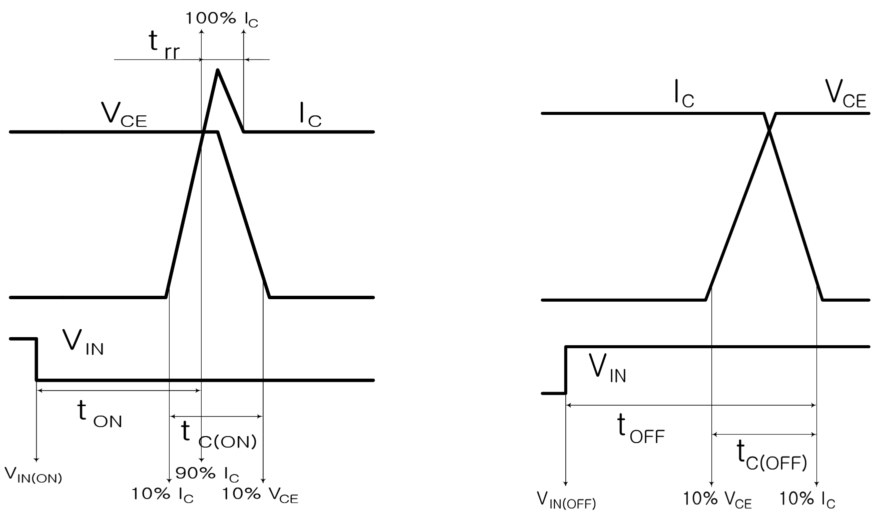
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)Q}$	Each IGBT under Inverter Operating Condition	-	-	2.2	°C/W
	$R_{th(j-c)F}$	Each FWDi under Inverter Operating Condition	-	-	3.0	°C/W
	$R_{th(j-c)QB}$	Brake IGBT	-	-	2.0	°C/W
	$R_{th(j-c)FB}$	Brake Diode	-	-	3.0	°C/W
	$R_{th(j-c)FR}$	Converter Diode	-	-	2.4	°C/W

Electrical Characteristics (T_J = 25°C, Unless Otherwise Specified)

Power Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector - Emitter Saturation Voltage	$V_{CE(SAT)}$	$V_{CC} = V_{BS}$ = 15V V_{IN} = 0V	I_C = 20A, T_J = 25°C	-	-	2.8	V
Collcetor-Emitter Saturation Voltage for Brake IGBT	$V_{CE(SAT)B}$	$V_{CC} = V_{BS}$ = 15V V_{IN} = 0V	I_C = 20A, T_J = 25°C	-	-	2.8	V
FWDi Forward Voltage	V_{FM}	V_{IN} = 5V	I_C = 20A, T_J = 25°C	-	-	2.7	V
Forward Voltage for Brake Diode	V_{FMB}	V_{IN} = 5V	I_C = 20A, T_J = 25°C	-	-	2.7	V
Forward Voltage for Converter Diode	V_{FR}	V_{IN}=5V	I_C = 30A, T_J = 25°C	-	-	1.5	V
Leakage Current for Converter Diode	I_{RRM}	V_R=V_{RRM} , T_J =125°C		-	-	8	mA
Switching Times	t_{ON}	V_{PN} = 300V, $V_{CC} = V_{BS}$ = 15V		-	0.35	-	us
	$t_{C(ON)}$	I_C = 20A, T_J = 25°C		-	0.16	-	us
	t_{OFF}	V_{IN} = 5V ↔ 0V, Inductive Load		-	0.75	-	us
	$t_{C(OFF)}$	(High-Low Side)		-	0.23	-	us
	t_{rr}	(Note 2)		-	0.13	-	us
Collector - Emitter Leakage Current	I_{CES}	$V_{CE} = V_{CES}$, T_J = 25°C		-	-	1	mA

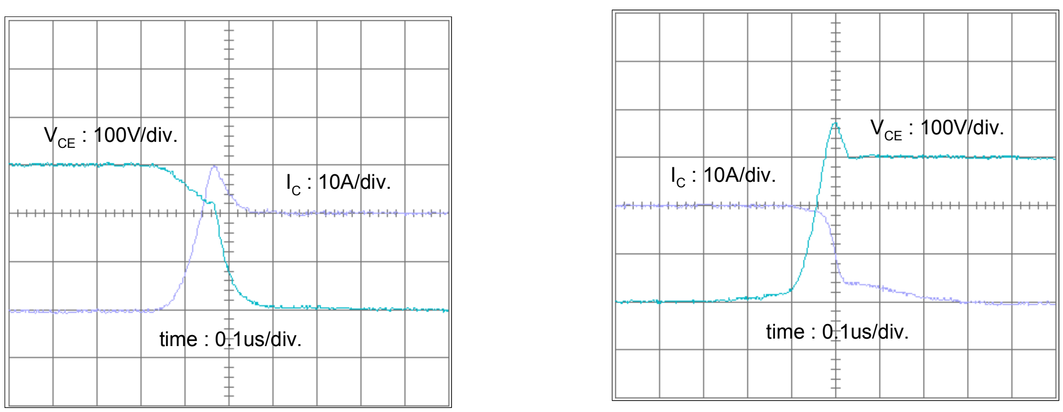
Note:
2. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Fig. 4.



(a) Turn-on

(b) Turn-off

Fig. 4. Switching Time Definition



(a) turn-on

(b) turn-off

Fig. 5. Experimental Results of Switching Waveforms
Test Condition: Vdc=300V, Vcc=15V, L=500uH (Inductive Load), T_J=25°C

Electrical Characteristics

Control Part (T_J = 25°C, Unless Otherwise Specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Control Supply Voltage	V_{CC}	Applied between V_{CC} - COM		13.5	15	16.5	V
High-side Bias Voltage	V_{BS}	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$		13.5	15	16.5	V
Quiescent V_{CC} Supply Current	I_{QCC}	V_{CC} = 15V $IN_{(UL, VL, WL, DB)}$ = 5V $IN_{(UH, VH, WH)}$ = 5V	V_{CC} - COM	-	-	36.5	mA
Quiescent V_{BS} Supply Current	I_{QBS}	V_{BS} = 15V $IN_{(UH, VH, WH)}$ = 5V	$V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ -$V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	-	-	420	uA
Fault Output Voltage	V_{FOH}	V_{SC} = 0V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up		4.5	-	-	V
	V_{FOL}	V_{SC} = 1V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up		-	-	1.1	V
PWM Input Frequency	f_{PWM}	$T_C \leq$ 100°C, $T_J \leq$ 125°C		-	15	-	kHz
Allowable Input Signal Blanking Time considering Leg Arm-short	t_{dead}	-20°C ≤ T_C ≤ 100°C		3	-	-	us
Short Circuit Trip Level	$V_{SC(ref)}$	V_{CC} = 15V (Note 3)		0.45	0.51	0.56	V
Sensing Voltage of IGBT Current	V_{SEN}	T_C =25°C, @ R_{SC} = 95Ω, R_{SU}=R_{SV}=R_{SW}=0Ω and I_C = 20A (Note Fig. 7)		-	0.51	-	V
Supply Circuit Under-Voltage Protection	UV_{CCD}	Detection Level		11.5	12	12.5	V
	UV_{CCR}	Reset Level		12	12.5	13	V
	UV_{BSD}	Detection Level		7.3	9.0	10.8	V
	UV_{BSR}	Reset Level		8.6	10.3	12	V
Fault-out Pulse Width	t_{FOD}	C_{FOD} = 33nF (Note 4)		-	1.8	-	ms
ON Threshold Voltage	$V_{IN(ON)}$	High-Side	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - COM	-	-	0.8	V
OFF Threshold Voltage	$V_{IN(OFF)}$			3.0	-	-	V
ON Threshold Voltage	$V_{IN(ON)}$	Low-Side	Applied between $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM	-	-	0.8	V
OFF Threshold Voltage	$V_{IN(OFF)}$			3.0	-	-	V
ON Threshold Voltage	$V_{IN(ON)}$	Brake	Applied between $IN_{(DB)}$ - COM	-	-	0.8	V
OFF Threshold Voltage	$V_{IN(OFF)}$			3.0	-	-	V
Resistance of Thermistor	R_{TH}	T_{TH} = 25°C (Note Fig. 6)		-	50	-	kΩ
		T_{TH} = 100°C (Note Fig. 6)		-	3.4	-	kΩ

Note:

3. Short-circuit current protection is functioning only at the low-sides. It would be recommended that the value of the external sensing resistor (R_{SC}) should be selected around 50 Ω in order to make the SC trip-level of about 30A at the shunt resistors (R_{SU},R_{SV},R_{SW}) of 0Ω . For the detailed information about the relationship between the external sensing resistor (R_{SC}) and the shunt resistors (R_{SU},R_{SV},R_{SW}), please see Fig. 7.
4. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : C_{FOD} = 18.3 x 10^{-6} x t_{FOD}[F]
5. T_{TH} is the temperature of thermistor.

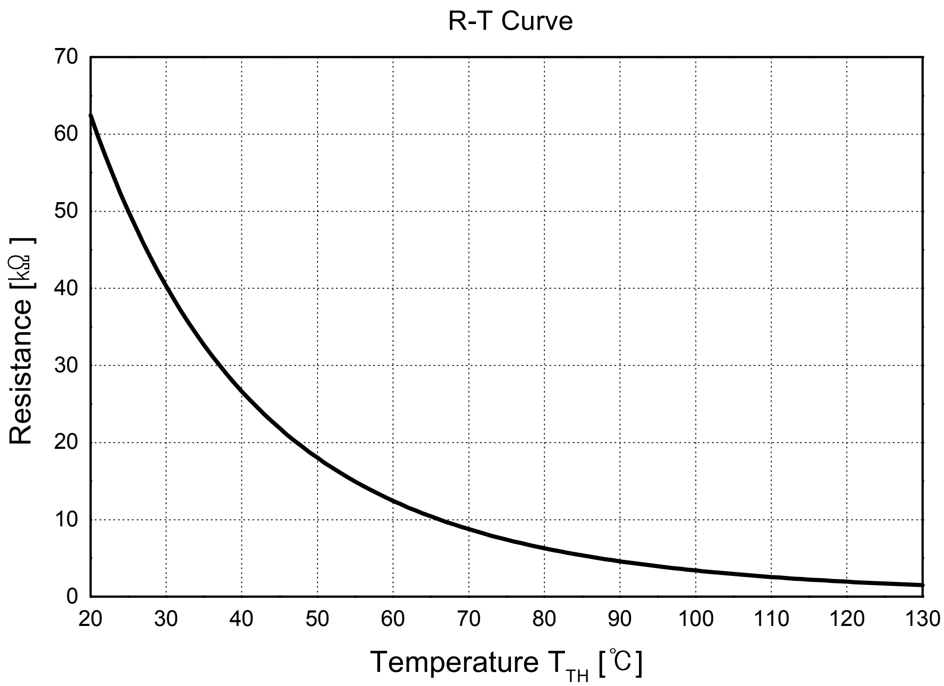


Fig. 6. R-T Curve of The Built-in Thermistor

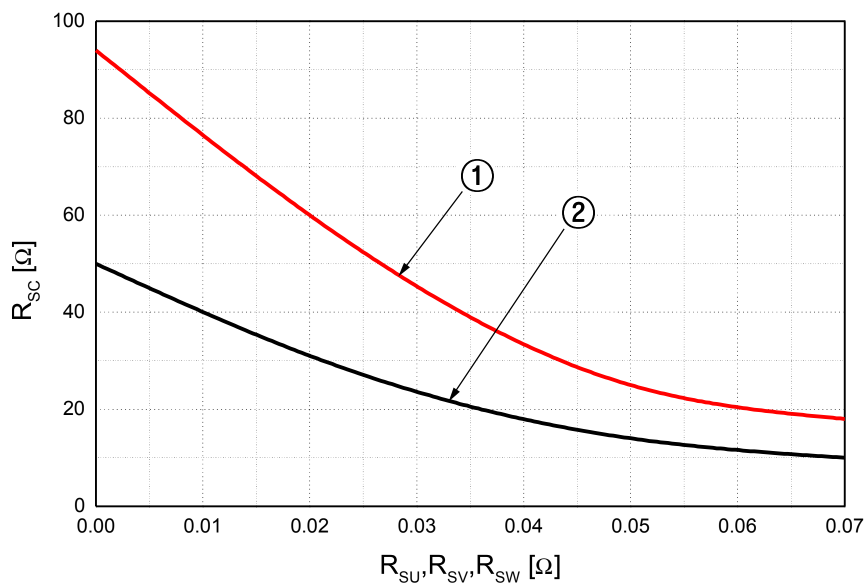
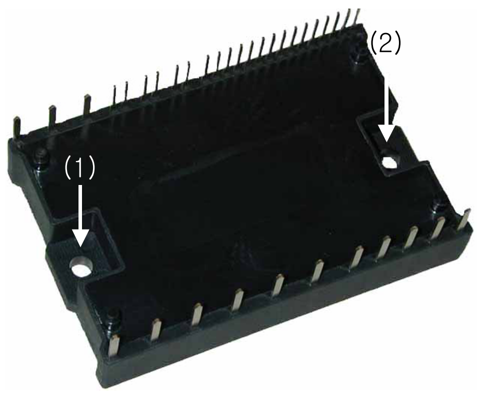


Fig. 7. R_{SC} Variation by Change of Shunt Resistors (R_{SU}, R_{SV}, R_{SW}) for Short-Circuit Protection
① @ around 100% Rated Current Trip ($I_C \doteq 20A$)
② @ around 150% Rated Current Trip ($I_C \doteq 30A$)

Mechanical Characteristics and Ratings

Item	Condition		Limits			Units
			Min.	Typ.	Max.	
Mounting Torque	Mounting Screw: M4 (Note 6)	Recommendation 17.9 Kg•cm	15.3	17.9	20.4	Kg•cm
		Recommendation 1.75 N•m	1.5	1.75	2	N•m
Weight			-	60	-	g



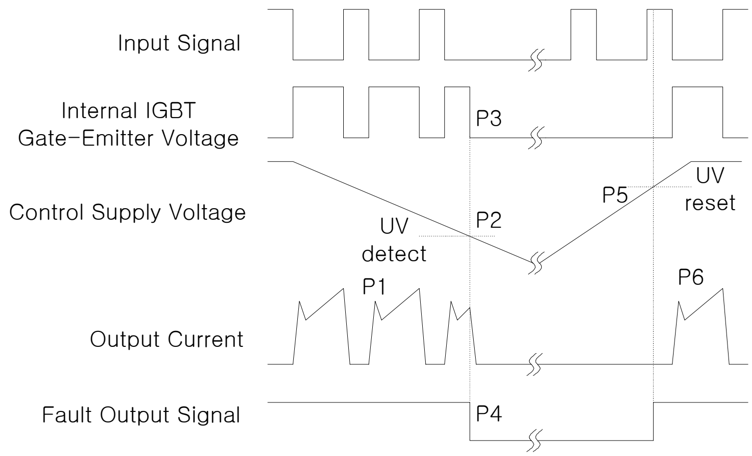
Note:
6. Avoid one side tightening stress. Fig.7 shows the recommended torque order for mounting screws. Uneven mounting can cause the SPIM DBC substrate to be damaged.

Fig. 7. Mounting Screws Torque Order (1 → 2)

Recommended Operating Conditions

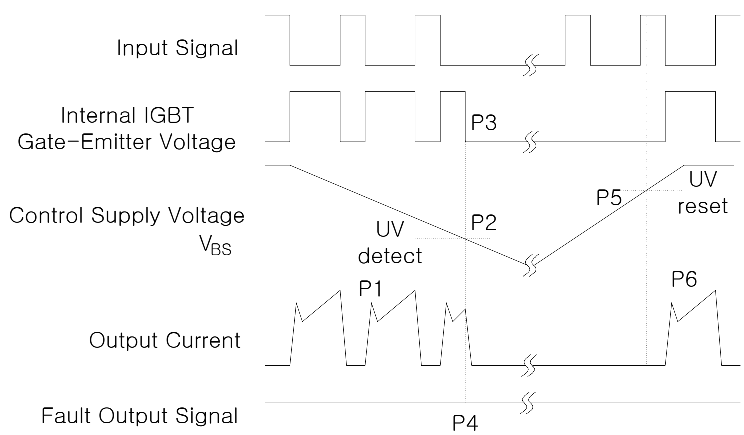
Item	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{PN}	Applied between P - N_U, N_V, N_W	-	300	400	V
Control Supply Voltage	V_{CC}	Applied between V_{CC} - COM	13.5	15	16.5	V
High-side Bias Voltage	V_{BS}	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	13.5	15	16.5	V
Blanking Time for Preventing Arm-short	t_{dead}	For Each Input Signal	3	-	-	us
PWM Input Signal	f_{PWM}	$T_C \le 100°C$, $T_J \le 125°C$	-	15	-	kHz
Input ON Threshold Voltage	$V_{IN(ON)}$	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(DB)}$ - COM	0 ~ 0.65			V
Input OFF Threshold Voltage	$V_{IN(OFF)}$	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(DB)}$ - COM	4 ~ 5.5			V

Time Charts of SPIMs Protective Function



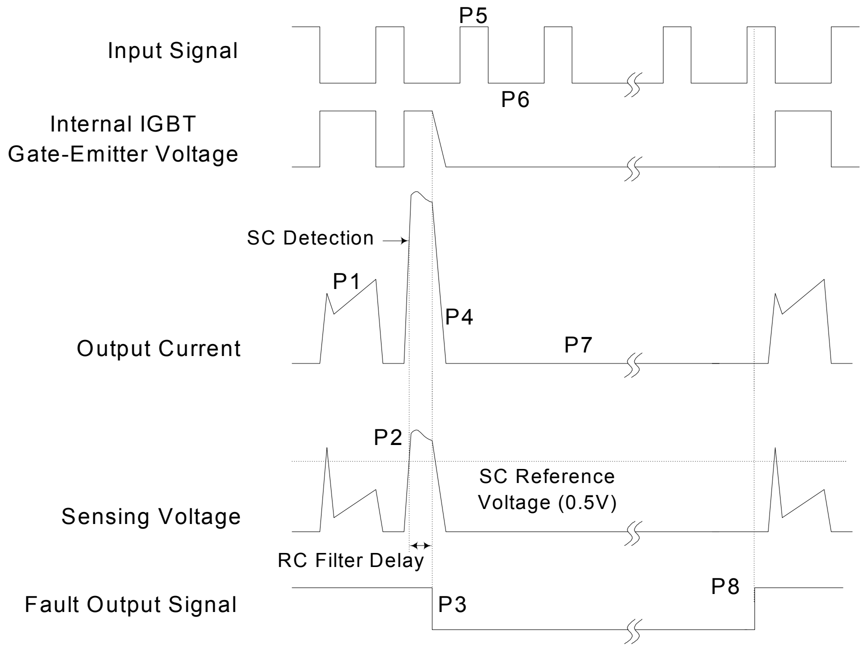
P1 : Normal operation - IGBT ON and conducting current
P2 : Under voltage detection
P3 : IGBT gate interrupt
P4 : Fault signal generation
P5 : Under voltage reset
P6 : Normal operation - IGBT ON and conducting current

Fig. 9. Under-Voltage Protection (Low-side)



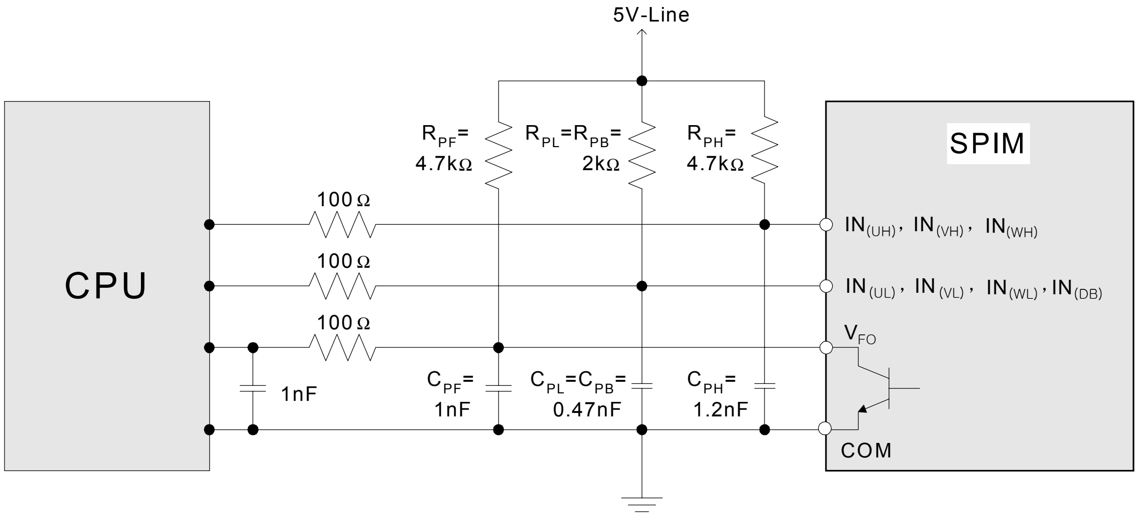
P1 : Normal operation - IGBT ON and conducting current
P2 : Under voltage detection
P3 : IGBT gate interrupt
P4 : No fault signal
P5 : Under voltage reset
P6 : Normal operation - IGBT ON and conducting current

Fig. 10. Under-Voltage Protection (High-side)



P1 : Normal operation - IGBT ON and conducting currents
P2 : Short-circuit current detection
P3 : IGBT gate interrupt / Fault signal generation
P4 : IGBT is slowly turned off
P5 : IGBT OFF signal
P6 : IGBT ON signal - but IGBT cannot be turned on during the fault-output activation
P7 : IGBT OFF state
P8 : Fault-output reset and normal operation start

Fig. 11. Short-circuit Current Protection (Low-side Operation only)



Note :

1) It would be recommended that by-pass capacitors for the gating input signals, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(DB)}$, $IN_{(UH)}$, $IN_{(VH)}$ and $IN_{(WH)}$ should be placed on the SPIM pins and on the both sides of CPU and SPIM for the fault output signal, V_{FO}, as close as possible.
2) The logic input is compatible with standard CMOS or LSTTL outputs.
3) $R_{PL}C_{PL}/R_{PH}C_{PH}/R_{PF}C_{PF}/R_{PB}C_{PB}$ coupling at each SPIM input is recommended in order to prevent input/output signals' oscillation and it should be as close as possible to each of SPIM pins.

Fig. 12. Recommended CPU I/O Interface Circuit

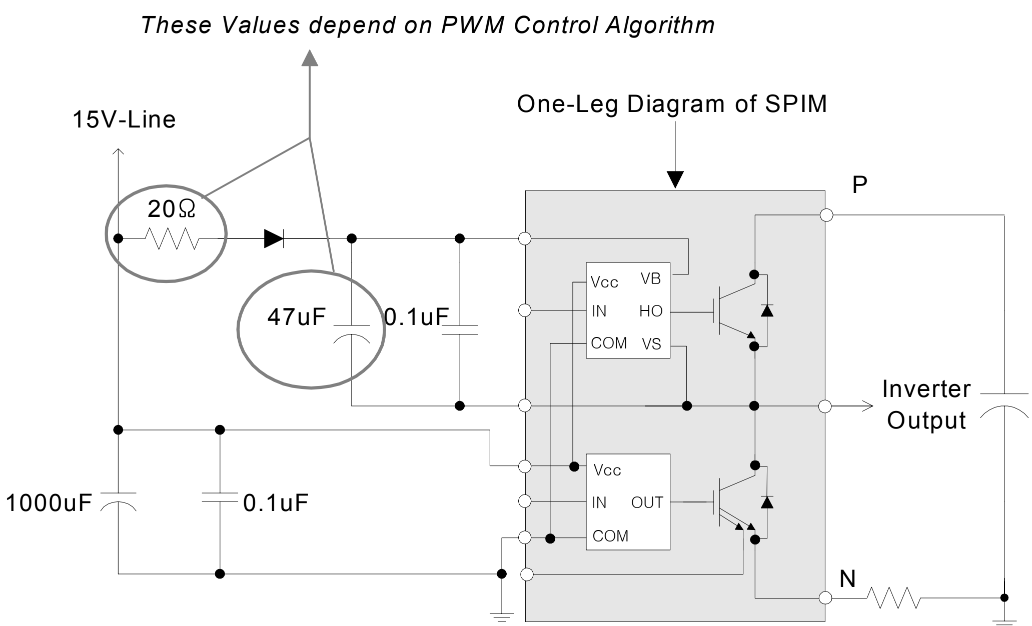
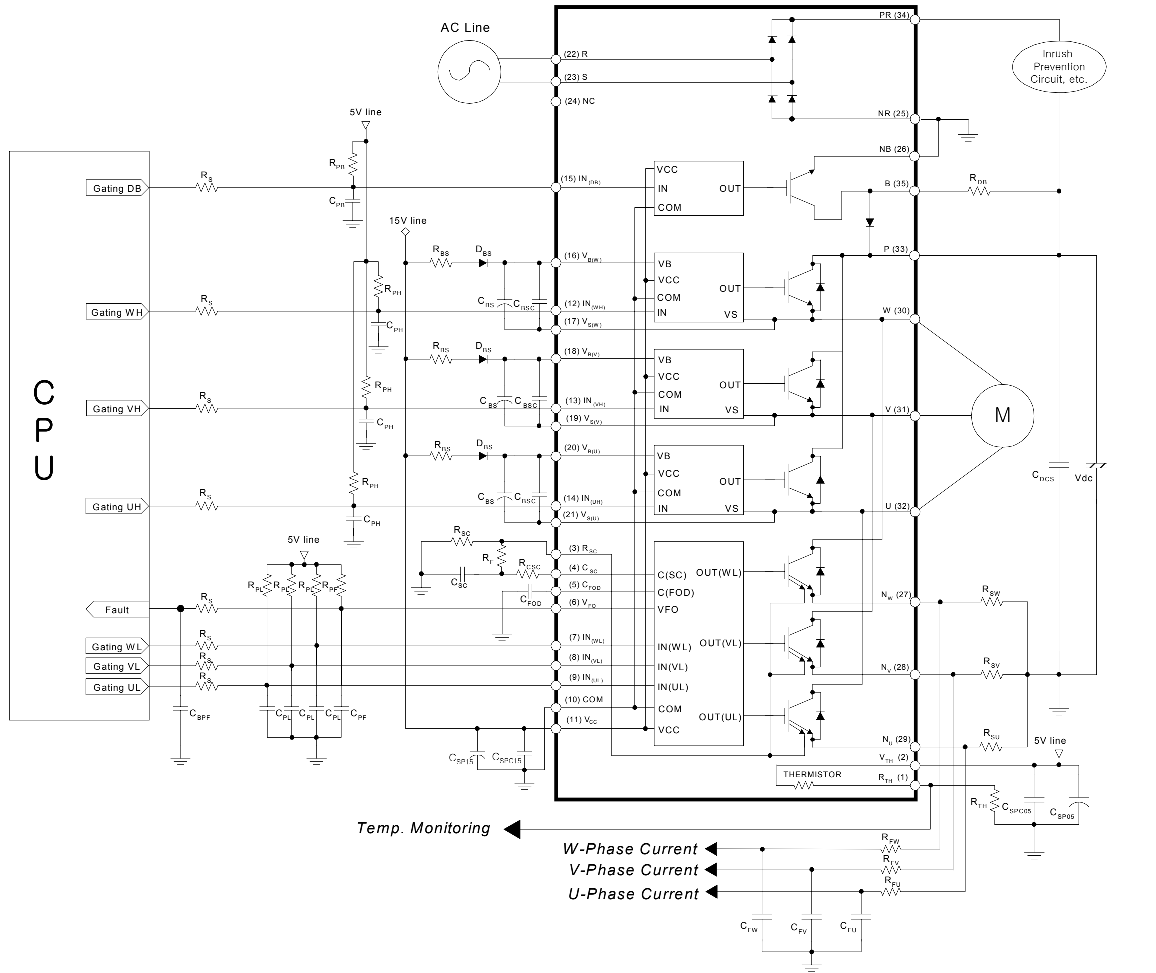


Fig. 13. Recommended Bootstrap Operation Circuit and Parameters

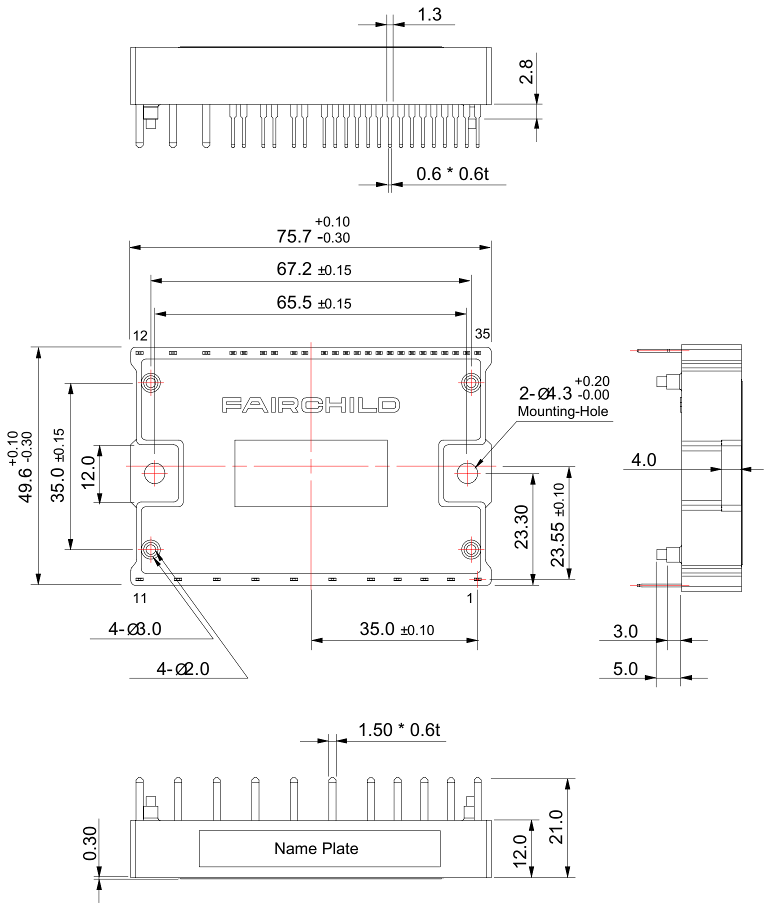


Note:

1) $R_{PL}C_{PL}$/$R_{PH}C_{PH}$ /$R_{PF}C_{PF}$ /$R_{PB}C_{PB}$ coupling at each SPIM input is recommended in order to prevent input signals' oscillation and it should be as close as possible to each SPIM input pin.
2) By virtue of integrating an application specific type HVIC inside the SPIM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
3) V_{FO} output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7kΩ resistance. Please refer to Fig. 14.
4) C_{SP15} of around 7 times larger than bootstrap capacitor C_{BS} is recommended.
5) V_{FO} output pulse width should be determined by connecting an external capacitor(C_{FOD}) between C_{FOD}(pin5) and COM(pin10). (Example : if C_{FOD} = 5.6 nF, then t_{FO} = 300 µs (typ.)) Please refer to the note 4 for calculation method.
6) Each input signal line should be pulled up to the 5V power supply with approximately 4.7kΩ (at high side input) or 2kΩ (at low side input) resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedance of the system's printed circuit board). Approximately a 0.22~2nF by-pass capacitor should be used across each power supply connection terminals.
7) To prevent errors of the protection function, the wiring around R_{SC}, R_F and C_{SC} should be as short as possible.
8) In the short-circuit protection circuit, please select the R_FC_{SC} time constant in the range 3~4 µs.
9) To enhance the noise immunity, C_{SC} pin should be conected to the external circuit through a series resistor, R_{CSC}, which is approximately 390Ω. R_{CSC} should be connected to C_{SC} pin as close as possible.
10) Each capacitor should be mounted as close to the pins of the SPIM as possible.
11) To prevent surge destruction, the wiring between the smoothing capacitor and the P&N pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22 uF between the P&N pins is recommended.
12) The stray inductance between N-pins(N_U, N_V and N_W) and their shunt-resistors(R_{SU}, R_{SV} and R_{SW}) should be less than 10nH. Pleae refer to Fig. 14.

Fig. 14. Application Circuit

Detailed Package Outline Drawings



-. Pin Coordinate

Pin #No	Coordinate x	Coordinate y
1	0.0	0.0
2	-5.6	0.0
3	-11.2	0.0
4	-16.8	0.0
5	-22.4	0.0
6	-30.5	0.0
7	-38.6	0.0
8	-46.7	0.0
9	-54.8	0.0
10	-62.9	0.0
11	-71.0	0.0
12	-71.0	47.1
13	-64.0	47.1
14	-57.0	47.1
15	-51.4	47.1
16	-49.1	47.1
17	-45.0	47.1
18	-42.7	47.1
19	-38.6	47.1
20	-36.3	47.1
21	-32.2	47.1
22	-29.9	47.1
23	-27.6	47.1
24	-25.3	47.1
25	-23.0	47.1
26	-20.7	47.1
27	-18.4	47.1
28	-16.1	47.1
29	-13.8	47.1
30	-11.5	47.1
31	-9.2	47.1
32	-6.9	47.1
33	-4.6	47.1
34	-2.3	47.1
35	0.0	47.1

* datum pin : #1
* Pin Tilt : ±0.10

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PRODUCT STATUS DEFINITIONS

Definition of Terms

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