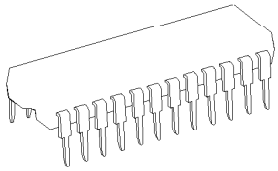
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA1294N

Integrated circuit for power-supply control



SDIP24-P-300-1.78
Weight : 1.22g(Typ.)

TA1294N is a switching power supply IC used as an AC-DC converter.

This IC, the Power Factor Correction(PFC) circuit which improves input current distortion, and PWM control circuit which controls DC output are built in, and this IC is optimum IC as objects for power-supply control, such as color TV, a monitor, and FAX, a printer, etc..

◎ Main characteristics

- Internally synchronized PFC and PWM in one.
- Achievable both the flyback or the half bridge power supply system.
- The over-current and the over-voltage protection circuits to power MOS-FET for a drive are built in.
  UVLO and soft start functions are built in.
- The starting current until UVLO is canceled is about 100uA.
- An external synchronization in the flyback mode. (fH=30kHz to 110kHz)
- Operating frequency is controllable by the terminal 6.
- With the built-in capacity, the internal oscillator is stable against external noise.
- Wide range input voltage :(85V to 264V).
- Achievable the power supply with low total harmonic distortion.
- Stabilized supply voltage (5V) the band gap circuit is available.
- The protection circuits for the pin short and pin open are built in.
- The protection circuits for the pin to GND short and pin to Vcc short are built in.

An outline

TA1294N is IC for the power-supply control which formed the function of power factor correction (PFC) and the switched mode power supplies by PWM control into 1Chip.

It is possible to constitute the power supply of a saving space from high performance when POWER MOS FET is combined with this IC and used.

Since TA1294N have the same frequency of PFC block and PWM block of operation, while they do not have the interference during the mutual block by the difference in frequency of operation, the external measure of various switching noises are easy.

Moreover, an external synchronization is possible and it is the optimum also as ICs for power-supply control, such as monitor display / TV.

PFC block is an average current mode "boost" type.

PWM block is performing the correspondence to a flyback converter, and half bridge type correspondence
PWM maximum-output duty are 80% with the half bridge type ,
50% or less with the flyback converter

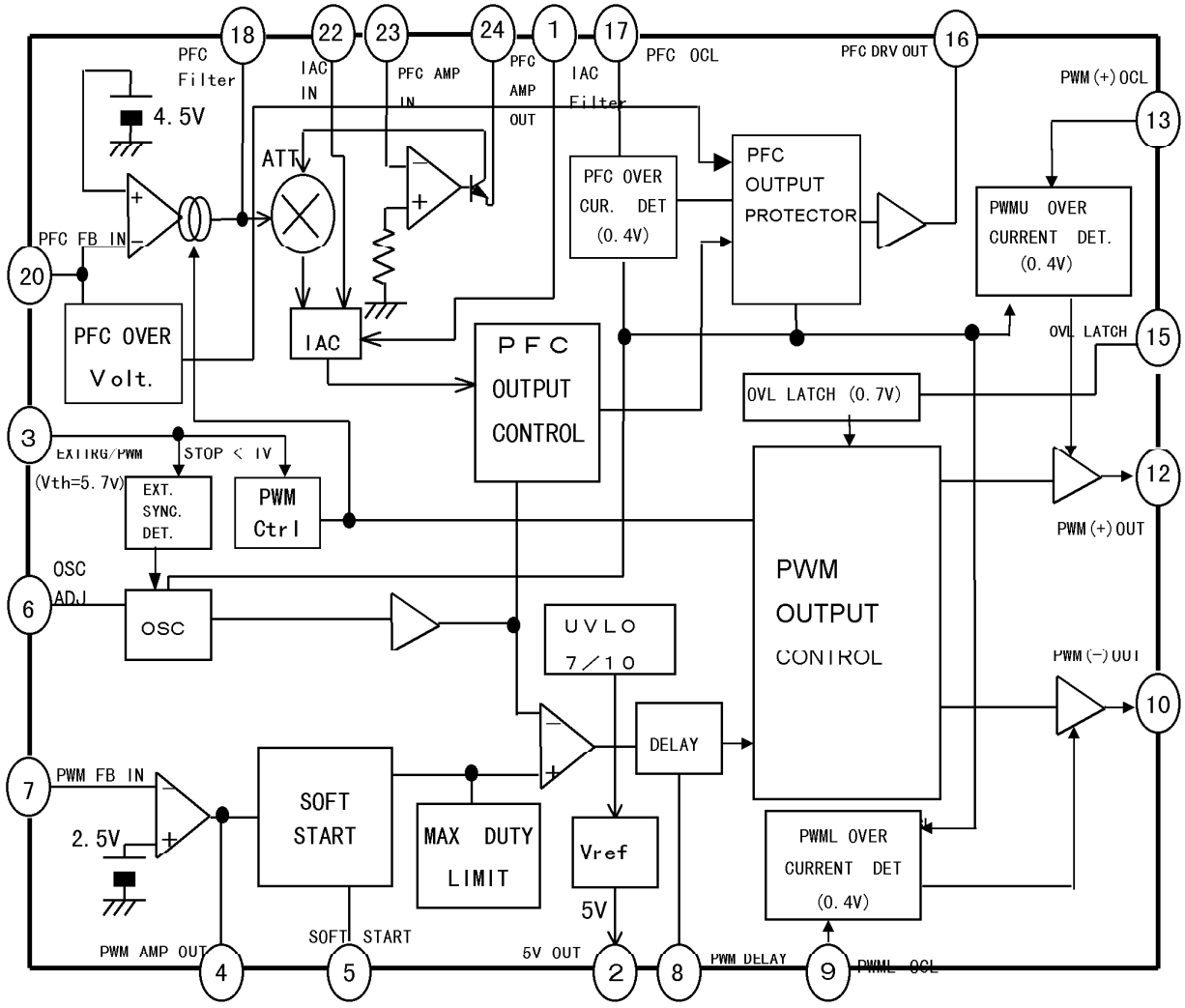
Especially half bridge type correspondence builds in the function that it has the function which controls independently two MOS-FETs for PWM control, and MOS-FET drive does not serve as simultaneous ON.

In PFC block, over-current protection toward MOS-FET for PFC drive,
over-voltage protection toward PFC output voltage are built in.

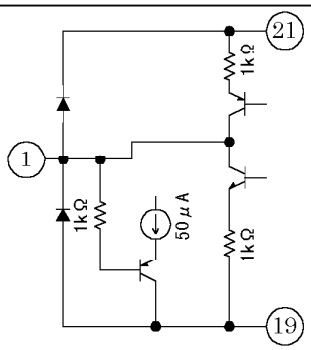
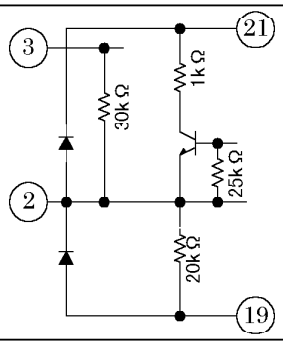
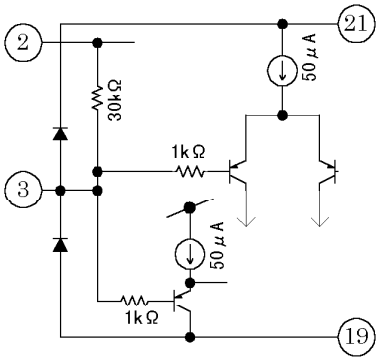
In PWM block, the over-current protection toward MOS-FET for PWM drive is built in
(receiving two MOS-FETs in half bridge type).

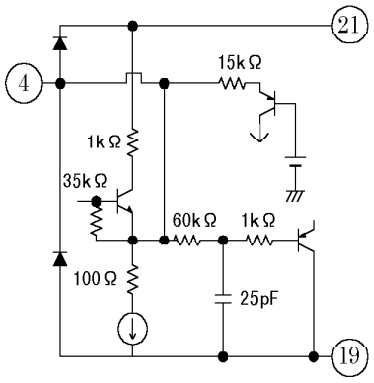
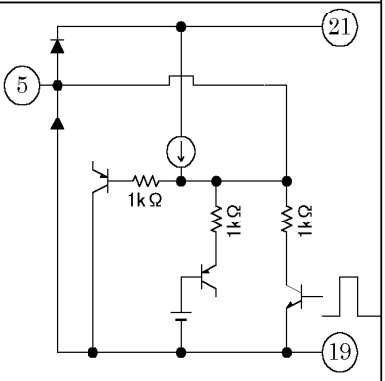
Moreover, since it was protection when abnormalities are in the secondary side voltage of PWM output stage, when the control signal was inputted into the 3 pin, the function which turns off PWM output was built in.

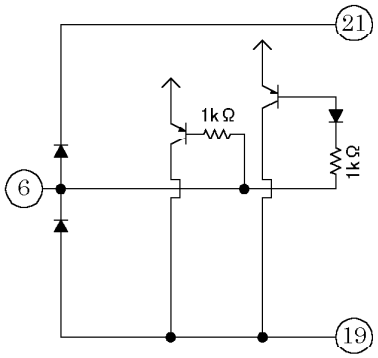
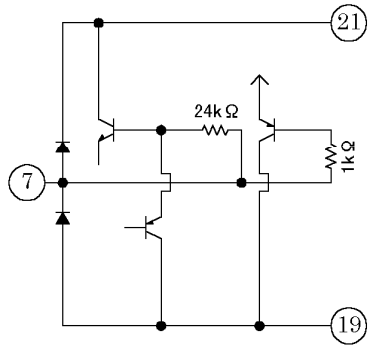
BLOCK DIAGRAM

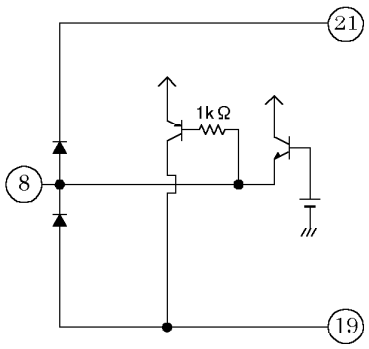
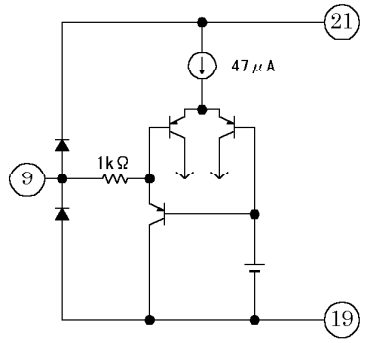


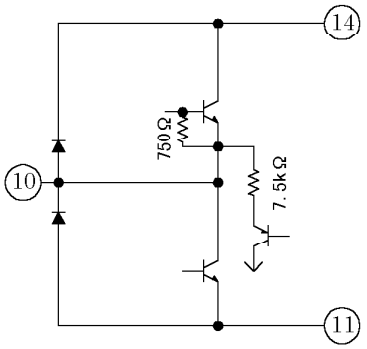
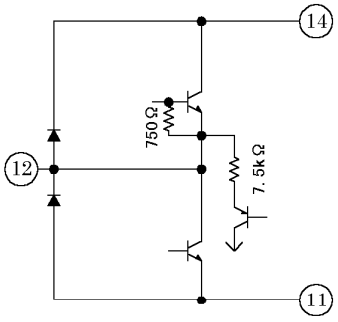
Pin Function

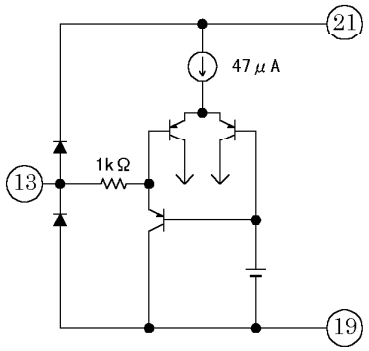
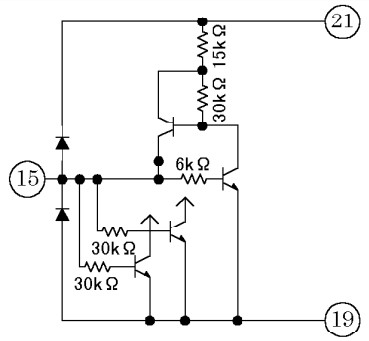
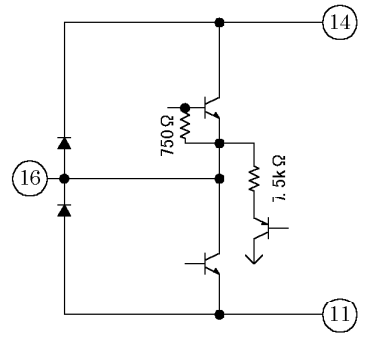
Pin No.	name	Function	Interface
1	IAC FILTER	・A filter is made to a terminal in order to change the difference of current inputted from IAC IN terminal (No. 22 terminal), and current outputted from ATT into DC. ・This terminal voltage turns into the criteria voltage of thetriangular wave threshold voltage which usually generates PFCoutput-pulse width at the time of operation.	
2	5V OUT	・It is the output of the stabilization power supply by the band gap with built-in IC. In IC circumference circuit, it can be used as a criteria power supply. Maximum I output current is next equation Vcc − 5V − Vf − Vceesat) / 1k ohm So Vcc = 9V then max. I out = about 3mA Vcc = 7V(UVLO) then max. I out = about 1mA	
3	EXT TRG ／PWM OFF	・When making it operate in the flyback mode, if the pulse over 5.7V is inputted into this terminal, oscillator oscillation frequency synchronizes with terminal input frequency. There is no external-synchronization function in the half bridge mode. If terminal voltage becomes less than 1V, PWM output will be compulsorily set to Low and the soft start capacity of a No. 5 terminal (SOFT START) will be discharged. Moreover, the charge discharge current to PFC filter of a No. 18 terminal (PFC FILTER) is made into the maximum. Usually it needs to make more than 1V. If this function detects secondary side voltage of a converter transformer in an external circuit and the external setup of this terminal voltage is carried out less than 1V in the case of the voltage more than predetermined, it can constitute the overvoltage protection network of power-supply output voltage. In the half bridge mode, it recommends carrying out to a No. 2 terminal (5V OUT) short.	

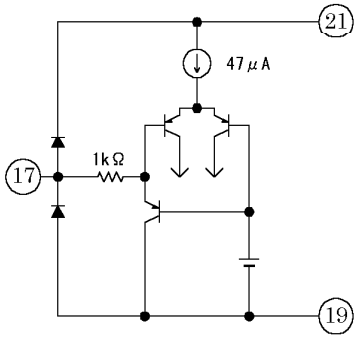
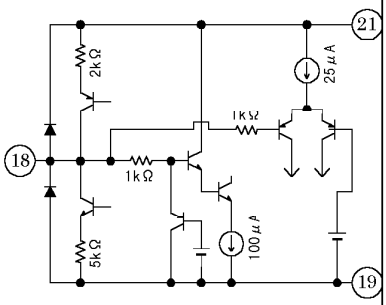
Pin No.	name	Function	Interface
4	PWM-AMP OUT	・It is the output of the error amplifier of PWM block. The capacitor for phase compensation (resistance is included by the case) is connected between the error amplifier inputs of a No. 7 terminal (PWM FB IN). ・It becomes the criteria voltage of triangular wave threshold for this terminal voltage generating PWM output-pulse width. ・If this terminal DC becomes Vcc-VF/2 over, PFC output and PWM output will be compulsorily set to Low.	
5	SOFT START	・It is PIN which connects the capacitor for a soft start of PWM section to opposite GND. The charging current from IC to a No. 5 terminal (SOFTSTART) is about 20microA. PWM output Duty spreads as terminal voltage will go up with an output of a pulse being possible to PWM output at a pan, if this terminal voltage becomes more than abbreviation 1V. At the time of the flyback mode, if terminal voltage is set to about 2.9v in about 5V and the half bridge mode, a soft start will be completed. As for this terminal voltage, the completion back of a soft start also goes up to abbreviation 5.7V. In addition, after the voltage of a No. 20 terminal (PFC FB IN) becomes more than 4.5V, start start of the soft start is carried out. When No. 20 terminal (PFC FB IN) becomes less than 1V or No. 3 terminal (EXT TRG/PWM OFF) less than 1V, the capacity of a No. 5 terminal discharges and it returns to a soft start start state.	

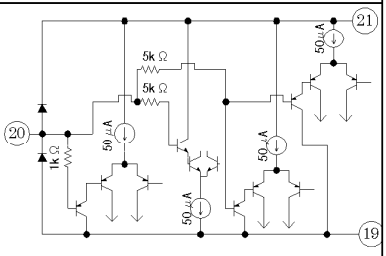
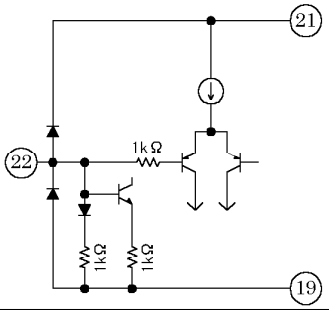
Pin No.	name	Function	Interface
6	OSC ADJ.	・It is a terminal for setting up oscillation frequency of a built-in oscillation circuit. Oscillation frequency is controllable by connecting resistance (REXT) to opposite GND and changing the value. Usual terminal voltage is 5V. Oscillation frequency is abbreviation f OSC(Hz) =10.4 x 109 / ext. R (Ω). *Details fosc= 5/6 x I / c x Vosc, I = 5[V]/R C =Capacitor inside IC(typ. 100pF), Vosc =Amplitude inside IC, 5[V]=terminal voltage, R = ext. Resistor If 100kohm fosc= 104kHz (typ.) If 390kohm fosc= 26.7kHz (typ.) When using an external-synchronization function at the time of the flyback mode, there is the necessity of setting oscillation frequency set up with this terminal as the minimum frequency. ・If this terminal voltage becomes less than 2V or terminal opening, PFC output / PWM output will be compulsorily set to Low.	
7	PWM FB IN	・By the reversal input terminal of the error amplifier of PWM block, external detection of the output DC voltage is carried out, and it is inputted. Another input (inphase input) of error amplifier is connected to the internal criteria power supply of 2.5V. If this voltage of PIN is high, duty of PWM (+) output will be downed. ・If this terminal voltage becomes less than 2V, PFC output and PWM output will be compulsorily set to Low.	

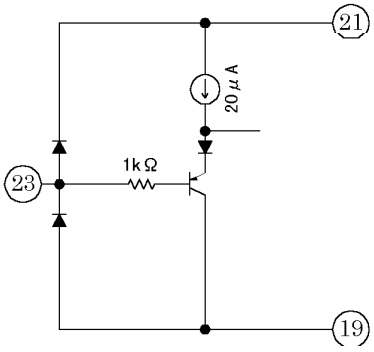
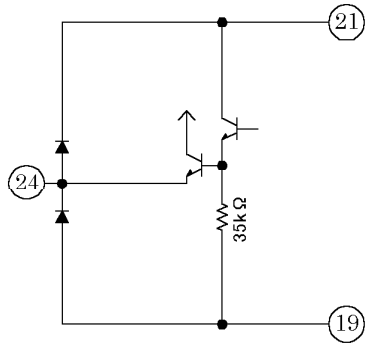
Pin No.	name	Function	Interface
8	PWM DELAY .	・When using PWM block in the half bridge mode, in order to prevent that power MOS-FET of PWM output carries out simultaneous ON, it is the terminal which connects resistance RDLY to opposite GND and sets up delay time between PWM (+) output and PWM(−) output. Usual terminal voltage is 5V. ・The delay time between PWM (+) output and PWM(−) outputs are abbreviation Tdelay(s) $=R_{DLY}x3x10^{-12.}$ ★If this terminal voltage becomes less than 2V, PFC output / PWM output will be compulsorily set to Low.	
9	PWM(−) OCL	・When using PWM output with a half bridge type, it is a terminal for detection for overcurrent protection of MOS-FET used for Vcc side (−side). ・Detection voltage of the detection resistance inserted in the primary side of a converter transformer is inputted into a No. 9 terminal through external LPF. ★Detection voltage is 0.4V. If voltage more than this threshold voltage is inputted, PWM (−) output will be set to Low by the real time, and Low will be held to the start phase of the following PWM (−) output pulse.	

Pin No.	name	Function	Interface
10	PWM(−) OUT	・It is the pulse output which drives MOS-FET used for GND side (- side) in the case of using a half bridge type for PWM output. Amplitude of an output pulse is abbreviation Vcc-1V. ・This terminal is connected to VCC when using a flyback type for PWM output. At this time, PWM (+) output of a No. 12 terminal (PWM (+) OUT) is used as an output. *If this terminal voltage becomes more than abbreviation Vcc more unusually, input-and-output current from this terminal will be intercepted. *Prohibition This terminal is connected to direct GND, and it connects with a low impedance power supply, and DC is impressed.	
11	GND2 (output)	・It is GND of a PFC/PWM drive pulse output transistor	—
12	PWM(+) OUT	・When using a half bridge type for PWM output, it is the pulse output which drives MOS-FET used for VCC side (+ side). ・Amplitude of an output pulse is abbreviation Vcc-1V. ・In using it with a flyback type, it uses this terminal as a PWM drive output. *If this terminal voltage becomes more than abbreviation Vcc more unusually, input-and-output current from this terminal will be intercepted. *Prohibition This terminal is connected to direct GND, and it connects with a low impedance power supply, and DC is impressed.	

Pin No.	name	Function	Interface
13	PWM(+) OCL	・When using PWM output , it is a terminal for detection for overcurrent protection of MOS-FET used for Vcc side (+side). ・Detection voltage of the detection resistance inserted in the primary side of a converter transformer is inputted into a No. 13 terminal through external LPF. ★Detection voltage is 0.4V. If voltage more than this threshold voltage is inputted, PWM (+) output will be set to Low by the real time, and Low will be held to the start phase of the following PWM (+) output pulse.	
14	Vcc2 (output)	・It is VCC of a PFC/PWM drive pulse output transistor. 7.0 to 14V (recommendation 12V) are impressed.	—
15	OVL LATCH	・External detection of the output DC voltage is carried out, and it is inputted. ・When an unusual overvoltage is also detected for a moment (when the voltage over 0.7V goes into a No. 15 terminal), the latch rise of the PFC and PWM output is carried out at Low and Latch.	
16	PFC DRV OUT	・It is the pulse output which drives power MOS-FET used for PFC output. ・Amplitude of an output pulse is abbreviation Vcc-1V. *If this terminal voltage becomes more than abbreviation Vcc more unusually, input-and-output current from this terminal will be intercepted. *Prohibition This terminal is connected to direct GND, and it connects with a low impedance power supply, and DC is impressed.	

Pin No.	name	Function	Interface
17	PFC OCL	・It is a terminal for detection for overcurrent protection of MOS-FET used for PFC output. ・Detection voltage of the detection resistance inserted in the source of power MOS-FET is inputted into a No. 17 terminal through external LPF. If the pulse beyond 0.4V is inputted, PFC output will be set to Low on real time, and Low will be held to the start phase of the following P FC output pulse.	
18	PFC FILTER	・The filter holding the output which compared and carried out current conversion of PFC output voltage and the internal criteria voltage with PFC comparator of the preceding paragraph is connected. ・The profit of ATT is controlled by this terminal voltage. It is the filter which determines the response of PFC control loop. A response needs to be made late in order to bring a power-factor close to 1. ・A response of PFC loop is slow at the time of starting etc., and in order to prevent that output voltage leaps up when PFC output Duty spreads, when PFC terminal voltage is low, PFC output Duty is restricted. Furthermore, the Mitsuru discharge current to PFC filter is made to increase, and the response of a filter is made quick. The time of a no-load changes current according to No. 18 terminal voltage at the time of the maximum, a light load, and starting, the Mitsuru discharge current is changed so that the time of a stationary may serve as the minimum, and it is changing the speed of response of PFC loop.	
19	GND1	・GND other than an output system.	—

Pin No.	name	Function	Interface
20	PFC FB IN	・To the input of PFC comparator, resistance division of the PFC output voltage is carried out, and it is inputted. ・PFC block is controlled so that the mean voltage in this terminal is set to 4.5V. ・After this terminal voltage becomes more than 4.5V, charge of the capacity for a soft start of a No. 5 terminal is started, and PWM output carries out the soft start of the time of power-supply ON. ★If this terminal voltage tends to become more than 5V, Low will be held until an overvoltage protection network works, it sets to Low PFC output of a No. 16 terminal (PFC DRV OUT) on real time and No. 20 terminal voltage is set to 4.5V. ★If this terminal voltage becomes less than 1V, after soft start start, the soft start capacity of a No. 5 terminal will be discharged, and PWM output will be set to Low. ★When this terminal voltage falls less than 0.5V by external abnormalities etc., PFC output of a No. 16 terminal (PFC DRV O UT) is set to Low.	
21	Vcc1	・Vcc other than an output system.UVLO (undershirt voltage lockout) function is in this IC, and circuit operation is made to start more than by 10V, and VCC stops an output less than 7V. ・7.6 to 14V (recommendation 12V) are impressed. ・Current for IC starting is 100microA (typ).	—
22	IAC IN	・With the terminal for obtaining criteria current of PFC block, current conversion of the AC input sine wave which carried out both waves rectification is carried out through resistance for bridge diode, and it inputs into a No. 22 terminal. ★If this terminal voltage becomes more than 2V, PFC output will be compulsorily set to Low.	

Pin No.	name	Function	Interface
23	PFC AMP IN	・It is the reversal input of AMP for taking out current similar to the voltage from the full-wave-rectification circuit of the preceding paragraph. ・ Resistance is inserted between the detection resistance by the side of GND of bridge diode, and a No. 23 terminal. ・The inphase input side of AMP is grounded by GND of IC. ・PFC loop is controlled so that current of the current-wave type of the IAC current-wave type and the similarity as a result flows to bridge diode, and it brings a power-factor close to 1.	
24	PFC AMP OUT	・ It is the output of the error amplifier of PFC block. Current which resistance RPFC is connected to opposite GND and inputted into ATT is set up. ・The filter for profit setting resistance and phase compensation is connected between a terminal 23 and the terminal 24.	

Outline of the functional block

(1) PFC comparator

It is the circuit which detects PFC output voltage.

By carrying out resistance division of the PFC output voltage, and inputting into PFC comparator input (PFC FB IN) of a Pin20, control and PFC output voltage are stabilized PFC loop so that the mean voltage in an input may be set to 4.5V.

Voltage current conversion of the PFC comparator output is carried out, it is held at PFC filter of the Pin18 connected, and controls ATT of the following stage.

(2) PFC error amplifier

Detect current which flows to GND side of the rectifier diode of exterior, and output to ATT.

PFC AMP IN of a Pin23 connects external resistance for PFC AMP OUT of an input and a Pin24 setting up with an output current outputted to ATT between an output and GND.

(3) ATT

It is the circuit which attenuates current from PFC error amplifier according to PFC filter voltage of a Pin18.

ATT output is outputted to IAC circuit.

(4) IAC circuit

Carry out current conversion of the current input from the ATT, and the full-wave-rectification voltage of rectifier diode by external resistance, and compare current inputted into IAC input of a Pin22, and output the error current to IAC filter of a Pin1.

(5) PFC output control-circuit

Generate PFC output pulse by threshold the triangular wave generated by OSC on the voltage generated with IAC filter of a Pin1.

(6) PFC drive circuit

Change drive current and output voltage and output to PFC drive output of a Pin16 so that external MOS-FET can be driven the pulse from a PFC output control circuit.

Obtaining the PFC output DC voltage which responded with pulse width by this PFC loop, it operates so that current of similarity on full-wave-rectification voltage may be passed to rectifier diode

Moreover, an output or stop is controlled by PFC drive circuit in response to the control signal from PFC over-current detector, PFC over-voltage detector, and the protection network of each terminal.

*Prohibition

This terminal is connected to direct GND, and it connects with a low impedance power supply, and DC is impressed.

(7) PFC OCL

Pin17 detects the over current of power MOS-FET connected to PFC drive output of PFC OCL Pin16, and carry out PFC drive output to compulsion Low at the time of an over current.

(8) PFC OVL

Detect the over voltage of PFC drive output to PFC comparater input (PFC FB IN) of a Pin20, and carry out PFC drive output to compulsion Low at the time of over voltage detection.

(9) OSC

It is the internal oscillator which generates triangular wave voltage for obtaining PFC output pulse and PWM output pulse.

Required pulse width has been obtained by threshold triangular wave voltage.

Oscillation frequency can be set up by the external resistance linked to OSC ADJ. of a Pin6.

(10) external-synchronization detection

Detect the external-synchronization signal inputted into the external-synchronization signal input of a Pin3 at the time of the flyback mode, and synchronize oscillation frequency of OSC with an external-synchronization signal.

The inputted standup point of an external-synchronization signal turns into the trigger point.

As for the No. 3 terminal, 5V power supply is supplied through 30kohm.

If the synchronizing signal of amplitude abbreviation 1Vpp is inputted through a capacitor, it will differentiate.

A synchronization requires the standup of a pulse more than by abbreviation 5.7V including bias-voltage 5V.

OSC wave stands/falls term ratio is 5:1.

There is the necessity of not applying an external synchronization after an end of a falling term.

Therefore the value of a capacitor is set up so that the pulse term which becomes more than 5.7V may become less than 20% of an oscillation cycle.

*Example of a setup

When OSC dispatch frequency is the maximum(130kHz),the cycle which is 20% serves as 1.5microsec.

When amplitude of the external-synchronization signal in front of a capacitor is 1.0Vpps,time-constant "tau" itself becomes the term beyond 5.7V.

(The decrease of 30% of input amplitude is a time constant)

Since an input impedance is Typ.30kohm, 50pF is computable from C=R/tau.

Since it needs to be made sufficiently smaller than this computed capacity value, about 20pF is suitable.

Please set up pulse-height value so that the maximum voltage value directly impressed to a No. 3 terminal does not exceed supply-voltage value +0.5V.
(Recommendation 1.0Vpp)

(11) PWM output ON / OFF control-circuit

It is a control circuit for ON or off turning compulsorily a PWM output from the exterior with PWM OFF of a Pin3.

(12) PWM error amplifier

It is the circuit which detects regulator output voltage.

By inputting regulator output voltage into PWM error amplifier input(PWM FBIN) of a Pin7 through an external circuit, PWM loop is controlled so that the mean voltage in an input is set to 2.5V.

PWM error amplifier output of a Pin4 serves as the criteria voltage of the triangular wave threshold voltage for generating PWM pulse, and is transmitted to a soft start circuit.

(13) soft start circuit

PWM output-pulse width is wide at the time of power-supply starting, and it is a circuit for extending PWM output-pulse width gradually to the predetermined pulse width which spends a certain time and is decided with PWM error amplifier so that final-output voltage may not leap up suddenly at high pressure.

Increase of PWM output duty is carried out from zero to predetermined value by charging capacity connected to the soft start terminal of a Pin5 with constant current from IC, rising terminal voltage, and going.

A soft start is started after PFC comparator input (PFC FB IN) of a Pin20 becomes more than 4.5V.

If PFC comparater input or PWM OFF terminal that Pin3 DC becomes less than 1V, it will discharge and soft start capacity connected to the Pin5 will be changed into an initial state.

(14) PWM maximum Duty setting circuit

It is the circuit where maximum duty of a PWM output is set up to about 75% at the time of the flyback mode. (set up the half bridge mode to about 47%)

(15) PWM comparater

By threshold the triangular wave of an oscillator on the threshold voltage generated in PWM error amplifier, the soft start, and the PWM maximum Duty setting circuit, generate PWM output pulse and transmit to PWM DELAY circuit.

(16) PWM DELAY circuit

When using it in half bridge mode, in order to prevent that PWM output power MOS-FET carries out simultaneous ON, it is the circuit which sets up delay time between PWM (+) output of a Pin12 terminal, and PWM(-) output of Pin10.

Delay time can be set up by the external resistance connected with PWM DELAY terminal of Pin 8 terminal between GNDs.

(17) PWM output drive circuit

Change drive current, drive voltage, and polarity so that external power MOS-FET may be driven PWM output pulse from a PWM DELAY circuit, and output straight polarity to PWM (+) output of Pin12, and output negative-electrode nature to PWM (-) output of a Pin10.

If a Pin10 is connected to Vcc, it will become effective Pin12 of PWM (+) output.
By this PWM loop, the regulator output which responded with this pulse width can be obtained.
Moreover, an output/stop is controlled in response to PWM(+) OCL and PWM (-) OCL, or OVER LATCH and the control signal from the protection network of each terminal.

*Prohibition

This terminal is connected to direct GND, and it connects with a low impedance power supply, and DC is impressed.

(18) The PWM(+) OCL

Pin13 PWM(+)OCL detects the over current of power MOS-FET controlled by PWM (+) output of Pin12, and carry out PWM (+) output to compulsion Low at the time of over-current detection.

(19) PWM(-)OCL

The PWM(-) OCL terminal of Pin9 detects the over current of power MOS-FET controlled by PWM (-) output of Pin10, and carry out PWM (-) output to compulsion Low at the time of over-current detection.

(20) OVL LATCH

If OVL LATCH terminal of Pin15 detects the over voltage of a regulator output and an over-voltage is also detected instantaneously, PFC output of a Pin16, PWM (+) output of a Pin12 and PWM (-) output of a Pin10 are latched to compulsion Low.

Only PFC output and PWM (+) output are carried out to compulsion Low at the time of flyback mode.

In order to carry out latch release, there is the necessity of restarting a power supply again or Vcc is dropped to GND at once.

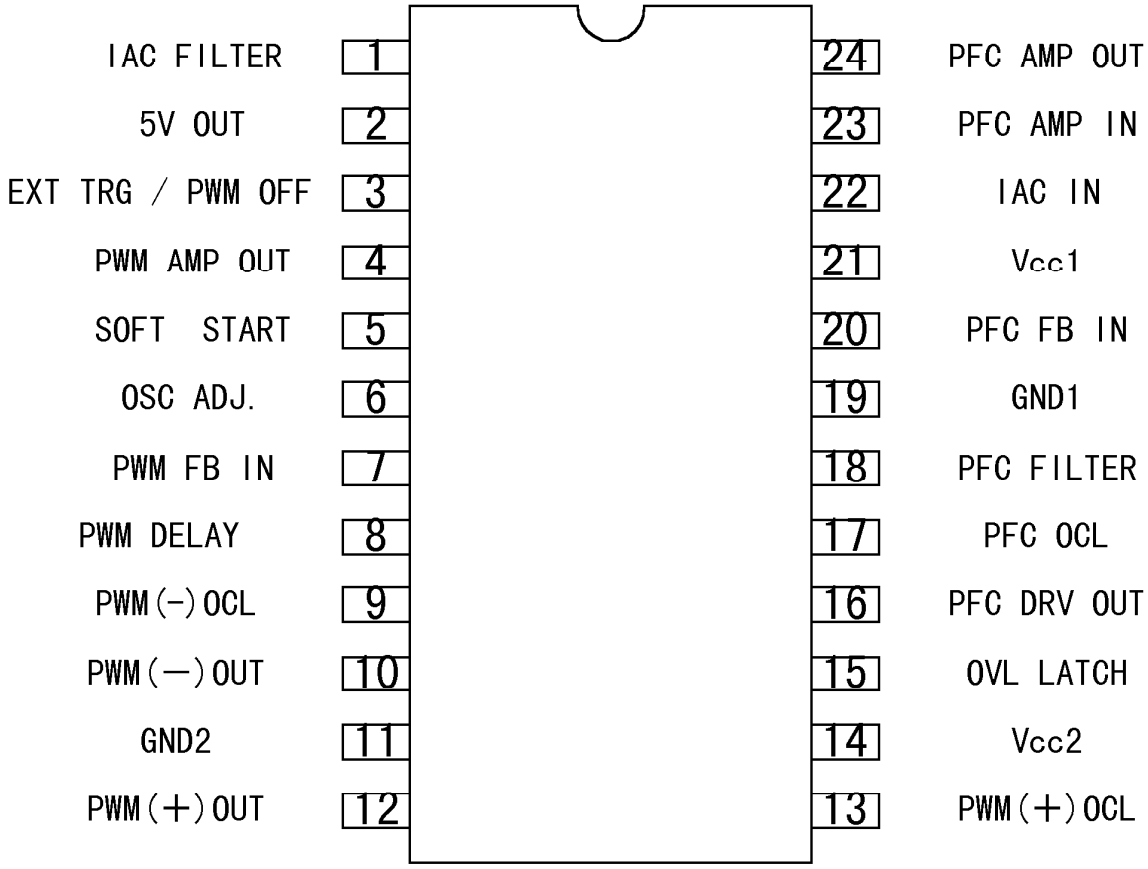
★The protection movement of each terminal or circuit movement

Pin No.	Name	Input Voltage or Comment	PFC DRV OUT	PWM(+)OUT	PWM(-)OUT	Reference Measurment method No.
(*)1	IAC FILTER	more than 5.0V	OutputDuty 0%	-	-	-
2	5V OUT	-	-	-	-	-
3	EXT TRG/PWM OFF	less than1V	-	Low	Low	54
4	PWM AMP OUT	more than Vcc-0.35V	Low	Low	Low	57
5	SOFT START	less than1V	-	Low	Low	34
6	OSC ADJ.	less than2Vor Open	Low	Low	Low	58
7	PWM FB IN	less than2V	Low	Low	Low	59
8	PWM DELAY	less than2V	Low	Low	Low	60
9	PWM(-)OCL	more than0.4V	-	-	Low	64
10	PWM(-)OUT	more than Vcc-0.35V	-	-	Output Current OFF	61
11	GND2	-	-	-	-	-
12	PWM(+)OUT	more than Vcc-0.35V	-	Output Current OFF	-	62
13	PWM(+)OCL	more than0.4V	-	Low	-	63
14	Vcc2	less than UVLO(7V)	Low	Low	Low	1
15	OVL LATCH	more than 0.7V	Low	Low	Low	65
16	PFC DRV OUT	more than Vcc-0.35V	Low	-	-	66
17	PFC OCL	more than0.4V	Low	-	-	67
(*)18	PFC FILTER	less than1.5V	Duty limited	-	-	-
19	GND1	-	-	-	-	-
20	PFC FB IN	less than0.5V	Low	-	-	14
		more than5V	Low	-	-	12
21	Vcc1	less than UVLO(7V)	Low	Low	Low	1
22	IAC IN	more than 2V	Low	-	-	31
(*)23	PFC AMP IN	more than 0V	OutputDuty 0%	-	-	-
(*)24	PFC AMP OUT	more than 4.25V	OutputDuty 0%	-	-	-

(ATTENTION1) - mark is meaning without an influence.

(ATTENTION2) (*)1, (*)18, (*)23, (*)24 is not a protection, The circuit movement is shown.

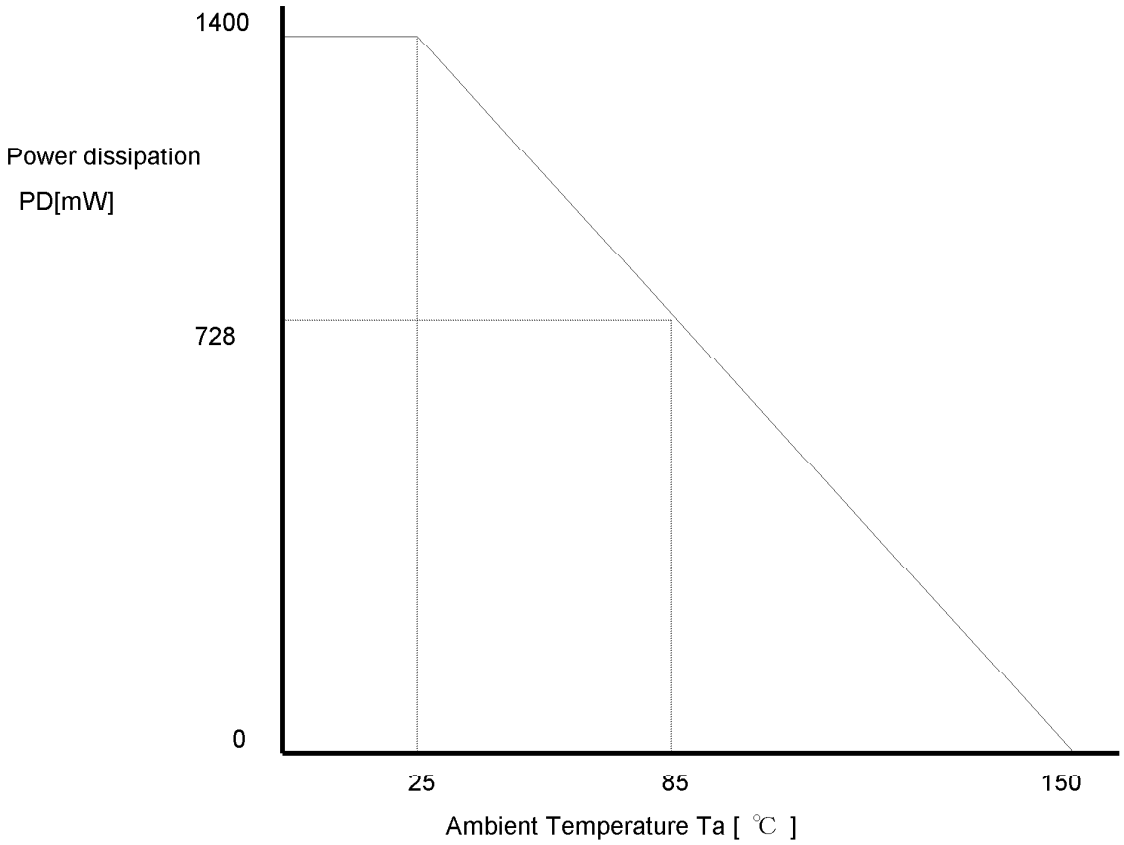
PIN CONNECTION (TOP VIEW)



MAXIMUM RATINGS(Ta=25℃)

CHARACTERISTICS	SYMBOL	RATING	UNIT
SUPPLY VOLTAGE	Vccmax	14	V
MAXIMUM INPUT VOLTAGE	Vinmax	Vcc+0.5	V
MINIMUN INPUT VOLTAGE	Vinmin	GND-0.5	V
POWER DISSIPATION(*1)	PDmax	1400	mW
OPERATING TEMPERATURE	Topr	-25 ～ 85	℃
STORAGE TEMPERATURE	Tstg	-55 ～ 150	℃

(*1)Derated above Ta=25℃ in the proportion of 11.2mW/℃。



PD - Ta curve

RECOMMENDED OPERATING CONDITION

CHARACTERISTIC	PIN No.	MIN.	TYP.	MAX.	UNIT
POWER SUPPLY VOLTAGE	PIN14、PIN21	7.0	12.0	14.0	V
POWER SUPPLY RIPPLE	PIN14、PIN21	-	-	±0.5	V

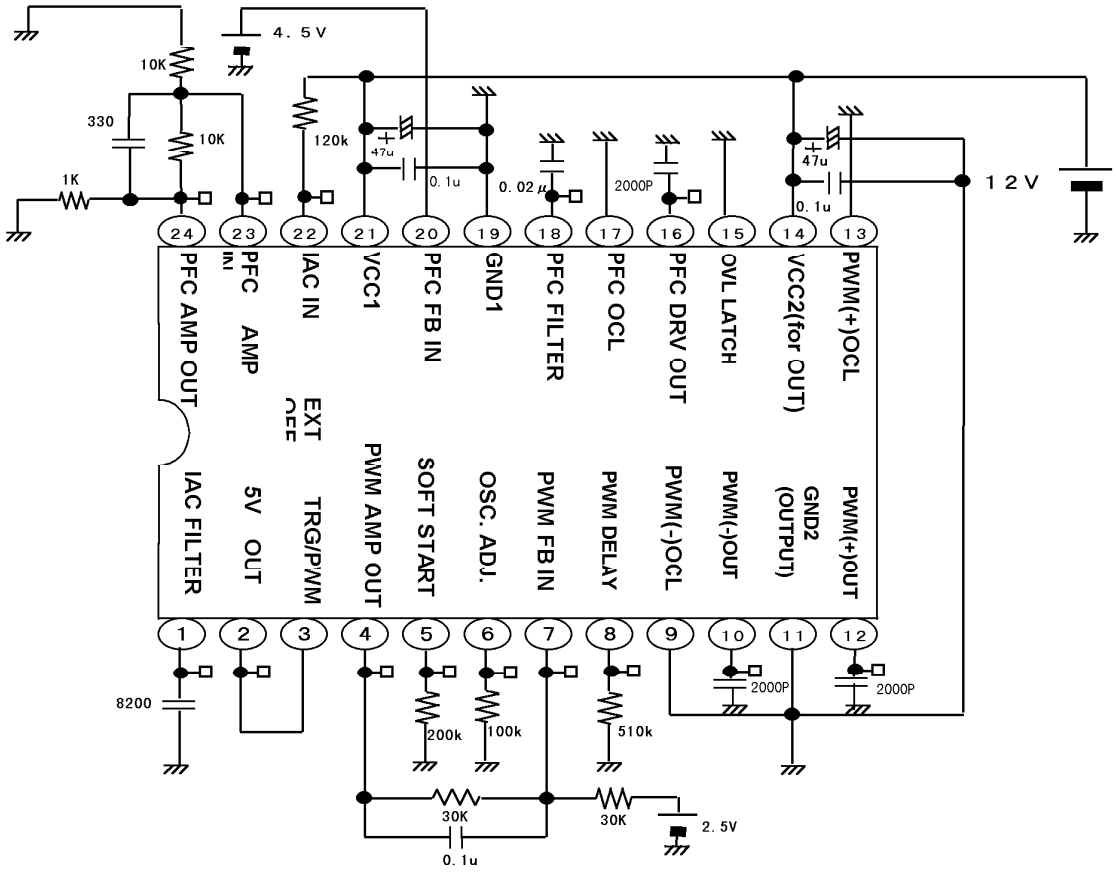
ELECTRICAL CHARACTERISTICS (Ta=25℃,Vcc=12V)

CHARACTERISTICS	PIN No.	SYMBOL	MIN.	TYP.	MAX.	UNIT
POWER CURRENT (12V)□Pin14		I14	7.8	13.0	18.2	mA
(Above CHARACTERISTICS : Load of 2000pF is connected with PIN10,PIN12,PIN16)						
POWER CURRENT (12V)□Pin21		I21	4.2	7.0	9.8	mA

ELECTRICAL CHARACTERISTICS

DC {Reference: A measurement circuit is the next page Ta=25℃、Vcc=12V}

PIN No.	PIN NAME	SYMBOL	MIN.	TYP.	MAX.	UNIT
2	5V OUT	V2	4.85	5.0	5.15	V
4	PWM AMP OUT	V4	2.0	2.5	3.0	V
5	SOFT START	V5	5.4	5.7	6.0	V
6	OSC ADJ.	V6	4.7	5.0	5.3	V
7	PWM FB IN	V7	2.2	2.5	2.8	V
8	PWM DELAY	V8	4.7	5.0	5.3	V
22	IAC IN	V22	0.5	0.8	1.1	V
23	PFC AMP IN	V23	-0.2	0.0	0.2	V
24	PFC AMP OUT	V24	-0.2	0.0	0.2	V



DC terminal Voltage measurement circuit

AC CHARACTERISTICS(There is no designation Vcc=12V、Ta=25℃、)

CHARACTERISTICS	SYMBOL	No.	MIN.	TYP.	MAX.	UNIT
UVLOmovement voltage	VUL	1	6.4	7.0	7.6	V
	VUH		9.5	10.0	10.5	
Start Up Current	Istrt	2	75	100	125	uA
5Voutput Voltage	Vref	3	4.85	5.00	5.15	V
5V output Voltage Vccdrift	ΔVv	4	-15	0	+15	mV
5Voutput Voltage temperature(Reference Data)	ΔVT	5	-15	0	+15	mV
5Voutput load regulation	ΔVL	6	-	-	40	mV
PFC comparator detection voltage	Vdpfc	7	1.3	1.55	1.7	V
PFC comparator Max. sink current	I18MNO	8	19	25	32	uA
	I18MXO		620	830	1040	
PFC comparator Max. source current	I18MNI	9	19	25	32	uA
	I18MXI		620	830	1040	
PFC comparator Max. output Voltage	VPFCCMX	10	4.6	5.85	7.1	V
PFC comparator Min. output Voltage	VPFCCMN	11	0.9	1.2	1.5	V
PFC comparator OVL hysteresis Voltage	VOVLOFF	12	4.75	5.00	5.25	V
	VOVLON		4.25	4.50	4.75	
PFC comparator input Low voltage detect Level	VPFOFF	14	0.35	0.50	0.65	V
	VPFSTOFF		0.75	1.00	1.25	
PFC comparator input Pin current (Reference Data)	IPFCIN	15	-0.5	-	+2	uA
PFC comparator Gain (Reference Data)	GPFAMP	16	50	60	80	dB
PFCerror amp Max. Output Voltage	VPFAMX	17	1.9	2.4	2.9	V

AC CHARACTERISTICS (There is no designation Vcc=12V, Ta=25℃,)

CHARACTERISTICS	SYMBOL	No.	MIN.	TYP.	MAX.	UNIT
PFC error amp Min. output voltage	VPFAMN	18	-0.2	0.0	0.5	V
PFC error amp input Pin current (Reference Data)	IPFAMN	19	-0.5	-	0.0	uA
PFC triangle wave threshold Min. Voltage	VTRMNPF	20	-	1.0	1.3	V
PFC triangle wave threshold Max. Voltage	VTRMXPF	21	4.8	5.0	5.2	V
PFC output pulse Max. Duty	TPFMX		72	76	80	%
triangle wave oscillate frequency	fOSC	22	76	96	116	kHz
PFC output pulse rise time (Reference Data)	TRPF	23	50	75	130	ns
PFC output pulse fall time (Reference Data)	TSPF	24	30	45	90	ns
PFC output pulse Max. voltage	VOPFMX	25	10.5	11.0	11.5	V
PFC output pulse Min. voltage	VOPFMN	26	-0.5	-	0.5	V
ATT Max. Gain	ATTMX	27	11	14	17	dB
ATT Max. attenuation	ATTMN	28	-	-46	-40	dB
ATT center Gain	ATTCT	29	5	8	11	dB
IAC Gain	GIAC	30	-1	0	1	dB
IAC input over voltage detect level	VIACOV	31	1.8	2.0	2.2	V

AC CHARACTERISTICS(There is no designation Vcc=12V、Ta=25℃、)

CHARACTERISTICS	SYMBOL	No.	MIN.	TYP.	MAX.	UNIT
PFC duty Limiter Limit width	PLIM	32	10	13	17	%
PFC output current source	IOPFC	33	300	400	500	mA
sink			490	650	800	
soft start detect start Level	TSTRSF	34	1.0	1.2	1.4	V
soft start time	TSOFT	35	0.14	0.25	0.37	s
soft start detect completion level	TSTPSF	36	4.8	5.0	5.2	V
PWM error amp Gain (Reference Data)	GPWAMP	37	44	54	74	dB
PWM error amp Max. output voltage	VPWAMX	38	8.5	10.5	11.0	V
PWM error amp Min. output voltage	VPWAMN	39	-0.2	0.0	0.5	V
PWM error amp Pin Input current (Reference Data)	IPWAMN	40	-0.5	-	0.0	uA
PWM error amp threshold Level	VTNPW	41	2.3	2.55	2.7	V
PWM triangle wave Min. threshold voltage	VTRMNPW	42	-	1.3	1.6	V
PWM triangle wave Max. threshold voltage	VTMXPWH	43	2.75	2.95	3.15	V
	VTMXPWF		4.90	5.10	5.30	

AC CHARACTERISTICS(There is no designation Vcc=12V、Ta=25℃、)

CHARACTERISTICS	SYMBOL	No.	MIN.	TYP.	MAX.	UNIT
PWM output pulse Max. Duty	TPWMXF	44	70	75	80	%
	TPWMXHR		43	47	51	
	TPWMXHS		48	52	56	
PWM output pulse DELAY quantity (Reference Data)	TDL	45	90	120	150	ns
PWM output pulse rise time (Reference Data)	TRPW	46	50	75	130	ns
PWM output pulse fall time (Reference Data)	TSPW	47	50	75	130	ns
PWM output pulse Max. voltage	VOPWMX	48	10.5	11.0	11.5	V
PWM output pulse Min voltage	VOPWMN	49	-0.5	-	0.5	V
Ext. Trigger pulse Input threshold level	VTEXT	50	5.4	5.7	6.0	V
Ext. Trigger pulse pull in Max frequency (Reference Data)	fEXMX	51	110	-	-	kHz
Ext. Trigger pulse pull in Min frequency (Reference Data)	fEXMN	52	-	-	30	kHz
Ext. Trigger needed Min. pulse width (Reference Data)	TTRG	53	1.5	-	-	us
PWM ON/OFF SW threshold level	VTRG	54	0.8	1.0	1.2	V
PWM(+)output current source	IOPWP	55	277	370	463	mA
sink			427	570	713	
PWM(-)output current source	IOPWN	56	277	370	463	mA
sink			427	570	713	
PWM amp output(Pin4) protect movement voltage	V4pt	57	11.2	11.6	12.0	V
OSC.ADJ.(Pin6) protect movement voltage	V6pt	58	1.7	2.0	2.3	V

OSC.ADJ.(Pin6) As for the terminal opening ,protection moves.

AC CHARACTERISTICS(There is no designation Vcc=12V、Ta=25℃、)

CHARACTERISTICS	SYMBOL	No.	MIN.	TYP.	MAX.	UNIT
PWM FB IN (Pin7) Protect Movement Voltage	V7pt	59	1.7	2.0	2.3	V
PWM DELAY (Pin8) Protect Movement Voltage	V8pt	60	1.7	2.0	2.3	V
PWM(-)OUT (Pin10) Protect Movement Voltage	V10pt	61	11.2	11.6	12.0	V
PWM(+)OUT (Pin12) Protect Movement Voltage	V12pt	62	11.2	11.6	12.0	V
PWM(+) OCL (Pin13) Protect Movement Voltage	V13pt	63	0.3	0.4	0.5	V
PWM(-) OCL (Pin9) Protect Movement Voltage	V9pt	64	0.3	0.4	0.5	V
OVL LATCH (Pin15) Protect Movement Voltage	V15pt	65	0.5	0.7	0.9	V
PFC DRV OUT (Pin16) Protect Movement Voltage	V16pt	66	11.2	11.6	12.0	V
PFC OCL (Pin17) Protect Movement Voltage	V17pt	67	0.3	0.4	0.5	V

(There is no designation Vcc=12V, Ta=25℃.)There is no designation SW15 to 20 =connect a

No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
1	UVLO movement voltage	c	off	a	b	d	a	a	Confirm Pin2(5V out)DC voltage is Output. Vcc voltage is lowered ,and measure Vcc voltage when Pin2 DC output disappears.(VUL) And Vcc voltage is upped ,and measure Vcc voltage when Pin2 DC output appears.(VUH)
		on	on	d	on	a	a	c	
2	Start Up current	↑	↑	↑	↑	↑	↑	↑	Input voltage Vcc= 9.0V (= Pin2(5V out)voltage is Not Outputed.) Measure source current through Vcc(I strt).
		↑	↑	↑	↑	↑	↑	↑	
3	5V output Voltage	↑	↑	↑	↑	↑	↑	↑	Measure Pin2(5V out)output DC voltage(Vref).
		↑	↑	↑	↑	↑	↑	↑	
4	5V output Voltage Vcc drift	↑	↑	↑	↑	↑	↑	↑	Measure Pin2 DC voltage change Level(ΔVv) against Vcc (8V～14V)
		↑	↑	↑	↑	↑	↑	↑	
5	5V output Voltage temperature drift	↑	↑	↑	↑	↑	↑	↑	Measure Pin2 DC voltage change Level(ΔVT) against Temp=-35℃～+85℃
		↑	↑	↑	↑	↑	↑	↑	
6	5Voutput load regulation	↑	on	↑	↑	↑	↑	↑	Pin2(5V out)connect Outside power Supply through 100Ω. Measure Pin2 voltage when 100Ωis current on 4mA (ΔVL)=(Vref)-(measured DC)
		↑	↑	↑	↑	↑	↑	↑	
7	PFC comparator detection voltage	↑	off	↑	↑	↑	↑	↑	Pin20(FPC FB IN) connect Outside power Supply. Measure Pin20 DC (Vdpfc) against Pin18(PFC FILTER)DC is from High to Low.
		↑	↑	↑	↑	↑	↑	↑	
8	PFC comparator Max. sink current	↑	↑	↑	↑	↑	↑	↑	Pin18 connect Outside power Supply(DC3.3V) through 1kΩ. Measure current through 1kΩagainst Pin20 is Inputed DC 0V(I18MMO), Outside power supply voltage changed from 3.3V to 1.0V(I18MXO).
		↑	↑	↑	↑	d	↑	↑	
9	PFC comparator Max. source current	↑	↑	↑	↑	↑	↑	↑	Pin18 connect Outside power Supply(DC3.3V) through 1kΩ. Measure current through 1kΩagainst Pin20 is Inputed DC 5V(I18MNI), Outside power supply voltage changed from 3.3V to 1.0V(I18MXI).
		↑	↑	↑	↑	↑	↑	↑	

(There is no designation Vcc=12V、Ta=25℃、)There is no designation SW15 to 20 =connect a

No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
10	PFC comparator Max. output Voltage	c	off	a	b	d	a	a	Pin20(FPC FB IN) = 0V. Measure Pin18(PFC FILTER) DC voltage. (VPFCCMX)
		on	on	d	on	a	a	c	
11	PFC comparator Min. output Voltage	↑	↑	↑	↑	↑	↑	↑	Pin20(FPC FB IN) = 5V. Measure Pin18(PFC FILTER) DC voltage. (VPFCCMN)
		↑	↑	↑	↑	↑	↑	↑	
12	PFC comparator OVL hysterics Voltage	b	↑	↑	↑	↑	↑	↑	Increase DC voltage for Pin1(IAC FILTER),Pin16 PFC pulse is made to output. Pin20 DC voltage is upped ,and measure Pin20 voltage when Pin16 PFC pulse disappears. (VOVLOFF) And Pin20 DC voltage is lowered ,and measure Pin20 voltage when Pin16 PFC pulse appears.(VUH)
		↑	↑	↑	↑	↑	↑	↑	
		↑	↑	↑	↑	↑	↑	↑	
14	PFC comparator input Low voltage detect Level	b	↑	↑	↑	↑	↑	↑	Increase DC voltage for Pin1(IAC FILTER),Pin16 PFC pulse is made to output. Pin20 DC voltage is lowered .and measure Pin20 voltage when Pin16 PFC pulse disappears.(VPFOFF)
		↑	↑	↑	↑	↑	↑	↑	
15	PFC comparator input Pin current	c	↑	↑	↑	↑	↑	↑	SW19= b , Pin10 connect Outside power Supply through 1kΩ. Pin20 connect Outside power Supply. Measure Pin20 Max. Min. current(IPFCIN) when change Pin18 and Pin20 voltage. FPC FB IN)
		↑	↑	↑	↑	d	↑	↑	
16	PFC comparator Gain	↑	↑	↑	↑	↑	↑	↑	Pin23(PFC AMP IN) connect Outside power Supply. Measure Pin 23 voltage when Pin24(PFC AMP OUT)voltage =-0.1Vto -0.2V, Look for ratio the output variety toward the input variety.(GPFAMX)
		↑	↑	↑	↑	a	d	a	

(There is no designation Vcc=12V, Ta=25℃.)There is no designation SW15 to 20 =connect a

No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
17	PFC error amp Max. Output Voltage	c	off	a	b	d	a	a	Pin23(PFC AMP IN) =-0.2V DC input. Measure Pin24 (PFC AMP OUT)DC voltage.(VPFAMX)
		on	on	d	on	a	d	a	
18	PFC error amp Min. output voltage	↑	↑	↑	↑	↑	↑	↑	Pin23(PFC AMP IN) =+0.2V DC input. Measure Pin24 (PFC AMP OUT)DC voltage.(VPFAMN)
		↑	↑	↑	↑	↑	↑	↑	
19	PFC error amp input Pin current	↑	↑	↑	↑	↑	↑	↑	Pin23(PFC AMP IN) =-0.2V DC input. Measure Pin23 (PFC AMP OUT)current.(IPFAMIN)
		↑	↑	↑	↑	↑	b	↑	
20	PFC triangle wave threshold Min. Voltage	b	↑	↑	↑	↑	↑	↑	Increase DC voltage for Pin1(IAC FILTER),Pin16(PFC DRV out) PFC pulse is made to output. Pin1 voltage is lowered ,and Measure Pin1 voltage ,when PFC pulse is Min. or zero.(VTRMNPF)
		↑	↑	↑	↑	↑	a	c	
21	PFC triangle wave threshold Max. Voltage	↑	↑	↑	↑	↑	↑	↑	Increase DC voltage for Pin1(IAC FILTER),Pin16 PFC pulse is made to output. Pin1 voltage is upped ,and Measure Pin1 voltage ,when PFC pulse width extent is stopped.(VTRMXPF) and measure PFC pulse duty in this time.(TPFMX)
	PFC output pulse Max. Duty	↑	↑	↑	↑	↑	↑	↑	

(There is no designation Vcc=12V, Ta=25℃.)There is no designation SW15 to 20 =connect a

No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
22	Triangle wave oscillate frequency	b	off	a	b	d	a	a	Increase DC voltage for Pin1(IAC FILTER),Pin16(PFC DRV out) PFC pulse is made to output. Measure PFC pulse period ,look for frequency.(Fosc)
		on	on	d	on	a	a	c	
23	PFC output pulse rise time	↑	↑	↑	↑	↑	↑	↑	Above condition ,measure PFC pulse rise time :pulse amplitude 10% to 90% (TRPF)
		↑	↑	↑	↑	↑	↑	↑	
24	PFC output pulse fall time	↑	↑	↑	↑	↑	↑	↑	Above condition ,measure PFC pulse fall time :pulse amplitude 10% to 90% (TSPF)
		↑	↑	↑	↑	↑	↑	↑	
25	PFC output pulse Max. voltage	↑	↑	↑	↑	↑	↑	↑	Above condition ,measure PFC pulse Max. voltage. (VOPFMX)
		↑	↑	↑	↑	↑	↑	↑	
26	PFC output pulse Min voltage	↑	↑	↑	↑	↑	↑	↑	Above condition ,measure PFC pulse Min voltage (VOPFMN)
		↑	↑	↑	↑	↑	↑	↑	
27	ATT Max. Gain	a	↑	↑	↑	↑	↑	↑	Pin1 connect 1kΩtoward GND. Pin18(PFC FILTER)=1V DC input. Pin23(PFC AMP IN)=-0.2V DC input. Measure difference voltage Pin24(PFC AMP OUT) to Pin1、Look for these Ratio.(ΔTTMX)
		↑	↑	↑	↑	b	d	a	
28	ATT Max. attenuation	↑	↑	↑	↑	↑	↑	↑	Above condition, Pin18 DC voltage change 5V, Measure difference voltage Pin24(PFC AMP OUT) to Pin1、Look for these Ratio.(ATTMIN)
		↑	↑	↑	↑	↑	↑	↑	
29	ATT center Gain	↑	↑	↑	↑	↑	↑	↑	Above condition, Pin18 DC voltage change 3.3V, Measure difference voltage Pin24(PFC AMP OUT) to Pin1、Look for these Ratio. (ATTCT)
		↑	↑	↑	↑	↑	↑	↑	

(There is no designation Vcc=12V, Ta=25℃.)There is no designation SW15 to 20 =connect a

No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
30	IAC Gain	d	off	a	b	d	a	a	Pin23(PFC AMP IN)=+0.2V DC input. Pin18(PFC FILTER)=5V DC input. Pin22(IAC IN) connect Outside power Supply through Resistance . adjust Pin22 voltage when Resistance current on 100uA. Connect ammeter between Pin1 and Vcc. Measure current for Pin1,look for Ratio with 100uA. (GIAC)
		on	on	d	on	b	d	a	
31	IAC input over voltage detect level	b	↑	↑	↑	↑	↑	↑	Increase DC voltage for Pin1(IAC FILTER),Pin16 PFC pulse is made to output. Pin22 DC voltage is upped ,and measure Pin22 voltage when Pin16 PFC pulse disappears.(VIAC0V)
		↑	↑	↑	↑	↑	a	c	
32	PFC duty Limiter Limit width	↑	↑	↑	↑	↑	↑	↑	Increase DC voltage for Pin1(IAC FILTER),Pin16 PFC pulse is made to output. Pin18=0V DC input. Measure PFC pulse width.(PLIM)
		↑	↑	↑	↑	↑	↑	↑	
33	PFC output current (source ,sink)	b	↑	↑	↑	↑	↑	↑	Measure by current probe.
		↑	↑	c	off	a	↑	↑	

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No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
34	soft start detect start Level	c	off	a	b	d	a	a	Return resistance is connected between Pin7(PWM FB IN) and Pin4(PWM AMP OUT), and the reversal amplifier of one time is formed. Increase reversal amplifier input Pin connect Outside power Supply voltage, Pin10 and Pin12 PWM pulse is made to output.
35	soft start time	on	on	d	on	a	a	c	Pin20(PFC FB IN)voltage is upped, and Measure the time after a Pin5(SOFT ATART) voltage begins to rise, until 5V is reached. (TSOFT) And measure Pin5 voltage when Pin12 PWM(+) pulse appears. (TSTRSF)
36	soft start detect completion level	↑	↑	↑	↑	a	↑	↑	In the same way as above, Increase Pin12 PWM pulse is made to output.
		↑	↑	↑	↑	↑	↑	↑	Pin5 voltage is upped for 0V,and measure Pin5 voltage ,when PWM pulse width extent is stopped. (TSTPSF)
37	PWM error amp Gain	↑	↑	↑	↑	d	b	c	Pin7 connect Outside power Supply.
		↑	↑	↑	↑	↑	↑	↑	Measure Pin7 voltage when Pin4(PWM AMP OUT)voltage =1.5Vto 3.5V. Look for ratio the output variety toward the input variety.(GPWAMP)
38	PWM error amp Max. output voltage	↑	↑	↑	↑	↑	↑	↑	Pin7=+1.5V DC input.
		↑	↑	↑	↑	↑	↑	↑	Measure Pin4 voltage(VPWAMX)
39	PWM error amp Min. output voltage	↑	↑	↑	↑	↑	↑	↑	Pin7=+3.5V DC input.
		↑	↑	↑	↑	↑	↑	↑	Measure Pin4 voltage.(VPWAMN)

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No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
40	PWM error amp Pin Input current	c	off	a	b	d	d	c	Pin7(PWM FB IN) =2.5V DC input. Measure Pin7 current.(IPWAMIN)
		on	on	d	on	a	a	c	
41	PWM error amp threshold Level	↑	↑	↑	↑	↑	b	↑	Pin7 connect Outside power Supply. Measure Pin7 DC (VTNPW) against Pin4(PWM AMP OUT)(DC is from High to Low.
		↑	↑	↑	↑	↑	↑	↑	
42	PWM triangle wave Min. threshold voltage	↑	↑	↑	↑	↑	a	a	Return resistance is connected between Pin7 and Pin4, and the reversal amplifier of one time is formed. Increase reversal amplifier input Pin connect Outside power Supply voltage, Pin10 and Pin12 PWM pulse is made to output. Pin7 voltage is upped ,and Measure Pin4 voltage, when PWM pulse is Min. or zero.(IPWAMIN)
		↑	↑	↑	↑	↑	↑	↑	
43	PWM triangle wave Max. threshold voltage	↑	↑	↑	↑	↑	↑	↑	In the same way as above, Pin7 voltage is upped ,and Measure Pin4 voltage(VTMXPWH) and Pin12 Pin10(TPWMXHR)(TPWMXHS) output pulse duty, when PWM pulse width extent is stopped.(VTRMXPF) Pin10(PWM(-)out is connected with Vcc, The same measurement is done, measure Pin4 voltage(VTMXPWF) and Pin12 output pulse duty. (TPWMXF)
		↑	↑	↑	↑	↑	↑	↑	
44	PWM output pulse Max. Duty	↑	↑	↑	↑	↑	↑	↑	
		↑	↑	a	↑	↑	↑	↑	
45	PWM output pulse delay quantity	↑	↑	↑	↑	↑	↑	↑	Return resistance is connected between Pin7 and Pin4, and the reversal amplifier of one time is formed. Increase reversal amplifier input Pin connect Outside power Supply voltage, Pin10 and Pin12 PWM pulse is made to output. Measure phase difference(TDL) between the Pin12 and Pin10 PWM DRV pulse, each rise and fall.
		off	off	d	↑	↑	↑	↑	
46	PWM output pulse rise time	c	off	a	b	d	a	a	Return resistance is connected between Pin7 and Pin4, and the reversal amplifier of one time is formed. Increase reversal amplifier input Pin connect Outside power Supply voltage, Pin10 and Pin12 PWM pulse is made to output. measure PFC pulse rise time (TRPW) :pulse amplitude 10% to 90%
		on	on	d	on	a	a	c	

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No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
47	PWM output pulse fall time	c	off	a	b	d	a	a	Return resistance is connected between Pin7 and Pin4, and the reversal amplifier of one time is formed. Increase reversal amplifier input Pin connect Outside power Supply voltage, Pin10 and Pin12 PWM pulse is made to output. measure PFC pulse fall time (TSPW) :pulse amplitude 90% to 10%
		on	on	d	on	a	a	c	
48	PWM output pulse Max voltage	↑	↑	↑	↑	↑	↑	↑	Above condition, measure PWM output pulse Max. voltage. (VOPWMX)
		↑	↑	↑	↑	↑	↑	↑	
49	PWM output pulse Min voltage	↑	↑	↑	↑	↑	↑	↑	Above condition, measure PWM output pulse Min. voltage. (VOPWMN)
		↑	↑	↑	↑	↑	↑	↑	
50	Ext. Trigger pulse Input threshold level	↑	↑	c	↑	↑	↑	↑	Return resistance is connected between Pin7 and Pin4, and the reversal amplifier of one time is formed. Increase reversal amplifier input Pin connect Outside power Supply voltage, Pin10 and Pin12 PWM pulse is made to output. Measure Ext. Trigger pulse Max. level(VTEXT) when a Ext. trigger pulse is inputted(start value :5V)to Pin3(EXT TRG/PWM OFF) and raised gradually and locked in the PWM DRV pulse.
		↑	↑	↑	↑	↑	↑	↑	
51	Ext. Trigger pulse pull in Max frequency	↑	↑	b	↑	↑	↑	↑	Above condition, Ext. trigger frequency is upped ,Measure unlock Ext. trigger frequency.(Fexmx) :Pin3 input Ext. trigger pulse(1Vpp) through condenser.
		↑	↑	↑	↑	↑	↑	↑	
52	Ext. Trigger pulse pull in Min frequency	↑	↑	↑	↑	↑	↑	↑	Above condition, Ext. trigger frequency is lowered ,Measure unlock Ext. trigger frequency.(fEXMN) :Pin3 input Ext. trigger pulse(1Vpp) through condenser.
		↑	↑	↑	↑	↑	↑	↑	
53	Ext. Trigger needed Min. pulse width	↑	↑	↑	↑	↑	↑	↑	Above condition, Ext. trigger pulse width is lowered ,Measure unlock Ext. trigger pulse width.(TTRG) :Pin3 input Ext. trigger pulse(100kHz) through condenser.
		↑	↑	↑	↑	↑	↑	↑	

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No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
54	PWM ON/OFF SW threshold level	c	off	c	b	d	a	a	Return resistance is connected between Pin7(PWM FB IN) and Pin4(PWM AMP OUT), and the reversal amplifier of one time is formed. Increase reversal amplifier input Pin connect Outside power Supply voltage, Pin10 and Pin12 PWM pulse is made to output. Pin3(EXT TRG/PWM OFF) =2V DC input. Pin3 DC voltage is lowered ,and measure Pin3 voltage when PWM pulse disappears.(VPWSW)
		on	on	d	on	a	a	c	
55	PWM(+)output current (source, sink)	↑	↑	a	↑	↑	↑	↑	Measure by current probe.
		↑	off	b	↑	↑	↑	↑	

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No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
56	PWM(-)output current (source, sink)	c	off	a	b	d	a	a	Measure by current probe.
		off	on	a	on	a	a	c	
57	PWM amp output (Pin4) protect movement voltage	↑	↑	↑	a	↑	b	c	Pin4(PWM AMP OUT) −10V DC input. Pin4 DC voltage is upped ,and measure Pin4 voltage when PWM pulse disappears.(VP4)
		on	↑	d	↑	↑	↑	↑	
58	OSC.ADJ.(Pin6) protect movement voltage	↑	↑	↑	↑	b	↑	↑	Increase DC voltage for Pin1(IAC FILTER),Pin16 PFC pulse is made to output. Increase DC voltage for Pin4(PWM AMP OUT), Pin10 and Pin12 PWM pulse are made to output. Pin5(OSC ADJ) connect Outside power Supply DC voltage. Pin5 DC voltage is lowered ,and measure Pin5 voltage when PWM pulse disappears.(VP6) and confirm PWM output is stopping when Pin6 is opened.
		↑	↑	↑	↑	↑	↑	↑	
59	PWM FB IN (Pin7) Protect Movement Voltage	b	↑	↑	b	d	b	c	Increase DC voltage for Pin1(IAC FILTER),Pin16 PFC pulse is made to output. Increase DC voltage for Pin4(PWM AMP OUT), Pin10 and Pin12 PWM pulse is made to output. Pin7=2.5V DC input. Pin7 DC voltage is lowered ,and measure Pin7 voltage when PFC & PWM pulse disappears.(VP7)
		↑	↑	↑	↑	↑	↑	↑	

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No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
60	PWM delay (Pin8) Protect Movement Voltage	b	off	a	a	c	b	c	Increase DC voltage for Pin1(IAC FILTER),Pin16 PFC pulse is made to output. Increase DC voltage for Pin4(PWM AMP OUT), Pin10 and Pin12 PWM pulse are made to output. Pin8(PWM DELAY) connect Outside power Supply DC voltage.
		on	on	d	on	a	a	c	Pin8 DC voltage is lowered ,and measure Pin8 voltage when PFC & PWM pulse disappears.(VP8)
61	PWM(-) OUT (Pin10) Protect Movement Voltage	c	↑	↑	↑	d	↑	↑	Increase DC voltage for Pin4(PWM AMP OUT), Pin10 PWM pulse is made to output. Pin10(PWM(-)OUT) connect Outside power Supply through Resistance.
		↑	↑	a	↑	↑	↑	↑	Pin10 DC voltage is upped ,and measure Pin10 voltage when PWM pulse disappears.(VP10)
62	PWM(+) OUT (Pin12) Protect Movement Voltage	↑	↑	↑	↑	↑	↑	↑	Increase DC voltage for Pin4(PWM AMP OUT), Pin12 PWM pulse is made to output. Pin12(PWM(+)OUT) connect Outside power Supply through Resistance.
		↑	↑	b	↑	↑	↑	↑	Pin12 DC voltage is upped ,and measure Pin12 voltage when PWM pulse disappears.(VP12)
63	PWM(+) OCL (Pin13) Protect Movement Voltage	↑	↑	↑	↑	↑	↑	↑	SW16=b、Increase DC voltage for Pin4(PWM AMP OUT), Pin12 PWM pulse is made to output. Pin13(PWM(+)OCL) connect Outside power Supply.
		↑	↑	d	↑	↑	↑	↑	Pin13 DC voltage is upped ,and measure Pin13 voltage when PWM (+)pulse disappears.(VP13)
64	PWM(-) OCL (Pin9) Protect Movement Voltage	↑	↑	↑	↑	↑	↑	↑	SW16=b、Increase DC voltage for Pin4(PWM AMP OUT), Pin10 PWM pulse is made to output. Pin9(PWM(-)OCL) connect Outside power Supply.
		↑	↑	↑	↑	↑	↑	↑	Pin9 DC voltage is upped ,and measure Pin9 voltage when PWM (-)pulse disappears.(VP9)

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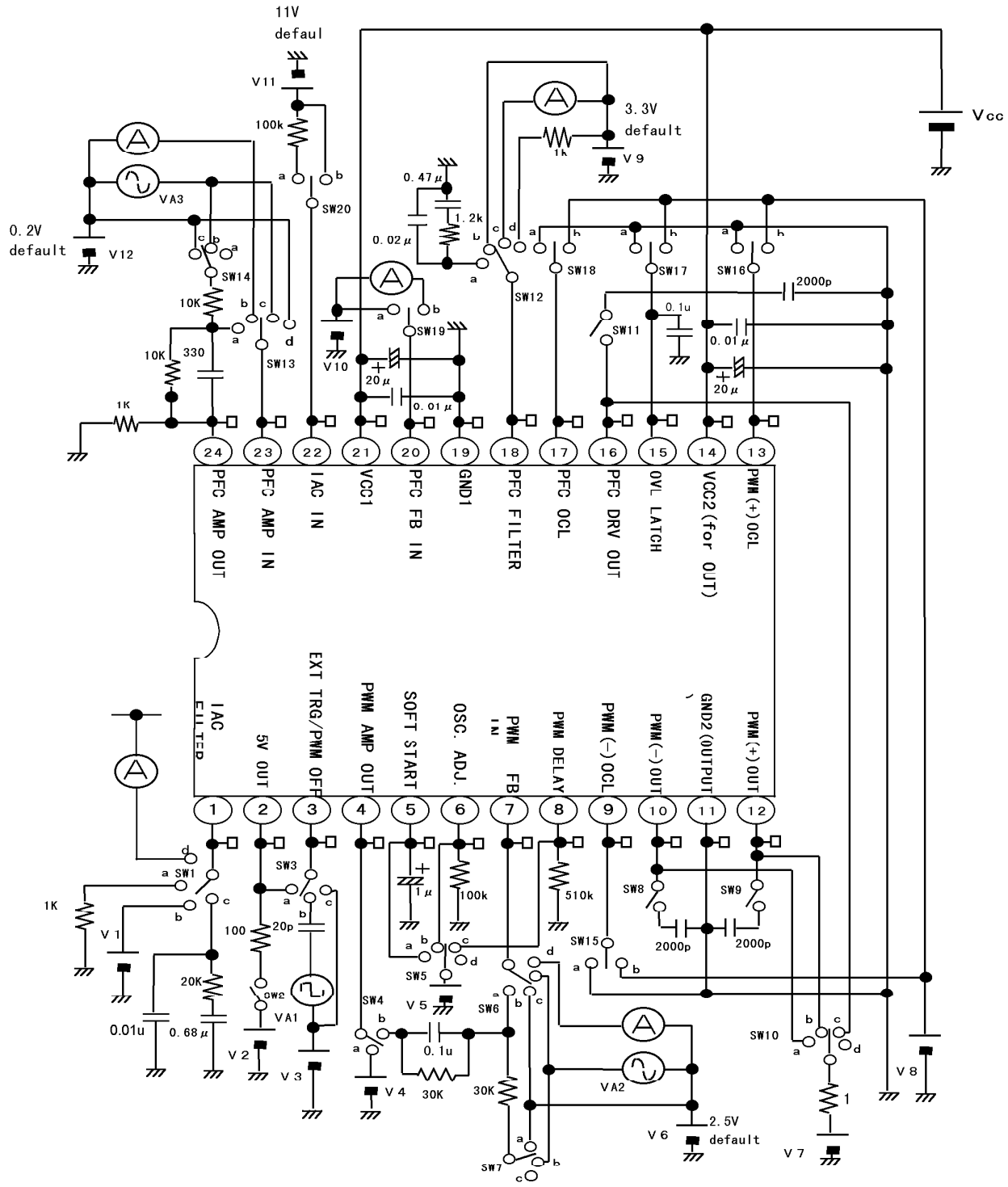
No	CHARACTERISTICS	SW MODE 1	2	3	4	5	6	7	Test Condition
		8	9	10	11	12	13	14	
65	OVL Latch (Pin15) Protect Movement Voltage	c	off	a	a	d	b	c	SW17=b、 Increase DC voltage for Pin4(PWM AMP OUT), Pin10 and Pin12 PWM pulse are made to output. Pin15(OVL LATCH) connect Outside power Supply through Resistance. Pin15 DC voltage is lowered ,and measure Pin15 voltage when PWM pulse disappears.(VP15)
		on	on	d	on	a	a	c	
66	PFC DRV OUT (Pin16) Protect Movement Voltage	b	↑	↑	b	↑	a	a	Increase DC voltage for Pin1(IAC FILTER),Pin16 PFC pulse is made to output. Pin16(PFC DRV OUT) connect Outside power Supply through Resistance. Pin16 DC voltage is upped ,and measure Pin12 voltage when PWM pulse disappears.(VP16)
		↑	↑	c	↑	↑	↑	↑	
67	PFC OCL (Pin17) Protect Movement Voltage	↑	↑	↑	↑	↑	↑	↑	Increase DC voltage for Pin1(IAC FILTER),Pin16 PFC pulse is made to output. Pin17(PFC OCL) connect Outside power Supply. Pin17 DC voltage is upped ,and measure Pin17 voltage when PWM pulse disappears.(VP17)
		↑	↑	d	↑	↑	↑	↑	



AC characteristics measurement circuit

Timing Chart of TA1294