

## Stereo Power Amplifier

### Description

The CXA1522P/M/N is a bipolar integrated circuit designed for power amplifiers of small-sized radio-cassette tape recorders. Included is a pre-amplifier, power amplifier, and an electrical volume control.

### Features

- CXA1522P: EIAJ output = 500mW (typ.),  
 $V_{CC} = 6V, R_L = 8\Omega$
- CXA1522M: EIAJ output = 110mW (typ.),  
 $V_{CC} = 3V, R_L = 8\Omega$
- CXA1522N: EIAJ output = 95mW (typ.),  
 $V_{CC} = 3V, R_L = 8\Omega$
- Built-in electronic volume control
- Built-in ripple filter (ripple rejection 34.5 dB typ.)

### Applications

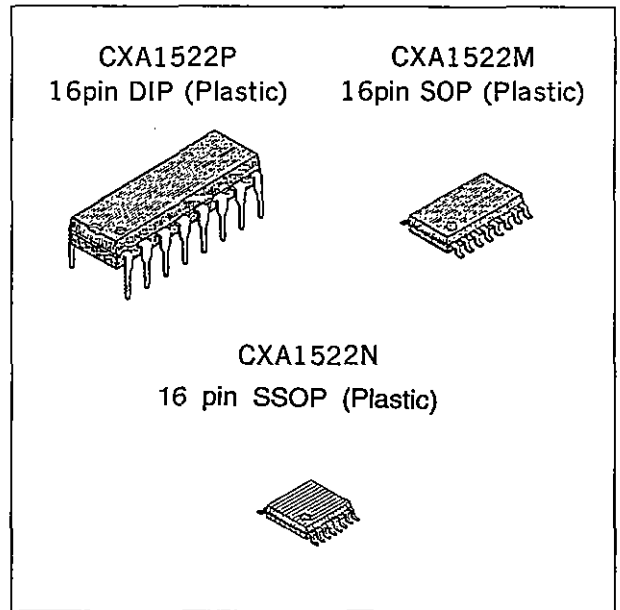
Ideal for use as a stereo radio power amplifier or a radio-cassette tape recorder/Walkman-type cassette tape player power amplifier.

### Structure

Bipolar silicon monolithic IC

### Absolute Maximum Ratings

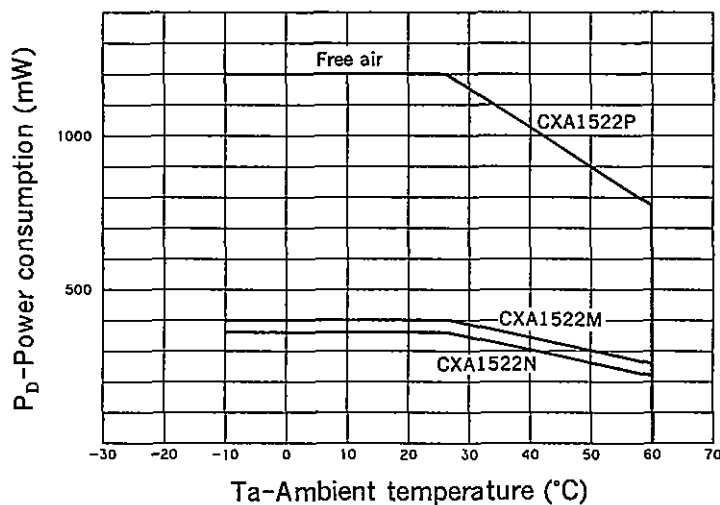
• Supply voltage	$V_{CC}$	8	V
• Operating temperature	$T_{opr}$	-10 to +60	°C
• Storage temperature	$T_{stg}$	-65 to +150	°C
• Allowable power dissipation	$P_D$	1200	mW (CXA1522P)
		410	mW (CXA1522M)
		350	mW (CXA1522N)



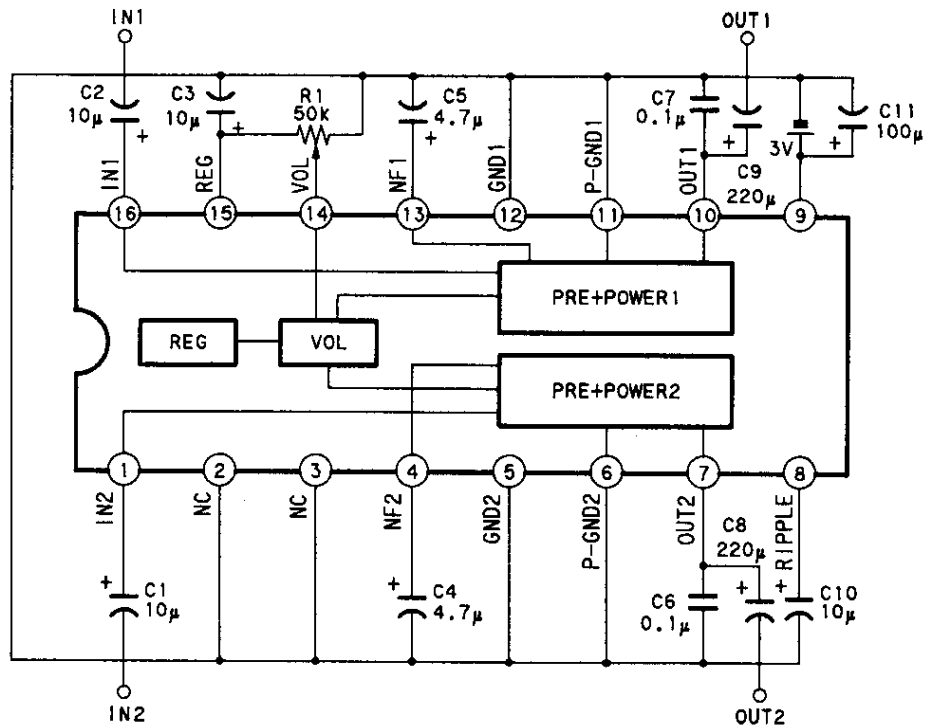
### Operating Conditions

- Supply voltage 1.8 to 7.0 V (CXA1522P)  
 1.8 to 4.5 V (CXA1522M, CXA1522N)

Power Dissipation Gradual Decrease Curve



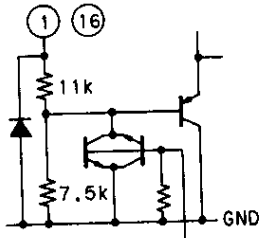
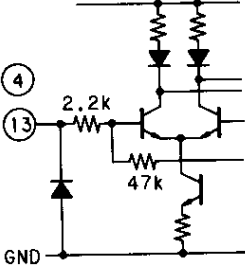
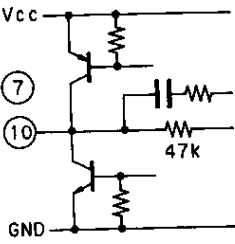
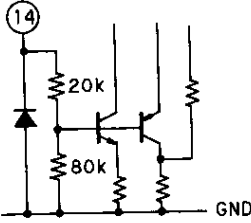
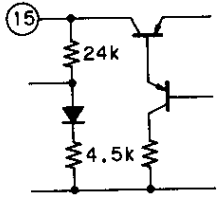
Block Diagram, Pin Configuration and Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Pin 14 DC causes the input signal to enter the preamplifier that controls the amount of attenuation. The power amplifier amplifies the signal output from the preamplifier by approximately 30dB (fixed) and generates the output.

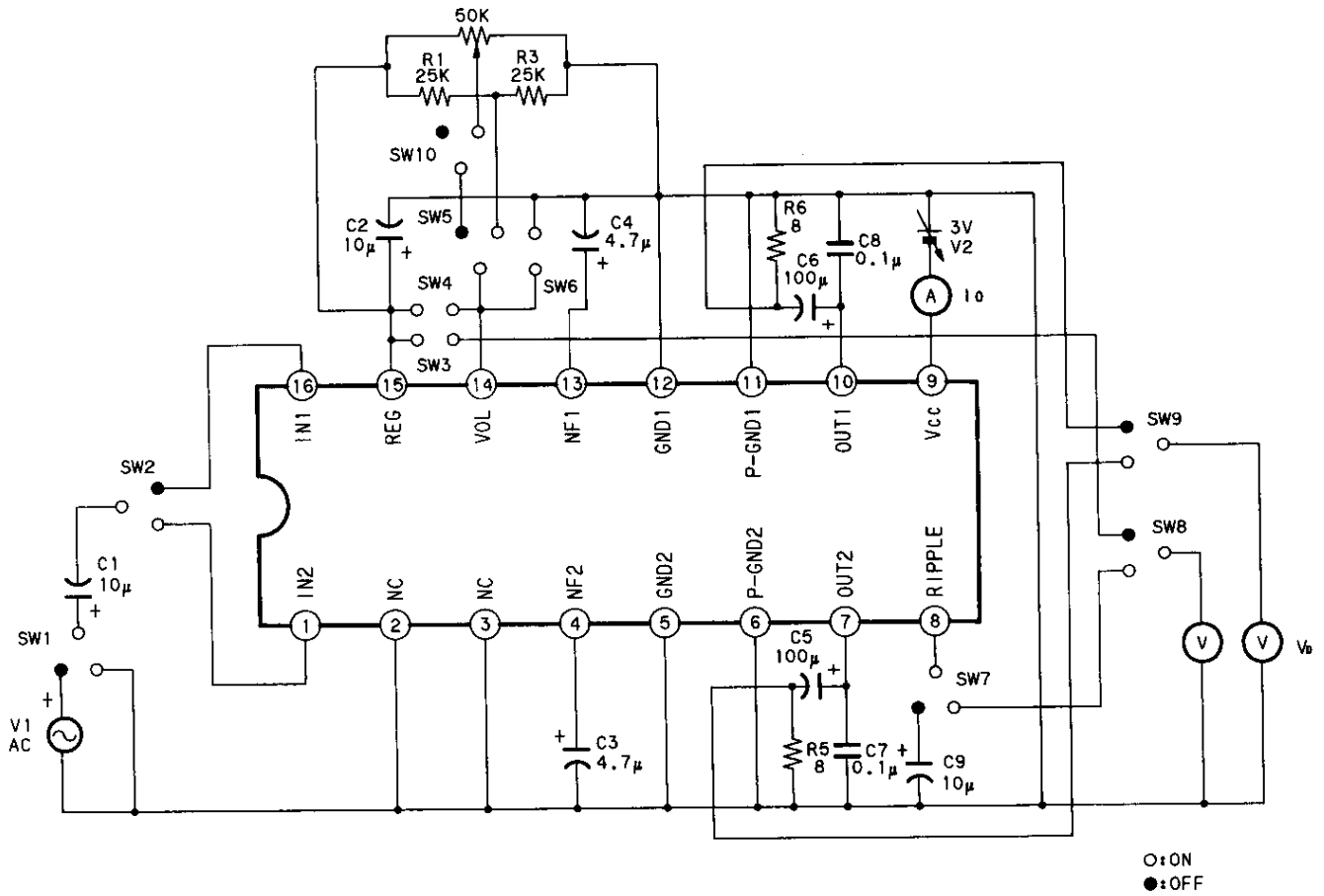
Pin Description

Pin No.	Symbol	Equivalent circuit	Pin voltage		Description
			3V	6V	
1, 16	IN1 IN2		0	0	Input pins
2, 3	NC		—	—	To be connected to the GND pin.
4, 13	NF1 NF2		1.5	3	Power amplifier NF pins A 4.7μF time constant is provided
5, 12	GND1 GND2		0	0	Preamplifier GND pins
6, 11	P-GND1 P-GND2		0	0	Power amplifier GND pins
7, 10	OUT1 OUT2		1.5	3	Power amplifier output pins
9	V <sub>CC</sub>		3	6	V <sub>CC</sub>
14	VOL		0 to 1.25	0 to 1.25	Electronic volume control pin The voltage is varied from 0 to 1.25V to change the gain
15	REG		1.25	1.25	Regulator pin

**Electrical Characteristics** (Ta = 25°C; Vcc = 6V [CXA1552P, upper line], 3V [CXA1522M, middle line], 3V [CXA1522N, lower line])

No.	Test items	SW conditions										Test point	Description of output waveform and test method	Min.	Typ.	Max.	Unit	
		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10							
1	Circuit current	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	IO	Circuit current in no-signal state	—	3.0 2.5 2.5	5.0 4.0 4.0	mA
2	Audio voltage gain (L)	OFF	→							ON			VD	VI = -30dBm, 1kHz	33.0 31.0 31.0	34.6 31.8 31.8	37.0 33.0 33.0	dB
3	Audio voltage gain (R)		ON	→						→	ON		VD	VI = -30dBm, 1kHz	33.0 31.0 31.0	34.6 31.8 31.8	37.0 33.0 33.0	dB
4	Attenuation (L)		OFF			ON	OFF				OFF		VD	VI = -30dBm, 1kHz Output difference between the maximum and center volume control settings	3.0 6.0 6.0	11.4 16.8 16.8	27.0 22.0 22.0	dB
5	Attenuation (R)		ON	→						ON			VD	VI = -30dBm, 1kHz Output difference between the maximum and center volume control settings	3.0 6.0 6.0	11.4 16.8 16.8	27.0 22.0 22.0	dB
6	EIAJ output (L)		OFF			OFF	ON				OFF	ON	VD	VI = -20dBm, 1kHz RL = 8Ω THD = 10% Output level at which the above conditions prevail	400 100 85	500 110 95	— — —	mW
7	EIAJ output (R)		ON	→							ON		VD	VI = -20dBm, 1kHz RL = 8Ω THD = 10% Output level at which the above conditions prevail	400 100 85	500 110 95	— — —	mW
8	Channel balance		→									→	VD	Balance between the L and R channels	-3	0	3	dB
9	Audio distortion factor (L)		OFF								OFF		VD	VI = -20dBm, 1kHz Distortion factor at an output level of 50mW	— — —	0.6 0.6 0.9	2.5 2.5 2.5	%
10	Audio distortion factor (R)		ON	→							ON		VD	VI = -20dBm, 1kHz Distortion factor at an output level of 50mW	— — —	0.6 0.6 0.9	2.5 2.5 2.5	%
11	Residual noise level (L)		OFF									OFF	VD	No-signal state noise level at the maximum volume control setting	—	-66	-60	dBm
12	Residual noise level (R)		ON	→							ON		VD	No-signal state noise level at the maximum volume control setting	—	-66	-60	dBm

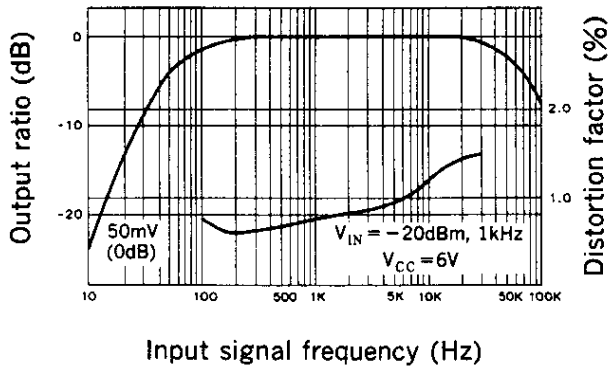
Electrical Characteristics Test Circuit



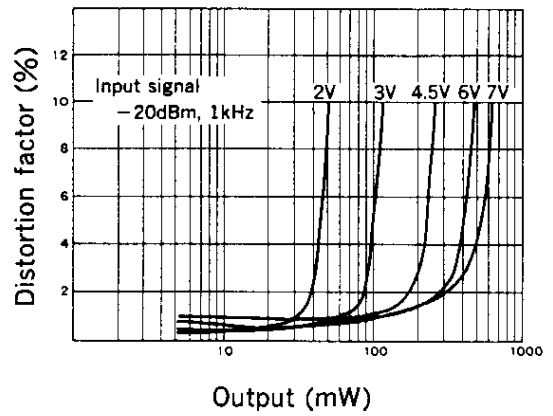
Notes on Operation

- As Pins 6 and 11 serve as the GND pins of the power amplifier output stage, ensure that the impedance of the print pattern is low.
- The phase correction capacitance provided for Pins 7 and 10 slightly varies with the print pattern.
- Because the DIP type Pin 5 doubles as a heat radiator pin, be sure to provide an ample land.

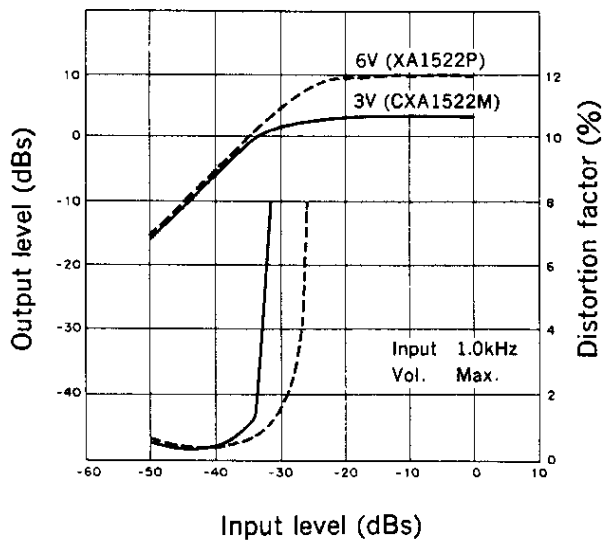
Frequency Characteristics



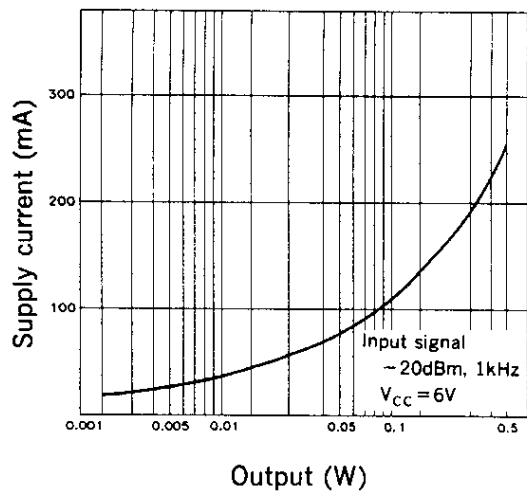
Output vs. Distortion Factor



Input vs. Output Characteristics



Output vs. Supply Current

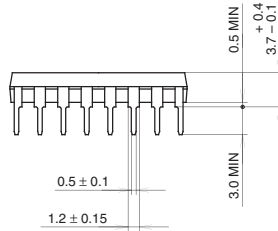
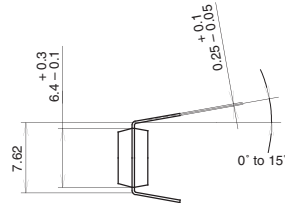
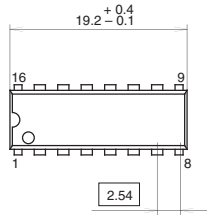


Package Outline Unit:mm

CXA1522P

16PIN DIP (PLASTIC)

Kokubu/SCT Ass'y



Two kinds of package surface:  
 1. All mat surface type.  
 2. All mirror surface type.

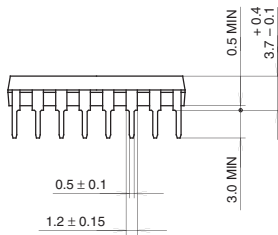
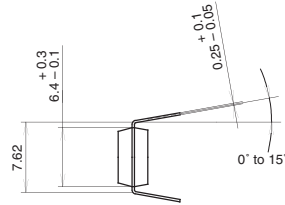
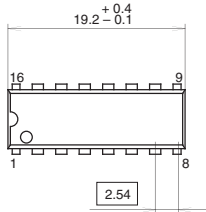
PACKAGE STRUCTURE

SONY CODE	DIP-16P-01
EIAJ CODE	DIP016-P-0300
JEDEC CODE	Similar to MO-001-AE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.0 g

16PIN DIP (PLASTIC)

SCT Ass'y



Two kinds of package surface:  
 1. All mat surface type.  
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SONY CODE	DIP-16P-01
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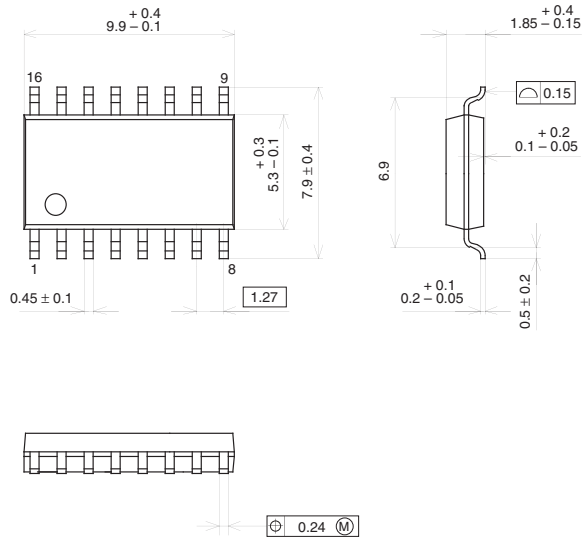
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.0 g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm

CXA1522M

16PIN SOP (PLASTIC)

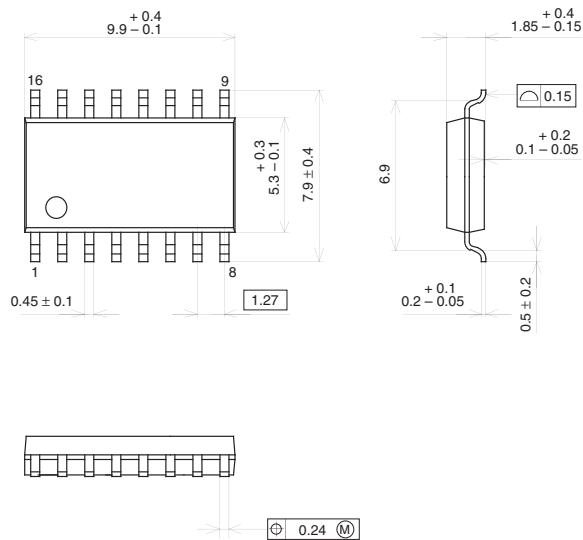


PACKAGE STRUCTURE

SONY CODE	SOP-16P-L01
EIAJ CODE	SOP016-P-0300
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

16PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-16P-L01
EIAJ CODE	SOP016-P-0300
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

LEAD PLATING SPECIFICATIONS

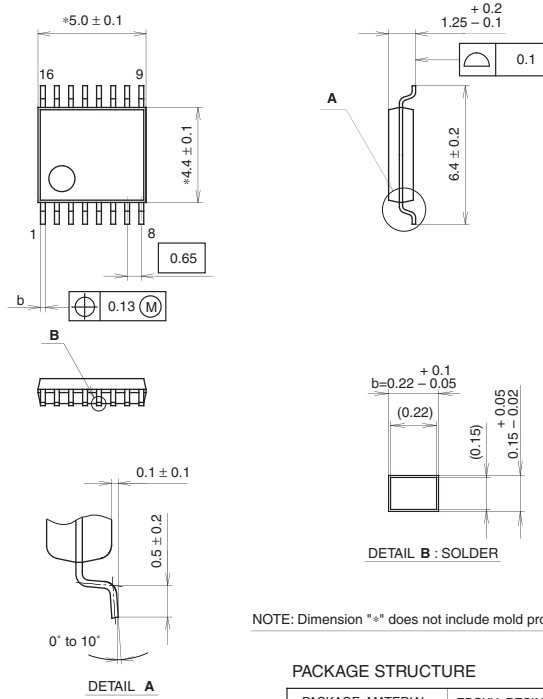
ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm



CXA1522N

16PIN SSOP (PLASTIC)

Kokubu/SCT Ass'y



NOTE: Dimension "\*" does not include mold protrusion.

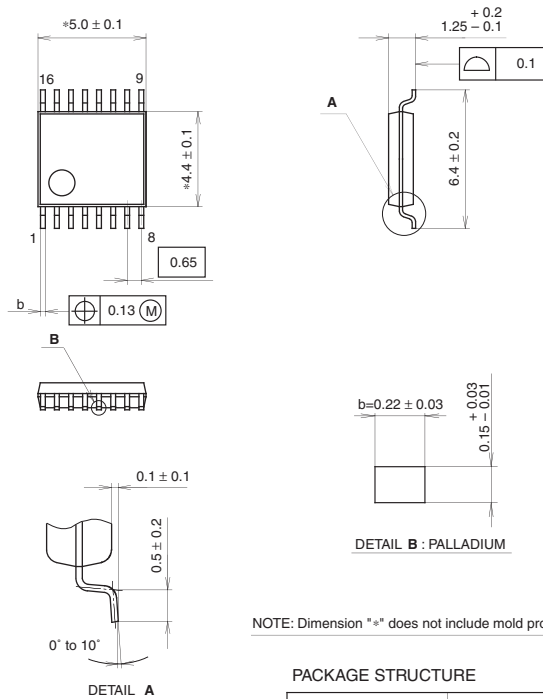
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP16-P-0044
JEDEC CODE	

SCT Ass'y

16PIN SSOP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

SONY CODE	SSOP-16P-L01
EIAJ CODE	P-SSOP16-4.4x5.0-0.65
JEDEC CODE	