The V850 Series of high-performance microcontrollers answers many different application system needs. It realizes superlatively low power consumption and low noise while offering high performance and a wide array of functions. The broad V850 product lineup provides optimum solutions for the next-generation systems of customers.
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**V850 Series Product Roadmap**

- **High-end lineup**
  - **V850E2 core**
    - Frequency: 200 to 400 MHz
  - **V850E1 core**
    - Frequency: 16 to 64 MHz
  - **V850 core**
    - Frequency: 150 MHz @ 215 MIPS
    - Memory size: ROM: ROM-less to 640 KB
    - Memory size: RAM: 4 to 48 KB
    - PKG: 64 to 257 pins (QFP & FBGA)
  - **V850ES core**
    - Frequency: 20 MHz @ 29 MIPS
    - Memory size: ROM: 64 to 256 KB
    - Memory size: RAM: 4 to 16 KB
    - PKG: 64 to 144 pins (QFP)

- **Middle-range lineup**
  - **V850 core**
    - Frequency: 33 MHz @ 38 MIPS
    - Memory size: ROM: ROM-less to 640 KB
    - Memory size: RAM: 4 to 48 KB
    - PKG: 100 to 144 pins (QFP & FBGA)

- **Low-end lineup**
  - **V850ES core**
    - Frequency: 20 MHz
    - Memory size: ROM: 64 to 256 KB
    - Memory size: RAM: 4 to 16 KB
    - PKG: 64 to 144 pins (QFP)

- **ASSP lineup**
  - **High performance: On-chip MEMC/DMA**
    - Frequency: 33 to 150 MHz
    - Memory size: ROM: ROM-less to 512 KB
    - Memory size: RAM: 4 to 128 KB
    - PKG: 100 to 240 pins (QFP & FBGA)

- **Realization of low EMI noise**
  - Frequency: 20 to 34 MHz
  - Memory size: ROM: ROM-less to 640 KB
  - Memory size: RAM: 4 to 48 KB
  - PKG: 100 to 144 pins (QFP & FBGA)

- **High cost-performance**
  - Frequency: 20 MHz
  - Memory size: ROM: 64 to 256 KB
  - Memory size: RAM: 4 to 16 KB
  - PKG: 64 to 144 pins (QFP)

- **Inverter control**
- **DVC control**
- **Car audio control**
- **Power meter control**
- **Dashboard control**
  - Frequency: 16 to 64 MHz
  - Memory size: ROM: ROM-less to 640 KB
  - Memory size: RAM: 4 to 48 KB
  - PKG: 64 to 257 pins (QFP & FBGA)

- **Roadmap/Features**
  - Continuously evolving V850 Series through an expanding product lineup
  - High-end lineup
  - Middle-range lineup
  - Low-end lineup
  - ASSP lineup
  - Standard lineups
  - Field-specific lineups
The V850 Series is suitable for various application fields and raises the commercial value of customer systems.

### Automotive
- Engines, dashboards, power steering, ABS

### Audio
- Car audio, portable audio, component stereo systems

### Portable devices
- PDA, IC recorders

### Camera
- DVC, DSC, SLR cameras

### Computer peripherals
- Laser-beam printers, inkjet printers, scanners, fax machines

### Home appliances
- Air conditioners, refrigerators, washing machines, microwave ovens

### Industrial equipment
- Industrial motors, control equipment, vending machines, power meters

### Video and recording equipment
- DVD players, D-VHS, industrial cameras

### Other
- Electronic instruments, electric bidets, toys, learning devices, remote controllers, etc.
5 Keys of V850

High performance

- Performance ranging from 20 to over 300 MIPS with single instruction set
- Compared to 8-/16-bit microcontroller, offer a MIPS performance 10 or more times higher for the same frequency, and 2 to 3 times higher at the actual application level (based on NEC evaluation)
- System operation at frequencies 1/2 to 1/3 those of 8-/16-bit microcontrollers is enabled, contributing to lowering system power consumption.
- The V850 core, V850ES core, V850E1 core, and V850E2 core are upward compatible at the object level.

Product lineup

Low-end/Middle-range/High-end/ASSP deployment

- Low-end lineup: Kx1 Series of general-purpose microcontrollers for 16 to 32-bit market designed for high cost-performance.
- Middle-range lineup: Low noise, low power consumption, large-capacity memory lineup, low-voltage operation support
- High-End lineup: Designed for high performance, on-chip memory controller and DMA
- ASSP lineup: Field-specific product lineup, on-chip dedicated hardware

Additional functions

Rich middleware lineup

- Realization of systems with high added value through the addition of supplementary functions to existing systems via middleware
- Realization of functions heretofore realized with peripheral ICs through V850 + middleware, reducing development time and reducing system costs
- Rich lineup of video, audio, network-related, and other middleware tuned for V850 Series
The V850 Series is also being actively expanded for ASIC CPU cores, realizing smooth transition to system LSIs.

The following elements essential for system LSIs are provided on a timely basis:
1. Leading-edge process technology
2. High-performance CPU core
3. Rich lineup of IP cores
4. Top-down design environment
5. Flexible application design

The following development environments are available:

- **IECUBE™**, a low-cost high-performance emulator, and N-Wire CARD, an ultra-low cost on-chip emulator are available.
- Realization of better connectivity with target boards, addition of GUI customization function, improved online help, etc.
- Realization of shorter development TAT through support of quick and accurate software development via a rich development environment lineup featuring easy operation and sophisticated functions.

**V850**
- Performance (MIPS)
  - 0.13 µm process
  - 0.18 µm process
  - 0.25 µm process
  - 0.35 µm process

**Next-generation core**
- 800 to 1000 MIPS

**V850E2**
- N85E2
  - 400 MHz
- N85E2
  - 200 MHz
- V850E2/xxx

**V850E1**
- N85E
  - 150 MHz
- N85E
  - 66 MHz
- V850E/MA1
  - MA1
- MA2
- MA3

**Development environment**
- Utilization of existing functions
- Improved usability
- Improved performance
- Debugging support
- Improved usability
- Support of high-speed PC I/F

**V850 products**
- Realization of high-performance powerful development environment making use of:
  - High performance
  - General-purpose registers
  - Large memory capacity

**System LSI**
- Smooth transition to system LSIs

**Design environment**
- Chip design environment
- Synthesis/verification
- Software development environment
- Hardware/software coordinated design

**IP cores**
- MPU, DSP, DRAM, SRAM, AV, communication, BUS, high-speed I/O

**Middleware**
- Voice recognition/synthesis
- AV processing
  - JPEG1, MPEG1, etc.
- Modem

**Chip design environment**
- Synthesis/verification

**Software development environment**
- Hardware/software coordinated design

**Processors**
- Micro-fabrication technology
- Multi-layer wiring technology
- Mixed-process technology
- High-pin-count packages

**Middleware**
- Voice recognition/synthesis
- AV processing
  - JPEG1, MPEG1, etc.
- Modem
Kx1 Series of general-purpose microcontrollers for 16 to 32-bit market designed for high cost-performance

**Low-End Lineup**

- Rich memory and package lineup
- Large array of on-chip peripheral functions common with 78K0/Kx1 of 8-bit microcontrollers
- Low EMI noise design
- Development environment usable in common for all series
- Wide voltage range support (2.7 to 5.5 V)
- Single-power-supply flash lineup (self programming, EEPROM™ emulation support)

**Kx1 Series lineup**

- Rich memory & package lineup
- Low EMI noise design
- Seamless lineup
- Rich memory & package lineup

**Kx1+ features**

- Runaway detection function: Watchdog timer running on main clock
- Voltage detection circuit: None
- Reset functions: External reset, WDT reset
- DMA function: None
- Oscillation stabilization: Fixed at reset release
- A/D converter: Conversion time 14 μs (min.)
- LIN bus interface: No hardware

**Product specifications**

<table>
<thead>
<tr>
<th>Item</th>
<th>V850ES/KE1</th>
<th>V850ES/KF1</th>
<th>V850ES/KG1</th>
<th>V850ES/KJ1</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU core</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
</tr>
<tr>
<td>Performance</td>
<td>24 MHz (5 x 20 MHz)</td>
<td>24 MHz (5 x 20 MHz)</td>
<td>24 MHz (5 x 20 MHz)</td>
<td>24 MHz (5 x 20 MHz)</td>
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<tr>
<td>Maximum clock frequency</td>
<td>20 MHz (5 x 20 MHz)</td>
<td>20 MHz (5 x 20 MHz)</td>
<td>20 MHz (5 x 20 MHz)</td>
<td>20 MHz (5 x 20 MHz)</td>
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<tr>
<td>Reset/external reset</td>
<td>integral</td>
<td>integral</td>
<td>integral</td>
<td>integral</td>
</tr>
<tr>
<td>I2C</td>
<td>supported</td>
<td>supported</td>
<td>supported</td>
<td>supported</td>
</tr>
<tr>
<td>UART/I2C</td>
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<td>supported</td>
<td>supported</td>
<td>supported</td>
</tr>
<tr>
<td>Power consumption, real-time</td>
<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
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<tr>
<td>Power consumption, real-time</td>
<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
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<tr>
<td>Power consumption, real-time</td>
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<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
</tr>
<tr>
<td>Power consumption, real-time</td>
<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
<td>100 mW (5 x 20 MHz)</td>
</tr>
</tbody>
</table>

*Only Y products have an on-chip FC interface.*
### System cost reduction

**Conventional set**
- Voltage detector
- Voltage drop detection
- WDT independent from CPU clock
- System reset voltage detection

**Kx1 Series**
- More functions on a single chip
- Lower number of used ports

**Set space reduction!**  
**Total set cost reduction!**  
**Higher reliability!!!**

**Peripheral functions on single chip**
- Reset IC
- System reset monitoring
- Oscillation stop monitoring

**Common peripheral functions**

Large array of peripheral functions common with 8-bit 78K0 Series

<table>
<thead>
<tr>
<th>Item</th>
<th>V850ES/Kx1+</th>
<th>K1+</th>
<th>KF1+</th>
<th>K1S+</th>
<th>K1J+</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU core</td>
<td>V850ES</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Performance</td>
<td>20 MIPS (16 MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum operating frequency</td>
<td>20 MHz (main clock)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal flash memory</td>
<td>128 KB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal flash PDM</td>
<td>128 KB</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Power supply voltage</td>
<td>4.5 V to 5.5 V @ 20 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>External bus</td>
<td>128 KB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer/counter</td>
<td>16-bit/2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC</td>
<td>16-bit/2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watch timer</td>
<td>16-bit/2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial interface</td>
<td>16-bit/2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UART</td>
<td>16-bit/2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPI</td>
<td>16-bit/2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>I2C</td>
<td>16-bit/2 ch</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>ADC</td>
<td>16-bit/2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watch monitor</td>
<td>16-bit/2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power consumption</td>
<td>16-bit/2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td>64-pin TQFP (12x12 mm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>80-pin QFP (12x16 mm)</td>
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</tr>
<tr>
<td></td>
<td>80-pin QFP (14x14 mm)</td>
<td></td>
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</tr>
<tr>
<td></td>
<td>100-pin QFP (14x14 mm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>144-pin LQFP (28x28 mm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Only Y products have an on-chip I²C interface.
### Middle Range Lineup

**Large-capacity memory, 2.5 V/3 V/5 V general-purpose product lineup**

#### Single-power-supply flash
- Larger capacity memory
- Enhanced peripheral functions

#### 5 V general-purpose, low noise

#### Low voltage, super-low power consumption

---

#### Product specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>V850ES/Sx2</th>
<th>V850ES/Sx2</th>
<th>µPD703229Y</th>
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<tbody>
<tr>
<td>CPU core</td>
<td>29 MHz (20 MHz)</td>
<td>29 MHz (20 MHz)</td>
<td>25 MHz (20 MHz)</td>
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<tr>
<td>Memory</td>
<td>32 KB/16 KB</td>
<td>32 KB/16 KB</td>
<td>32 KB/16 KB</td>
</tr>
<tr>
<td>Flash memory</td>
<td>256 KB/16 KB</td>
<td>256 KB/16 KB</td>
<td>256 KB/16 KB</td>
</tr>
<tr>
<td>External ROM</td>
<td>16 KB/8 KB</td>
<td>16 KB/8 KB</td>
<td>16 KB/8 KB</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>3.3 V to 5.5 V</td>
<td>3.3 V to 5.5 V</td>
<td>3.3 V to 5.5 V</td>
</tr>
<tr>
<td>External bus</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer/counter</td>
<td>16-bit/14-bit</td>
<td>16-bit/14-bit</td>
<td>16-bit/14-bit</td>
</tr>
<tr>
<td>Watch timer</td>
<td>1-bit/1-bit</td>
<td>1-bit/1-bit</td>
<td>1-bit/1-bit</td>
</tr>
<tr>
<td>UART</td>
<td>3 ch, 2-ch UART</td>
<td>3 ch, 2-ch UART</td>
<td>3 ch, 2-ch UART</td>
</tr>
<tr>
<td>CSI</td>
<td>1 ch, 2-ch P8 interface</td>
<td>1 ch, 2-ch P8 interface</td>
<td>1 ch, 2-ch P8 interface</td>
</tr>
<tr>
<td>Serial interface</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UART</td>
<td>1 ch, 2-ch UART</td>
<td>1 ch, 2-ch UART</td>
<td>1 ch, 2-ch UART</td>
</tr>
<tr>
<td>USB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPI</td>
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<tr>
<td>I²C</td>
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<td></td>
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<td>GPIO</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Application code memory</td>
<td>256 KB/128 KB</td>
<td>256 KB/128 KB</td>
<td>256 KB/128 KB</td>
</tr>
<tr>
<td>RAM</td>
<td>384 KB/256 KB</td>
<td>384 KB/256 KB</td>
<td>384 KB/256 KB</td>
</tr>
<tr>
<td>Power consumption</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU core</td>
<td>66 mW (20 MHz @ 3.3 V)</td>
<td>66 mW (20 MHz @ 3.3 V)</td>
<td>66 mW (20 MHz @ 3.3 V)</td>
</tr>
<tr>
<td>Memory</td>
<td>100 mW (20 MHz@3.3 V)</td>
<td>100 mW (20 MHz@3.3 V)</td>
<td>100 mW (20 MHz@3.3 V)</td>
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<tr>
<td>Package</td>
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<tr>
<td>100-pin QFP (14 x 14 mm)</td>
<td>100-pin QFP (14 x 14 mm)</td>
<td>100-pin QFP (14 x 14 mm)</td>
<td></td>
</tr>
<tr>
<td>121-pin FBGA (12 x 12 mm)</td>
<td>121-pin FBGA (12 x 12 mm)</td>
<td>121-pin FBGA (12 x 12 mm)</td>
<td></td>
</tr>
</tbody>
</table>

Note: Products without automotive bus, products with on-chip I²C bus, and products with on-chip aFCAN are available.
**V850ES/SG2, SJ2**

- Low EMI noise
- 20 MHz @ 2.85 to 3.6 V operation
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting the N-ch open-drain output
- On-chip large-capacity single-power-supply flash memory
- ROM/RAM: 256 KB/16 KB (SA2, SA3), 128 K/8 KB (SA2 mask ROM version)
- Thin and compact package support: 100-pin TQFP/121-pin FBGA (SA3)

**V850ES/SA2, SA3**

- Min. 2.2 V low-voltage operation (including A/D, D/A converter, flash)
- Low power consumption and high-speed operation during 38 mW @ 2.5 V, 20 MHz operation
- Single-power-supply flash
- ROM/RAM: 256 KB/16 KB, 128 KB/4 KB, 64 KB/2 KB, 32 KB/2 KB
- Large-capacity memory (ROM/RAM: 256 KB/8 KB, 128 KB/4 KB, 64 KB/4 KB)
- 100-pin QFP/100-pin LQFP

**V850/SB1**

- Low EMI noise
- Large-capacity memory and large memory selection
- ROM/RAM: 512 KB/24 KB, 384 KB/24 KB, 256 KB/16 KB, 128 KB/8 KB
- 100-pin QFP/100-pin LQFP

**V850/SC1**

- Low EMI noise
- Large-capacity memory (ROM/RAM: 512 KB/24 KB)
- Enhanced peripheral functions for SB1
- 144-pin LQFP
# Product Lineup

## Features

**V850E/ME2**
- 215 MIPS @ 150 MHz, internal 1.5 V/external 3.3 V operation ROM-less microcontroller
- Large-capacity internal RAM (128 KB), real-time control
- On-chip SSCG*, EMI peak reduction
- USB full-speed (function), on-chip debugging function
- On-chip SDRAM interface
- 176-pin LQFP/240-pin FBGA

*Spread Spectrum Frequency Synthesizer Clock Generator

**V850E/MA1,MA2**
- 67 MIPS @ 50 MHz, Internal 3.3 V/external 5 V tolerant operation single-chip microcontroller (MA1)
- ROM-less product lineup also available
- 40 MHz @ 3.3 V ROM-less microcontroller (MA2)
- On-chip SDRAM interface, DMA
- 144-pin LQFP/161-pin FBGA (MA1), 100-pin LQFP (MA2)

**V850E/MA3**
- 106 MIPS @ 80 MHz, internal 2.5 V/external 3.3 V operation single-chip microcontroller
- Large-capacity internal ROM/RAM (512 KB/32 KB)
- Internal single power supply flash
- SDRAM interface, motor control function, on-chip debugging function
- 144-pin LQFP/161-pin FBGA

**V850E/MS1,MS2**
- 47 MIPS @ 33 MHz, 3.3 V & 5 V single-chip microcontroller (MS1)
- ROM-less product (Max. 40 MHz) lineup available
- 33 MHz @ internal 3.3 V/external 5 V ROM-less microcontroller (MS2)
- ROM/RAM: 128 KB/4 KB (MS1), ROM-less/4 KB (MS1, MS2)
- On-chip SDRAM interface, DMA
- 144-pin LQFP/157-pin FBGA (MS1)/100-pin LQFP (MS2)

## Product specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>V850E/ME2</th>
<th>V850E/MA1</th>
<th>V850E/MA2</th>
<th>V850E/MA3</th>
<th>V850E/MS1</th>
<th>V850E/MS2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Performance</td>
<td>215 MIPS</td>
<td>106 MIPS</td>
<td>67 MIPS</td>
<td>47 MIPS</td>
<td>33 MIPS</td>
<td>33 MIPS</td>
</tr>
<tr>
<td>(op @ 150 MHz)</td>
<td>@ 80 MHz</td>
<td>@ 80 MHz</td>
<td>@ 50 MHz</td>
<td>@ 33 MHz</td>
<td>@ 215 MHz</td>
<td>@ 215 MHz</td>
</tr>
<tr>
<td>Maximum operating frequency</td>
<td>90 MHz</td>
<td>90 MHz</td>
<td>40 MHz</td>
<td>40 MHz</td>
<td>40 MHz</td>
<td>40 MHz</td>
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<tr>
<td>Memory capacity</td>
<td>102 KB</td>
<td>256 KB</td>
<td>256 KB</td>
<td>102 KB</td>
<td>102 KB</td>
<td>102 KB</td>
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<tr>
<td>External bus</td>
<td>128 KB</td>
<td>256 KB</td>
<td>256 KB</td>
<td>128 KB</td>
<td>128 KB</td>
<td>128 KB</td>
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<tr>
<td>Internal RAM</td>
<td>32 KB/16 KB</td>
<td>33 KB Rom</td>
<td>32 KB/16 KB</td>
<td>4 KB</td>
<td>4 KB</td>
<td>4 KB</td>
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<tr>
<td>Power supply voltage</td>
<td>1.35 V to 1.85 V (external)</td>
<td>2.3 V to 2.7 V (external)</td>
<td>3.0 V to 3.6 V (external)</td>
<td>3.0 V to 3.6 V (external)</td>
<td>3.0 V to 3.6 V (internal)</td>
<td>3.0 V to 3.6 V (internal)</td>
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<tr>
<td>Memory controller</td>
<td>SDRAM, RAM, etc.</td>
<td>SDRA M, RAM, etc.</td>
<td>SDRA M, EDO DRAM, RAM, etc.</td>
<td>EDO DRAM, RAM, etc.</td>
<td>EDO DRAM, RAM, etc.</td>
<td>EDO DRAM, RAM, etc.</td>
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<tr>
<td>External bus</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
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<td>Internal bus</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
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<tr>
<td>Sensor interface</td>
<td>8 bits/16 bits</td>
<td>16 bits/32 bits</td>
<td>16 bits/32 bits</td>
<td>16 bits/32 bits</td>
<td>16 bits/32 bits</td>
<td>16 bits/32 bits</td>
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<tr>
<td>ADC converter</td>
<td>10 bits</td>
<td>10 bits</td>
<td>10 bits</td>
<td>10 bits</td>
<td>10 bits</td>
<td>10 bits</td>
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<tr>
<td>RAM controller</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
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<tr>
<td>Other peripheral functions</td>
<td>102 ch (on-chip debugging function (with trace), PWM output 2 ch)</td>
<td>2 ch</td>
<td>2 ch</td>
<td>2 ch</td>
<td>2 ch</td>
<td>2 ch</td>
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<tr>
<td>Power consumption</td>
<td>50 mW (150 MHz @ 1.5 V)</td>
<td>65 mW (50 mW @ 3.3 V)</td>
<td>112 mW (40 MHz @ 3.3 V)</td>
<td>112 mW (40 MHz @ 3.3 V)</td>
<td>218 mW (33 MHz @ 3.3 V)</td>
<td>218 mW (33 MHz @ 3.3 V)</td>
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<tr>
<td>Package</td>
<td>144-pin LQFP (24 x 24 mm)</td>
<td>168-pin LQFP (20 x 20 mm)</td>
<td>144-pin LQFP (50 x 50 mm)</td>
<td>144-pin LQFP (50 x 50 mm)</td>
<td>144-pin LQFP (20 x 20 mm)</td>
<td>144-pin LQFP (20 x 20 mm)</td>
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</tbody>
</table>

* Only Y products have an on-chip FG interface.
Application examples

- **MFP (Multifunction printer)**

  **Multi Function Printer V850E/ME2**

- **Thermal printer**

  **Thermal Printer V850E/MA3**

- **DVD player**

  **DVD Player V850E/MA2**

- **Fax machine**

  **FAX Machine V850E/MS1**
### Features

#### V850E/IA3, IA4

- For inverter control
- 82 MIPS @ 64 MHz, internal 2.5 V/external 5 V operation
- On-chip 6-phase sinusoidal PWM timer, on-chip operational amplifier/comparator, on-chip high-speed A/D
- On-chip debugging function (IA4 only)
- ROM/RAM: 256 KB/12 KB, 128 KB/6 KB (mask ROM version only)
- On-chip debugging and ROM correction functions
- 80-pin QFP (IA3), 100-pin LQFP/100-pin QFP (IA4)

#### V850ES/IK1

- For inverter control
- 41 MIPS @ 32 MHz, 4.5 V to 5.5 V (on-chip regulator)
- On-chip 6-phase sinusoidal PWM timer, POC/LVI, and clock monitor functions
- ROM/RAM: 128 KB/6 KB, 64 KB/4 KB
- 64-pin LQFP

### Product specifications

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<th>V850E/IA3</th>
<th>V850ES/IA4</th>
<th>V850ES/IK1</th>
<th>V850ES/PM1</th>
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<tbody>
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<td>CPU core</td>
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<td>V850E</td>
<td>V850E</td>
<td>V850E</td>
<td>V850E/IK1</td>
<td>V850E/PM1</td>
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<tr>
<td>Performance</td>
<td>67 MIPS (60 MHz)</td>
<td>64 MIPS (60 MHz)</td>
<td>82 MIPS (64 MHz)</td>
<td>82 MIPS (64 MHz)</td>
<td>81 MIPS (64 MHz)</td>
<td>55 MIPS (64 MHz)</td>
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<td>Memory bandwidth</td>
<td>256 KB</td>
<td>128 KB</td>
<td>256 KB</td>
<td>256 KB</td>
<td>256 KB</td>
<td>512 KB</td>
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<tr>
<td>Internal main ROM</td>
<td>256 KB</td>
<td>128 KB</td>
<td>256 KB</td>
<td>256 KB</td>
<td>256 KB</td>
<td>256 KB</td>
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<tr>
<td>Power supply voltage</td>
<td>3.5 V to 5.5 V (internal)</td>
<td>4.5 V to 5.5 V (external)</td>
<td>3.5 V to 5.5 V (internal)</td>
<td>4.5 V to 5.5 V (internal)</td>
<td>4.5 V to 5.5 V (internal)</td>
<td>4.5 V to 5.5 V (internal)</td>
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<td>Address: Multiplexed</td>
<td>Address: Multiplexed</td>
<td>Address: Multiplexed</td>
<td>Address: Multiplexed</td>
<td>Address: Multiplexed</td>
</tr>
<tr>
<td>Timer/counter</td>
<td>16-bit</td>
<td>16-bit</td>
<td>16-bit</td>
<td>16-bit</td>
<td>16-bit</td>
<td>16-bit</td>
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<tr>
<td>Serial interface</td>
<td>C/Si/UART = 3 ch</td>
<td>C/Si/UART = 3 ch</td>
<td>C/Si/UART = 1 ch</td>
<td>C/Si/UART = 1 ch</td>
<td>C/Si/UART = 1 ch</td>
<td>C/Si/UART = 1 ch</td>
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<td>SPI/IC/SSP</td>
<td>10-bit (6-bit)</td>
<td>10-bit (6-bit)</td>
<td>10-bit (6-bit)</td>
<td>10-bit (6-bit)</td>
<td>10-bit (6-bit)</td>
<td>10-bit (6-bit)</td>
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<td>I/O pins</td>
<td>44-pin</td>
<td>44-pin</td>
<td>44-pin</td>
<td>44-pin</td>
<td>44-pin</td>
<td>64-pin</td>
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<td>Optional peripheral functions</td>
<td>TCAW/TDR</td>
<td>TCAW/TDR</td>
<td>TCAW/TDR</td>
<td>TCAW/TDR</td>
<td>TCAW/TDR</td>
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<tr>
<td>Power consumption</td>
<td>15 mW</td>
<td>20 mW</td>
<td>150 mW</td>
<td>170 mW</td>
<td>175 mW</td>
<td>175 mW</td>
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<td>Package</td>
<td>144-pin LQFP (100×15 mm)</td>
<td>100-pin LQFP (14×14 mm)</td>
<td>100-pin LQFP (14×14 mm)</td>
<td>100-pin LQFP (14×14 mm)</td>
<td>100-pin LQFP (14×14 mm)</td>
<td>100-pin LQFP (14×14 mm)</td>
</tr>
</tbody>
</table>

#### Inverter control

- On-chip inverter and timer

#### DVC control

- On-chip VCR servo timer

#### Power meter instrument measuring control

- On-chip 16-bit ΔΣADC

**For camcorders (incl. DVC)**

- 32-bit servo timer ideal for camcorder control, boundary scan function, on-chip debugging function, and many other on-chip peripheral functions
- 55 MIPS @ 40.5 MHz, 2.5 V low-voltage/high-speed operation
- Large-capacity memory (ROM/RAM: 512 KB/24 KB)
- Internal single-power-supply flash
- Compact high-pin-count 257-pin FBGA (14×14 mm, 0.65 mm pitch)

**For power meter control**

- On-chip high-resolution, high-accuracy 16-bit ΔΣADC
- ROM/RAM: 128 KB/10 KB, ROM-less/10 KB
- 29 MIPS @ 20 MHz, 3.0 V to 3.6 V operation
- 100-pin LQFP
### Application examples

#### Air conditioner

**V850E/IA4**
- **Compressor motor**
- **Power module**
- **Fan motor**

#### Digital Video Camera

**V850E/SV2**
- **Camera control block**
- **Camera DSP block**
- **Moving picture processing block**

#### Power meter

**V850ES/PM1**
- **Main power 20 MHz**
- **Subclock 32 kHz**

---

### Technical Specifications

<table>
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<tr>
<th>Item</th>
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<th>V850E/SV2</th>
<th>V850ES/PM1</th>
</tr>
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<tbody>
<tr>
<td>CPU type</td>
<td>V850</td>
<td>V850E1</td>
<td>V850ES</td>
</tr>
<tr>
<td>Performance</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>55 MIPS (@ 40.5 MHz)</td>
<td>29 MIPS (@ 20 MHz)</td>
</tr>
<tr>
<td>Frequency</td>
<td>20 MHz</td>
<td>40.5 MHz</td>
<td>20 MHz</td>
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<tr>
<td>On-chip flash ROM</td>
<td>384 KB/256 KB</td>
<td>512 KB</td>
<td>192 KB</td>
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<tr>
<td>Internal flash ROM</td>
<td>32 KB</td>
<td>32 KB</td>
<td>32 KB</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>3.1 V to 3.6 V @ 20 MHz, 2.7 V to 3.6 V @ 16 MHz</td>
<td>3.1 V to 3.6 V @ 20 MHz, 2.7 V to 3.6 V @ 16 MHz</td>
<td>2.3 V to 3.6 V @ 2.7 MHz, 2.7 V to 3.6 V @ 32.768 kHz</td>
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<tr>
<td>External bus</td>
<td>Address: Multiplexed</td>
<td>Address: Multiplexed/separate</td>
<td>Address: Separate</td>
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<tr>
<td>Data:</td>
<td>16 bits</td>
<td>8/16 bits</td>
<td>32-bit</td>
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<tr>
<td>Timer/counter</td>
<td>24-bit</td>
<td>16-bit</td>
<td>16-bit</td>
</tr>
<tr>
<td>Serial interface</td>
<td>CSI = 1 ch, CSUAR = 2 ch, CSUH = 2 ch</td>
<td>CSI = 5 ch, CSIUR = 2 ch, UAR1 = 1 ch, UAR1 = 1 ch, UAR1 = 1 ch</td>
<td>CSI = 2 ch, UAR1 = 2 ch</td>
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<tr>
<td>A/D converter</td>
<td>20-bit</td>
<td>16-bit</td>
<td>16-bit</td>
</tr>
<tr>
<td>On-chip debugging function, boundary scan function</td>
<td>ROM correction function, dedicated PWM output: 4 ch</td>
<td>Real-time counter (watch function)</td>
<td></td>
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<tr>
<td>ROM correction function, dedicated PWM output: 4 ch</td>
<td>ROM correction function, dedicated PWM output: 4 ch</td>
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<tr>
<td>LCD display</td>
<td>On-chip LCD C/D 8-bit microcontroller</td>
<td>8-bit microcontroller</td>
<td></td>
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<tr>
<td>Communication function</td>
<td>EEPROM</td>
<td>EEPROM</td>
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<tr>
<td>Memory</td>
<td>32-bit RAM</td>
<td>16-bit RAM</td>
<td>8-bit RAM</td>
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<tr>
<td>Power consumption (mask ROM version, Typ.)</td>
<td>124 mW</td>
<td>195 mW</td>
<td>80 mW</td>
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<tr>
<td>Package</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>256-pin PGA</td>
<td>100-pin LQFP (14 x 14 mm)</td>
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</table>

* : Only Y products have an on-chip I 2 C interface.
Product Lineup

ASSP Lineup (2)

Field-specific lineups

Dashboard control
- On-chip meter driver
  On-chip LCD driver

Body control
- On-chip CAN

Car audio control
- On-chip CAN
- On-chip IEBus
- Low noise

Dashboard
- Control
- Body control
- Car audio
  - Control
  - On-chip IEBus

Features

V850/DB1
- For automotive electronics (body control applications)
- ROM/RAM: 128 KB/6 KB
- On-chip DCAN controller (2 ch. max.)
- 18 MIPS @ 16 MHz, 4.0 to 5.5 V operation
- 128-pin QFP

V850/SC2
- 5 V low-power version 19 MHz, 144-pin, IEBus
- Large capacity

V850/SC3
- 5 V low-power version 16 MHz, 144-pin, FCAN

V850/SB2
- 5 V low-power version 16 MHz, 100-pin, IEBus

V850/ES/F2
- 48-pin
- Large capacity internal flash, on-chip aFCAN, on-chip LIN, POCl/LVI

V850/ES/FE2, FF2, FG2, FJ2
- For automotive electronics (body control applications)
- On-chip large-capacity single-power-supply flash memory
- ROM/RAM: 512 KB/20 KB, 384 KB/16 KB, 256 KB/12 KB, 128 KB/6 KB
- On-chip aFCAN controller (4 ch. max.), LIN function compatible UART, POCl/LVI
- 29 MIPS @ 20 MHz, 4.0 to 5.5 V operation
- 64-pin TOQFP (FF2)/80-pin TOQFP (F2)/100-pin LQFP (FG2)/144-pin LQFP (FJ2)

V850/ES/SJ2
- For car audio
- Low EMI noise
- On-chip aFCAN controller (2 ch. max.)
- On-chip IEBus controller (1 ch.), on-chip aFCAN controller (2 ch. max.)
- 29 MIPS @ 20 MHz, 2.85 to 3.6 V operation
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting the N-ch open-drain output
- On-chip debugging function
- 100-pin LQFP/100-pin QFP (SJ2)

V850/ES/SJx
- Peripheral function
- Memory capacity
- Optimization

V850/ES/SGx
- Larger capacity

V850/ES/SF1
- For car audio
- Low EMI noise
- On-chip FCAN controller (2 ch. max.)
- ROM/RAM: 256 KB/16 KB, 128 KB/12 KB
- 100-pin LQFP/100-pin QFP

V850/ES/SG2
- On-chip IEBus controller (1 ch.), on-chip aFCAN controller (2 ch. max.)
- 29 MIPS @ 20 MHz, 2.85 to 3.6 V operation
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting the N-ch open-drain output
- On-chip debugging function
- 100-pin LQFP/100-pin QFP (SG2), 144-pin LQFP (SJ2)

V850/ES/SFx2
- On-chip meter driver, On-chip DCAN, On-chip LCD driver,
- Large capacity

<product specifications>

<table>
<thead>
<tr>
<th>Item</th>
<th>FE2</th>
<th>FF2</th>
<th>FG2</th>
<th>FJ2</th>
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<tr>
<td>CPU core</td>
<td>V850/DB1</td>
<td>V850/SC2</td>
<td>V850/SC3</td>
<td>V850/SB2</td>
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<tr>
<td>Performance</td>
<td>23 MIPS @ 20 MHz</td>
<td>29 MIPS @ 20 MHz</td>
<td>29 MIPS @ 20 MHz</td>
<td>29 MIPS @ 20 MHz</td>
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<td>Address: Multiplexed bus</td>
<td>64-bit</td>
<td>64-bit</td>
<td>64-bit</td>
<td>64-bit</td>
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<tr>
<td>External bus</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Timercontroller</td>
<td>16-bit 5-ch</td>
<td>16-bit 7-ch</td>
<td>16-bit 7-ch</td>
<td>16-bit 7-ch</td>
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<tr>
<td>WDT</td>
<td>1-ch, watch timer</td>
<td>1-ch, watch timer</td>
<td>1-ch, watch timer</td>
<td>1-ch, watch timer</td>
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<tr>
<td>Serial interface</td>
<td>CSI = 3 ch, LIN-compatible UART = 3 ch</td>
<td>CSI = 3 ch, LIN-compatible UART = 3 ch</td>
<td>CSI = 3 ch, LIN-compatible UART = 3 ch</td>
<td>CSI = 3 ch, LIN-compatible UART = 3 ch</td>
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<tr>
<td>Real time counter</td>
<td>10-bit 1-ch</td>
<td>16-bit 1-ch</td>
<td>16-bit 1-ch</td>
<td>16-bit 1-ch</td>
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<tr>
<td>Power consumption</td>
<td>51</td>
<td>64</td>
<td>64</td>
<td>64</td>
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<td>Package</td>
<td>84-pin TOQFP (19 x 19 mm)</td>
<td>80-pin TOQFP (12 x 12 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>144-pin LQFP (10 x 20 mm)</td>
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<td>Function</td>
<td>aFCAN = 2-ch</td>
<td>aFCAN = 2-ch</td>
<td>aFCAN = 2-ch</td>
<td>aFCAN = 2-ch</td>
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</tbody>
</table>

<Peripheral function>

- POCl/LVI function: clock monitor function, ROM matching
- aFCAN: CAN interface
- IEBus: IEBus controller
- On-chip meter driver
- On-chip DCAN
- On-chip LCD driver

<Memory capacity>

- Larger capacity

<Optimization>

- Larger capacity

16 Pamphlet U15412EJ4V1PF
### Application examples

#### Dashboard

**V850/ES/Fx2**

- Low EMI noise
- Large-capacity memory and large memory selection
- ROM/RAM: 512KB/24KB, 384KB/24KB, 256KB/16KB, 128KB/8KB
- On-chip IEBus controller (1 ch)
- 100-pin QFP/100-pin LQFP

**V850/DB1**

- Low EMI noise
- Large-capacity memory (ROM/RAM: 512KB/24KB)
- Enhanced peripheral functions for SB1
- On-chip IEBus controller (V850/SC2 : 1 ch)
- On-chip FCAN controller (V850/SC3 : 2 ch max.)
- 144-pin LQFP

#### Car audio

**V850/SF1**

- Low EMI noise
- Large-capacity memory (ROM/RAM: 512KB/24KB)
- Enhanced peripheral functions for SB1
- On-chip IEBus controller (V850/SC2 : 1 ch)
- On-chip FCAN controller (V850/SC3 : 2 ch max.)
- 144-pin LQFP

---

**Table:**

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<th>Feature</th>
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<th>V850/SC2,SC3</th>
<th>V850/SF1</th>
<th>V850/DB1</th>
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<tr>
<td>CPU core</td>
<td>V850ES/Fx2</td>
<td>V850/SFx2</td>
<td>V850/SF1</td>
<td>V850/DB1</td>
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<tr>
<td>Performance</td>
<td>18 MIPS @ 16 MHz</td>
<td>18 MIPS @ 16 MHz</td>
<td>21 MIPS @ 16 MHz</td>
<td>18 MIPS @ 16 MHz</td>
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<tr>
<td>Mainframe operating frequency</td>
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<td>32.768 kHz</td>
<td>32.768 kHz</td>
<td>32.768 kHz</td>
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<td>Internal RAM memory</td>
<td>512 KB/384 KB/256 KB</td>
<td>384 KB/256 KB</td>
<td>256 KB/16 KB</td>
<td>128 KB/8 KB</td>
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<td>Power consumption</td>
<td>125 mW @ 5 V</td>
<td>120 mW @ 5 V</td>
<td>100 mW @ 5 V</td>
<td>120 mW @ 5 V</td>
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<tr>
<td>Power supply voltage</td>
<td>4.0 V to 5.5 V</td>
<td>3.5 V to 5.5 V</td>
<td>3.5 V to 5.5 V</td>
<td>4.0 V to 5.5 V</td>
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<tr>
<td>External bus</td>
<td>Address: Multiplexed, separate</td>
<td>Address: Multiplexed, separate</td>
<td>Address: Multiplexed, separate</td>
<td>Address: Multiplexed, separate</td>
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<tr>
<td>Serial interface</td>
<td>UART 1 ch, 8-ch UART 2 ch</td>
<td>UART 1 ch, 8-ch UART 2 ch</td>
<td>UART 1 ch, UART 1 ch, UART 1 ch</td>
<td>UART 1 ch, UART 1 ch</td>
</tr>
<tr>
<td>ADC converter</td>
<td>10-bit, 18 ch</td>
<td>10-bit, 18 ch</td>
<td>10-bit, 18 ch</td>
<td>10-bit, 18 ch</td>
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<tr>
<td>ROM controller</td>
<td>6-ch external RAM (on-chip peripheral)</td>
<td>6-ch external RAM (on-chip peripheral)</td>
<td>6-ch external RAM (on-chip peripheral)</td>
<td>6-ch external RAM (on-chip peripheral)</td>
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<td>Input interface</td>
<td>CAN = 2 ch, 8-ch CAN = 2 ch</td>
<td>CAN = 2 ch, 8-ch CAN = 2 ch</td>
<td>CAN = 2 ch, 8-ch CAN = 2 ch</td>
<td>CAN = 2 ch, 8-ch CAN = 2 ch</td>
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<td>Power consumption</td>
<td>125 mW (19 MHz @ 5 V)</td>
<td>120 mW (19 MHz @ 5 V)</td>
<td>110 mW (16 MHz @ 5 V)</td>
<td>120 mW (16 MHz @ 5 V)</td>
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<tr>
<td>Package</td>
<td>144-pin LQFP (14 x 14 mm)</td>
<td>144-pin LQFP (14 x 14 mm)</td>
<td>144-pin LQFP (14 x 14 mm)</td>
<td>128-pin DFP (20 x 20 mm)</td>
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### Product Lineup

#### Memory Lineup

<table>
<thead>
<tr>
<th>ROM Size (bytes)</th>
<th>RAM size (bytes)</th>
</tr>
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<tbody>
<tr>
<td>4K</td>
<td>4K</td>
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<tr>
<td>6K</td>
<td>6K</td>
</tr>
<tr>
<td>8K</td>
<td>8K</td>
</tr>
<tr>
<td>10K</td>
<td>10K</td>
</tr>
<tr>
<td>12K</td>
<td>12K</td>
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<td>20K</td>
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<td>40K</td>
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<tr>
<td>48K</td>
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</table>

<table>
<thead>
<tr>
<th>ROM Size (bytes)</th>
<th>RAM size (bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>64K</td>
<td>64K</td>
</tr>
<tr>
<td>96K</td>
<td>96K</td>
</tr>
<tr>
<td>128K</td>
<td>128K</td>
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<td>192K</td>
<td>192K</td>
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<td>256K</td>
<td>256K</td>
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<td>384K</td>
<td>384K</td>
</tr>
<tr>
<td>512K</td>
<td>512K</td>
</tr>
<tr>
<td>640K</td>
<td>640K</td>
</tr>
</tbody>
</table>

**Flash memory version**

**Mask ROM version**

**Mask ROM/flash memory version**

* : Under development
## Package Lineup

<table>
<thead>
<tr>
<th>No. of pins</th>
<th>Type</th>
<th>Size</th>
<th>Pitch</th>
<th>Thickness</th>
<th>Mounted products</th>
</tr>
</thead>
<tbody>
<tr>
<td>121 pins</td>
<td>FBGA (F1)</td>
<td>12×12 mm</td>
<td>0.8 mm</td>
<td>1.13 mm</td>
<td>SA1, SA3</td>
</tr>
<tr>
<td>161 pins</td>
<td>FBGA (F1)</td>
<td>13×13 mm</td>
<td>0.8 mm</td>
<td>1.13 mm</td>
<td>MA1, MA3</td>
</tr>
<tr>
<td>180 pins</td>
<td>FBGA (F1)</td>
<td>14×14 mm</td>
<td>0.8 mm</td>
<td>0.96 mm</td>
<td>SV1</td>
</tr>
<tr>
<td>157 pins</td>
<td>FBGA (F1)</td>
<td>14×14 mm</td>
<td>0.8 mm</td>
<td>0.96 mm</td>
<td>MS1</td>
</tr>
<tr>
<td>257 pins</td>
<td>FBGA (F1)</td>
<td>14×14 mm</td>
<td>0.8 mm</td>
<td>1.13 mm</td>
<td>SV2</td>
</tr>
<tr>
<td>240 pins</td>
<td>FBGA (F1)</td>
<td>16×16 mm</td>
<td>0.8 mm</td>
<td>1.13 mm</td>
<td>ME2</td>
</tr>
<tr>
<td>64 pins</td>
<td>LFQFP (GB)</td>
<td>10×10 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KE1, KE1+</td>
</tr>
<tr>
<td>64 pins</td>
<td>LFQFP (GC)</td>
<td>14×14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KG1, KG1+, SB1, SB2, SF1, SG2, PM1, FG2, MS2, MA2, IA2, IA4, VB53, μPD70F3229Y, 703229Y</td>
</tr>
<tr>
<td>64 pins</td>
<td>LFQFP (GC)</td>
<td>14×14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KG1, KG1+, SB1, SB2, SF1, SG2, IA2, IA4</td>
</tr>
<tr>
<td>64 pins</td>
<td>LFQFP (GC)</td>
<td>14×14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KG1, KG1+, SB1, SB2, SF1, SG2, IA2, IA4</td>
</tr>
<tr>
<td>64 pins</td>
<td>LFQFP (GC)</td>
<td>20×20 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KG1, KG1+, SB1, SB2, SF1, SG2, IA2, IA4</td>
</tr>
<tr>
<td>64 pins</td>
<td>LFQFP (GC)</td>
<td>24×24 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>SV1, ME2</td>
</tr>
<tr>
<td>100 pins</td>
<td>LFQFP (GB)</td>
<td>14×14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KE1, KE1+</td>
</tr>
<tr>
<td>100 pins</td>
<td>LFQFP (GB)</td>
<td>14×14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KG1, KG1+, SB1, SB2, SF1, SG2, PM1, FG2, MS2, MA2, IA2, IA4, VB53, μPD70F3229Y, 703229Y</td>
</tr>
<tr>
<td>100 pins</td>
<td>LFQFP (GB)</td>
<td>14×14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KG1, KG1+, SB1, SB2, SF1, SG2, IA2, IA4</td>
</tr>
<tr>
<td>100 pins</td>
<td>LFQFP (GB)</td>
<td>14×14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KG1, KG1+, SB1, SB2, SF1, SG2, IA2, IA4</td>
</tr>
<tr>
<td>100 pins</td>
<td>LFQFP (GB)</td>
<td>14×14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KG1, KG1+, SB1, SB2, SF1, SG2, IA2, IA4</td>
</tr>
<tr>
<td>128 pins</td>
<td>LFQFP (GF)</td>
<td>14×14 mm</td>
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<td>1.4 mm</td>
<td>KG1, KG1+, SB1, SB2, SF1, SG2, IA2, IA4</td>
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<tr>
<td>128 pins</td>
<td>LFQFP (GF)</td>
<td>14×14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KG1, KG1+, SB1, SB2, SF1, SG2, IA2, IA4</td>
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<tr>
<td>144 pins</td>
<td>LFQFP (GF)</td>
<td>14×14 mm</td>
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<td>1.4 mm</td>
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<tr>
<td>176 pins</td>
<td>LFQFP (GM)</td>
<td>24×24 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>SV1, ME2</td>
</tr>
<tr>
<td>568x12</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**CPU Roadmap**

**Performance range of 20 to over 300 MIPS with single instruction set**

- Utilization of existing software resources
- Maintenance of real-time performance
- Pursuit of low power consumption

**CPU Core Function Comparison**

<table>
<thead>
<tr>
<th>CPU Core Function</th>
<th>V850</th>
<th>V850ES</th>
<th>V850E1</th>
<th>V850E2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum operating frequency</td>
<td>20/33 MHz</td>
<td>20/32 MHz</td>
<td>66 MHz to 150 MHz</td>
<td>200 MHz to 266 MHz to 400 MHz</td>
</tr>
<tr>
<td>Instructions</td>
<td>47</td>
<td>80</td>
<td>80</td>
<td>89</td>
</tr>
<tr>
<td>Maximum program memory space</td>
<td>16 MB</td>
<td>16 MB</td>
<td>64 MB</td>
<td>512 MB (internal 128 MB)</td>
</tr>
<tr>
<td>Maximum data memory space</td>
<td>16 MB</td>
<td>16 MB</td>
<td>256 MB</td>
<td>4 GB</td>
</tr>
<tr>
<td>Higher performance</td>
<td>5-stage pipeline Harvard architecture</td>
<td>Improved pipeline • Non-blocking load/store instructions • Parallel instruction execution (instruction execution in internal ROM) • Addition of branching/load pipe • Shift to 3-operand manipulations in 1 slot</td>
<td>• 7-stage pipeline Simultaneous execution of 2 instructions with 3 pipelines that can operate independently from each other</td>
<td></td>
</tr>
<tr>
<td>High code efficiency</td>
<td>2-byte instructions CISC instructions</td>
<td>Addition of C language compatible instructions (Switch instruction, Call instruction, data conversion instruction, Prepare/Dispose instruction)</td>
<td>32-bit relative branch instruction 3-operand instruction • Sum of products instruction • Bit search instruction</td>
<td></td>
</tr>
<tr>
<td>Multiplier</td>
<td>16 × 16 bits → 32-bit multiplication</td>
<td>16 × 16 bits → 32-bit operation 32-bit → 64-bit operation (32-bit multiply instruction support)</td>
<td>16 × 16 bits → 32-bit operation 32-bit → 64-bit operation</td>
<td></td>
</tr>
<tr>
<td>Interrupt responsiveness</td>
<td>4 to 10 clocks</td>
<td>4 to 10 clocks</td>
<td>4 to 10 clocks</td>
<td>4 to 10 clocks</td>
</tr>
</tbody>
</table>
System LSI Support

◆ Use of same development methods for standard V850 Series products, ASIC microcontrollers
  ◆ Quick market introduction of standard products
  ◆ System optimization through shift to system LSIs

◆ CPU core development considering system LSIs
  ◆ Release of cores that support on-chip debugging
  ◆ 2-stage structure consisting of 32-bit sync system bus & 16-bit async peripheral function bus
  ◆ Large choice of peripheral function macros

◆ Many supported processes and large range of required performance, and power consumption

V850E1 system configuration example

V850E2 system configuration example
The V850 Series, which consists of single-chip RISC microcontrollers that use an architecture optimized for embedding, has the following features.

- 5-stage pipeline processing
- Harvard architecture
- 32 general-purpose registers
- Simple addressing
- 2-byte basic instruction set
- Support of CISC-like instructions
- Multi-status flags
- 32-bit barrel shifter
- DSP function

### 5-stage pipeline processing

The V850 Series uses a 5-stage pipeline structure (5 stages from instruction fetch to writeback) that supports simultaneous processing of 5 instructions, thus enabling the execution of almost all instructions in just one clock.

#### Harvard architecture

The V850 Series uses the Harvard architecture, which is designed so that the instruction bus and data bus can operate completely independently from each other, thereby preventing pipeline operation problems and ensuring efficient instruction execution.
32 general-purpose registers

The V850 Series provides 32 general-purpose registers. Along with a hardware environment that is ideal for program execution, the development environment, including compilers, exploits these 32 registers to achieve program generation with superior code efficiency and execution performance.

For example, looking at the program execution time and code size changes when the number of registers used by the compiler is changed using the servo control module, we can see that the larger the number of registers, the better the program execution speed and the smaller the code size. However, from about 26 registers, the improvement in terms of execution speed and code size becomes smaller, and in the neighborhood of 32 registers, there are no more changes. This is why the V850 Series has been provided with 32 registers as the strict minimum requirement.

Software register bank

The number of registers can be selected from among 22, 26, and 32 as a compiler option to efficiently execute application programs. Unused registers can be used as a software register bank for which save and restore processing is not required during interrupt servicing or task switching, which increases the processing speed.

General-purpose register configuration

The V850 Series provides 32 general-purpose registers. The number of registers can be selected from among 22, 26, and 32 as a compiler option to efficiently execute application programs. Unused registers can be used as a software register bank for which save and restore processing is not required during interrupt servicing or task switching, which increases the processing speed.

### General-purpose register configuration

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Application</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Zero register</td>
<td>Always holds &quot;0&quot;</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Assembler reservation</td>
<td>Used as working register for address generation</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Address/data variable register (If real-time OS being used does not use r2)</td>
<td>Used for stack frame generation during function call</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Stack pointer</td>
<td>Used for accessing global variables in the data area</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Global pointer</td>
<td>Used when accessing global variables in the data area</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Text pointer</td>
<td>Used as register for specifying the beginning of the text area (program code allocation)</td>
<td></td>
</tr>
<tr>
<td>6-29</td>
<td>Address/data variable register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Element pointer</td>
<td>Used as base pointer for address generation during memory access</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Link pointer</td>
<td>Used during function call by compiler</td>
<td></td>
</tr>
<tr>
<td>PC</td>
<td>Program counter</td>
<td>Holds instruction addresses during program execution</td>
<td></td>
</tr>
</tbody>
</table>

### System register configuration

<table>
<thead>
<tr>
<th>No.</th>
<th>System Register Name</th>
<th>Operation Specification</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>EIPC</td>
<td>LDSCR</td>
<td>Register for saving status during interrupt</td>
</tr>
<tr>
<td>1</td>
<td>EIPSW</td>
<td></td>
<td>Register for saving status during NMI</td>
</tr>
<tr>
<td>2</td>
<td>FEPC</td>
<td></td>
<td>Register for saving status during CALLT execution</td>
</tr>
<tr>
<td>3</td>
<td>FEPSW</td>
<td></td>
<td>Register for saving status during CALLT execution</td>
</tr>
<tr>
<td>4</td>
<td>ECR</td>
<td></td>
<td>Interrupt source register</td>
</tr>
<tr>
<td>5</td>
<td>PSW</td>
<td></td>
<td>Program status word</td>
</tr>
<tr>
<td>16</td>
<td>CTIPC</td>
<td></td>
<td>Register for saving status during CALLT execution</td>
</tr>
<tr>
<td>17</td>
<td>CTPSW</td>
<td></td>
<td>Register for saving status during CALLT execution</td>
</tr>
<tr>
<td>18</td>
<td>DBIPC</td>
<td></td>
<td>Register for saving status during exception/debug trap</td>
</tr>
<tr>
<td>19</td>
<td>DBPSW</td>
<td></td>
<td>Register for saving status during exception/debug trap</td>
</tr>
<tr>
<td>20</td>
<td>CTBP</td>
<td></td>
<td>CALLT base pointer</td>
</tr>
<tr>
<td>6-15, 21-31</td>
<td>Reserved</td>
<td>× ×</td>
<td></td>
</tr>
</tbody>
</table>

× : Access prohibited  
LDSCR: Instruction to load general-purpose register contents to system register  
STSR: Instruction to store system register contents to general-purpose register  
○ : Access enabled
### Simple addressing

The increased amount of address calculations in the CPU in the case of complex addressing causes disturbances in the pipeline operation. As a result, address calculation becomes a bottleneck for pipeline processing and raising the frequency to increase the performance becomes difficult. The V850 Series avoids this problem by supporting only simple addressing.

### Addressing mode

- **Instruction addresses**
  - Relative addressing (PC dependent)
    
    Add 9 signed bits or 22 signed bits of data of the instruction code to the program counter.

- **Operand addresses**
  - Register addressing
    
    Addressing that accesses the general-purpose register specified by the general-purpose specification field or a system register as an operand.

  - Immediate addressing
    
    Addressing of 5-bit data or 16-bit data for manipulation in the instruction code.

  - Based addressing
    
    Addressing that accesses memory, with the sum of the contents of the general-purpose register (reg1) and 16-bit displacement (disp16) as the operand address.

  - Bit addressing
    
    Addressing that accesses 1 bit of 1 byte of the memory space, with the sum of the contents of the general-purpose register (reg1) and 16-bit displacement (disp16) that has been sign extended to word length as the operand address.

### 2-byte basic instruction set

The V850 Series employs a 2-byte instruction code to perform basic processing to enable compact program development equivalent to 16-bit CISC microcontrollers.

- **Object Code Size Comparison**
  
  (Dhrystone 1.1/Large model)

<table>
<thead>
<tr>
<th>Object Code Size Comparison (Dhrystone 1.1/Large model)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-bit(CISC)</td>
</tr>
<tr>
<td>1.00</td>
</tr>
</tbody>
</table>

- **Improved object efficiency through ROMization programming**
  
  Application of 2-byte instructions to all basic processing, consisting of load, store, arithmetic/logic operations, and branching.

- **To realize ease of use, restrictions on 16-bit fixed-length instructions are partially removed through incorporation of 32-bit instructions.**

- **Bit manipulation instructions, etc.**
CISC-like instructions for embedding (bit manipulation instructions)
The V850 Series supports bit manipulation instructions suitable for flag manipulation on I/O registers, which play a large role in embedding control.

- Improvement of operability of memory mapped I/Os for control purposes
- Manipulation of any 1 bit of byte data in the memory space
- Provision of test (test1)/set (set1)/clear (cle1)/invert (in1)
- Effective for reducing object size and execution time since flags can be manipulated in 1-bit units with 1 instruction

Multi-status flags
In the V850 Series, calculation results are reflected in registers as status flags. As a result, delay branching such as can be seen in the RISC microcontrollers of other manufacturers does not occur and programs can be coded with the same feel as CISC microcontrollers.

- Easy recording with assembler
- Improved object efficiency and execution speed

DSP function
The V850 Series provides a DSP function for executing high-speed calculations and product-sum operations indispensable for digital signal processing such as image and speech processing.

- Direct data handling via general-purpose registers
- Realization of digital signal processing through general-purpose CPU
- High-speed 16-bit (V850, V850ES CPU), 32-bit (V850ES CPU) multiply/sum-of-products
  (Multiply: 1 to 2 clocks, sum-of-products: 3 clocks)
- Effective for filter operations and matrix operations for feedback calculations in speed, position, and other servo control.

32-bit barrel shifter
V850 Series can realize bit manipulations frequently used during signed data and image data processing in 1 instruction per clock.

- Shifting of any number of bits (0 to 31) executable in 1 instruction per clock
- Improved execution speed/object efficiency
- Effective for extracting arbitrary bit lengths of image data and signed data (extracting code during MH/MR/MMR encoding, etc.)
The V850E1 and V850ES cores achieve high performance and higher code efficiency through the implementation of the following improvements to the V850 CPU core. 

**Non-blocking load/store**
- Improved bus use efficiency
- Shorter interrupt insensitivity period

**Addition of branch/load pipes**
- 2-clock branching
- Parallel execution of instructions

**Pipeline configuration**

```
<table>
<thead>
<tr>
<th>Pipeline</th>
<th>Instruction Fetch</th>
<th>Decode Immediate Data</th>
<th>Instruction Address Calculation</th>
<th>Load/Store Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ID</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EX</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

**Addition of branch/load pipes**

**Parallel instruction execution (when executed by internal ROM)**

```
<table>
<thead>
<tr>
<th>Pipeline</th>
<th>Instruction Fetch</th>
<th>Decode Immediate Data</th>
<th>Instruction Address Calculation</th>
<th>Load/Store Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ID</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EX</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

**Shift to 3-operand manipulations in 1 slot**

```
<table>
<thead>
<tr>
<th>Instruction Fetch</th>
<th>Decode Immediate Data</th>
<th>Instruction Address Calculation</th>
<th>Load/Store Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ID</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WB</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

**Addition of high-level language-compatible instructions**

The V850E1 and V850ES cores have enhanced the instruction set of the V850 core as follows.

- **switch** (2 bytes)
- C language switch statement processing converted into instruction
- **callt** (2 bytes)/**ctret** (4 bytes)
- Table reference branching
- Reduction of call code that frequently appears
- **Data conversion instructions** (2 bytes)
- Short type cast executed with 1 instruction
- **sxh, sxb, zxb, and zxh instructions**
- **prepare/dispose** (4 bytes)
- Function start/end processing executed in 1 instruction
- **unsigned Load**
- Reduction of unsigned manipulation code

**Non-blocking load/store**

- Pipeline is stopped until MEM stage complete

**Addition instruction**

```
<table>
<thead>
<tr>
<th>Pipeline</th>
<th>Instruction Fetch</th>
<th>Decode Immediate Data</th>
<th>Instruction Address Calculation</th>
<th>Load/Store Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ID</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EX</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

**Addition instruction**

```
<table>
<thead>
<tr>
<th>Pipeline</th>
<th>Instruction Fetch</th>
<th>Decode Immediate Data</th>
<th>Instruction Address Calculation</th>
<th>Load/Store Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ID</td>
<td></td>
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</tr>
<tr>
<td>EX</td>
<td></td>
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</tr>
<tr>
<td>MEM</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>WB</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>
```
V850E2 Architecture

V850E2 core features

- Real-time performance of 250 MIPS
  - Operation at over 200 MHz
- Inheritance of V850E1 performance and features
  - Upward instruction compatibility with V850E1 and V850ES cores at object level
  - Use of 7-stage pipeline
  - Parallel pipeline configuration (2 parallel superscalar)
  - 128-bit instruction fetch bus
- Support of expanding application software sizes
  - Address space (program/data) expansion
  - Strengthened cache memory support

V850E2 core Main added functions

- 32-bit relative branch instruction
  - Support of program space expansion
  - Long-distance branching performance, elimination of code efficiency losses
- 3-operand instructions (addition of target operations)
  - Higher speed processing of operations such as multiplex add/subtract (64-bit operation, saturate operation) and bit shift, contributing to higher code efficiency
- Sum-of-products instruction
  - Higher speed 32-bit sum-of-products operation (32 × 32 + 64→64 bits)
- Bit search instruction
  - Bit row change point search for run length measurement, contributing to increased speed of conversion from integers to floating decimals, etc.

V850E2 core CPU pipeline configuration

Instruction memory, instruction cache

2 instructions simultaneously executable using 2 instruction execution units

Instruction memory, instruction cache

Data memory, data cache

V850E2 core CPU pipeline operation

Execution of up to 2 instructions/clock possible (dependent on instruction set)
## Memory Access Functions

### SDRAM controller

- **Products:** V850E/MA1, MA2, MA3, ME2
  - SDRAM connectable without external circuit
  - CAS latency: 2, 3 supported
  - CBR (automatic) refresh: Self refresh supported
- **Diagram:**
  - [SDRAM Controller Diagram](#)

### DMA controller (provided in V850E products)

- **Products:** V850E/MA1, MA2, MA3, MS1, MS2, IA1, IA2, IA3, IA4, ME2, SV2
  - Transfer targets: Memory-peripheral I/O, memory-memory
  - Transfer mode: Single, single step, block transfer
  - Transfer units: 8/16 bits
  - Transfer type: 1-cycle transfer, 2-cycle transfer
  - Number of transfers: 65536 Max.
- **Diagram:**
  - [DMA Controller Diagram](#)

### DMA controller (provided in V850ES products)

- **Products:** V850ES/SA2, SA3, SG2, SJ2, KG1+, KJ1+, FG2, FJ2, µPD703229Y, 70F3229Y
  - Transfer targets: Memory-peripheral I/O, memory-memory
  - Transfer mode: Single
  - Transfer units: 8/16 bits
  - Transfer type: 2-cycle transfer
  - Number of transfers: 65536 Max.
- **Diagram:**
  - [DMA Controller Diagram](#)

### DMA controller (provided in V850/Sxx products)

- **Products:** V850/SA1, SB1, SB2, SV1, SF1, SC1, SC2, SC3
  - Transfer targets: Internal RAM-on-chip peripheral I/O
  - Transfer mode: Single
  - Transfer units: 8/16 bits
  - Transfer clock: 4 clocks Min.
  - Number of transfers: 256 Max.
- **Diagram:**
  - [DMA Controller Diagram](#)

---

[Note: The address signal used differs depending on the SDRAM product.]
Analog Circuits

**A/D converter (multi-stage buffer type)**

Products: V850E/MA1, MA3, ME2, IA1, IA2, MS1, SV2, V850/SV1, V853, etc.
- Conversion startable by software or hardware
- 8 on-chip conversion result registers (24 for SV2)
- Select/scan mode switching possible

**D/A converter**

Products: V850E/SA2, SA3, SG2, SJ2, V850/MA3, V853
- R-2R ladder method (except for V850ES/SA2, SA3)
- R string method (V850ES/SA2, SA3 only)
- 8-bit resolution
- Operation mode: Normal mode/real-time output mode

**High-speed A/D converter**

Products: V850E/IA3, IA4
- Simultaneous 10-bit A/D converter sampling for 2 circuits
- On-chip operational amplifier \((2.5 \times 5)\) for input level amplification
- On-chip overvoltage detection comparator
**Timer/Counter**

- **Timer configuration during inverter control**
  - Products: V850E/IA3, IA4, MA3, V850ES/IK1
  - 0% and 100% output and 6-phase PWM output with deadtime possible
  - Switchable anytime/batch overwrite for compare register
  - A/D converter conversion start trigger generator

- **32-bit servo timer**
  - Products: V850E/SV2
  - 32-bit timer unit for servo control
  - Capture registers: 12
  - Compare registers: 2
  - External input detection circuit with 1 to 256 dividers
  - On-chip 8-bit mask timers: 2

- **Up/down counter**
  - Products: V850E/IA1, IA2, IA3, IA4, MA3, ME2
  - 16-bit 2-phase encoder input possible
  - Compare registers: 2
  - Capture/compare registers: 2

- **Real-time counter**
  - Products: V850ES/SA2, SA3, PM1
  - On-chip week, day, hour, minute, second counters
  - Counting up to 4095 periods
  - Support of interval interrupt generation at fixed intervals selectable from: 0.015625 s, 0.03125 s, 0.0625 s, 0.125 s, 0.25 s, 0.5 s, 1 s, 1 mn, 1 hr, 1 day
### Serial Interface

**Serial interface with automatic send/receive function**

Products: V850E/SV2, V850ES/KF1, KG1, KJ1, KF1+, KG1+, KJ1+  
- 32-byte internal buffer RAM  
- Automatic send/receive function  
  - 1 to 32 bytes of transfer bytes specifiable  
  - Transfer interval specifiable (0 to 63 clocks)  
  - Single transfer/repeated transfer specifiable

### LINBus

Products: V850ES/KE1+, KF1+, KG1+, KJ1+, SG2, SJ2, µPD703229Y, 70F3229Y, V850ES/FE2, FF2, FG2, FJ2  
- Low-cost 1-line network bus  
- Sync break field (SBF) send/receive possible through hardware  
  (Send: 13 bits ≤ SBF ≤ 20 bits; Receive: SBF ≥ 11 bits)  
- Also generally usable as UART

### CAN

Products: V850ES/SG2, SJ2, FE2, FF2, FG2, FJ2, V850E/IA1, V850/SF1, SC3, DB1  
- CAN protocol ver. 2.0 Part B (send/receive of standard and extended frames)  
- Max. transfer rate: 500 kbps (V850/DB1 only) 1 Mbps  
- 32 message buffer

### IEBus controller

Products: V850ES/SG2, SJ2, V850/SB2, SC2  
- Communication mode 1 supported  
- Max. transfer bytes: 32 bytes/frame  
- Max. transfer speed: Approx. 17 kbps
**USB**

Products: V850E/ME2
- Compliant with Universal Serial Bus Specification
- Support of 12 Mbps (full speed) transfer
- Many endpoint configurations

**SSCG function (Spread spectrum Frequency Synthesizer Clock Generator)**

Products: V850E/ME2
- EMI peak noise reduction through input frequency modulation
- Large reduction in noise countermeasure time and cost possible
- Frequency modulation rate and modulation period changeable by register setting

**ROM correction function**

Products: V850 core: V850/SB1, SB2, SV1, SF1, SC1, SC2, SC3, V850E, V850ES cores: V850ES/SA2, SA3, SG2, SJ2, KE1, KF1, KG1, KJ1, KE1+, KF1+, KG1+, PM1, IK1, µPD703229Y, 70F3229Y, V850E/MA3, SV2, IA3, IA4
- Instructions of address to be modified inserted to replace DBTRAP instruction (JMP r0 instruction in case of V850 core), branching to 0060H (0000H in case of V850 core)
- Program modification following switch to mask ROM possible
- Modified addresses: 4 points, 8 points

Note V850E/SV2

**Explanation of ROM correction operation**

- Instruction data bus
- Instruction address bus
- ROM correction address register
- Comparator
- Output trigger control circuit
- Instruction replacement part
- Instruction address bus
- Internal ROM
- ROM correction address enable setting information
- Correction address enable setting information
- Correction address = XXX, ROM correction enable flag = 1
- Correction point
- Instruction data bus
- Instruction address bus
- ROM correction address register
- Comparator
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- Instruction address bus
- Internal ROM
- ROM correction address enable setting information
- Correction address enable setting information
- Correction address = xxx, ROM correction enable flag = 1
- Correction point
- Instruction data bus
- Instruction address bus
- ROM correction address register
- Comparator
- Output trigger control circuit
- Instruction replacement part
- Instruction address bus
- External RAM, EEPROM, etc.
- Correction address enable setting information
- Correction address = XXX, ROM correction enable flag = 1
- Correction point
- Instruction data bus
- Instruction address bus
- ROM correction address register
- Comparator
- Output trigger control circuit
- Instruction replacement part
- Instruction address bus
- Internal ROM
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- Correction address enable setting information
- Correction address = XXX, ROM correction enable flag = 1
- Correction point
- Instruction data bus
- Instruction address bus
- ROM correction address register
- Comparator
- Output trigger control circuit
- Instruction replacement part
- Instruction address bus
- Internal RAM
- Internal RAM
- ROM correction request flag = 0?
- Yes
- No
- Read modification program to RAM
- Modification program execution
- Normal flow
- ROM correction flow
- Jump to modification program
- Internal RAM
- Modification program download
- Download modification program
- Correction point
- Initialization
- Jump to modification program
**Low-voltage detection circuit (LVI)**

Products: V850ES/KE1+, KF1+, KG1+, KJ1+, SG2, SJ2, µPD703229Y, 70F3229Y, V850ES/FE2, FF2, FG2, FJ2, IK1

- Detection voltage level changeable by software
- Usable instead of reset IC, contributing to lower system cost
- Detection voltage not changeable after mode transition (security protection)

**Clock monitor function**

Products: V850ES/KE1+, KF1+, KG1+, KJ1+, SG2, SJ2, µPD703229Y, 70F3229Y, V850ES/FE2, FF2, FG2, FJ2, IK1

- Monitors abnormal stops of main clock with internal Ring-Oscillator
- During abnormal stop, entire system can be set to reset status
- Prevention of destruction due to system deadlock or runaway

![Clock monitor function diagram](image)

**On-chip debugging function**

Products: V850E/ME2\textsuperscript{lin}, V850E/MA3, IA4, SV2, V850ES/KJ1, KJ1+, SG2, SJ2, FE2, FF2, FG2, FJ2, µPD70F3229Y

- Realization of on-chip debugging of microcontroller with DCU (Debug Control Unit)
- Compact and low-cost PC card-type emulator
- Flash programmer function
- Integrated debugger (ID850) supported

**Boundary scan function**

Products: V850E/SV2

- Use of JTAG (Joint Test Action Group) communication specifications, IEEE1149.1 compliant
- Progressive scan of device's external I/O pins, test data input/output possible
- Connection check of devices soldered on user board possible

![Boundary scan function diagram](image)

**Note**

- Trace function support is possible by using the RTE-2000-TP made by Midas Lab Co., Ltd., or PARTNER-ET II, PARTNER-J made by Kyoto Micro Computer Co., Ltd.
**V850 Series Benchmark**

The V850 Series realizes high speed, high performance, and high code efficiency.

**Minimum instruction execution time**

<table>
<thead>
<tr>
<th>Product</th>
<th>Cycle time (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V850ES/Kxx</td>
<td>0.05</td>
</tr>
<tr>
<td>78K4</td>
<td>0.125</td>
</tr>
<tr>
<td>78K0/Kx1</td>
<td>0.20</td>
</tr>
<tr>
<td>78K0</td>
<td>0.24</td>
</tr>
<tr>
<td>78K0/S5S</td>
<td>0.40</td>
</tr>
</tbody>
</table>

- 12 MHz (0.168 µs) supported for some products
- 10 MHz (0.2 µs) supported for some products

**V850 Series performance**

**Performance comparison**

- V850ES: 20 MHz
- A: 16x 20 MHz
- A: 16x 16 MHz
- B: 32x 50 MHz

**Code size comparison**

- V850ES: 20 MHz
- A: 16x 20 MHz
- A: 16x 16 MHz
- B: 32x 50 MHz

*NEC Electronics measurement results using sample program*

**Low Power Consumption**

Thanks to thorough energy-saving design, a superior current/performance ratio of 1.1 to 0.7 mA/MIPS is realized, particularly for V850ES and V850/Sxx products. As a result, a reduction in power consumption to 1/5 or less compared to 16-bit CISC microcontrollers of similar performance is realized. Lower system power consumption and higher performance are simultaneously realized through this extremely high power performance.

**Power performance**

- **8-bit CISC**: 9.2 mA/MIPS
- **16-bit CISC**: 7.3 mA/MIPS
- **V850/SV1**: 1.1 mA/MIPS
- **V850/SB1**: 0.9 mA/MIPS
- **V850/SA1**: 0.7 mA/MIPS

Realization of low consumption current that is 1/5 or less compared to 16-bit CISC of similar performance

**Clock gear function**

- Reduction in 8 MHz through clock gear (1/8)
- Reduction in 8 MHz through clock gear (1/32)
- Reduction to 1/400 through switch from main clock to subclock

**Standby mode**

- Normal operation mode
- HALT mode
- ICE mode
- Sub normal operation mode
- Sub IDLE mode
- STOP mode (sub operation)
- STOP mode (sub stop)

Consumption current

- Operating: •
- Stopped: •
Low Noise Countermeasures

Minimizing the influence of electromagnetic interference (EMI) emitted from the microcontroller and the influence of noise applied to the microcontroller (EMS) is a high priority, particularly for AV equipment such as car audio systems, and thus superior noise performance is required of microcontrollers. Various noise countermeasures are implemented in the V850 Series, and noise performance equivalent or superior to that of 16-bit products has been realized.

**EMS countermeasures**

- Use of PLL for oscillation circuit
- Voltage control oscillator
- Oscillation circuit
- LPF
- VCO
- Divider
- To CPU peripheral functions
- High-frequency noise cut through PLL filter

**EMS measurement results (power supply coupling measurement)**

- Noise application voltage
- 0 kV
- 1.0 kV
- 2.0 kV or higher

<table>
<thead>
<tr>
<th></th>
<th>V850ES/KJ1</th>
<th>Existing V850 products</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc=5 V</td>
<td>Vcc=5 V</td>
<td></td>
</tr>
<tr>
<td>Resonator</td>
<td>4 MHz</td>
<td>16 MHz</td>
</tr>
<tr>
<td>Internal operation frequency</td>
<td>16 MHz (PLL = ON)</td>
<td>Internal operation frequency: 16 MHz</td>
</tr>
</tbody>
</table>

**EMI noise countermeasures: Power supply circuit countermeasures**

- Port power supply separation
- Insertion of capacitance between VDD and GND
- Port power supply separation
- CPU power supply separation
- Reg. (OFF setting position)
- CPU
- OSC AMP

Due to the relation between the power supply and GND pad positions and the lead frame, placement is done so as to lower the power supply impedance.

**EMS noise measurement results**

- Power supply voltage: 5V
- Operating frequency: 78K0 V
- V850ES/KJ1 16MHz

Existing 78K0

V850ES/KJ1

Frequency [MHz]
Middleware plays a major role for maximizing processor performance and realizing high-speed processing of complex data with flexibility and ease.

NEC Electronics offers a large array of middleware that is optimized for the CPU architecture and importantly contributes to shortening development time, while also facilitating additions and changes to dedicated functions whose implementation as hardware for devices, etc., used to have high cost and time requirements, and the creation of user-friendly interfaces.

Middleware merits:

- Shortening of development time
- Reduction in development cost
- Realization of latest technology and functions
- Easy performance enhancement and function expansion
- Easy creation of user-friendly interface
- Multimedia processing realizable just with CPU
- Realization of higher reliability and quality
- Maximization of system added value

Shift to middleware accelerating deployment to optimum processors

An increasing number of processors optimized for various systems and based on NEC Electronics' original technology and the superb technology of third parties, as well as other technologies that have been established as standards, are being deployed from.

Middleware product list

<table>
<thead>
<tr>
<th>Category</th>
<th>Middleware</th>
<th>V850 Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>Image</td>
<td>JPEG</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>MPEG-4/H.263 Video</td>
<td>—</td>
</tr>
<tr>
<td>Speech</td>
<td>Text-To-Speech</td>
<td>Japanese</td>
</tr>
<tr>
<td></td>
<td>Speech CODEC</td>
<td>Japanese (large vocabulary)</td>
</tr>
<tr>
<td></td>
<td>G.729 Annex A/B</td>
<td>Japanese (small vocabulary)</td>
</tr>
<tr>
<td></td>
<td>AMR</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>MPEG-4 CELP</td>
<td>—</td>
</tr>
<tr>
<td>Sound</td>
<td>Audio decoder</td>
<td>AAC</td>
</tr>
<tr>
<td></td>
<td>MP3</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>WMA</td>
<td>—</td>
</tr>
</tbody>
</table>

Middleware performance list

<table>
<thead>
<tr>
<th>Middleware</th>
<th>Performance</th>
<th>Power (MIPS)</th>
<th>ROM</th>
<th>RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>JPEG</td>
<td>QVGA×24: Enc0.32s/Dec0.24s</td>
<td>—</td>
<td>17.5 KB</td>
<td>15 KB</td>
</tr>
<tr>
<td>G.726 (ADPCM)</td>
<td>32Kbps, 16Kbps</td>
<td>Eno8/Dec8.2</td>
<td>9 KB</td>
<td>60 B</td>
</tr>
<tr>
<td>Speech recognition (small vocabulary)</td>
<td>0.4s</td>
<td>19 (20 words)</td>
<td>82 KB</td>
<td>3.5 KB</td>
</tr>
<tr>
<td>Speech recognition (large vocabulary)</td>
<td>—</td>
<td>63 (100 words)</td>
<td>(15 words)</td>
<td>—</td>
</tr>
</tbody>
</table>

 Middleware V850 Series

- Development completed

Overview

- Customers
- Development support system
- Planning
- System design
- Development
- Mass production
- V850 Series
- IP vendors
- Standards
- Middleware
- Solution development
- Performance verification
- Consultation
- Customization
- Maintenance
- Next-generation processors
- Standards
- Platforms
- Middleware: Development completed

Middlewares

- Speech recognition: Japanese (large vocabulary)
- Speech recognition: Japanese (small vocabulary)
- Speech recognition: Chinese (small vocabulary)
- Speech recognition: English (small vocabulary)
- Handwriting recognition: Japanese (input frame required)
- Handwriting recognition: Japanese (input frame not required)
- Encryption: CIPHERUNICORN
- Fingerprint recognition
- Internet: TCP/IP
- Storage: PC-compatible file system

- Audio decoder: AAC
- Audio decoder: MP3
- Audio decoder: WMA
Speech Recognition

Speech recognition is realized on a single chip using the memory and peripheral I/Os in the V850 Series. Ideal for applications such as games and home appliances that must feature speech recognition but are subject to large restrictions.

- Realization of speech recognition with memory and peripheral I/Os contained in V850 Series
- Expansion of number of recognized words
  Recognized number of words: 30 words (in case of V850/SA1, 20 MHz)

JPEG

- Conforms to JPEG international standard
- Conforms to DCT baseline process (non-reverse coding)
- Versatile compression and decompression processing
  - Compression functions:
    - User-customizable VRAM input module
    - User-specified Huffman and quantization tables
    - APPn marker insertion
    - Compression suspend function
  - Decompression processing:
    - User-customizable VRAM output module
    - Support of various JPEG markers (DRI, RSTn, DNL)
    - Decompression suspend function

Text to Speech (for Japanese Text)

- Speech synthesized from Japanese Kana and Kanji text (SJIS code)
- Versatile speech synthesis
  - Synthesis of female voices possible
  - Various adjustable parameters such as intonation and reading speed
  - Rhythm of synthesized speech (pitch, phoneme duration) can be designed (Speech Designer compatible)
  - Speech synthesis using natural rhythm possible (synthesis of more natural sounding speech)
  - Support of special characters (Reading of special characters settable in user dictionaries)
  - Synthesis speed
    Works also with V850/SA1 (20 MHz). (However, text is placed in internal ROM.)

<table>
<thead>
<tr>
<th>Description</th>
<th>Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROM</td>
<td>126 KB</td>
</tr>
<tr>
<td>Data</td>
<td>35 KB</td>
</tr>
<tr>
<td>Dictionary data (approx. 60,000 words)</td>
<td>1.2 MB</td>
</tr>
<tr>
<td>Phoneme data</td>
<td>567 KB (8 kHz sampling)</td>
</tr>
<tr>
<td>Work</td>
<td>160 KB</td>
</tr>
<tr>
<td>Stack</td>
<td>506 bytes</td>
</tr>
<tr>
<td>Speech output buffer</td>
<td>12 KB</td>
</tr>
</tbody>
</table>
Flash

To answer the need for shorter development time and maintenance after shipping, NEC Electronics offers microcontrollers with on-chip flash memory available in a large range of capacities from 64 KB to 640 KB as part of the V850 Series. NEC Electronics’ flash memory microcontrollers offer the following features.

- **Flash capacity**
  64 to 640 KB

- **Overwrite unit**
  Entire memory at one time, or block units

- **Rewrite method**
  Serial communication with dedicated flash memory programmer (on-board, off-board)

- **Self-flash programming**

- **Rewrite voltage**
  Single-power-supply flash: Operation voltage
  Dual-power-supply flash: Operation voltage 7.8 V/10.3 V

- **Rewrite count**
  100 times

---

### Features

<table>
<thead>
<tr>
<th>Flash Memory Size (bytes)</th>
<th>64K</th>
<th>128K</th>
<th>192K</th>
<th>256K</th>
<th>384K</th>
<th>512K</th>
<th>64K</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAM size (bytes)</td>
<td>4K</td>
<td>4K</td>
<td>8K</td>
<td>16K</td>
<td>16K</td>
<td>24K</td>
<td>20K</td>
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<tr>
<td>V850ES/KE1</td>
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<td></td>
<td></td>
<td></td>
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<td></td>
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<td>V850ES/KF1</td>
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<td></td>
<td></td>
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<tr>
<td>V850ES/KG1</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>V850ES/KJ1</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>V850ES/KE1+*</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>V850ES/KF1+*</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>V850ES/KG1+*</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>V850ES/KJ1+*</td>
<td></td>
<td></td>
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<td></td>
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<td>V850/E/SO2</td>
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<td>V850/E/SJ2</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>µPD70F3229Y</td>
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<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>V850/E/SX02.SX3</td>
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<td></td>
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<td>V850/SX1</td>
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<td>V850/SDD,SC2,SC3</td>
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<td>V850/ES/MA3</td>
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<tr>
<td>V850/ES/MA1</td>
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<tr>
<td>V853</td>
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</tr>
<tr>
<td>V850/ES/A0, IA4</td>
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<td></td>
</tr>
<tr>
<td>V850/ES/A0</td>
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<tr>
<td>V850/ES/A1</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V850/ES/JK1*</td>
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<td></td>
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<tr>
<td>V850/ES/FE2*</td>
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<tr>
<td>V850/ES/FF2*</td>
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<td></td>
</tr>
<tr>
<td>V850/ES/G12*</td>
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<td></td>
</tr>
<tr>
<td>V850/ES/FG2*</td>
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<td></td>
</tr>
<tr>
<td>V850/ES/FJ2*</td>
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<td></td>
</tr>
<tr>
<td>V850/ES/SV2</td>
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<td></td>
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</tr>
<tr>
<td>V850/DB1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- : Single power supply
- : Dual power supply
- : Single power supply/dual power supply

<sup>1</sup>: Under development

---

### Rewrite Modes

To enable integrated use ranging from development to mass production and maintenance, the V850 Series supports a programmer rewrite mode that uses serial communication supporting on-board programming, as well as a self-programming mode that rewrites flash memory with user programs.

- **On-board programming mode**
  This programming mode is used to rewrite the flash memory mounted on the target system using a dedicated flash memory programmer.

- **Off-board programming mode**
  This programming mode is used to rewrite flash memory using a dedicated flash memory programmer and dedicated program adapter (FA Series<sup>Note 1</sup>).

- **Self-programming mode**
  This programming mode is used to rewrite flash memory by executing the user program written beforehand to the flash memory using on-board/off-board programming.<sup>Note 2</sup>

---

### Programmer program (on-board/off-board)

To answer the need for shorter development time and maintenance after shipping, NEC Electronics offers microcontrollers with on-chip flash memory available in a large range of capacities from 64 KB to 640 KB as part of the V850 Series. NEC Electronics’ flash memory microcontrollers offer the following features.

## Flash memory microcontroller lineup

**Note 1.** In the case of dual-power-supply flash, don’t connect.

---

**Note 2.** In the case of dual-power-supply flash, don’t connect.
Self-programming flow

Flash memory can be erased and rewritten using a self-programming library from a program placed in an area outside the flash memory.

Flash Specifications List

<table>
<thead>
<tr>
<th>Category</th>
<th>Part No.</th>
<th>Flash Memory Capacity</th>
<th>Max. Operating Frequency</th>
<th>Rewrite Voltage</th>
<th>Rewrite Mode</th>
<th>Rewrite Count (Times)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low end</td>
<td>V850ES/E1</td>
<td>128 KB</td>
<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
<td>On-Board</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/F1</td>
<td>256 KB/128 KB</td>
<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
<td>Off-Board</td>
<td>100</td>
</tr>
<tr>
<td>Middle range</td>
<td>V850ES/G1</td>
<td>256 KB/128 KB</td>
<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/K1</td>
<td>256 KB/128 KB</td>
<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/G1+</td>
<td>256 KB/128 KB</td>
<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td>High end</td>
<td>V850ES/M3</td>
<td>512 KB</td>
<td>80 MHz</td>
<td>2.3 V to 2.7 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/A3</td>
<td>256 KB</td>
<td>50 MHz</td>
<td>3.0 V to 3.6 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/S1</td>
<td>512 KB/384 KB/256 KB</td>
<td>20 MHz</td>
<td>4.0 V to 5.5 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/S1+</td>
<td>512 KB/384 KB/256 KB</td>
<td>20 MHz</td>
<td>4.0 V to 5.5 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/SC1</td>
<td>512 KB</td>
<td>20 MHz</td>
<td>3.5 V to 5.5 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/S2</td>
<td>640 KB/384 KB</td>
<td>20 MHz</td>
<td>2.85 V to 3.6 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/SC2</td>
<td>640 KB/384 KB</td>
<td>20 MHz</td>
<td>2.85 V to 3.6 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>µPD7F03229Y</td>
<td>384 KB</td>
<td>20 MHz</td>
<td>3.5 V to 5.5 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/SA2</td>
<td>256 KB</td>
<td>20 MHz</td>
<td>2.2 V to 2.7 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/SA3</td>
<td>256 KB</td>
<td>20 MHz</td>
<td>2.2 V to 2.7 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/SA1</td>
<td>256 KB/128 KB</td>
<td>20 MHz</td>
<td>3.0 V to 3.6 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/SB1</td>
<td>512 KB/384 KB/256 KB</td>
<td>20 MHz</td>
<td>4.0 V to 5.5 V</td>
<td>Programming</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/SB1+</td>
<td>512 KB/384 KB/256 KB</td>
<td>20 MHz</td>
<td>4.0 V to 5.5 V</td>
<td>Programming</td>
<td>100</td>
</tr>
</tbody>
</table>

*: Under development
NEC Electronics flash memory programmer: PG-FP4

[Features]
- Supports write to all NEC Electronics microcontrollers with internal flash memory.
- USB support through host machine interface
- Allows verification of various types of information, including programmer setting information, error messages, and check-sum, even in stand-alone configuration, from the main unit’s LCD.
- Enables downloading of two types of user code and selecting of valid code
- Device-specific information required for writing automatically settable with parameter files
- Supports both on-board programming and program adapter programming.
- Easy-to-carry A5 size
- Simple operation either on stand-alone basis and on Windows™ 95/Windows 98/Windows Me/Windows 2000/Windows XP, Windows NT™ 4.0 using a dedicated application (Flashpro4)

Flash memory programmer configuration
PG-FP4 allows single-microcontroller programming when used with a program adapter (FA Series of Naito Densei Machida Mfg. Co., Ltd.). On-board programming can also be performed.

A sample rewrite environment when using the program adapter is shown below.

Rewrite environment example

Cautions 1. Install the PG-FP4 control software and target device parameter file in the host machine.
- PG-FP4 control software: Bundled with PG-FP4
- PG-FP4 parameter file: Distributed via online delivery service

2. In addition to programming using the program adapter, on-board programming on the target system is also possible.

Third-party flash memory programmers (1/2)

Programming system Y1000-8

[Manufacturer/Distributor] Wave Technology Co., Ltd.
[Target Devices] V850/SV1, SB1 (μPD70F3032B, 70F3033B), SB2 (70F3035B, 70F3037H), V850E/IA1 (70F3116), MA1

[Features]
- Gang programmer enabling simultaneous programming and verification of up to 8 devices
- Enables reading of master data directly from floppy disk to internal memory
- Data dump display and editing functions
- Master data storable on internal hard disk
- Designed for simple and comfortable operation via touch panel, and superior operability via PASS/FAIL display, check-sum display, and task count display supporting sockets.

[Additional information]
TEL: +81-3-5304-1885 FAX: +81-3-5304-1886
E-mail: sales@y1000.com
Website: http://www.y1000.com/index_e.html
Third-party flash memory programmers (2/2)

FlashPRO IV: FL-PR4

[Target Devices] V850 Series
[Features]
- Supports writing to all NEC Electronics microcontrollers with internal flash memory.
- USB support through host machine interface
- Allows verification of various types of information, including programmer setting information, error messages, and check-sum, even in stand-alone configuration, from the main unit's LCD.
- Enables downloading of two types of user code and selecting of valid code
- Device-specific information required for writing automatically settable with parameter files
- Supports both on-board programming and program adapter programming.
- Easy-to-carry A5 size
- Simple operation either on stand-alone basis and on Windows 95/Windows 98/Windows Me/Windows 2000/Windows XP, Windows NT 4.0 using a dedicated application (Flashpro4)
[Additional information]
TEL: +81-45-475-4191 FAX: +81-45-475-4091
E-mail: info@ndk-m.co.jp
Website: http://www.ndk-m.co.jp/asmis/eng/index.html

NET IMPRESS

[Manufacturer/Distributor] Yokogawa Digital Computer Corporation
[Target Devices] V850/SB1 (μPD70F3033B), SB2(70F3037H), SA1(70F3017A), SC3(70F3089Y), V853(70F3003A, 70F3025A), V856E/MS1(70F3102A), MA1(70F3107), IA1, IA2(70F3114), V850ES/KF1(70F3210), FE2, FF2, FG2, FJ2, SG2, SJ2
[Features]
- Enables programming of flash memory microcontrollers of various writing specifications solder mounted on user system boards.
- One control module is the key to this product’s versatility.
- Microcontrollers of the same family are supported by changing parameters, and microcontrollers of different families are supported by purchasing the required license for the descriptor part.
- Can be used on standalone basis as well as via a host machine.
- Rich lineup of downloadable freeware
[Additional Information]
TEL: Japan +81-42-333-6224
U.S.A +408-941-8132 (Yokogawa Corporation of America)
Europe +44-1256-811998 (Ashling Microsystems Limited)
Korea +82-2-785-3929 (KM DATA INC.)
South East Asia +65-6563-2082 (Unidux Electronics Pte Ltd.)
FAX: Japan +81-42-352-6109
U.S.A +408-941-8121 (Yokogawa Corporation of America)
Europe +44-1256-811761 (Ashling Microsystems Limited)
Korea +82-2-785-3117 (KM DATA INC.)
South East Asia +65-6569-4661 (Unidux Electronics Pte Ltd.)
Website: http://www.ydc.co.jp/miccom/index_E.htm

Flash Burner Forward FL-S01, Flash Gang Forward FL-G01

[Manufacturer] Forward Electric Co., Ltd. (Hong Kong)
[Distributor] Application Co., Ltd.
[Target Devices] V850/SB1(70F3033A), V860E/MA1
[Features]
- Host machine interface supports USB.
- Easy operation and rich array of GUI software provided
- Low cost from development to mass production
- Compact and easy to carry (FL-S01)
- Gang programmer enabling simultaneous programming of up to 8 devices (FL-G01)
- Can be used on standalone basis using compact flash (FL-G01)
- Programming adapter board (option) usable in common for FL-S01 and FL-G01.
[Additional Details]
Website: http://www.apply.co.jp/index_eng.html
### Product Specifications List

#### Low-End Lineup (1/2)

<table>
<thead>
<tr>
<th>Item</th>
<th>V850ES/K1</th>
<th>V850ES/K1F</th>
<th>V850ES/K1F1</th>
<th>V850ES/K2</th>
<th>V850ES/K2F</th>
<th>V850ES/K2F1</th>
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<tbody>
<tr>
<td>Part No.</td>
<td>µPD703207/3207Y</td>
<td>µPD703207/3207HF</td>
<td>µPD703207/3207HY</td>
<td>µPD703209/3209Y</td>
<td>µPD703209/3209HY</td>
<td>µPD703210/3210Y</td>
</tr>
<tr>
<td>CPU core</td>
<td>V850ES</td>
<td>V850ES</td>
<td>V850ES</td>
<td>V850ES</td>
<td>V850ES</td>
<td>V850ES</td>
</tr>
<tr>
<td>CPU performance</td>
<td>25 MIPS (80 MHz: 5 kHz x 4)</td>
<td>29 MIPS (80 MHz: 5 kHz x 4)</td>
<td>100 MIPS (160 MHz: 5 kHz x 4)</td>
<td>25 MIPS (80 MHz: 5 kHz x 4)</td>
<td>29 MIPS (80 MHz: 5 kHz x 4)</td>
<td>100 MIPS (160 MHz: 5 kHz x 4)</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>128 KB (mask)</td>
<td>128 KB (flash)</td>
<td>64 KB (mask)</td>
<td>64 KB (mask)</td>
<td>128 KB (mask)</td>
<td>128 KB (mask)</td>
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<tr>
<td></td>
<td>96 KB (mask)</td>
<td>256 KB (mask)</td>
<td>96 KB (mask)</td>
<td>128 KB (mask)</td>
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<td>256 KB (mask)</td>
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<tr>
<td>Internal RAM</td>
<td>4 KB</td>
<td>4 KB</td>
<td>8 KB</td>
<td>8 KB</td>
<td>12 KB</td>
<td>12 KB</td>
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<td>Address bus</td>
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<td>24 bits</td>
<td>24 bits</td>
<td>24 bits</td>
</tr>
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<td>Data bus</td>
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<td>8/16 bits</td>
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<td>Chip select signal</td>
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<td>2</td>
<td>2</td>
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<tr>
<td></td>
<td>Memory controller</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>25 (Y products: 26)</td>
<td>25 (Y products: 26)</td>
<td>28 (Y products: 28)</td>
<td>28 (Y products: 28)</td>
<td>28 (Y products: 28)</td>
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<td>Notes:</td>
<td>1. Number of external interrupts that can be used to release STOP mode</td>
<td>2. Only Y products have an on-chip I2C interface</td>
<td>3. µPD703207/3207Y, 70F3207HY only</td>
<td>4. Only Y products have an on-chip I2C interface</td>
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### Notes

1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I2C interface
3. µPD703207/3207Y, 70F3207HY only
4. Only Y products have an on-chip I2C interface

---

### Pamphlet U15412EJ4V1PF

42
### Low-End Lineup (2/2)

#### Item 1

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<tr>
<th>Part No.</th>
<th>V850ES/KE1+</th>
<th>V850ES/KF1+</th>
<th>V850ES/KKF1+</th>
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<td>µPD703302/3302Y</td>
<td>µPD70F3302/3302Y</td>
<td>µPD703306/3306Y</td>
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<td>29 MIPS (802 MHz: 5 MHz x 4)</td>
<td>29 MIPS (802 MHz: 5 MHz x 4)</td>
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<td>128 KB (flash)</td>
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#### Item 2

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<td>29 MIPS (802 MHz: 5 MHz x 4)</td>
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### Notes
1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I2C interface.
3. These UARTs are the identical and the number of channels in KJ1+ totals 3 channels.
## Middle-Range Lineup (1/3)

### Item V850ES/SG2

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<th>Without EB ISA, aFCAN</th>
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<th>µPD703261/3261Y</th>
<th>µPD703261F/3261Y</th>
<th>µPD703262/3262Y</th>
<th>µPD703262F/3262Y</th>
<th>µPD703263/3263Y</th>
<th>µPD703263F/3263Y</th>
<th>µPD703264/3264Y</th>
<th>µPD703265/3265Y</th>
<th>µPD703266/3266Y</th>
<th>µPD703267/3267Y</th>
<th>µPD703268/3268Y</th>
<th>µPD703269/3269Y</th>
<th>µPD70F63263F/3263Y</th>
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<tr>
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<td>aFCAN controller: 1 ch</td>
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**Notes:**
1. Only products with IEBUS or aFCAN
2. Only products with two aFCAN channels
3. Only products with two IEBUS channels
4. Only products without IEBUS or aFCAN
5. Only products have an on-chip I ² C interface.

### Item V850ES/SG2

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<th>µPD703286/3286Y</th>
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<tr>
<td>Other peripheral functions</td>
<td>Watch timer: 1 ch</td>
<td>IEBUS controller: 1 ch</td>
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<td>ROM correction function: 4 points</td>
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<td>LV Clock monitor</td>
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<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. Only products with IEBUS or aFCAN
2. Only products with two aFCAN channels
3. Only products with two IEBUS channels
4. Only products without IEBUS or aFCAN
5. Only products have an on-chip I ² C interface.

---

**Pamphlet U15412EJAV1PF**
### Middle-Range Lineup (2/3)

#### V850/SC1, V850/SC2, V850/SC3

<table>
<thead>
<tr>
<th>Part No.</th>
<th>µPD703229Y</th>
<th>µPD7070329Y</th>
<th>µPD700068Y</th>
<th>µPD70703068Y</th>
<th>µPD703088Y</th>
<th>µPD703089Y</th>
<th>µPD70F3088Y</th>
<th>µPD70F3089Y</th>
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</thead>
<tbody>
<tr>
<td>CPU core</td>
<td>V850ES</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
</tr>
<tr>
<td>CPU performance</td>
<td>29 MIPS (@ 20 MHz)</td>
<td>23 MIPS (@ 19 MHz)</td>
<td>18 MIPS (@ 16 MHz)</td>
<td>23 MIPS (@ 20 MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal ROM</td>
<td>384 KB (mask)</td>
<td>384 KB (flash)</td>
<td>512 KB (mask)</td>
<td>512 KB (flash)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>External bus interface</td>
<td>Bus type: Multiplexed</td>
<td>Multiplexed</td>
<td>Multiplexed (can be separated only for V850/SC1, V850/SC2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address bus</td>
<td>18 bits</td>
<td>22 bits</td>
<td>16 bits</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data bus</td>
<td>8/16 bits</td>
<td>22 bits</td>
<td>16 bits</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory controller</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>38 sources</td>
<td>42</td>
<td>44</td>
<td>46</td>
<td>49</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ports</td>
<td>I/O</td>
<td>Input</td>
<td>6 ch (dedicated internal RAM+ on-chip peripheral I/O)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Debug control unit</td>
<td>–</td>
<td>–</td>
<td>12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>3.5 to 5.5 V</td>
<td>4.0 to 5.5 V (A/D converter: 4.5 to 5.5 V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>125 mW (5 V, @ 20 MHz)</td>
<td>165 mW (5 V, @ 20 MHz)</td>
<td>125 mW (5 V, @ 20 MHz)</td>
<td>185 mW (5 V, @ 20 MHz)</td>
<td>125 mW (5 V, @ 20 MHz)</td>
<td>210 mW (5 V, @ 20 MHz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin QFP (14 x 20 mm)</td>
<td>100-pin QFP (14 x 20 mm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Other peripheral functions

- **Interrupt sources:**
  - Internal
- **External:**
  - 2 ch
- **D/A converter:**
  - 4 ch
- **A/D converter:**
  - 2 ch
- **DMA controller:**
  - 6 ch (dedicated internal RAM+ on-chip peripheral I/O)
- **Ports:**
  - I/O
- **Input:**
  - 12
- **Power supply voltage:**
  - 3.5 to 5.5 V
- **Power consumption (Typ.):**
  - 125 mW (5 V, @ 20 MHz)

#### Notes
1. Number of external interrupts that can be used to release STOP mode
2. Only products with an on-chip PC interface.

---

### Middle-Range Lineup (2/3)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU core</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
</tr>
<tr>
<td>CPU performance</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>21 MIPS (@ 19 MHz)</td>
<td>18 MIPS (@ 16 MHz)</td>
<td>23 MIPS (@ 20 MHz)</td>
<td></td>
</tr>
<tr>
<td>Internal ROM</td>
<td>256 KB (mask)</td>
<td>256 KB (flash)</td>
<td>512 KB (mask)</td>
<td>512 KB (flash)</td>
<td></td>
</tr>
<tr>
<td>External bus interface</td>
<td>Bus type: Multiplexed</td>
<td>Multiplexed (can be separated only for V850/SC1, V850/SC2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address bus</td>
<td>18 bits</td>
<td>22 bits</td>
<td>16 bits</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Data bus</td>
<td>8/16 bits</td>
<td>22 bits</td>
<td>16 bits</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Memory controller</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>8 (6) Note 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>38 sources</td>
<td>42</td>
<td>44</td>
<td>46</td>
</tr>
<tr>
<td>Ports</td>
<td>I/O</td>
<td>Input</td>
<td>6 ch (dedicated internal RAM+ on-chip peripheral I/O)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Debug control unit</td>
<td>–</td>
<td>–</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Other peripheral functions</td>
<td>ROM correction function: 4 points, watch timer: 1 ch</td>
<td>ROM correction function: 4 points, watch timer: 1 ch, IEBus controller: 1 ch (V850/SC2 only), FCAN controller: 2 ch (1 ch: µPD703089Y only) (V850/SC3 only)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>3.5 to 5.5 V</td>
<td>3.5 to 5.5 V (A/D converter: 4.5 to 5.5 V)</td>
<td>4.0 to 5.5 V (A/D converter: 4.5 to 5.5 V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>100 mW (5 V, @ 25 MHz)</td>
<td>145 mW (5 V, @ 25 MHz)</td>
<td>125 mW (5 V, @ 20 MHz)</td>
<td>120 mW (5 V, @ 19 MHz)</td>
<td>110 mW (5 V, @ 16 MHz)</td>
</tr>
<tr>
<td>Package</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>144-pin LQFP (20 x 20 mm)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Notes
1. Number of external interrupts that can be used to release STOP mode.
2. Only products with an on-chip PC interface.

---

### Additional Information

- **Part No.**
- **Operating ambient temperature:**
  - -40°C to +85°C
- **Power supply voltage:**
  - 3.5 to 5.5 V
- **Power consumption (Typ.):**
  - 100 mW (5 V, @ 25 MHz)
- **Package:**
  - 100-pin LQFP (14 x 14 mm)
- **Power supply voltage:**
  - 3.5 to 5.5 V
- **Power consumption (Typ.):**
  - 100 mW (5 V, @ 25 MHz)

---

*Pamphlet U15412EJ41VPF*
### Middle-Range Lineup (3/3)

#### Item

<table>
<thead>
<tr>
<th>Part No.</th>
<th>CPU core</th>
<th>CPU performance</th>
<th>Internal ROM</th>
<th>Internal RAM</th>
<th>External bus interface</th>
<th>Memory controller</th>
<th>Interrupt sources</th>
<th>Timer/clock</th>
<th>Interface</th>
<th>Package</th>
<th>Operating ambient temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V850ES/SA2</strong></td>
<td>µPD703200/3200Y</td>
<td>29 MIPS (@ 20 MHz)</td>
<td>128 KB (mask)</td>
<td>8 KB</td>
<td>Multiplexed/separate</td>
<td>SRAAM, etc.</td>
<td>Internal</td>
<td>16-bit timer/event counter = 2 ch</td>
<td>Separate/multiplexed</td>
<td>160-pin TQFP (14 x 14 mm)</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td><strong>V850ES/SA3</strong></td>
<td>µPD703201/3201Y</td>
<td>29 MIPS (@ 20 MHz)</td>
<td>256 KB (mask)</td>
<td>256 KB (flash)</td>
<td>Separate/multiplexed</td>
<td>SRAAM, etc.</td>
<td>Internal</td>
<td>8-bit timer/event counter = 4 ch</td>
<td>Separate/multiplexed</td>
<td>121-pin FBGA (12 x 12 mm)</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td><strong>V850ES/S12</strong></td>
<td>µPD703204/3204Y</td>
<td>29 MIPS (@ 20 MHz)</td>
<td>256 KB (mask)</td>
<td>256 KB (flash)</td>
<td>Separate/multiplexed</td>
<td>SRAAM, etc.</td>
<td>Internal</td>
<td>16-bit timer/event counter = 2 ch</td>
<td>Separate/multiplexed</td>
<td>120-pin TQFP (14 x 14 mm)</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td><strong>µPD703220</strong></td>
<td>29 MIPS (@ 20 MHz)</td>
<td>16 KB</td>
<td>16 KB</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Internal</td>
<td>16-bit timer/event counter = 2 ch</td>
<td>-</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

**Notes:**
1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip PCI interface.

---

### Item

<table>
<thead>
<tr>
<th>Part No.</th>
<th>CPU core</th>
<th>CPU performance</th>
<th>Internal ROM</th>
<th>Internal RAM</th>
<th>External bus interface</th>
<th>Memory controller</th>
<th>Interrupt sources</th>
<th>Timer/clock</th>
<th>Interface</th>
<th>Package</th>
<th>Operating ambient temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V850/SA1</strong></td>
<td>µPD703014A/3014AY</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>64 KB (mask)</td>
<td>4 KB</td>
<td>Multiplexed/separate</td>
<td>SRAAM, etc.</td>
<td>Internal</td>
<td>16-bit timer/event counter = 2 ch</td>
<td>Separate/multiplexed</td>
<td>121-pin FBGA (12 x 12 mm)</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td><strong>µPD703015A/3015AY</strong></td>
<td>µPD703016B/3016BY</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>128 KB (mask)</td>
<td>128 KB (flash)</td>
<td>Separate/multiplexed</td>
<td>SRAAM, etc.</td>
<td>Internal</td>
<td>8-bit timer/event counter = 4 ch</td>
<td>Separate/multiplexed</td>
<td>120-pin TQFP (14 x 14 mm)</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td><strong>µPD703017A/3017AY</strong></td>
<td>µPD703018B/3018BY</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>256 KB (mask)</td>
<td>256 KB (flash)</td>
<td>Separate/multiplexed</td>
<td>SRAAM, etc.</td>
<td>Internal</td>
<td>16-bit timer/event counter = 2 ch</td>
<td>Separate/multiplexed</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td><strong>µPD703017A/3017AY</strong></td>
<td>µPD703018B/3018BY</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>256 KB (mask)</td>
<td>256 KB (flash)</td>
<td>Separate/multiplexed</td>
<td>SRAAM, etc.</td>
<td>Internal</td>
<td>16-bit timer/event counter = 2 ch</td>
<td>Separate/multiplexed</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

**Notes:**
1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip PCI interface.
## ASSP Lineup (1/3)

<table>
<thead>
<tr>
<th>Item</th>
<th>V800ES/IA1</th>
<th>V800ES/IA3</th>
<th>V800ES/PA1</th>
<th>V800ES/AC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part No.</td>
<td>µPD703185</td>
<td>µPD703186</td>
<td>µPD70F3186</td>
<td>µPD703116</td>
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<tr>
<td>CPU core</td>
<td>V806E1</td>
<td>V806E1</td>
<td>V806E1</td>
<td>V806E1</td>
</tr>
<tr>
<td>CPU performance</td>
<td>82 MPS (@ 64 MHz)</td>
<td>67 MPS (@ 50 MHz)</td>
<td>54 MPS (@ 40 MHz)</td>
<td>75 MPS (@ 32 MHz)</td>
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<tr>
<td>Internal ROM</td>
<td>128 KB (mask)</td>
<td>128 KB (mask)</td>
<td>512 KB (flash)</td>
<td>512 KB (flash)</td>
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<tr>
<td>Internal RAM</td>
<td>6 KB</td>
<td>12 KB</td>
<td>12 KB</td>
<td>12 KB</td>
</tr>
<tr>
<td>External bus interface</td>
<td>Bus type</td>
<td>Address bus</td>
<td>Data bus</td>
<td>Bus type</td>
</tr>
<tr>
<td>Data type</td>
<td>Multiplexed</td>
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<td>Multiplexed</td>
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<tr>
<td>Memory controller</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>External</td>
<td>53</td>
<td>49</td>
<td>External</td>
</tr>
<tr>
<td>Timer/counter</td>
<td>16-bit timer/event counter (TMQ) = 2 ch</td>
<td>16-bit timer/event counter (TMQ) = 1 ch</td>
<td>16-bit timer/event counter (TMQ) = 2 ch</td>
<td>16-bit timer/event counter (TMQ) = 2 ch</td>
</tr>
<tr>
<td></td>
<td>(inverter timer support possible)</td>
<td>(inverter timer support possible)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16-bit encoder counter/timer (TMENC) = 2 ch</td>
<td>16-bit encoder counter/timer (TMENC) = 1 ch</td>
<td>16-bit encoder counter/timer (TMENC) = 2 ch</td>
<td>16-bit encoder counter/timer (TMENC) = 2 ch</td>
</tr>
<tr>
<td></td>
<td>16-bit timer/event counter (TMP) = 2 ch</td>
<td>16-bit timer/event counter (TMP) = 1 ch</td>
<td>16-bit timer/event counter (TMP) = 2 ch</td>
<td>16-bit timer/event counter (TMP) = 2 ch</td>
</tr>
<tr>
<td></td>
<td>16-bit timer interval (TMM) = 1 ch</td>
<td>16-bit timer interval (TMM) = 1 ch</td>
<td>16-bit timer interval (TMM) = 1 ch</td>
<td>16-bit timer interval (TMM) = 1 ch</td>
</tr>
<tr>
<td>Watchdog timer</td>
<td>1 ch</td>
<td>1 ch</td>
<td>1 ch</td>
<td>1 ch</td>
</tr>
<tr>
<td>Serial interface</td>
<td>SCI = 1 ch</td>
<td>UART = 1 ch</td>
<td>SCI = 1 ch</td>
<td>UART = 1 ch</td>
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<td>SCI/UART = 1 ch</td>
<td>SCI/UART = 1 ch</td>
<td>SCI/UART = 1 ch</td>
<td>SCI/UART = 1 ch</td>
</tr>
<tr>
<td>A/D converter</td>
<td>10-bit × 4 ch, 2 units (conversion time: 2 μs)</td>
<td>10-bit × 2 ch (conversion time: 2 μs)</td>
<td>10-bit × 2 ch (conversion time: 2 μs)</td>
<td>10-bit × 8 ch, 2 units</td>
</tr>
<tr>
<td></td>
<td>8/10-bit × 8 ch</td>
<td>8/10-bit × 8 ch</td>
<td>8/10-bit × 8 ch</td>
<td>8/10-bit × 8 ch</td>
</tr>
<tr>
<td>DMA controller</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
</tr>
<tr>
<td>Ports</td>
<td>10</td>
<td>44</td>
<td>75</td>
<td>47</td>
</tr>
<tr>
<td>Debug control unit</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>1 ch</td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>0.5 to 64 MHz</td>
<td>4 to 64 MHz</td>
<td>4 to 64 MHz</td>
<td>4 to 64 MHz</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>2.5 V (internal), 5 V (A/D converter)</td>
<td>3.3 V (internal), 5 V (A/D converter)</td>
<td>5 V (external)</td>
<td>5 V (external)</td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>175 mW (internal 2.5 V, @ 64 MHz)</td>
<td>175 mW (internal 2.5 V, @ 64 MHz)</td>
<td>175 mW (internal 2.5 V, @ 64 MHz)</td>
<td>440 mW (5 V, @ 64 MHz operation)</td>
</tr>
<tr>
<td>Package</td>
<td>10-pin PLDF (14 × 14 mm)</td>
<td>14-pin LHFP (14 × 14 mm)</td>
<td>16-pin LHFP (14 × 14 mm)</td>
<td>16-pin LHFP (14 × 14 mm)</td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>–40°C to +85°C</td>
<td>–40°C to +85°C</td>
<td>–40°C to +85°C</td>
<td>–40°C to +85°C</td>
</tr>
</tbody>
</table>

### Notes
1. Number of external interrupts that can be used to release STOP mode.
2. Only V products have an on-chip HC interface.

## ASSP Lineup (2/3)

<table>
<thead>
<tr>
<th>Item</th>
<th>V800ES/IKA1</th>
<th>V800ES/IKA3</th>
<th>V800ES/PA1</th>
<th>V800ES/AC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part No.</td>
<td>µPD703327</td>
<td>µPD703329</td>
<td>µPD703034B/3034BY</td>
<td>µPD703036H/3036HY</td>
</tr>
<tr>
<td>CPU core</td>
<td>V806E1</td>
<td>V806E1</td>
<td>V806E1</td>
<td>V806E1</td>
</tr>
<tr>
<td>CPU performance</td>
<td>411 MPS (@ 32 MHz)</td>
<td>420 MPS (@ 13 MHz)</td>
<td>220 MPS (@ 19 MHz)</td>
<td>220 MPS (@ 19 MHz)</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>64 KB (mask)</td>
<td>128 KB (mask)</td>
<td>384 KB (mask)</td>
<td>512 KB (mask)</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>4 KB</td>
<td>6 KB</td>
<td>8 KB</td>
<td>16 KB</td>
</tr>
<tr>
<td>External bus interface</td>
<td>Bus type</td>
<td>Address bus</td>
<td>Data bus</td>
<td>Bus type</td>
</tr>
<tr>
<td>Data type</td>
<td>Multiplexed/separate</td>
<td>–</td>
<td>–</td>
<td>Multiplexed/separate</td>
</tr>
<tr>
<td>Memory controller</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>8</td>
<td>16</td>
<td>Internal</td>
</tr>
<tr>
<td>Timer/counter</td>
<td>6-bit timer/event counter (TBD) = 1 ch (inverter timer support possible)</td>
<td>16-bit timer/event counter (TMQ) = 1 ch</td>
<td>8-bit timer/event counter (TBD) = 1 ch</td>
<td>8-bit timer/event counter (TBD) = 1 ch</td>
</tr>
<tr>
<td></td>
<td>16-bit timer/event counter (TMQ) = 1 ch</td>
<td>(inverter timer support possible)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16-bit encoder counter/timer (TMENC) = 1 ch</td>
<td>(inverter timer support possible)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16-bit timer/event counter (TMP) = 1 ch</td>
<td>16-bit encoder counter/timer (TMENC) = 1 ch</td>
<td>16-bit encoder counter/timer (TMENC) = 1 ch</td>
<td>16-bit encoder counter/timer (TMENC) = 1 ch</td>
</tr>
<tr>
<td></td>
<td>16-bit timer/event counter (TMM) = 3 ch</td>
<td>16-bit timer/event counter (TMM) = 1 ch</td>
<td>16-bit timer/event counter (TMM) = 1 ch</td>
<td>16-bit timer/event counter (TMM) = 1 ch</td>
</tr>
<tr>
<td>Watchdog timer</td>
<td>1 ch</td>
<td>1 ch</td>
<td>–</td>
<td>–</td>
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<tr>
<td>Serial interface</td>
<td>SCI = 1 ch</td>
<td>UART = 2 ch</td>
<td>SCI = 1 ch</td>
<td>UART = 2 ch</td>
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<tr>
<td></td>
<td>UART = 1 ch</td>
<td>SCI/UART = 2 ch</td>
<td>SCI/UART = 2 ch</td>
<td>SCI/UART = 2 ch</td>
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<tr>
<td>A/D converter</td>
<td>10-bit × 4 ch, 2 units (conversion time: 2 μs)</td>
<td>10-bit × 4 ch, 2 units (conversion time: 2 μs)</td>
<td>10-bit × 4 ch, 2 units (conversion time: 2 μs)</td>
<td>10-bit × 4 ch, 2 units</td>
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<tr>
<td></td>
<td>8/10-bit × 8 ch</td>
<td>8/10-bit × 8 ch</td>
<td>8/10-bit × 8 ch</td>
<td>8/10-bit × 8 ch</td>
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<tr>
<td>DMA controller</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
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<tr>
<td>Ports</td>
<td>10</td>
<td>44</td>
<td>75</td>
<td>47</td>
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<tr>
<td>Debug control unit</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>1 ch</td>
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<tr>
<td>Power consumption (Typ.)</td>
<td>630 mW (internal 3.3 V, external 5 V, @ 50 MHz operation)</td>
<td>18-bit 3-phase sinusoidal PWM timer = 2 ch</td>
<td>16-bit timer/event counter = 2 ch</td>
<td>16-bit timer/event counter = 2 ch</td>
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<tr>
<td>Operating frequency</td>
<td>20 to 32 MHz</td>
<td>4 to 8 MHz</td>
<td>4 to 8 MHz</td>
<td>4 to 8 MHz</td>
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### Notes
1. Number of external interrupts that can be used to release STOP mode.
2. Only V products have an on-chip HC interface.
### ASSP Lineup (2/3)

<table>
<thead>
<tr>
<th>Item</th>
<th>µPD703230</th>
<th>µPD70F3230</th>
<th>µPD703231</th>
<th>µPD70F3231</th>
<th>µPD703232</th>
<th>µPD70F3232</th>
<th>µPD703233</th>
<th>µPD70F3233</th>
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<tbody>
<tr>
<td><strong>Part No.</strong></td>
<td><strong>V850ES/FE2</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES/FP2</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
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<tr>
<td><strong>CPU core</strong></td>
<td>µPD703230</td>
<td>µPD70F3230</td>
<td>µPD703231</td>
<td>µPD70F3231</td>
<td>µPD703232</td>
<td>µPD70F3232</td>
<td>µPD703233</td>
<td>µPD70F3233</td>
</tr>
<tr>
<td><strong>CPU performance</strong></td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
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<tr>
<td><strong>Internal RAM</strong></td>
<td>64 KB (mask)</td>
<td>64 KB (flash)</td>
<td>128 KB (mask)</td>
<td>128 KB (flash)</td>
<td>128 KB (mask)</td>
<td>128 KB (flash)</td>
<td>256 KB (mask)</td>
<td>256 KB (flash)</td>
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<td><strong>External bus interface</strong></td>
<td>Bus type</td>
<td>Address bus</td>
<td>Data bus</td>
<td>Chip select signal</td>
<td></td>
<td></td>
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<tr>
<td><strong>Memory controller</strong></td>
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<td><strong>Interrupt sources</strong></td>
<td>Internal</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Power supply voltage</strong></td>
<td>5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
</tr>
<tr>
<td><strong>Power consumption (Typ.)</strong></td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>64-pin TQFP (10 x 10 mm)</td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Operating ambient temperature</strong></td>
<td>-40°C to +85°C, -40°C to +110°C</td>
<td></td>
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**Note:** Number of external interrupts that can be used to release STOP mode

---

<table>
<thead>
<tr>
<th>Item</th>
<th>µPD703234</th>
<th>µPD70F3234</th>
<th>µPD703235</th>
<th>µPD70F3235</th>
<th>µPD703236</th>
<th>µPD70F3236</th>
<th>µPD703237</th>
<th>µPD70F3237</th>
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<tbody>
<tr>
<td><strong>Part No.</strong></td>
<td><strong>V850ES/FE2</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES/FP2</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
</tr>
<tr>
<td><strong>CPU core</strong></td>
<td>µPD703234</td>
<td>µPD70F3234</td>
<td>µPD703235</td>
<td>µPD70F3235</td>
<td>µPD703236</td>
<td>µPD70F3236</td>
<td>µPD703237</td>
<td>µPD70F3237</td>
</tr>
<tr>
<td><strong>CPU performance</strong></td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
</tr>
<tr>
<td><strong>Internal RAM</strong></td>
<td>128 KB (mask)</td>
<td>128 KB (flash)</td>
<td>256 KB (mask)</td>
<td>256 KB (flash)</td>
<td>384 KB (flash)</td>
<td>384 KB (flash)</td>
<td>512 KB (flash)</td>
<td>512 KB (flash)</td>
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<td><strong>External bus interface</strong></td>
<td>Bus type</td>
<td>Address bus</td>
<td>Data bus</td>
<td>Chip select signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td><strong>Memory controller</strong></td>
<td></td>
<td></td>
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<td></td>
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</tr>
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<td><strong>Interrupt sources</strong></td>
<td>Internal</td>
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<tr>
<td><strong>Power supply voltage</strong></td>
<td>5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
</tr>
<tr>
<td><strong>Power consumption (Typ.)</strong></td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>64-pin TQFP (10 x 10 mm)</td>
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<td></td>
<td></td>
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<tr>
<td><strong>Operating ambient temperature</strong></td>
<td>-40°C to +85°C, -40°C to +110°C</td>
<td></td>
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</table>

**Note:** Number of external interrupts that can be used to release STOP mode

---

**Note:** Number of external interrupts that can be used to release STOP mode

---

<table>
<thead>
<tr>
<th>Item</th>
<th>µPD703230</th>
<th>µPD70F3230</th>
<th>µPD703231</th>
<th>µPD70F3231</th>
<th>µPD703232</th>
<th>µPD70F3232</th>
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<th>µPD70F3233</th>
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<tbody>
<tr>
<td><strong>Part No.</strong></td>
<td><strong>V850ES/FE2</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES/FP2</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
<td><strong>V850ES</strong></td>
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<tr>
<td><strong>CPU core</strong></td>
<td>µPD703230</td>
<td>µPD70F3230</td>
<td>µPD703231</td>
<td>µPD70F3231</td>
<td>µPD703232</td>
<td>µPD70F3232</td>
<td>µPD703233</td>
<td>µPD70F3233</td>
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<tr>
<td><strong>CPU performance</strong></td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
<td>32 MPPS (20 MHz)</td>
</tr>
<tr>
<td><strong>Internal RAM</strong></td>
<td>64 KB (mask)</td>
<td>64 KB (flash)</td>
<td>128 KB (mask)</td>
<td>128 KB (flash)</td>
<td>128 KB (mask)</td>
<td>128 KB (flash)</td>
<td>256 KB (mask)</td>
<td>256 KB (flash)</td>
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<tr>
<td><strong>External bus interface</strong></td>
<td>Bus type</td>
<td>Address bus</td>
<td>Data bus</td>
<td>Chip select signal</td>
<td></td>
<td></td>
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<tr>
<td><strong>Memory controller</strong></td>
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<td></td>
<td></td>
</tr>
<tr>
<td><strong>Interrupt sources</strong></td>
<td>Internal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Power supply voltage</strong></td>
<td>5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
</tr>
<tr>
<td><strong>Power consumption (Typ.)</strong></td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
<td>155 mW @ (5.0 V, 20 MHz)</td>
<td>170 mW @ (5.0 V, 20 MHz)</td>
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<tr>
<td><strong>Package</strong></td>
<td>64-pin TQFP (10 x 10 mm)</td>
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<td></td>
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</tr>
<tr>
<td><strong>Operating ambient temperature</strong></td>
<td>-40°C to +85°C, -40°C to +110°C</td>
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**Note:** Number of external interrupts that can be used to release STOP mode

---

**Note:** Number of external interrupts that can be used to release STOP mode
### ASSP Lineup (3/3)

<table>
<thead>
<tr>
<th>Item</th>
<th>V850ES/F1</th>
<th>V850ES/F1B1</th>
<th>V850ES/F1S8</th>
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<tbody>
<tr>
<td><strong>Part No.</strong></td>
<td>μPD703075AY</td>
<td>μPD703076AY</td>
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<tr>
<td>CPU core</td>
<td>V850</td>
<td>V850</td>
<td>V850ES</td>
</tr>
<tr>
<td>CPU performance</td>
<td>16 MIPS (@ 15 MHz)</td>
<td>16 MIPS (@ 15 MHz)</td>
<td>25 MIPS (@ 20 MHz)</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>128 KB (mask)</td>
<td>256 KB (mask)</td>
<td>128 KB (mask)</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>12 KB</td>
<td>16 KB</td>
<td>9 KB</td>
</tr>
<tr>
<td>Internal bus interface</td>
<td>Multiplexed</td>
<td>Multiplexed</td>
<td>Multiplexed</td>
</tr>
<tr>
<td>Address bus</td>
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<tr>
<td>Data bus</td>
<td>16 bits</td>
<td>16 bits</td>
<td>16 bits</td>
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<tr>
<td>Memory controller</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
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<tr>
<td>Interrupt sources</td>
<td>Internal 35</td>
<td>Internal 35</td>
<td>Internal 35</td>
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<td>Operating frequency</td>
<td>10 to 40.5 MHz</td>
<td>10 to 40.5 MHz</td>
<td>10 to 40.5 MHz</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>2.3 to 2.7 V (internal)</td>
<td>2.7 to 3.6 V (external)</td>
<td>2.3 to 3.6 V (@ 20 MHz)</td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>134 mW (@ 2.5 V, 40.5 MHz)</td>
<td>159 mW (@ 2.5 V, 40.5 MHz)</td>
<td>82 mW (@ 3.3 V, 20 MHz)</td>
</tr>
<tr>
<td>Package</td>
<td>257-pin FBGA (14 x 14 mm)</td>
<td>176-pin LQFP (24 x 24 mm)</td>
<td>180-pin FBGA (13 x 13 mm)</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

**Notes:**
1. Number of external interrupts that can be used to release STOP mode.
2. Only Y products have an on-chip I 2 C interface.
3. Input port has an on-chip I 2 C interface.

### Itemized List

<table>
<thead>
<tr>
<th>Item</th>
<th>V850/F5Y</th>
<th>V850/F3Y</th>
<th>V850/F3Y1</th>
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<tbody>
<tr>
<td><strong>Part No.</strong></td>
<td>μPD703166/3166Y</td>
<td>μPD70F3166/F3166Y</td>
<td>μPD70F3166/F3166Y</td>
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<tr>
<td>CPU core</td>
<td>V850</td>
<td>V850</td>
<td>V850ES</td>
</tr>
<tr>
<td>CPU performance</td>
<td>25 MIPS (@ 20 MHz)</td>
<td>25 MIPS (@ 20 MHz)</td>
<td>25 MIPS (@ 20 MHz)</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>512 KB (mask)</td>
<td>512 KB (flash)</td>
<td>295 KB (mask)</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>24 KB</td>
<td>8 KB</td>
<td>16 KB</td>
</tr>
<tr>
<td>Memory controller</td>
<td>Watchdog timer</td>
<td>Watchdog timer</td>
<td>Watchdog timer</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>2.7 to 3.6 V (A/D converter: 4.5 to 5.5 V)</td>
<td>4.0 to 5.5 V</td>
<td>4.0 to 5.5 V</td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>75 mW (@ 5 V, 16 MHz)</td>
<td>125 mW (@ 5 V, 16 MHz)</td>
<td>180 mW (@ 5 V, 16 MHz)</td>
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<tr>
<td>Package</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin QFP (14 x 20 mm)</td>
<td>100-pin QFP (14 x 20 mm)</td>
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<td>Operating temperature</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

**Notes:**
- Boundary scan function: 12- to 16-bit PWM output: 5 ch, real-time output, ROM correction function: 4 points
- Watch timer: 1 ch, 12- to 16-bit PWM output: 4 ch, ROM correction function: 4 points
- Real-time output, ROM correction function: 8 points
- I 2 C: 1 ch
- UART: 1 ch
- CAN 1 ch
- DCAN controller: 1 ch
- Real-time counter: 1 ch

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Pamphlet U15412EJ4V1PF
### High-End Lineup (1/2)

<table>
<thead>
<tr>
<th>Item</th>
<th>µPD703131A/3131AY</th>
<th>µPD703132A/3132AY</th>
<th>µPD703133A/3133AY</th>
<th>µPD703134A/3134AY</th>
<th>µPD703144A/3144AY</th>
<th>µPD703111A</th>
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<td>V850E1</td>
<td>V850E1</td>
<td>V850E1</td>
<td>V850E1</td>
<td>V850E1</td>
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<td>CPU performance</td>
<td>106 MIPS (@ 80 MHz)</td>
<td>215 MIPS (@ 150 MHz)</td>
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</tr>
<tr>
<td>Internal ROM</td>
<td>256 KB (mask)</td>
<td>512 KB (mask)</td>
<td>512 KB (flash)</td>
<td>ROM-less (instruction cache: 8 KB)</td>
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<td></td>
</tr>
<tr>
<td>External bus interface</td>
<td>Bus type</td>
<td>Multiple/external</td>
<td>Separate</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Address bus</td>
<td>26 bits</td>
<td>26 bits</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data bus</td>
<td>8/16 bits</td>
<td>8/16/32 bits</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Memory controller</td>
<td>SDRAM, SRAM, etc.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>41</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>External</td>
<td>20(20)</td>
<td></td>
<td>40(40)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer/counter</td>
<td>16-bit timer/event counter (TMD) = 4 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16-bit timer/event counter (TMP) = 3 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16-bit timer/event counter (TMC) = 1 ch ( external timer support possible)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16-bit encoder counter/timer (TMENC) = 1 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watchdog timer</td>
<td>1 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial interface</td>
<td>CSUIAR = 3 ch</td>
<td>CSUIAR/T = 1 x/2 x</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A/D converter</td>
<td>8-bit = 8 ch</td>
<td>10-bit = 8 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D/A converter</td>
<td>8-bit = 2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMA controller</td>
<td>4 ch</td>
<td>4 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ports</td>
<td>I/O</td>
<td>101</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Debug control unit</td>
<td>Provided (RUN, break)</td>
<td>Provided (RUN, break, trace)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>2.3 to 2.7 V (internal)/3.0 to 3.6 V (external)</td>
<td>1.35 to 1.65 V (internal)/3.0 to 3.6 V (external) (@ 135 MHz)</td>
<td>1.40 to 1.65 V (internal)/3.0 to 3.6 V (external) (@ 150 MHz)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>T.B.D.</td>
<td>575 mW (@2.5 V, 80 MHz)</td>
<td>200 mW (@ 1.5 V, 150 MHz)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td>144-pin LFQVF (20 × 20 mm)</td>
<td>161-pin FBGA (13 × 13 mm)</td>
<td>176-pin LFQVF (24 × 24 mm)</td>
<td>240-pin FBGA (16 × 16 mm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Number of external interrupts that can be used to release STOP mode
2. Only Y ports have an on-chip I²C interface

### High-End Lineup (2/2)

<table>
<thead>
<tr>
<th>Item</th>
<th>µPD703103A</th>
<th>µPD703105A</th>
<th>µPD703107A</th>
<th>µPD703107A</th>
<th>µPD703108</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU core</td>
<td>V850E1</td>
<td>V850E1</td>
<td>V850E1</td>
<td>V850E1</td>
<td>V850E1</td>
</tr>
<tr>
<td>CPU performance</td>
<td>67 MIPS (@ 50 MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal ROM</td>
<td>ROM-less</td>
<td>128 KB (mask)</td>
<td>256 KB (mask)</td>
<td>256 KB (flash)</td>
<td>ROM-less</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>4 KB</td>
<td>10 KB</td>
<td>4 KB</td>
<td>4 KB</td>
<td></td>
</tr>
<tr>
<td>External bus interface</td>
<td>Bus type</td>
<td>Separate</td>
<td>Separate</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Address bus</td>
<td>26 bits</td>
<td>26 bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data bus</td>
<td>8/16 bits</td>
<td>8/16/32 bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory controller</td>
<td>SDRAM, SRAM, etc.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>33</td>
<td></td>
<td></td>
<td>23</td>
</tr>
<tr>
<td></td>
<td>External</td>
<td>26 (17)</td>
<td></td>
<td>8 (4)</td>
<td></td>
</tr>
<tr>
<td>Timer/counter</td>
<td>16-bit timer/event counter (TMD) = 4 ch</td>
<td></td>
<td></td>
<td></td>
<td>16-bit timer/event counter (TMD) = 2 ch</td>
</tr>
<tr>
<td></td>
<td>16-bit timer/event counter (TMP) = 3 ch</td>
<td></td>
<td></td>
<td></td>
<td>16-bit timer/event counter (TMD) = 4 ch</td>
</tr>
<tr>
<td>Watchdog timer</td>
<td>CSUIAR = 2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial interface</td>
<td>CSUIAR = 2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>UART = 1 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A/D converter</td>
<td>10-bit = 8 ch</td>
<td>10-bit = 4 ch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D/A converter</td>
<td></td>
<td>4 ch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMA controller</td>
<td>4 ch</td>
<td>4 ch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ports</td>
<td>I/O</td>
<td>106</td>
<td></td>
<td></td>
<td>74</td>
</tr>
<tr>
<td>Debug control unit</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>3.0 to 3.6 V</td>
<td></td>
<td></td>
<td></td>
<td>3.0 to 3.6 V</td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>528 mW (@ 3.3 V, 50 MHz)</td>
<td>627 mW (@ 3.3 V, 50 MHz)</td>
<td>416 mW (@ 3.3 V, 40 MHz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td>144-pin LFQVF (20 × 20 mm)</td>
<td>144-pin LFQVF (20 × 20 mm)</td>
<td>161-pin FBGA (13 × 13 mm)</td>
<td>100-pin LFQVF (14 × 14 mm)</td>
<td></td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

Note: Number of external interrupts that can be used to release STOP mode
## High-End Lineup (2/2)

<table>
<thead>
<tr>
<th>Item</th>
<th>V850E/MS1</th>
<th>V850E/MS2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part No.</td>
<td>µPD703108A-33/40</td>
<td>µPD703108A-33/40</td>
</tr>
<tr>
<td>CPU core</td>
<td>V850E1</td>
<td>V850E1</td>
</tr>
<tr>
<td>CPU performance</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>ROM-less</td>
<td>96 KB (mask)</td>
</tr>
<tr>
<td>External RAM</td>
<td>4 KB</td>
<td>4 KB</td>
</tr>
<tr>
<td>External bus interface</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Address bus</td>
<td>24 bits</td>
<td>20 bits</td>
</tr>
<tr>
<td>Data bus</td>
<td>8/16 bits</td>
<td>8/16 bits</td>
</tr>
<tr>
<td>Chip select signal</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>Memory controller</td>
<td>EDO DRAM, SRAM, etc.</td>
<td>EDO DRAM, SRAM, etc.</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>Internal</td>
</tr>
<tr>
<td>Interface</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Bus type</td>
<td>Separate</td>
<td>Separate</td>
</tr>
<tr>
<td>Address bus</td>
<td>20 bits</td>
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<tr>
<td>Data bus</td>
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<tr>
<td>Chip select signal</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Memory controller</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>External timer/counters</td>
<td>16-bit timer/event counter = 6 ch</td>
<td>16-bit timer/event counter = 4 ch</td>
</tr>
<tr>
<td>Internal</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Serial interface</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>A/D converter</td>
<td>10-bit × 8 ch</td>
<td>10-bit × 4 ch</td>
</tr>
<tr>
<td>D/A converter</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>DMA controller</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Ports</td>
<td>1/0</td>
<td>1/0</td>
</tr>
<tr>
<td>I/O</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Debug control unit</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Other peripheral functions</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>2 to 40 MHz (-40 product)</td>
<td>2 to 33 MHz (-33 product)</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>3.0 to 3.6 V (internal, external) (A products)</td>
<td>3.0 to 3.6 V (internal)</td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>272 mW (@ 3.3 V, 33 MHz)</td>
<td>294 mW (@ 3.3 V, 33 MHz)</td>
</tr>
<tr>
<td>Package</td>
<td>100-pin LQFP (14 × 20 mm)</td>
<td>–</td>
</tr>
</tbody>
</table>

### Notes
1. Number of external interrupts that can be used to release STOP mode
2. µPD703108A-33, 703101A-33, 703102A-33, and 70F3102A-33 only
3. µPD703100A-40, 703100A-40: -40°C to +70°C
4. Others: -40°C to +85°C

<table>
<thead>
<tr>
<th>Item</th>
<th>V853</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part No.</td>
<td>µPD703003A</td>
</tr>
<tr>
<td>CPU core</td>
<td>V850</td>
</tr>
<tr>
<td>CPU performance</td>
<td>–</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>128 KB (mask)</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>4 KB</td>
</tr>
<tr>
<td>External bus interface</td>
<td>–</td>
</tr>
<tr>
<td>Address bus</td>
<td>20 bits</td>
</tr>
<tr>
<td>Data bus</td>
<td>16 bits</td>
</tr>
<tr>
<td>Chip select signal</td>
<td>–</td>
</tr>
<tr>
<td>Memory controller</td>
<td>–</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
</tr>
<tr>
<td>Interface</td>
<td>–</td>
</tr>
<tr>
<td>External timer/counters</td>
<td>16-bit timer/event counter = 4 ch</td>
</tr>
<tr>
<td>Internal</td>
<td>–</td>
</tr>
<tr>
<td>Serial interface</td>
<td>–</td>
</tr>
<tr>
<td>A/D converter</td>
<td>10-bit × 8 ch</td>
</tr>
<tr>
<td>D/A converter</td>
<td>–</td>
</tr>
<tr>
<td>DMA controller</td>
<td>–</td>
</tr>
<tr>
<td>Ports</td>
<td>I/O</td>
</tr>
<tr>
<td>I/O</td>
<td>–</td>
</tr>
<tr>
<td>Debug control unit</td>
<td>–</td>
</tr>
<tr>
<td>Other peripheral functions</td>
<td>–</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>–</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>–</td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>365 mW (@ 5 V, 33 MHz)</td>
</tr>
<tr>
<td>Package</td>
<td>100-pin LFQFP (14 × 14 mm)</td>
</tr>
</tbody>
</table>

### Notes
1. Number of external interrupts that can be used to release STOP mode

---

Pamphlet U15412EJ4V1PF
The V850 Series development environment consists of tools designed to make the development of application systems using the V850 Series of high-performance microcontrollers made by NEC Electronics more pleasant, faster, and more accurate. Each one of these development tools features functions to fully exploit the performance of the V850 Series.
Low-Priced Development Environment Lineup

Emulator and evaluation board available at low prices

Low-priced full-function emulator
IECUBE
- Low prices 1/3 or 1/4 the price of conventional emulators
- Connectable to PC via USB
- Enhanced real-time RAM monitor and time measuring function
- On-chip self-diagnosis function
- Debugger and simple programmer provided
- Palm size

Ultra-low-priced on-chip emulator
N-Wire CARD
- Ultra low price 1/10 the price of conventional emulators
- Connectable to PC via PCMCIA
- Writing to the microcontroller on-chip flash memory possible
- Debugger provided

Starter kit for simple evaluation
TK-850 Series
- Evaluation kit enabling easy performance testing
- Lineup for V850ES/Kx1, V850ES/SA2, and V850ES/SG2
- Debugger, compiler, and circuit diagrams provided as standard

* For details, refer to V850 Series Development Environment Pamphlet (U15763E)
Development Environment

Development Tools (1/3)

Software tools

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Product Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software package</td>
<td>SP850</td>
</tr>
<tr>
<td>C compiler</td>
<td>CA850</td>
</tr>
<tr>
<td>Device file</td>
<td>DF703xxx</td>
</tr>
<tr>
<td>Project Manager</td>
<td>PM plus</td>
</tr>
<tr>
<td>Integrated debugger</td>
<td>ID850</td>
</tr>
<tr>
<td>System simulator</td>
<td>SM850</td>
</tr>
<tr>
<td>Real-time OS</td>
<td>RX850, RX850 Pro</td>
</tr>
<tr>
<td>Task debugger</td>
<td>RD850, RD850 Pro</td>
</tr>
<tr>
<td>System performance analyzer</td>
<td>AZ850</td>
</tr>
<tr>
<td>Middleware</td>
<td>AP703000-Bxxxx, AP703100-Bxxxx</td>
</tr>
<tr>
<td>Performance analysis tool</td>
<td>TW850</td>
</tr>
</tbody>
</table>

Notes
1. Packaged in SP850
2. Downloaded from the NEC Electronics Website. (URL: http://www.necel.com/micro/index_e.html)
3. Included with CA850
4. Included with IECUBE and IE-V850E1-CD-NW.
5. Instruction simulation version: Included with SP850.
6. Instruction + peripheral simulation version: Only the SM plus for the μPD70F3261Y is included with SP850.
7. Included with RX850, RX850 Pro

Remark For details, refer to the V850 Series Development Environment Pamphlet (U15763E).
## Development Tools (2/3)

### Hardware tools (when using IECUBE)

<table>
<thead>
<tr>
<th>Target Device</th>
<th>In-Circuit Emulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>V850ES/SC2, V850ES/SC2</td>
<td>QB-V850ESX2-ZZZ</td>
</tr>
<tr>
<td>V850ES/A2, V850ES/A4, V850ES/K1</td>
<td>QB-V850ESA4-ZZZ</td>
</tr>
<tr>
<td>V850ES/KE1, V850ES/KE1+, V850ES/KF1, V850ES/KF1+, V850ES/KG1, V850ES/KG1+, V850ES/KJ1, V850ES/KJ1+, μPD703229Y, 70F3229Y</td>
<td>QB-V850ES9KX1H-ZZZ</td>
</tr>
</tbody>
</table>

Remarks:
1. A separate socket is required for each above emulator.
2. A power supply, a USB interface cable, a debugger, and a simple programmer are included. A PC interface board is not required.
3. For details, refer to the V850 Series Development Environment Pamphlet (U15763E).

### Hardware tools (when using N-Wire CARD)

<table>
<thead>
<tr>
<th>Target Device</th>
<th>On-Chip Debug Emulator</th>
</tr>
</thead>
</table>

Remarks:
1. A target connection cable, a connector conversion board, a target connector, and a debugger are included.
2. A power supply and a PC interface board are not required.
3. For details, refer to the V850 Series Development Environment Pamphlet (U15763E).

### Hardware tools (using other emulators)

<table>
<thead>
<tr>
<th>Target Device</th>
<th>Main Unit</th>
<th>In-Circuit Emulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>V850ES/SA2, V850ES/SA3</td>
<td>IE-V850ES-G1</td>
<td>IE-703204-G1-EM1***</td>
</tr>
<tr>
<td>V850ES/SC2, V850ES/SC2</td>
<td>IE-V850E-MC-A</td>
<td>IE-703166-MC-EM1</td>
</tr>
<tr>
<td>V850ES/KA1, V850E/MA2</td>
<td>IE-V850E-MC</td>
<td>IE-703107-MC-EM1***</td>
</tr>
<tr>
<td>V850ES/SC2, V850ES/SC2</td>
<td>IE-V850E-MC</td>
<td>IE-703114-MC-EM1</td>
</tr>
<tr>
<td>V850ES/SC2, V850ES/SC2</td>
<td>IE-V850E-MC</td>
<td>IE-703102-MC-EM1A</td>
</tr>
<tr>
<td>V850ES/SC2, V850ES/SC2</td>
<td>IE-V850E-MC</td>
<td>IE-703031-MC-EM1***</td>
</tr>
<tr>
<td>V850ES/SC2, V850ES/SC2</td>
<td>IE-V850E-MC</td>
<td>IE-703040-MC-EM1***</td>
</tr>
<tr>
<td>V850ES/SC2, V850ES/SC2</td>
<td>IE-V850E-MC</td>
<td>IE-703079-MC-EM1***</td>
</tr>
<tr>
<td>V850ES/SC2, V850ES/SC2</td>
<td>IE-V850E-MC</td>
<td>IE-703089-MC-EM1</td>
</tr>
<tr>
<td>V850ES/SC2, V850ES/SC2</td>
<td>IE-V850E-MC</td>
<td>IE-703093-MC-EM1</td>
</tr>
</tbody>
</table>

Notes:
1. A separate socket and probe are required for connection to the target system.
2. A separate socket may be required for connection to the target system.
3. Depending on the target device package, a separate socket and probe may be required.
4. The optional PC interface board (IE-70000-PCI-I-A or IE-70000-CD-I-F-A) are required as a common part.
5. The following items are required as common items.
   - Power supply: IE-70000-SC-P2
   - For details, refer to the V850 Series Development Environment Pamphlet (U15763E).
**Development Tools (3/3)**

- **IECUBE configuration example**
  - 1. In-circuit emulator (IECUBE)
  - 2. AC adapter (provided with ①)
  - 3. USB interface cable (provided with ③)
  - 4. Extension probe
  - 5. Exchange adapter (provided with ⑤ Note)
  - 6. Target connector (provided with ① Note)
  - 7. Mount adapter

  **Note** If ordering the in-circuit emulator (①), if the part number ends in “-ZZZ”, the above exchange adapter (⑤) and target connector (⑥) are not provided.

- **IE-V850ES-G1 configuration example**
  - 1. In-circuit emulator (main unit)
  - 2. Emulation board (connected inside main unit)
  - 3. Emulation probe
  - 4. Conversion adapter/conversion socket
  - 5. PC interface cable (provided with ③)
  - 6. Power supply cable (provided with ⑤)

- **N-Wire CARD configuration example**
  - 1. Host machine (with PCMCIA slot)
  - 2. On-chip emulator IE-V850E1-CD-NW
  - 3. In-circuit emulator connection cable
  - 4. Connector conversion board
  - 5. In-circuit emulator connector

- **IE-V850E-MC, IE-V850E-MC-A, IE-703102-MC, IE-703002-MC configuration example**
  - 1. In-circuit emulator (main unit)
  - 2. Option board
  - 3. Power supply unit
  - 4. Conversion adapter/conversion socket (provided with ②)
  - 5. PC interface cable (provided with ⑤)
Development environment using in-circuit emulator, N-Wire emulator

Integrated development environment

Note: The RD850, RD850 Pro, and AZ850 can be used with the ID850, ID850QB, MULTI, PARTNER, and WATCHPOINT.

Refer to Development Tools Hardware tools (when using N-Wire CARD) (p. 55)

Refer to Development Tools Hardware tools (when using IECUBE) (p. 55)

Refer to Development Tools Hardware tools (when using IECUBE) (p. 55)
Development Environment

V850 Series Development Environment (2/2)

Development environment using ROM emulator, evaluation board

Note: RD850, RD850 Pro, and AZ850 can be used with MULTI, PARTNER.

APPLY: Application Corporation
ATI: Accelerated Technology, Inc.
Cosmo: Cosmo Co., Ltd.
Red Hat: Red Hat Corporation
GAIO: Gaio Technology Co., Ltd.
GHS: Green Hills Software, Inc.
KMC: Kyoto Microcomputer Corporation
Lightwell: Lightwell Co., Ltd.

Metrowerks: Metrowerks Corporation
Midas Lab: Midas Lab, Co., Ltd.
Midoriya: Midoriya Electric Co., Ltd.
Misp: MiSPO, Inc.
WRS: Wind River Systems, Inc.
eSOL: eSOL Co., Ltd.
Unmarked: NEC Electronics
Software package (SP850)

Product configuration
The SP850 software package consists of the following software development tools.
• C compiler (CA850)
• Project Manager (PM plus)
• Integrated debugger (ID850, ID850NW) (to be packaged)
• System simulator (SM850, SM plus) (to be packaged)
• Performance analysis tuning tool (TW850)
• Device file (DF703xxx)

Features
• Complies with ANSI-C, a C language standard.
• Supports libraries for embedded systems
• Compact code size and faster execution speed can be realized through powerful optimization
• Utilities useful for embedded systems (ROMization processor, etc.)
• Description of embedded systems in C language (specification of memory allocation and I/O register access) is possible.

System simulator (SM850, SM plus)

Features
• Same operability as debugger
• Target-less evaluation prior to target completion possible
• In addition to the operation of the CPU itself, target system operation including on-chip peripheral unit and interrupt servicing can also be simulated.
• Pseudo-target system construction and I/O operation are possible through external parts.
• Data generated by 0/1 logic and timing charts can be input to the program being simulated.
• Larger number of events than in-circuit emulator
• Execution speed estimates can be done on the host machine to accurately simulate pipeline operation
• Construction by user target system users is possible through user open interface
• A peripheral I/O register status can be specified and when this status occurs, the system can be made to output an interrupt at the desired timing or transfer data to memory (peripheral I/O register event & action function).

Project manager (PM plus)

Features
• Project management (management of target chip, source, and environment during debugging is possible.)
• Supports wizard function during project creation
• Automation of series of operations consisting of edit, build, and debug
• Integration of Help function

N-Wire card (IE-V850E1-CD-NW)

Features
• Supports V850E and V850ES
• Emulator for on-chip debugging
• Enables realization of low-cost development environment
• Compact PC card type
• Function for download to internal flash ROM
• Same ease of operation as ID850

Target Devices

Note Only SM plus is supported
Development Environment

Integrated debugger (ID850, ID850NW, ID850QB)

- Features
  - Supports object files
  - Debugging at source level
  - Debugging using target resources
  - Real-time execution on target
  - Event setting according to complex software operation
  - Online help function

Real-time OSs (RX850, RX850 Pro)

- Features
  - Comply with global standard (μITRON 3.0 specifications).
  - Support power management function.
  - Enable embedding of required functions only (selection of system calls to be used).
  - Support sophisticated task development through task debugger (RD).
  - Support application operation analysis through system performance analyzer (AZ)
  - Inherit attributes of real-time OS of 16-bit V Series and 78K Series

System performance analyzer (AZ850)

- Features
  - Detection of bugs through system timing errors
  - Detection of bugs due to simultaneous operation of complex tasks
  - Detection/analysis of real-time system execution performance
  - Operation linked to various debuggers

Task debuggers (RD850, RD850 Pro)

- Features
  - Display detailed information on OS resources such as tasks.
  - Display source of referenced tasks.
  - Included with real-time OS (RX850, RX850 Pro)

TCP/IP software library (RX-NET) for V850E products

- Product configuration
  - TCP/IP protocol stack
  - Applications
  - LAN control driver

- Features
  - RFC-compliant
  - Support of numerous socket interfaces/libraries
  - Support of applications as option products
  - Provided device driver
  - Support of NEC Electronics real-time OS (RX850 Pro)

Target devices
V850E products

Performance analysis tuning tool (TW850)

- Features
  - Performance analysis changing the internal ROM size, instruction cache size, etc., is possible.
  - Display of inter-function call relationships, call count information, function execution time information, and cache mishit information
  - Functions optimally placed to reduce cache mishit count
  - Functions causing bottlenecks placed into internal ROM or other high-speed access memory

In-circuit emulator (IE, IECUBE)

- Features
  - Emulator functions loaded in dedicated chip to realize high equivalence
  - Connectable to variety of computers
  - Large array of emulation functions
  - Realization of maximum operating frequency equivalent to that of device
OSEK/VDX specifications compliant OS (RX-OSEK850)

- **Features**
  - **Kernel**
    Compliant with OSEK/VDX OS Ver. 2.0 specifications
    Supports 4 conformance classes: BCC1, BCC2, ECC1, and ECC2.
  - **Configurator**
    Configurator (OIL850) allowing easy system information creation provided as standard.
    Configuration files support formats compatible with OIL Ver. 2.0.
  - **Task debugger (RD-OSEK850)**
    Task debugger effective for application debugging using RX-OSEK850 provided as standard

RISC microcontroller reference platform (SolutionGear™)

- **Features**
  - General-purpose evaluation boards available as RISC microcontroller software development platform
  - Target CPU: V850E/MA1, V850E/ME2
  - Industry standard PC-compatible interfaces including PCI, ISA, PCMCIA, E-IDE, Ethernet™, Serial, Parallel, PS/2, and USB, provided
  - CPU independent motherboards and CPU boards used combined
  - Bundled real-time OS, middleware, and sample drivers
  - MULTI-PARTNER remote monitor version can be used
  - Reference design information provided

Cooperation with third parties

By deepening cooperation with third-party companies and forming an array of tools combining NEC Electronics-made tools and third-party-made tools, NEC Electronics offers development environments that support the diverse needs of users.
Information about V850 microcontrollers and V850 microcontroller development environment can be viewed at the NEC Electronics Microcomputer website.

http://www.necel.com/micro/index_e.html

**Microcontroller Search Tool**
- Facility for searching for V850 Series microcontrollers by function

**Product Lineup**
- Microcontroller product information

**Document Download**
- Microcontroller, development environment, and middleware documents can be downloaded from this area.

**Development Tool Download**
- V850 Series development tools can be downloaded from this area. Customers who are registered users receive upgrade information by email.
Microcontroller Search Tool

Facility for searching V850 Series microcontrollers by function.

Specify search condition(s) here.

The corresponding NEC Electronics development environment documents can be searched from here with a single link.
Product Lineup

32V850 Series

High-end evolution
- Highly efficient pursuit, MENC, On-chip DMA
- Frequency: 33~150MHz
- Memory ROM: 64~640KB
- Memory RAM: 4~48KB
- Packages: 100~176-pin (QFP & FBGA)

Middle-range evolution
- Realization of a low EMI noise
- Frequency: 20~32MHz
- Memory ROM: 64~256KB
- Memory RAM: 4~16KB
- Packages: 100~144-pin (QFP)

Low-end evolution
- Pursuit of performance
- Frequency: 33MHz
- Memory ROM: 64~250KB
- Memory RAM: 4~16KB
- Packages: 64~144-pin (QFP)

Core release of CPU is completed.
In the midst of product development plan.

Inverter control
DVC control
Airbag control
Car audio control
Electric power meter control
Car electronics control

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