NEC

MOS INTEGRATED CIRCUIT

μPD78P218A

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78P218A, a product of the 78K/II series, is an 8-bit single-chip microcomputer which one-time PROM or EPROM in place of the mask ROM in the μPD78218A. Since the μPD78P218A is user-programmable, it is suitable for system development evaluation and small production.

Functions are described in detail in the following user's manuals, which should be read when carrying out design work

μPD78218A Subseries User's Manual Hardware Volume: IEM-755
78K/II Series User's Manual Instruction Volume: IEU-754

FEATURES

- Upward compatibility with the μPD78214 subseries (pin compatibility)
- Compatibility with the μPD78218A (except PROM programming)
- High-speed instruction execution (at 12 MHz operation): 333ns
- On-chip memory
  - PROM: 32K bytes
    μPD78P218ADW : Reprogrammable (suitable for system evaluation)
    μPD78P218ACW, GC: Programmable only once (suitable for small production)
- RAM: 1024 bytes
- QTOP™ microcomputer compatibility

Remarks The QTOP microcomputer is a general term for one-time PROM incorporated single-chip microcomputers offered by NEC, which cover totally program writing, marking, screening and verification.

ORDERING INFORMATION

Ordering Code	Package	On-Chip ROM
μPD78P218ACW	64-pin plastic shrink DIP (750 mil)	One-time PROM
μPD78P218AGC-AB8	64-pin plastic QFP (□ 14 mm)	One-time PROM
μPD78P218ADW	64-pin ceramic shrink DIP (CERDIP) (with window) (750mil)	EPROM

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.
In this manual, PROM indicates the features common to the one-time PROM products and the EPROM.

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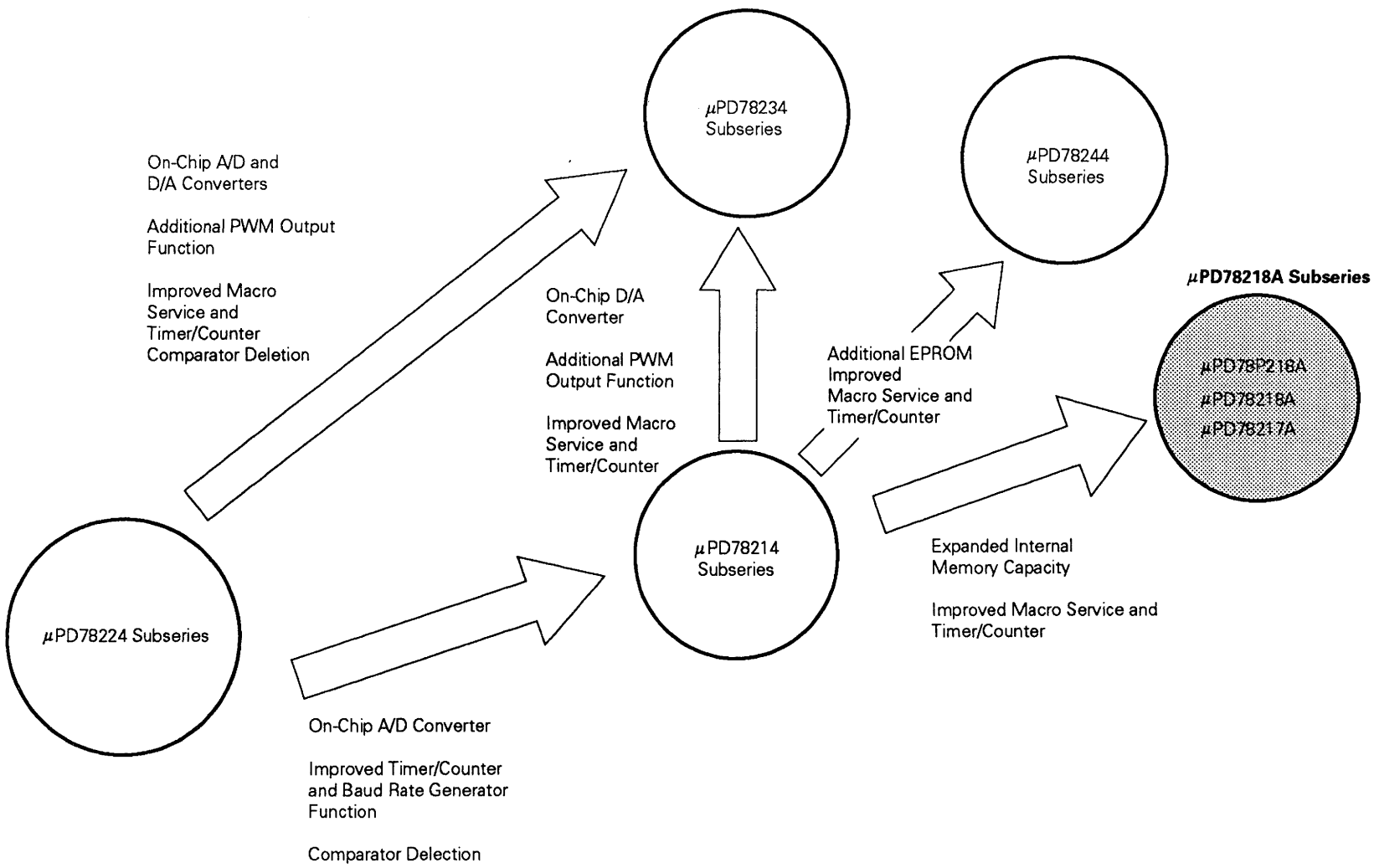
Date Published May 1994 P
Printed in Japan

The mark ★ shows major revised points.

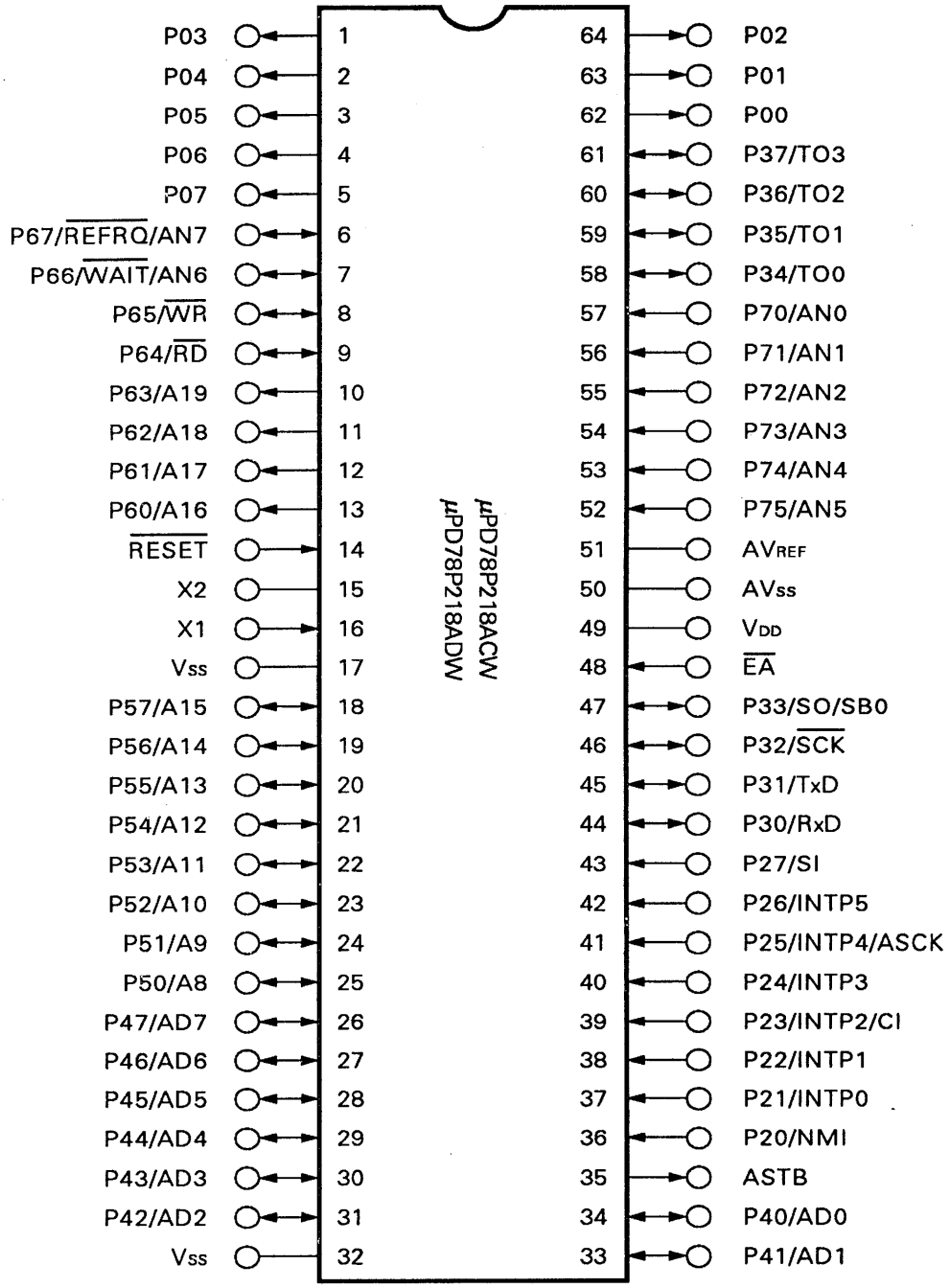
78K/II Product Developments



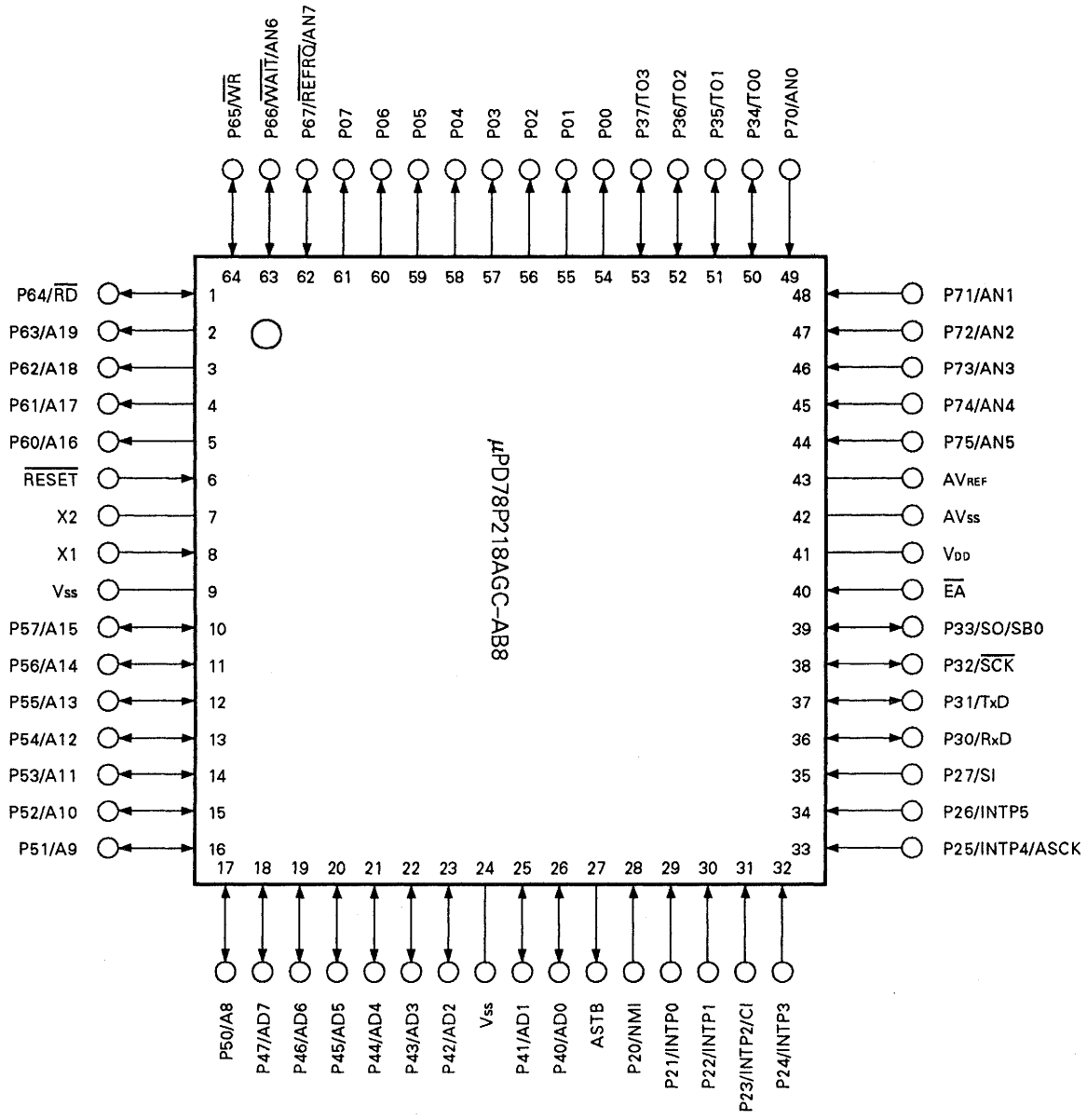
PIN CONFIGURATION (TOP VIEW)

(1) Normal operating modes

(a) 64-pin plastic shrink DIP and 64-pin ceramic shrink DIP (CERDIP) (with window)

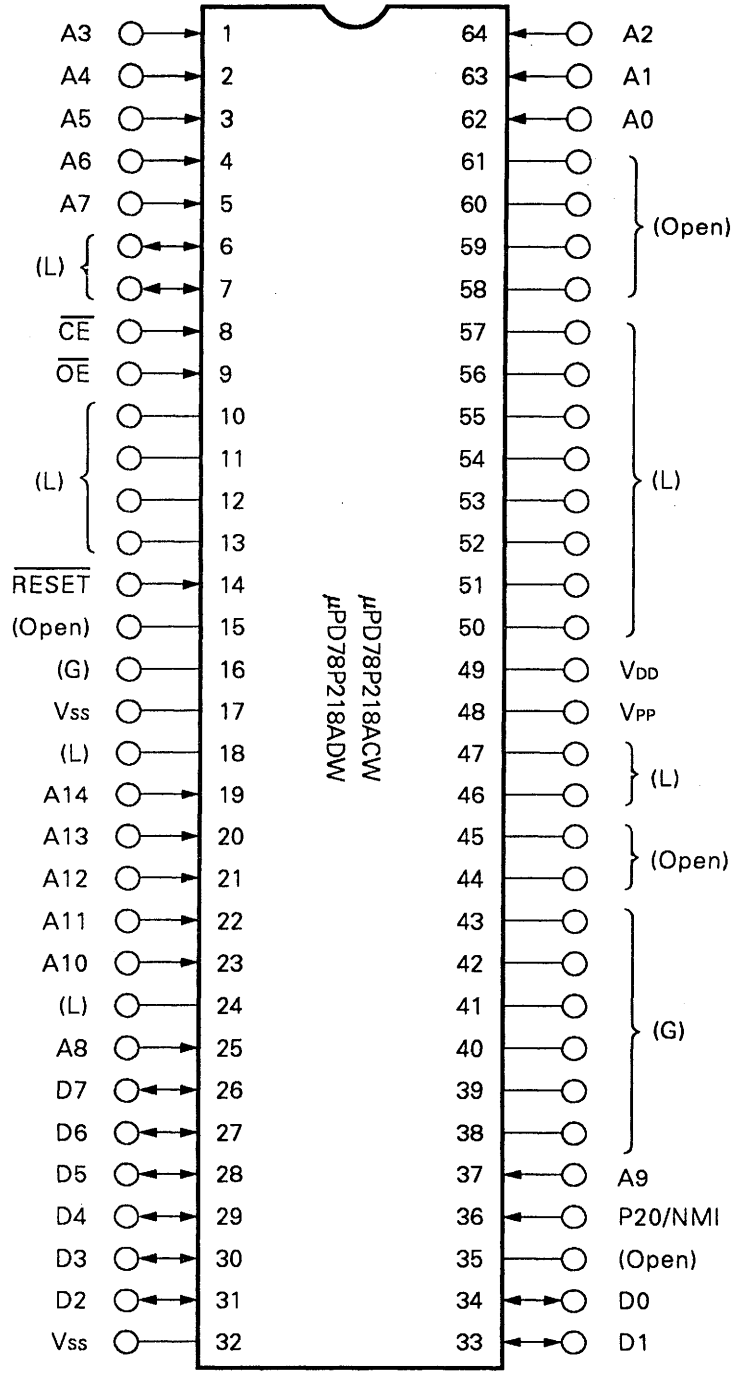


(b) 64-pin plastic QFP



(2) PROM programming mode (P20/NMI = 12.5 V, $\overline{\text{RESET}}$ = L)

(a) 64-pin plastic shrink DIP and 64-pin ceramic shrink DIP (CERDIP) (with window)



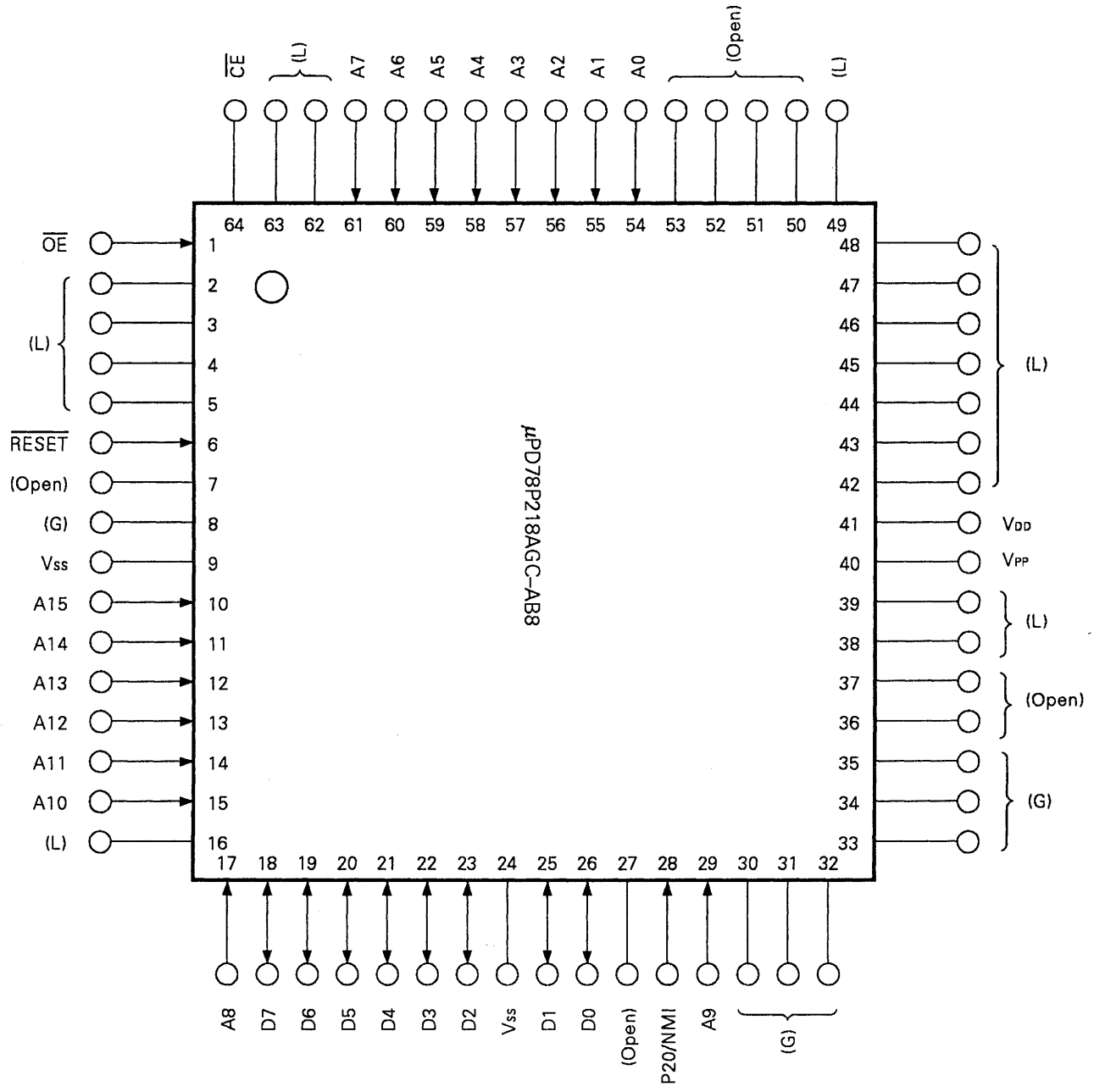
Note **Processing for pins which are not used in the PROM programming mode is indicated in parentheses.**

L : Connect these pins independently to Vss via a 10 kΩ resistor. ★

G : Connect these pins to Vss.

Open : Leave open.

(b) 64-pin plastic QFP



Note **Processing for pins which are not used in the PROM programming mode is indicated in parentheses.**

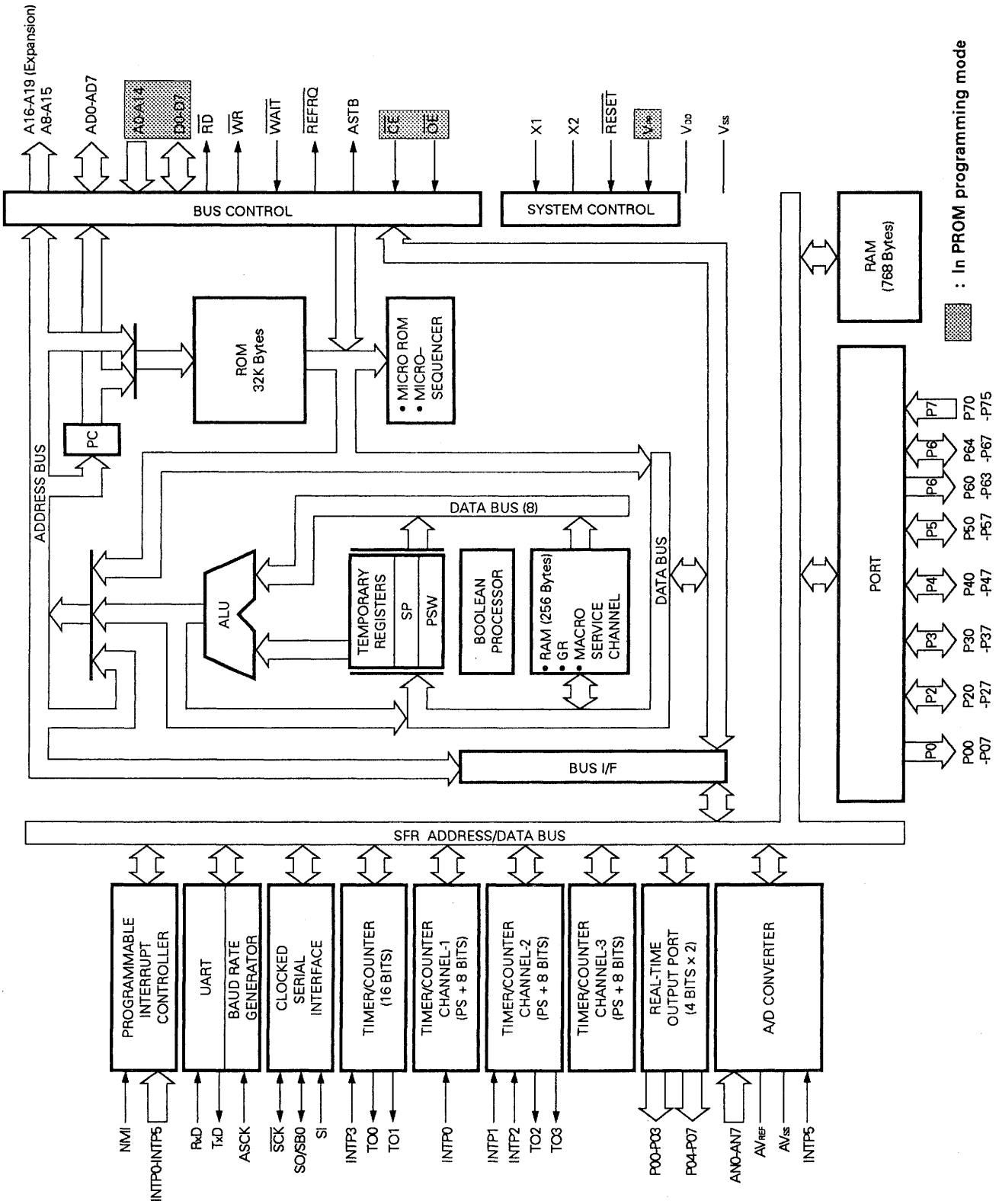
★ **L : Connect these pins independently to Vss via a 10 kΩ resistor.**

G : Connect these pins to Vss.

Open : Leave open.

P00 to P07	:	Port 0
P20 to P27	:	Port 2
P30 to P37	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P60 to P67	:	Port 6
P70 to P75	:	Port 7
TO0 to TO3	:	Timer Output
CI	:	Clock Input
R_xD	:	Receive Data
T_xD	:	Transmit Data
$\overline{SCK}$	:	Serial Clock
ASCK	:	Asynchronous Serial Clock
SB0	:	Serial Bus
SI	:	Serial Input
SO	:	Serial Output
NMI	:	Non-maskable Interrupt
INTP0 to INTP5	:	Interrupt From Peripherals
AD0 to AD7	:	Address/Data Bus
A8 to A19	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
$\overline{REFRQ}$	:	Refresh Request
$\overline{RESET}$	:	Reset
X1, X2	:	Crystal
$\overline{EA}$	:	External Access
AN0 to AN7	:	Analog Input
AV_{REF}	:	Reference Voltage
AVss	:	Analog Ground
V_{DD}	:	Power Supply
Vss	:	Ground
$\overline{CE}$	:	Chip Enable
$\overline{OE}$	:	Output Enable
V_{PP}	:	Programming Power Supply

INTERNAL BLOCK DIAGRAM



CONTENTS

Series		μPD78218A Subseries			μPD78214 Subseries			
Product Name		μPD78217A	μPD78218A	**μPD78P218A**	μPD78212	μPD78213	μPD78214	μPD78P214
Minimum instruction cycle (at 12 MHz operation)		500 ns	333 ns		333 ns	500 ns	333 ns	
PUSH PSW instruction execution time (number of clocks)		When the stack area is internal dual-port RAM: 6 Other than above: 8			When the stack area is internal dual-port RAM: 5 or 7 Other than above: 7 or 9			
Supply voltage range		+5 V ± 10%		+5 V ± 0.3 V	+5 V ± 10 %			
On-chip memory	ROM	ROM-less	32K bytes (Mask ROM)	32K bytes (PROM)	8K bytes (Mask ROM)	ROM-less	16K bytes (Mask ROM)	16K bytes (PROM)
	RAM	1024 bytes			384 bytes	512 bytes		
Number of I/O pins		36	54		54	36	54	
AV_{REF} input voltage		3.6 V to V_{DD}			3.4 V to V_{DD}			
Restrictions concerning input voltage		0V to AV_{REF} pin voltage is applied to pins relevant to A/D conversion during A/D conversion only			Constant 0V to AV_{REF} pin voltage is applied to pins selected by ADM register ANI0 to ANI2 bits only.			
16-bit timer/counter one-shot pulse output		Yes			No			
Macro service counter bit width		8-/16-bit select capability (except type A)			only 8-bit			
Macro service type C MPD, MPT increment		16-bit increment			Only low-order 8-bits increment (High-order 8 bits are unchanged.)			
Macro service execution time		Varies depending on mode. Please refer to users manual with each product.						
Restrictions in data transfer from memory of macro service type A to SFR		Generates when address range of transfer source buffer (memory) is 0FED0H to 0FEDFH			Generates when transfer data is in the range of D0H to DFH.			
Stabilization time for oscillation when STOP mode is released		Dedicated counter 15 bits or $\overline{NMI}$ active pulse width + dedicated counter 16 bits			$\overline{NMI}$ active pulse width + dedicated counter 16 bits			
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (□14 mm) • 64-pin ceramic shrink DIP (CERDIP) (with window) (750mil): μPD78P218A only			• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QUIP: Except μPD78212 • 68-pin plastic QFJ: Except μPD78212 • 64-pin plastic QFP (□ 14 mm) • 74-pin plastic QFP (□ 20 mm) • 64-pin ceramic shrink DIP (CERDIP) (with window) (750mil): μPD78P214 only			

2. PIN FUNCTIONS

2.1 NORMAL OPERATING MODE

(1) Ports

Pin Name	I/O	Dual-Function Pin	Function
P00 to P07	Output	——	Port 0 (P0): Use enabled as a real-time output port (4 bits × 2) Transistor drive possible
P20	Input	NMI	Port 2 (P2): P20 is disabled for use as a general-purpose port (nonmaskable interrupt). However, input level can be checked in the interrupt routine. Specification of the internal pull-up resistor for P22 to P27 by software in 6-bit units is possible.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP/ASCK	
P26		INTP5	
P27		SI	
P30	Input/output	RxD	Port 3 (P3): Input/output specifiable bit-wise. Concerning input mode pins, specification of the internal pull-up resistor by software at one time is possible.
P31		TxD	
P32		$\overline{SCK}$	
P33		SO/SB0	
P34 to P37		TO0 to TO3	
P40 to P47	Input/output	AD0 to AD7	Port 4 (P4): Input/output specifiable in 8-bit units at one time. Specification of the internal pull-up resistor by software in 8-bit units at one time is possible. LED direct drive is possible.
P50 to P57	Input/output	A8 to A15	Port 5 (P5): Input/output specifiable bit-wise. Concerning input mode pins, specification of the internal pull-up resistor by software at one time is possible. LED direct drive capability.
P60 to P63	Output	A16 to A19	Port 6 (P6): Input/output specifiable bit-wise for P64 to P67. Concerning input mode pins, specification of the internal pull-up resistor by software at one time is possible for P64 to P67.
P64	Input/output	$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$/AN6	
P67		$\overline{REFRQ}$/AN7	
P70 to P75	Input	AN0 to AN5	Port 7 (P7)

(2) Other Than Ports

Pin Name	I/O	Function	Dual-Function Pin
TO0 to TO3	Output	Timer output	P34 to P37
CI	Input	Count clock input to 8-bit timer/counter 2	P23 /INTP2
RxD	Input	Serial data input (UART)	P30
TxD	Output	Serial data output (UART)	P31
ASCK	Input	Baud rate clock input (UART)	P25/INTP4
SB0	Input /output	Serial data input/output (SBI)	P33/SO
SI	Input	Serial data input (3-wire serial I/O)	P27
SO	Output	Serial data output (3-wire serial I/O)	P33/SB0
$\overline{SLK}$	Input /output	Serial clock input/output (SBI, 3-wire serial I/O)	P32
NMI	Input	External interrupt request	P20
INTP0			P21
INTP1			P22
INTP2			P23/CI
INTP3			P24
INTP4			P25/ASCK
INTP5			P26
AD0 to AD7	Input /output	Time multiplexing address/data bus (external memory connection)	P40 to P47
A8 to A15	Output	Higher address bus (external memory connection)	P50 to P57
A16 to A19	Output	Expanded higher adderss (external memory connection)	P60 to P63
$\overline{RD}$	Output	Read strobe for external memory	P64
$\overline{WR}$	Output	Write strobe into external memory	P65
$\overline{WAIT}$	Input	Wait insert	P66/AN6
ASTB	Output	Latch timing output of time-multiplexing addresses (A0 to A7) (in external memory accessed)	—
$\overline{REFRQ}$	Output	Refresh pulse output to external pseudo-static memory	P67/AN7
$\overline{RESET}$	Input	Chip reset	—
X1	Input	Crystal connection for system clock oscillation (clock input to X1 enabled)	—
X2	—		
$\overline{EA}$	Input	ROM-less operation specification (external access in the same space as internal ROM).	—
AN0 to AN5	Input	Analog voltage input for A/D converter	P70 to P75
AN6, AN7			P66/$\overline{WAIT}$, P67/$\overline{REFRQ}$
AV_{REF}	—	Reference voltage application for A/D converter	
AV_{SS}		GND for A/D converter	—
V_{DD}		Positive power supply	
V_{SS}		GND	

2.2 PROM PROGRAMMING MODE (P20/NMI = +12.5 V, $\overline{\text{RESET}}$ = L)

Pin Name	Input/Output	Function
P20/NMI	Input	PROM programming mode
$\overline{\text{RESET}}$		
A0 to A14		Address bus
D0 to D7	Input/output	Data bus
$\overline{\text{CE}}$	Input	PROM enable input
$\overline{\text{OE}}$		Read strobe for PROM
V_{PP}	———	Write power supply
V_{DD}		Positive power supply
V_{SS}		GND

3. PROGRAMMING

The on-chip program memory of the μPD78P218A is a 32768×8-bit electrically programmable PROM. For PROM programming mode is set using the NMI and $\overline{\text{RESET}}$ pins.

The programming characteristics are compatible with the μPD27C256A.

3.1 OPERATING MODE

When +6 V and +12.5 V are applied to V_{DD} pin and V_{PP} pin, respectively, the μPD78P218A is set to the program-write/verify mode. This mode can be reset to the operating mode described in Table 3-1 by setting $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins.

In the read mode, the μPD78P218A can read the PROM contents.

Table 3-1 PROM Programming Operating Mode

Mode \ Pin	NMI	$\overline{\text{RESET}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{DD}	D0 to D7
Program write	+ 12.5 V	L	L	H	+ 12.5 V	+ 6 V	Data input
Program verify			H	L			Data output
Program inhibit			H	H			High-impedance
Read			L	L	+ 5 V	+ 5 V	Data output
Output disable			L	H			High-impedance
Standby			H	L/H			High-impedance

Note When V_{PP} is set to +12.5 V and V_{DD} is set to +6 V, it is inhibited to set both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ to L.

3.2 PROM WRITE PROCEDURE

PROM write can be executed at high speeds using the following procedure:

(1) Fix the $\overline{\text{RESET}}$ pin to the low level. Apply +12.5 V to the NMI pin. Treat all other unused pins as shown in **PIN CONFIGURATION (2)**.
(2) Apply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
(3) Supply the initial address.
(4) Supply write data.
(5) Supply a 1 ms program pulse (active low) to the $\overline{\text{CE}}$ pin.
(6) Set the verify mode. If data has been written, procedure to step (8). If data has not been written, repeat steps (4) to (6). If data cannot yet be written after repeating the three steps 25 times, proceed to step (7).
(7) Stop carrying out the write operation assuming that the device is defective.
(8) Supply write data and then supply (number of repetitions of steps (4) to (6): X) × 3ms program pulses (additional write).
(9) Increment the address.
(10) Repeat steps (4) to (9) up to the final address.

The timings in steps (2) to (8) are shown in Fig. 3-1.

Fig. 3-1 PROM Write/Verify Timing

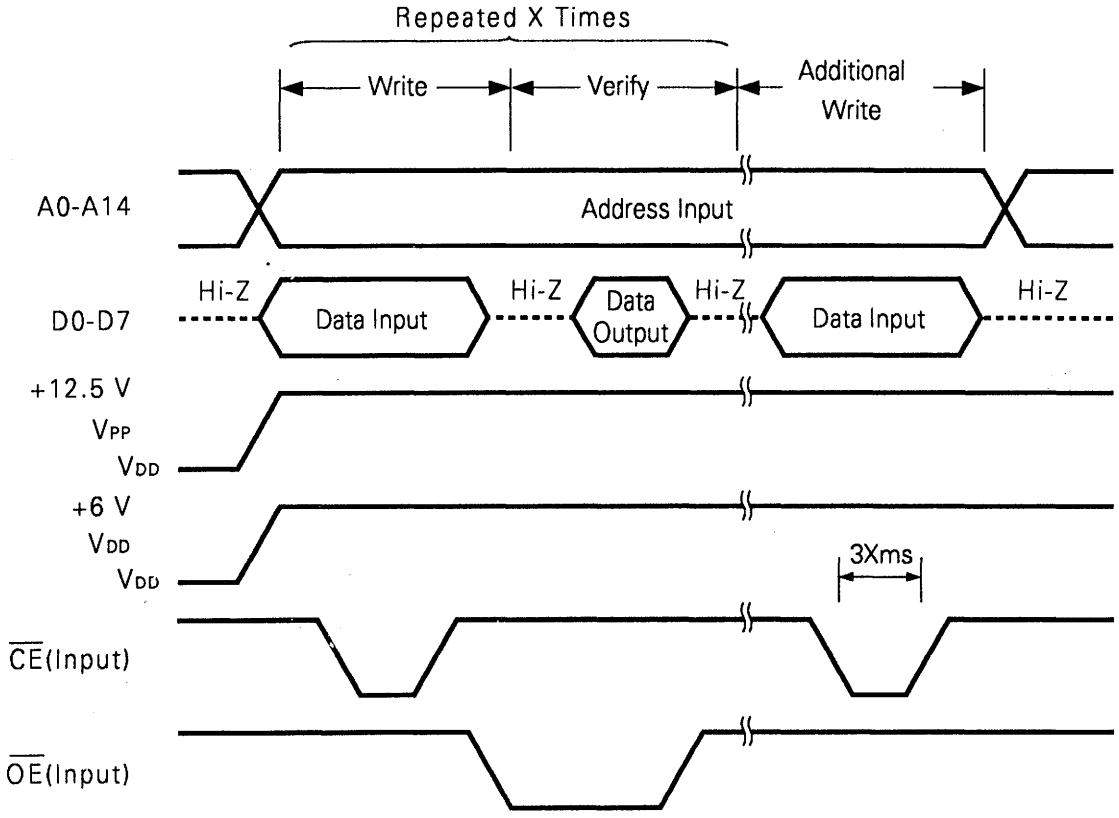
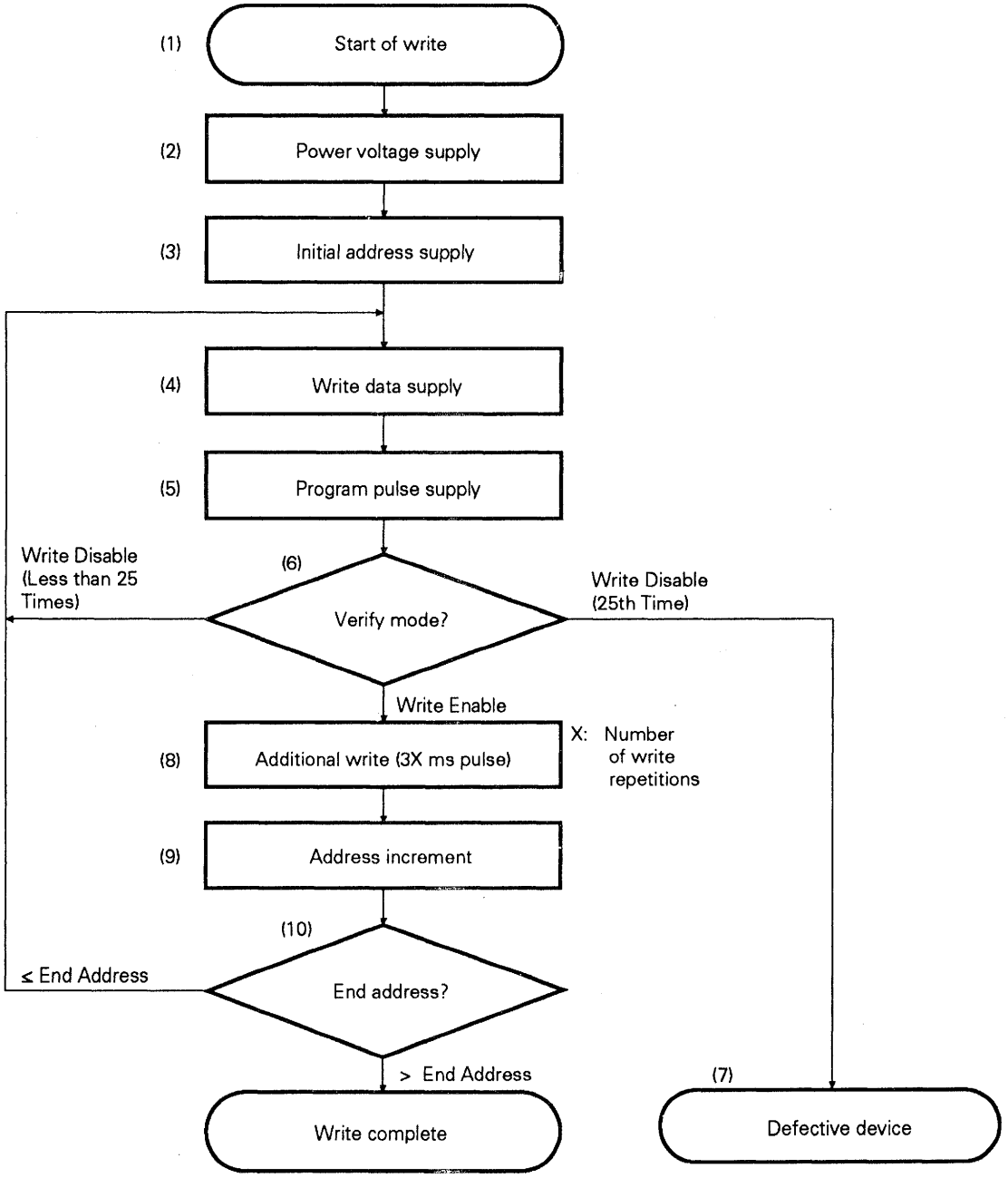


Fig. 3-2 Write Operation Flowchart



3.3 PROM READ PROCEDURE

PROM contents can be read into the external data bus (D0 to D7) using the following procedure:

(1) Fix the $\overline{\text{RESET}}$ pin to the low level. Apply +12.5 V to the NMI pin. Treat all other unused pins as shown in **PIN CONFIGURATION (2)**.

(2) Apply +5 V to the V_{DD} and V_{PP} pins.

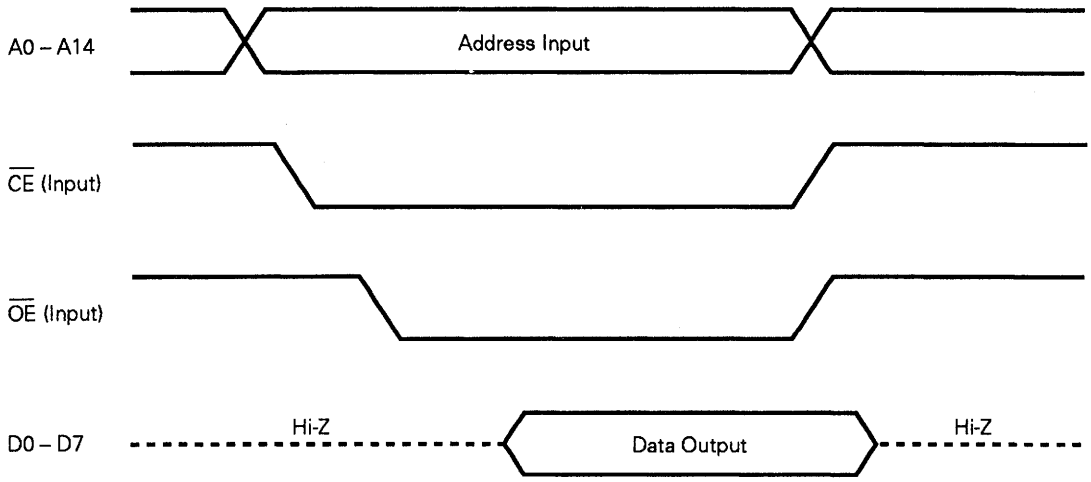
(3) Input the address of the data to be read to the A0 to A14 pins.

(4) Set the read mode.

(5) Output data to the D0 to D7 pins.

The timings in steps (2) to (5) are shown in Fig.3-3.

Fig. 3-3 PROM Read Timings



4. ERASURE CHARACTERISTICS (μPD78P218ADW ONLY)

The μPD78P218ADW can erase the programmed data content (FFH) by applying light having wavelengths of less than about 400 nm.

To erase the μPD78P218ADW program memory contents, normally apply ultraviolet rays having a wavelength of 254 nm. The total radiation required to erase the μPD78P218ADW contents completely is a minimum of 15 W•s /cm² (ultraviolet strength × erasure time). The erasure time is approximately 15 to 20 minutes (when a 12000 μW/cm² ultraviolet lamp is used). The erase time may possible become longer due to deterioration in the performance of the ultraviolet lamp or fouling of the package window.

For the erasure operation, place the μPD78P218ADW within 2.5 cm from the ultraviolet lamp. Use the ultraviolet lamp with the filter removed.

5. ERASURE WINDOW SEALING (μPD78P218ADW ONLY)

Except when erasing EPROM contents, apply a protective seal to the erasure window. This is important to prevent the EPROM contents from being inadvertently erased due to light other than the erasure lamp or the internal circuits other than the EPROM form error due to light.

6. SCREENING OF ONE-TIME PROM PRODUCTS

By reason of their structure, one-time PROM products (μPD78P218ACW and μPD78P218AGC-AB8) cannot be fully tested by NEC prior to shipment. After the necessary data has been written, it is recommended that screening be performed for PROM verification after high-temperature storage under the following conditions.

Storage Temperature	Storage Period
125 °C	24 hrs.

Under the generic name "QTOP microcomputer", NEC offers a charged service covering one-time PROM writing, marking, screening and verifications. Please consult our sales representative for details.

7. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = +25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.5 to +7.0	V
	AV_{REF}		−0.5 to V_{DD} +0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input voltage	V_{I1}		−0.5 to V_{DD} +0.5	V
	V_{I2}	*1	−0.5 to AV_{REF} +0.5	V
	V_{I3}	*2	−0.5 to +13.5	V
Output voltage	V_O		−0.5 to V_{DD} +0.5	V
Output current low	I_{OL}	1 pin	15	mA
		All output pins total	100	mA
Output current high	I_{OH}	1 pin	−10	mA
		All output pins total	−50	mA
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

* 1. Those of pins P70/AN0 to P75/AN5, P66/$\overline{WAIT}$/AN6, P67/$\overline{REFRQ}$/AN7 which are used as A/D converter input pins.

2. Pins P20/NMI, $\overline{EA}$/V_{PP} and P21/INTP0/A9 in PROM programming mode.

Note **Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. The absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.** ★

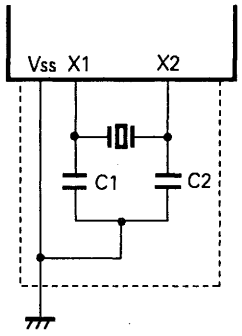
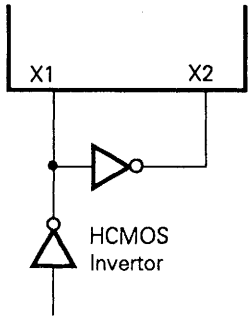
OPERATING CONDITIONS

CLOCK FREQUENCY	OPERATING TEMPERATURE (T_{opt})	SUPPLY VOLTAGE (V_{DD})
4 MHz ≤ fxx ≤ 12 MHz	−40 to +85 °C	+5.0 ± 0.3 V

CAPACITANCE (Ta = +25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	f = 1 MHz unmeasured pins returned to 0 V.			20	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

OSCILLATOR CHARACTERISTICS (Ta = −40 to +85 °C, V_{DD} = +5.0 ±0.3 V, V_{SS} = 0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	MIN.	MAX.	UNIT
Ceramic resonator or crystal resonator		Oscillator frequency (f_{XX})	4	12	MHz
External clock		X1 input frequency (f_X)	4	12	MHz
		X1 input rising/falling time (t_{XR}, t_{XF})	0	30	ns
		X1 input high/low level width (t_{WXH}, t_{WXL})	30	130	ns

Note When the system clock oscillator is used, the following points should be noted concerning wiring in the section enclosed by dots, in order to prevent the effects of wiring capacitance, etc.

- **Keep the wiring as short as possible.**
- **Do not cross any other signal lines.**
- **Keep away from lines carrying a high fluctuating current.**
- **Ensure that oscillator capacitor connection points are always at the same potential as V_{SS}. Do not ground in a ground pattern in which a high current flows.**
- **Do not take a signal from the oscillator.**

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = +5.0 ±0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage low	V_{IL}		0		0.8	V
Input voltage high	V_{IH1}	Pins except for *1 and *2	2.2		V_{DD}	V
	V_{IH2}	Pin of *1	2.2		AV_{REF}	V
	V_{IH3}	Pin of *2	0.8V_{DD}		V_{DD}	V
Output voltage low	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
	V_{OL2}	I_{OL} = 8.0 mA *3			1.0	V
Output voltage high	V_{OH1}	I_{OH} = –1.0 mA	V_{DD}–1.0			V
	V_{OH2}	I_{OH} = –100 μA	V_{DD}–0.5			V
	V_{OH3}	I_{OH} = –5.0 mA *4	2.0			V
X1 input current low	I_{IL}	0 V ≤ V_I ≤ V_{IL}			–100	μA
X1 input current high	I_{IH}	V_{IH3} ≤ V_I ≤ V_{DD}			100	μA
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD}				
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				
AV_{REF} current	AI_{REF}	Operating mode fxx = 12 MHz		1.5	5.0	mA
V_{DD} supply current	I_{DD1}	Operating mode fxx = 12 MHz		20	40	mA
	I_{DD2}	HALT mode fxx = 12 MHz		7	20	mA
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.3	V
Data retention current	I_{DDDR}	STOP mode V_{DDDR} = 2.5 V		2	20	μA
		STOP mode V_{DDDR} = +5.0 ±0.3 V		5	50	μA
Pull-up resistor	R_L	V_I = 0 V	15	40	80	kΩ

* 1. Those of pins P70/AN0 to P75/AN5, P66/$\overline{WAIT}$/AN6, P67/$\overline{REFRQ}$/AN7 which are used as A/D converter input pins.

2. X1, X2, $\overline{RESET}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{SCK}$, P33/SO/SB0, $\overline{EA}$ pins
3. P40/AD0 to P47/AD7, P50/A8 to P57/A15 pins
4. P00 to P07 pins

AC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = +5.0 ±0.3 V, V_{SS} = 0 V)
Read/Write Operation (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
X1 input clock cycle time	t_{CYX}		82	250	ns
Address setup time (to ASTB↓)	t_{SAST}		52		ns
Address hold time (from ASTB↓) *	t_{HSTA} •		25		ns
Address hold time (from $\overline{RD}$↑)	t_{HRA}		30		ns
Address hold time (from $\overline{WR}$↑)	t_{HWA}		30		ns
$\overline{RD}$↓ delay time from address	t_{DAR} •		129		ns
Address float time (from $\overline{RD}$↓)	t_{FAR} •		11		ns
Data input time from address	t_{DAID} •	No. of waits = 0		228	ns
Data input time from ASTB↓	t_{DSTID} •	No. of waits = 0		181	ns
Data input time from $\overline{RD}$↓	t_{DRID} •	No. of waits = 0		100	ns
$\overline{RD}$↓ delay time from ASTB↓	t_{DSTR} •		52		ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}		0		ns
Address active time from $\overline{RD}$↑	t_{DRA} •		124		ns
ASTB↑ delay time from $\overline{RD}$↑	t_{DRST} •		124		ns
$\overline{RD}$ low-level width	t_{WRL} •	No. of waits = 0	124		ns
ASTB high-level width	t_{WSTH} •		52		ns
$\overline{WR}$↓ delay time from address	t_{DAW} •		129		ns
Data output time from ASTB↓	t_{DSTOD} •			142	ns
Data output time from $\overline{WR}$↓	t_{DWOD}			60	ns
$\overline{WR}$↓ delay time from ASTB↓	t_{DSTW1} •	In refresh disabled	52		ns
	t_{DSTW2} •	In refresh enabled	129		ns
Data setup time (to $\overline{WR}$↑)	t_{SODWR} •	No. of waits = 0	146		ns
Data setup time (to $\overline{WR}$↓)	t_{SODWF} •	In refresh enabled	22		ns
Data hold time (from $\overline{WR}$↑) *	t_{HWOD}		20		ns
ASTB↑ delay time from $\overline{WR}$↑	t_{DWST} •		42		ns
$\overline{WR}$ low-level width	t_{WWL1} •	In refresh disabled no. of waits = 0	196		ns
	t_{WWL2} •	In refresh enabled no. of waits = 0	114		ns
$\overline{WAIT}$↓ input time from address	t_{DAWT} •			146	ns
$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT} •			84	ns

* The hold time includes the time to hold the V_{OH} and V_{OL} under the load conditions of C_L = 100 pF and R_L = 2kΩ.

Remarks 1. The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".
2. For a parameter with a dot (•) in the SYMBOL column, refer to "t_{CYX} **DEPENDENT BUS TIMING**

Read/Write Operation (2/2)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
$\overline{WAIT}$ hold time from ASTB↓		$t_{HSTWT\bullet}$	No. of external waits = 1	174		ns
$\overline{WAIT}$↑ delay time from ASTB↓		$t_{DSTWTH\bullet}$	No. of external waits = 1		273	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓		$t_{DRWTL\bullet}$			22	ns
$\overline{WAIT}$ hold time from $\overline{RD}$↓		$t_{HRWT\bullet}$	No. of external waits = 1	87		ns
$\overline{WAIT}$↑ delay time from $\overline{RD}$↓		$t_{DRWTH\bullet}$	No. of external waits = 1		186	ns
Data input time from $\overline{WAIT}$↑		$t_{DWTID\bullet}$			62	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑		$t_{DWTW\bullet}$		154		ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑		$t_{DWTR\bullet}$		72		ns
$\overline{WAIT}$ input time from $\overline{WR}$↓ (At refresh disabled)		$t_{DWWTL\bullet}$			22	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	Refresh disabled	$t_{HWWT1\bullet}$	No. of external waits = 1	87		ns
	Refresh enabled	$t_{HWWT2\bullet}$	No. of external waits = 1	5		ns
$\overline{WAIT}$↑ delay time from $\overline{WR}$↓	Refresh disabled	$t_{DWWTH1\bullet}$	No. of external waits = 1		186	ns
	Refresh enabled	$t_{DWWTH2\bullet}$	No. of external waits = 1		104	ns
$\overline{REFRQ}$↓ delay time from $\overline{RD}$↑		$t_{DRRFQ\bullet}$		154		ns
$\overline{REFRQ}$↓ delay time from $\overline{WR}$↑		$t_{DWRFQ\bullet}$		72		ns
$\overline{REFRQ}$ low-level width		$t_{WRFQL\bullet}$		120		ns
ASTB↑ delay time from $\overline{REFRQ}$↑		$t_{DRFQST\bullet}$		280		ns

Remarks 1. The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".

2. For a parameter with a dot (•) in the SYMBOL column, refer to "t_{CYX} **DEPENDENT BUS TIMING DEFINITION**" as well.

Serial Operation

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		μs
		Output	Internal divided by 16	1.3		μs
			Internal divided by 64	5.3		μs
Serial clock low-level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internal divided by 16	556		ns
			Internal divided by 64	2.5		μs
Serial clock high-level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internal divided by 16	556		ns
			Internal divided by 64	2.5		μs
SI, SB0 setup time (to $\overline{SCK}\uparrow$)	t_{SSSK}			150		ns
SI, SB0 hold time (from $\overline{SCK}\uparrow$)	t_{HSSK}			400		ns
SO/SB0 output delay time (from $\overline{SCK}\downarrow$)	t_{DSBSK1}	CMOS push-pull output (3-wire serial I/O mode)		0	300	ns
	t_{DSBSK2}	Open-drain output (SBI mode), R_L = 1 kΩ		0	800	ns
SB0 high hold time (from $\overline{SCK}\uparrow$)	t_{HSBSK}	SBI mode		4		t_{CYX}
SB0 low setup time (to $\overline{SCK}\downarrow$)	t_{SSBSK}			4		t_{CYX}
SB0 low-level width	t_{WSBL}			4		t_{CYX}
SB0 high-level width	t_{WSBH}			4		t_{CYX}

Remarks The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".

Other Operations

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0 to INTP5 low-level width	t_{WITL}		24		t_{CYX}
INTP0 to INTP5 high-level width	t_{WITH}		24		t_{CYX}
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		10		μs

External Clock Timing

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
X1 input low-level width	t_{WXL}		30	130	ns
X1 input high-level width	t_{WXH}		30	130	ns
X1 input rise time	t_{XR}		0	30	ns
X1 input fall time	t_{XF}		0	30	ns
X1 input clock cycle time	t_{CYX}		82	250	ns

A/D CONVERTER CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +5.0 ±0.3 V, V_{SS} = AV_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution			8			bit
Overall error*		4.0 V ≤ AV_{REF} ≤ V_{DD} Ta = −10 to +70°C			0.4	%
		3.6 V ≤ AV_{REF} ≤ V_{DD} Ta = −10 to +70°C			0.8	%
		4.0 V ≤ AV_{REF} ≤ V_{DD}			0.8	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	82 ns ≤ t_{CYX} < 125 ns (The FR bit of ADM is to be "0")	360			t_{CYX}
		125 ns ≤ t_{CYX} ≤ 250 ns (The FR bit of ADM is to be "1")	240			t_{CYX}
Sampling time	t_{SAMP}	82 ns ≤ t_{CYX} < 125 ns (The FR bit of ADM is to be "0")	72			t_{CYX}
		125 ns ≤ t_{CYX} ≤ 250 ns (The FR bit of ADM is to be "1")	48			t_{CYX}
Analog input voltage	V_{IAN}		−0.3		AV_{REF} +0.3	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF}		3.6		V_{DD}	V
AV_{REF} current	AI_{REF}	f_{XX} = 12 MHz		1.5	5.0	mA
		STOP mode		0.2	1.5	mA

* Quantization error is not included. Represented by the ratio to full-scale value.

t_{CYX} DEPENDENT BUS TIMING DEFINITION (1/2)

PARAMETER	SYMBOL	FORMULA	MIN./MAX.	12 MHz	UNIT
X1 input clock cycle time	t_{CYX}		MIN.	82	ns
Address setup time (to ASTB↓)	t_{SAST}	t_{CYX} – 30	MIN.	52	ns
$\overline{RD}$↓ delay time from address	t_{DAR}	2t_{CYX} – 35	MIN.	129	ns
Address float time (from $\overline{RD}$↓)	t_{FAR}	t_{CYX}/2 – 30	MIN.	11	ns
Data input time from address	t_{DAID}	(4 + 2n) t_{CYX} – 100	MAX.	228 *	ns
Data input time from ASTB↓	t_{DSTID}	(3 + 2n) t_{CYX} – 65	MAX.	181 *	ns
Data input time from $\overline{RD}$↓	t_{DRID}	(2 + 2n) t_{CYX} – 64	MAX.	100 *	ns
$\overline{RD}$↓ delay time from ASTB↓	t_{DSTR}	t_{CYX} – 30	MIN.	52	ns
Address active time from $\overline{RD}$↑	t_{DRA}	2t_{CYX} – 40	MIN.	124	ns
ASTB↑ delay time from $\overline{RD}$↑	t_{DRST}	2t_{CYX} – 40	MIN.	124	ns
$\overline{RD}$ low-level width	t_{WRL}	(2 + 2n) t_{CYX} – 40	MIN.	124 *	ns
ASTB high-level width	t_{WSTH}	t_{CYX} – 30	MIN.	52	ns
$\overline{WR}$↓ delay time from address	t_{DAW}	2t_{CYX} – 35	MIN.	129	ns
Data output time from ASTB↓	t_{DSTOD}	t_{CYX} + 60	MAX.	142	ns
$\overline{WR}$↓ delay time from ASTB↓	t_{DSTW1}	t_{CYX} – 30 (In refresh disabled)	MIN.	52	ns
	t_{DSTW2}	2t_{CYX} – 35 (In refresh enabled)	MIN.	129	ns
Data setup time (to $\overline{WR}$↑)	t_{SODWR}	(3 + 2n) t_{CYX} – 100	MIN.	146 *	ns
Data setup time (to $\overline{WR}$↓)	t_{SODWF}	t_{CYX} – 60 (In refresh enabled)	MIN.	22	ns
ASTB↑ delay time from $\overline{WR}$↑	t_{DWST}	t_{CYX} – 40	MIN.	42	ns
$\overline{WR}$ low-level width	t_{WWL1}	(3 + 2n) t_{CYX} – 50 (In refresh disabled)	MIN.	196 *	ns
	t_{WWL2}	(2 + 2n) t_{CYX} – 50 (In refresh enabled)	MIN.	114 *	ns
$\overline{WAIT}$↓ input time from address	t_{DAWT}	3t_{CYX} – 100	MAX.	146	ns
$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT}	2t_{CYX} – 80	MAX.	84	ns

Remarks "n" indicates the number of waits.

* When n = 0

t_{CYX} DEPENDENT BUS TIMING DEFINITION (2/2)

PARAMETER		SYMBOL	FORMULA	MIN./MAX.	12 MHz	UNIT
$\overline{WAIT}$ hold time from ASTB↓		t_{HSTWT}	2Xt_{CYX} + 10	MIN.	174 *	ns
$\overline{WAIT}$↑ delay time from ASTB↓		t_{DSTWTH}	2(1 + X)t_{CYX} – 55	MAX.	273 *	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓		t_{DRWTL}	t_{CYX} – 60	MAX.	22	ns
$\overline{WAIT}$ hold time from $\overline{RD}$↓		t_{HRWT}	(2X – 1)t_{CYX} + 5	MIN.	87 *	ns
$\overline{WAIT}$↑ delay time from $\overline{RD}$↓		t_{DRWTH}	(2X + 1)t_{CYX} – 60	MAX.	186 *	ns
Data input time from $\overline{WAIT}$↑		t_{DWTID}	t_{CYX} – 20	MAX.	62	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑		t_{DWTW}	2t_{CYX} – 10	MIN.	154	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑		t_{DWTR}	t_{CYX} – 10	MIN.	72	ns
$\overline{WAIT}$ input time from $\overline{WR}$↓ (At refresh disabled)		t_{DWWTL}	t_{CYX} – 60	MAX.	22	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	Refresh disabled	t_{HWWT1}	(2X – 1)t_{CYX} + 5	MIN.	87 *	ns
	Refresh enabled	t_{HWWT2}	2(X – 1)t_{CYX} + 5	MIN.	5 *	ns
$\overline{WAIT}$↑ delay time from $\overline{WR}$↓	Refresh disabled	t_{DWWTH1}	(2X + 1)t_{CYX} – 60	MAX.	186 *	ns
	Refresh enabled	t_{DWWTH2}	2Xt_{CYX} – 60	MAX.	104 *	ns
$\overline{REFRQ}$↓ delay time from $\overline{RD}$↑		t_{DRRFQ}	2t_{CYX} – 10	MIN.	154	ns
$\overline{REFRQ}$↓ delay time from $\overline{WR}$↑		t_{DWRFQ}	t_{CYX} – 10	MIN.	72	ns
$\overline{REFRQ}$ low-level width		t_{WRFQL}	2t_{CYX} – 44	MIN.	120	ns
ASTB↑ delay time from $\overline{REFRQ}$↑		t_{DRFQST}	4t_{CYX} – 48	MIN.	280	ns

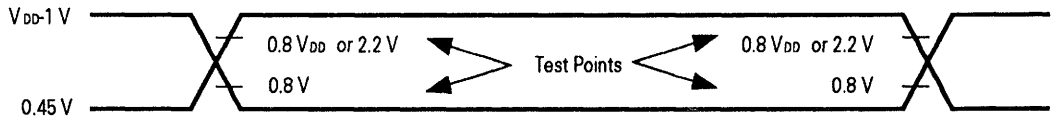
Remarks
1. X: The number of the external wait. (1, 2, ...)
2. $t_{CYX} \cong 82$ ns (f_{XX} = 12 MHz)
3. "n" indicates the number of waits.

DATA RETENTION CHARACTERISTICS (Ta = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.3	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.5 V		2	20	μA
		V_{DDDR} = 5 V ±0.3 V		5	50	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-level input voltage	V_{IL}	Specified pin*	0		0.1 V_{DDDR}	V
High-level input voltage	V_{IH}		0.9 V_{DDDR}		V_{DDDR}	V

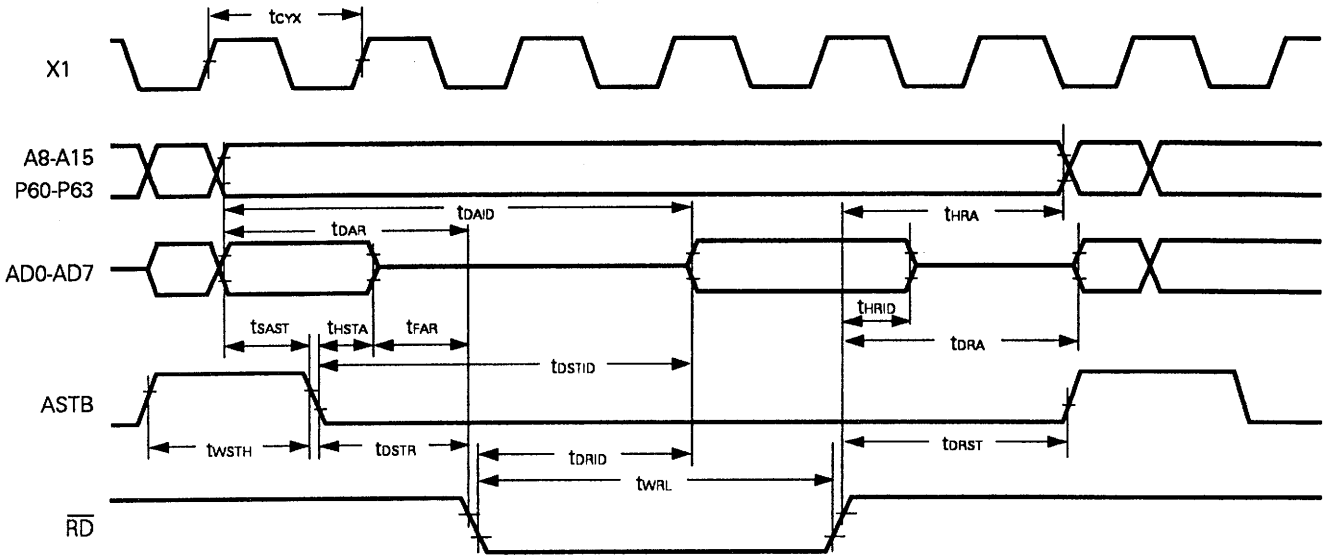
* $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0 and $\overline{\text{EA}}$ pins

AC Timing Test Point

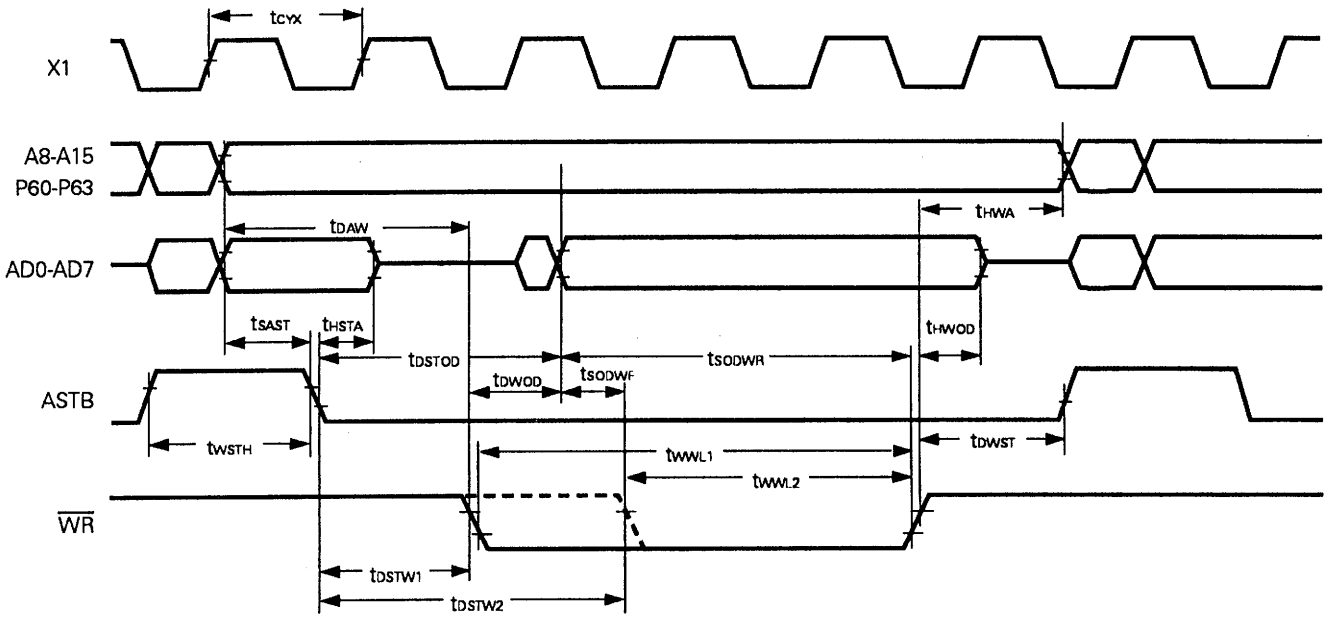


Timing Waveform

Read operation

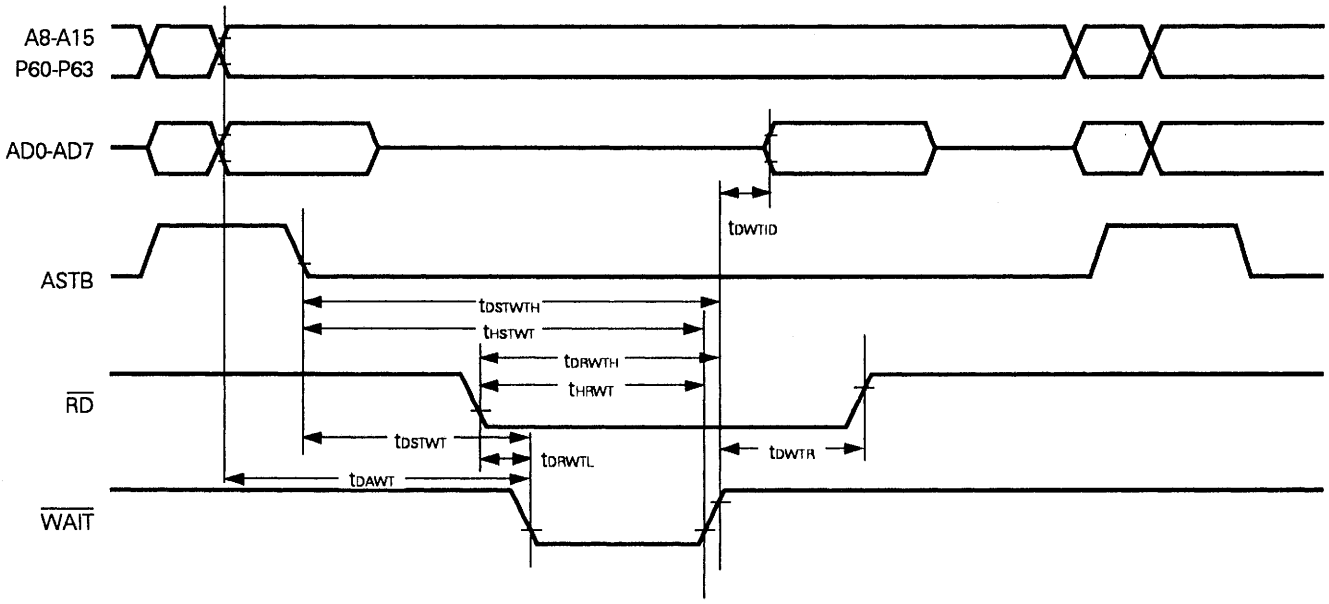


Write operation

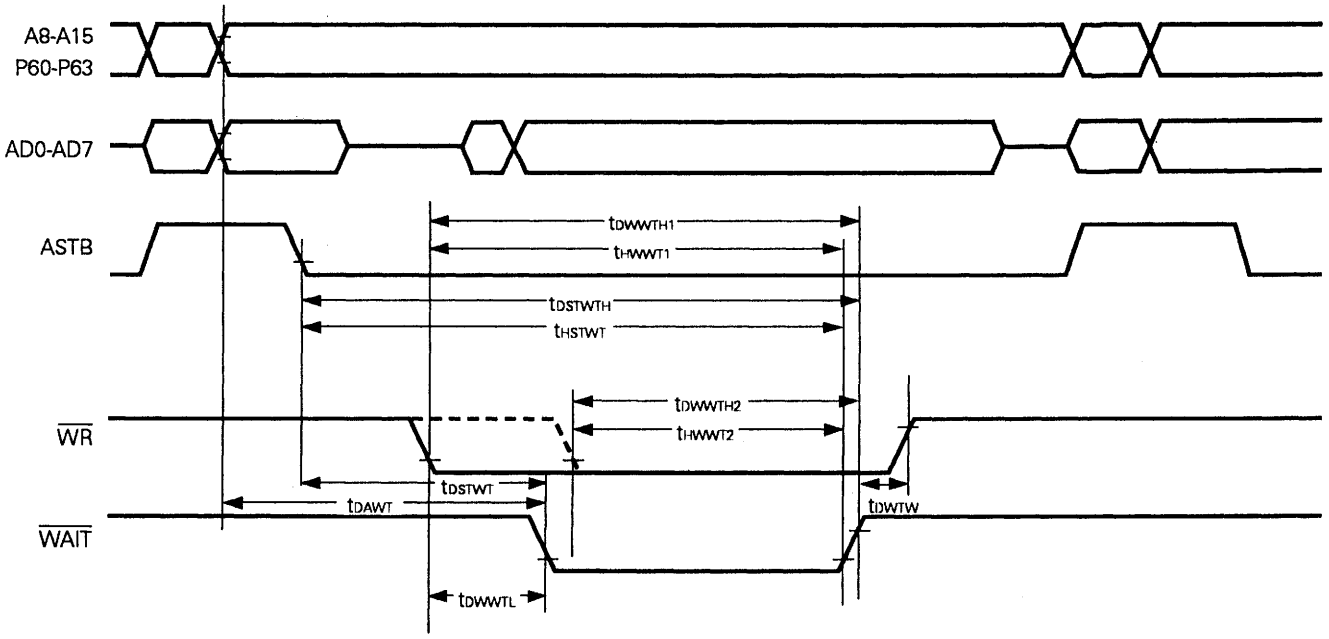


External WAIT Signal Input Timing

Read operation

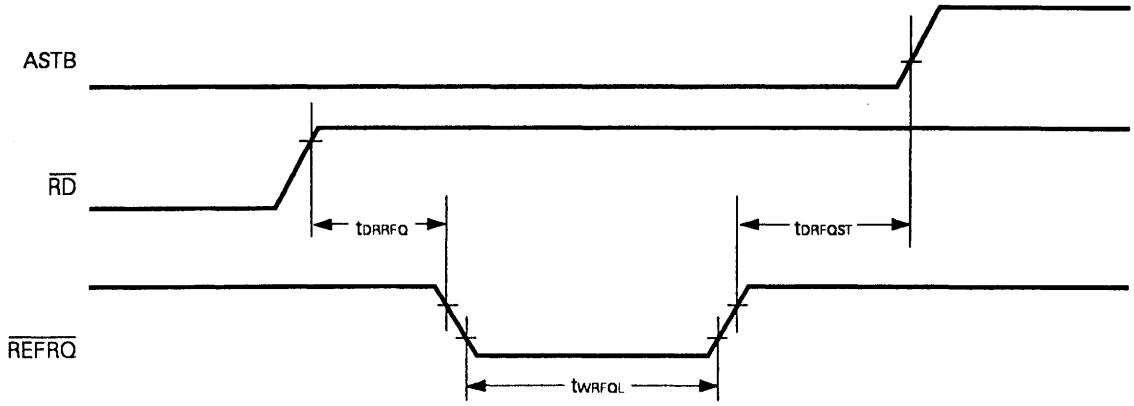


Write operation

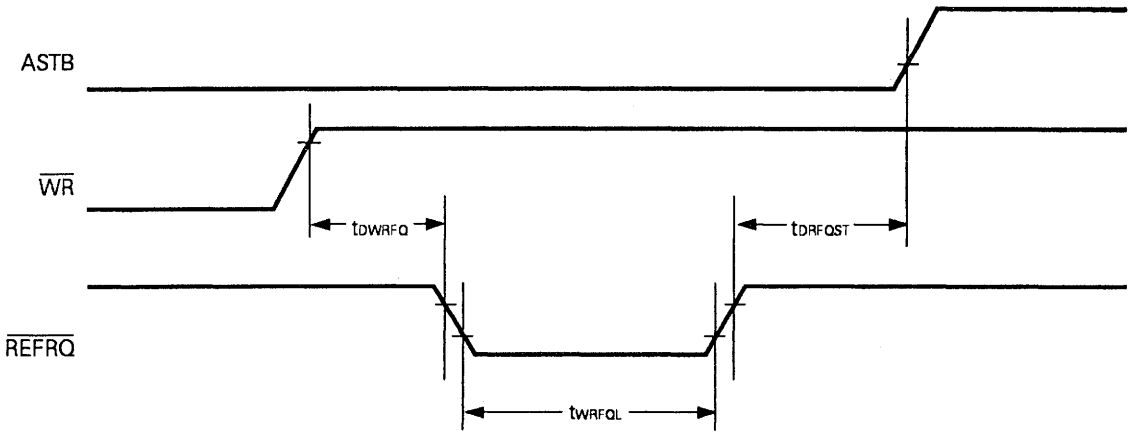


Refresh Timing Waveform

Refresh after read

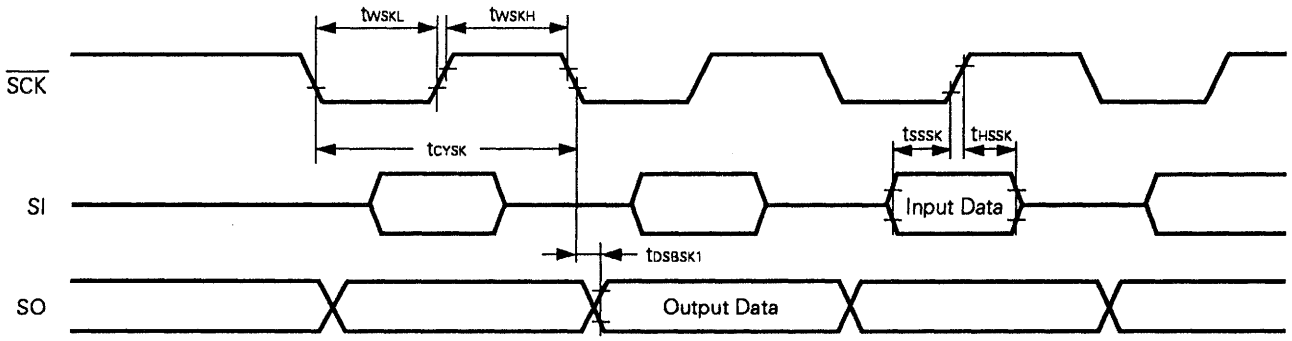


Refresh after write



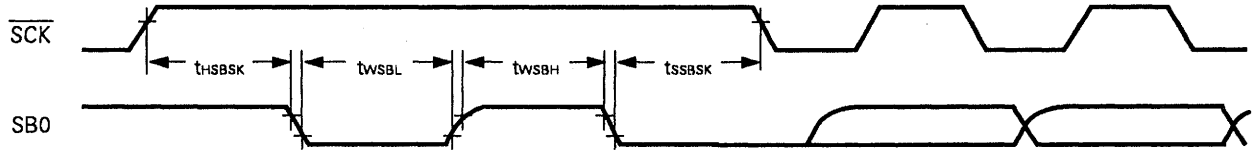
Serial Operation

3-wire serial I/O mode

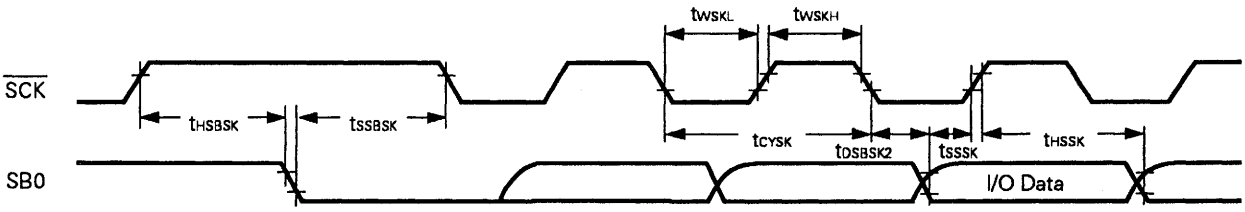


SBI Mode

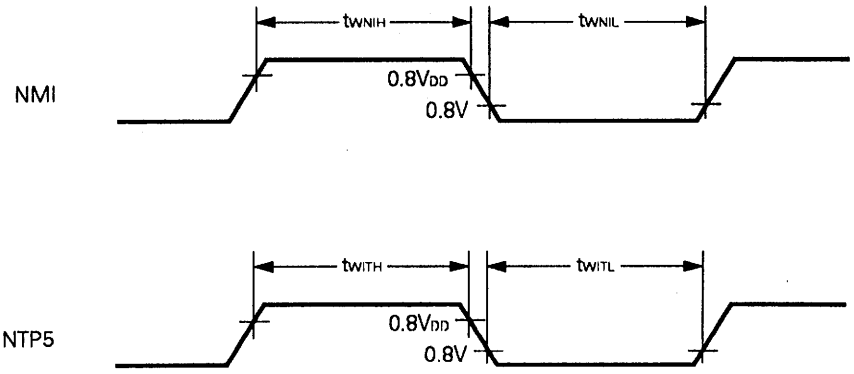
Bus release signal transfer



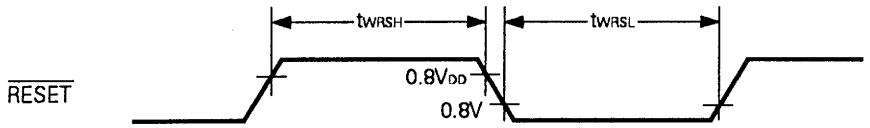
Command signal transfer



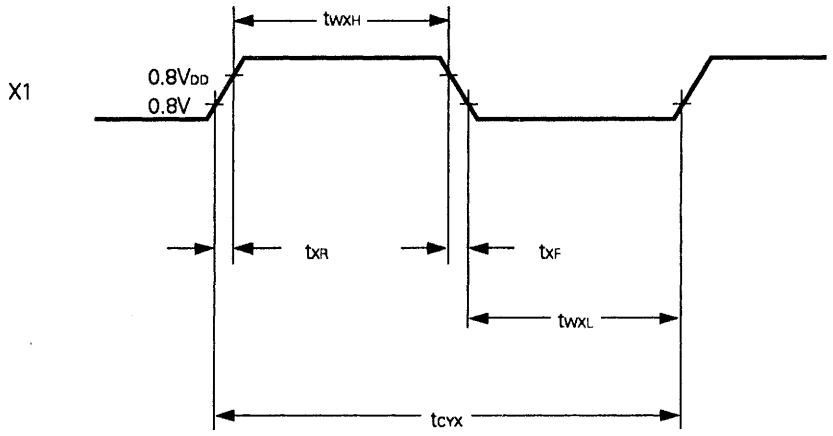
Interrupt Input Timing



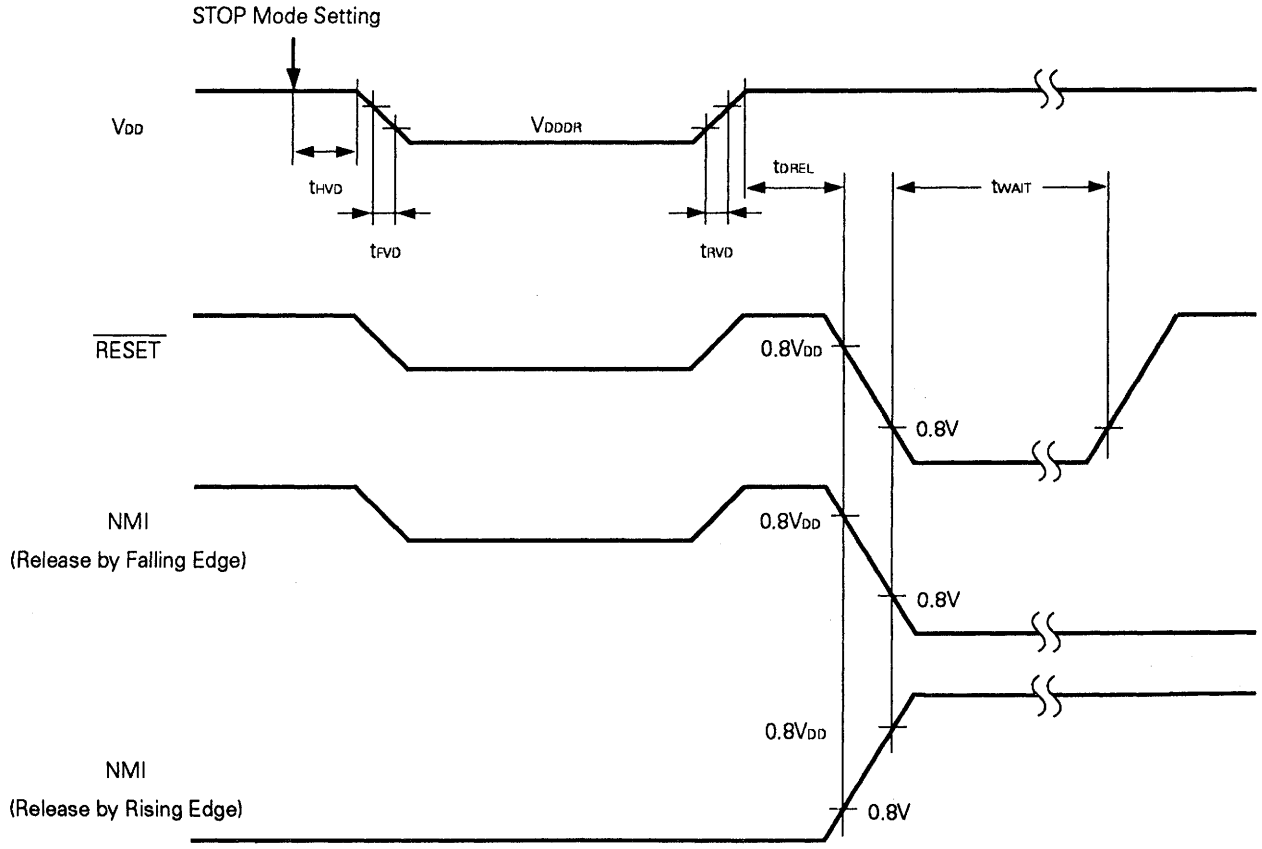
Reset Input Timing



External Clock Timing



Data Retention Characteristics



DC PROGRAMMING CHARACTERISTICS (T_a = +25 to ±5 °C, V_{IP} *1 = +12.5 ±0.5 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	SYMBOL *2	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH}	V_{IH}		2.4		V_{DDP} + 0.3	V
Input voltage low	V_{IL}	V_{IL}		−0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$			10	μA
Output voltage high	V_{OH1}	V_{OH1}	I_{OH} = − 400 μA	2.4			V
	V_{OH2}	V_{OH2}	I_{OL} = − 100 μA	V_{DD}−0.7			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output leakage current	I_{OL}		$0 \le V_O \le V_{DDP}$, $\overline{OE} = V_{IH}$			10	μA
NMI pin high-voltage input current	I_{IP}					± 10	μA
V_{DDP} supply voltage	V_{DDP}	V_{CC}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	$V_{PP} = V_{DDP}$			V
V_{DDP} supply current	I_{DD}	I_{CC}	Program memory write mode		5	30	mA
			Program memory read mode $\overline{CE} = V_{IL}$, $V_I = V_{IH}$		5	30	mA
V_{PP} supply current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		5	30	mA
			Program memory read mode		1	100	μA

* 1. Voltage applied to P20/NMI pin
2. Symbol of the corresponding μPD27C256A

PROGRAM OPERATION

AC CHARACTERISTICS (Ta = +25 to ±5 °C, V_{IP} *1 = +12.5 ±0.5 V, V_{DD} = +6 ±0.25 V, V_{PP} = +12.5 ±0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	SYMBOL *2	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address setup time (to $\overline{CE}$ ↓)	t_{SAC}	t_{AS}		2			μs
$\overline{OE}$ ↓ hold time from data	t_{DDOO}	t_{OES}		2			μs
Input data setup time (to $\overline{CE}$ ↓)	t_{SIDC}	t_{DS}		2			μs
Address hold time (from $\overline{CE}$ ↑)	t_{HCA}	t_{AH}		2			μs
Input data hold time (from $\overline{CE}$ ↑)	t_{HCID}	t_{DH}		2			μs
Output data hold time (from $\overline{OE}$ ↑)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time (to $\overline{CE}$ ↓)	t_{SVPC}	t_{VPS}		1			ms
V_{DDP} setup time (to $\overline{CE}$ ↓)	t_{SVDC}	t_{VCS}		1			ms
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
NMI high-voltage input setup time (to $\overline{CE}$ ↓)	t_{SPC}			2			μs
Data output time from $\overline{OE}$ ↓	t_{DOOD}	t_{OE}				150	ns

* 1. Voltage applied to P20/NMI pin
2. Symbol of the corresponding μPD27C256A

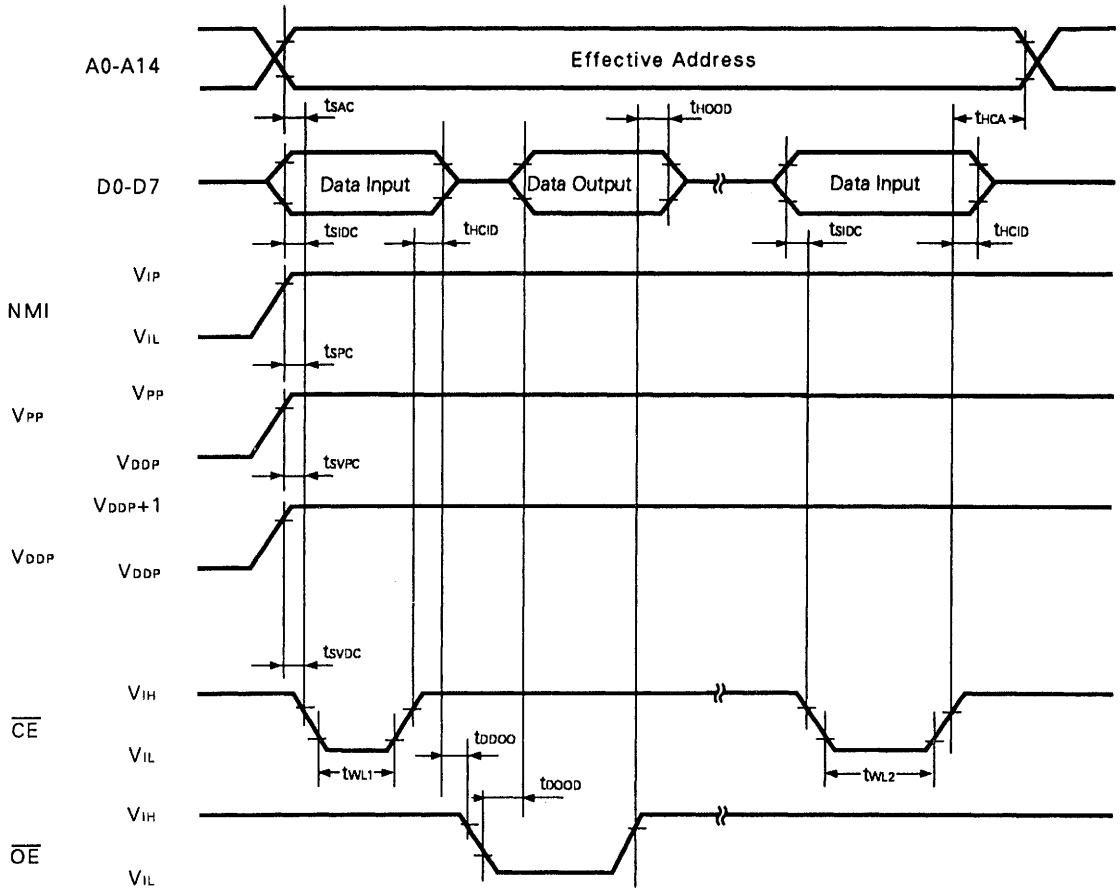
READ OPERATION

AC CHARACTERISTICS (Ta = +25 ±5 °C, V_{IP} *1 = +12.5 ±0.5 V, V_{DD} = +5 ±0.5 V, V_{PP} = V_{DDP}, V_{SS} = 0 V)

PARAMETER	SYMBOL	SYMBOL *2	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address data output time	t_{DAOD}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			200	ns
Data output time from $\overline{CE}$ ↓	t_{DCOD}	t_{CE}	$\overline{OE}$ = V_{IL}			200	ns
Data output time from $\overline{OE}$ ↓	t_{DOOD}	t_{OE}	$\overline{CE}$ = V_{IL}			75	ns
Data hold time (from $\overline{OE}$ ↑, $\overline{CE}$ ↑)*3	t_{HCOD}	t_{DF}	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}	0		60	ns
Data hold time (from address)	t_{HAOD}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

* 1. Voltage applied to P20/NMI pin
2. Symbol of the corresponding μPD27C256A
3. t_{HCOD} is the time from the point at which either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

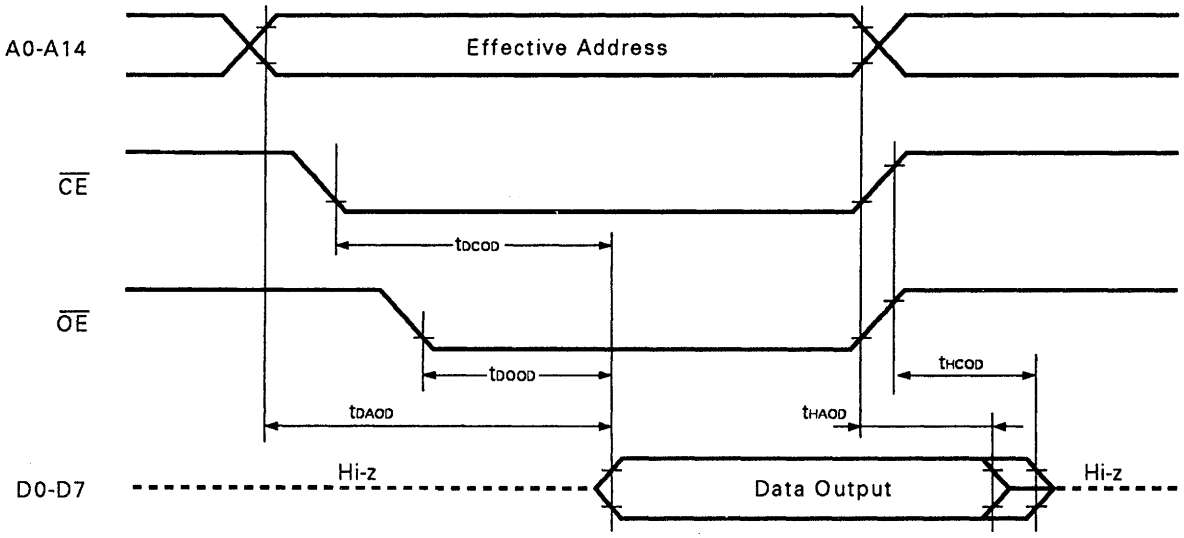
PROM Write Mode Timing



Note 1. Apply V_{DDP} before V_{PP} and shut it off after V_{PP}.

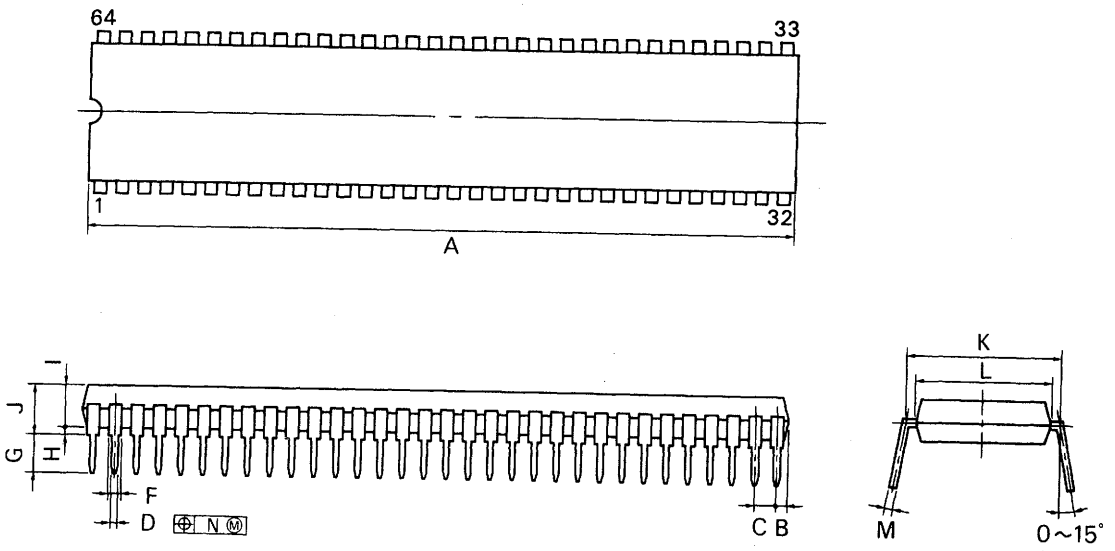
2. Do not allow V_{PP} to become +13 V or more including an overshoot.

PROM Read Mode Timing



8. PACKAGE INFORMATION

64PIN PLASTIC SHRINK DIP (750 mil)



P64C-70-750A,C

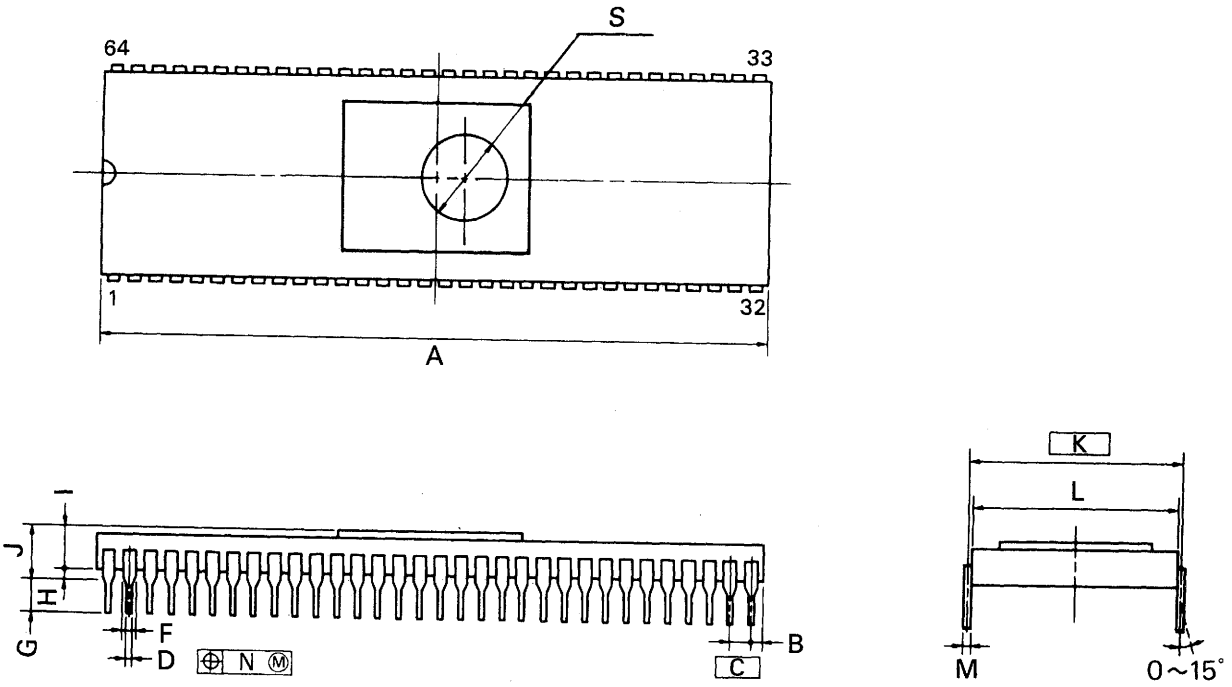
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

64PIN CERAMIC SHRINK DIP (CERDIP) (WINDOW) (750 mil)



P64DW-70-750A1

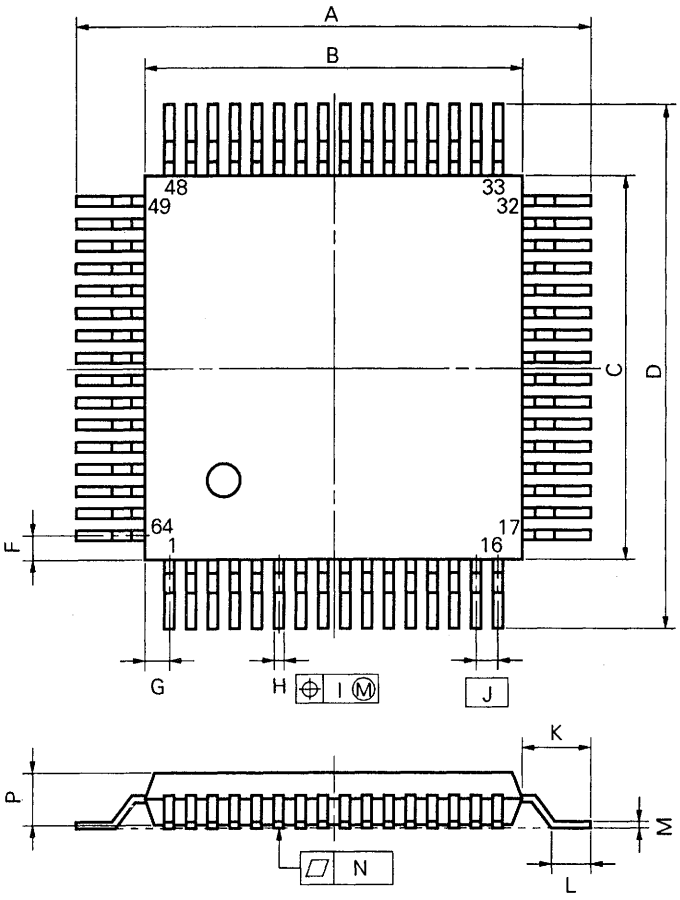
ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.310 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.46^{\pm 0.05}$	$0.018^{\pm 0.002}$
F	0.8 MIN.	0.031 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	1.0 MIN.	0.039 MIN.
I	3.0	0.118
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	$0.25^{\pm 0.05}$	$0.010^{+0.002}_{-0.003}$
N	0.25	0.01
S	ϕ7.62	ϕ0.300

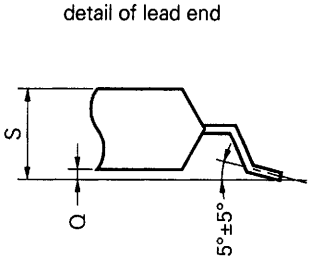
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

64 PIN PLASTIC QFP (□14)





P64GC-80-AB8-3

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

9. RECOMMENDED SOLDERING CONDITIONS

The μPD78P218A should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document "Semiconductor Device Mounting Technology Manual" (IEI-1207).

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 9-1 Surface Mounted Type Soldering Conditions

μPD78P218AGC-AB8: 64-pin plastic QFP (□14 mm)

	Soldering Method	Soldering Conditions	Recommended Condition Symbol
	Infrared reflow	Package peak temperature: 230°C Duration: 30 sec. max. (at 210°C or above) Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C)	IR30162-1
	VPS	Package peak temperature: 215°C Duration: 40 sec. max. (at 200°C or above) Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C)	VP15-162-1
★	Infrated reflow	Package peak temperature : 235°C Duration : 30 sec. max. (at 210°C or above) Number of times : once Time limit : 2 days* (thereafter 20 hours prebaking required at 125°C)	IR35-202-1
★	VPS	Package peak temperature : 215°C Duration : 40 sec. max. (at 200°C or above) Number of times : once Time limit : 2 days* (thereafter 20 hours prebaking required at 125°C)	VP15-202-1
	Pin part heating	Pin part temperature: 300°C max. Duration: 3 sec. max. (Per side of the device)	———

* For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

Note Use more than one soldering method should be avoided (except in the case of pin part heating).

Table 9-2 Insert Type Soldering Conditions

μPD78P218ACW: 64-pin plastic shrink DIP (750 mil)
μPD78P218ADW: 64-pin ceramic shrink DIP (CERDIP)(with window) (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (lead part only)	Solder bath temperature : 260°C max. Duration: 10 sec. max.
Pin part heating	Pin part temperature: 260°C max. Duration: 10 sec. max.

Note The wave soldering applies to the lead part only. Ensure that no solder touches the body directly.

Notice

A version of this product with improved recommended soldering conditions is available. For details (improvements such as infrared reflow peak temperature extension (235°C), number of times: twice, relaxation of time limit, etc.), contact NEC sales personnel.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD78P218A.

Language Processing Software

RA78K/II *1,2,3	78K/II series common assembler package
CC78K/II *1,2,3	78K/II series common C compiler package
CC78K/II-L *1,2,3	78K/II series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P214CW PA-78P214GC	Programmer adapters connected to PG-1500
PG-1500 controller *1,2	PG-1500 control program

Debugging Tools

IE-78240-R-A IE-78240-R *4	μPD78218A subseries common in-circuit emulators
IE-78200-R-BK	78K/II series common break board
IE-78240-R-EM IE-78200-R-EM *4	μPD78218A subseries evaluation emulation boards
EP-78210CW *4 EP-78240CW-R EP-78210GC *4 EP-78240GC-R	μPD78218A subseries common emulation probes
EV-9200GC-64	Socket to be mounted on a user system board made for 64-pin plastic QFP
SD78K/II *1,2	IE-78240-R-A screen debugger
DF78210 *1,2	μPD78218A subseries device file

Real-Time OS

RX78K/II *1,2,3	78K/II series common real-time OS

* 1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ (PC DOS™) based
3. HP9000 series 300™ (HP-UX™) based, SPARCstation™ (Sun OS™) based, EWS-4800 series™ (EWS-UX/V™) based
4. No longer manufactured and not available for purchase

Fuzzy Inference Development Support System

FE9000 *1, FE9200 *2	Fuzzy knowledge data creation tool
FT9080 *1, FT9085 *2	Translator
FI78K/II *1,2	Fuzzy inference module
FD78K/II *1,2	Fussy inference debugger

* 1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ (PC DOS™) based

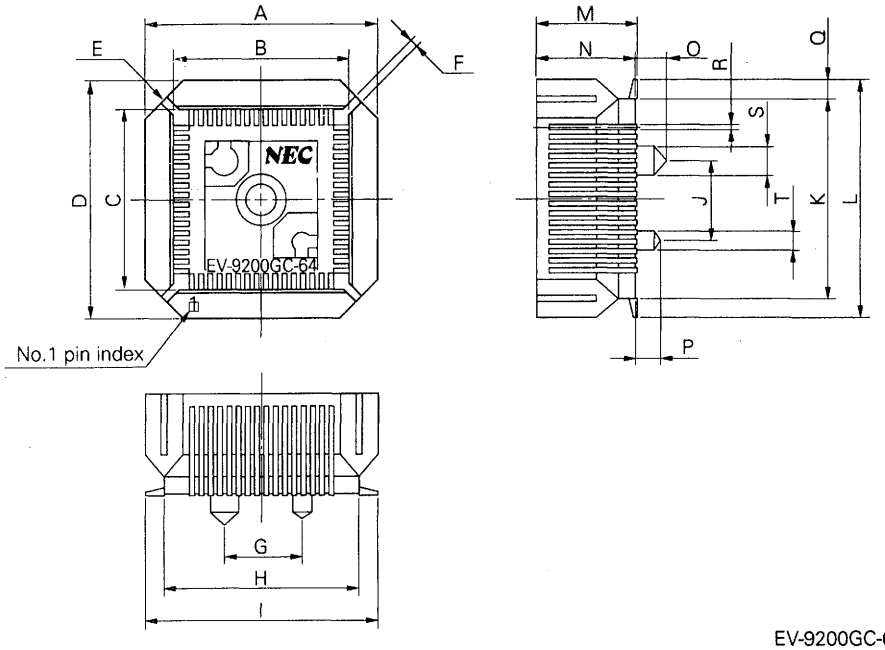
Remarks For third party development tools, see the **78K/II Series Development Tools Selection Guide (EF-231)**.

APPENDIX B. EXTERNAL VIEW OF CONVERSION SOCKET AND RECOMMANDED BOARD MOUNTING PATTERN

The μPD78P218AGC-AB8 (64-pin plastic QFP (□14mm) is mounted on the board in conjunction with the conversion socket (EV-9200GC-64).

The external view of the conversion socket and recommended board mounting pattern are shown below.

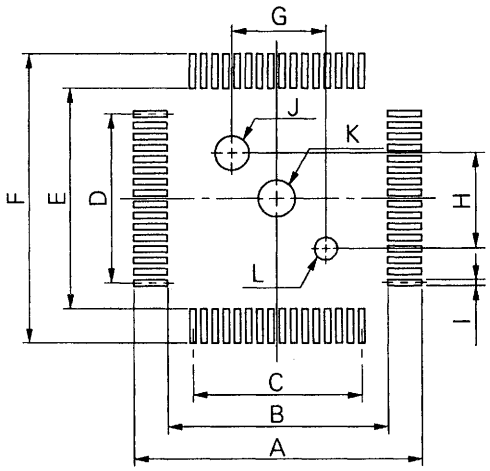
Fig. B-1 EV-9200GC-64 External View (Reference)



EV-9200GC-64-G0

ITEM	MILLIMETERS	INCHES
A	18.8	0.74
B	14.1	0.555
C	14.1	0.555
D	18.8	0.74
E	4-C 3.0	4-C 0.118
F	0.8	0.031
G	6.0	0.236
H	15.8	0.622
I	18.5	0.728
J	6.0	0.236
K	15.8	0.622
L	18.5	0.728
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35±0.1	$0.014^{+0.004}_{-0.005}$
S	φ2.3	φ0.091
T	φ1.5	φ0.059

Fig. B-2 Recommended EV-9200GC-64 Board Mounting Pattern (Reference)



EV-9200GC-64-P0

ITEM	MILLIMETERS	INCHES
A	19.5	0.768
B	14.8	0.583
C	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
D	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
E	14.8	0.583
F	19.5	0.768
G	6.00 ± 0.08	$0.236^{+0.004}_{-0.003}$
H	6.00 ± 0.08	$0.236^{+0.004}_{-0.003}$
I	0.5 ± 0.02	$0.197^{+0.001}_{-0.002}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.2\pm0.1$	$\phi0.087^{+0.004}_{-0.005}$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

APPENDIX C. RELATED DOCUMENTS

Device Related Documents

Document Name		Document No. (Japanese)	Document No. (English)
μPD78218A Subseries User's Manual Hardware Volume		IEU-755	IEU-1313
78K/II Series User's Manual Instruction Volume		IEU-754	IEU-1311
78K/II Series Application Note	Introductory Volume	IEA-607	IEA-1220
	Application Volume	IEA-700	IEA-1282
	Floating-Point Operation Program Volume	IEA-686	IEA-1273
78K/II Series Selection Guide		IF-304	IF-1160
78K/II Series Instruction Application Table		IEM-5101	——
78K/II Series Instruction Set		IEM-5102	——
μPD78218A Series Special Function Register Application Table		IEM-5532	——

Development Tool Related Documents (User's Manuals)

Document Name		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation Volume	EEU-809	EEU-1399
	Language Volum	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation Volume	EEU-656	EEU-1280
	Language Volume	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	——
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller		EEU-704	EEU-1291
IE-78240-R-A In-Circuit Emulator		EEU-796	EEU-1395
IE-78240-R In-Circuit Emulator	Hardware Volume	EEU-705	EEU-1322
	Software Volume	EEU-706	EEU-1331
SD78K/II Screen Debugger MS-DOS Based	Primer	EEU-841	——
	Reference	EEU-813	——
SD78K/II Screen Debugger PC DOS Based	Primer	——	——
	Reference	——	EEU-1447
78K/II Series Development Tools Selection Guide		EF-231	——

Note The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

Built-In Software Related Documents (User's Manuals)

Document Name		Document No. (Japanese)	Document No. (English)
RX78K/II Real-Time OS	Introductory Volume	EEU-910	——
	Installation Volume	EEU-884	——
	Debugger Volume	EEU-895	——
	Technical Volume	EEU-885	——
Fuzzy Knowledge Data Creation Tools		EEU-829	EEU-1438
78/0, 78K/II, 87AD Series Fuzzy Inference Development Support System	Translator	EEU-862	EEU-1444
78K/II Series Fuzzy Inference Development Support System	Fuzzy Inference Module	EEU-860	EEU-1440
78K/II Series Fuzzy Inference Debugger		EEU-917	EEU-1459

Other Related Documents

Document Name	Document No. (Japanese)	Document No. (English)
QTOP Microcomputer Brochure	IB-5040	——
Semiconductor Device Package Manual	IEI-635	IEI-1213A
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207B
Quality Grades on Semiconductor Devices	IEI-620	IEI-1209A
NEC Semiconductor Device Reliability & Quality Control	IEM-5068	——
Electrostatic Discharge (ESD) Test	MEM-539	——
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202
Microcomputer Related Products Guide Other Manufacturers Volume	MEI-604	——

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