NEC

MOS INTEGRATED CIRCUIT

μPD78P238

8 BIT SINGLE-CHIP MICROCOMPUTER

The μPD78P238 is an 8-bit single-chip microcomputer produced by replacing the mask ROM in the μPD78238 with one-time PROM or EPROM. Since a user program can be written on the one-time PROM or EPROM, this microcomputer is suitable for the evaluation of the system to be developed and small production.

The following user's manual describes the details of the functions of the μPD78P238. Be sure to read it before designing an application system.

μPD78234 Series User's Manual, Hardware: IEU-718
78K/II Series User's Manual, Instruction : IEU-754

FEATURES

- Compatible with the μPD78234 or the μPD78238
- Built-in EPROM
  - μPD78P238KF : Reprogrammable (suitable for system evaluation)
  - μPD78P238GC/GJ/LQ: Programmable only once (suitable for small production)
  - QTOP™ microcomputer

Remark The QTOP microcomputer is a single-chip microcomputer with a built-in one-time PROM that is totally supported by NEC. The support includes writing application programs, marking, screening, and verification. ★

ORDERING INFORMATION

Part number	Package	Internal ROM	
μPD78P238GC-3B9	80-pin plastic QFP (14 × 14 mm)	One-time PROM	
μPD78P238GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm)	One-time PROM (QTOP microcomputer)	★
μPD78P238GJ-5BG	94-pin plastic QFP (20 × 20 mm)	One-time PROM	
μPD78P238GJ-xxx-5BG	94-pin plastic QFP (20 × 20 mm)	One-time PROM (QTOP microcomputer)	★
μPD78P238LQ	84-pin plastic QFJ (1150 × 1150 mil)	One-time PROM	
μPD78P238LQ-xxx	84-pin plastic QFJ (1150 × 1150 mil)	One-time PROM (QTOP microcomputer)	★
μPD78P238KF	94-pin ceramic WQFN (20 × 20 mm)	EPROM	

Remark xxx: ROM code number

QUALITY GRADE

Standard

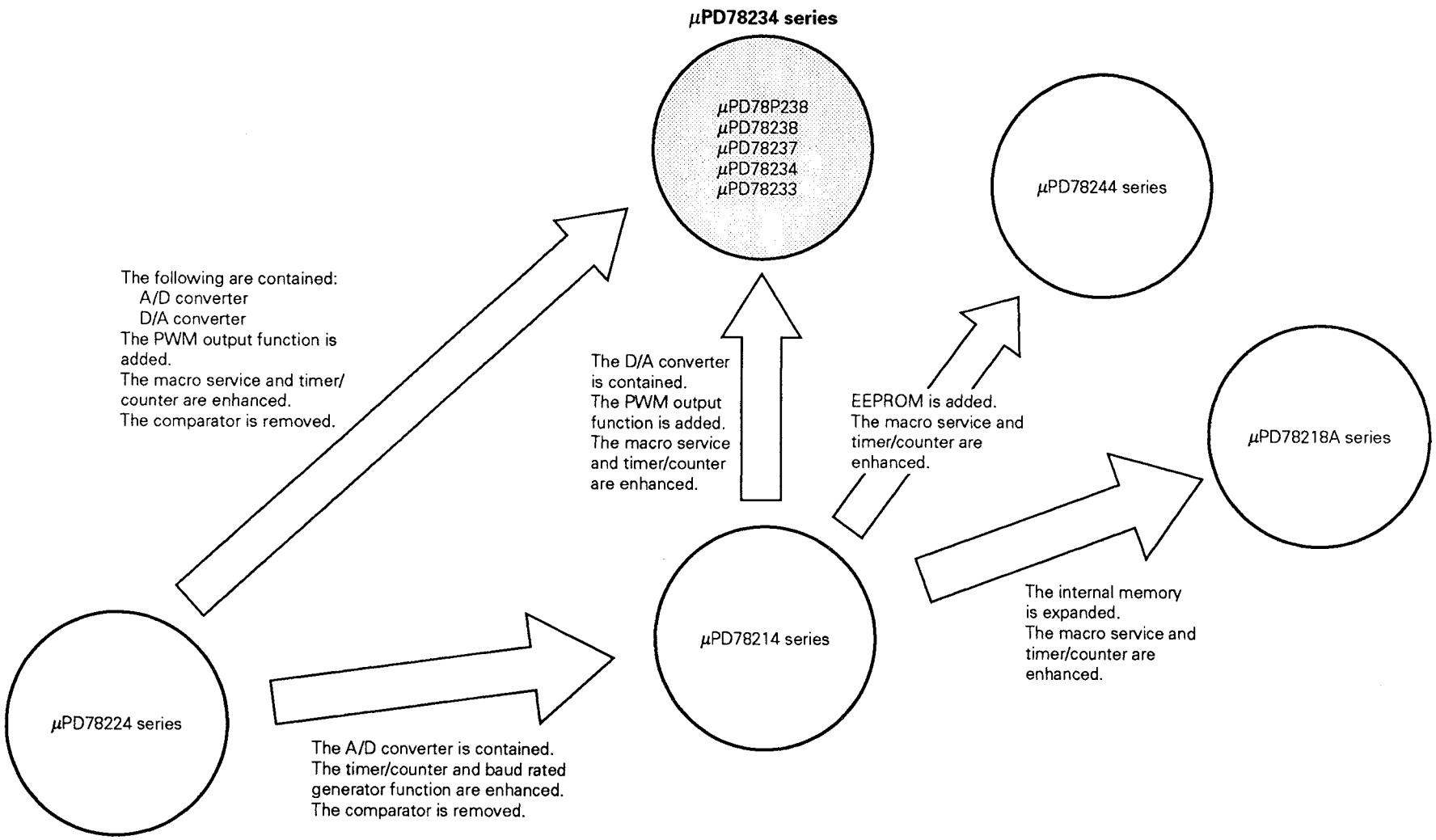
Please refer to *Quality Grades on NEC Semiconductor Devices* (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

In this document, the word "PROM" refers to both one-time PROM and EPROM.

Document No. IC-2607B
(O. D. No. IC-8030B)
Date Published January 1994 P
Printed in Japan

Major changes in this revision are indicated by stars (★) in the margins.

DIAGRAM OF 78K/II PRODUCT DEVELOPMENT



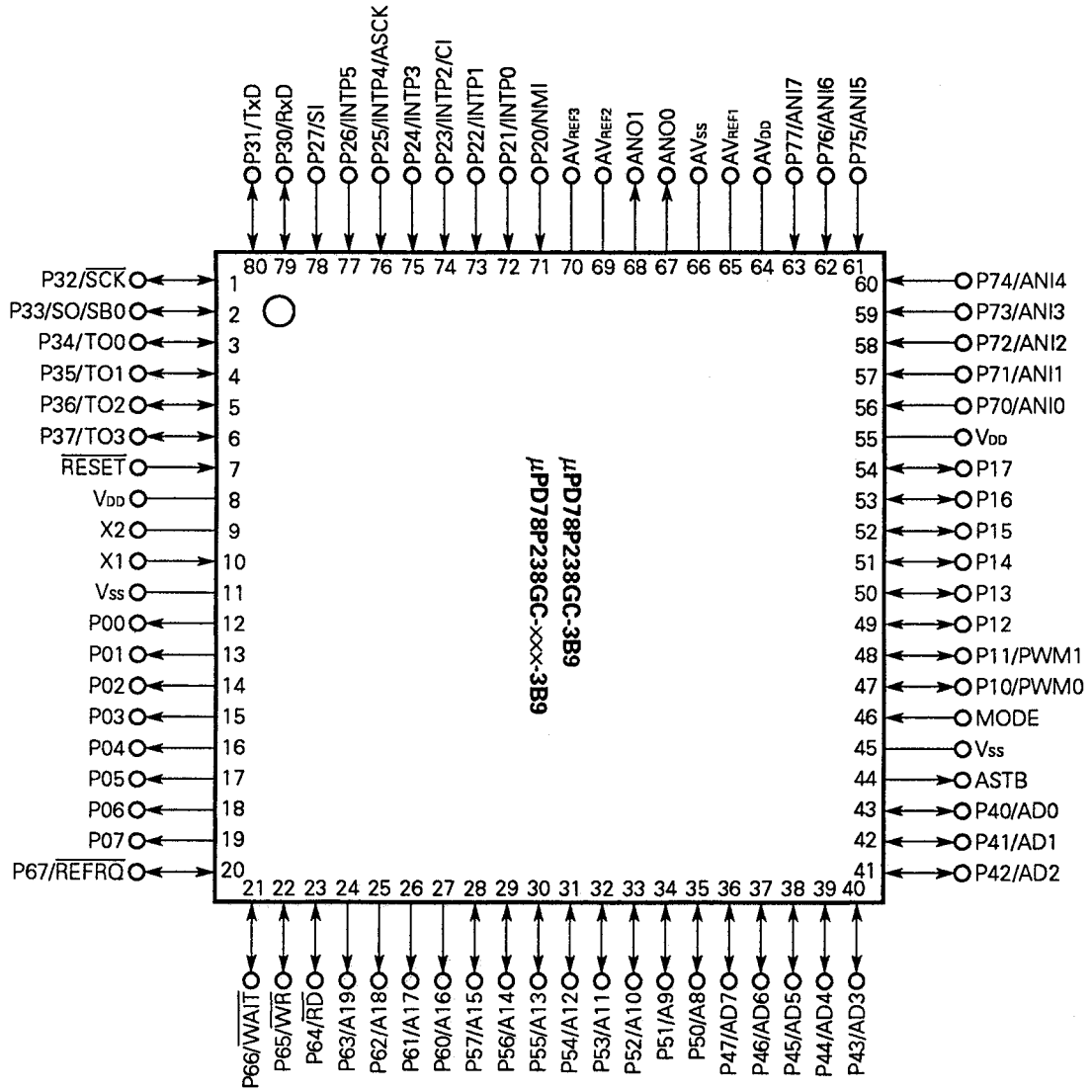
FUNCTIONS

Item		Function
Number of basic instructions (mnemonics)		65
Minimum instruction execution time		333 ns (at 12 MHz)
Internal memory size	PROM	32K bytes
	RAM	1024 bytes
Address space		1M bytes
Number of I/O pins		Input ports : 16 } Pull-up resistor provided I/O ports : 36 } (to be specified by software): 42 inputs LED operable : 24 outputs Transistor operable: 8 outputs Output ports : 12
General register		8 bits × 8 × 4 banks (memory mapping)
Timer/counter		16-bit timer/counter {Timer register × 1 Capture register × 1 Compare register × 2 Pulse output possible (Toggled output PWM/PPG output One-shot pulse output)
		8-bit timer/counter 1 {Timer register × 1 Capture/compare register × 1 Compare register × 1 Pulse output possible (Real-time output: 4 bits × 2)
		8-bit timer/counter 2 {Timer register × 1 Capture register × 1 Compare register × 2 Pulse output possible (Toggled output PWM/PPG output)
		8-bit timer/counter 3 {Timer register × 1 Compare register × 1
PWM output function		12-bit resolution × 2 channels
Serial interface		UART : 1 channel (baud rate generator contained) Clock synchronous serial I/O : 1 channel
A/D converter		8-bit resolution × 8 channels
D/A converter		8-bit resolution × 2 channels
Interrupt function		19 sources (external: 7, internal: 12) and BRK instruction 2 priority levels (programmable) Two types of interrupt processing modes (vectored interrupt function and macro service function)
Instruction set		16-bit arithmetic/logical instructions Multiply/divide instructions (8 bits × 8 bits, 16 bits ÷ 8 bits) Bit manipulation instructions BCD correction instructions, etc.
Package		94-pin ceramic WQFN (20 × 20 mm) 80-pin plastic QFP (14 × 14 mm) 94-pin plastic QFP (20 × 20 mm) 84-pin plastic QFJ (1150 × 1150 mil)

PIN CONFIGURATION (TOP VIEW)

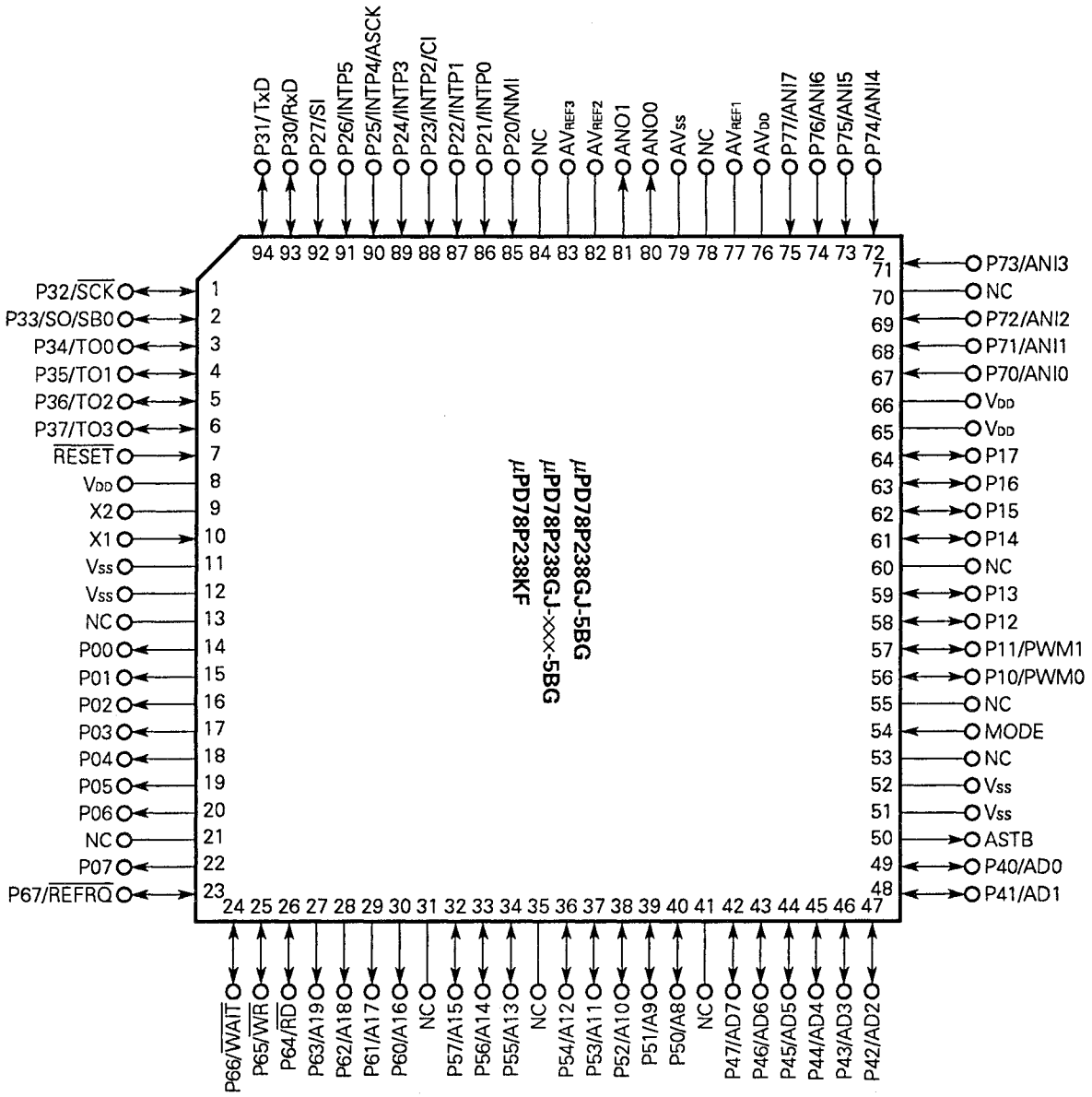
(1) Normal operation mode

80-pin plastic QFP (14 × 14 mm)

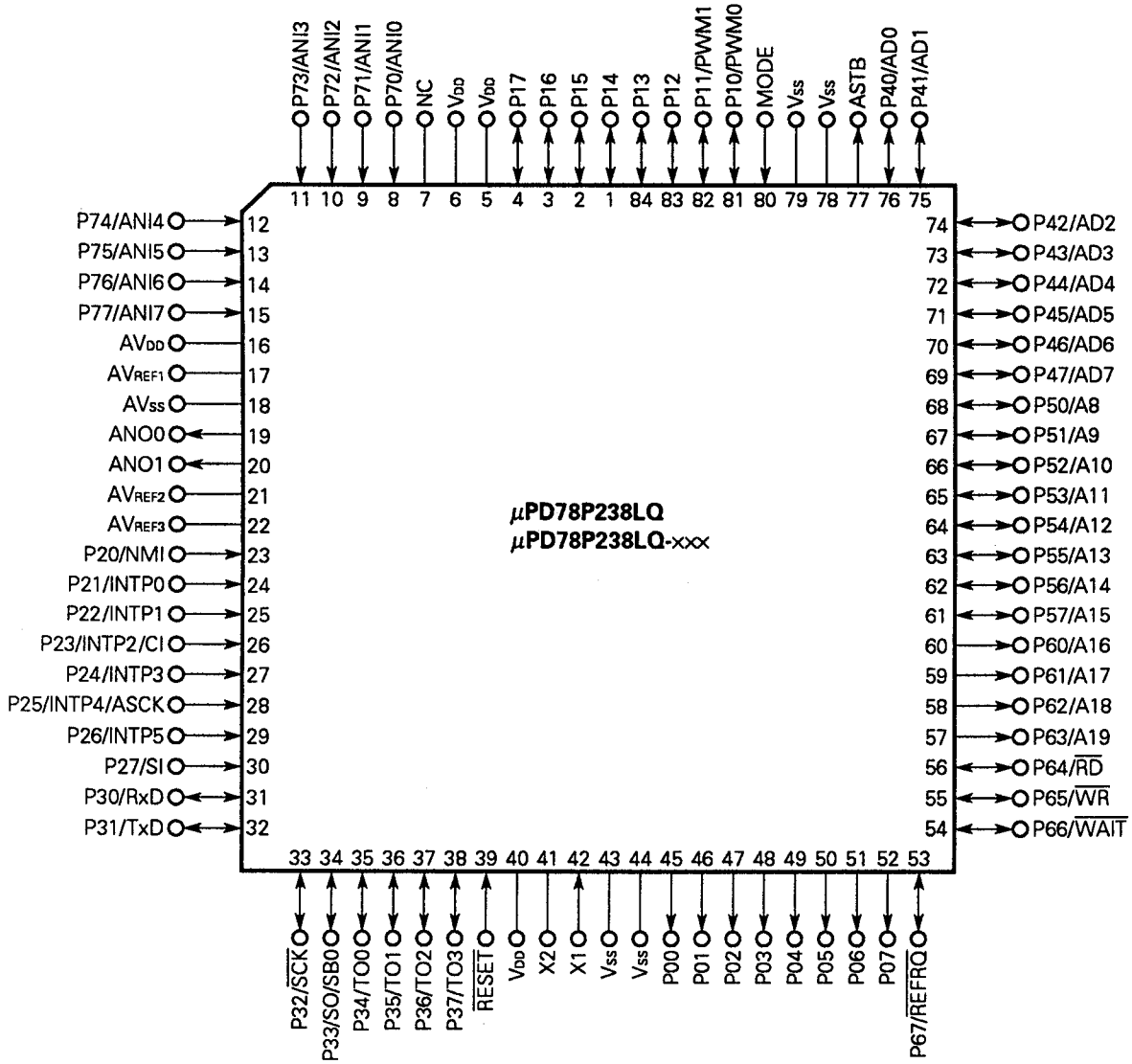


94-pin plastic QFP (20 × 20 mm)

94-pin ceramic WQFN (20 × 20 mm)



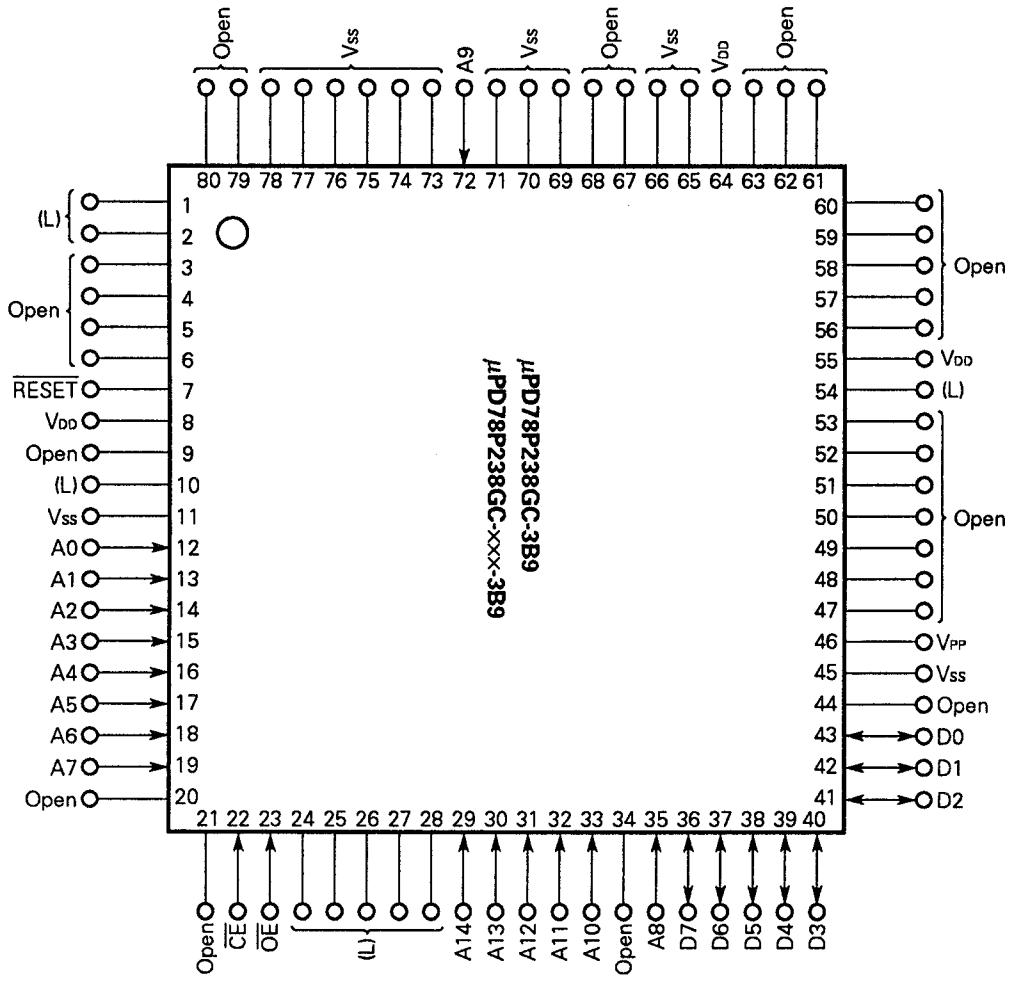
84-pin plastic QFJ (1150 × 1150 mil)



P00-P07 : Port 0
P10-P17 : Port 1
P20-P27 : Port 2
P30-P37 : Port 3
P40-P47 : Port 4
P50-P57 : Port 5
P60-P67 : Port 6
P70-P77 : Port 7
TO0-TO3 : Timer output
CI : Clock input
RxD : Receive data
TxD : Transmit data
$\overline{SCK}$: Serial clock
ASCK : Asynchronous serial clock
SB0 : Serial bus
SI : Serial input
SO : Serial output
PWM0, PWM1: Pulse width modulation output
NMI : Non-maskable interrupt
INTP0-INTP5 : Interrupt from peripherals
AD0-AD7 : Address/data bus
A8-A19 : Address bus
$\overline{RD}$: Read strobe
$\overline{WR}$: Write strobe
$\overline{WAIT}$: Wait
ASTB : Address strobe
$\overline{REFRQ}$: Refresh request
$\overline{RESET}$: Reset
X1, X2 : Crystal
MODE : Mode
ANI0-ANI7 : Analog input
ANO0, ANO1 : Analog output
AV_{REF1}-AV_{REF3} : Reference voltage
AV_{DD} : Analog power supply
AV_{SS} : Analog ground
V_{DD} : Power supply
V_{SS} : Ground
NC : No connection

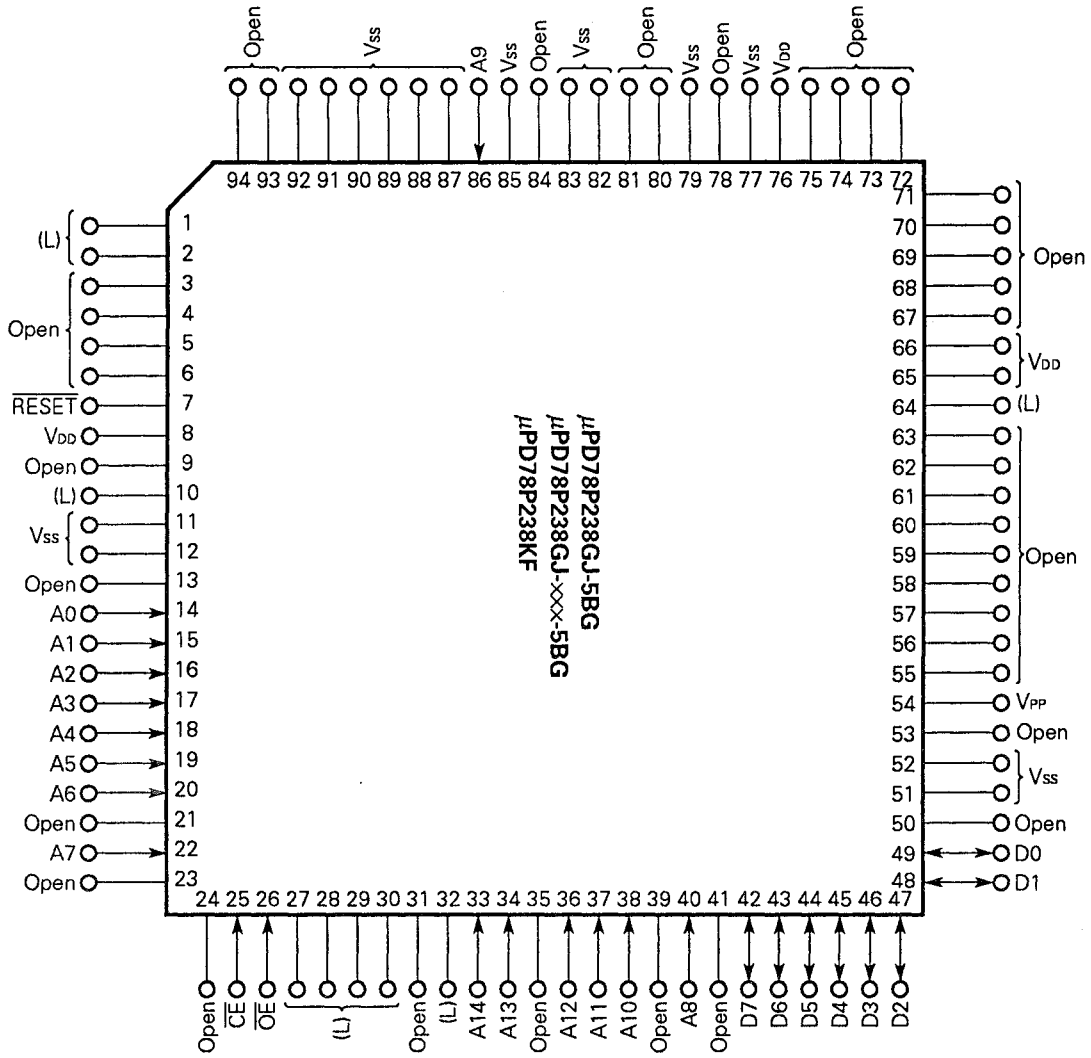
(2) PROM programming mode

80-pin plastic QFP (14 × 14 mm)



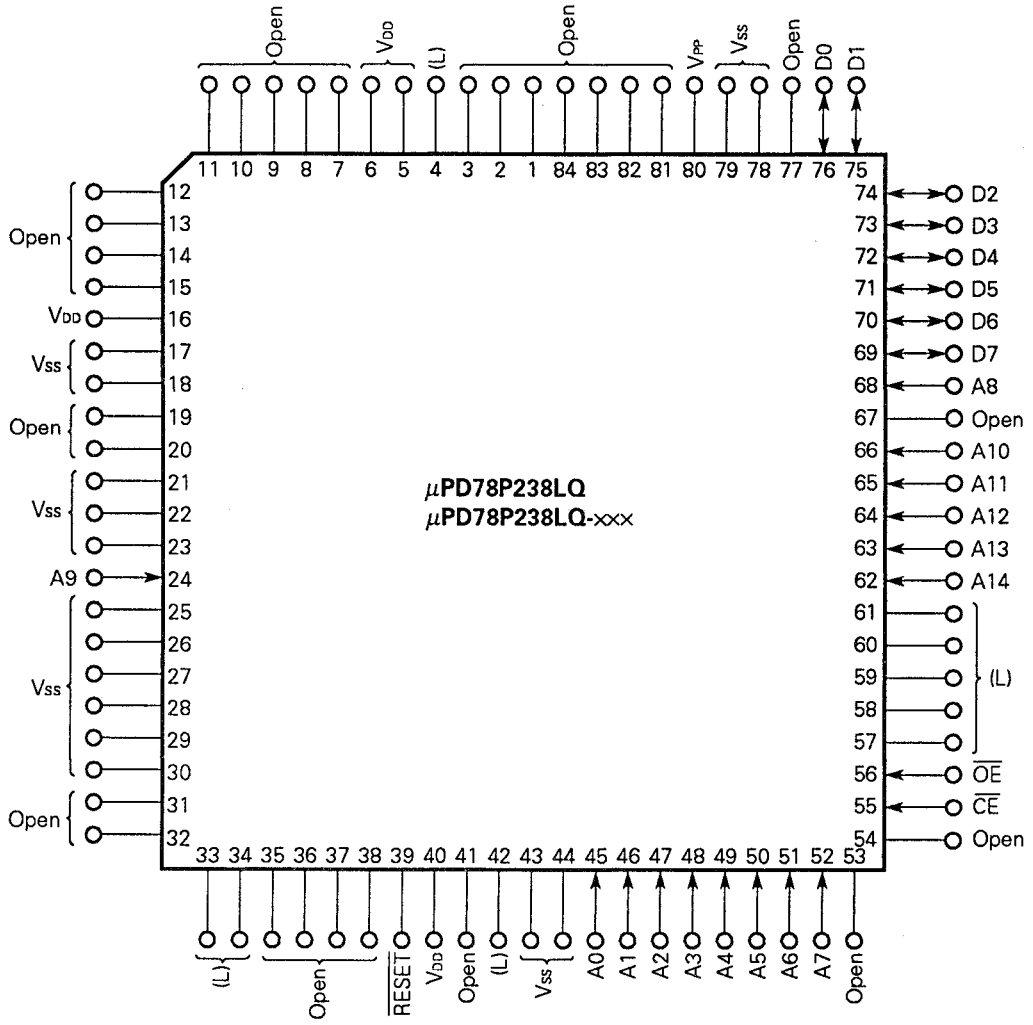
Caution L : Connect these pins separately to the Vss pins through pull-down resistors.
Vss : To be connected to the ground.
Open : Nothing should be connected on these pins.
RESET : Set a low-level input.

94-pin plastic QFP (20 × 20 mm)
94-pin ceramic WQFN (20 × 20 mm)



Caution L : Connect these pins separately to the Vss pins through pull-down resistors.
Vss : To be connected to the ground.
Open : Nothing should be connected on these pins.
$\overline{\text{RESET}}$: Set a low-level input.

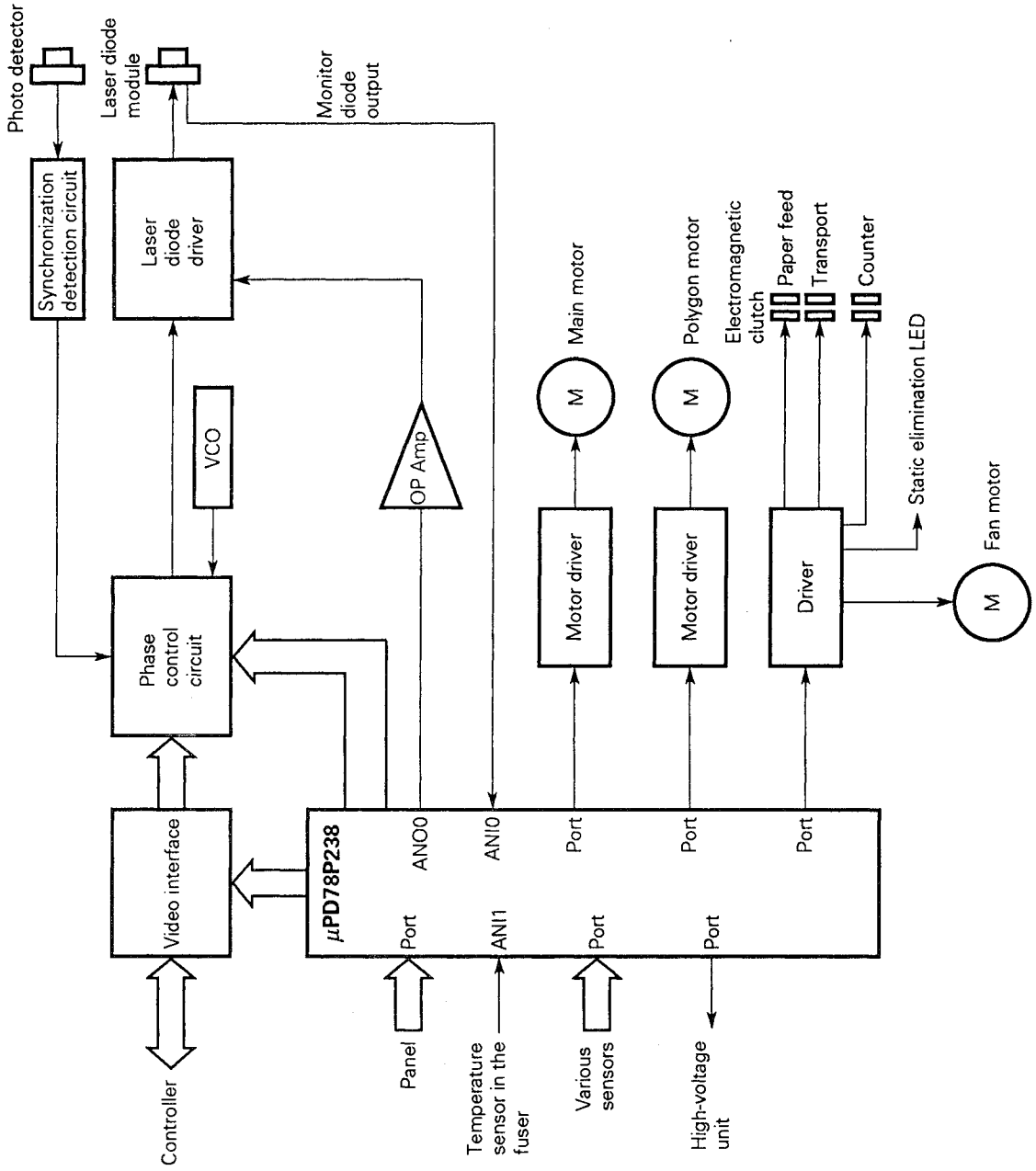
84-pin plastic QFJ (1150 × 1150 mil)



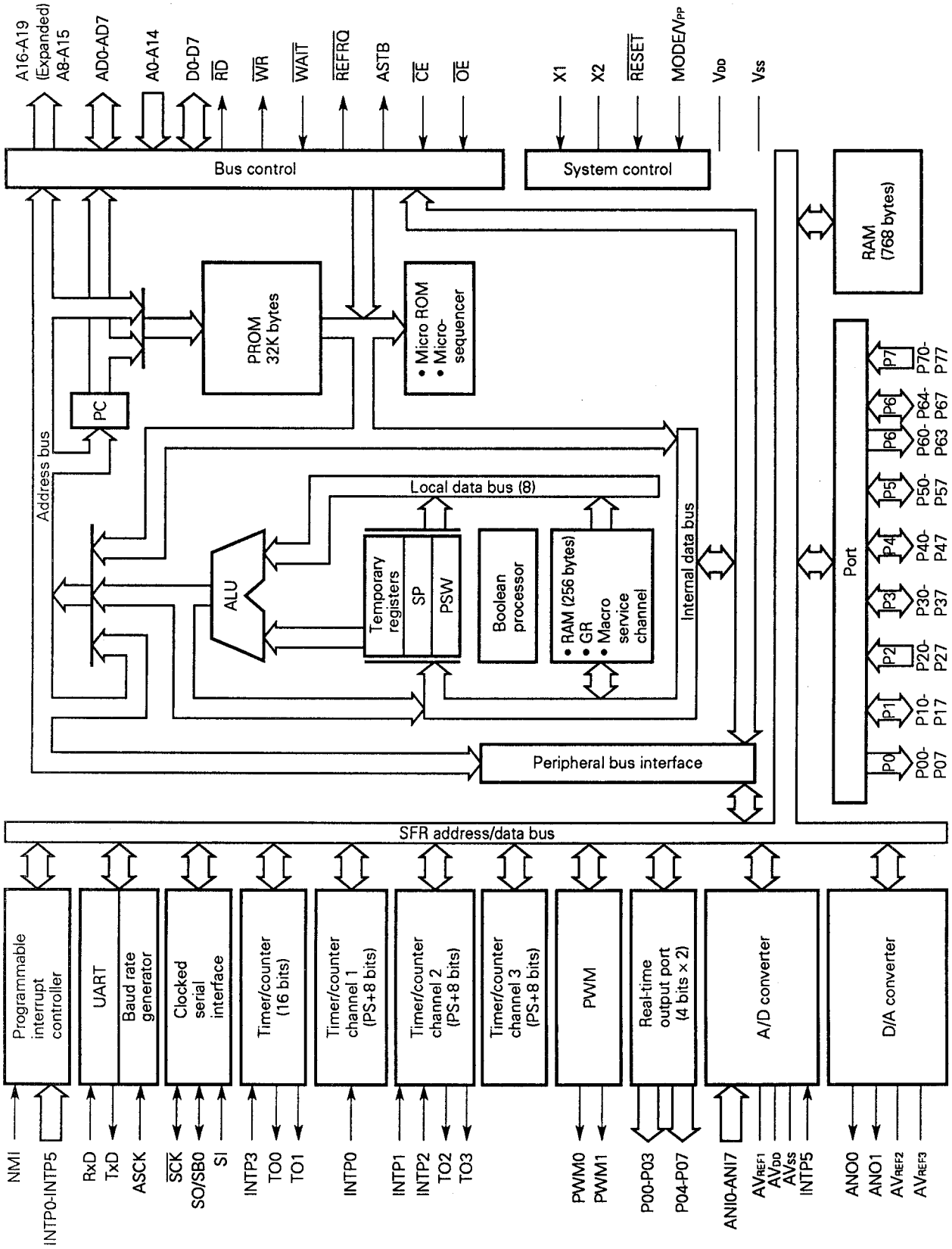
Caution L : Connect these pins separately to the Vss pins through pull-down resistors.
Vss : To be connected to the ground.
Open : Nothing should be connected on these pins.
RESET : Set a low-level input.

VPP : Programming power supply
RESET : Reset
A0-A14: Address bus
D0-D7 : Data bus
CE : Chip enable
OE : Output enable
VDD: Power supply
Vss: Ground

EXAMPLE OF SYSTEM CONFIGURATION (LASER BEAM PRINTER)



INTERNAL BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN THE μPD78P238 AND μPD78234/μPD78238

The μPD78P238 is produced by replacing the mask ROM in the μPD78238 with PROM on which data can be written. The functions of the μPD78P238 are the same as those of the μPD78238 except for the PROM specification such as writing and verification, and except that a ROM-less operation cannot be performed. Setting the internal memory select register (IMS) allows the PROM specification and the functions, except for the ROM-less operation, of the μPD78P238 to be the same as those of the μPD78234. Table 1-1 shows the differences between these products.

For the details of the CPU function and built-in hardware, refer to *μPD78234 User's Manual, Hardware* or other manuals.

Table 1-1 Differences between the μPD78P238 and μPD78234/μPD78238

Item	μPD78P238	μPD78238	μPD78234
Internal program memory	32K-byte PROM 16K bytes can also be selected by the IMS register.	32K-byte mask ROM	16K-byte mask ROM
Built-in RAM	1024 bytes: 640 bytes can also be selected by the IMS register.	1024 bytes	640 bytes
ROM-less operation	Impossible	Possible by setting the MODE pin to high.	
Package	80-pin plastic QFP (14 × 14 mm) 94-pin plastic QFP (20 × 20 mm) 84-pin plastic QFJ (1150 × 1150 mil)		
	94-pin ceramic WQFN (20 × 20 mm)	–	

2. PIN FUNCTIONS

2.1 PORT PINS

Pin	I/O	Dual-function	Function	
P00-P07	O	–	Port 0 (P0): Functions as a real-time output port (4 bits × 2). Can drive a transistor.	
P10	I/O	PWM0	Port 1 (P1): Inputs and outputs can be specified bit by bit. The use of the pull-up resistors can be specified by software for the pins in the input mode together. Can drive LED.	
P11		PWM1		
P12-P17		–		
P20	I	NMI	Port 2 (P2): P20 does not function as a general port (nonmaskable interrupt). However, the input level can be checked in an interrupt service routine. The use of the pull-up resistors can be specified by software for pins P22 to P27 (in units of 6 bits).	
P21		INTP0		
P22		INTP1		
P23		INTP2/CI		
P24		INTP3		
P25		INTP4/ASCK		
P26		INTP5		
P27		SI		
P30	I/O	RxD	Port 3 (P3): Inputs and outputs can be specified bit by bit. The use of the pull-up resistors can be specified by software for the pins in the input mode together.	
P31		TxD		
P32		$\overline{SCK}$		
P33		SO/SB0		
P34-P37		TO0-TO3		
P40-P47	I/O	AD0-AD7	Port 4 (P4): Inputs and outputs can be specified in units of 8 bits. The use of the pull-up resistors can be specified by software in units of 8 bits.	Can drive LED.
P50-P57	I/O	A8-A15	Port 5 (P5): Inputs and outputs can be specified bit by bit. The use of the pull-up resistors can be specified by software for the pins in the input mode together.	
P60-P63	O	A16-A19	Port 6 (P6): Inputs and outputs can be specified for P64-P67 bit by bit. The use of the pull-up resistors can be specified by software for pins P64 to P67 in the input mode together.	
P64	I/O	$\overline{RD}$		
P65		$\overline{WR}$		
P66		$\overline{WAIT}$		
P67		$\overline{REFRQ}$		
P70-P77	I	ANI0-ANI7	Port 7 (P7)	

2.2 NON-PORT PINS

Pin	I/O	Function	Dual-function
TO0-TO3	O	Timer output	P34-P37
CI	I	Input of a count clock for an 8-bit timer/counter 2	P23/INTP2
RxD	I	Serial data input (UART)	P30
TxD	O	Serial data output (UART)	P31
ASCK	I	Baud rate clock input (UART)	P25/INTP4
SB0	I/O	Serial data I/O (SBI)	P33/SO
SI	I	Serial data input (three-wire serial I/O)	P27
SO	O	Serial data output (three-wire serial I/O)	P33/SB0
$\overline{SCK}$	I/O	Serial clock I/O (SBI, three-wire serial I/O)	P32
NMI	I	External interrupt request	P20
INTP0			P21
INTP1			P22
INTP2			P23/CI
INTP3			P24
INTP4			P25/ASCK
INTP5			P26
AD0-AD7	I/O	Time multiplexing address/data bus (for connecting external memory)	P40-P47
A8-A15	O	High-order address bus (for connecting external memory)	P50-P57
A16-A19	O	High-order address bus during address expansion (for connecting external memory)	P60-P63
$\overline{RD}$	O	Strobe signal output for reading the contents of external memory	P64
$\overline{WR}$	O	Strobe signal output for writing on external memory	P65
$\overline{WAIT}$	I	Wait signal insertion	P66
ASTB	O	Latch timing output of time multiplexing address (A0-A7) (for connecting external memory)	–
$\overline{REFRQ}$	O	Refresh pulse output to external pseudostatic memory	P67
$\overline{RESET}$	I	Chip reset	–
X1	I	Crystal input for system clock generation (A clock pulse can also be input to the X1 pin.)	–
X2	–		
MODE	I	Specification of PROM operation Normally, low-level input	–
ANI0-ANI7	I	Analog voltage inputs for the A/D converter	P70-P77
ANO0, ANO1	O	Analog voltage outputs for the D/A converter	–
AV_{REF1}	–	Application of A/D converter reference voltage	–
AV_{REF2}, AV_{REF3}		Application of D/A converter reference voltage	
AV_{DD}		Positive power supply for the A/D converter	
AV_{SS}		Ground for the A/D converter	
V_{DD}		Positive power supply	
V_{SS}		Ground	
NC		Not connected internally	

2.3 PROM PROGRAMMING MODE ($V_{PP} \geq 5$ V, $\overline{RESET}$ = L)

2.3.1 List of Pin Functions

Pin	I/O	Function
V_{PP}	–	Setting the μPD78P238 to the PROM programming mode: High-voltage apply pin for writing or verifying a program
$\overline{RESET}$	I	PROM programming mode
A0 - A14		Address bus
D0 - D7	I/O	Data bus
$\overline{CE}$	I	PROM enable input or program pulse input
$\overline{OE}$		Read strobe input to PROM
V_{DD}	–	Positive power supply
V_{SS}		Ground

2.3.2 Pin Functions

(1) **V_{PP} (Programming power supply): Input**
Input pin for setting the μPD78P238 to the PROM programming mode. When the input voltage on this pin is 5 V or more and when $\overline{RESET}$ input goes low, the μPD78P238 the PROM programming mode. When $\overline{CE}$ is made low for V_{PP} = 12.5 V and $\overline{OE}$ = high, program data on D0 to D7 can be written into the internal PROM cell selected by A0 to A14.

(2) **$\overline{RESET}$: Input**
Input pin for setting the μPD78P238 to the PROM programming mode. When input on this pin is low, and when the input voltage on the V_{PP} pin goes 5 V or more, the μPD78P238 enters the PROM programming mode.

(3) **A0 to A14 (Address bus): Input**
Address bus that selects an internal PROM address (0000H to 7FFFH)

(4) **D0 to D7 (Data bus): I/O**
Data bus through which a program is written on or read from internal PROM

(5) **$\overline{CE}$ (Chip enable): Input**
This pin inputs the enable signal from internal PROM. When this signal is active, a program can be written or read.

(6) **$\overline{OE}$ (Output enable): Input**
This pin inputs the read strobe signal to internal PROM. When this signal is made active for $\overline{CE}$ = low, a one-byte program in the internal PROM cell selected A0 to A14 can be read onto D0 to D7.

(7) V_{DD}
Positive power supply pin

(8) V_{SS}
Ground potential pin

2.4 MEMORY MAPPING IN THE μPD78P238

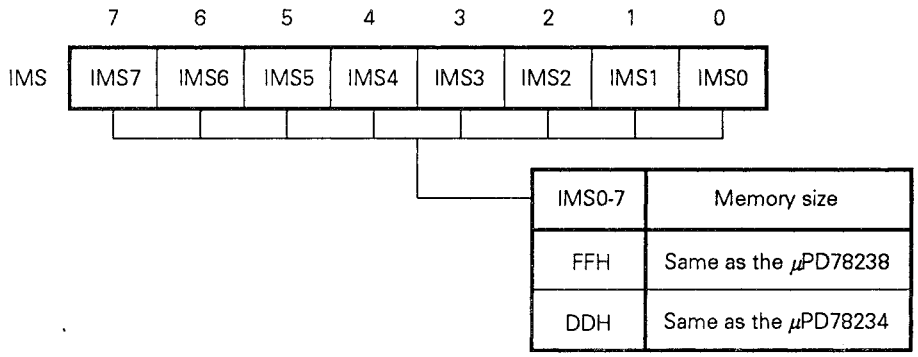
The μPD78P238 contains 32K-byte PROM and 1024-byte RAM. It differs a little in memory mapping from the μPD78234. To eliminate the difference, the μPD78P238 is provided with the memory-size change function to make part of internal memory unused by software.

A memory-size change register (IMS) is used to change the size of memory. To map memory into the μPD78P238 in the same way as the μPD78234, be sure to write on this register immediately after resetting the μPD78P238.

Writing on the IMS register is enabled by an 8-bit manipulation instruction. Fig. 2-1 shows the format of the register.

$\overline{\text{RESET}}$ input changes the size of memory in the μPD78P238 to FFH (the same size of memory as that in the μPD78238).

Fig. 2-1 Memory-Size Change Register (IMS)



IMS0-7	Memory size
FFH	Same as the μPD78238
DDH	Same as the μPD78234

Caution The μPD78234 and μPD78238 are not provided with this register. However, the write instruction to the register does not influence their operations.

3. PROGRAMMING IN THE μPD78P238

The program memory in the μPD78P238 is an electrically writable PROM of 32768 × 8 bits. Use the MODE/V_{PP} and $\overline{RESET}$ pins to set the μPD78P238 to the PROM programming mode when programming on the PROM. Other unused pins are handled as shown in pin configuration (2).

The μPD78P238 provides programming characteristics compatibility with the μPD27C256A[Note].

★ **Note** The μPD27C256A is not provided with the 100-μs program-pulse mode.

3.1 OPERATING MODE

When 5 V or more is applied to the MODE/V_{PP} pin and when a low-level pulse is applied to the $\overline{RESET}$ pin, the μPD78P238 enters the PROM programming mode. This mode varies to each operating mode shown in Table 3-1 according to how to set the $\overline{CE}$ and $\overline{OE}$ pins.

Setting the μPD78P238 to the read mode enables it to read the contents of PROM.

Table 3-1 Operating Modes for Programming on PROM

Mode / Pin	$\overline{RESET}$	MODE/V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	D0 to D7
Program write	L	+12.5 V	+6 V	L	H	Data input
Program verify				H	L	Data output
Program inhibit				H	H	High impedance
Read		+5 V	+5 V	L	L	Data output
Output disable				L	H	High impedance
Standby				H	L/H	High impedance

Caution Do not set both $\overline{CE}$ and $\overline{OE}$ to L when MODE/V_{PP} is set to +12.5 V and V_{DD} to +6 V.

3.2 PROCEDURE FOR WRITING ON PROM

The following is a procedure for writing on PROM. Data can be written at high speed.

(1) Always set the $\overline{\text{RESET}}$ pin to low. Apply +5 V to the MODE/V_{PP} pin. Connect other unused pins as shown in **pin configuration (2)**.
(2) Apply +6 V to the V_{DD} pin and +12.5 V to the MODE/V_{PP} pin.
(3) Set an initial address.
(4) Input write data.
(5) Input a 1 ms program pulse (active low) to the $\overline{\text{CE}}$ pin.
(6) Verify mode: If data are written, go to step (8); if not, repeats steps (4) to (6). If no data are written yet after they are repeated 25 times, go to step (7).
(7) Assume the device to be defective and stop write operation.
(8) Input write data and a program pulse of (number of times steps (4) to (6) were repeated) × 3 ms (additional writing).
(9) Increment the address.
(10) Repeat steps (4) to (9) until the address exceeds the last address.

Fig. 3-1 is a timing chart of these steps (2) to (8).

Fig. 3-1 PROM Write/Verify Timing Chart

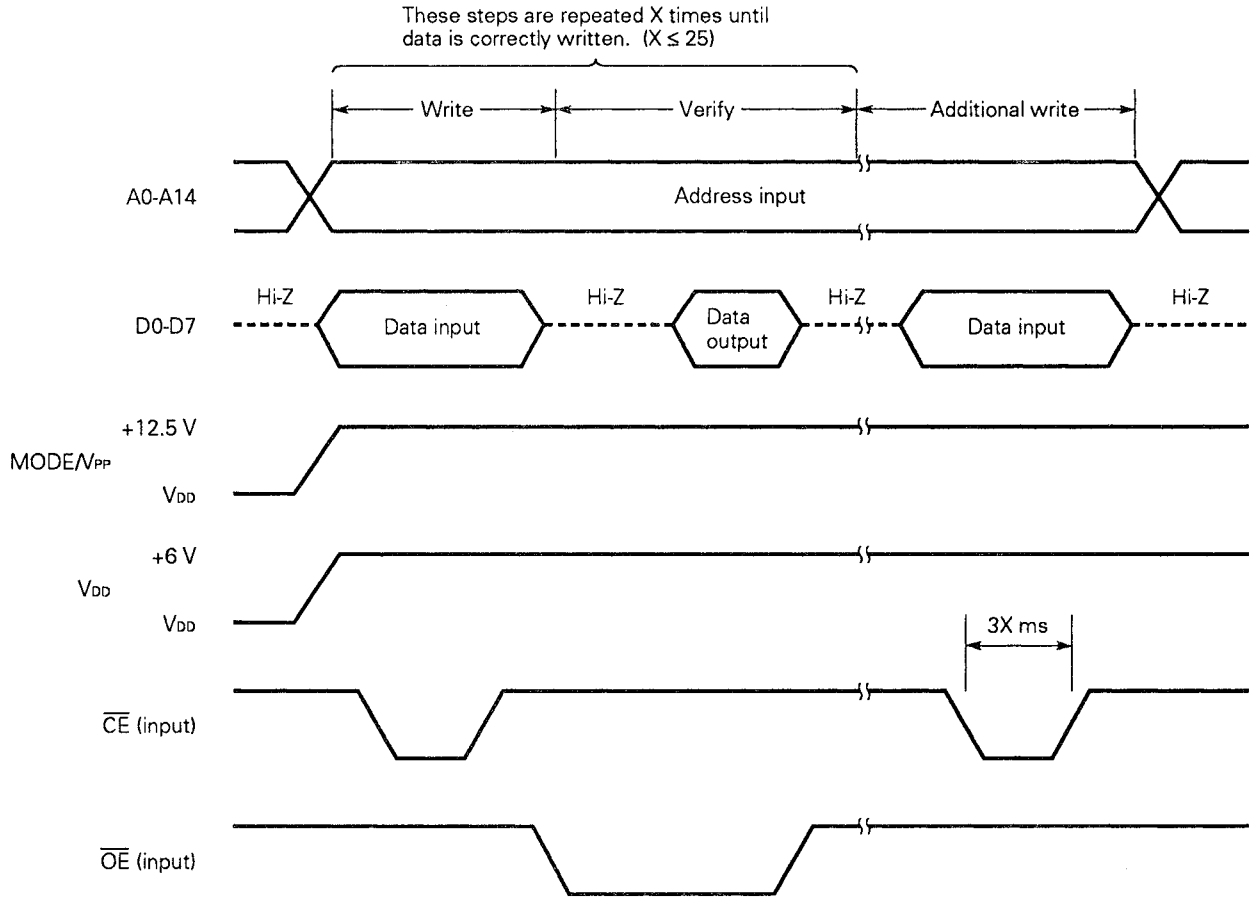
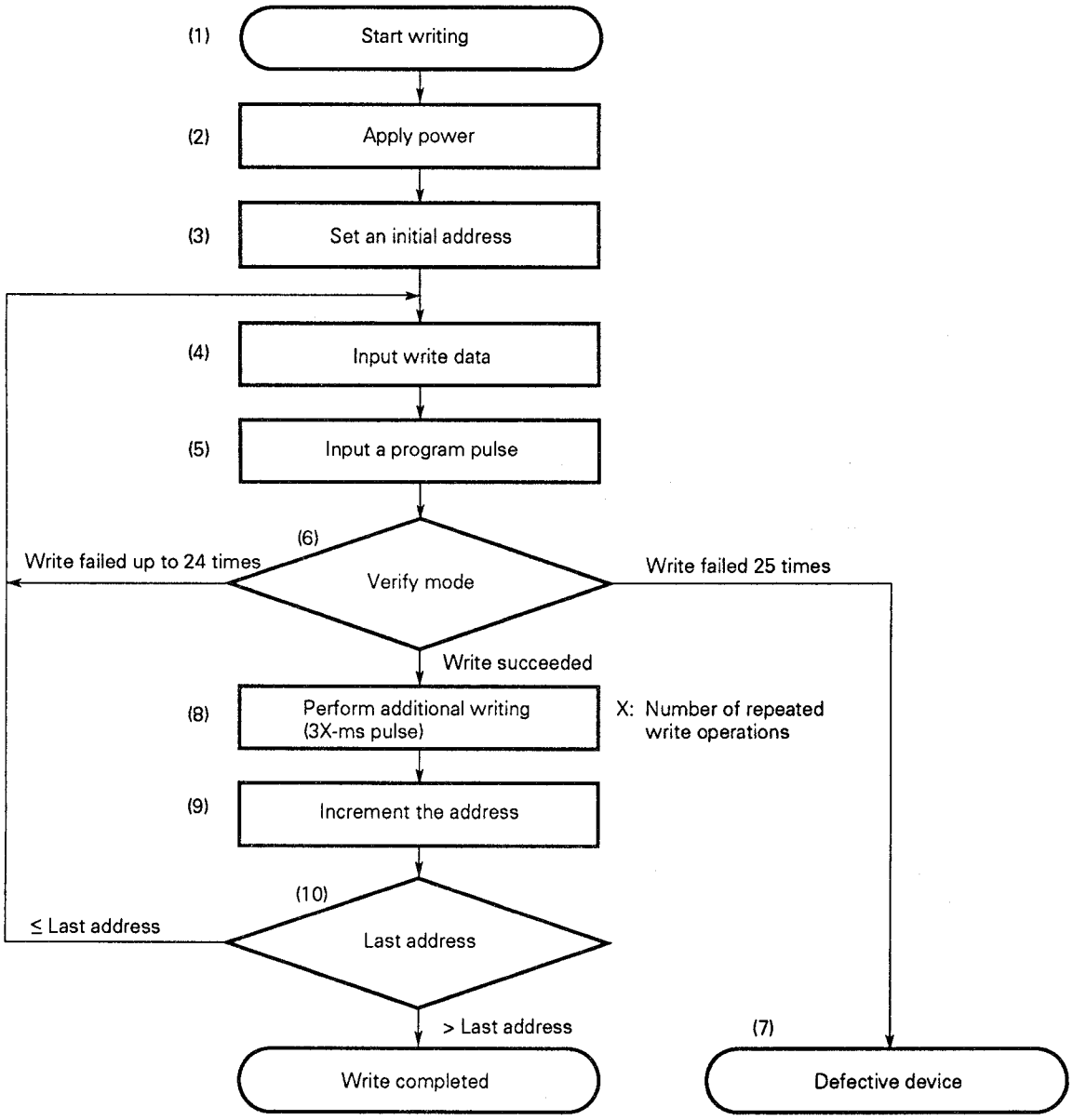


Fig. 3-2 Flowchart of Procedure for Writing



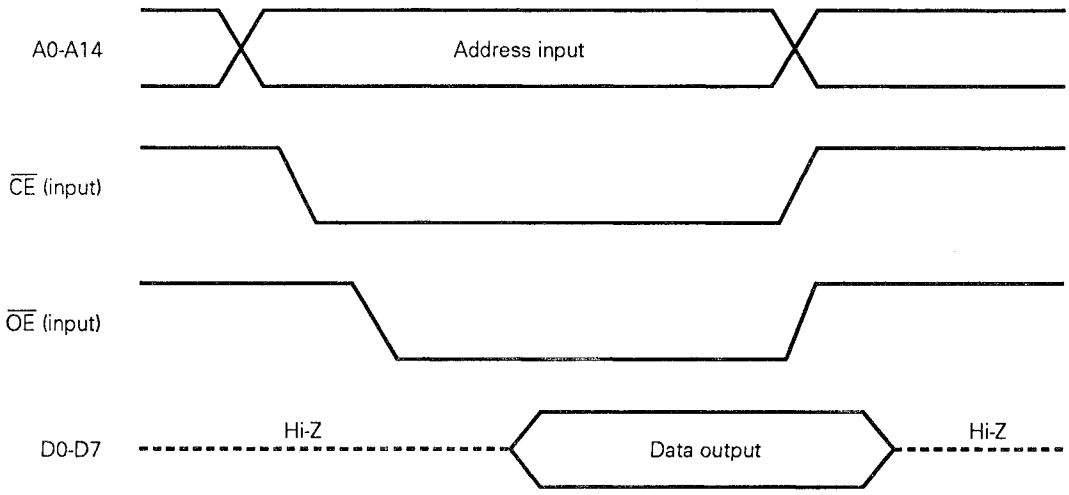
3.3 PROCEDURE FOR READING FROM PROM

The contents of PROM can be read out to the external data bus (D0 to D7) in the following steps:

(1) Always set the $\overline{\text{RESET}}$ pin to low. Apply +5 V to the MODE/V_{PP} pin. Connect other unused pins as shown in **pin configuration (2)**.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of data to be read into the A0 to A14 pins.
(4) Read mode
(5) Output the data on the D0 to D7 pins.

Fig. 3-3 is a timing chart of these steps (2) to (5).

Fig. 3-3 PROM Read Timing Chart



4. ERASURE CHARACTERISTICS ONLY FOR THE μPD78P238KF

The programmed data (FFH) of the μPD78P238KF can be erased by exposure to light with a wavelength less than approx. 400 nm.

To erase the contents of program memory in the μPD78P238KF, expose the erasure window to ultraviolet light with the wavelength of 254 nm. The amount of light required to completely erase the contents of program memory is a minimum of 15 W•s/cm^2 (intensity of ultraviolet light × erasing time). It takes about 15 to 20 minutes to expose the erasure window to a 12,000 μW/cm^2 ultraviolet lamp. It may, however, take more time due to the fallen performance of this ultraviolet lamp, dirt on the package window, or suchlike. Note that the μPD78P238KF should be placed less than 2.5 cm from the ultraviolet lamp during erasure. In addition, if a filter is attached to the ultraviolet lamp, remove the filter before erasure.

5. PROTECTIVE FILM COVERING THE ERASURE WINDOW ONLY FOR THE μPD78P238KF

The erasure window should be covered with a protective film when not erasing the contents of EPROM to prevent erroneously erasing the contents of memory by exposure to light other than that of the lamp for erasing the contents of the EPROM, and to prevent internal circuits other than the EPROM from malfunctioning due to the light.

6. SCREENING ONE-TIME PROM PRODUCTS

NEC cannot execute a complete test of one-time PROM products (μPD78P238GC-3B9, μPD78P238GJ-5BG, and μPD78P238LQ) due to their structure before shipment. It is recommended that you screen (verify) PROM products after writing necessary data into them and storing them at 125 °C for 24 hours.

NEC offers a charged service called QTOP microcomputer service. This service includes writing to one-time PROM, marking, screening, and verification.

Ask your sales representative for details.

7. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AVss to V_{DD} +0.5	V
	AVss		−0.5 to +0.5	V
Input voltage	V_{I1}		−0.5 to V_{DD} +0.5	V
	V_{I2}	MODE/V_{PP} and P21/INTP0/A9 pins in the PROM programming mode	−0.5 to +13.5	V
Output voltage	V_O		−0.5 to V_{DD} +0.5	V
Low-level output current	I_{OL}	1 pin	15	mA
		Total of all output pins	100	mA
High-level output current	I_{OH}	1 pin	−10	mA
		Total of all output pins	−50	mA
A/D converter reference input voltage	AV_{REF1}		−0.5 to V_{DD} +0.3	V
D/A converter reference input voltage	AV_{REF2}		−0.5 to V_{DD} +0.3	V
	AV_{REF3}		−0.5 to V_{DD} +0.3	V
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values. ★

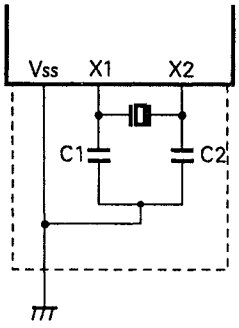
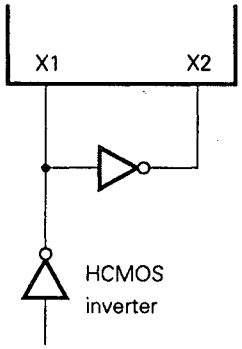
OPERATING CONDITIONS

Clock frequency	Operating temperature (T_{opt})	Supply voltage (V_{DD})
4 MHz ≤ fxx ≤ 12 MHz	−40 to +85 °C	+5.0 V ±10 %

CAPACITANCE (T_a = 25 °C, V_{DD} = Vss = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_I	f = 1 MHz 0 V on pins other than measured pins			20	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

OSCILLATOR CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +5 V ±10 %, Vss = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Ceramic resonator or crystal		Oscillator frequency (fxx)	4	12	MHz
External clock		X1 input frequency (fx)	4	12	MHz
		X1 input rising and falling times (t_{XR}, t_{XF})	0	30	ns
		X1 input high-level and low-level widths (t_{WXH}, t_{WXL})	30	130	ns

Caution When the clock oscillator is used, conform to the following guidelines when wiring at the portions surrounded by dotted lines in the figure above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas.**
- **Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of Vss. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = AV_{DD} = +5 V ±10 %, Vss = AVss = 0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	Pins other than those shown in **Note 1**		2.2		V_{DD}	V
	V_{IH2}	Pins shown in **Note 1**		0.8V_{DD}		V_{DD}	V
Low-level output voltage	V_{OL1}	I_{OL} = 2.0 mA				0.45	V
	V_{OL2}	I_{OL} = 8.0 mA **Note 2**				1.0	V
High-level output voltage	V_{OH1}	I_{OH} = −1.0 mA		V_{DD} − 1.0			V
	V_{OH2}	I_{OH} = −100 μA		V_{DD} − 0.5			V
	V_{OH3}	I_{OH} = −5.0 mA **Note 3**		2.0			V
X1 low-level input current	I_{IL}	0 V ≤ V_I ≤ V_{IL}				−100	μA
X1 high-level input current	I_{IH}	V_{IH2} ≤ V_I ≤ V_{DD}				100	μA
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD}				±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operating mode, fxx = 12 MHz			20	40	mA
	I_{DD2}	HALT mode, fxx = 12 MHz			7	20	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5		5.5	V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V			10	μA
			V_{DDDR} = 5 V ±10 %			20	μA
Pull-up resistor	R_L	V_I = 0 V		15	40	80	kΩ

Notes 1. Pins X1, X2, $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, and MODE

2. Pins P10-P17, P40/AD0-P47/AD7, and P50/A8-P57/A15
3. Pins P00-P07

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = AV_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Read/write operation (1/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
X1 input clock cycle time	t_{CYX}		82	250	ns
Address setup time (referred to ASTB↓)	t_{SAST}*		52		ns
Address hold time (referred to ASTB↓) Note	t_{HSTA}		25		ns
Address hold time (referred to $\overline{RD}$↑)	t_{HRA}		30		ns
Address hold time (referred to $\overline{WR}$↑)	t_{HWA}		30		ns
Delay from address to $\overline{RD}$↓	t_{DAR}*		129		ns
Address float time (referred to $\overline{RD}$↓)	t_{FAR}*		11		ns
Delay from address to data input	t_{DAID}*	The number of wait cycles = 0		228	ns
Delay from ASTB↓ to data input	t_{DSTID}*	The number of wait cycles = 0		181	ns
Delay from $\overline{RD}$↓ to data input	t_{DRID}*	The number of wait cycles = 0		99	ns
Delay from ASTB↓ to $\overline{RD}$↓	t_{DSTR}*		52		ns
Data hold time (referred to $\overline{RD}$↑)	t_{HRID}		0		ns
Delay from $\overline{RD}$↑ to address active	t_{DRA}*		124		ns
Delay from $\overline{RD}$↑ to ASTB↑	t_{DRST}*		124		ns
$\overline{RD}$ low-level width	t_{WRL}*	The number of wait cycles = 0	124		ns
ASTB high-level width	t_{WSTH}*		52		ns
Delay from address to $\overline{WR}$↓	t_{DAW}*		129		ns
Delay from ASTB↓ to data output	t_{DSTOD}*			142	ns
Delay from $\overline{WR}$↓ to data output	t_{DWOD}			60	ns
★ Delay from ASTB↓ to $\overline{WR}$↓	t_{DSTW1}*	When refresh is inhibited	52		ns
	t_{DSTW2}*	When refresh is allowed	129		ns
Data setup time (referred to $\overline{WR}$↑)	t_{SODWR}*	The number of wait cycles = 0	146		ns
Data setup time (referred to $\overline{WR}$↓)	t_{SODWF}*	When refresh is allowed	22		ns
Data hold time (referred to $\overline{WR}$↑) Note	t_{HWOD}		20		ns
Delay from $\overline{WR}$↑ to ASTB↑	t_{DWST}*		42		ns

Note The hold time includes the time for holding V_{OH} and V_{OL} on the load conditions of C_L = 100 pF and R_L = 2 kΩ.

Remarks 1. The values listed in the above table are obtained when fxx = 12 MHz and C_L = 100 pF.

2. See **t_{CYX}-dependent bus timing definition** for additional information about the parameters with an asterisk in the symbol column.

Read/write operation (2/2)

Parameter		Symbol	Conditions	Min.	Max.	Unit
$\overline{WR}$ low-level width		t_{WWL1}*	When refresh is inhibited The number of wait cycles = 0	196		ns ★
		t_{WWL2}*	When refresh is allowed The number of wait cycles = 0	114		ns
Delay from address to $\overline{WAIT}$↓ input		t_{DAWT}*			146	ns
Delay from ASTB↓ to $\overline{WAIT}$↓ input		t_{DSTWT}*			84	ns
Hold time from ASTB↓ to $\overline{WAIT}$		t_{HSTWT}*	The number of external cycles = 1	174		ns
Delay from ASTB↓ to $\overline{WAIT}$↑		t_{DSTWTH}*	The number of external cycles = 1		273	ns
Delay from $\overline{RD}$↓ to $\overline{WAIT}$↓ input		t_{DRWTL}*			22	ns
Hold time from $\overline{RD}$↓ to $\overline{WAIT}$		t_{HRWT}*	The number of external cycles = 1	87		ns
Delay from $\overline{RD}$↓ to $\overline{WAIT}$↑		t_{DRWTH}*	The number of external cycles = 1		186	ns
Delay from $\overline{WAIT}$↑ to data input		t_{DWTID}*			62	ns
Delay from $\overline{WAIT}$↑ to $\overline{WR}$↑		t_{DWTW}*		154		ns
Delay from $\overline{WAIT}$↑ to $\overline{RD}$↑		t_{DWTR}*		72		ns
Delay from $\overline{WR}$↓ to $\overline{WAIT}$ input (when refresh is inhibited)		t_{DWWTL}*			22	ns
Hold time from $\overline{WR}$↓ to $\overline{WAIT}$	When refresh is inhibited	t_{HWWT1}*	The number of external cycles = 1	87		ns
	When refresh is allowed	t_{HWWT2}*	The number of external cycles = 1	5		ns
Delay from $\overline{WR}$↓ to $\overline{WAIT}$↑	When refresh is inhibited	t_{DWWTH1}*	The number of external cycles = 1		186	ns
	When refresh is allowed	t_{DWWTH2}*	The number of external cycles = 1		104	ns
Delay from $\overline{RD}$↑ to $\overline{REFRQ}$↓		t_{DRRFQ}*		154		ns
Delay from $\overline{WR}$↑ to $\overline{REFRQ}$↓		t_{DWRFQ}*		72		ns
$\overline{REFRQ}$ low-level width		t_{WRFQL}*		120		ns
Delay from $\overline{REFRQ}$↑ to ASTB↑		t_{DRFQST}*		280		ns

Remarks 1. The values listed in the above table are obtained when fxx = 12 MHz and C_L = 100 pF.

2. See **t_{CYX}-dependent bus timing definition** for additional information about the parameters with an asterisk in the symbol column.

Serial operation

Parameter	Symbol	Conditions		Min.	Max.	Unit
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		μs
		Output	Internal clock divided by 16	1.3		μs
			Internal clock divided by 64	5.3		μs
Serial clock low-level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internal clock divided by 16	556		ns
			Internal clock divided by 64	2.5		μs
Serial clock high-level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internal clock divided by 16	556		ns
			Internal clock divided by 64	2.5		μs
SI, SB0 setup time (referred to $\overline{SCK}$↑)	t_{SSSK}			150		ns
SI, SB0 hold time (referred to $\overline{SCK}$↑)	t_{HSSK}			400		ns
SO/SB0 output delay time (referred to $\overline{SCK}$↓)	t_{DSBSK1}	CMOS push-pull output (three-wire serial I/O mode)		0	300	ns
	t_{DSBSK2}	Open-drain output (SBI mode), R_L = 1 kΩ		0	800	ns
SB0 high hold time (referred to $\overline{SCK}$↑)	t_{HSBSK}	SBI mode		4		t_{CYX}
SB0 low setup time (referred to $\overline{SCK}$↓)	t_{SSBSK}			4		t_{CYX}
SB0 low-level width	t_{WSBL}			4		t_{CYX}
SB0 high-level width	t_{WSBH}			4		t_{CYX}

Remark The values listed in the above table are obtained when f_{XX} = 12 MHz and C_L = 100 pF.

Other operations

Parameter	Symbol	Conditions	Min.	Max.	Unit
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0-INTP5 low-level width	t_{WITL}		24		t_{CYX}
INTP0-INTP5 high-level width	t_{WITH}		24		t_{CYX}
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		10		μs

External clock timing

Parameter	Symbol	Conditions	Min.	Max.	Unit
X1 input low-level width	t_{WXL}		30	130	ns
X1 input high-level width	t_{WXH}		30	130	ns
X1 input rising time	t_{XR}		0	30	ns
X1 input falling time	t_{XF}		0	30	ns
X1 input clock cycle time	t_{CYX}		82	250	ns

A/D CONVERTER CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = AV_{DD} = +5 V ±10 %, Vss = AVss = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution			8			bit
Total error **Note 1**		4.0 V ≤ AV_{REF1} ≤ AV_{DD} T_a = −10 to +70 °C			0.4	%
		3.4 V ≤ AV_{REF1} ≤ AV_{DD}			0.8	%
		4.0 V ≤ AV_{REF1} ≤ AV_{DD}			0.6	%
Quantizing error					±1/2	LSB
Conversion time	t_{CONV}	When the FR bit in ADM is 0	360			t_{CYX}
		When the FR bit in ADM is 1	240			t_{CYX}
Sampling time	t_{SAMP}	When the FR bit in ADM is 0	72			t_{CYX}
		When the FR bit in ADM is 1	48			t_{CYX}
Analog input voltage	V_{IAN}		−0.3		AV_{REF1} + 0.3	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF1}		3.4		AV_{DD}	V
AV_{REF} current	AI_{REF1}	f_{XX} = 12 MHz		1.5	3.0	mA
		Note 2		0.7	1.5	mA
AV_{DD} supply current	AI_{DD1}	f_{XX} = 12 MHz		1.4	3.0	mA
	AI_{DD2}	**Note 3**		10	20	μA

Notes 1. Quantizing error is excluded. The total error is represented in percent with respect to a full-scale value.

2. When the CS bit in the ADM register is set to 0.
3. When the CS bit in the ADM register is set to 0 in the STOP mode.

D/A CONVERTER CHARACTERISTICS (T_a = −40 to +85 °C, AV_{REF2} = V_{DD} = AV_{DD} = +5 V ±10 %, AV_{REF3} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution					8	bit
Total error		Load condition: 4 MΩ, 30 pF			0.4	%
		Load condition: 2 MΩ, 30 pF			0.6	%
		AV_{REF2} = 0.75V_{DD}, AV_{REF3} = 0.25V_{DD} Load condition: 4 MΩ, 30 pF			0.6	%
		AV_{REF2} = 0.75V_{DD}, AV_{REF3} = 0.25V_{DD} Load condition: 2 MΩ, 30 pF			0.8	%
Settling time		Load condition: 2 MΩ, 30 pF			10	μs
Output resistor	R_O	**Note**		20		kΩ
Analog reference voltage	AV_{REF2}		0.75V_{DD}		V_{DD}	V
Analog reference voltage	AV_{REF3}		0		0.25V_{DD}	V
Reference supply input current	AI_{REF2}		0		5	mA
Reference supply input current	AI_{REF3}		−5		0	mA

Note When DACS0 and DACS1 are set to 7FH.

tCYX-dependent bus timing definition (1/2)

Parameter	Symbol	Calculation formula	Min./Max.	12 MHz	Unit	
X1 input clock cycle time	tCYX		Min.	82	ns	
Address setup time (referred to ASTB↓)	tSAST	tCYX – 30	Min.	52	ns	
Delay from address to $\overline{RD}$↓	tDAR	2tCYX – 35	Min.	129	ns	
Address float time (referred to $\overline{RD}$↓)	tFAR	tCYX/2 – 30	Min.	11	ns	
Delay from address to data input	tDAID	(4 + 2n)tCYX – 100	Max.	228 Note	ns	
Delay from ASTB↓ to data input	tDSTID	(3 + 2n)tCYX – 65	Max.	181 Note	ns	
Delay from $\overline{RD}$↓ to data input	tDRID	(2 + 2n)tCYX – 64	Max.	100 Note	ns	
Delay from ASTB↓ to $\overline{RD}$↓	tDSTR	tCYX – 30	Min.	52	ns	
Delay from $\overline{RD}$↑ to address active	tDRA	2tCYX – 40	Min.	124	ns	
Delay from $\overline{RD}$↑ to ASTB↑	tDRST	2tCYX – 40	Min.	124	ns	
$\overline{RD}$ low-level width	tWRL	(2 + 2n)tCYX – 40	Min.	124 Note	ns	
ASTB high-level width	tWSTH	tCYX – 30	Min.	52	ns	
Delay from address to $\overline{WR}$↓	tDAW	2tCYX – 35	Min.	129	ns	
Delay from ASTB↓ to data output	tDSTOD	tCYX + 60	Max.	142	ns	
Delay from ASTB↓ to $\overline{WR}$↓	tDSTW1	tCYX – 30 (When refresh is inhibited)	Min.	52	ns	★
	tDSTW2	2tCYX – 35 (When refresh is allowed)	Min.	129	ns	
Data setup time (referred to $\overline{WR}$↑)	tSODWR	(3 + 2n)tCYX – 100	Min.	146 Note	ns	
Data setup time (referred to $\overline{WR}$↓)	tSODWF	tCYX – 60 (When refresh is allowed)	Min.	22	ns	
Delay from $\overline{WR}$↑ to ASTB↑	tDWST	tCYX – 40	Min.	42	ns	
$\overline{WR}$ low-level width	tWWL1	(3 + 2n)tCYX – 50 (When refresh is inhibited)	Min.	196 Note	ns	★
	tWWL2	(2 + 2n)tCYX – 50 (When refresh is allowed)	Min.	114 Note	ns	
Delay from address to $\overline{WAIT}$↓ input	tDAWT	3tCYX – 100	Max.	146	ns	
Delay from ASTB↓ to $\overline{WAIT}$↓ input	tDSTWT	2tCYX – 80	Max.	84	ns	

Remark n represents the number of wait cycles.

Note When n = 0

tcyx-dependent bus timing definition (2/2)

Parameter		Symbol	Calculation formula	Min./Max.	12 MHz	Unit
Hold time from ASTB↓ to $\overline{WAIT}$		tHSTWT	2Xtcyx + 10	Min.	174 Note	ns
Delay from ASTB↓ to $\overline{WAIT}$↑		tDSTWTH	2(1 + X)tcyx – 55	Max.	273 Note	ns
Delay from $\overline{RD}$↓ to $\overline{WAIT}$↓ input		tDRWTL	tcyx – 60	Max.	22	ns
Hold time from $\overline{RD}$↓ to $\overline{WAIT}$		tHRWT	(2X – 1)tcyx + 5	Min.	87 Note	ns
Delay from $\overline{RD}$↓ to $\overline{WAIT}$↑ delay		tDRWTH	(2X + 1)tcyx – 60	Max.	186 Note	ns
Delay from $\overline{WAIT}$↑ to data input		tDWTID	tcyx – 20	Max.	62	ns
Delay from $\overline{WAIT}$↑ to $\overline{WR}$↑		tDWTW	2tcyx – 10	Min.	154	ns
Delay from $\overline{WAIT}$↑ to $\overline{RD}$↑		tDWTR	tcyx – 10	Min.	72	ns
Delay from $\overline{WR}$↓ to $\overline{WAIT}$ input (when refresh is inhibited)		tDWWTL	tcyx – 60	Max.	22	ns
Hold time from $\overline{WR}$↓ to $\overline{WAIT}$	When refresh is inhibited	tHWWT1	(2X – 1)tcyx + 5	Min.	87 Note	ns
	When refresh is allowed	tHWWT2	2(X – 1)tcyx + 5	Min.	5 Note	ns
Delay from $\overline{WR}$↓ to $\overline{WAIT}$↑	When refresh is inhibited	tDWWTH1	(2X +1)tcyx – 60	Max.	186 Note	ns
	When refresh is allowed	tDWWTH2	2Xtcyx – 60	Max.	104 Note	ns
Delay from $\overline{RD}$↑ to $\overline{REFRQ}$↓		tDRRFQ	2tcyx – 10	Min.	154	ns
Delay from $\overline{WR}$↑ to $\overline{REFRQ}$↓		tDWRFQ	tcyx – 10	Min.	72	ns
$\overline{REFRQ}$ low-level width		tWRFQL	2tcyx – 44	Min.	120	ns
Delay from $\overline{REFRQ}$↑ to ASTB↑		tDRFQST	4tcyx – 48	Min.	280	ns

Remarks 1. X: External wait cycle (1, 2, ···)

2. tcyx ≒ 82 ns (fxx = 12 MHz)

3. n represents the number of wait cycles.

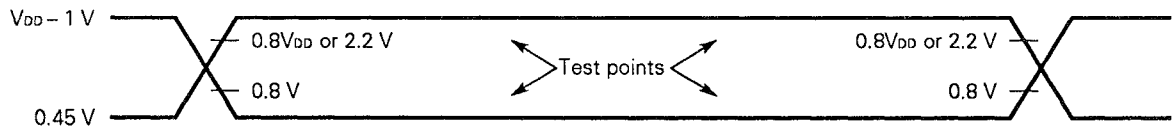
Note When X = 1

DATA RETENTION CHARACTERISTICS (T_a = −40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.5 V			10	μA
		V_{DDDR} = 5 V ±10 %			20	μA
V_{DD} rising time	t_{RVD}		200			μs
V_{DD} falling time	t_{FVD}		200			μs
V_{DD} hold time (referred to STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation settling wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-level input voltage	V_{IL}	Specified pins **Note**	0		$0.1V_{DDDR}$	V
High-level input voltage	V_{IH}		$0.9V_{DDDR}$		V_{DDDR}	V

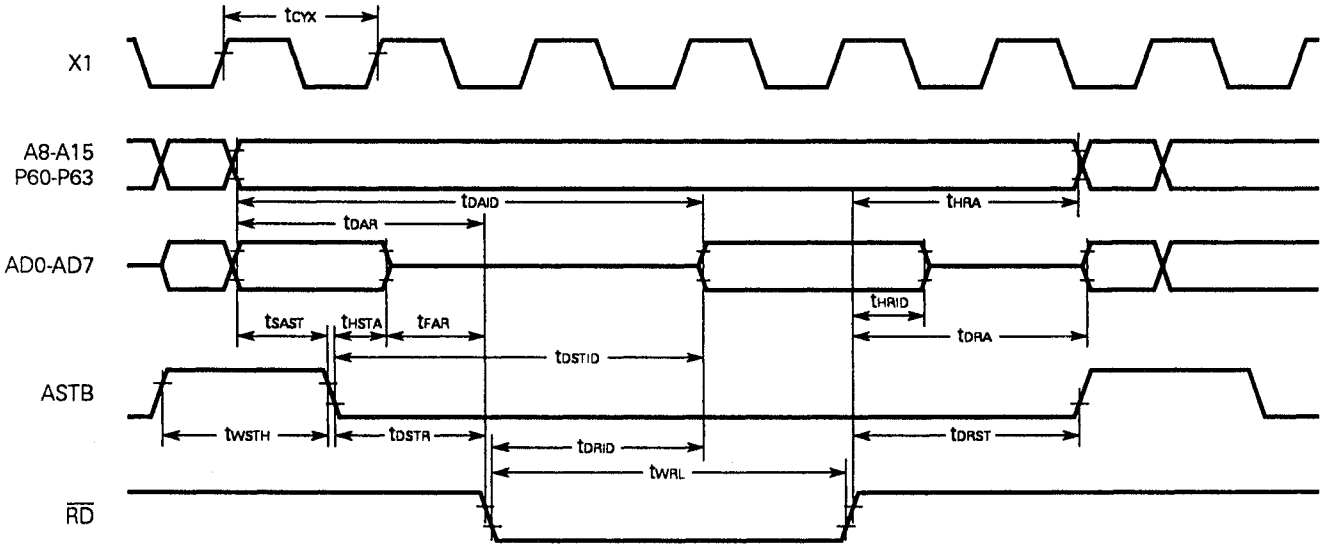
Note Pins $\overline{\text{RESET}}$, MODE, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{\text{SCK}}$, and P33/SO/SB0

AC Timing Test Points

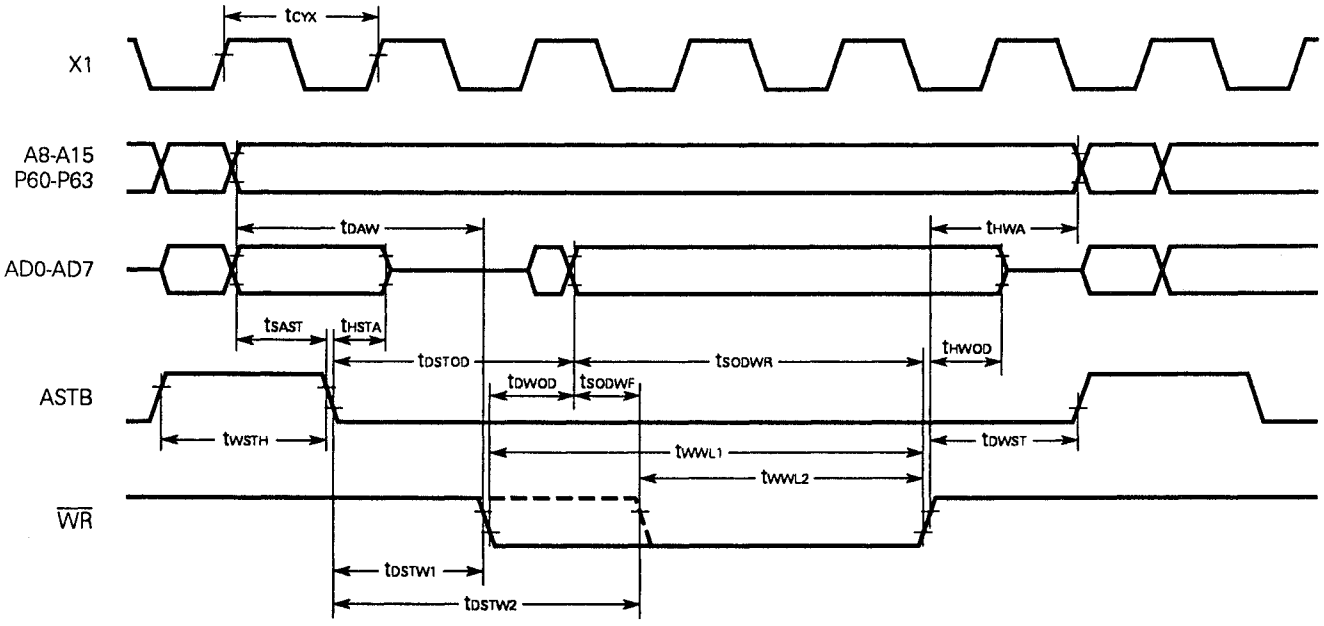


Timing Waveform

Read operation:

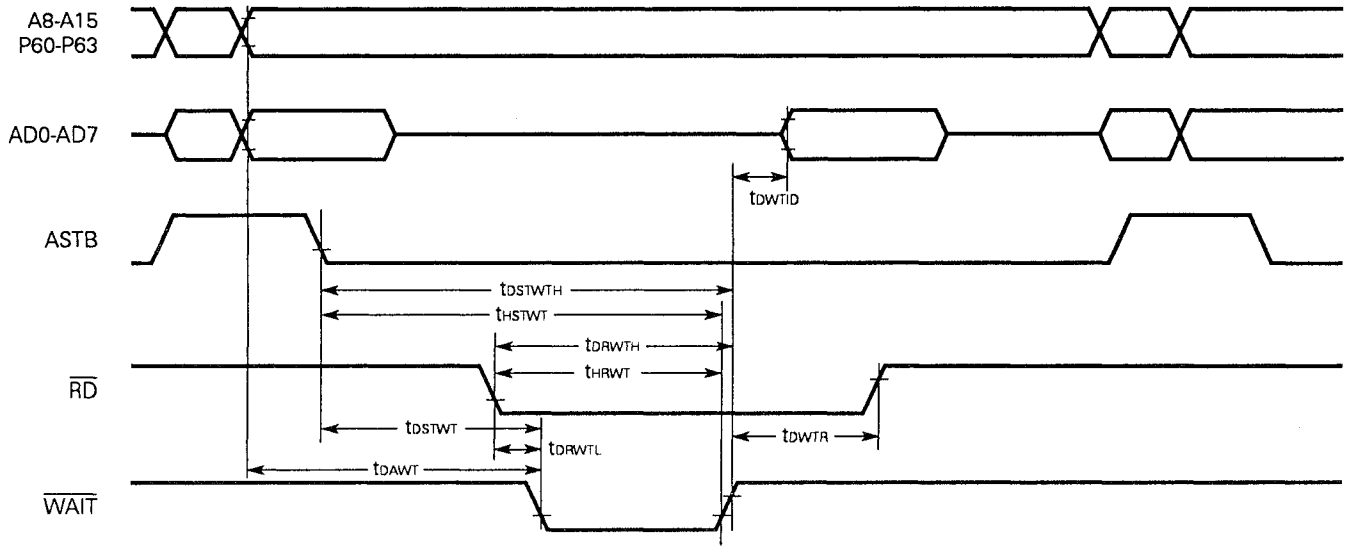


Write operation:

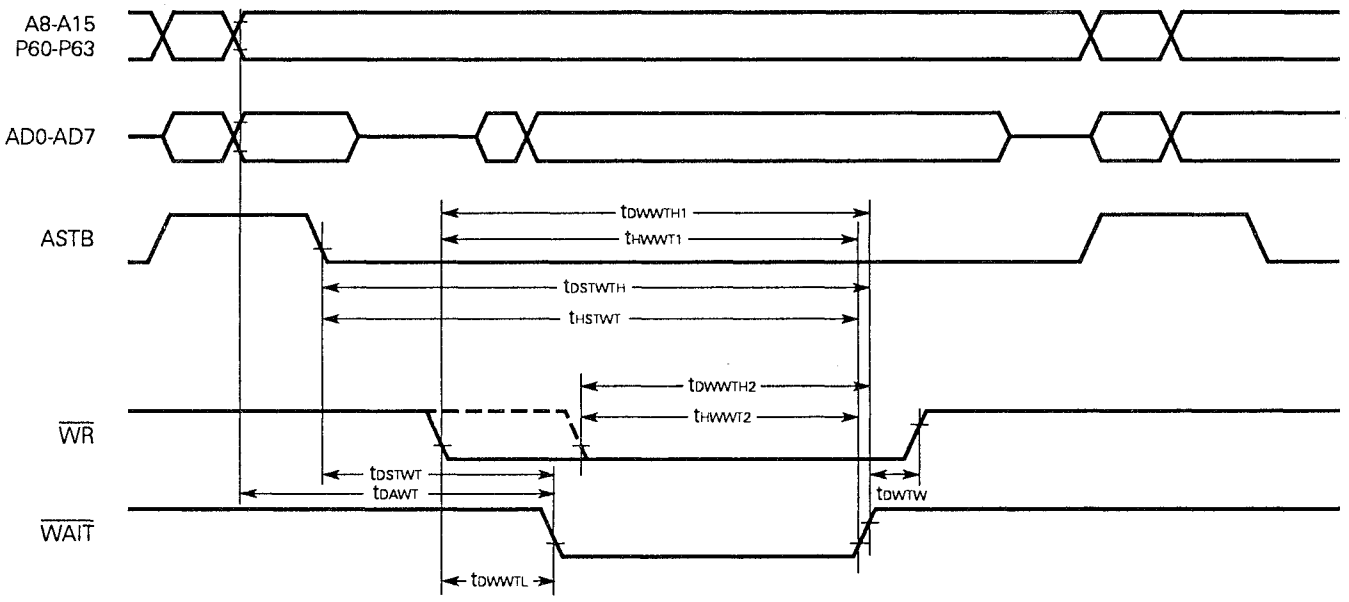


External WAIT Signal Input Timing

Read operation: ★

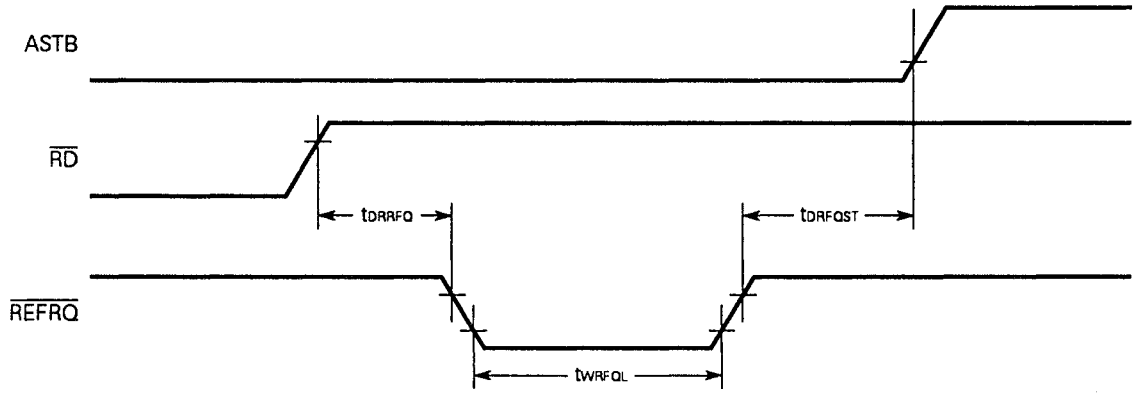


Write operation:

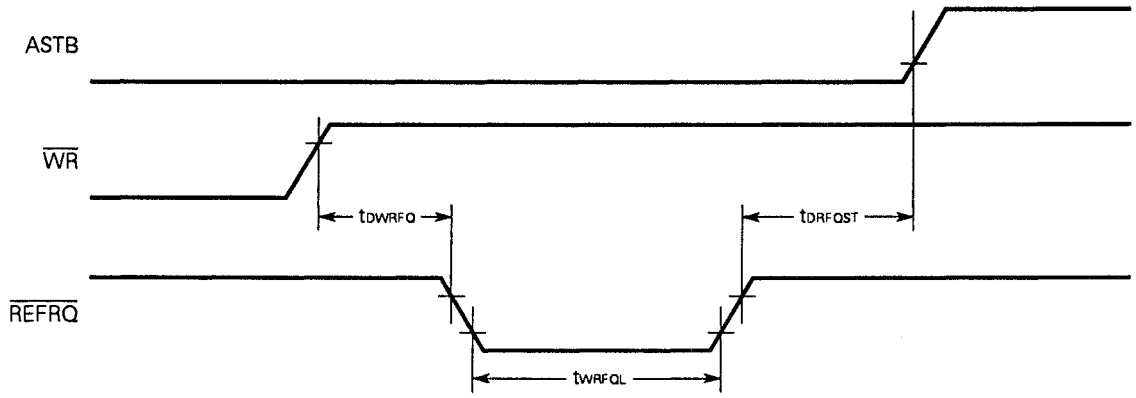


Timing Waveform for Refresh

Refresh after reading:

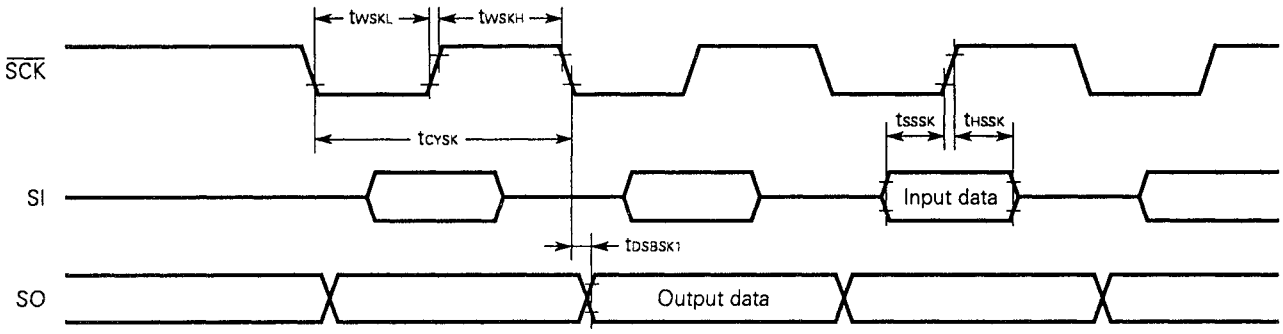


Refresh after writing:



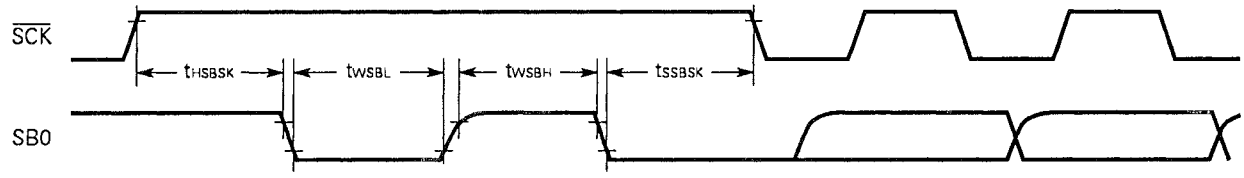
Serial Operation

Three-wire serial I/O mode:

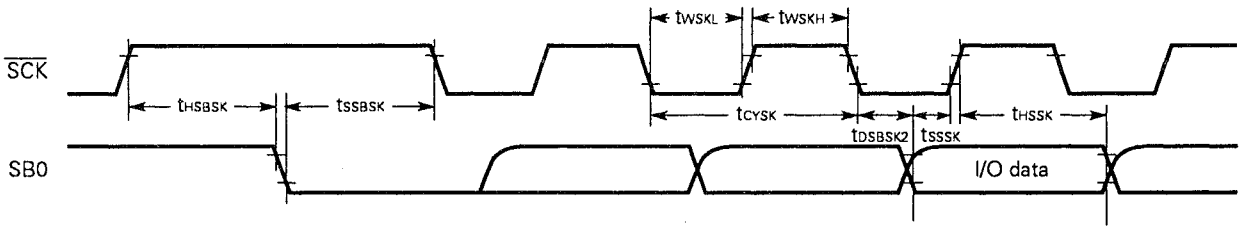


SBI Mode

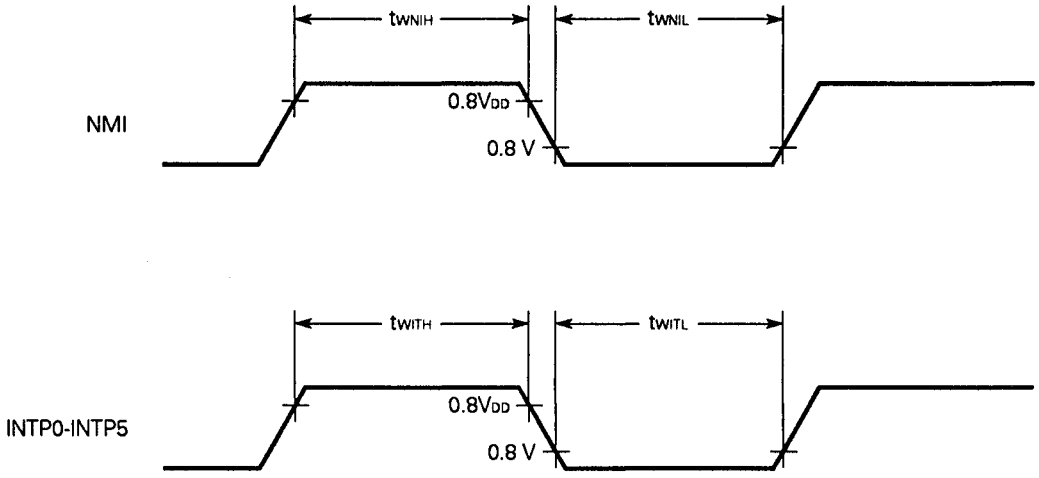
Bus release signal transfer:



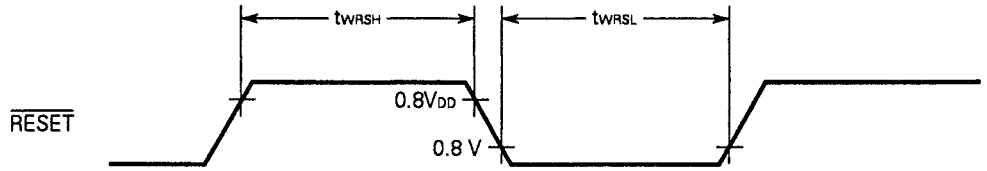
Command signal transfer:



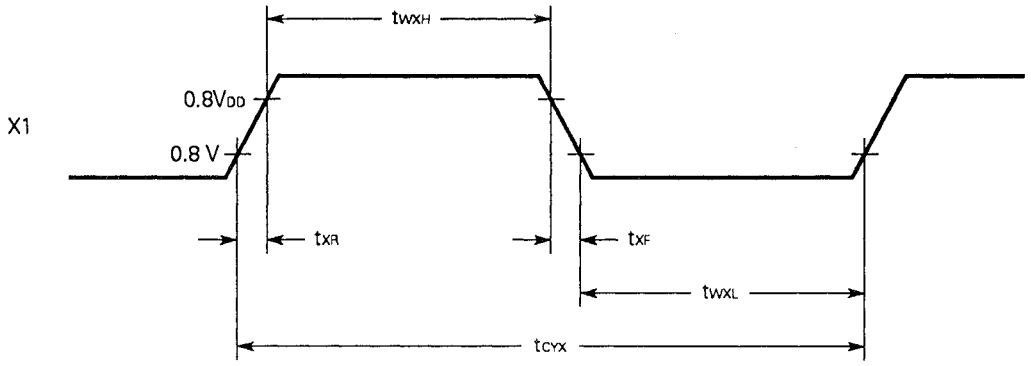
Interrupt Input Timing



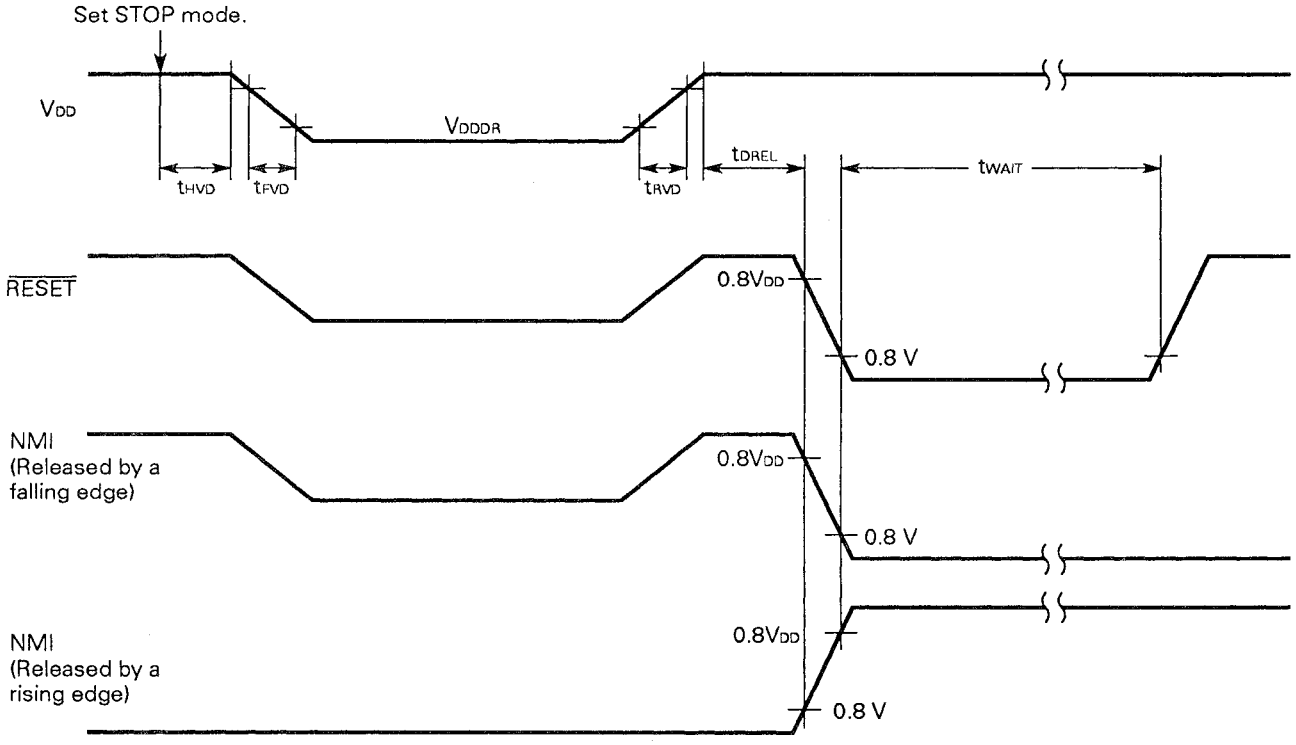
Reset Input Timing



External Clock Timing



Data Retention Timing



DC PROGRAMMING CHARACTERISTICS (T_a = 25 ±5 °C, $V_{PP} \geq$ 4.5 V, Vss = 0 V)

Parameter	Symbol	Symbol Note	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}	V_{IH}		2.4		V_{DDP}+0.3	V
Low-level input voltage	V_{IL}	V_{IL}		−0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	$0 \leq V_I \leq V_{DDP}$			10	μA
High-level output voltage	V_{OH1}	V_{OH1}	I_{OH} = −400 μA	2.4			V
	V_{OH2}	V_{OH2}	I_{OH} = −100 μA	V_{DD} - 0.7			V
Low-level output voltage	V_{OL}	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output leakage current	I_{LO}		$0 \leq V_O \leq V_{DDP}$, $\overline{OE}$ = V_{IH}			10	μA
V_{DDP} supply voltage	V_{DDP}	V_{CC}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			V
V_{DDP} supply current	I_{DD}	I_{CC}	Program memory write mode		5	30	mA
			Program memory read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}		5	30	mA
V_{PP} supply current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		5	30	mA
			Program memory read mode		1	100	μA

Note Symbols for the corresponding μPD27C256A

PROGRAM OPERATION

AC characteristics (T_a = 25 ±5 °C, V_{PP} ≥ 4.5 V, V_{DD} = 6 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Symbol Note	Conditions	Min.	Typ.	Max.	Unit
Address set up time (referred to $\overline{CE}\downarrow$)	t_{SAC}	t_{AS}		2			μs
$\overline{OE}$ high level hold time (referred to input data disable)	t_{HOID}	t_{OES}		2			μs
Input data setup time (referred to $\overline{CE}\downarrow$)	t_{SIDC}	t_{DS}		2			μs
Address hold time (referred to $\overline{CE}\uparrow$)	t_{HCA}	t_{AH}		2			μs
Input data hold time (referred to $\overline{CE}\uparrow$)	t_{HCID}	t_{DH}		2			μs
Output data hold time (referred to $\overline{OE}\uparrow$)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time (referred to $\overline{CE}\downarrow$)	t_{SVPC}	t_{VPS}		1			ms
V_{DDP} setup time (referred to $\overline{CE}\downarrow$)	t_{SVDC}	t_{VCS}		1			ms
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
Delay from $\overline{OE}\downarrow$ to data output time	t_{DOOD}	t_{OE}				150	ns

Note Symbols for corresponding μPD27C256A

READ OPERATION

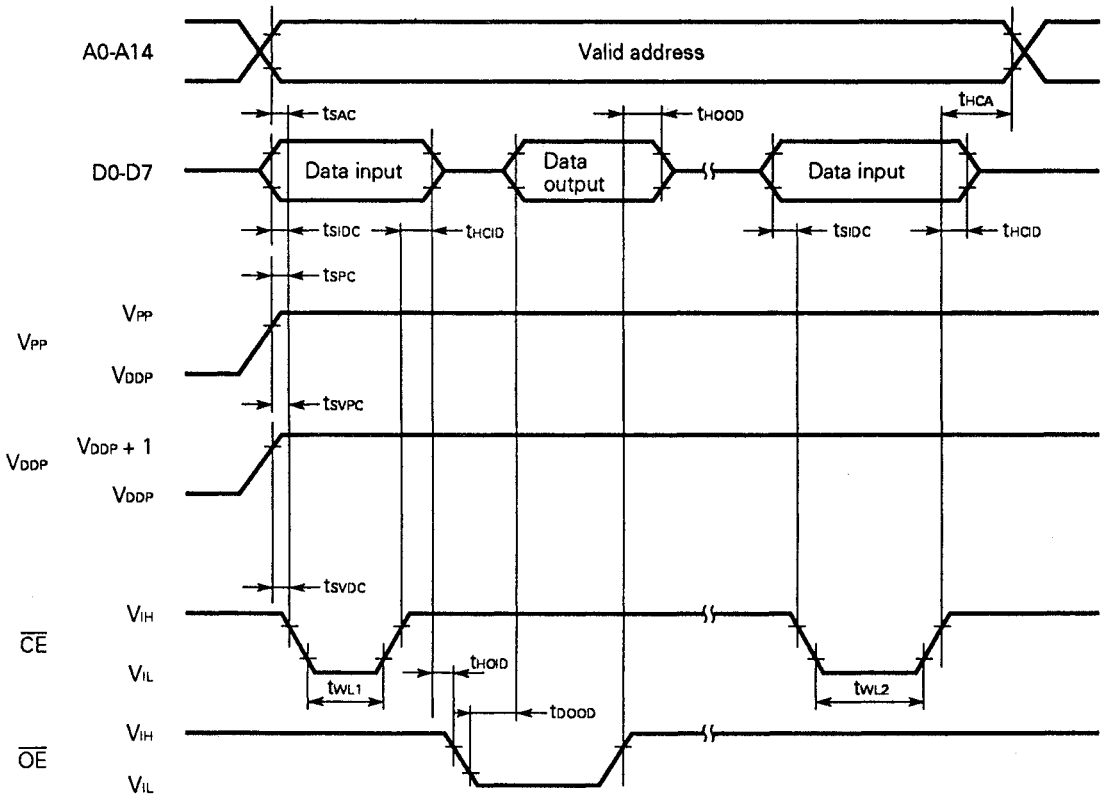
AC characteristics (T_a = 25 ±5 °C, V_{PP} ≥ 4.5 V, V_{DD} = 5 ±0.5 V, V_{PP} = V_{DDP}, V_{SS} = 0 V)

Parameter	Symbol	Symbol Note 1	Conditions	Min.	Typ.	Max.	Unit
Delay from address to data output	t_{DAOD}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			200	ns
Delay from $\overline{CE}\downarrow$ to data output	t_{DCOD}	t_{CE}	$\overline{OE}$ = V_{IL}			200	ns
Delay from $\overline{OE}\downarrow$ to data output	t_{DOOD}	t_{OE}	$\overline{CE}$ = V_{IL}			75	ns
Data hold time (referred to $\overline{OE}\uparrow$ or $\overline{CE}\uparrow$) Note 2	t_{HCOD}	t_{DF}	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}	0		60	ns
Data hold time (referred to address)	t_{HAOD}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Notes 1. Symbols for the corresponding μPD27C256A

2. t_{HCOD} is the time measured from when either $\overline{OE}$ or $\overline{CE}$ reaches V_{IH}, whichever is faster.

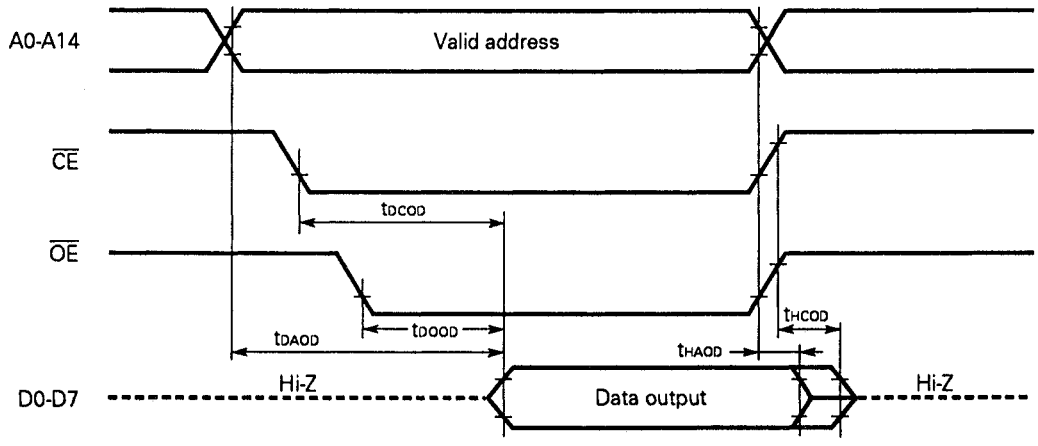
PROM Write Mode Timing



Cautions 1. V_{DDP} must be applied before V_{PP}, and must be cut after V_{PP}.

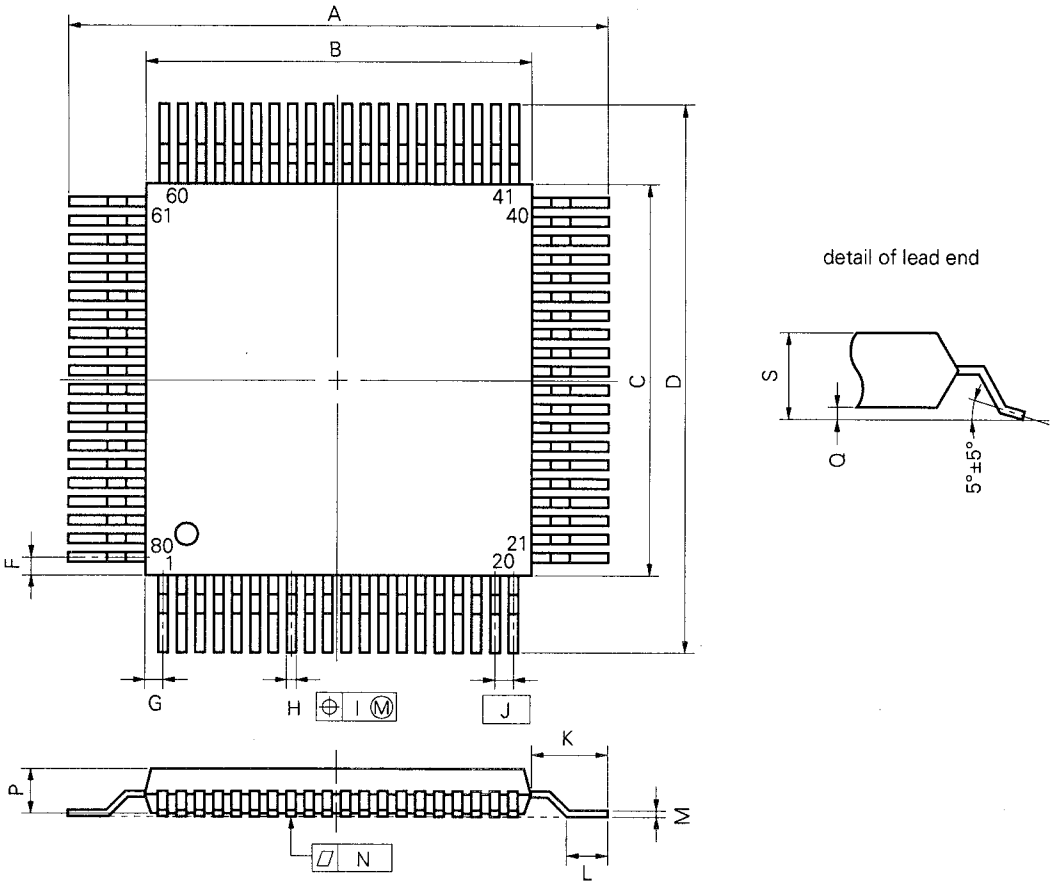
2. V_{PP} including overshoot must not exceed +13 V.

PROM Read Mode Timing



8. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (□14)



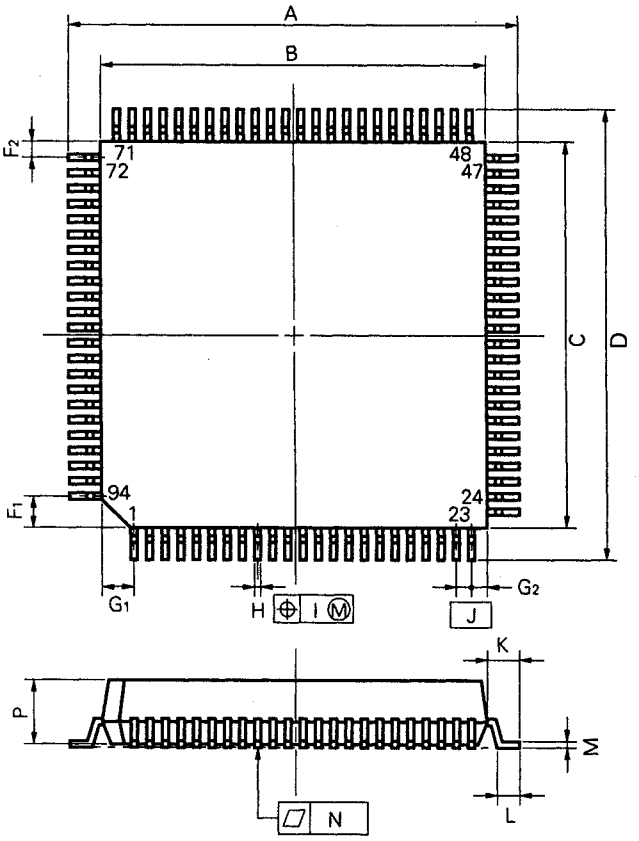
S80GC-65-3B9-3

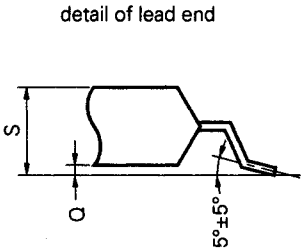
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

94 PIN PLASTIC QFP (□20)





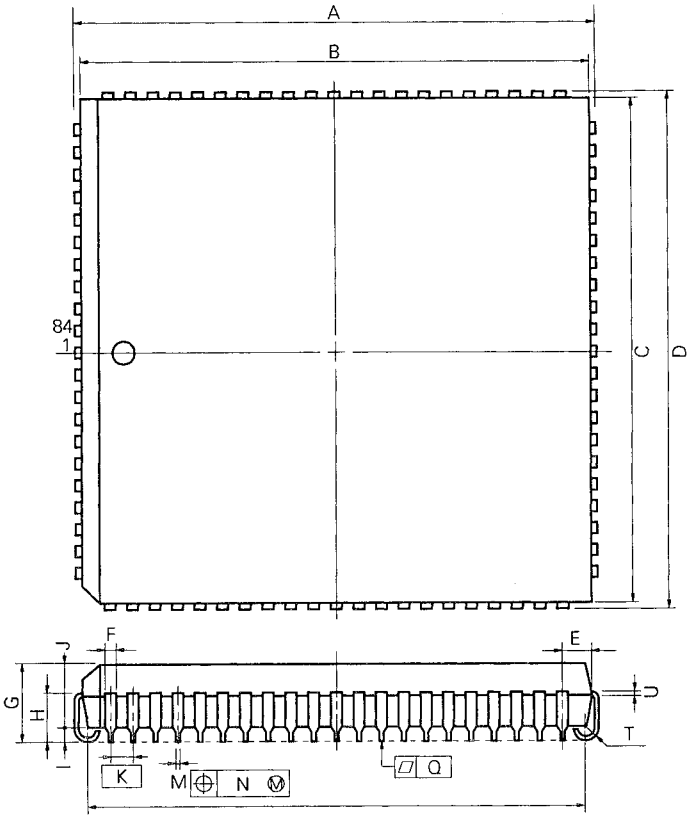
S94GJ-80-5BG-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.4	$0.913^{+0.017}_{-0.016}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	23.2±0.4	$0.913^{+0.017}_{-0.016}$
F_1	1.6	0.063
F_2	0.8	0.031
G_1	1.6	0.063
G_2	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	3.7	0.146
Q	0.1±0.1	0.004±0.004
S	4.0 MAX.	0.158 MAX.

84 PIN PLASTIC QFJ (□1150 mil)



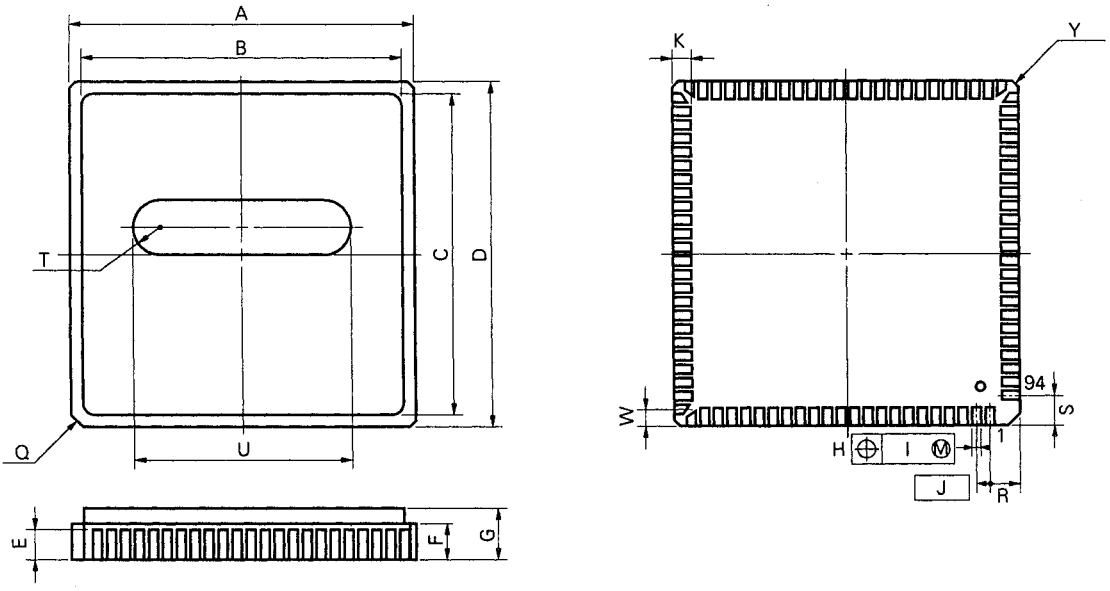
P84L-50A3-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	30.2±0.2	1.189±0.008
B	29.28	1.153
C	29.28	1.153
D	30.2±0.2	1.189±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	28.20±0.20	$1.110^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

94 PIN CERAMIC WQFN



X94KW-80A-1

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	18.0	0.709
C	18.0	0.709
D	20.0±0.4	$0.787^{+0.017}_{-0.016}$
E	1.94	0.076
F	2.14	0.084
G	4.064 MAX.	0.160 MAX.
H	0.51±0.10	0.020±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 1.0	C 0.039
R	1.6	0.063
S	1.6	0.063
T	R 1.75	0.069
U	11.5	0.453
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$

9. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

For the details of the recommended soldering conditions refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 9-1 Soldering Conditions for Surface-Mount Devices

(1) μPD78P238GC-3B9: 80-pin plastic QFP (14 × 14 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or less (at 210 °C or more) Number of reflow processes: 1 Exposure limit: 2 days[Note] (16 hours of pre-baking is required at 125 °C afterward.)	IR30-162-1
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Number of reflow processes: 1 Exposure limit: 2 days[Note] (16 hours of pre-baking is required at 125 °C afterward.)	VP15-162-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	–

(2) μPD78P238GJ-5BG: 94-pin plastic QFP (20 × 20 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or less (at 210 °C or more) Number of reflow processes: 1 Exposure limit: 7 days[Note] (10 hours of pre-baking is required at 125 °C afterward.)	IR30-107-1
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Number of reflow processes: 1 Exposure limit: 7 days[Note] (10 hours of pre-baking is required at 125 °C afterward.)	VP15-107-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	–

(3) μPD78P238LQ: 84-pin plastic QFJ (1150 × 1150 mil)

Soldering process	Soldering conditions	Symbol
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Number of reflow processes: 1 Exposure limit: 7 days[Note] (10 hours of pre-baking is required at 125 °C afterward.)	VP15-107-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	–

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 °C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

Notice

Other versions of the products are available. For these versions, the recommended reflow soldering conditions have been mitigated as follows:
Higher peak temperature (235 °C), two-stage, and longer exposure limit.
Contact an NEC representative for details.

APPENDIX A DEVELOPMENT TOOLS

The following tools are prepared for developing a system that uses the μPD78P238:

Software for language processing

RA78K/II[Note 1, Note 2]	Assembler package used for all 78K/II series products
CC78K/II[Note 1, Note 2]	C compiler package used for all 78K/II series products
CC78K/II-L[Note 1, Note 2]	C compiler library source file used for all 78K/II series products

PROM programming tools

PG-1500	PROM programmer
PA-78P238GC PA-78P238GJ PA-78P238KF PA-78P238LQ	Programmer adapter for connecting to the PG-1500
PG-1500 controller[Note 1]	Control program for the PG-1500

Debugging tools

IE-78230-R-A IE-78230-R[Note 3]	In-circuit emulator used for all μPD78234 series products
IE-78200-R-BK	Break board used for all 78K/II series products
IE-78230-R-EM IE-78200-R-EM[Note 3]	Emulation board for evaluating μPD78234 series products
EP-78230GC-R EP-78230GJ-R EP-78230LQ-R	Emulation probe used for all μPD78234 series products
EV-9200G-94 EV-9200GC-80	Socket to be mounted on the circuit board of the user system. It is used for the 94-pin plastic QFP and 80-pin plastic QFP.
EV-9900	Jig for removing the μPD78P238KF from the EV-9200G-94
SD78K/II[Note 1]	Screen debugger for the IE-78230-R-A
DF78230[Note 1]	Device file for μPD78234 series products

Real-time OS

RX78K/II[Note 1, Note 2]	Real-time OS used for all 78K/II series products

Notes 1. For the PC-9800 series (MS-DOS™) or IBM PC/AT™ (PC DOS™)

2. For the HP9000 series 300™ (HP-UX™), SPARCstation™ (Sun OS™), or EWS-4800 series™ (EWS-UX/V™)

3. For maintenance only

Fuzzy inference development support system

FE9000[Note 1]	Tool for creating fuzzy knowledge data
FT9080[Note 1]	Translator
FI78K/II[Note 1]	Fuzzy inference module
FD78K/II[Note 1, Note 4]	Fuzzy inference debugger

Notes 1. For the PC-9800 series (MS-DOS™) or IBM PC/AT™ (PC DOS™)

2. For the HP9000 series 300™ (HP-UX™), SPARCstation™ (Sun OS™), or EWS-4800 series™ (EWS-UX/V™)

3. For maintenance only

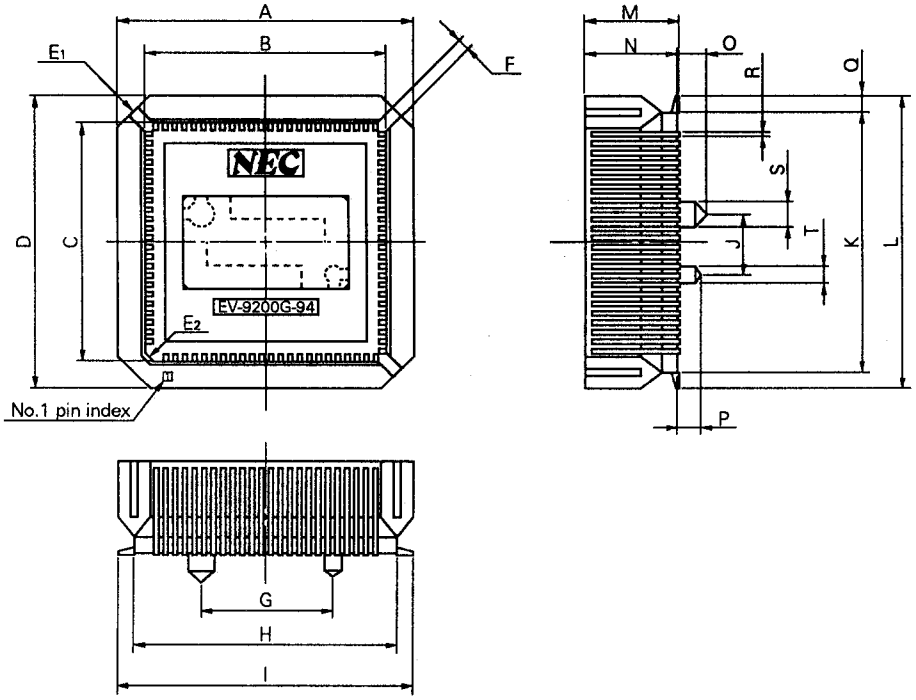
4. Under development

Remark Refer to the *78K/II Series Development Tools Selection Guide* (EF-231) for development tools manufactured by third parties.

★ DRAWINGS OF THE CONVERSION SOCKET (EV-9200G-94) AND RECOMMENDED PATTERN ON BOARDS (UNIT: mm)

Fig. A-1 Drawings of the EV-9200G-94 (Reference)

Based on EV-9200G-94
(1) Package drawing (in mm)

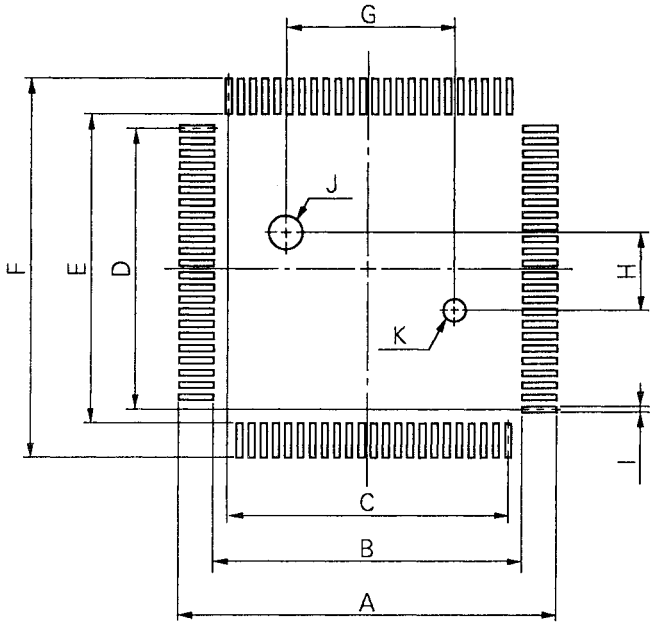


EV-9200G-94-G0

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.35	0.801
C	20.35	0.801
D	25.0	0.984
E_1	4-C 2.8	4-C 0.11
E_2	C 1.5	C 0.059
F	0.8	0.031
G	11.0	0.433
H	22.0	0.866
I	24.7	0.972
J	5.0	0.197
K	22.0	0.866
L	24.7	0.972
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35±0.1	$0.014^{+0.004}_{-0.005}$
S	φ2.3	φ0.091
T	φ1.5	φ0.059

Fig. A-2 Recommended Pattern on Boards for the EV-9200G-94 (Reference)

Based on EV-9200G-94
(2) Pad drawing (in mm)



EV-9200G-94-P0

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	$0.8\pm0.02\times23=18.4\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.906=0.724^{+0.003}_{-0.002}$
D	$0.8\pm0.02\times23=18.4\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.906=0.724^{+0.003}_{-0.002}$
E	21.0	0.827
F	25.7	1.012
G	11.00 ± 0.08	$0.433^{+0.004}_{-0.003}$
H	5.00 ± 0.08	$0.197^{+0.003}_{-0.004}$
I	0.5 ± 0.02	$0.02^{+0.001}_{-0.002}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

★ APPENDIX B RELATED DOCUMENTS

Documents related to the device

Document name		Document No.
μPD78234 Series User's Manual, Hardware		IEU-718
78K/II Series User's Manual, Instruction		IEU-754
78K/II Series Application Note	Basic	IEA-607
	Application	IEA-700
	Floating-Point Arithmetic Operation Programs	IEA-686
78K/II Series Selection Guide		IF-304
78K/II Series Instruction Set		IEM-5102
μPD78234 Series Special Function Registers		IEM-5515

Documents related to development tools (user's manual)

Document name		Document No.
RA78K Series Assembler Package	Operation	EEU-809
	Language	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-817
CC78K Series C Compiler	Operation	EEU-656
	Language	EEU-655
CC78K Series Library Source File		EEU-777
PG-1500 PROM Programmer		EEU-651
PG-1500 Controller		EEU-704
IE-78230-R-A In-Circuit Emulator		EEU-789
IE-78230-R In-Circuit Emulator	Hardware	EEU-682
	Software	EEU-685
SD78K/II Screen Debugger	Tutorial	EEU-841
	Reference	EEU-813
78K/II Series Development Tools Selection Guide		EF-231

Caution The above documents may be revised without notice. Use the latest versions when you design an application system.

Documents related to software to be incorporated into the product (user's manual)

Document name		Document No.
RX78K/II Real Time OS	Tutorial	EEU-910
	Installation	EE7-884
	Debugger	EEU-895
	Technical	EEU-885
Tool for Creating Fuzzy Knowledge Data		EEU-829
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System	Translator	EEU-862
78K/II Series Fuzzy Inference Development Support System	Fuzzy Inference Module	EEU-860
78K/II Series Fuzzy Inference Debugger		EEU-917

Other documents

Document name	Document No.
QTOP Microcomputer Pamphlet	IB-5040
Package Manual	IEI-1213
SMD Surface Mount Technology Manual	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-1203
Electrostatic Discharge (ESD) Test	MEM-1201
Guide to Quality Assurance for Semiconductor Devices	MEI-1202

Caution The above documents may be revised without notice. Use the latest versions when you design an application system.

[MEMO]

Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution **When handling MOS devices, take care so that they are not electrostatically charged.**

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution **Hold CMOS devices at a fixed input level.**

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution **The initial status of a MOS device is unpredictable when power is turned on.**

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

[MEMO]