FINAL

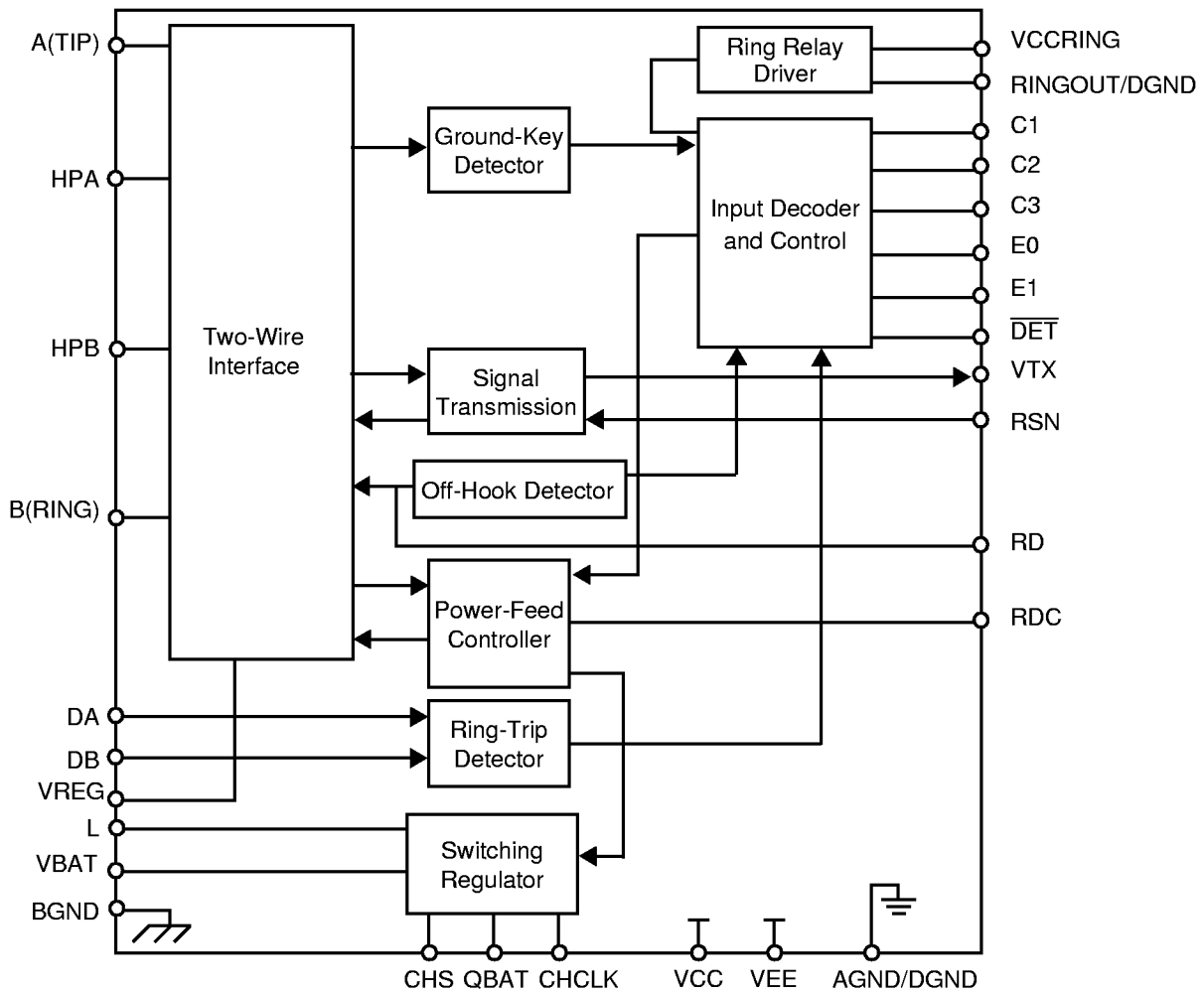
Am79M576A

Metering Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Programmable constant-resistance feed
- Programmable loop-detect threshold
- Ground-key detect
- Performs polarity reversal
- Ring relay driver
- Supports 2.2 Vrms metering (12 and 16 kHz)
- Line feed characteristics independent of battery variations
- On-chip switching regulator for low-power dissipation
- Two-wire impedance set by single external impedance
- Tip Open state for ground-start lines
- On-hook transmission

BLOCK DIAGRAM



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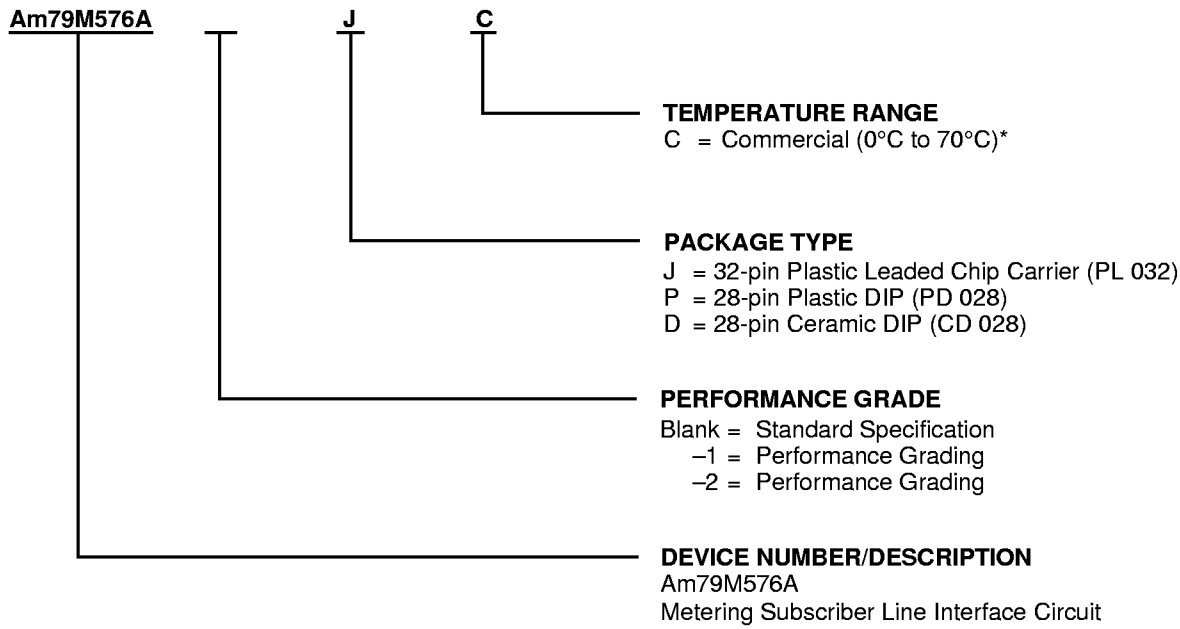
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am79M576A	–1 –2	JC PC DC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

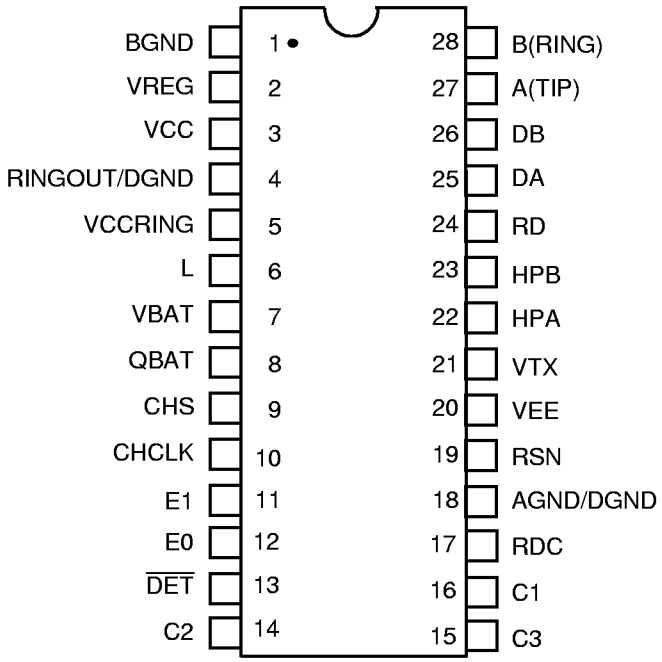
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

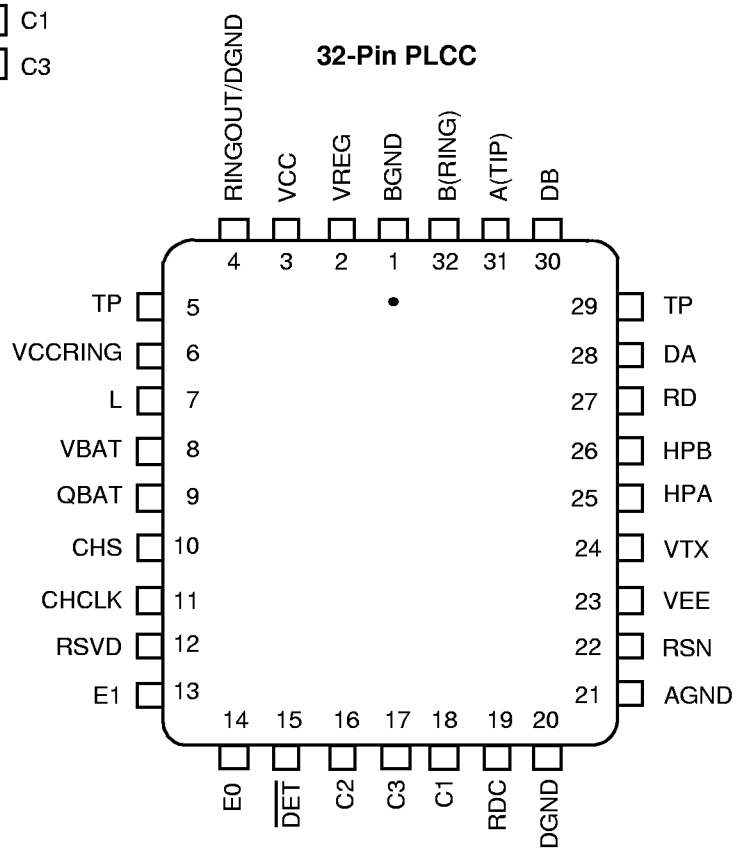
CONNECTION DIAGRAMS

Top View

28-Pin DIP



32-Pin PLCC



Notes:

1. *Pin 1 is marked for orientation.*
2. *TP is a thermal conduction pin tied to substrate.*
3. *RSVD = Reserved. Do not connect to this pin.*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND	Gnd	(32-pin PLCC) Analog (quiet) ground.
AGND/DGND	Gnd	(28-pin DIP) Analog and Digital ground are connected internally to a single pin.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Inputs	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
CHCLK	Input	Chopper clock. Input to switching regulator (TTL compatible). Freq = 256 kHz (nominal).
CHS	Input	Chopper Stabilization. Connection for external stabilization components.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Detector. Logic Low indicates that the selected detector is tripped. Logic inputs C3–C1, E1, and E0 select the detector. Open-collector with a built-in 15 kΩ pull-up resistor.
DGND	Gnd	(32-pin PLCC) Digital ground.
E0	Input	A logic High enables $\overline{\text{DET}}$. A logic Low disables $\overline{\text{DET}}$.
E1	Input	E1 = High connects the ground-key detector to $\overline{\text{DET}}$, and E1 = Low connects the off-hook or ring-trip detector to $\overline{\text{DET}}$.
HPA	Capacitor	High-pass filter capacitor; A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor; B(RING) side of high-pass filter capacitor.
L	Input	Switching Regulator Power Transistor . Connection point for filter inductor and anode of catch diode. Has up to 60 V of pulse waveform and must be isolated from sensitive circuits. Keep the diode connections short because of the high currents and high di/dt.
QBAT	Battery	Quiet Battery. Filtered battery supply for the signal processing circuits.
RD	Resistor	Detector resistor. Threshold modification/filter point for the off-hook detector.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network, which also connects to the receiver summing node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT/ DGND	Output	Relay ground for 5 V relays—externally connected to DGND.
RSN	Input	The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation
VBAT	Battery	Battery supply.
VCC	Power	+5 V power supply.
VCCRING	Input	Ring relay driver (sinks current to RINGOUT).
VEE	Power	–5 V power supply.
VREG	Input	Regulated Voltage. Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor, and chopper stabilization.
VTX	Output	Transmit Audio. This output is 0.510 times the A(TIP) and B(RING) metallic voltage. The other end of the two-wire input impedance programming network connects here.

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... –55°C to +150°C

Ambient temperature, operating ..... –0°C to +70°C

V_{CC} with respect to AGND ..... –0.4 V to +7.0 V

V_{EE} with respect to AGND ..... +0.4 V to –7.0 V

V_{BAT} with respect to AGND ..... +0.4 V to –70 V

Note: *Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass is 0.33 µF.*

BGND with respect to AGND/DGND.. +1.0 V to –3.0 V

A(TIP) or B(RING) to BGND:

- Continuous ..... –70 V to +2 V
- 10 ms (f = 0.1 Hz) ..... –70 V to +5 V
- 1 µs (f = 0.1 Hz) ..... –90 V to +10 V
- 250 ns (f = 0.1 Hz) ..... –120 V to +15 V

Current from A(TIP) or B(RING)..... ±150 mA

Voltage on VCCRING ..... –0.3 V to +7 V

Current through relay drivers or internal driver catch diodes ..... 60 mA

Voltage on ring-trip inputs DA and DB ..... V_{BAT} to 0 V

Current into ring-trip inputs..... ±10 mA

Peak current into regulator switch (L pin) ..... 150 mA

Switcher transient peak off voltage on L pin ..... +1.0 V

C3–C1, E0, E1, CHCLK to AGND..... –0.4 V to V_{CC} + 0.4 V

Maximum power dissipation (see note) ..... T_A = 70°C

- In 28-pin ceramic DIP package..... 1.5 W
- In 28-pin plastic DIP package ..... 1.2 W
- In 32-pin PLCC package..... 1.2 W

Note: *Thermal limiting circuitry on-chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature ..... 0°C to +70°C*

V_{CC} ..... 4.75 V to 5.25 V

V_{EE} ..... –4.75 V to –5.25 V

V_{BAT} ..... –46.4 V to –54 V

V_{CC}RING..... 0 V to 5.25 V

AGND/DGND..... 0 V

BGND with respect to AGND..... –2 V to +2 V

Load resistance on VTX to ground..... 10 kΩ min

Operating Ranges define those limits between which device functionality is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Analog output (V_{TX}) impedance			3	20	Ω	
Analog (V_{TX}) output offset	0°C to +25°C +25°C to +85°C –40°C to 0°C	–40 –35 –45		+40 +35 +45	mV	4 — 4
Analog (RSN) input impedance Longitudinal impedance at A or B	300 Hz to 3.4 kHz		1	20 35	Ω	4
Overload level 4-wire 2-wire	Z_{IN} = 600 to 900 Ω	–3.1 –5.5		+3.1 +5.5	Vpk	2
Transmission Performance, 2-Wire Impedance						
2-wire return loss (See Test Circuit D)	300 Hz to 500 Hz 500 Hz to 2.5 kHz 2.5 kHz to 3.4 kHz OHT 300 Hz to 3.4 kHz	26 26 20 14			dB	4
Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C); R_L = 600 Ω						
Longitudinal to metallic L-T, L-4	300 Hz to 3.4 kHz	48			dB	
Longitudinal sum (L-T) + (T-L)	300 Hz to 3.4 kHz	95				
Longitudinal signal generation 4-L or T-L	300 Hz to 800 Hz 800 Hz to 3.4 kHz	40 35				
Longitudinal current capability per wire	Active state, 50 Hz to 200 Hz OHT state, 50 Hz to 200 Hz	17 8			mA peak	4
Dial pulse make or break response time of $\overline{DET}$				3	ms	
Insertion Loss (See Test Circuits A and B)						
2- to 4-wire	V_{AB} = 0 dBm, 1 kHz 0°C to +70°C –40°C to +85°C	5.70 5.65	5.85 5.85	6.00 6.05	dB	— 4
4- to 2-wire	V_{RX} = 0 dBm, 1 kHz 0°C to +70°C –40°C to +85°C	–0.15 –0.20		+0.15 +0.20		— 4
4- to 2-wire (In the presence of 2.2 Vrms metering)				1.5		4
Metering Signal Insertion Loss (See Test Circuit B)						
4- to 2-wire	R_L = 260, V_{AB} = 2.86 Vrms R_{TMG} = 139.5 kΩ f = 12 kHz or 16 kHz	–0.8	–0.2	+0.4	dB	4
Insertion Loss vs. Frequency (See Test Circuits A and B)						
2- to 4-wire or 4- to 2-wire	300 Hz to 3.4 kHz 0°C to +70°C Relative to 1 kHz –40°C to +85°C	–0.1 –0.15		+0.1 +0.15	dB	— 4
Gain Tracking (See Test Circuits A and B)						
2- to 4-wire or 4- to 2-wire	+7 dBm to –55 dBm 0°C to +70°C Reference: 0 dBm –40°C to +85°C	–0.1 –0.15		+0.1 +0.15	dB	— 4
Balance Return Signal (4- to 4-Wire, See Test Circuit B)						
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C –40°C to +85°C	–6.00 –6.05	–5.85 –5.85	–5.70 –5.65	dB	— 4
Variation with frequency relative to 1 kHz	300 Hz to 3.4 kHz 0°C to +70°C –40°C to +85°C	–0.1 –0.15		+0.1 +0.15		3, 4 4
Gain tracking	+3 dBm to –55 dBm 0°C to +70°C Reference: –4 dBm –40°C to +85°C	–0.1 –0.15		+0.1 +0.15		— 4
Group delay	f = 1 kHz	3.3	5.3	7.3	µs	4

ELECTRICAL CHARACTERISTICS (continued)

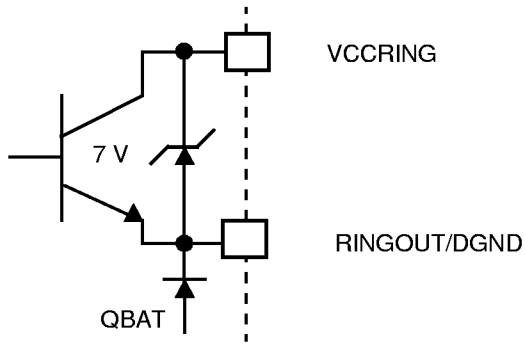
Description	Test Condition (See Note 1)	Min	Typ	Max	Unit	Note
Total Harmonic Distortion (2- to 4-Wire or 4- to 2-Wire) without Metering (See Test Circuits A and B)						
0 dBm +9 dBm	300 Hz to 3.4 kHz		–64 –55	–50 –40	dB	
Total Harmonic Distortion with metering				–35		4, 11
Idle Channel Noise without Metering						
Psophometric weighted noise	2-wire 4-wire			–75 –80	dBmp	7
Psophometric idle channel noise with metering	2-wire 4-wire			–46 –52		4, 7, 12 4, 7, 12
Single Frequency Out-of-Band Noise (See Test Circuit E)						
Metallic	4 kHz to 9 kHz 9 kHz to 1 MHz 256 kHz and harmonics		–76 –76 –57		dBm	4, 5, 9 4, 5, 9 4, 5
Longitudinal	1 kHz to 15 kHz Above 15 kHz 256 kHz and harmonics		–70 –85 –57			4, 5, 9 4, 5, 9 4, 5
Line Characteristics (See Figures 1a, 1b, and 1c) BAT = 48 V, V_{BAT} = –47.3 V, R_L = 600 Ω and 900 Ω						
Apparent battery voltage	Active state	47	50	53	V	
Loop current accuracy	Active state	–7.5		+7.5	%	
Loop current, Tip Open state Open Circuit state	R_L = 600 Ω R_L = 0 Ω			1.0	mA	
Loop current limit accuracy	OHT state I_L = 13.5 mA, R_L = 0 Ω	–15		+15	%	10
Loop current—Active state	R_L = 2.25 kΩ	14.33				
Loop current—Active state Battery = –48.0 V	R_L = 1.96 kΩ R_L = 0 Ω	17.5 41		50	mA	
Loop current—OHT Battery = –47.0 V	R_L = 2.25 kΩ R_L = 0 Ω	9.35		15.5		
Fault current limit, I_LLIM, A and B shorted to GND in OHT state			56	80		
Fault current limit, I_LLIM, A and B shorted to GND in Active state				110		
Battery Current in Fault Condition						
OHT state	A and B to GND			40	mA	
Active state	A and B to GND			55		
Power Dissipation						
On hook, Open Circuit state On hook, OHT state On hook, Active state Off hook, OHT state	 R_L = 600 Ω		40 140 190 350	80 200 300 500	mW	
Off hook, Active state (See Figure 2)	R_L = 600 Ω R_L = 220 Ω		750 900	900 1100		

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Supply Currents						
V_{CC}, on-hook supply current	Open Circuit state OHT state Active state		2 5 6	4.0 7.0 9.0	mA	
V_{EE}, on-hook supply current	Open Circuit state OHT state Active state		1.0 2.3 2.3	2.0 4.0 4.5		
V_{BAT}, on-hook supply current	Open Circuit state OHT state Active state		0.4 2.2 3.2	1.0 3.5 5.0		
V_{BAT}, off-hook supply current	OHT state R_L = 0 to 2.2 kΩ			15.5		
Power Supply Rejection Ration (V_{RIPPLE} = 50 mVrms, Saturation Guard Inactive)						
V_{CC}	40 Hz to 3.4 kHz 3.4 kHz to 50 kHz	18 18	35 30		dB	6, 7
V_{EE}	40 Hz to 3.4 kHz 3.4 kHz to 50 kHz	20 13	30 25			6, 7
V_{BAT}	40 Hz to 3.4 kHz 3.4 kHz to 50 kHz	27 20	30 30			6, 7
Off-Hook Detector						
Current threshold	$I_{DET} = 365/R_D$	–15		+15	%	
Ground-Key Off-Hook Detector Thresholds, Active State						
Resistance threshold	B(RING) to GND	2.0	5	10.0	kΩ	
Current threshold	B(RING) to GND Midpoint to GND		9		mA	8
Ring-Trip Detector Inputs						
Bias current		–5	–0.05		µA	
Offset voltage	Source resistance = 0 to 200 kΩ	–50	0	+50	mV	
Logic Inputs (C3–C1, E0, E1, and CHCLK)◆						
Input High voltage		2.0			V	
Input Low voltage				0.8		
Input High current	All inputs except E1 Input E1	–75 –75		40 45	µA	
Input Low current		–0.4			mA	
Logic Output ($\overline{DET}$)						
Output Low voltage	I_{OUT} = 0.8 mA			0.4	V	
Output High voltage	I_{OUT} = –0.1 mA	2.4				
Relay Driver						
On voltage (VCCRING to RINGOUT)	50 mA to VCCRING, RINGOUT connected to AGND/DGND			1.25	V	*
Off leakage			0.5	100	µA	
Zener breakover voltage	100 µA	6.0	7.2		V	
Zener On voltage	30 mA		10.0	11.0		

Note:
◆ *C3–C1, and E0 have an internal pull up. E1 has an internal pull down.*

RELAY DRIVER SCHEMATIC

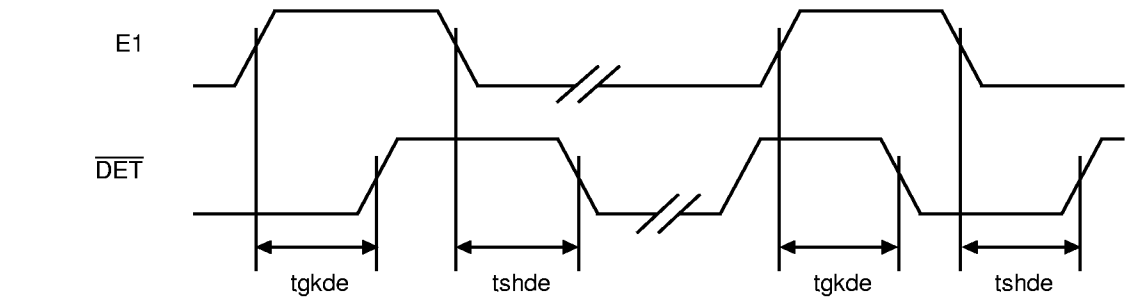


SWITCHING CHARACTERISTICS

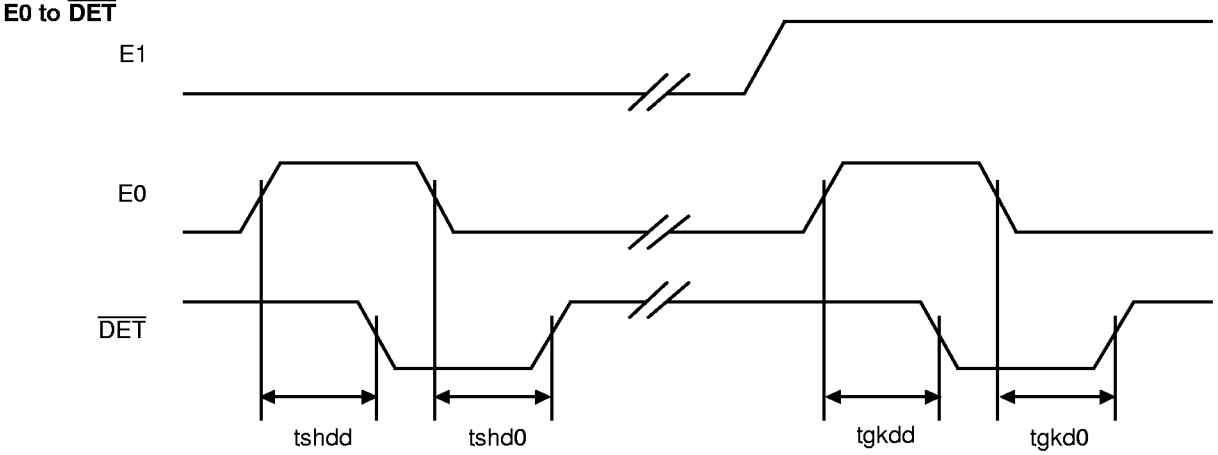
Symbol	Parameter	Test Conditions	Temperature Ranges	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground-Key Detect state R_L open, R_G connected (See Figure H)	0°C to +70°C –40°C to 85°C			3.8 4.0	µs	4
	E1 Low to $\overline{DET}$ Low (E0 = 1)		0°C to +70°C –40°C to 85°C			1.1 1.6		
tgkdd	E0 High to $\overline{DET}$ Low (E1 = 0)		0°C to +70°C –40°C to 85°C			1.1 1.6		
tgkd0	E0 Low to $\overline{DET}$ High (E1 = 0)		0°C to +70°C –40°C to 85°C			3.8 4.0		
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switchhoook Detect state R_L = 600 Ω, R_G open (See Figure G)	0°C to +70°C –40°C to 85°C			1.2 1.7		
	E1 High to $\overline{DET}$ High (E0 = 1)		0°C to +70°C –40°C to 85°C			3.8 4.0		
tshdd	E0 High to $\overline{DET}$ Low (E1 = 1)		0°C to +70°C –40°C to 85°C			1.1 1.6		
tshd0	E0 Low to $\overline{DET}$ High (E1 = 1)		0°C to +70°C –40°C to 85°C			3.8 4.0		

SWITCHING WAVEFORMS

E1 to $\overline{\text{DET}}$



E0 to $\overline{\text{DET}}$



Note:

All delays measured at 1.4 V level.

Notes:

* *When any power supplies to the MSLIC are removed and the MSLIC is not in the Ringing state, the relay driver must not activate when the relay coil connected to VCCRING is supplied by the same V_{CC} used for powering the MSLIC.*

If the relay coil connected to VCCRING is supplied by a voltage other than the V_{CC} used for powering the MSLIC, you must:
– Provide redundancy of V_{CC} from the supply voltage of the relay
– As an alternative, limit the current flowing to all digital inputs to less than 1 mA.

1. *Unless otherwise noted, test conditions are BAT = 48 V (voltage at chip VBAT pin = –47.3 V), V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, C_{HP} = 0.22 µF, R_{DC1} = R_{DC2} = 18.7 kΩ, C_{DC} = 0.15 µF, R_d = 57.6 kΩ, no fuse resistors, two-wire AC output impedance programming impedance (Z_T) = 306 kΩ resistive, receive input summing impedance (Z_{RX}) = 300 kΩ resistive. (See Table 2 for component formulas.) Operation in polarity reverse is tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *These tests are performed with a longitudinal impedance of 90 Ω and metallic impedance of 300 Ω for frequencies < 12 kHz and 135 Ω for frequencies >12 kHz. These tests are extremely sensitive to circuit board layout. Refer to application notes for details.*
6. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
7. *When the SLIC is in the anti-sat 2 operating region, this parameter will be degraded. The exact degradation will depend on system design. The anti-sat 2 region occurs at high loop resistances when $|V_{BAT}| - |V_{AX} - V_{BX}|$ is less than approximately 13 V.*
8. *"Midpoint" is defined as the connection point between two 300 Ω series resistors connected between A(TIP) and B(RING).*
9. *Fundamental and harmonics from 256 kHz switch regulator chopper are not included.*
10. *Calculate loop current limit, which depends upon the programmed apparent open circuit voltage and the feed resistance, is as follows:*
    In OHT state: I_{LIMIT} = 0.202 and
    In Active state: I_{LIMIT} = 0.68

$$\frac{50 \bullet V_{APPARENT}}{R_{DC}}$$

11. Total Harmonic distortion with metering is specified with a metering signal of 2.2 Vrms at the two-wire output, and a transmit signal of +3 dBm or receive signal of –4 dBm. The transmit or receive signals are single-frequency inputs, and the distortion is measured as the highest in band harmonic at the two-wire or the four-wire output relative to the input signal.

12. Noise with metering is measured by applying a 2.2 Vrms metering signal (measured at the two-wire output) and measuring the psophometric noise at the two-wire outputs over a 200 ms time interval.

Table 1. SLIC Decoding

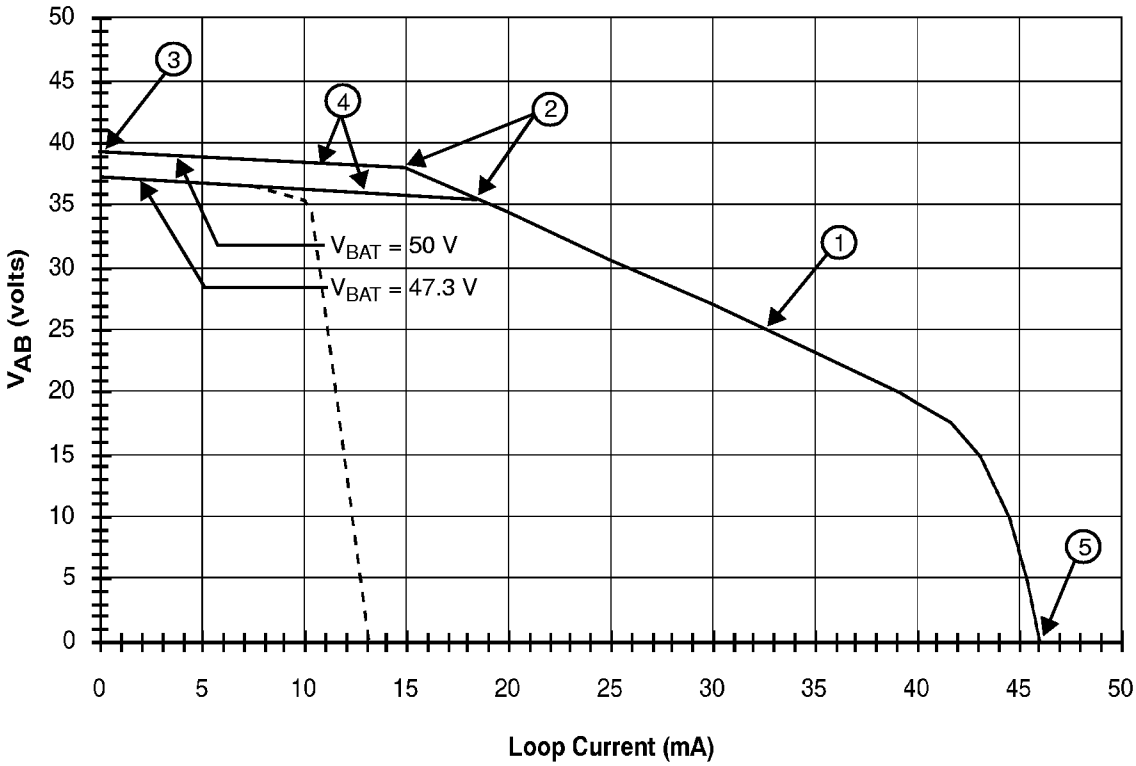
				$\overline{\text{DET}}$ Output	
State	**C3**	**C2**	**C1**	**Two-Wire Status**	**E0 = 1* E1 = 0**	**E0 = 1* E1 = 1**
0	0	0	0	Open Circuit	Ring trip	Ring trip
1	0	0	1	Ringing	Ring trip	Ring trip
2	0	1	0	Active	Loop detector	Ground key
3	0	1	1	On-hook TX (OHT)	Loop detector	Ground key
4	1	0	0	Tip Open	Loop detector	—
5	1	0	1	Reserved	Loop detector	—
6	1	1	0	Active Polarity Reversal	Loop detector	Ground key
7	1	1	1	OHT Polarity Reversal	Loop detector	Ground key

Note:
** A logic Low on E0 disables $\overline{\text{DET}}$ output into the Open Collector state.*

Table 2. User-Programmable Components

$Z_T = 510(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = 0.98(Z_T)$	Z_{RX} is connected from V_{RX} to RSN. Z_T is defined above. This equation sets the receive gain to 0 dB when the SLIC terminates with an impedance equal to Z_{2WIN}.
$R_{DC1} + R_{DC2} = 50 \bullet (R_{FEED} - 2R_F)$ $C_{DC} = 1.5\ \text{ms} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = \frac{365}{I_T}, \quad C_D = \frac{0.5\ \text{ms}}{R_D}$	R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on-hook and off-hook.
$Z_M = \frac{V_{MG}}{V_{M2W}} \bullet \frac{K_1(\omega) Z_L \bullet Z_T}{Z_T + 0.51\ \text{V} \bullet K_1(\omega) \bullet (2R_F + Z_L)}$	Z_M is connected from V_{MG} (metering source) to the RSN pin, V_{M2W} is the desired magnitude of the metering signal at the 2-wire output (usually 2.2 Vrms) and $K_1(\omega)$ is defined below. $K_1(\omega) = \frac{1000}{1 + j\omega\left(11.5 \bullet 10^{-9} + \frac{CX}{2}\right)(36 + Z_L + 2R_F)}$ where: CX = The values of the identical capacitors from A and B to GND $\omega = 2\pi \bullet$ metering frequency

DC FEED CHARACTERISTICS



Notes:

1. *Constant-resistance read region:* $V_{AB} = 49.6 - I_L\left(\frac{R_{DC}}{49.87}\right)$

2. *Anti-sat (battery-tracking) turn-on:* $V_{AB} = 0.8975|V_{BAT}| - 6.835$

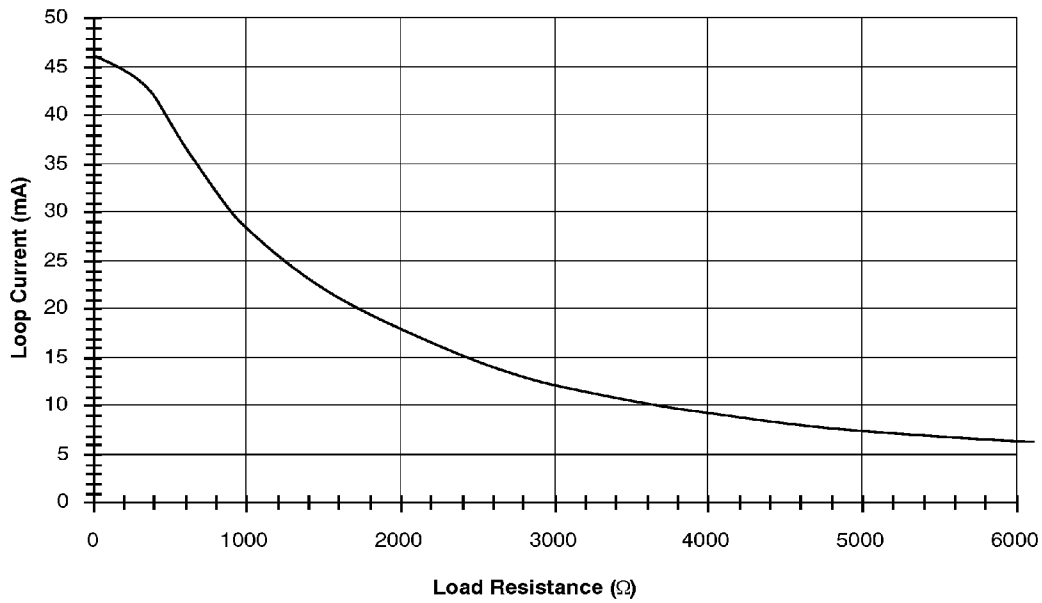
3. *Open Circuit voltage:* $V_{AB} = 0.7915|V_{BAT}| - 0.113$, $|V_{BAT}| < 62.8$ V
   $V_{AB} = 49.6$ V, $|V_{BAT}| \geq 62.8$ V

4. *Anti-sat (battery-tracking) region:* $V_{AB} = 0.7915|V_{BAT}| - 0.113 - I_L\left(\frac{R_{DC}}{815}\right)$

5. *Current limit:* $I_L = \frac{1724}{R_{DC}}$

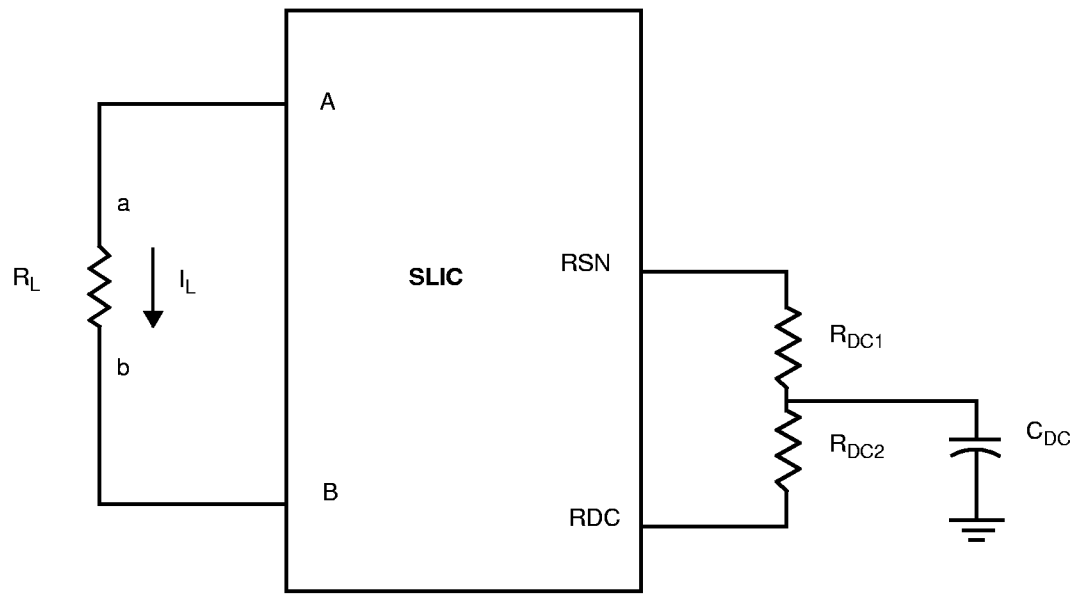
a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)

DC FEED CHARACTERISTICS (continued)



V_{BAT} = 47.3 V
R_{DC} = 37.5 kΩ

b. Loop Current vs. Load Resistance (Typical)



Feed current programmed by R_{DC1} and R_{DC2}

c. Feed Programming

Figure 1. DC Feed Characteristics

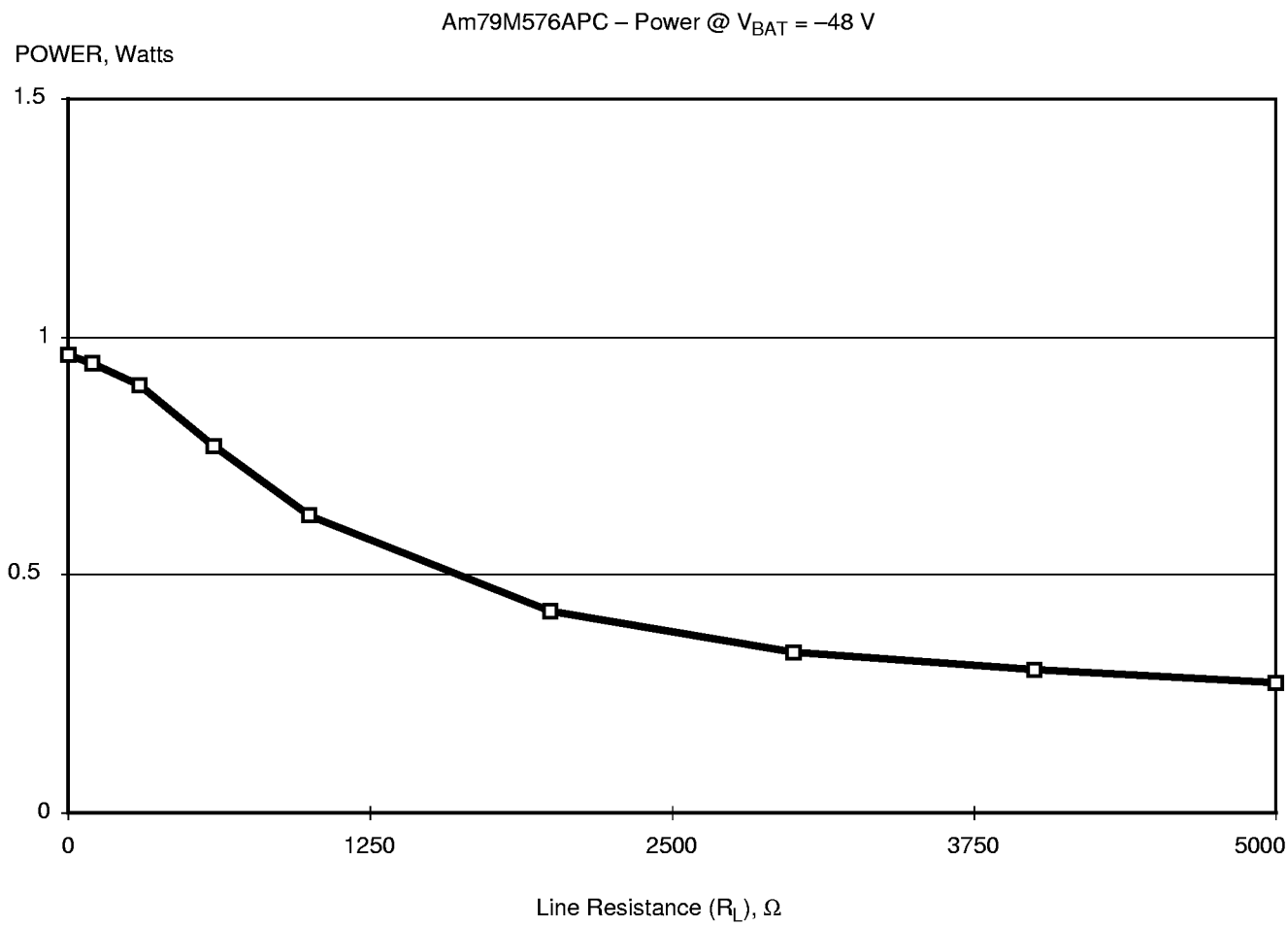
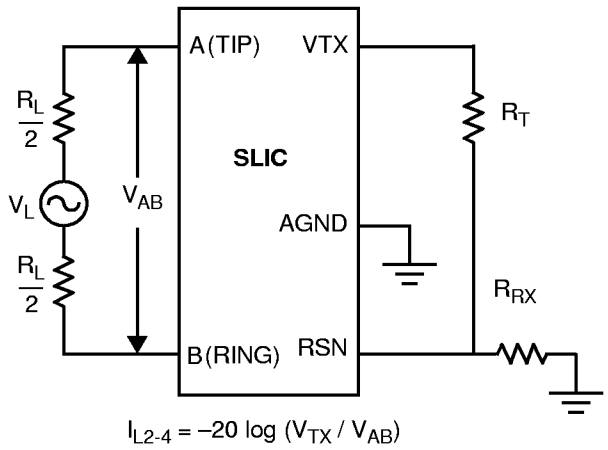
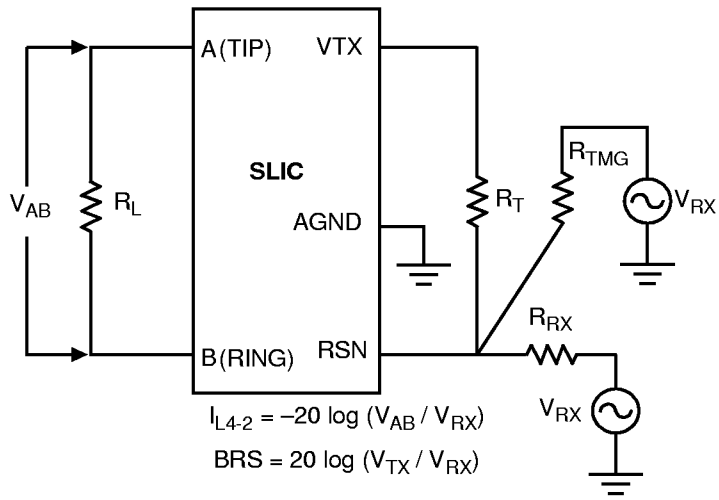


Figure 2. Active State Total Power Dissipation (Typical)

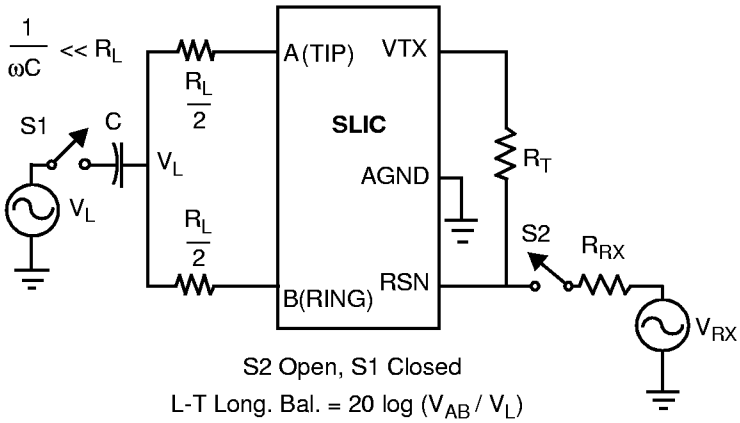
TEST CIRCUITS



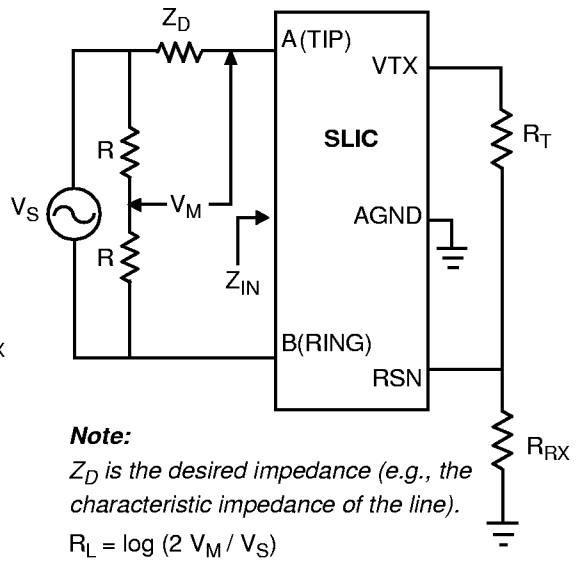
A. Two- to Four-Wire Insertion Loss



B. Four- to Two-Wire Insertion Loss and Balance Return Signal



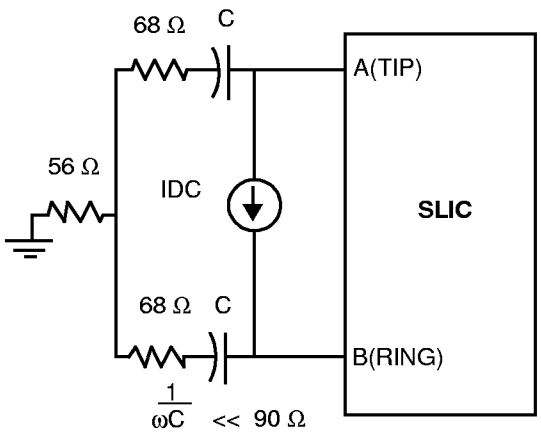
C. Longitudinal Balance



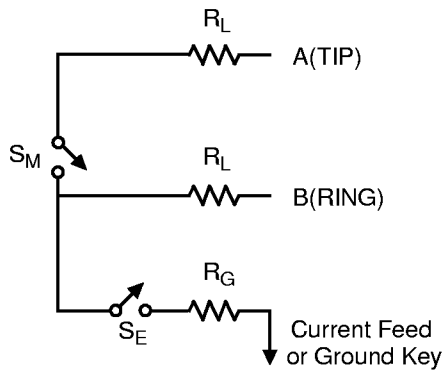
Note:
Z_D is the desired impedance (e.g., the characteristic impedance of the line).
$R_L = \log (2 V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

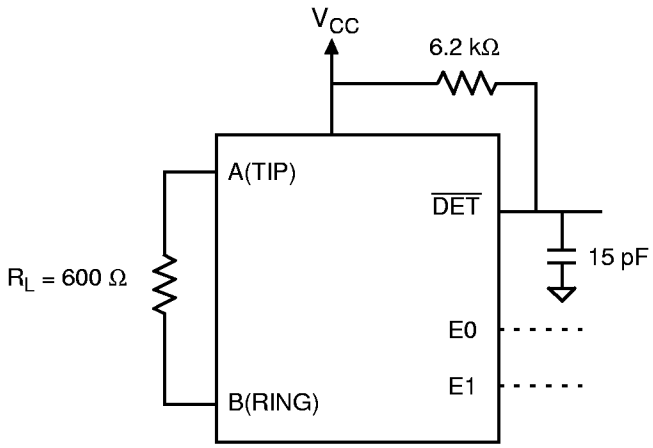
TEST CIRCUITS (continued)



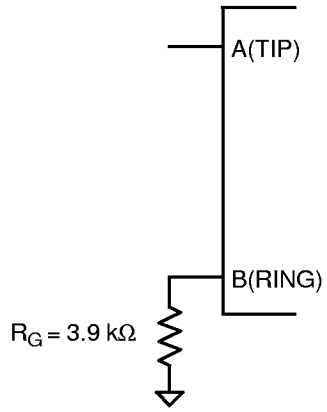
E. Single Frequency Noise



F. Ground-Key Detection



G. Loop-Detector Switching



H. Ground-Key Switching

REVISION SUMMARY

Revision A to Revision B

- Minor changes were made to the data sheet style and format to conform to AMD standards.

Revision B to Revision C

- In Pin Description table, inserted/changed TP pin description to: “Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.”
- Minor changes were made to the data sheet style and format to conform to AMD standards.

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Count Registers

Each of the three timers has a 16-bit count register. The contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

The count registers should be programmed before attempting to use the timers, since they are not automatically initialized to zero.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while Timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two MAX COUNT values whenever the current maximum count is reached. A timer resets when the timer count register equals the MAX COUNT value being used. If the timer count register or the MAX COUNT register is changed so that the MAX COUNT is less than the timer count the timer does not immediately reset. Instead, the timer counts up to 0FFFFH, "wraps around" to zero, counts up to the MAX COUNT value, and then resets.

Timers and Reset

Upon RESET, the Timers will perform the following actions:

- All EN (Enable) bits are reset preventing timer counting.
- For Timers 0 and 1, the RIU bits are reset to zero and the ALT bits are set to one. This results in the Timer Out pins going High.
- The contents of the count registers are indeterminate.

INTERRUPT CONTROLLER

The 80C186 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The 80C186 interrupt controller has its own control register that sets the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may themselves be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Figure 19.

The 80C186 has a special slave mode in which the internal interrupt controller acts as a slave to an external master. The controller is programmed into this mode by setting bit 14 in the peripheral control block relocation register (see Slave Mode section).

MASTER MODE OPERATION

Interrupt Controller External Interface

Five pins are provided for external interrupt sources. One of these pins is NMI, the non-maskable interrupt. NMI is generally used for unusual events such as power-fail interrupts. The other four pins may be configured in any of the following ways:

- As four interrupt lines with internally generated interrupt vectors.
- As an interrupt line and interrupt acknowledge line pair (cascade mode) with externally generated interrupt vectors plus two interrupt input lines with internally generated vectors.
- As two pairs of interrupt/interrupt acknowledge lines (cascade mode) with externally generated interrupt vectors.

External sources in the cascade mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the 80C186 on the second cycle. The capability to interface to external 82C59A programmable interrupt controllers is provided when the inputs are configured in cascade mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the 82C59A. The interrupt controller responds identically to internal interrupts in all three modes; the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

Fully Nested Mode

When in the fully nested mode four pins are used as direct interrupt requests as in Figure 20. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in-service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate

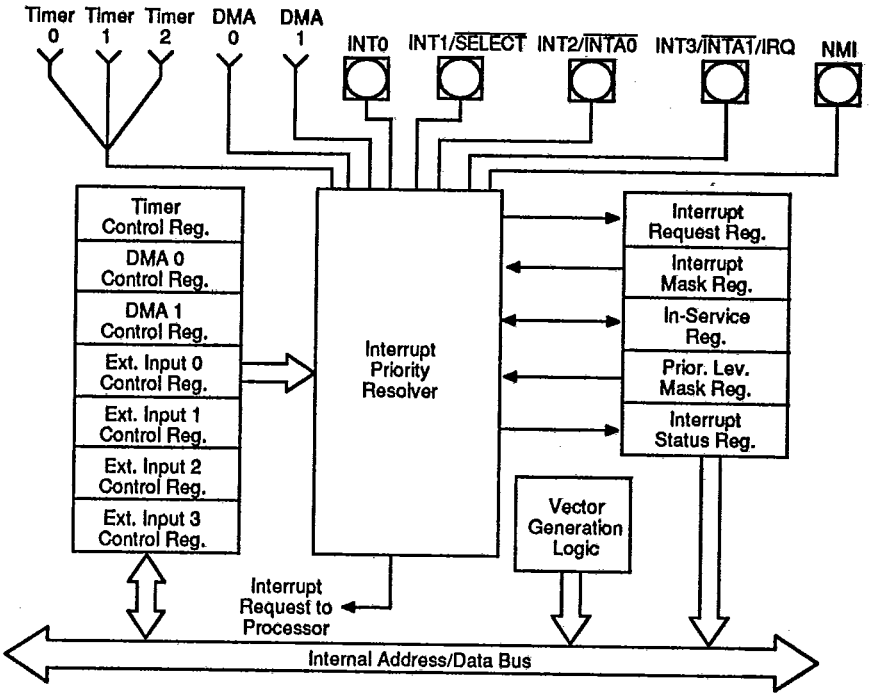

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Figure 19. Interrupt Controller Block Diagram

Master Mode Features

Programmable Priority

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority.) All interrupt sources have preprogrammed default priority levels (see Table 3).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 3 is used. If the serviced interrupt routine reenables interrupts, it allows other interrupt requests to be serviced.

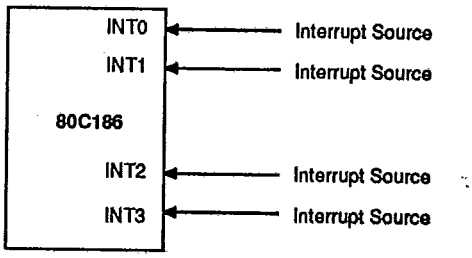

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Figure 20. Fully Nested (Direct) Mode Interrupt Controller Connections

SWITCHING CHARACTERISTICS (continued)

Ready, Peripheral, and Queue Status Timings

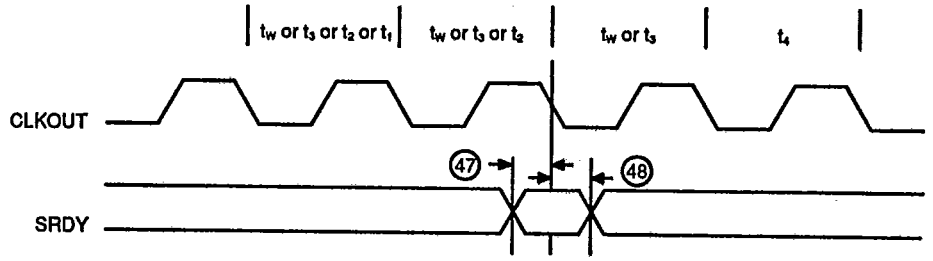
$T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$ except $V_{CC} = 5\ V \pm 5\%$ at $f > 12.5$ MHz

			Preliminary								
			80C186		80C186-12		80C186-16		80C186-20		
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Unit
80C186 Ready and Peripheral Timing Requirements											
47	t_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	15		15		15		10		ns
48	t_{CLSRY}	SRDY Transition Hold Time(1)	15		15		15		10		ns
49	t_{ARYCH}	ARDY Resolution Transition Setup Time(2)	15		15		15		10		ns
50	t_{CLARX}	ARDY Active Hold Time(1)	15		15		15		10		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	15		15		15		10		ns
52	t_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	25		25		25		20		ns
53	t_{INVCH}	INTx, NMI, TEST/BUSY, TMR IN Setup Time(2)	15		15		15		15		ns
54	t_{INVCL}	DRQ0, DRQ1, Setup Time(2)	15		15		15		15		ns
80C186 Peripheral and Queue Status Timing Responses											
55	t_{CLTMV}	Timer Output Delay		40		33		27		25	ns
56	t_{CHQSV}	Queue Status Delay		37		32		30		23	ns

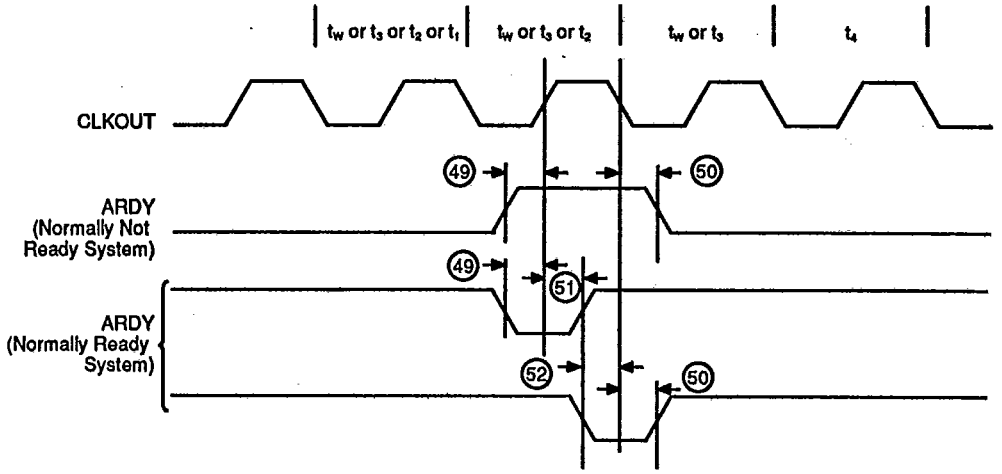
All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$–200 pF (10 MHz) and $C_L = 50$–100 pF (12.5–20 MHz).
For AC tests, input $V_{IL} = 0.45$ V and $V_{IH} = 2.4$ V except at X_1 where $V_{IH} = V_{CC} - 0.5$ V.

Notes: 1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

Synchronous Ready (SRDY) Waveforms



Asynchronous Ready (ARDY) Waveforms



Peripheral and Queue Status Waveforms