SC56D Modem

V.92/V.90 CX06827 Single Chip ACF Modem with Optional CX20437 Voice Codec

Data Sheet

Doc. No. 101098E
March 26, 2002

CONEXANT™

Revision Record

Revision	Date	Comments
E	3/26/2002	Revision E release. Supersedes 101098D.
D	3/15/2001	Revision D release. Supersedes 101098C.
C	10/26/2000	Revision C release. Supersedes 101098B.
B	9/6/2000	Revision B release. Supersedes 101098A.
A	6/26/2000	Initial release.

Reader Response: Conexant strives to produce quality documentation and welcomes your feedback. Please send comments and suggestions to tech.pubs@conexant.com. For technical questions, contact your local Conexant sales office or field applications engineer.

Contents

Figures

Tables

Revision History

Changes Incorporated in Doc. No. 101098E

1. Section 1.1: Added introduction to support for optional direct connect to an AMPS analog cellular phone and, for parallel host interface model, support for direct connect to a GSM phone.
2. Section 1.2.1: Added features for optional direct connect to an AMPS analog cellular phone, direct connect to a GSM phone (parallel host interface model), and fax class 2 commands. Revised serial maximum rate to 115.2 kbps.
3. Section 1.3.1: Added description for support for optional direct connect to an AMPS analog cellular phone and, for parallel host interface model, support for direct connect to a GSM phone.
4. Section 1.3.2: Added fax class 2 support.
5. Section 1.3.3.1: Added fax class 2 support.
6. Section 1.3.5: Added GSM supported features
7. Section 1.4: Added hardware descriptions for support or optional direct connect to an AMPS analog cellular phone and, for parallel host interface model, support for direct connect to a GSM phone.
8. Section 1.5: Added fax class 2 command support.
9. Section 2.1.1: Revised serial maximum rate to 115.2 kbps.
10. Section 2.4.5: Deleted Receive and Send Space Disconnect.
11. Section 2.6.3: Deleted V.44 parameter descriptions.
12. Section 2.10: Added Full-Duplex Receive and Transmit Mode to introductory text.
13. Section 2.13: Added Type I and Type II Caller ID support.
14. Section 2.16: Added GSM Operation description.
15. Section 3, throughout: Added interface signal descriptions for optional direct connect to an AMPS analog cellular phone and, for parallel host interface model, direct connect to a GSM phone.
16. Table 3-15: Revised timing values.

Changes Incorporated in Doc. No. 101098D

1. Throughout: reformatted.
2. Throughout: Added V.92, added V.44, added Call Waiting Caller ID Detect, and deleted K56flex functions
3. Figure 3-1: Added VOICE# and EXTOH# signals, swapped MIC_IN and LINE_IN signals.
4. Figure 3-2: Added VOICE# and EXTOH# signals.
5. Table 3-1: Added VOICE# and EXTOH# signals, swapped MIC_IN and LINE_IN signals.
6. Figure 3-3: Added VOICE# and EXTOH# signals, swapped MIC_IN and LINE_IN signals.

7. Figure 3-4: Added VOICE# and EXTOH# signals.
8. Table 3-2: Added VOICE# and EXTOH# signals, swapped MIC_IN and LINE_IN signals.
9. Table 3-3: Added VOICE# and EXTOH# signals, swapped MIC_IN and LINE_IN signals.

Changes Incorporated in Doc. No. 101098C

1. Section 1.2.1: Added power values.
2. Table 3-12: Added power values.

Changes Incorporated in Doc. No. 101098B

Throughout: Reformatted.

This page is intentionally blank.

1. Introduction

1.1 Overview

The Conexant™ SC56D V.92/V.90 Single Chip ACF Modem supports V.92 and V.90 analog data modem operation with V.44 data compression and supports 14.4 kbps fax modem operation. In addition, the modem supports remote TAM, speakerphone (optional), and parallel/serial host interface operation depending on model. Table 1-1 lists the available models. A simplified device interface drawing is shown in Figure 1-1. A functional interface drawing showing supporting memory is shown in Figure 1-2.

The modem operates with PSTN telephone lines worldwide and supports optional direct connect to an AMPS analog cellular phone. The parallel host interface model also supports direct connect to a GSM phone.

The CX06827 ACF device integrates modem controller (MCU), modem data pump (MDP), bootloader ROM, and analog line interface codec functions into a single 144-pin TQFP.

The modem operates by executing firmware from external flash ROM and RAM. Customized modem firmware and added/modified country profiles can also be executed from external memory, either from flash ROM or from serial EEPROM/flash ROM and RAM.

In V.92/V.90 (SC56 models) data mode, the modem can receive data at speeds up to 56 kbps from a digitally connected V.92/V.90-compatible central site modem. A V.92/V.90 modem takes advantage of the PSTN which is primarily digital except for the client modem to central office local loop and are ideal for applications such as remote access to an Internet Service Provider (ISP), on-line service, or corporate site. In this mode, the modem can transmit data at speeds up to 48 kbps in V.92 or up to V.34 rates in V.90.

In V.34 data mode (SC56 and SC33 models), the modem operates at line speeds up to 33.6 kbps.

In V.32 bis data mode, the modem operates at lines speeds up to 14.4 kbps.

Data compression (V.44/V.42 bis/MNP 5) and error correction (V.42/MNP 2-4) modes are supported to maximize data throughput and data transfer integrity. V.44 is a more efficient data compression than V.42 bis that significantly increases downstream throughput thus reducing the download time for the types of files associated with Internet use, such as Web pages and uncompressed files such as graphics, image, audio, and document files. V.44 data compression can achieve compression rates of more than 25% over V.42bis. Typical compression ratio for V.44 on Web type data is approximately 6-1 resulting in overall effective data throughput rate up to 300 kbps for a 56 kbps connection. Non-error-correcting mode is also supported.

In V.22 bis fast connect mode, the modem can connect at 2400 bps with a very short training time, which is very efficient for small data transfers.

Fax Group 3 send and receive rates are supported up to 14.4 kbps with T.30 protocol.

Downloadable architecture supports downloading of updated/upgraded or customized MCU firmware and MDP code modules from the host/DTE to the CX06827 ACF.

V.80 synchronous access mode supports host-controlled communication protocols, e. g., H.324 video conferencing.

In TAM mode, enhanced 2-bit or 4-bit per sample coding schemes at 8 kHz sample rate provide flexible format compatibility and allows efficient digital storage of voice/audio. Also supported are 8-bit linear and IMA 4-bit ADPCM coding. This mode supports applications such as digital telephone answering machine (TAM), voice annotation, and recording from and playback to the telephone line.

S models, using the optional CX20437 Voice Codec (VC) in a 32-pin TQFP, support position independent, full-duplex speakerphone (FDSP) operation using microphone and speaker, as well as other voice/TAM applications using handset or headset. S models can also support analog cellular operation with direct connection to an analog cellular phone (in lieu of a telephone handset/headset connection).

GSM operation supports data services offered by the Global System for Mobile Communications network: data transmissions to PSTN, ISDN or GSM users. GSM data operation allows data and fax transfer, and connection to videotex.

Analog cellular and GSM direct connect operation is supported by licensed firmware for specific phone types.

This data sheet describes the modem capabilities. Commands and parameters are defined in the Commands Reference Manual (Doc. No. 100722).

Table 1-1. CX06827 ACF Modem Models and Functions

Model/Order/Part Numbers				Supported Functions			
Marketing Name	**Device Set Order No.**	**Single Chip ACF Modem [144-Pin TQFP] Part No.**	**Voice Codec (VC) [32-Pin TQFP] Part No.**	**V.92/V.90 Data**	**V.34 Data,**	**V.32 bis Data, V.44 Data Compression, V.17 Fax, TAM**	**Voice/FDSP**
EMBEDDED APPLICATIONS							
SC56D	DS56-L147-021	CX06827-11	—	Y	Y	Y	—
SC56D/S	DS56-L147-031	CX06827-11	20437-11	Y	Y	Y	Y
SC336D	DS28-L147-021	CX06827-13	—	—	Y	Y	—
SC336D/S	DS28-L147-031	CX06827-13	20437-11	—	Y	Y	Y
SC144D	DS96-L147-021	CX06827-14	—	—	—	Y	—
SC144D/S	DS96-L147-031	CX06827-14	20437-11	—	—	Y	Y
AFTERMARKET APPLICATIONS							
SC56D	DS56-L144-301	CX06827-11	—	Y	Y	Y	—
SC56D/S	DS56-L144-311	CX06827-11	20437-11	Y	Y	Y	Y

Notes:

1. Model options:
   - S — Voice/full-duplex speakerphone (FDSP) and analog cellular
   - 56 — 56 kbps max. rate per V.90
   - 33 — 33.6 kbps max. rate per V.34
   - 14 — 14.4 kbps max. rate per V.32 bis.
2. Supported functions (Y = Supported; — = Not supported):
   - TAM — Telephone answering machine (Voice playback and record through telephone line)
   - FDSP — Full-duplex speakerphone and voice playback and record through telephone line, handset, and mic/speaker.
3. For ordering purposes, the CX prefix may not be included in the part number for some devices. Also, the CX prefix may not appear in the part number as branded on some devices.

Figure 1-1. CX06827 ACF Modem Simplified Interface Diagram

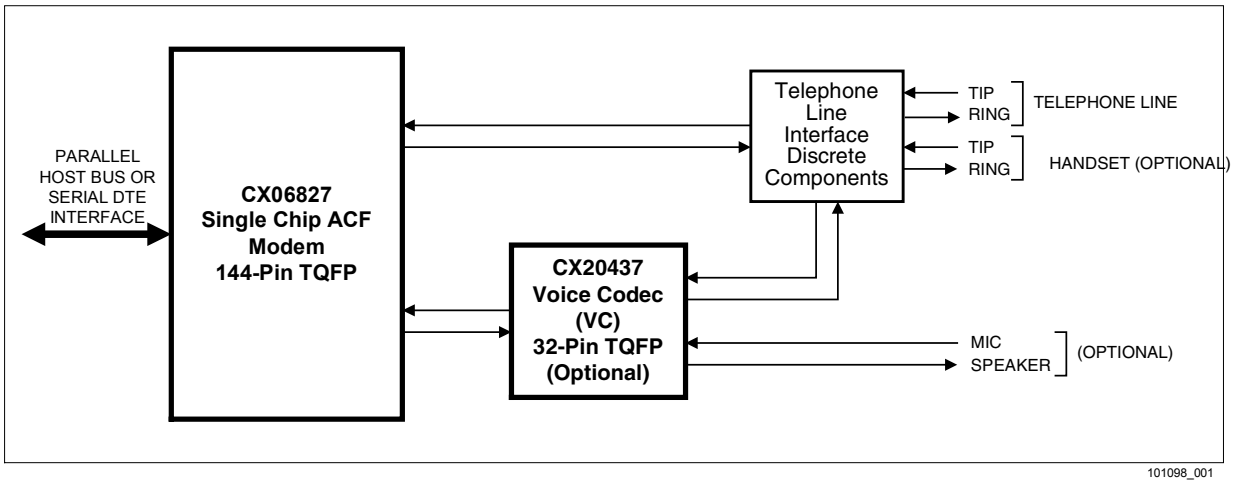
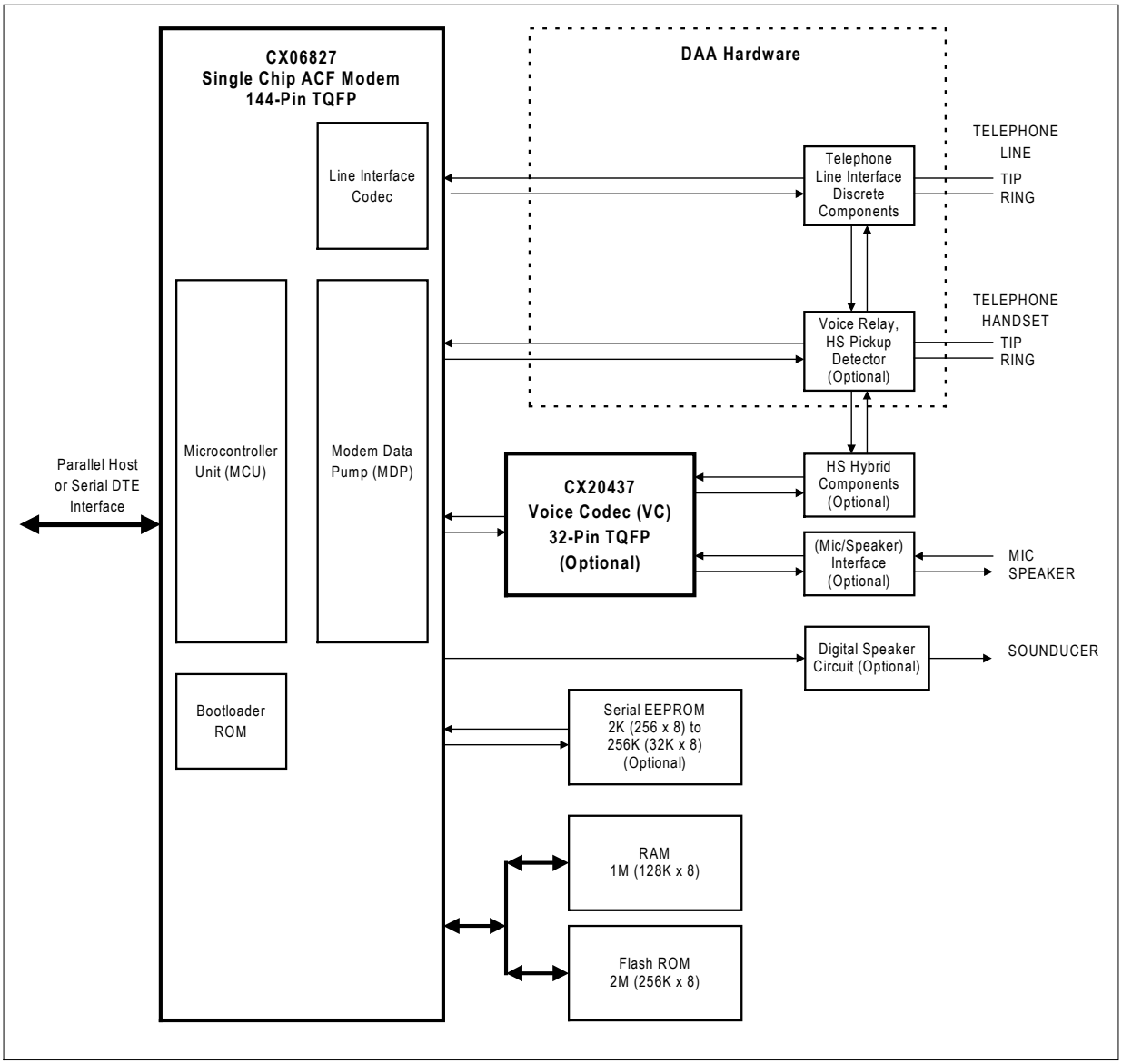


Figure 1-2. CX06827 ACF Modem Major Interfaces



1.2 Features

1.2.1 General Modem Features

- Data modem
  - ITU-T V.92 (SC56 models) with PCM upstream rates up to 48 kbps, QuickConnect, and Modem-on-hold functions
  - V.90 (SC56 models), V.34 (SC56 and SC33 models), V.32bis, V.32, V.22 bis, V.22, V.23, and V.21; Bell 212A and Bell 103
  - MNP 10EC™ enhanced cellular performance
  - V.250 and V.251 commands
  - V.22 bis fast connect
- Analog cellular direct connect using optional CX20437 Voice Codec (S models)
- GSM cellular direct connect (parallel interface only)
- Data compression and error correction
  - V.44 data compression for optimal downloading of Internet Web pages and files
  - V.42 bis and MNP 5 data compression
  - V.42 LAPM and MNP 2-4 error correction
- Fax modem
  - V.17, V.29, V.27 ter, and V.21 channel 2
  - EIA/TIA 578 Class 1 and T.31 Class 1.0, and EIA/TIA 578 Class 2 commands
- V.80 synchronous access mode supports host-controlled communication protocols with H.324 interface support
- Interfaces to external flash ROM, RAM, and optional serial EEPROM
- Downloadable Architecture
  - Downloadable MCU firmware from the host/DTE to flash ROM
  - Downloadable MDP code modules from the MCU transparent to the host
- Data/Fax/Voice call discrimination
- Hardware-based modem controller and digital signal processor (DSP)
- Worldwide operation
  - Complies to TBR21 and other country requirements
  - Caller ID detection
  - Call progress, blacklisting
  - External flash ROM includes default values for 29 countries
- Caller ID detect
  - On-hook Caller ID detection
  - Off-hook Call Waiting Caller ID detection during data mode in V.92, V.90, V.34 V.32bis, or V.32
- Distinctive ring detect
- Telephony/TAM
  - V.253 commands
  - 2-bit and 4-bit Conexant ADPCM, 8-bit linear PCM, and 4-bit IMA coding
  - 8 kHz sample rate
  - Concurrent DTMF, ring, and Caller ID detection

- Full-duplex speakerphone (FDSP) mode using optional CX20437 Voice Codec (S models)
  - Microphone and speaker interface
  - Telephone handset or headset interface
  - Acoustic and line echo cancellation
  - Microphone gain and muting
  - Speaker volume control and muting
- Built-in host/DTE interface
  - Parallel 16550A UART-compatible interface with speeds up to 230.4 kbps
  - Serial ITU-T V.24 (EIA/TIA-232-E) logical interface with speeds up to 115.2 kbps
- Direct mode (serial DTE interface)
- Flow control and speed buffering
- Automatic format/speed sensing
- Serial async/sync data; parallel async data
- Thin packages support low profile designs (1.6 mm max. height)
  - CX06827 ACF: 144-pin TQFP
  - CX20437 VC: 32-pin TQFP
- +3.3V operation with +5V tolerant digital inputs
- Typical power use
  - CX06827 ACF: 274 mW (Normal Mode); 27.7 mW (Sleep Mode)
  - CX20437 VC: 5 mW (Normal Mode)

1.2.2 Applications

- Desktop Modems
- Serial box modems
- Remote monitoring and data collection systems
- Standalone TAM/fax machines
- Set-top boxes

1.3 Technical Overview

1.3.1 General Description

Modem operation, including dialing, call progress, telephone line interface, telephone handset interface, optional voice/speakerphone interface, optional analog cellular phone interface, GSM interface, and host interface functions are supported and controlled through the V.250, V.251, and V.253-compatible command set.

The modem hardware connects to the host via a parallel or serial interface as selected by the PARIF input. The OEM adds a crystal circuit, flash ROM, RAM, telephone line interface, telephone handset/telephony extension interface, voice/speakerphone interface, cellular interface, GSM interface, optional external serial EEPROM, and other supporting discrete components as supported by the modem model (Table 1-1) and required by the application to complete the system.

Customized modem firmware and additional or modified country profiles can be supported by the use external flash ROM (optional serial EEPROM can also be used if external flash ROM capacity is exceeded). Customized code can include OEM-defined commands, i.e., identification codes (I3), identifier string (I4), manufacturer identification (+GMI), model identification (+GMM), and revision identification (+GMR), as well as code modification.

Parallel interface operation is selected by PARIF input high. Telephone line, cellular (AMPS) phone, or GSM phone interface operation is selected by the LINE/CELL and LINE/GSM inputs. Installation of cellular phone driver is also required for cellular phone interface operation. Installation of GSM firmware is also required for GSM phone interface operation.

Serial interface operation is selected by PARIF input low. Telephone line or cellular (AMPS) phone interface operation is selected by the LINE/CELL input. Installation of cellular phone driver is also required for cellular phone interface operation.

1.3.2 MCU Firmware

MCU firmware performs processing of general modem control, command sets, data modem, error correction and data compression (ECC), fax class 1, fax class 1.0, fax class 2, voice/audio/TAM/speakerphone, worldwide, V.80, and serial DTE/parallel host interface functions according to modem models.

MCU firmware can be customized to include OEM-defined commands, i.e., identification codes (I3), identifier string (I4), manufacturer identification (+GMI), model identification (+GMM), and revision identification (+GMR), as well as code modification.

The modem firmware is provided in object code form for the OEM to program into external flash ROM. The modem firmware may also be provided in source code form under a source code addendum license agreement.

1.3.3 Operating Modes

1.3.3.1 Data/Fax Modes

In V.92 data modem (SC56 models), the modem can support the following:

- Receive data from a digital source supporting V.92 over the digital telephone network portion of the PSTN at line speeds up to 56 kbps.
- PCM upstream which transmits data at line speeds up to 48 kbps.
- QuickConnect which allows quicker subsequent connection to a V.92 server using stored line parameters obtained during the initial connection.
- Modem-on-Hold which allows detection and reporting of incoming phone calls on the PSTN with enabled Call Waiting. If the incoming call is accepted by the user, the user has a pre-defined amount of time of holding the data connection for a brief conversation. The data connection resumes upon incoming call termination.
- V.92 mode can fallback to full-duplex V.90 mode.

In V.90 data modem mode (SC56 models), the modem can receive data from a digital source using a V.90-compatible central site modem over the digital telephone network portion of the PSTN at line speeds up to 56 kbps. Asymmetrical data transmission supports sending data at line speeds up to V.34 rates. This mode can fallback to full-duplex V.34 mode and to slower rates as dictated by line conditions.

In V.34 data modem mode (SC56 and SC33 models), the modem can operate in 2-wire, full-duplex, asynchronous modes at line rates up to 33.6 kbps. Data modem modes perform complete handshake and data rate negotiations. Using V.34 modulation to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps down to 2400 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standards are supported.

In V.32 bis data modem mode, the modem can operate at line speeds up to 14.4 kbps.

In V.22 bis fast connect data mode, the modem can connect at 2400 bps with a very short training time, which is very efficient for small data transfers.

In fax modem mode, the modem can operate in 2-wire, half-duplex, synchronous modes and can support Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps. Fax data transmission and reception performed by the modem are controlled and monitored through the EIA/TIA-578 Fax Class 1, T.31 Fax Class 1.0, or Fax Class 2 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking are provided.

1.3.3.2 V.44 Data Compression

V.44 provides more efficient data compression than V.42 bis that significantly decreases the download time for the types of files associated with Internet use. This significant improvement is most noticeable when browsing and searching the web since HTML text files are highly compressible. (The improved performance amount varies both with the actual format and with the content of individual pages and files.)

1.3.3.3 Synchronous Access Mode (SAM) - Video Conferencing

V.80 Synchronous Access Mode between the modem and the host/DTE is provided for host-controlled communication protocols, e.g., H.324 video conferencing applications.

Voice-call-first (VCF) before switching to a videophone call is also supported.

1.3.3.4 Worldwide Operation

The modem operates in TBR21-compliant and other countries. Country-dependent modem parameters for functions such as dialing, carrier transmit level, calling tone, call progress tone detection, answer tone detection, blacklisting, caller ID, and relay control are programmable (see Section 2.13).

Country code IDs are defined by ITU-T T.35.

External flash ROM includes default profiles for 29 countries including TBR21-compliant profiles. These profiles can be overridden by modified values stored in external serial EEPROM. A maximum of 31 country profiles can be stored in external flash ROM. Additional country profiles can be stored in external serial EEPROM (request additional country profiles from a Conexant Sales Office). The default countries supported are listed in Table 1-2.

Table 1-2. Default Supported Countries

Country	Country Code	Country	Country Code	Country	Country Code
Australia	09	India	53	Portugal	8B
Austria	0A	Ireland	57	Singapore	9C
Belgium	0F	Italy	59	South Africa	9F
Brazil	16	Japan	00	Spain	A0
China	26	Korea	61	Sweden	A5
Denmark	31	Malaysia	6C	Switzerland	A6
Finland	3C	Mexico	73	Taiwan	FE
France	3D	Netherlands	7B	United Kingdom	B4
Germany	42	Norway	82	United States	B5
Greece	46	Poland	8A		

1.3.3.5 TAM Mode

TAM Mode features include 8-bit linear coding at 8 kHz sample rate. Tone detection/generation, call discrimination, and concurrent DTMF detection are also supported. ADPCM (4-bit IMA) coding is also supported to meet Microsoft WHQL logo requirements.

TAM Mode is supported by four submodes:

- Online Voice Command Mode supports connection to the telephone line or, for S models, a microphone/speaker/handset/headset.
- Voice Receive Mode supports recording voice or audio data input from the telephone line or, for S models, a microphone/handset/headset.
- Voice Transmit Mode supports playback of voice or audio data to the telephone line or, for S models, a speaker/handset/headset.
- Full-duplex Receive and Transmit Mode.

1.3.3.6 Voice/Speakerphone Mode (S Models)

S models include additional telephone handset, external microphone, and external speaker interfaces which support voice and full-duplex speakerphone (FDSP) operation.

Hands-free full-duplex telephone operation is supported in Speakerphone Mode under host control. Speakerphone Mode features an advanced proprietary speakerphone algorithm which supports full-duplex voice conversation with acoustic, line, and handset echo cancellation. Parameters are constantly adjusted to maintain stability with automatic fallback from full-duplex to pseudo-duplex operation. The speakerphone algorithm allows position independent placement of microphone and speaker. The host can separately control volume, muting, and AGC in microphone and speaker channels.

1.3.4 Reference Design

A data/fax/TAM/speakerphone reference design for an external modem (RD00-D930) is available to minimize application design time, reduce development cost, and accelerate market entry.

A design package is available in electronic form. This package includes schematics, bill of materials (BOM), vendor part list (VPL), board layout files in Gerber format, and complete documentation.

1.3.5 GSM (Parallel Host Interface)

Supported GSM features include:

- Data modem
  - V.21, V.23, V.22, V.22 bis, V.32
  - ISDN interoperability: 300 bps to 9600 bps
- Transparent asynchronous mode up to 9600 bps
- Non-transparent mode (RLP) up to 9600 bps
- Fax modem send and receive rate up to 9600 bps
- AT GSM commands (ETSI 07.07)
- GSM direct connect
- Firmware interface for OEM-provided phone driver
- Automatic GSM cable presence detection
- Built-in parallel host (16550A UART) interface

GSM operation requires 1M of an external 4M (512k x 8) ROM/flash ROM.

1.4 Hardware Description

1.4.1 CX06827 Modem Controller and DSP

The CX06827 Modem Controller and DSP (ACF), packaged in a 144-pin TQFP, includes a Microcontroller (MCU), a Modem Data Pump (MDP), bootloader ROM, and line interface functions.

The ACF connects to host via a parallel host (PARIF = high) or a logical V.24 (EIA/TIA-232-E) serial DTE interface (PARIF = low).

The ACF performs the command processing and host interface functions. The crystal frequency is 28.224 MHz. The ACF also performs telephone line signal modulation/demodulation in a hardware digital signal processor (DSP) which reduces computational load on the host processor.

The ACF connects to external OEM-supplied flash ROM and RAM over a non-multiplexed 19-bit address bus and 8-bit data bus. GSM operation requires 1 Mbit of an external 4 Mbits (512k x 8) ROM/flash ROM.

The ACF optionally connects to an external OEM-supplied serial EEPROM over a dedicated 2-line serial interface. The capacity of the EEPROM can be 256 bytes up to 32k bytes. The EEPROM can hold information such as firmware configuration customization, country code parameters, and cellular drivers.

1.4.2 CX20437 Voice Codec

The optional CX20437 Voice Codec (VC), packaged in a 32-pin TQFP, supports voice/full-duplex speakerphone (FDSP) operation with interfaces to a microphone and speaker and to a telephone handset/headset. The VC also supports and analog cellular operation with direct connect interface to a cellular phone (in lieu of telephone handset/headset connection).

1.5 Commands

The modem supports data modem, fax class 1 and 1.0 modem, fax class 2 modem, voice/audio, FDSP, MNP 10/MNP 10EC, and V.80 commands, and S Registers depending upon modem model. See Doc. No. 100722 for a description of the commands.

Data Modem Operation. Data modem functions operate in response to the AT commands when +FCLASS=0. Default parameters support U.S./Canada operation.

MNP 10 Operation. MNP 10 functions operate in response to MNP 10 commands.

MNP 10EC Operation. MNP 10EC is enabled by the -SEC=1 command.

Fax Modem Operation. Facsimile functions operate in response to fax class 1 commands when +FCLASS=1, fax class 1.0 commands when +FCLASS=1.0, or to fax class 2 commands when +FCLASS=2.

Voice/Audio Operation. Voice/audio mode functions operate in response to voice/audio commands when +FCLASS=8.

Speakerphone Operation. FDSP functions operate in response to speakerphone commands when +FCLASS=8 and +VSP=1 is selected.

This page is intentionally blank.

2. Technical Specifications

2.1 Serial DTE Interface Operation

2.1.1 Automatic Speed/Format Sensing

Command Mode and Data Modem Mode. The modem can automatically determine the speed and format of the data sent from the DTE. The modem can sense speeds of 300, 600, 1200, 2400, 4800, 7200, 9600, 12000, 14400, 16800, 19200, 21600, 24000, 26400, 28800, 38400, 57600, and 115200 bps and the following data formats:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Character Length (No. of Bits)
None	7	2	10
Odd	7	1	10
Even	7	1	10
None	8	1	10
Odd	8	1	11*
Even	8	1	11*
*11-bit characters are sensed, but the parity bit is stripped off during data transmission in Normal and Error Correction modes.			

The modem can speed sense data with mark or space parity and configures itself as follows:

DTE Configuration	Modem Configuration
7 mark	7 none
7 space	8 none
8 mark	8 none
8 space	8 even

Fax Modem Mode. In V.17 fax mode, the modem can sense speeds up to 115.2 kbps.

2.2 Parallel Host Bus Interface Operation

Command Mode and Data Modem Mode. The modem can operate at rates up to 230.4 kbps by programming the Divisor Latch in the parallel interface registers if supported by communications software and/or driver (a Windows 95/98 driver is available from Conexant).

Fax Modem Mode. In V.17 mode, the modem can operate at rates up to 230.4 kbps by programming the Divisor Latch in the parallel interface registers if supported by communications software and/or driver (a Windows 95/98 driver is available from Conexant).

2.3 Establishing Data Modem Connections

2.3.1 Telephone Number Directory

The modem supports four telephone number entries in a directory that can be saved in a serial NVRAM. Each telephone number can be up to 32 characters (including the command line terminating carriage return) in length. A telephone number can be saved using the &Zn=x command, and a saved telephone number can be dialed using the DS=n command.

2.3.2 Dialing

DTMF Dialing. DTMF dialing using DTMF tone pairs is supported in accordance with ITU-T Q.23. The transmit tone level complies with Bell Publication 47001.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Blind Dialing. The modem can blind dial in the absence of a dial tone if enabled by the X0, X1, or X3 command.

2.3.3 Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

2.3.4 Call Progress Tone Detection

Ringback, equipment busy, congested tone, warble tone, and progress tones can be detected in accordance with the applicable standard.

2.3.5 Answer Tone Detection

Answer tone can be detected over the frequency range of 2100 ± 40 Hz in ITU-T modes and 2225 ± 40 Hz in Bell modes.

2.3.6 Ring Detection

A ring signal can be detected from a TTL-compatible 15.3 Hz to 68 Hz square wave input.

2.3.7 Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for 2 seconds (data modem) or 4 seconds (fax adaptive answer) to allow transmission of the billing tone signal.

2.3.8 Connection Speeds

The modem functions as a data modem when the +FCLASS=0 command is active.

Line connection can be selected using the +MS command. The +MS command selects modulation, enables/disables automode, and selects minimum and maximum line speeds (Table 2-1).

2.3.9 Automode

Automode detection can be enabled by the +MS command to allow the modem to connect to a remote modem in accordance with draft PN-3320 for V.34 (Table 2-1).

Table 2-1. +MS Command Automode Connectivity

<mod>	Modulation	Possible Rates (bps) [1]	Notes
V21	V.21	300	
V22	V.22	1200	
V22B	V.22 bis	2400 or 1200	
V23	V.23	1200	See Note 2
V32	V.32	9600 or 4800	
V32B	V.32 bis	14400, 12000, 9600, 7200, or 4800	Default for SC14 models
V34	V.34	33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, or 2400	Default for SC33 models
V90	V.90	56000, 54667, 53333, 52000, 50667, 49333, 48000, 46667, 45333, 44000, 42667, 41333, 40000, 38667, 37333, 36000, 34667, 33333, 32000, 30667, 29333, 28000	
V92	V.92	56000, 54667, 53333, 52000, 50667, 49333, 48000, 46667, 45333, 44000, 42667, 41333, 40000, 38667, 37333, 36000, 34667, 33333, 32000, 30667, 29333, 28000	Default for SC56 models
B103	Bell 103	300	
B212	Bell 212	1200	

Notes:

1. See optional <automode>, <min_rate>, and <max_rate> subparameters for the +MS command.
2. For V.23, originating modes transmit at 75 bps and receive at 1200 bps; answering modes transmit at 1200 bps and receive at 75 bps. The rate is always specified as 1200 bps. V.23 half duplex is not supported.
3. If the DTE speed is set to less than the maximum supported DCE speed in automode, the maximum connection speed is limited to the DTE speed.

2.4 Data Mode

Data mode exists when a telephone line connection has been established between modems and all handshaking has been completed.

2.4.1 Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send data to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

2.4.2 Flow Control

DTE-to-Modem Flow Control. If the modem-to-line speed is less than the DTE-to-modem speed, the modem supports XOFF/XON or RTS/CTS flow control with the DTE to ensure data integrity.

2.4.3 Escape Sequence Detection

The +++ escape sequence can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by an S2 Register value greater than 127.

2.4.4 BREAK Detection

The modem can detect a BREAK signal from either the DTE or the remote modem. The \Kn command determines the modem response to a received BREAK signal.

2.4.5 Telephone Line Monitoring

GSTN Cleardown (V.92, V.90, V.34, V.32 bis, V.32). Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Loss of Carrier (V.22 bis and Below). If carrier is lost for a time greater than specified by the S10 register, the modem disconnects (except MNP 10).

2.4.6 Fall Forward/Fallback (V.92/V.90/V.34/V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within V.92/V.90/V.34/V.32 bis/V.32 mode depending upon signal quality if automode is enabled by the +MS or N1 command.

When connected in V.92/V.90/V.34/V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within the current modulation depending upon signal quality if fall forward/fallback is enabled by the %E2 command.

2.4.7 Retrain

The modem may lose synchronization with the received line signal under poor or changing line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved, or until 30 seconds elapse resulting in line disconnect.

2.4.8 Programmable Inactivity Timer

The modem disconnects from the line if data is not sent or received for a specified length of time. In normal or error-correction mode, this inactivity timer is reset when data is received from either the DTE or from the line. This timer can be set to a value between 0 and 255 seconds by using register S30. A value of 0 disables the inactivity timer.

2.4.9 DTE Signal Monitoring (Serial DTE Interface Only)

DTR#. When DTR# is asserted, the modem responds in accordance with the &Dn and &Qn commands.

RTS#. RTS# is used for flow control if enabled by the &K command in normal or error-correction mode.

2.5 Modem-on-Hold

The Modem-on-Hold (MOH) function enables the modem to place a data call to the Internet on hold while using the same line to accept an incoming or place an outgoing voice call. This feature is available only with a connection to a V.92 server and can be executed through two methods.

One method is to enable MOH through the +PMH command. With Call Waiting Detection (+PCW command) enabled, an incoming call can be detected while on-line. Using a string of commands, the modem negotiates with the server to place the data connection on hold while the line is released so that it can be used to conduct a voice call. Once the voice call is completed, the modem can quickly renegotiate with the server back to the original data call.

An alternative method is to use communications software that makes use of the Conexant Modem-on-Hold drivers. Using this method, the software can detect an incoming call, place the data connection on hold, and switch back to a data connection.

2.6 Error Correction and Data Compression

2.6.1 V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a fallback, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the best method of error correction between two modems.

2.6.2 MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. Supporting stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

2.6.3 V.44 Data Compression

V.44 data compression encodes pages and files associated with Web pages more efficiently than V.42 bis. These files include WEB pages, graphics and image files, and document files. V.44 can provide an effective data throughput rate up to DTE rate for a 56-kbps connection. The improved performance amount varies both with the actual format and with the content of individual pages and files.

V.44 data compression is controlled by the +DS44 extended-format compound parameter.

2.6.4 V.42 bis Data Compression

V.42 bis data compression mode, enabled by the %Cn command or S46 register, operates when a LAPM or MNP 10 connection is established.

The V.42 bis data compression employs a “string learning” algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two 2k-byte dictionaries are used to store the strings. These dictionaries are dynamically updated during normal operation.

2.6.5 MNP 5 Data Compression

MNP 5 data compression mode, enabled by the %Cn command, operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

2.7 MNP 10 Data Throughput Enhancement

MNP 10 protocol and MNP Extended Services enhance performance under adverse channel conditions such as those found in rural, long distance, or cellular environments. An MNP 10 connection is established when an MNP 2-4 connection is negotiated with a remote modem supporting MNP 10.

MNP Extended Services. The modem can quickly switch to MNP 10 operation when the remote modem supports MNP 10 and both modems are configured to operate in V.42.

V.42 bis/MNP 5 Support. V.42 bis/MNP 10 can operate with V.42 bis or MNP 5 data compression.

2.8 MNP 10EC™ Enhanced Cellular Connection

A traditional landline modem, when used for high-speed cellular data transmission, typically encounters frequent signal interference and degradation in the connection due to the characteristics of the analog cellular network. In this case, cellular-specific network impairments, such as non-linear distortion, fading, hand-offs, and high signal-to-noise ratio, contribute to an unreliable connection and lower data transfer performance. Implementations relying solely on protocol layer methods, such as MNP 10, generally cannot compensate for the landline modem's degraded cellular channel performance.

The modem achieves higher cellular performance by implementing enhanced cellular connection techniques at both the physical and protocol layers, depending on modem model. The modem enhances the physical layer within the modulation by optimizing its responses to sudden changes in the cellular connection. The MNP 10EC protocol layer implemented in the modem firmware improves data error identification/correction and maximizes data throughput by dynamically adjusting speed and packet size based on signal quality and data error performance.

2.9 Fax Class 1 and Fax Class 1.0 Operation

Facsimile functions operate in response to fax class 1 commands when +FCLASS=1 or to fax class 1.0 commands when +FCLASS=1.0.

In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by fax commands. Some AT commands are still valid but may operate differently than in data modem mode.

Calling tone is generated in accordance with T.30.

2.10 Voice/Audio Mode

Voice and audio functions are supported by the Voice Mode. Voice Mode includes four submodes: Online Voice Command Mode, Voice Receive Mode, Voice Transmit Mode, and Full-Duplex Receive and Transmit Mode.

2.10.1 Online Voice Command Mode

This mode results from the connection to the telephone line or a voice/audio I/O device (e.g., microphone, speaker, or handset) through the use of the +FCLASS=8 and +VLS commands. After mode entry, AT commands can be entered without aborting the connection.

2.10.2 Voice Receive Mode

This mode is entered when the +VRX command is active in order to record voice or audio data input at the RIN pin, typically from a microphone/handset or the telephone line.

Received analog voice samples are converted to digital form and compressed for reading by the host. AT commands control the codec bits-per-sample rate.

Received analog mono audio samples are converted to digital form and formatted into 8-bit unsigned linear PCM format for reading by the host. AT commands control the bit length and sampling rate. Concurrent DTMF/tone detection is available at the 8 kHz sample rate.

2.10.3 Voice Transmit Mode

This mode is entered when the +VTX command is active in order to playback voice or audio data to the TXA output, typically to a speaker/handset or to the telephone line.

Digitized voice data is decompressed and converted to analog form at the original compression quantization sample-per-bits rate then output to the TXA output.

Digitized audio data is converted to analog form then output to the TXA output.

2.10.4 Full-Duplex Receive and Transmit Mode

This mode is entered when the +VTR command is active in order to concurrently receive and transmit voice.

2.10.5 Audio Mode

The audio mode enables the host to transmit and receive 8-bit audio signals. In this mode, the modem directly accesses the internal analog-to-digital (A/D) converter (ADC) and the digital-to-analog (D/A) converter (DAC). Incoming analog audio signals can then be converted to digital format and digital signals can be converted to analog audio output.

2.10.6 Tone Detectors

The tone detector signal path is separate from the main received signal path thus enabling tone detection to be independent of the configuration status. In Tone Mode, all three tone detectors are operational.

2.10.7 Speakerphone Modes

Speakerphone modes are controlled in voice mode with the following commands:

Use Speakerphone After Dialing or Answering (+VSP=1). +VSP=1 selects speakerphone mode while in +FCLASS=8 mode. Speakerphone operation is entered during Voice Online Command mode after completing dialing or answering.

Speakerphone Settings. The +VGM and +VGS commands can be used to control the microphone gain and speaker volume, respectively. VGM and +VGS commands are valid only after the modem has entered the Voice Online mode while in the +VSP=1 setting.

2.11 Full-Duplex Speakerphone (FDSP) Mode (S Model)

The modem operates in FDSP mode when +FCLASS=8 and +VSP=1 (Section 2.10.7).

In FDSP Mode, speech from a microphone or handset is converted to digital form, shaped, and output to the telephone line through the line interface circuit. Speech received from the telephone line is shaped, converted to analog form, and output to the speaker or handset. Shaping includes both acoustic and line echo cancellation.

2.12 Caller ID

Both Type I Caller ID (On-Hook Caller ID) and Type II Caller ID (Call Waiting Caller ID) are supported for U.S. and many other countries (see Section 2.13). Both types of Caller ID are enabled/disabled using the +VCID command. Call Waiting Tone detection must be enabled using the +PCW command to detect and decode Call Waiting Caller ID. When enabled, caller ID information (date, time, caller code, and name) can be passed to the DTE in formatted or unformatted form. Inquiry support allows the current caller ID mode and mode capabilities of the modem to be retrieved from the modem.

Type II Caller ID (Call Waiting Caller ID) detection operates only during data mode in V.92, V.90, V.34, V.32bis, or V.32.

2.13 Worldwide Country Support

Internal modem firmware supports 29 country profiles (see Section 1.3.2). These country profiles include the following country-dependent parameters:

- Dial tone detection levels and frequency ranges.
- DTMF dialing parameters: Transmit output level, DTMF signal duration, and DTMF interdigit interval.
- Pulse dialing parameters: Make/break times, set/clear times, and dial codes are programmable
- Ring detection frequency range.
- Type I and Type II Caller ID are supported for many countries. Consult firmware release notes for a list of the supported countries and the criteria for additional country support.
- Blind dialing enabled/disable.
- Carrier transmit level (through S91 for data and S92 for fax). The maximum, minimum, and default values can be defined to match specific country and DAA requirements.
- Calling tone is generated in accordance with V.25. Calling tone may be toggled (enabled/disabled) by inclusion of a "^" character in a dial string. It may also be disabled.
- Frequency and cadence of tones for busy, ringback, congested, warble, dial tone 1, and dial tone 2.
- Answer tone detection period.
- Blacklist parameters. The modem can operate in accordance with requirements of individual countries to prevent misuse of the network by limiting repeated calls to the same number when previous call attempts have failed. Call failure can be detected for reasons such as no dial tone, number busy, no answer, no ringback detected, voice (rather than modem) detected, and key abort (dial attempt aborted by user). Actions resulting from such failures can include specification of minimum inter-call delay, extended delay between calls, and maximum numbers of retries before the number is permanently forbidden ("blacklisted").

These country profiles may be altered or customized by modifying the country-dependent parameters. Additional profiles may also be included. There are two ways to add or modify profiles:

- Incorporating additional or modified profiles into external flash ROM containing the entire modem firmware code.
- Linking additional or modified profiles from an external serial EEPROM (needed only if the external flash ROM capacity is exceeded.

Please contact an FAE at the local Conexant sales office if a country code customization is required.

2.14 Diagnostics

2.14.1 Commanded Tests

Diagnostics are performed in response to &T commands.

Analog Loopback (&T1 Command). Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

2.14.2 Power On Reset Tests

Upon power on, the modem performs tests of the modem, internal and external RAM, and NVRAM. If the modem, internal RAM, or external RAM test fails, the TMIND# output is pulsed (serial interface version) or the DCD bit in the parallel interface register is pulsed (parallel interface version) as follows:

- Internal or external RAM test fails: One pulse cycle (pulse cycle = 0.5 sec. on, 0.5 sec. off) every 1.5 seconds.
- Modem device test fails: Three pulse cycles every 1.5 seconds.

If the NVRAM test fails (due to NVRAM failure or if NVRAM is not installed), the test failure is reported by AT commands that normally use the NVRAM, e.g., the &V command.

2.15 Low Power Sleep Mode

Sleep Mode Entry. The modem enters the low power sleep mode when no line connection exists and no host activity occurs for the period of time specified in the S24 register. All modem circuits are turned off except the internal clock circuitry in order to consume reduced power while being able to immediately wake up and resume normal operation.

Wake-up. Wake-up occurs when a ring is detected on the telephone line, the host writes to the modem (parallel interface), or the DTE sends a character to the modem (serial interface).

2.16 GSM Operation

Once the modem is connected to the GSM phone and the phone is powered on, dial/answer functions will be routed through the phone instead of the wireline DAA. No special commands are needed to place or answer GSM calls and the same AT commands and software packages that are used for wireline communication sessions can be used.

While the modem is being used with a GSM phone, result messages are changed from wireline operation status to reflect GSM operation status as follows:

NO DIALTONE - Indicates that GSM service is not currently available or the cellular phone is powered off.

RING - Indicates that the GSM phone is receiving an incoming call.

BUSY - The network reports the number dialed is busy.

CARRIER - The carrier is established with the IWF (Interworking function) modem.

PROTOCOL RLP - The error corrected protocol on the radio link is established.

This page is intentionally blank.

3. Hardware Interface

3.1 CX06827 ACF Hardware Pins and Signals

3.1.1 CX06827 ACF Interface Signals

ACF hardware interface signals for parallel interface are shown by major interface in Figure 3-1, are shown by pin number in Figure 3-2, and are listed by pin number in Table 3-1. The ACF hardware interface signals for parallel interface are defined in Table 3-2.

ACF hardware interface signals for serial interface are shown by major interface Figure 3-3, are shown by pin number in Figure 3-4, and are listed by pin number in Table 3-3. The ACF hardware interface signals for serial interface are defined in Table 3-4.

ACF I/O types are defined in Table 3-5.

ACF DC electrical characteristics are listed in Table 3-6.

Figure 3-1. CX06827 ACF Hardware Signals for Parallel Interface (PARIF = High)

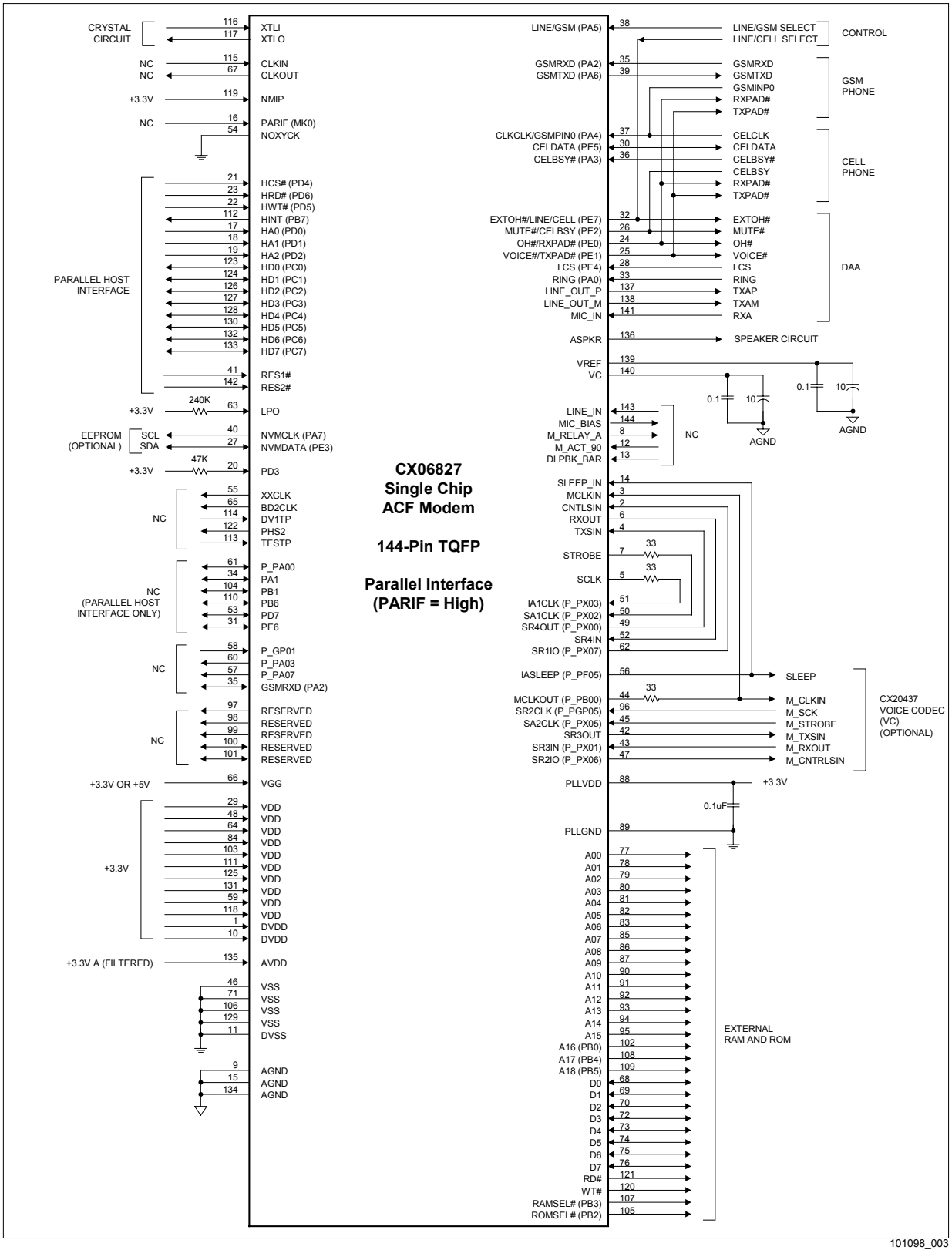
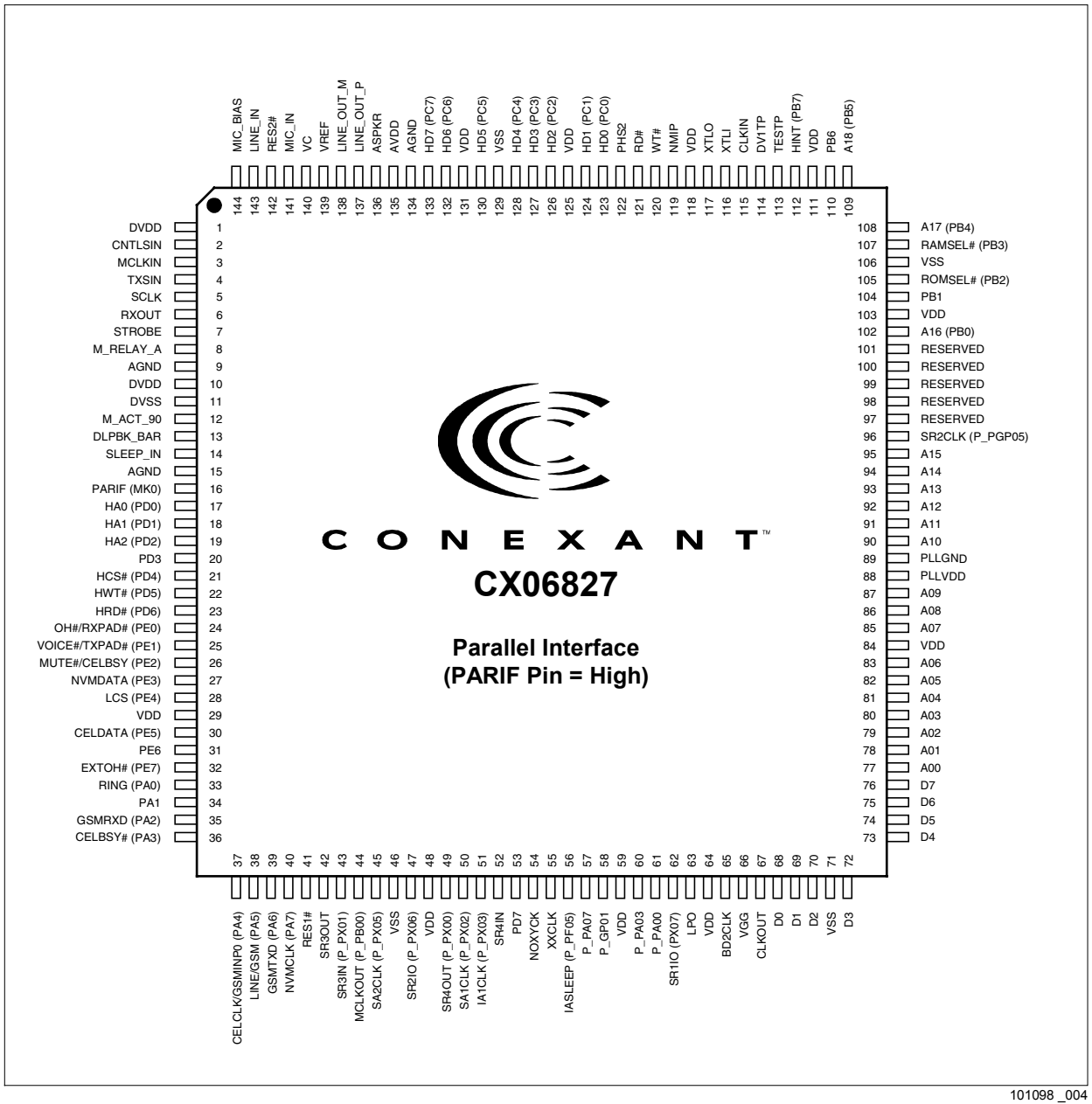


Figure 3-2. CX06827 ACF 144-Pin TQFP Pin Signals for Parallel Interface (PARIF = High)



101098 _004

Table 3-1. CX06827 ACF 144-Pin TQFP Pin Signals for Parallel Interface (PARIF = High)

Pin	Signal Label	I/O	Interface	Pin	Signal Label	I/O	Interface
1	DVDD	P	+3.3V	73	D4	I/O	EB: D4
2	CNTLSIN	I	ACF: SR1IO	74	D5	I/O	EB: D5
3	MCLKIN	I	ACF: MCLKOUT through 33 ohms	75	D6	I/O	EB: D6
4	TXSIN	I	ACF: SR4OUT	76	D7	I/O	EB: D7
5	SCLK	O	ACF: IA1CLK through 33 ohms	77	A00	O	EB: A00
6	RXOUT	O	ACF: SR4IN	78	A01	O	EB: A01
7	STROBE	O	ACF:SA1CLK through 33 ohms	79	A02	O	EB: A02
8	M_RELAY_A	O	NC	80	A03	O	EB: A03
9	AGND	G	AGND	81	A04	O	EB: A04
10	DVDD	P	+3.3V	82	A05	O	EB: A05
11	DVSS	G	GND	83	A06	O	EB: A06
12	M_ACT_90	I	NC	84	VDD	P	+3.3V
13	DLPBK_BAR	I	NC	85	A07	O	EB: A07
14	SLEEP_IN	I	ACF: IASLEEP	86	A08	O	EB: A08
15	AGND	G	AGND	87	A09	O	EB: A09
16	PARIF (MK0)	I	NC (Parallel Host)	88	PLLVDD	P	+3.3V and to GND through 1 µF
17	HA0 (PD0)	I	HB: HA0	89	PLLGND	G	GND
18	HA1 (PD1)	I	HB: HA1	90	A10	O	EB: A10
19	HA2 (PD2)	I	HB: HA2	91	A11	O	EB: A11
20	PD3	I	+3.3V through 47 K	92	A12	O	EB: A12
21	HCS# (PD4)	I	HB: CS#	93	A13	O	EB: A13
22	HWT# (PD5)	I	HB: WT#	94	A14	O	EB: A14
23	HRD# (PD6)	I	HB: RD#	95	A15	O	EB: A15
24	OH#/RXPAD# (PE0)	O	DAA: Off-Hook Relay Circuit; CELL/GSM: RXPAD#	96	SR2CLK (P_PGP05)	I	VC: M_SCK
25	VOICE#/TXPAD# (PE1)	O	DAA: Voice Relay Circuit (Optional); DAA: VOICE#; CELL/GSM:TXPAD#	97	RESERVED	I/O	NC
26	MUTE#/CELBSY (PE2)	O	DAA: Mute Circuit (Optional); CELL: CELBSY	98	RESERVED	I/O	NC
27	NVMDATA (PE3)	I/O	NVRAM: SDA	99	RESERVED	O	NC
28	LCS (PE4)	I	DAA: Line Current Sense Circuit	100	RESERVED	O	NC
29	VDD	P	+3.3V	101	RESERVED	O	NC
30	CELDATA (PE5)	I	CELL: CEL_DATA	102	A16 (PB0)	O	EB: A16
31	PE6	I/O	NC	103	VDD	P	+3.3V
32	EXTOH#/ LINE/CELL (PE7)	I	DAA: Extension Pickup Circuit (Optional); Line/Cell select	104	PB1	I/O	NC
33	RING (PA0)	I	DAA: Ring Detect Circuit	105	ROMSEL# (PB2)	O	EB: ROM CE#
34	PA1	I/O	NC	106	GND	G	GND
35	GSMRXD (PA2)	I	GSM: GSMRXD	107	RAMSEL# (PB3)	O	EB: RAM CS#
36	CELBSY# (PA3)	I	CELL: CELBSY#	108	A17 (PB4)	O	EB: A17
37	CELCLK/ GSMINP0 (PA4)	I	CELL: CELCLK; GSM: GSMINP0	109	A18 (PB5)	O	EB: A18
38	LINE/GSM (PA5)	I	Line/GSM select	110	PB6	I/O	NC
39	GSMTXD (PA6)	O	GSM: GSMTXD	111	VDD	P	+3.3V
40	NVMCLK (PA7)	O	NVRAM: SCL	112	HINT (PB7)	O	HB: HINT
41	RES1#	I	HB: RESET#	113	TESTP	I	NC
42	SR3OUT	O	VC: M_TXSIN	114	DV1TP	I	NC
43	SR3IN (P_PX01)	I	VC: M_RXOUT	115	CLKIN	I	NC
44	MCLKOUT (P_PB00)	O	Through 33 ohms to ACF:MCLKIN and VC: M_CLKIN	116	XTLI	I	Crystal Circuit
45	SA2CLK (P_PX05)	I	VC: M_STROBE	117	XTLO	O	Crystal Circuit
46	GND	G	GND	118	VDD	P	+3.3V
47	SR2IO (P_PX06)	O	VC: M_CNTRLSIN	119	NMIP	I	+3.3V
48	VDD	P	+3.3V	120	WT#	O	EB: WRITE#

Table 3-1. CX06827 ACF 144-Pin TQFP Pin Signals for Parallel Interface (PARIF = High) (Continued)

Pin	Signal Label	I/O	Interface	Pin	Signal Label	I/O	Interface
49	SR4OUT (P_PX00)	O	ACF: TXSIN	121	RD#	O	EB: READ#
50	SA1CLK (P_PX02)	I	ACF: STROBE through 33 ohms	122	PHS2	O	NC
51	IA1CLK (P_PX03)	I	ACF: SCLK through 33 ohms	123	HD0 (PC0)	I/O	HB: HD0
52	SR4IN	I	ACF: RXOUT	124	HD1 (PC1)	I/O	HB: HD1
53	PD7	I/O	NC	125	VDD	P	+3.3V
54	NOXYCK	I	GND	126	HD2 (PC2)	I/O	HB: HD2
55	XXCLK	O	NC	127	HD3 (PC3)	I/O	HB: HD3
56	IASLEEP (P_PF05)	O	VC: SLEEP	128	HD4 (PC4)	I/O	HB: HD4
57	P_PA07	O	NC	129	GND	G	GND
58	P_GP01	I	NC	130	HD5 (PC5)	I/O	HB: HD5
59	VDD	P	+3.3V	131	VDD	P	+3.3V
60	P_PA03	O	NC	132	HD6 (PC6)	I/O	HB: HD6
61	P_PA00	I/O	NC	133	HD7 (PC7)	I/O	HB: HD7
62	SR1IO (P_PX07)	O	ACF: CNTLSIN	134	AGND	G	AGND
63	LPO	I	+3.3V through 240K	135	AVDD	P	+3.3VA (Filtered)
64	VDD	P	+3.3V	136	ASPKR	O	AI: Speaker Circuit
65	BD2CLK	O	NC	137	LINE_OUT_P	O	DAA: TXAP
66	VGG	R	+5V or +3.3V	138	LINE_OUT_M	O	DAA: TXAM
67	CLKOUT	O	NC	139	VREF	R	AGND through C circuit
68	D0	I/O	EB: D0	140	VC	R	AGND through C circuit
69	D1	I/O	EB: D1	141	MIC_IN	I	DAA: RXA
70	D2	I/O	EB: D2	142	RES2#	I	HB: RESET#
71	GND	G	GND	143	LINE_IN	I	NC
72	D3	I/O	EB: D3	144	MIC_BIAS	O	NC

Table 3-2. CX06827 ACF Pin Signal Definitions for Parallel Interface (PARIF = High)

Label	Pin	I/O	I/O Type	Signal Name/Description
System				
XTLI, XTLO	116, 117	I, O	Ix, Ox	**Crystal In and Crystal Out.** If an external 28.224 MHz crystal circuit is used instead of an external clock circuit, connect XTLI and XTLO to the external crystal circuit and leave CLKIN open.
CLKIN	115	I	It	**Clock In.** If an external 28.224 MHz clock circuit is used instead of an external crystal circuit, connect CLKIN to the clock output and leave XTLI and XTLO open.
CLKOUT	67	O	It/Ot2	**Clock Out.** 28.224 MHz output clock. Leave open.
NOXYCK	54	I	Itpu	**Disable XCLK Output.** Low disables XCLK output (reduces internal power consumption). High enables XCLK output.
PARIF	16	I	Itpu	**Parallel/Serial Interface Select.** PARIF input high (open) selects parallel host interface operation. PARIF low (GND) selects serial DTE interface operation.
NMI#	119	I	Ithpu	**Non-Maskable Interrupt.** Not used. Connect to +3.3V.
RES1# RES2#	41 142	I	It	**Reset.** The active low RES1# and RES2# input resets the ACF logic, and restores the saved configuration from serial EEPROM or returns the modem to the factory default values if NVRAM is not present. RESET# low holds the modem in the reset state; RESET# going high releases the modem from the reset state. After application of VDD, RESET# must be held low for at least 15 ms after the VDD power reaches operating range. The modem device set is ready to use 25 ms after the low-to-high transition of RESET#. For parallel Interface, connect RESET# input to the host bus RESET line through an inverter. For serial Interface, connect RESET# input to a reset switch circuit.
Power and Ground				
VGG	66	P	PWRG	**I/O Signaling Voltage Source.** Connect to +5V or +3.3V.
VDD	29, 48, 59, 64, 66, 84, 103, 111, 118, 125, 131	P	PWR	**Digital Supply Voltage for Digital Circuits.** Connect to +3.3V.
DVDD	1, 10	P	PWR	**Digital Supply Voltage for Analog Circuits.** Connect to +3.3V
AVDD	135	P	PWR	**Analog Supply Voltage for Analog Circuits.** Connect to analog power.
VSS	46, 71, 106, 129	G	GND	**Digital Ground for Digital Circuits.** Connect to digital ground.
DVSS	11	G	GND	**Digital Ground for Analog Circuits.** Connect to digital ground.
AGND	9, 15, 134	G	AGND	**Analog Ground for Analog Circuits.** Connect to analog ground.
PLLVDD	88	P	PWR	**Supply Voltage for PLL Circuit.** Connect to +3.3V and to analog ground through 0.1 μF.
PLLGND	89	G	GND	**Digital Ground for PLL Circuit.** Connect to digital ground.
Serial EEPROM (NVRAM) Interface				
NVMCLK (PA7)	40	O	It/Ot2	**NVRAM Clock.** NVMCLK output high enables the EEPROM. Connect to the EEPROM SCL pin.
NVMDATA (PE3)	27	I/O	It/Ot2	**NVRAM Data.** NVMDATA supplies serial data to and from the EEPROM. Connect to the EEPROM SDA pin and to +3.3V through 10 KΩ.

Table 3-2. CX06827 ACF Pin Signal Definitions for Parallel Interface (PARIF = High)

Label	Pin	I/O	I/O Type	Signal Name/Description
External Bus Interface				
A00-A06, A07-A09, A10-A15, A16 (PB0), A17 (PB4), A18 (PB5)	77-83, 85-87, 90-95, 102, 108, 109	O, O, O, O, O, O	It/Ot8, It/Ot8, It/Ot2, It/Ot2, It/Ot2, It/Ot2	**Address Lines 0-18.** A0-A18 are the address output lines used to access external memory; up to 4 Mbits (512k bytes) flash ROM using A0-A18 and up to 1 Mbit (128k bytes) RAM using A0-A16.
D0-D2, D3-D7	68-70, 72-76	I/O	Ith/Ot2	**Data Line 0-7.** D0-D7 are bidirectional external memory bus data lines.
READ#	121	O	It/Ot2	**Read Enable.** READ# output low enables data transfer from the selected device to the D0-D7 lines.
WRITE#	120	O	It/Ot2	**Write Enable.** WRITE# output low enables data transfer from the D0-D7 lines to the selected device.
RAMSEL# PB3)	107	O	It/Ot2	**RAM Select.** RAMSEL# output low selects the external RAM.
ROMSEL# (PB2)	105	O	Ot2	**ROM Select**. ROMSEL# output low selects the external flash ROM.
Telephone Line/Telephone/Audio Interface Signals and Reference Voltage				
OH#/RXPAD# (PE0)	24	O	It/Ot2	**Off-Hook Relay Control.** The active low output can be used to control the normally open off-hook relay.
VOICE#/TXPAD# (PE1)	25	O	It/Ot2	**Voice Relay Control.** The active low VOICE# output can optionally be used to switch the handset from the telephone line to the voice codec interface to be used as a microphone and speaker. Leave open if not used.
MUTE#/CELBSY (PE2)	26	O	It/Ot2	**Mute Relay Control.** The active low MUTE# output can optionally be used to used to control the normally open mute relay. Leave open if not used.
LCS (PE4)	28	I	It/Ot2	**Loop Current Sense.** LCS is an active high input that indicates a handset off-hook status.
EXTOH#/LINE/CELL (PE7)	32	I	It/Ot2	**Extension Off-Hook.** Active low input optionally used to indicate when the telephone handset connected to the modem goes off-hook state. Connect to +3.3V through 47K Ω if not used.
RING (PA0)	33	I	It/Ot2	**Ring Frequency.** A rising edge on the RING input initiates an internal ring frequency measurement. The RING input from an external ring detect circuit is monitored to determine when to wake up from sleep or stop mode. The RING input is typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be low.
LINE_OUT_P, LINE_OUT_M	137, 138	O, O	O(DF)	**Transmit Analog 1 and 2.** The LINE_OUT_P and LINE_OUT_M outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 Ω load. Connect LINE_OUT_P and LINE_OUT_M to the DAA telephone line interface transmit circuit.
MIC_IN	141	I	I(DA)	**Receive Analog.** MIC_IN is a single-ended input from the telephone line interface or an optional external hybrid circuit with 70K Ω input impedance. Connect MIC_IN to the DAA telephone line interface receive circuit.
VREF	139	R	REF	**High Voltage Reference.** Connect to AGND through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VREF pin. Use a short path and a wide trace to AGND pin.
VC	140	R	REF	**Low Voltage Reference.** Connect to AGND through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VC pin. Use a short path and a wide trace to AGND pin.

Table 3-2. CX06827 ACF Pin Signal Definitions for Parallel Interface (PARIF = High)

Label	Pin	I/O	I/O Type	Signal Name/Description
Telephone Line/Telephone/Audio Interface Signals and Reference Voltage (Continued)				
ASPKR	136	O	O(DF)	**Speaker Analog Output.** The ASPKR analog output can originate from one of five different sources: RIN, TELIN, MICM or MICV or from the MDP's internal voice playback mode. The ASPKR on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the ASPKR output is clamped to the voltage at the VC pin. The ASPKR output can drive an impedance as low as 300 ohms. In a typical application, the ASPKR output is an input to an external LM386 audio power amplifier.
LINE_IN	143	I	I(DA)	**Not Used.** Leave open.
MIC_BIAS	144	O	Oa	**Not Used.** Leave open.
M_RELAYA	8	O	Ot	**Not Used.** Leave open.
M_ACT90	12	I	Itpu	**Not Used.** Leave open.
DLPBK_BAR	13	I	It	**Not Used.** Leave open.
Telephone Line/Analog Cellular Phone/GSM Phone Interface Select				
LINE/GSM (PA5)	38	I	It/Ot2	**Line/GSM Interface Select.** In conjunction with the LINE/CELL input, selects telephone line, cellular phone (AMPS), or GSM phone interface.
LINE/CELL (PE7)	32	I	It/Ot8	**Line/Cellar Interface Select.** In conjunction with the LINE/GSM input, selects telephone line, cellular phone (AMPS), or GSM phone interface, as follows: **LINE/CELL** / **LINE/GSM** / **Interface Selected** H / H / Telephone Line L / H / Cellular (AMPS) H / L / GSM L / L / Invalid The following ports operate as indicated for the selected interface: **Port** / **Telephone Line** / **Analog Cellular** / **GSM** PE0 / — / RXPAD# / RXPAD# PE1 / VOICE# / TXPAD# / TXPAD# PE2 / — / CELBSY / — PE5 / — / CELDATA / — PA2 / — / — / GSMRXD PA3 / — / CELBSY# / — PA4 / — / CELCLK / GSMINP0 PA6 / — / — / GSMTXD **Note:** Ports marked "—" are not used.
Analog Cellular Phone Interface (LINE/CELL = Low and LINE/GSM = High)				
CELCLK/GSMINP0 (PA4)	37	I	Itpu/Ot2	**Cellular Clock.** Defined by the cellular firmware driver.
CELDATA (PE5)	30	I/O	It/Ot2	**Cellular Data**. Defined by the cellular firmware driver.
MUTE#/CELBSY (PE2)	26	O	It/Ot2	**Cellular Busy.** Defined by the cellular firmware driver.
CELBSY# (PA3)	36	I	Itpu/Ot2	**Cellular Not Busy.** Defined by the cellular firmware driver.
OH#/RXPAD# (PE0)	24	O	It/Ot8	**Cellular RX Bias.** Defined by the cellular firmware driver.
VOICE#/TXPAD# (PE1)	25	O	It/Ot2	**Cellular TX Bias.** Defined by the cellular firmware driver.

Table 3-2. CX06827 ACF Pin Signal Definitions for Parallel Interface (PARIF = High)

Label	Pin	I/O	I/O Type	Signal Name/Description
Telephone Interface (LINE/CELL = High and LINE/GSM = High)				
VOICE#/TXPAD# (PE1)		O	It/Ot2	**Voice Relay Control.** When the LINE/CELL input is high, this output (typically active low) used to control the normally open voice relay. See cellular interface signals for TXPAD# usage.
HS_LCS (PE4)		I	It/Ot2	**Handset Line Current Sense.** LCS is an active high input that indicates a handset off-hook status. Not required for data/fax/voice/speakerphone operation. If not used, connect to GND through 47 KΩ.
GSM Cellular Phone Interface (LINE/CELL = High and LINE/GSM = Low)				
CELCLK/GSMINP0 (PA4)	37	I	Itpu/Ot2	**GSM Input Control.** Defined by the GSM firmware driver.
GSMRXD (PA2)	35	I	It/Ot2	**GSM Serial Receive Data.** Defined by the GSM firmware driver.
GSMTXD (PA6)	39	O	It/Ot2	**GSM Serial Transmit Data.** Defined by the GSM firmware driver.
OH#/RXPAD# (PE0)	24	O	It/Ot8	**GSM RX Bias.** Defined by the GSM firmware driver.
VOICE#/TXPAD# (PE1)		O	It/Ot2	**GSM TX Bias.** Defined by the GSM firmware driver.
ACF Interconnect and Optional CX20437 VC Interface				
SLEEP_IN	14	I	Itpd	**Modem Codec Sleep In.** Connect to ACF: IASLEEP pin.
MCLKIN	3	I	Ipd	**Modem Codec Serial Clock In**. Connect to ACF: MCLKOUT pin through 33 Ω.
CNTLSIN	2	I	Itpd	**Modem Codec Serial Control In.** Connect to ACF: SR1IO pin.
RXOUT	6	O	Ot2	**Modem Codec Serial Receive Data Out.** Connect to ACF: SR4IN pin.
TXSIN	4	I	Itpd	**Modem Codec Serial Transmit Data In.** Connect to ACF: SR4OUT pin.
STROBE	7	O	Ot2	**Modem Codec Serial Frame Sync Out.** Connect to ACF: SA1CLK pin through 33 Ω.
SCLK	5	O	Ot2	**Modem Codec Serial Clock Out.** Connect to ACF: IA1CLK pin through 33 Ω.
IA1CLK (P_PX03)	51	I	Itpu/Ot2	**DSP Modem Serial Clock In**. Connect to ACF: SCLK pin through 33 Ω.
SA1CLK (P_PX02)	50	I	Itpu/Ot2	**DSP Modem Serial Frame Sync In.** Connect to ACF: STROBE pin through 33 Ω.
SR4OUT (P_PX00)	49	O	Itk/Ot2	**DSP Modem Serial Transmit Data Out.** Connect to ACF: TXSIN pin.
SR4IN	52	I	Itk/Ot2	**DSP Modem Serial Receive Data In**. Connect to ACF: RXOUT pin.
IASLEEP (P_PF05)	56	O	Ot2	**DSP Sleep Out.** Connect to ACF: SLEEP_IN pin and to VC SLEEP pin.
M_CLKOUT (P_PB00)	44	O	It/Ot2	**DSP Master Serial Clock Out**. Connect through 33 Ω to ACF: MCLKIN pin and to VC M_CLKIN pin.
SR2CLK (P_PGP05)	96	I	Itpu/Ot2	**DSP Voice Serial Clock In.** Connect to VC M_SCK pin. Leave open if VC is not installed.
SA2CLK (P_PX05)	45	I	Itpu/Ot2	**DSP Voice Serial Frame Sync In.** Connect to VC M_STROBE pin. Leave open if VC is not installed.
SR3OUT	42	O	Ot2	**DSP Voice Serial Transmit Data Out.** Connect to VC M_TXSIN pin. Leave open if VC is not installed.
SR3IN (P_PX01)	43	I	Itk/Ot2	**DSP Voice Serial Receive Data In.** Connect to VC M_RXOUT pin. Leave open if VC is not installed.
SR2IO (P_PX06)	47	O	It/Ot2	**DSP Voice Serial Control Out.** Connect to VC M_CNTRLSIN pin. Leave open if VC is not installed.

Table 3-2. CX06827 ACF Pin Signal Definitions for Parallel Interface (PARIF = High)

Label	Pin	I/O	I/O Type	Signal Name/Description
Not Used – Connect to +3.3V through Resistor				
LPO	63	I	I/O	**Low Power Oscillator.** Not used. Connect to +3.3V through 240 KΩ.
PC3	127	I	Ith/Ot2	**Port PC3.** Not used. Connect to +3.3V through 47K Ω.
PC7	133	I	Ith/Ot2	**Port PC7.** Not used. Connect to +3.3V through 47K Ω.
PD3	20	I	Ith/Ot2	**Port PD7.** Not used. Connect to +3.3V through 47K Ω.
Parallel Host Interface				
HCS# (PD4)	21	I	It	**Host Bus Chip Select.** HCS# input low enables the MCU host bus interface.
HRD# (PD6)	23	I	Ithpu	**Host Bus Read.** HRD# is an active low, read control input. When HCS# is low, HRD# low allows the host to read status information or data from a selected MCU register.
HWT# (PD5)	22	I	Ithpu	**Host Bus Write.** HWT# is an active low, write control input. When HCS# is low, HWT# low allows the host to write data or control words into a selected MCU register.
HINT (PB7)	112	O	It/Ot8	**Host Bus Interrupt.** HINT output is set high when the receiver error flag, received data available, transmitter holding register empty, or modem status interrupt is asserted. HINT is reset low upon the appropriate interrupt service or master reset operation.
HA0-HA2 (PD0-PD2)	17-19	I	Ithpd/Ot2	**Host Bus Address Lines 0-2.** During a host read or write operation with HCS# low, HA0-HA2 select an internal MCU 16550A-compatible register.
HD0-HD7 (PC0-PC7)	123-124, 126-128, 130-133	I/O	Ith/Ot8	**Host Bus Data Lines 0-7**. HD0-HD7 are three-state input/output lines providing bidirectional communication between the host and the MCU. Data, control words, and status information are transferred over HD0-HD7.
Not Used				
BD2CLK	65	O	Itpu/Ot2	**Not Used.** Leave open.
DV1TP	114	I	Itpu	**Not Used.** Leave open.
PHS2	122	O	Ot2	**Not Used.** Leave open.
TESTP	113	I	Itpu	**Not Used.** Leave open.
XXCLK	55	O	It/Ot2	**Not Used.** Leave open.
P_GP01	58	I	It	**Port P_GP01**. Leave open.
P_PA00	61	I/O	Itpu/Ot2	**Port P_PA00.** Leave open.
P_PA03	60	O	Ot2	**Port P_PA03**. Leave open.
P_PA07	57	O	Ot2	**Port P_PA07**. Leave open.
PA1	34	I/O	It/Ot2	**Port PA1.** Leave open.
PB1	104	I/O	It/Ot2	**Port PB1.** Leave open.
PB6	110	I/O	It/Ot2	**Port PB6.** Leave open.
PD7	53	I/O	It/Ot2	**Port PD7.** Leave open.
PE6	31	I/O	It/Ot2	**Port PE6.** Leave open.
RESERVED	97-101			**Reserved.** Connected to internal circuitry. Leave open.

Notes:

1. I/O Types: See Table 3-5.
2. Interface Legend:
   - EB Expansion Bus
   - HB Host Bus
   - NC No internal pin connection
   - VC Voice Codec

   RESERVED = No external connection allowed (may have internal connection).

Figure 3-3. CX06827 ACF Hardware Signals for Serial Interface (PARIF = Low)

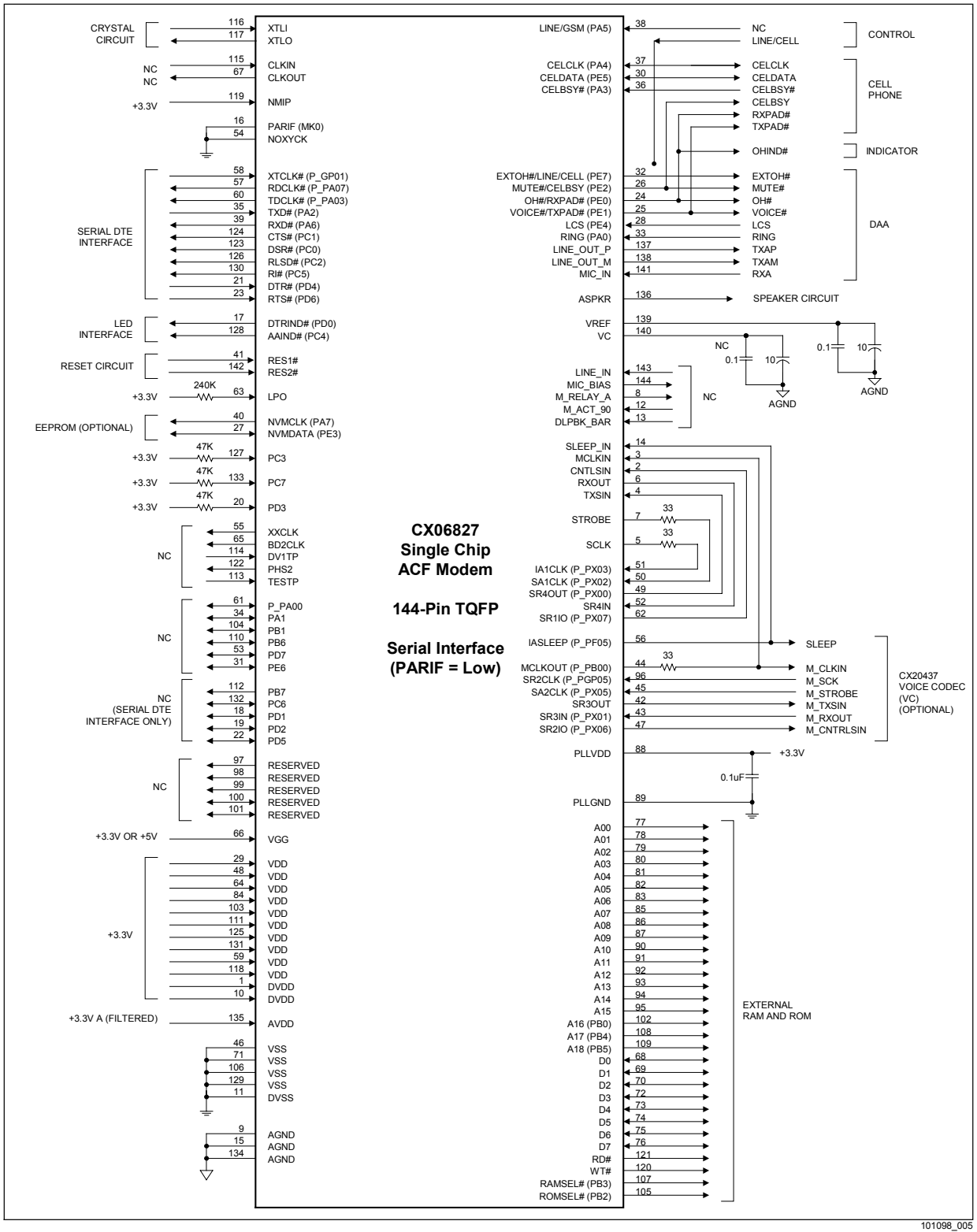
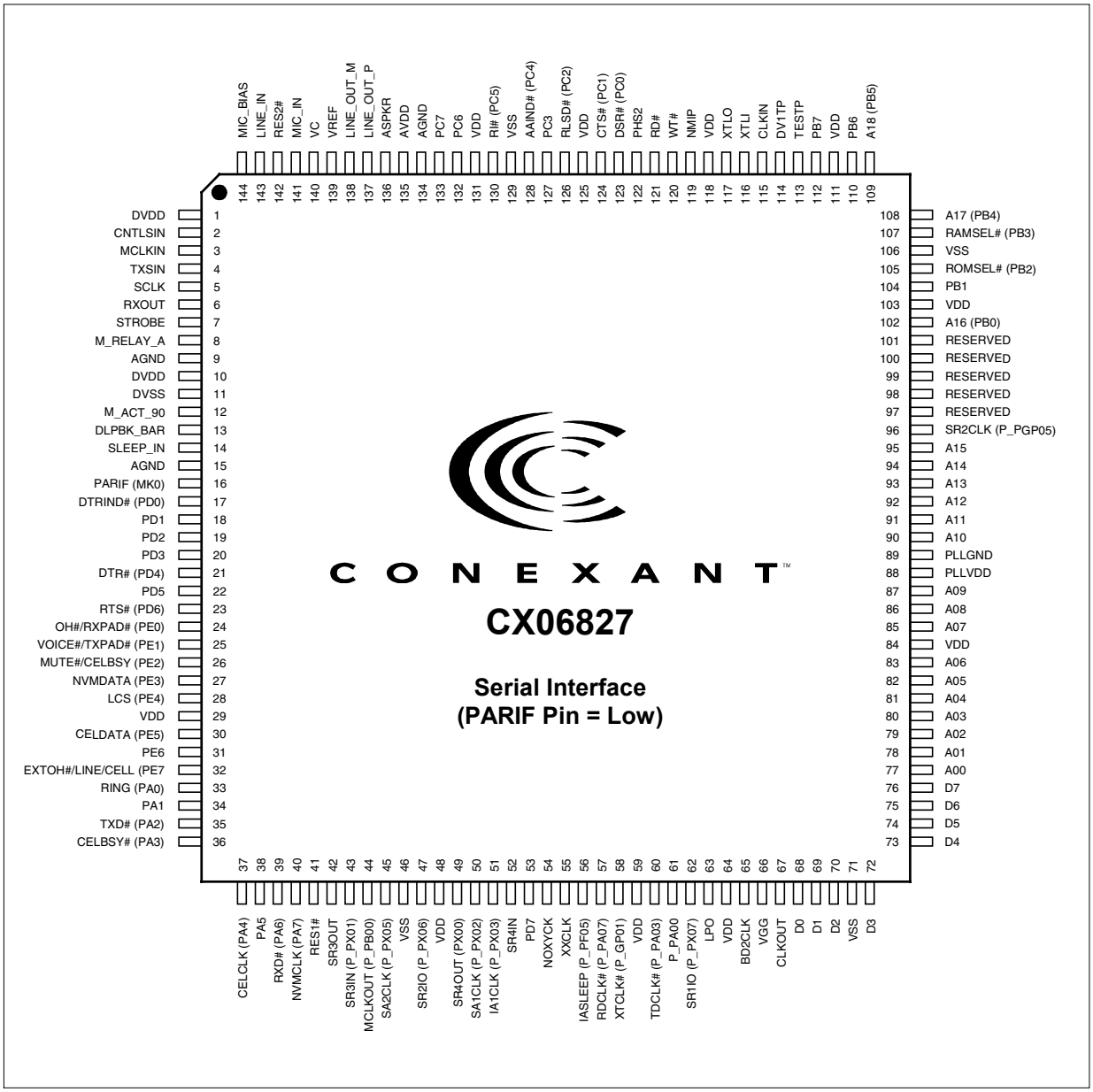


Figure 3-4. CX06827 ACF 144-Pin TQFP Pin Signals for Serial Interface (PARIF = Low)



101098_006

Table 3-3. CX06827 ACF 144-Pin TQFP Pin Signals for Serial Interface (PARIF = Low)

Pin	Signal Label	I/O	Interface	Pin	Signal Label	I/O	Interface
1	DVDD	P	+3.3V	73	D4	I/O	EB: D4
2	CNTLSIN	I	ACF: SR1IO	74	D5	I/O	EB: D5
3	MCLKIN	I	ACF: MCLKOUT through 33 ohms	75	D6	I/O	EB: D6
4	TXSIN	I	ACF: SR4OUT	76	D7	I/O	EB: D7
5	SCLK	O	ACF: IA1CLK through 33 ohms	77	A00	O	EB: A00
6	RXOUT	O	ACF: SR4IN	78	A01	O	EB: A01
7	STROBE	O	ACF:SA1CLK through 33 ohms	79	A02	O	EB: A02
8	M_RELAY_A	O	NC	80	A03	O	EB: A03
9	AGND	G	AGND	81	A04	O	EB: A04
10	DVDD	P	+3.3V	82	A05	O	EB: A05
11	DVSS	G	GND	83	A06	O	EB: A06
12	M_ACT_90	I	NC	84	VDD	P	+3.3V
13	DLPBK_BAR	I	NC	85	A07	O	EB: A07
14	SLEEP_IN	I	ACF: IASLEEP	86	A08	O	EB: A08
15	AGND	G	AGND	87	A09	O	EB: A09
16	PARIF (MK0)	I	GND (Serial DTE)	88	PLLVDD	P	+3.3V and to GND through 1 μF
17	DTRIND# (PD0)	O	LED: DTRIND#	89	PLLGND	G	GND
18	PD1	I/O	NC	90	A10	O	EB: A10
19	PD2	I/O	NC	91	A11	O	EB: A11
20	PD3	I	+3.3V through 47 KΩ	92	A12	O	EB: A12
21	DTR# (PD4)	I	DTE: DTR#	93	A13	O	EB: A13
22	PD5	I/O	NC	94	A14	O	EB: A14
23	RTS# (PD6)	I	DTE: RTS#	95	A15	O	EB: A15
24	OH#/ RXPAD# (PE0)	O	DAA: Off-Hook Relay Circuit; CELL: RXPAD#	96	SR2CLK (P_PGP05)	I	VC: M_SCK
25	VOICE# (PE1)	O	DAA: Voice Relay Circuit (Optional)	97	RESERVED	I/O	NC
26	MUTE#/ CELBSY (PE2)	O	DAA: Mute Circuit (Optional); CELL: CELBSY	98	RESERVED	I/O	NC
27	NVMDATA (PE3)	I/O	NVRAM: SDA	99	RESERVED	O	NC
28	LCS (PE4)	I	DAA: Line Current Sense Circuit	100	RESERVED	O	NC
29	VDD	P	+3.3V	101	RESERVED	O	NC
30	CELDATA (PE5)	I	CELL: CEL_DATA	102	A16 (PB0)	O	EB: A16
31	PE6	I/O	NC	103	VDD	P	+3.3V
32	EXTOH# (PE7)	I	DAA: Extension Pickup Circuit (Optional)	104	PB1	I/O	NC
33	RING (PA0)	I	DAA: Ring Detect Circuit	105	ROMSEL# (PB2)	O	EB: ROM CE#
34	PA1	I/O	NC	106	GND	G	GND
35	TXD# (PA2)	I	DTE: TXD#	107	RAMSEL# (PB3)	O	EB: RAM CS#
36	PA3	I/O	NC	108	A17 (PB4)	O	EB: A17
37	CELCLK (PA4)	I/O	CELL: CELCLK	109	A18 (PB5)	O	EB: A18
38	PA5	I/O	NC	110	PB6	I/O	NC
39	RXD# (PA6)	O	DTE: RXD#	111	VDD	P	+3.3V
40	NVMCLK (PA7)	O	NVRAM: SCL	112	PB7	O	NC
41	RES1#	I	Reset Circuit	113	TESTP	I	NC
42	SR3OUT	O	VC: M_TXSIN	114	DV1TP	I	NC
43	SR3IN (P_PX01)	I	VC: M_RXOUT	115	CLKIN	I	NC
44	MCLKOUT (P_PB00)	O	Through 33 ohms to ACF:MCLKIN and VC: M_CLKIN	116	XTLI	I	Crystal Circuit
45	SA2CLK (P_PX05)	I	VC: M_STROBE	117	XTLO	O	Crystal Circuit
46	GND	G	GND	118	VDD	P	+3.3V
47	SR2IO (P_PX06)	O	VC: M_CNTRLSIN	119	NMIP	I	+3.3V
48	VDD	P	+3.3V	120	WT#	O	EB: WRITE#

Table 3-3. CX06827 ACF 144-Pin TQFP Pin Signals for Serial Interface (PARIF = Low) (Continued)

Pin	Signal Label	I/O	Interface	Pin	Signal Label	I/O	Interface
49	SR4OUT (P_PX00)	O	ACF: TXSIN	121	RD#	O	EB: READ#
50	SA1CLK (P_PX02)	I	ACF: STROBE through 33 ohms	122	PHS2	O	NC
51	IA1CLK (P_PX03)	I	ACF: SCLK through 33 ohms	123	DSR# (PC0)	O	DTE: DSR#
52	SR4IN	I	ACF: RXOUT	124	CTS# (PC1)	O	DTE: CTS#
53	PD7	I/O	NC	125	VDD	P	+3.3V
54	NOXYCK	I	GND	126	RLSD# (PC2)	O	DTE: RLSD#
55	XXCLK	O	NC	127	PC3	I/O	+3.3V through 47 K
56	IASLEEP (P_PF05)	O	VC: SLEEP	128	AAIND# (PC4)	O	LED: AAIND#
57	RDCLK# (P_PA07)	O	DTE: RDCLK#	129	GND	G	GND
58	XTCLK# (P_GP01)	I	DTE: XTCLK#	130	RI# (PC5)	O	DTE: RI#
59	VDD	P	+3.3V	131	VDD	P	+3.3V
60	TDCLK# (P_PA03)	O	DTE: TDCLK#	132	PC6	I/O	NC
61	P_PA00	I/O	NC	133	PC7	I/O	+3.3V through 47 K
62	SR1IO (P_PX07)	O	ACF: CNTLSIN	134	AGND	G	AGND
63	LPO	I	+3.3V through 240K	135	AVDD	P	+3.3VA (Filtered)
64	VDD	P	+3.3V	136	ASPKR	O	AI: Speaker Circuit
65	BD2CLK	O	NC	137	LINE_OUT_P	O	DAA: TXAP
66	VGG	R	+5V or +3.3V	138	LINE_OUT_M	O	DAA: TXAM
67	CLKOUT	O	NC	139	VREF	R	AGND through C circuit
68	D0	I/O	EB: D0	140	VC	R	AGND through C circuit
69	D1	I/O	EB: D1	141	MIC_IN	I	DAA: RXA
70	D2	I/O	EB: D2	142	RES2#	I	
71	GND	G	GND	143	LINE_IN	I	NC
72	D3	I/O	EB: D3	144	MIC_BIAS	O	NC

Table 3-4. CX06827 ACF Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
System				
XTLI, XTLO	116, 117	I, O	Ix, Ox	**Crystal In and Crystal Out.** If an external 28.224 MHz crystal circuit is used instead of an external clock circuit, connect XTLI and XTLO to the external crystal circuit and leave CLKIN open.
CLKIN	115	I	It	**Clock In.** If an external 28.224 MHz clock circuit is used instead of an external crystal circuit, connect CLKIN to the clock output and leave XTLI and XTLO open.
CLKOUT	67	O	It/Ot2	**Clock Out.** 28.224 MHz output clock. Leave open.
NOXYCK	54	I	Itpu	**Disable XCLK Output.** Low disables XCLK output (reduces internal power consumption). High enables XCLK output.
PARIF	16	I	Itpu	**Parallel/Serial Interface Select.** PARIF input high (open) selects parallel host interface operation. PARIF low (GND) selects serial DTE interface operation.
NMI#	119	I	Ithpu	**Non-Maskable Interrupt.** Not used. Connect to +3.3V.
RES1# RES2#	41 142	I	It	**Reset.** The active low RES1# and RES2# input resets the ACF logic, and restores the saved configuration from serial EEPROM or returns the modem to the factory default values if NVRAM is not present. RESET# low holds the modem in the reset state; RESET# going high releases the modem from the reset state. After application of VDD, RESET# must be held low for at least 15 ms after the VDD power reaches operating range. The modem device set is ready to use 25 ms after the low-to-high transition of RESET#. For parallel Interface, connect RESET# input to the host bus RESET line through an inverter. For serial Interface, connect RESET# input to a reset switch circuit.
Power and Ground				
VGG	66	P	PWRG	**I/O Signaling Voltage Source.** Connect to +5V or +3.3V.
VDD	29, 48, 59, 64, 66, 84, 103, 111, 118, 125, 131	P	PWR	**Digital Supply Voltage for Digital Circuits.** Connect to +3.3V.
DVDD	1, 10	P	PWR	**Digital Supply Voltage for Analog Circuits.** Connect to +3.3V
AVDD	135	P	PWR	**Analog Supply Voltage for Analog Circuits.** Connect to analog power.
VSS	46, 71, 106, 129	G	GND	**Digital Ground for Digital Circuits.** Connect to digital ground.
DVSS	11	G	GND	**Digital Ground for Analog Circuits.** Connect to digital ground.
AGND	9, 15, 134	G	AGND	**Analog Ground for Analog Circuits.** Connect to analog ground.
PLLVDD	88	P	PWR	**Supply Voltage for PLL Circuit.** Connect to +3.3V and to analog ground through 0.1 μF.
PLLGND	89	G	GND	**Digital Ground for PLL Circuit.** Connect to digital ground.
Serial EEPROM (NVRAM) Interface				
NVMCLK (PA7)	40	O	It/Ot2	**NVRAM Clock.** NVMCLK output high enables the EEPROM. Connect to the EEPROM SCL pin.
NVMDATA (PE3)	27	I/O	It/Ot2	**NVRAM Data.** NVMDATA supplies serial data to and from the EEPROM. Connect to the EEPROM SDA pin and to +3.3V through 10 KΩ.

Table 3-4. CX06827 ACF Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
External Bus Interface				
A00-A06, A07-A09, A10-A15, A16 (PB0), A17 (PB4), A18 (PB5)	77-83, 85-87, 90-95, 102, 108, 109	O, O, O, O, O, O	It/Ot8, It/Ot8, It/Ot2, It/Ot2, It/Ot2, It/Ot2	**Address Lines 0-18.** A0-A18 are the address output lines used to access external memory; up to 4 Mbits (512k bytes) flash ROM using A0-A18 and up to 1 Mbit (128k bytes) RAM using A0-A16.
D0-D2, D3-D7	68-70, 72-76	I/O	Ith/Ot2	**Data Line 0-7.** D0-D7 are bidirectional external memory bus data lines.
READ#	121	O	It/Ot2	**Read Enable.** READ# output low enables data transfer from the selected device to the D0-D7 lines.
WRITE#	120	O	It/Ot2	**Write Enable.** WRITE# output low enables data transfer from the D0-D7 lines to the selected device.
RAMSEL# PB3)	107	O	It/Ot2	**RAM Select.** RAMSEL# output low selects the external RAM.
ROMSEL# (PB2)	105	O	Ot2	**ROM Select**. ROMSEL# output low selects the external flash ROM.
Telephone Line/Telephone/Audio Interface Signals and Reference Voltage				
OH#/RXPAD# (PE0)	24	O	It/Ot2	**Off-Hook Relay Control.** The active low output can be used to control the normally open off-hook relay.
VOICE#/TXPAD# (PE1)	25	O	It/Ot2	**Voice Relay Control.** The active low VOICE# output can optionally be used to switch the handset from the telephone line to the voice codec interface to be used as a microphone and speaker. Leave open if not used.
MUTE# (PE2)	26	O	It/Ot2	**Mute Relay Control.** The active low MUTE# output can optionally be used to used to control the normally open mute relay. Leave open if not used.
LCS (PE4)	28	I	It/Ot2	**Loop Current Sense.** LCS is an active high input that indicates a handset off-hook status.
EXTOH#/LINE/CELL (PE7)	32	I	It/Ot2	**Extension Off-Hook.** Active low input optionally used to indicate when the telephone handset connected to the modem goes off-hook state. Connect to +3.3V through 47K Ω if not used.
RING (PA0)	33	I	It/Ot2	**Ring Frequency.** A rising edge on the RING input initiates an internal ring frequency measurement. The RING input from an external ring detect circuit is monitored to determine when to wake up from sleep or stop mode. The RING input is typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be low.
LINE_OUT_P, LINE_OUT_M	137, 138	O, O	O(DF)	**Transmit Analog 1 and 2.** The LINE_OUT_P and LINE_OUT_M outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 Ω load. Connect LINE_OUT_P and LINE_OUT_M to the DAA telephone line interface transmit circuit.
MIC_IN	141	I	I(DA)	**Receive Analog.** MIC_IN is a single-ended input from the telephone line interface or an optional external hybrid circuit with 70K Ω input impedance. Connect MIC_IN to the DAA telephone line interface receive circuit.
VREF	139	R	REF	**High Voltage Reference.** Connect to AGND through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VREF pin. Use a short path and a wide trace to AGND pin.
VC	140	R	REF	**Low Voltage Reference.** Connect to AGND through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VC pin. Use a short path and a wide trace to AGND pin.

Table 3-4. CX06827 ACF Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
Telephone Line/Telephone/Audio Interface Signals and Reference Voltage (Continued)				
ASPKR	136	O	O(DF)	**Speaker Analog Output.** The ASPKR analog output can originate from one of five different sources: RIN, TELIN, MICM or MICV or from the MDP's internal voice playback mode. The ASPKR on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the ASPKR output is clamped to the voltage at the VC pin. The ASPKR output can drive an impedance as low as 300 ohms. In a typical application, the ASPKR output is an input to an external LM386 audio power amplifier.
LINE_IN	143	I	I(DA)	**Not Used.** Leave open.
MIC_BIAS	144	O	Oa	**Not Used.** Leave open.
M_RELAYA	8	O	Ot	**Not Used.** Leave open.
M_ACT90	12	I	Itpu	**Not Used.** Leave open.
DLPBK_BAR	13	I	It	**Not Used.** Leave open.
ACF Interconnect and Optional CX20437 VC Interface				
SLEEP_IN	14	I	Itpd	**Modem Codec Sleep In.** Connect to ACF: IASLEEP pin.
MCLKIN	3	I	Ipd	**Modem Codec Serial Clock In**. Connect to ACF: MCLKOUT pin through 33 Ω.
CNTLSIN	2	I	Itpd	**Modem Codec Serial Control In.** Connect to ACF: SR1IO pin.
RXOUT	6	O	Ot2	**Modem Codec Serial Receive Data Out.** Connect to ACF: SR4IN pin.
TXSIN	4	I	Itpd	**Modem Codec Serial Transmit Data In.** Connect to ACF: SR4OUT pin.
STROBE	7	O	Ot2	**Modem Codec Serial Frame Sync Out.** Connect to ACF: SA1CLK pin through 33 Ω.
SCLK	5	O	Ot2	**Modem Codec Serial Clock Out.** Connect to ACF: IA1CLK pin through 33 Ω.
IA1CLK (P_PX03)	51	I	Itpu/Ot2	**DSP Modem Serial Clock In**. Connect to ACF: SCLK pin through 33 Ω.
SA1CLK (P_PX02)	50	I	Itpu/Ot2	**DSP Modem Serial Frame Sync In.** Connect to ACF: STROBE pin through 33 Ω.
SR4OUT (P_PX00)	49	O	Itk/Ot2	**DSP Modem Serial Transmit Data Out.** Connect to ACF: TXSIN pin.
SR4IN	52	I	Itk/Ot2	**DSP Modem Serial Receive Data In**. Connect to ACF: RXOUT pin.
IASLEEP (P_PF05)	56	O	Ot2	**DSP Sleep Out.** Connect to ACF: SLEEP_IN pin and to VC SLEEP pin.
M_CLKOUT (P_PB00)	44	O	It/Ot2	**DSP Master Serial Clock Out**. Connect through 33 Ω to ACF: MCLKIN pin and to VC M_CLKIN pin.
SR2CLK (P_PGP05)	96	I	Itpu/Ot2	**DSP Voice Serial Clock In.** Connect to VC M_SCK pin. Leave open if VC is not installed.
SA2CLK (P_PX05)	45	I	Itpu/Ot2	**DSP Voice Serial Frame Sync In.** Connect to VC M_STROBE pin. Leave open if VC is not installed.
SR3OUT	42	O	Ot2	**DSP Voice Serial Transmit Data Out.** Connect to VC M_TXSIN pin. Leave open if VC is not installed.
SR3IN (P_PX01)	43	I	Itk/Ot2	**DSP Voice Serial Receive Data In.** Connect to VC M_RXOUT pin. Leave open if VC is not installed.
SR2IO (P_PX06)	47	O	It/Ot2	**DSP Voice Serial Control Out.** Connect to VC M_CNTRLSIN pin. Leave open if VC is not installed.

Table 3-4. CX06827 ACF Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
Not Used – Connect to +3.3V through Resistor				
LPO	63	I	I/O	**Low Power Oscillator.** Not used. Connect to +3.3V through 240 KΩ.
PC3	127	I	Ith/Ot2	**Port PC3.** Not used. Connect to +3.3V through 47K Ω.
PC7	133	I	Ith/Ot2	**Port PC7.** Not used. Connect to +3.3V through 47K Ω.
PD3	20	I	Ith/Ot2	**Port PD7.** Not used. Connect to +3.3V through 47K Ω.
PE5	30	I	Ith/Ot2	**Port PE5.** Not used. Connect to +3.3V through 47K Ω.
V.24 (EIA/TIA-232-E) DTE Serial Interface				
XTCLK# (P_GP01)	58	I	It/Ot2	**External Data Clock.** Synchronous External Transmit Data Clock input in synchronous modes. Leave open if not used.
RDCLK# (P_PA07)	57	O	Itpu/Ot2	**Receive Data Clock.** Synchronous Receive Data Clock output in synchronous modes. The RDCLK frequency is the data rate (±0.01%) with a duty cycle of 50±1%. Leave open if not used.
TDCLK# (P_PA03)	60	O	Itpu/Ot2	**Transmit Data Clock.** Synchronous Transmit Data Clock output in synchronous modes. The TDCLK# frequency is the data rate (±0.01%) with a duty cycle of 50±1%. Leave open if not used.
TXD# (PA2)	35	I	It/Ot2	**Transmitted Data (EIA BA/ITU-T CT103).** The DTE uses the TXD# line to send data to the modem for transmission over the telephone line or to transmit commands to the modem.
RXD# (PA6)	39	O	It/Ot2	**Received Data (EIA BB/ITU-T CT104).** The modem uses the RXD# line to send data received from the telephone line to the DTE and to send modem responses to the DTE. During command mode, RXD# data represents the modem responses to the DTE.
CTS# (PC1)	124	O	Ith/Ot8	**Clear To Send (EIA CB/ITU-T CT106).** CTS# output ON (low) indicates that the modem is ready to accept data from the DTE. In asynchronous operation, in error correction or normal mode, CTS# is always ON (low) unless RTS/CTS flow control is selected by the &Kn command. In synchronous operation, the modem also holds CTS# ON during asynchronous command state. The modem turns CTS# OFF immediately upon going off-hook and holds CTS# OFF until both DSR# and RLSD# are ON and the modem is ready to transmit and receive synchronous data. The modem can also be commanded by the &Rn command to turn CTS# ON in response to an RTS# OFF-to-ON transition.
DSR# (PC0)	123	O	Ith/Ot8	**Data Set Ready (EIA CC/ITU-T CT107).** DSR# indicates modem status to the DTE. DSR# OFF (high) indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator (RI#). DSR# output is controlled by the AT&Sn command.
RLSD# (PC2)	126	O	Ith/Ot8	**Received Line Signal Detector (EIA CF/ITU-T CT109).** When AT&C0 command is not in effect, RLSD# output is ON when a carrier is detected on the telephone line or OFF when carrier is not detected.
RI# (PC5)	130	O	Ith/Ot8	**Ring Indicator (EIA CE/ITU-T CT125).** RI# output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line.
DTR# (PD4)	21	I	It	**Data Terminal Ready (EIA CD/ITU-T CT108).** The DTR# input is turned ON (low) by the DTE when the DTE is ready to transmit or receive data. DTR# ON prepares the modem to be connected to the telephone line, and maintains the connection established by the DTE (manual answering) or internally (automatic answering). DTR# OFF places the modem in the disconnect state under control of the &Dn and &Qn commands.

Table 3-4. CX06827 ACF Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
V.24 (EIA/TIA-232-E) DTE Serial Interface (Continued)				
RTS# (PD6)	23	I	Ithpu	**Request To Send (EIA CA/ITU-T CT105).** RTS# input ON (low) indicates that the DTE is ready to send data to the modem. In the command state, the modem ignores RTS#. In asynchronous operation, the modem ignores RTS# unless RTS/CTS flow control is selected by the &Kn command. In synchronous on-line operation, the modem can be commanded by the &Rn command to ignore RTS# or to respond to RTS# by turning on CTS# after the delay specified by Register S26.
LED Indicator Interface				
AAIND# (PC4)	128	O	Ith/Ot8	**Auto Answer Indicator.** AAIND# output ON (low) corresponds to the indicator on. AAIND# output is active when the modem is configured to answer the ring automatically (ATS0 command ≠ 0).
DTRIND# (PD0)	17	O	Ithpd/Ot2	**DTR Indicator.** DTRIND# output ON (low) corresponds to the indicator on. The DTRIND# state reflects the DTR# output state except when the &D0 command is active, in which case DTRIND# is low.
Telephone Line/Analog Cellular Phone Interface Select				
LINE/GSM (PA5)		I	It/Ot2	**Line/GSM Interface Select.** Not used. Leave open.
LINE/CELL (PE7)		I	It/Ot8	**Line/Cellar Interface Select.** Selects telephone line or cellular phone (AMPS) interface, as follows: **LINE/CELL** — **Interface Selected** H — Telephone Line L — Cellular (AMPS) The following ports operate as indicated for the selected interface: **Port*** — **Telephone Line** — **Analog Cellular** PE0 — OHIND# — RXPAD# PE1 — — — TXPAD# PE2 — — — CELBSY PE5 — — — CELDATA PA2 — — — — PA3 — — — CELBSY# PA4 — — — CELCLK PA6 — — — GSMTXD * Ports marked "—" are not used.
Analog Cellular Phone Interface (LINE/CELL = Low)				
CELCLK/GSMINP0 (PA4)		I	Itpu/Ot2	**Cellular Clock.** Defined by the cellular firmware driver.
CELDATA (PE5)		I/O	It/Ot2	**Cellular Data**. Defined by the cellular firmware driver.
CELBSY (PE2)		O	It/Ot2	**Cellular Busy.** Defined by the cellular firmware driver.
CELBSY# (PA3)		I	Itpu/Ot2	**Cellular Not Busy.** Defined by the cellular firmware driver.
OH#/RXPAD# (PE0)	24	O	It/Ot8	**Cellular RX Bias.** In Line Mode (LINE/CELL = high), OHIND#/RXPAD# (PE0) indicates the status of the off-hook relay. In Cell Mode (LINE/CELL = low), this signal is defined by the cellular firmware driver.
VOICE#/TXPAD# (PE1)	25	O	It/Ot2	**Cellular TX Bias.** Defined by the cellular firmware driver.
Telephone Interface (LINE/CELL = High and LINE/GSM = High)				
VOICE#/TXPAD# (PE1)		O	It/Ot2	**Voice Relay Control.** When the LINE/CELL input is high, this output (typically active low) used to control the normally open voice relay. See cellular interface signals for TXPAD# usage.
HS_LCS (PE4)		I	It/Ot2	**Handset Line Current Sense.** LCS is an active high input that indicates a handset off-hook status. Not required for data/fax/voice/speakerphone operation. If not used, connect to GND through 47 KΩ.

Table 3-4. CX06827 ACF Pin Signal Definitions for Serial Interface (PARIF = Low)

Label	Pin	I/O	I/O Type	Signal Name/Description
Not Used				
BD2CLK	65	O	Itpu/Ot2	**Not Used.** Leave open.
DV1TP	114	I	Itpu	**Not Used.** Leave open.
PHS2	122	O	Ot2	**Not Used.** Leave open.
TESTP	113	I	Itpu	**Not Used.** Leave open.
XXCLK	55	O	It/Ot2	**Not Used.** Leave open.
P_PA00	61	I/O	Itpu/Ot2	**Port P_PA00.** Leave open.
PA1	34	I/O	It/Ot2	**Port PA1.** Leave open.
PA3	36	I/O	Itpu/Ot2	**Port PA3.** Leave open.
PA4	37	I/O	Itpu/Ot2	**Port PA4.** Leave open.
PA5	35	I/O	It/Ot2	**Port PA5.** Leave open.
PB1	104	I/O	It/Ot2	**Port PB1.** Leave open.
PB6	110	I/O	It/Ot2	**Port PB6.** Leave open.
PC6	132	I/O	Ith/Ot8	**Port PC6**. Leave open.
PD1	18	I/O	Ithpd/Ot2	**Port PD1**. Leave open.
PD2	19	I/O	Ithpd/Ot2	**Port PD2**. Leave open.
PD5	22	I/O	Ithpu	**Port PD5**. Leave open.
PD7	53	I/O	It/Ot2	**Port PD7.** Leave open.
PE2	26	I/O	It/Ot2	**Port PE2.** Leave open.
PE6	31	I/O	It/Ot2	**Port PE6.** Leave open.
RESERVED	97-101			**Reserved.** Connected to internal circuitry. Leave open.

Notes:

1. I/O Types: See Table 3-5.
2. Interface Legend:
   - EB Expansion Bus
   - HB Host Bus
   - NC No internal pin connection
   - VC Voice Codec

   RESERVED = No external connection allowed (may have internal connection).

Table 3-5. CX06827 ACF I/O Type Definitions

I/O Type	Description
Ix/Ox	I/O, wire
It/Ot2	Digital input, +5V tolerant/ Digital output, 2 mA, Z_{INT} = 120 Ω
Itk/Ot2	Digital input, +5V tolerant, keeper/ Digital output, 2 mA, Z_{INT} = 120 Ω
Itpu/Ot2	Digital input, +5V tolerant, 75k Ω pull up/ Digital output, 2 mA, Z_{INT} = 120 Ω
It/Ot8	Digital input, +5V tolerant,/ Digital output, 8 mA, Z_{INT} = 50 Ω
Ithpd/Ot2	Digital input, +5V tolerant, hysteresis, 75k Ω pull down/ Digital output, 2 mA, Z_{INT} = 120 Ω
Ith/Ot2	Digital input, +5V tolerant, hysteresis/Digital output, 2 mA, Z_{INT} = 120 Ω
Ith/Ot8	Digital input, +5V tolerant, hysteresis/Digital output, 8 mA, Z_{INT} = 50 Ω
It	Digital input, +5V tolerant
Itk	Digital input, +5V tolerant, keeper
Itkpu	Digital input, +5V tolerant, keeper, 75k Ω pull up
Itpu	Digital input, +5V tolerant, 75k Ω pull up
Ithpu	Digital input, +5V tolerant, hysteresis, 75k Ω pull up
Ot2	Digital output, three-state, 2 mA, Z_{INT} = 120 Ω
PWR	VCC Power
PWRG	VGG Power
GND	Ground

Notes:
1. See DC characteristics in Table 3-6.
2. I/O Type corresponds to the device Pad Type. The I/O column in signal interface tables refers to signal I/O direction used in the application.

Table 3-6. CX06827 ACF DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	VIL					
+5V tolerant		0	–	0.8	V	
+5V tolerant hysteresis		0	–	0.3 *VGG	V	
Input Voltage High	VIH		–		V	
+5V tolerant		2	–	5.25	V	
+5V tolerant hysteresis		0.7 * VDD	–	5.25	V	
Input Hysteresis	VH		–		V	
+3V hysteresis		0.5	–		V	
+5V tolerant, hysteresis		0.3	–		V	
Output Voltage Low	VOL					
Z_{INT} = 120 Ω		0	–	0.4	V	IOL = 2 mA
Z_{INT} = 50 Ω		0	–	0.4	V	IOL = 8 mA
Output Voltage High	VOH		–		V	
Z_{INT} = 120 Ω		2.4	–	VDD	V	IOL = -2 mA
Z_{INT} = 50 Ω		2.4	–	VDD	V	IOL = -8 mA
Pull-Up Resistance	Rpu	50	–	200	kΩ	
Pull-Down Resistance	Rpd	50	–	200	kΩ	
Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF.						

3.2 CX20437 VC Hardware Pins and Signals (S Model)

Microphone and analog speaker interface signals, as well as telephone handset/headset interface signals are provided to support functions such as speakerphone mode, telephone emulation, microphone voice record, speaker voice playback, and call progress monitor.

VC hardware interface signals are shown by major interface in Figure 3-5, are shown by pin number in Figure 3-6, and are listed by pin number in Table 3-7.

VC hardware interface signals are defined in Table 3-8.

VC pin signal DC electrical characteristics are defined in Table 3-9.

VC pin signal analog electrical characteristics are defined in Table 3-10.

Figure 3-5. CX20437 VC Hardware Interface Signals

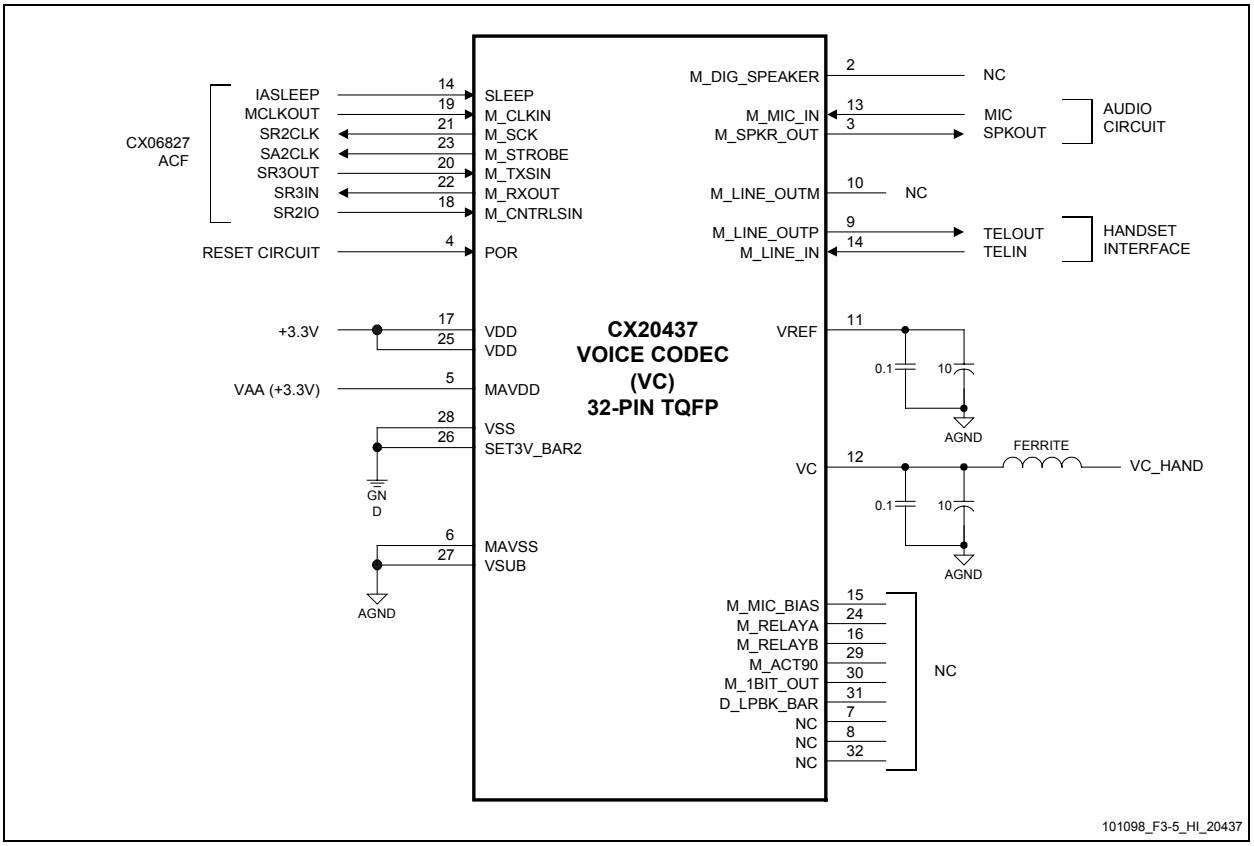


Figure 3-6. CX20437 VC 32-Pin TQFP Pin Signals

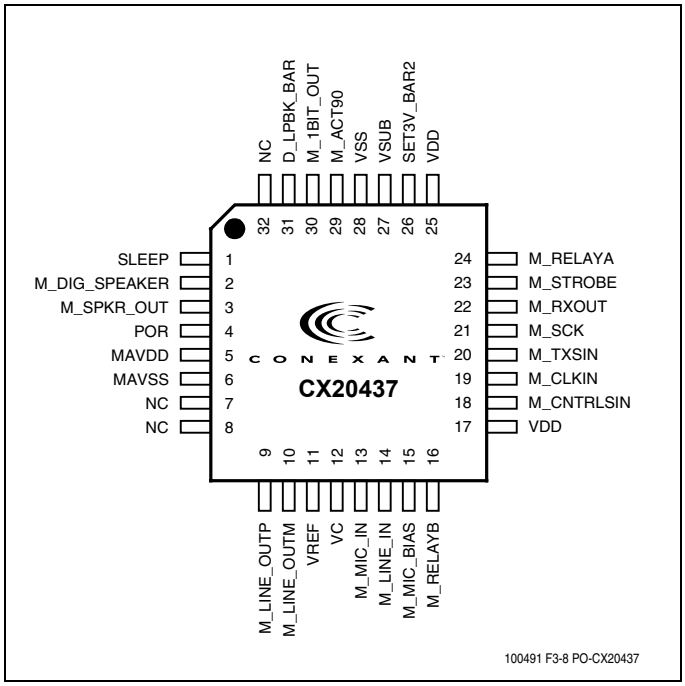


Table 3-7. CX20437 VC 32-Pin TQFP Pin Signals

Pin	Signal Label	I/O	Interface
1	SLEEP	I	ACF: IASLEEP
2	M_DIG_SPEAKER	O	NC
3	M_SPKR_OUT	O	Speaker interface circuit
4	POR	I	Host: RESET# or reset circuit
5	MAVDD		VAA (+3.3V)
6	MAVSS		AGND
7	NC		NC
8	NC		NC
9	M_LINE_OUTP	O	Handset interface circuit: TELOUT
10	M_LINE_OUTM	O	NC
11	VREF		AGND through capacitors
12	VC		AGND through capacitors For handset interface, connect also to VC_HAND through ferrite bead
13	M_MIC_IN	I	Microphone interface circuit
14	M_LINE_IN	I	Handset interface circuit: TELIN
15	M_MIC_BIAS		NC
16	M_RELAYB		NC
17	VDD		+3.3V
18	M_CNTRLSIN	I	ACF: V_CTRL
19	M_CLKIN	I	ACF: M_CLK
20	M_TXSIN	I	ACF: V_TXSIN
21	M_SCK	O	ACF: V_SCLK
22	M_RXOUT	O	ACF: V_RXOUT
23	M_STROBE	O	ACF: V_STROBE
24	M_RELAYA	O	NC
25	VDD		+3.3V
26	M_SET3V_BAR2	I	GND
27	VSUB		AGND
28	VSS		GND
29	M_ACT90	I	NC
30	M_1BIT_OUT	O	NC
31	D_LPBK_BAR	I	NC
32	NC		NC

Table 3-8. CX20437 VC Pin Signal Definitions

Label	Pin	I/O	I/O Type	Signal Name/Description
System Signals				
VDD	17, 25	P	PWR	**Digital Power Supply.** Connect to +3.3V and digital circuits power supply filter.
MAVDD	5	P	PWR	**Analog Power Supply.** Connect to +3.3V and analog circuits power supply filter.
VSS	28	G	GND	**Digital Ground.** Connect to GND.
MAVSS	6	G	AGND	**Analog Ground.** Connect to AGND.
VSUB	27	G	GND	**Analog Ground.** Connect to AGND.
POR	4	I	Itpu	**Power-On Reset.** Active low reset input. Connect to Host RESET# or reset circuit.
SET3V_BAR2	26	I	Itpu	**Set +3.3V Analog Reference.** Connect to GND.
ACF Interconnect				
SLEEP	1	I	Itpd	**IA Sleep.** Active high sleep input. Connect to ACF IASLEEP pin.
M_CLKIN	19	I	Itpd	**Master Clock Input**. Connect to ACF M_CLK pin.
M_SCK	21	O	Ot2	**Serial Clock Output.** Connect to ACF V_SCLK pin.
M_CNTRL_SIN	18	I	Itpd	**Control Input.** Connect to ACF V_CTRL pin.
M_STROBE	23	O	Ot2	**Serial Frame Sync.** Connect to ACF V_STROBE pin.
M_TXSIN	20	I	Itpd	**Serial Transmit Data.** Connect to ACF V_TXSIN pin.
M_RXOUT	22	O	Ot2	**Serial Receive Data.** Connect to ACF V_RXOUT pin.
Microphone/Speaker Interface				
M_MIC_IN	13	I	I(DA)	**Microphone Input.** Single-ended analog input from the microphone circuit.
M_SPKR_OUT	3	O	O(DF)	**Modem Speaker Analog Output.** The M_SPKR_OUT analog output reflects the received analog input signal. The M_SPKR_OUT on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the M_SPKR_OUT output is clamped to the voltage at the VC pin. The M_SPKR_OUT output can drive an impedance as low as 300 ohms. In a typical application, the M_SPKR_OUT output is an input to an external LM386 audio power amplifier.
Handset/Headset Interface				
M_LINE_OUTP	9	O	O(DF)	**Telephone Handset Out (TELOUT).** Single-ended analog data output to the telephone handset circuit. The output can drive a 300 Ω load.
M_LINE_IN	14	I	I(DA)	**Telephone Handset Out (TELIN).** Single-ended analog data input from the telephone handset circuit.
Reference Voltage				
VREF	11	R	REF	**High Voltage Reference.** Connect to AGND through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VREF pin. Use a short path and a wide trace to AGND pin.
VC	12	R	REF	**Low Voltage Reference.** Connect to AGND through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VC pin. Use a short path and a wide trace to AGND pin. For handset interface, also connect to handset interface circuit (VC_HAND) through a ferrite bead.

Table 3-7. CX20437 VC Pin Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Not Used				
M_DIG_SPEAKER	2	O	Ot2	**Not Used.** Leave open.
M_LINE_OUTM	10	O	Oa	**Not Used.** Leave open.
M_RELAYA	24	O	Ot	**Not Used.** Leave open.
M_RELAYB	16	O	Ot	**Not Used.** Leave open.
M_MIC_BIAS	15	O	Oa	**Not Used.** Leave open.
M_ACT90	29	I	Itpu	**Not Used.** Leave open.
M_1BIT_OUT	30	O	Ot2	**Not Used.** Leave open.
D_LPBK_BAR	31	I	It	**Not Used.** Leave open.
NC	7, 8, 32		NC	**Internal No Connect.** Leave open.

Notes:

1. I/O types*:

Ia	Analog input
It	Digital input, TTL-compatible
Itpd	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-down
Itpu	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-up
Oa	Analog output
Ot2	Digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
Ot2od	Digital output, TTL-compatible, 2 mA, open drain, $Z_{INTERNAL}$ = 120 Ω
AGND	Analog Ground
GND	Digital Ground

Table 3-9. CX20437 VC DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	V_{IN}	-0.30	–	VDD+0.3	V	
Input Voltage Low	V_{IL}	-0.30	–	VDD+0.3	V	
Input Voltage High	V_{IH}	0.4*VDD	–	–	V	
Output Voltage Low	V_{OL}	0	–	0.4	V	
Output Voltage High	V_{OH}	0.8*VDD	–	VDD	V	
Input Leakage Current	–	-10	–	10	µA	
Output Leakage Current (High Impedance)	–	-10	–	10	µA	
Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF						

Table 3-10. CX20437 VC Analog Electrical Characteristics

Signal Name	Type	Characteristic	Value
M_LINE_IN,	I (DA)	Input Impedance	> 70K Ω
M_MIC_IN		AC Input Voltage Range	1.1 VP-P
		Reference Voltage	+1.35 VDC
M_LINE_OUTP	O (DD)	Minimum Load	300 Ω
		Maximum Capacitive Load	0 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	1.4 VP-P (with reference to ground and a 600 Ω load)
		Reference Voltage	+1.35 VDC
		DC Offset Voltage	± 200 mV
M_SPKR_OUT	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	1.4 VP-P
		Reference Voltage	+1.35 VDC
		DC Offset Voltage	± 20 mV
Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; MAVDD = +3.3 ± 0.3 VDC, TA = 0°C to 70°C			

Parameter	Min	Typ	Max	Units
DAC to Line Driver output (600Ω load, 3dB in SCF and CTF) SNR/SDR at:				dB
4Vp-p differential		88/85		
2Vp-p differential		82/95		
-10dBm differential		72/100		
DAC to Speaker Driver output (150Ω load, 3dB in SCF and CTF, -6dB in speaker driver) SNR/SDR at:				dB
2Vp-p		88/75		
1Vp-p		82/80		
-10dBm		72/83		
Line Input to ADC (6dB in AAF) SNR/SDR at –10 dBm		80/95		dB
Input Leakage Current (analog inputs)	-10		10	µA
Output Leakage Current (analog outputs)	-10		10	µA

3.3 Electrical and Environmental Specifications

3.4 Operating Conditions, Absolute Maximum Ratings, and Power Requirements

The operating conditions are specified in Table 3-11.

The absolute maximum ratings are listed in Table 3-12.

The current and power requirements are listed in Table 3-13.

Table 3-11. Operating Conditions

Parameter	Symbol	Limits	Units
Supply Voltage	VDD	+3.0 to +3.6	VDC
Operating Ambient Temperature	T_A	0 to +70	°C

Table 3-12. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	VDD	-0.5 to +4.0	VDC
Input Voltage	V_{IN}	-0.5 to (VGG +0.5)*	VDC
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (VAA + 0.5)	VDC
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VGG +0.5)*	VDC
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	VDC
Latch-up Current (25°C)	I_{TRIG}	±400	mA
* VGG = +3.3V ± 0.3V or +5V ± 5%.			

Handling CMOS Devices

The device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage.

An unterminated input can acquire unpredictable voltages through coupling with stray capacitance and internal cross talk. Both power dissipation and device noise immunity degrades. Therefore, all inputs should be connected to an appropriate supply voltage.

Input signals should never exceed the voltage range from -0.5V to VGG + 0.5V. This prevents forward biasing the input protection diodes and possibly entering a latch up mode due to high current transients.

Table 3-13. Current and Power Requirements

Mode	Typical Current (Ityp) (mA)	Maximum Current (Imax) (mA)	Typical Power (Ptyp) (mW)	Maximum Power (Pmax) (mW)	Notes
CX06827 SCFACF					
Normal Mode: Off-hook, normal data connection	83	91	274	328	f = 28.224 MHz
Normal Mode: On-hook, idle, waiting for ring	83	91	274	328	f = 28.224 MHz
Sleep Mode	8.4	9.2	27.7	33.1	f = 0 MHz
CX20437 VC (Optional)					
Normal Mode	1.5	2	5	7	

Notes:

1. Operating voltage: VDD = +3.3V ± 0.3V.
2. Test conditions: VDD = +3.3V for typical values; VDD = +3.6V for maximum values.
3. Input Ripple ≤ 0.1 Vpeak-peak.
4. f = Internal frequency.
5. Maximum current computed from Ityp: Imax = Ityp * 1.1.
6. Typical power (Ptyp) computed from Ityp: Ptyp = Ityp * 3.3V; Maximum power (Pmax) computed from Imax: Pmax = Imax * 3.6V.

3.5 Interface and Timing Waveforms

3.5.1 External Memory Bus Timing

The external memory bus timing is listed in Table 3-14 and illustrated in Figure 3-7.

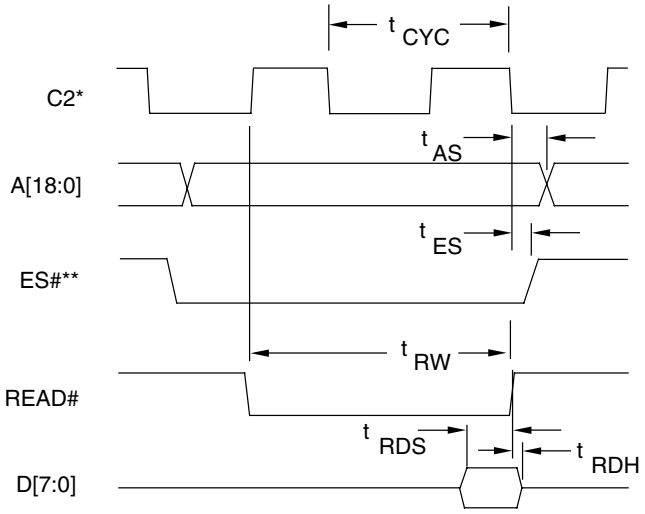
Table 3-14. Timing - External Memory Bus

Symbol	Parameter	Min	Typ.	Max	Units
t_{FI}	Internal Operating Frequency	28.224			MHz
t_{CYC}	Internal Operating Clock Cycle	35.43			ns
Read					
t_{AS}	READ# High to Address Valid	–	11.2	12.5	ns
t_{ES}	READ# High to ES Valid	–	12.2	13.5	ns
t_{RW}	READ# Pulse Width	17.72		124.01	ns
t_{RDS}	Read Data Valid to READ# High	6.1		–	ns
t_{RDH}	READ# High to Read Data Hold	0		–	ns
Write					
t_{AS}	WRITE# High to Address Valid	–	11.2	12.5	ns
t_{ES}	WRITE# High to ES Valid	–	12.2	13.5	ns
t_{WW}	WRITE# to WRITE# Pulse Width	17.72		124.01	ns
t_{WTD}	WRITE# Low to Write Data Valid	–	7.1	8.0	ns
t_{WTH}	WRITE# High to Write Data Hold	5.0		–	ns

Notes:

1. ES = RAMSEL# or ROMSEL#.
2. Read pulse width and write pulse width:
   RAM: t_{RW}, t_{WW} = 0.5 t_{CYC} = 17.72 for Non-Extended Cycle Timing
   ROM: t_{RW}, t_{WW} = 3.5 t_{CYC} = 124.01 for Extended Cycle Timing
3. Memory speed determination:
   RAM: $t_{ACCESS} = t_{CYC} - t_{ES} - t_{RDS}$ = 35.43 - 13.5 - 6.3 = 15.63 ns (i.e., use 15 ns memory)
   ROM: $t_{ACCESS} = 4(t_{CYC}) - t_{ES} - t_{RDS}$ = 4(35.43) - 13.5 - 6.3 = 121.92 ns (i.e., use 90 ns memory).
4. Output Enable to Output Delay Timing:
   RAM: $t_{OE} = t_{RW} - t_{RDS} = 0.5(t_{CYC}) - t_{RDS}$ = 17.72 - 6.3 = 11.42 ns
   ROM: $t_{OE} = t_{RW} - t_{RDS} = 3.5(t_{CYC}) - t_{RDS}$ = 124.01 - 6.3 = 117.71 ns.

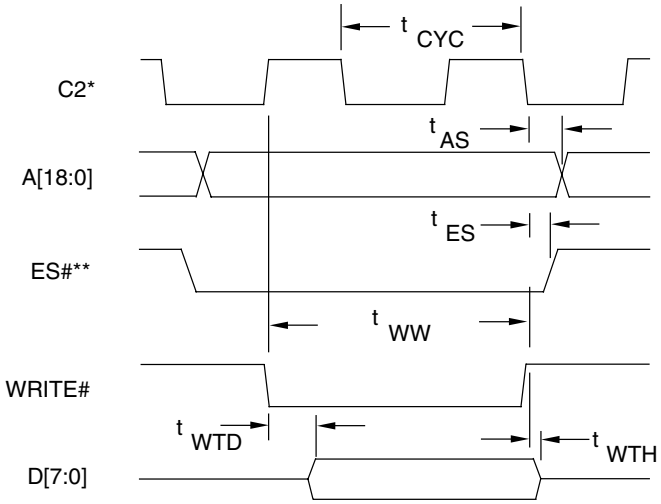
Figure 3-7. Waveforms - External Memory Bus



* C2 = Internal Phase 2 clock.

** ES# = RAMSEL# or ROMSEL#.

Read Timing



* C2 = Internal Phase 2 clock.

** ES# = RAMSEL# or ROMSEL#.

Write Timing

100491 F3-09 WF EB

3.5.2 Parallel Host Bus Timing

The parallel host bus timing is listed in Table 3-15 and illustrated in Figure 3-8.

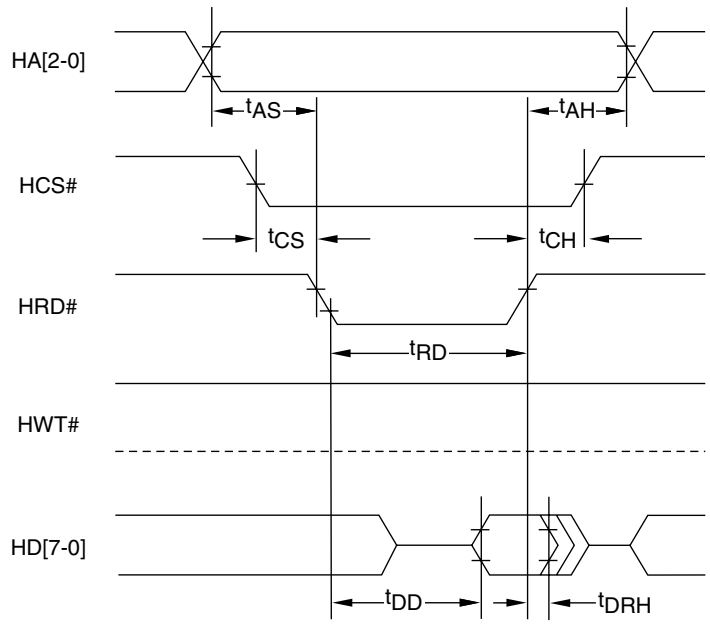
Table 3-15. Timing - Parallel Host Bus

Symbol	Parameter	Min.	Max.	Units
READ (See Notes 1, 2, 3, 4, and 5)				
t_{AS}	Address Setup	5	–	ns
t_{AH}	Address Hold	10	–	ns
t_{CS}	Chip Select Setup	0	–	ns
t_{CH}	Chip Select Hold	10	–	ns
t_{RD}	HRD# Strobe Width	54	–	ns
t_{DD}	Read Data Delay	–	25	ns
t_{DRH}	Read Data Hold	5	–	ns
WRITE (See Notes 1, 2, 3, 4, and 5)				
t_{AS}	Address Setup	5	–	ns
t_{AH}	Address Hold	15	–	ns
t_{CS}	Chip Select Setup	0	–	ns
t_{CH}	Chip Select Hold	10	–	ns
t_{WT}	HWT# Strobe Width	89	–	ns
t_{DS}	Write Data Setup (see Note 4)	–	29	ns
t_{DWH}	Write Data Hold (see Note 5)	5	–	ns

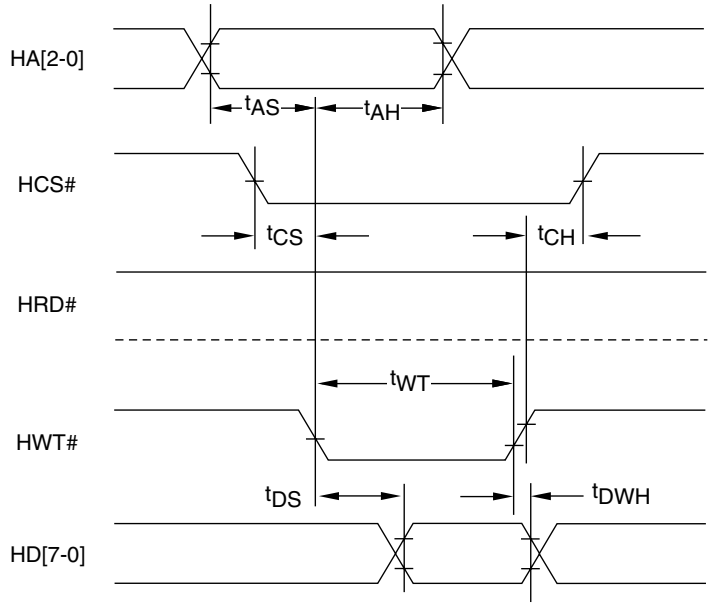
Notes:

1. When the host executes consecutive Rx FIFO reads, a minimum delay of 2 times the internal CPU clock cycle plus 15 ns (85.86 ns at 28.224 MHz) is required from the falling edge of HRD# to the falling edge of the next Host Rx FIFO HRD# clock.
2. When the Host executes consecutive Tx FIFO writes, a minimum delay of 2 times the internal CPU clock cycle plus 15 ns (85.86 ns at 28.224 MHz) is required from the falling edge of HWT# to the falling edge of the next Host Tx FIFO HWT# clock.
3. t_{DS} is measured from the point at which both HCS# and HWT# are active.
4. t_{DWH} is measured from the point at which either HCS# and HWT# become inactive.
5. Clock frequency = 28.224 MHz clock.

Figure 3-8. Waveforms - Parallel Host Bus



a. Host Read



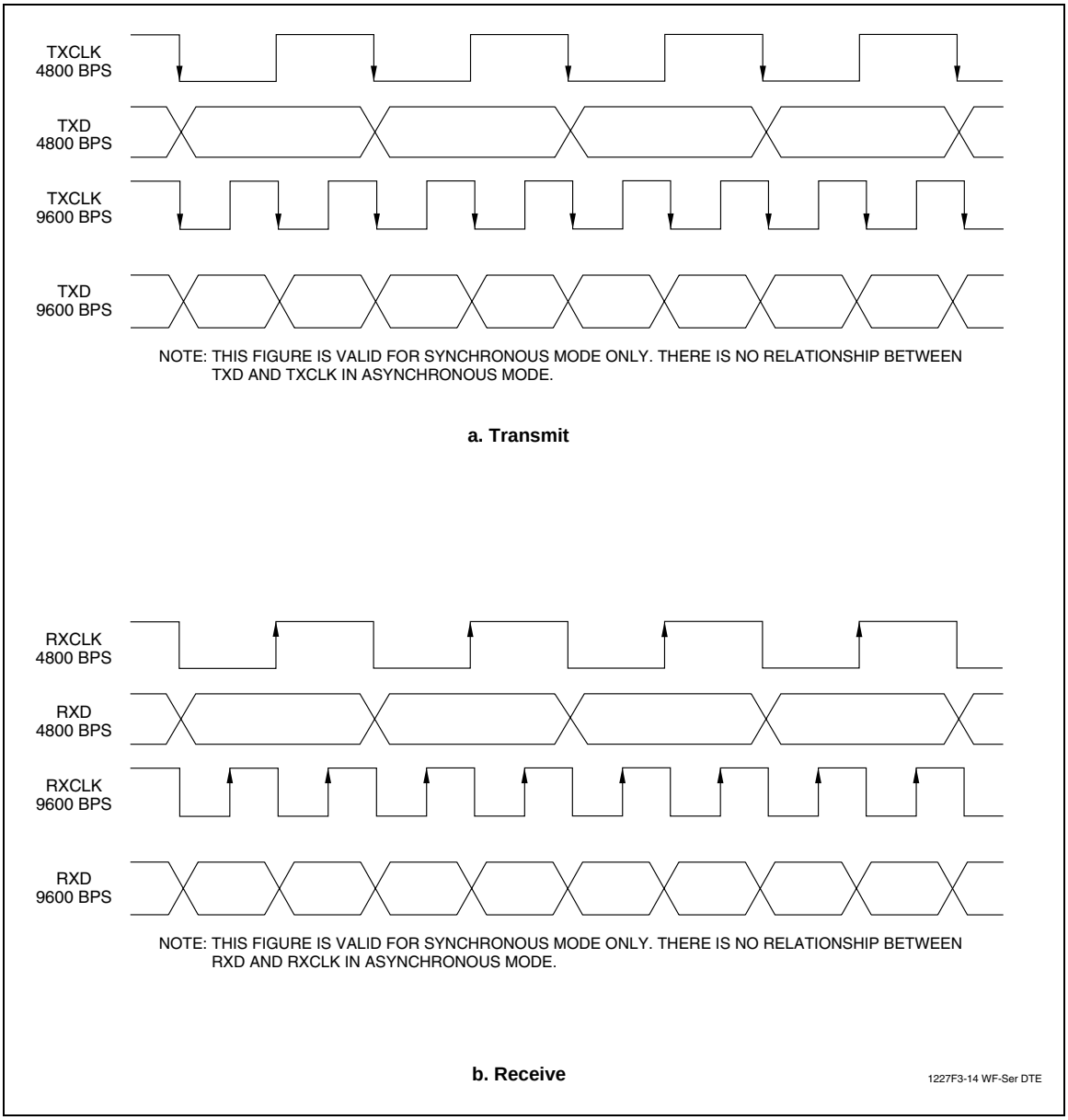
b. Host Write

100491 F3-10 WF-HB

3.5.3 Serial DTE Interface

The serial DTE interface waveforms for 4800 and 9600 bps are illustrated in Figure 3-9.

Figure 3-9. Waveforms - Serial DTE Interface



3.6 Crystal Specifications

Crystal specifications are listed in Table 3-16.

Table 3-16. Crystal Specifications

Characteristic	Value
Frequency	28.224 MHz nominal
Calibration tolerance including effects due to temperature and aging	±100 ppm at 25°C (C_L = 16.5 and 19.5 pF)
Oscillation mode	Fundamental
Calibration mode	Parallel resonant
Load capacitance, C_L	18 pF nom.
Shunt Capacitance, C_O	7 pF max.
Series resistance, R_1	35-60 Ω max. @20 nW drive level
Drive level	100µW correlation; 500µW max.
Operating temperature	0°C to 70°C
Storage temperature	–40°C to 85°C

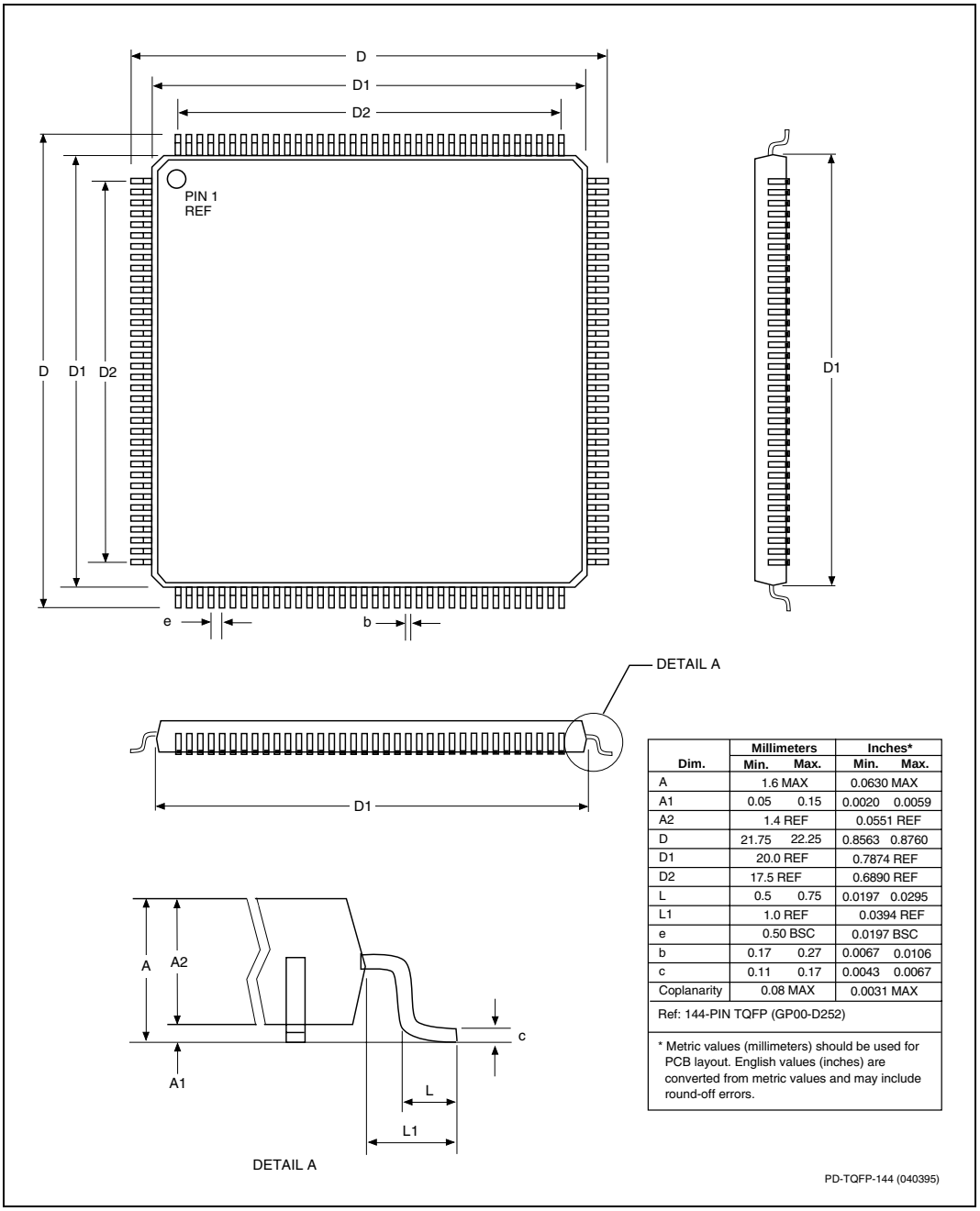
This page is intentionally blank.

4. Package Dimensions

The 144-pin TQFP package dimensions are shown in Figure 4-1.

The 32-pin TQFP package dimensions are shown in Figure 4-2.

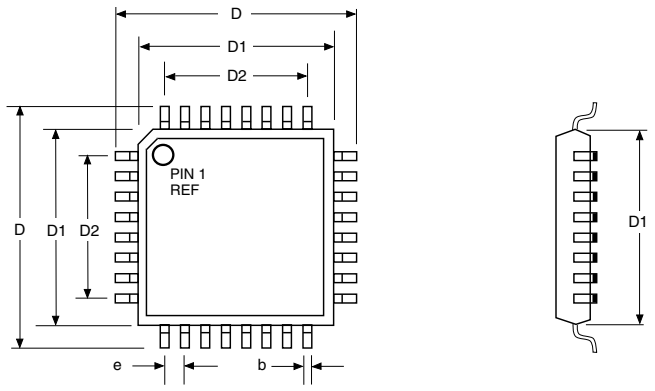
Figure 4-1. Package Dimensions - 144-Pin TQFP

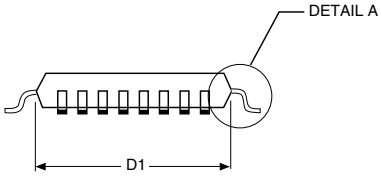


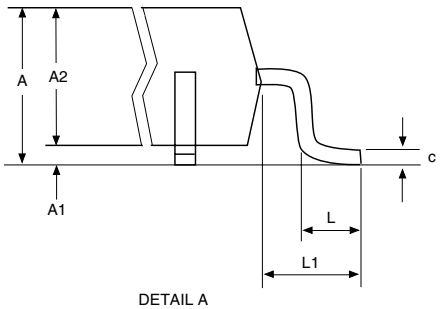
Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	21.75	22.25	0.8563	0.8760
D1		20.0 REF		0.7874 REF
D2		17.5 REF		0.6890 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.50 BSC		0.0197 BSC
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.08 MAX		0.0031 MAX
Ref: 144-PIN TQFP (GP00-D252)				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 4-2. Package Dimensions - 32-pin TQFP







Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	8.75	9.25	0.3445	0.3642
D1	7.0 REF		0.2756 REF	
D2	5.6 REF		0.2205 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.80 BSC		0.0315 BSC	
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.10 MAX		0.004 MAX	

Ref: 32-PIN TQFP (GP00-D262)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-TQFP-32 (040395)

5. Parallel Host Interface

The modem supports a 16550A interface in parallel interface versions. The 16550A interface can operate in FIFO mode or non-FIFO mode. Non-FIFO mode is the same as 16450 interface operation. FIFO mode unique operations are identified.

5.1 Overview

The parallel interface registers and the corresponding bit assignments are shown in Table 5-1.

The modem emulates the 16450/16550A interface and includes both a 16-byte receiver data first-in first-out buffer (RX FIFO) and a 16-byte transmit data first-in first-out buffer (TX FIFO). When FIFO mode is selected in the FIFO Control Register (FCR0 = 1), both FIFOs are operative. Furthermore, when FIFO mode is selected, DMA operation of the FIFO can also be selected (FCR3 = 1). When FIFO mode is not selected, operation is restricted to 16450 interface operation.

The received data is read by the host from the Receiver Buffer (RX Buffer). The RX Buffer corresponds to the Receiver Buffer Register in a 16550A device. In FIFO mode, the RX FIFO operates transparently behind the RX Buffer. Interface operation is described with reference to the RX Buffer in both FIFO and non-FIFO modes.

The transmit data is loaded by the host into the Transmit Buffer (TX Buffer). The TX Buffer corresponds to the Transmit Holding Register in a 16550A device. In FIFO mode, the TX FIFO operates transparently behind the TX Buffer. Interface operation is described with reference to the TX Buffer in both FIFO and non-FIFO modes.

Table 5-1. Parallel Interface Registers

Register	Register	Bit No.							
No.	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
7	Scratch Register (SCR)	Scratch Register							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	RX FIFO Error	Transmitter Empty (TEMT)	Transmitter Buffer Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Receiver Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Local Loopback	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	Interrupt Identify Register (IIR) (Read Only)	FIFOs Enabled	FIFOs Enabled	0	0	Pending Interrupt ID Bit 2	Pending Interrupt ID Bit 1	Pending Interrupt ID Bit 0	“0" if Interrupt Pending
2	FIFO Control Register (FCR) (Write Only)	Receiver Trigger MSB	Receiver Trigger LSB	Reserved	Reserved	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
1 (DLAB = 0)	Interrupt Enable Register (IER)	0	0	0	0	Enable Modem Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available Interrupt (ERBFI)
0 (DLAB = 0)	Transmitter Buffer Register (THR)	Transmitter FIFO Buffer Register (Write Only)							
0 (DLAB = 0)	Receiver Buffer Register (RBR)	Receiver FIFO Buffer Register (Read Only)							
1 (DLAB = 1)	Divisor Latch MSB Register (DLM)	Divisor Latch MSB							
0 (DLAB = 1)	Divisor Latch LSB Register (DLL)	Divisor Latch LSB							

5.2 Register Signal Definitions

5.2.1 IER - Interrupt Enable Register (Addr = 1, DLAB = 0)

The IER enables five types of interrupts that can separately assert the HINT output signal (Table 5-2). A selected interrupt can be enabled by setting the corresponding enable bit to a 1, or disabled by setting the corresponding enable bit to a 0. Disabling an interrupt in the IER prohibits setting the corresponding indication in the IIR and assertion of HINT. Disabling all interrupts (resetting IER0 - IER3 to a 0) inhibits setting of any Interrupt Identifier Register (IIR) bits and inhibits assertion of the HINT output. All other system functions operate normally, including the setting of the Line Status Register (LSR) and the Modem Status Register (MSR).

Bits 7-4 Not used.

Always 0.

Bit 3 Enable Modem Status Interrupt (EDSSI).

This bit, when a 1, enables assertion of the HINT output whenever the Delta CTS (MSR0), Delta DSR (MSR1), Delta TER (MSR2), or Delta DCD (MSR3) bit in the Modem Status Register (MSR) is a 1. This bit, when a 0, disables assertion of HINT due to setting of any of these four MSR bits.

Bit 2 Enable Receiver Line Status Interrupt (ELSI).

This bit, when a 1, enables assertion of the HINT output whenever the Overrun Error (LSR1), Parity Error (LSR2), Framing Error (LSR3), or Break Interrupt (LSR4) receiver status bit in the Line Status Register (LSR) changes state. This bit, when a 0, disables assertion of HINT due to change of the receiver LSR bits 1-4.

Bit 1 Enable Transmitter Holding Register Empty Interrupt (ETBEI).

This bit, when a 1, enables assertion of the HINT output when the Transmitter Empty bit in the Line Status Register (LSR5) is a 1. This bit, when a 0, disables assertion of HINT due to LSR5.

Bit 0 Enable Receiver Data Available Interrupt (ERBFI) and Character Timeout in FIFO Mode.

This bit, when a 1, enables assertion of the HINT output when the Receiver Data Ready bit in the Line Status Register (LSR0) is a1 or character timeout occurs in the FIFO mode. This bit, when a 0, disables assertion of HINT due to the LSR0 or character timeout.

5.2.2 FCR - FIFO Control Register (Addr = 2, Write Only)

The FCR is a write-only register used to enable FIFO mode, clear the RX FIFO and TX FIFO, enable DMA mode, and set the RX FIFO trigger level.

Bits 7-6 RX FIFO Trigger Level.

FCR7 and FCR6 set the trigger level for the RX FIFO (Receiver Data Available) interrupt.

FCR7	FCR6	RX FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Bits 5-4 Not used.

Bit 3 DMA Mode Select.

When FIFO mode is selected (FCR0 = 1), FCR3 selects non-DMA operation (FCR3 = 0) or DMA operation (FCR3 = 1). When FIFO mode is not selected (FCR0 = 0), this bit is not used (the modem operates in non-DMA mode in 16450 operation).

DMA operation in FIFO mode

RXRDY will be asserted when the number of characters in the RX FIFO is equal to or greater than the value in the RX FIFO Trigger Level (IIR0-IIR3 = 4h) or the received character timeout (IIR0-IIR3 = Ch) has occurred. RXRDY will go inactive when there are no more characters in the RX FIFO.

TXRDY will be asserted when there are one or more empty (unfilled) locations in the TX FIFO. TXRDY will go inactive when the TX FIFO is completely full.

Non-DMA operation in FIFO mode

RXRDY will be asserted when there are one or more characters in the RX FIFO. RXRDY will go inactive when there are no more characters in the RX FIFO.

TXRDY will be asserted when there are no characters in the TX FIFO. TXRDY will go inactive when the first character is loaded into the TX FIFO Buffer.

Bit 2 TX FIFO Reset.

When FCR2 is a 1, all bytes in the TX FIFO are cleared. This bit is cleared automatically by the modem.

Bit 1 RX FIFO Reset.

When FCR1 is a 1, all bytes in the RX FIFO are cleared. This bit is cleared automatically by the modem.

Bit 0 FIFO Enable.

When FCR0 is a 0, 16450 mode is selected and all bits are cleared in both FIFOs. When FCR0 is a 1, FIFO mode (16550A mode) is selected and both FIFOs are enabled. FCR0 must be a 1 when other bits in the FCR are written or they will not be acted upon.

5.2.3 IIR - Interrupt Identifier Register (Addr = 2)

The Interrupt Identifier Register (IIR) identifies the existence and type of up to five prioritized pending interrupts. Four priority levels are set to assist interrupt processing in the host. The four levels, in order of decreasing priority, are: Highest: Receiver Line Status, 2: Receiver Data Available or Receiver Character Timeout, 3: TX Buffer Empty, and 4: Modem Status.

When the IIR is accessed, the modem freezes all interrupts and indicates the highest priority interrupt pending to the host. Any change occurring in interrupt conditions are not indicated until this access is complete.

Bits 7-6 FIFO Mode.

These two bits copy FCR0.

Bits 5-4 Not Used.

Always 0.

Bits 3-1 Highest Priority Pending Interrupt.

These three bits identify the highest priority pending interrupt (Table 5-2). Bit 3 is applicable only when FIFO mode is selected, otherwise bit 3 is a 0.

Bit 0 Interrupt Pending.

When this bit is a 0, an interrupt is pending; IIR bits 1-3 can be used to determine the source of the interrupt. When this bit is a1, an interrupt is not pending.

Table 5-2. Interrupt Sources and Reset Control

Interrupt Identification Register					Interrupt Set and Reset Functions		
Bit 3[1]	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error OE (LSR1), Parity Error (PE) (LSR2), Framing Error (FE) (LSR3), or Break Interrupt (BI) (LSR4)	Reading the LSR
0	1	0	0	2	Received Data Available	Received Data Available (LSR0) or RX FIFO Trigger Level (FCR6-FCR7) Reached[1]	Reading the RX Buffer or the RX FIFO drops below the Trigger Level
1	1	0	0	2	Character Time-out Indication [1]	The RX FIFO contains at least 1 character and no characters have been removed from or input to the RX FIFO during the last 4 character times.	Reading the RX Buffer
0	0	1	0	3	TX Buffer Empty	TX Buffer Empty	Reading the IIR or writing to the TX Buffer
0	0	0	0	4	Modem Status	Delta CTS (DCTS) (MSR0), Delta DSR (DDSR) (MSR1), Trailing Edge Ring Indicator (TERI) (MSR3), or Delta DCD (DCD) (MSR4)	Reading the MSR

Notes:
1. FIFO Mode only.

5.2.4 LCR - Line Control Register (Addr = 3)

The Line Control Register (LCR) specifies the format of the asynchronous data communications exchange.

Bit 7 Divisor Latch Access Bit (DLAB).

This bit must be set to a 1 to access the Divisor latch registers during a read or write operation. It must be reset to a 0 to access the Receiver Buffer, the Transmitter Buffer, or the Interrupt Enable Register.

Bit 6 Set Break.

When bit 6 is a 1, the transmit data is forced to the break condition, i.e., space (0) is sent. When bit 6 is a 0, break is not sent. The Set Break bit acts only on the transmit data and has no effect on the serial in logic.

Bit 5 Stick Parity.

When parity is enabled (LCR3 = 1) and stick parity is selected (LCR5 = 1), the parity bit is transmitted and checked by the receiver as a 0 if even parity is selected (LCR4 = 1) or as a 1 if odd parity is selected (LCR4 = 0). When stick parity is not selected (LCR3 = 0), parity is transmit and checked as determined by the LCR3 and LCR4 bits.

Bit 4 Even Parity Select (EPS).

When parity is enabled (LCR3 = 1) and stick parity is not selected (LCR5 = 0), the number of 1s transmitted or checked by the receiver in the data word bits and parity bit is either even (LCR4 = 1) or odd (LCR4 = 0).

Bit 3 Enable Parity (PEN).

When bit 3 is a 1, a parity bit is generated in the serial out (transmit) data stream and checked in the serial in (receive) data stream as determined by the LCR 4 and LCR5 bits. The parity bit is located between the last data bit and the first stop bit.

Bit 2 Number of Stop Bits (STB).

This bit specifies the number of stop bits in each serial out character. If bit 2 is a 0, one stop bit is generated regardless of word length. If bit 2 is a 1 and 5-bit word length is selected, one and one-half stop bits are generated. If bit 2 is a 1 and a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The serial in logic checks the first stop bit only, regardless of the number of stop bits selected.

Bits 1-0 Word Length Select (WLS0 and WLS1).

These two bits specify the number of bits in each serial in or serial out character. The encoding of bits 0 and 1 is:

Bit 1	Bit 0	Word Length
0	0	5 Bits (Not supported)
0	1	6 Bits (Not supported)
1	0	7 Bits
1	1	8 Bits

5.2.5 MCR - Modem Control Register (Addr = 4)

The Modem Control Register (MCR) controls the interface with the modem or data set.

Bit 7-5 Not used.

Always 0.

Bit 4 Local Loopback.

When this bit is set to a 1, the diagnostic mode is selected and the following occurs:

1. Data written to the Transmit Buffer is looped back to the Receiver Buffer.
2. The DTS (MCR0), RTS (MCR1), Out1 (MCR2), and Out2 (MCR3) modem control register bits are internally connected to the DSR (MSR5), CTS (MSR4), RI (MSR6), and DCD (MSR7) modem status register bits, respectively.

Bit 3 Output 2.

When this bit is a 1, HINT is enabled. When this bit is a 0, HINT is in the high impedance state.

Bit 2 Output 1.

This bit is used in local loopback (see MCR4).

Bit 1 Request to Send (RTS).

This bit controls the Request to Send (RTS) function. When this bit is a 1, RTS is on. When this bit is a 0, RTS is off.

Bit 0 Data Terminal Ready (DTR).

This bit controls the Data Terminal Ready (DTR) function. When this bit is a 1, DTR is on. When this bit is a 0, DTR is off.

5.2.6 LSR - Line Status Register (Addr = 5)

This 8-bit register provides status information to the host concerning data transfer.

Bit 7 RX FIFO Error.

In the 16450 mode, this bit is not used and is always 0.

In the FIFO mode, this bit is set if there are one or more characters in the RX FIFO with a parity error, framing error, or break indication detected. This bit is reset to a 0 when the host reads the LSR and none of the above conditions exist in the RX FIFO.

Bit 6 Transmitter Empty (TEMT).

This bit is set to a 1 whenever the TX Buffer (THR) and equivalent of the Transmitter Shift Register (TSR) are both empty. It is reset to a 0 whenever either the THR or the equivalent of the TSR contains a character.

In the FIFO mode, this bit is set to a 1 when ever the TX FIFO and the equivalent of the TSR are both empty.

Bit 5 Transmitter Holding Register Empty (THRE) [TX Buffer Empty].

This bit, when set, indicates that the TX Buffer is empty and the modem can accept a new character for transmission. In addition, this bit causes the modem to issue an interrupt to the host when the Transmit Holding Register Empty Interrupt Enable bit (IIR1) is set to 1. The THRE bit is set to a 1 when a character is transferred from the TX Buffer. The bit is reset to 0 when a byte is written into the TX Buffer by the host.

In the FIFO mode, this bit is set when the TX FIFO is empty; it is cleared when at least one byte is in the TX FIFO.

Bit 4 Break Interrupt (BI).

This bit is set to a 1 whenever the received data input is a space (logic 0) for longer than two full word lengths plus 3 bits. The BI bit is reset when the host reads the LSR.

Bit 3 Framing Error (FE).

This bit indicates that the received character did not have a valid stop bit. The FE bit is set to a 1 whenever the stop bit following the last data bit or parity bit is detected as a logic o (space). The FE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, the error indication is associated with the particular character in the FIFO it applies to; the FE bit is set to a 1 when this character is loaded into the RX Buffer.

Bit 2 Parity Error (PE).

This bit indicates that the received data character in the RX Buffer does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR4) and the Stick Parity bit (LCR5). The PE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, the error indication is associated with the particular character in the it applies to; the PE bit is set to a 1 when this character is loaded into the RX Buffer.

Bit 1 Overrun Error (OE).

This bit is set to a 1 whenever received data is loaded into the RX Buffer before the host has read the previous data from the RX Buffer. The OE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, if data continues to fill beyond the trigger level, an overrun condition will occur only if the RX FIFO is full and the next character has been completely received.

Bit 0 Receiver Data Ready (DR).

This bit is set to a 1 whenever a complete incoming character has been received and has been transferred into the RX Buffer. The DR bit is reset to a 0 when the host reads the RX Buffer.

In the FIFO mode, the DR bit is set when the number of received data bytes in the RX FIFO equals or exceeds the trigger level specified in FCR0-FCR1.

5.2.7 MSR - Modem Status Register (Addr = 6)

The Modem Status Register (MSR) reports current state and change information of the modem. Bits 4-7 supply current state and bits 0-3 supply change information. The change bits are set to a 1 whenever a control input from the modem changes state from the last MSR read by the host. Bits 0-3 are reset to 0 when the host reads the MSR or upon reset.

Whenever bits 0, 1, 2, or 3 are set to a 1, a Modem Status Interrupt (IIR0-IIR3 = 0) is generated.

Bit 7 Data Carrier Detect (DCD).

This bit indicates the logic state of the DCD# (RLSD#) output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the Out2 bit in the MCR (MCR3).

Bit 6 Ring Indicator (RI).

This bit indicates the logic state of the RI# output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the Out1 bit in the MCR (MCR2).

Bit 5 Data Set Ready (DSR).

This bit indicates the logic state of the DSR# output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the DTR bit in the MCR (MCR0).

Bit 4 Clear to Send (CTS).

This bit indicates the logic state of the CTS# output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the RTS bit in the MCR (MCR1).

Bit 3 Delta Data Carrier Detect (DDCD).

This bit is set to a 1 when the DCD bit changes state since the MSR was last read by the host.

Bit 2 Trailing Edge of Ring Indicator (TERI).

This bit is set to a 1 when the RI bit changes from a 1 to a 0 state since the MSR was last read by the host.

Bit 1 Delta Data Set Ready (DDSR).

This bit is set to a 1 when the DSR bit has changed since the MSR was last read by the host.

Bit 0 Delta Clear to Send (DCTS).

This bit is set to a 1 when the CTS bit has changed since the MSR was last read by the host.

5.2.8 RBR - RX Buffer (Receiver Buffer Register) (Addr = 0, DLAB = 0)

The RX Buffer (RBR) is a read-only register at location 0 (with DLAB = 0). Bit 0 is the least significant bit of the data, and is the first bit received.

5.2.9 THR - TX Buffer (Transmitter Holding Register) (Addr = 0, DLAB = 0)

The TX Buffer (THR) is a write-only register at address 0 when DLAB = 0. Bit 0 is the least significant bit and the first bit sent.

5.2.10 Divisor Registers (Addr = 0 and 1, DLAB = 1)

The Divisor Latch LS (least significant byte) and Divisor Latch MS (most significant byte) are two read-write registers at locations 0 and 1 when DLAB = 1, respectively.

The baud rate is selected by loading each divisor latch with the appropriate hex value.

Programmable values corresponding to the desired baud rate are listed in Table 5-3.

5.2.11 SCR - Scratch Register (Addr = 7)

The Scratchpad Register is a read-write register at location 7. This register is not used by the modem and can be used by the host for temporary storage.

Table 5-3. Programmable Baud Rates

Divisor Latch (Hex)			
MS	**LS**	**Divisor (Decimal)**	**Baud Rate**
06	00	1536	75
04	17	1047	110
03	00	768	150
01	80	384	300
00	C0	192	600
00	60	96	1200
00	30	48	2400
00	18	24	4800
00	0C	12	9600
00	06	6	19200
00	04	4	28800
00	03	3	38400
00	02	2	57600
00	01	1	115200
00	00	NA	230400

5.3 Receiver FIFO Interrupt Operation

5.3.1 Receiver Data Available Interrupt

When the FIFO mode is enabled (FCR0 = 1) and receiver interrupt (RX Data Available) is enabled (IER0 = 1), receiver interrupt operation is as follows:

1. The Receiver Data Available Flag (LSR0) is set as soon as a received data character is available in the RX FIFO. LSR0 is cleared when the RX FIFO is empty.
2. The Receiver Data Available interrupt code (IIR0-IIR4 = 4h) is set whenever the number of received data bytes in the RX FIFO reaches the trigger level specified by FCR6-FCR7 bits; it is cleared whenever the number of received data bytes in the RX FIFO drops below the trigger level specified by FCR6-FCR7 bits.
3. The HINT interrupt is asserted whenever the number of received data bytes in the RX FIFO reaches the trigger level specified by FCR6-FCR7 bits. HINT interrupt is de-asserted when the number of received data bytes in the RX FIFO drops below the trigger level specified by FCR6-FCR7 bits.

5.3.2 Receiver Character Timeout Interrupts

When the FIFO mode is enabled (FCR0 = 1) and receiver interrupt (Receiver Data Available) is enabled (IER0 = 1), receiver character timeout interrupt operation is as follows:

1. A Receiver character timeout interrupt code (IIR0-IIR3 = Ch) is set if at least one received character is in the RX FIFO, the most recent received serial character was longer than four continuous character times ago (if 2 stop bits are specified, the second stop bit is included in this time period), and the most recent host read of the RX FIFO was longer than four continuous character times ago.

5.4 Transmitter FIFO Interrupt Operation

5.4.1 Transmitter Empty Interrupt

When the FIFO mode is enabled (FCR0 = 1) and transmitter interrupt (TX Buffer Empty) is enabled (IER0 = 1), transmitter interrupt operation is as follows:

1. The TX Buffer Empty interrupt code (IIR0-IIR3 = 2h) will occur when the TX Buffer is empty; it is cleared when the TX Buffer is written to (1 to 16 characters) or the IIR is read.
2. The TX Buffer Empty indications will be delayed 1 character time minus the last stop bit time whenever the following occur: THRE = 1 and there have not been at least two bytes at the same time in the TX FIFO Buffer since the last setting of THRE was set. The first transmitter interrupt after setting FCR0 will be immediate.

This page is intentionally blank.

NOTES

www.conexant.com
General Information:
U.S. and Canada: (800) 854-8099
International: (949) 483-6996
Headquarters – Newport Beach
4311 Jamboree Rd.
Newport Beach, CA 92660-3007

CONEXANT™
What's next in communications technologies