



# CY62128

## 128K x 8 Static RAM

### Features

- 4.5V – 5.5V operation
- CMOS for optimum speed/power
- Low active power (70 ns, LL version) — 330 mW (max.) (60 mA)
- Low standby power (70 ns, LL version) — 110 μW (max.) (20 μA)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  options

### Functional Description

The CY62128 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}_1$ ), an active HIGH chip enable ( $CE_2$ ), an active LOW output enable ( $\overline{OE}$ ), and three-state drivers. This device has an automatic power-down

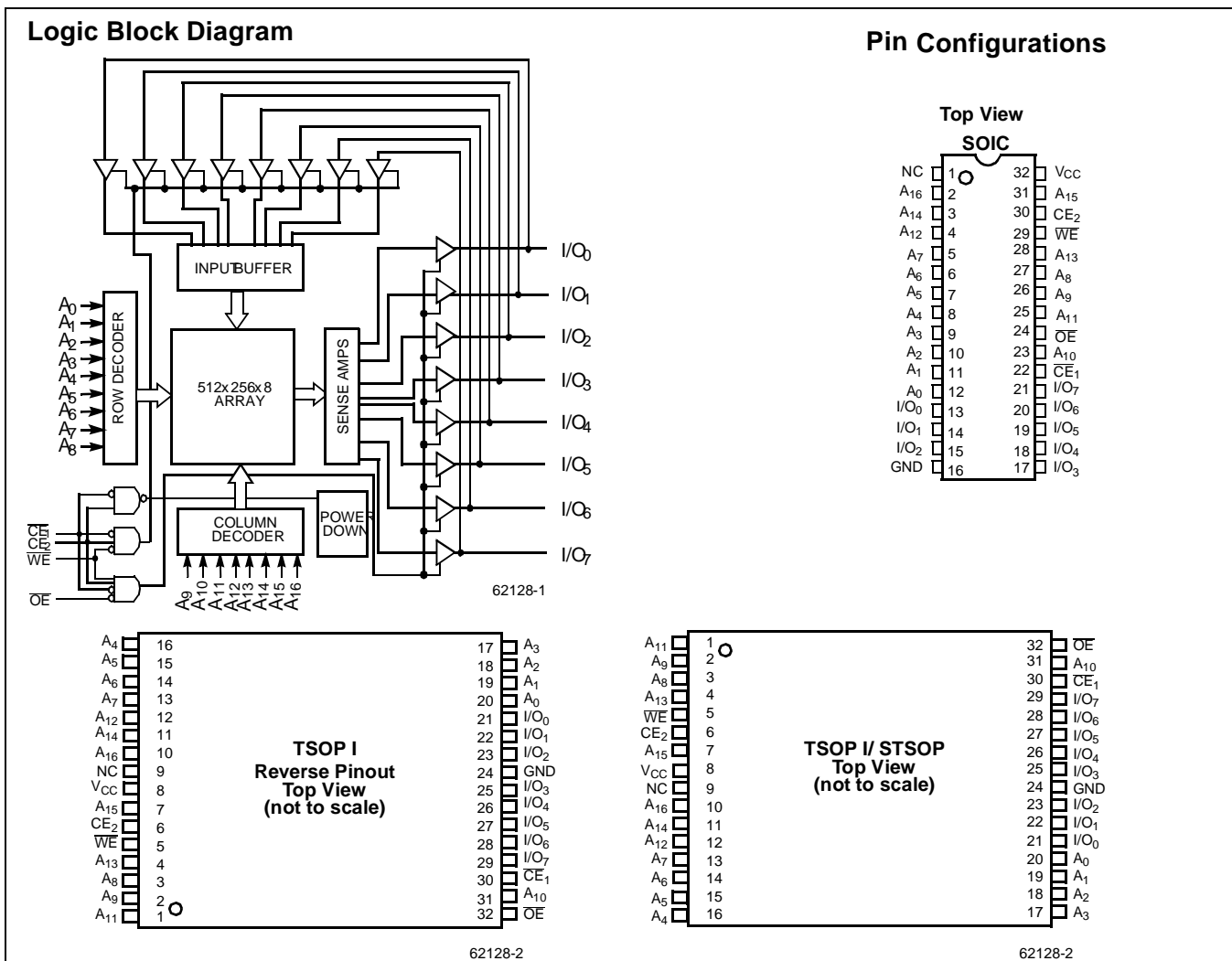
feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking chip enable one ( $\overline{CE}_1$ ) and write enable ( $\overline{WE}$ ) inputs LOW and chip enable two ( $CE_2$ ) input HIGH. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

Reading from the device is accomplished by taking chip enable one ( $\overline{CE}_1$ ) and output enable ( $\overline{OE}$ ) LOW while forcing write enable ( $\overline{WE}$ ) and chip enable two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

The CY62128 is available in a standard 450-mil-wide SOIC, 32-pin TSOP type I and STSOP packages.



**Selection Guide**

			CY62128-55	CY62128-70
Maximum Access Time (ns)			55	70
Maximum Operating Current	Commercial	L	50	40
		LL	50	40
Maximum CMOS Standby Current	Commercial	L	80	80
		LL	15	15

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

**Notes:**

- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- $T_A$  is the "instant on" case temperature.

**Electrical Characteristics** Over the Operating Range

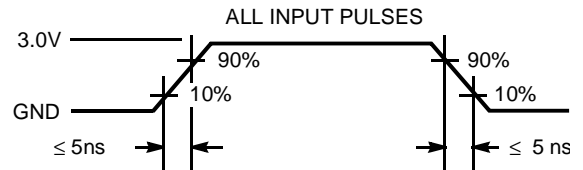
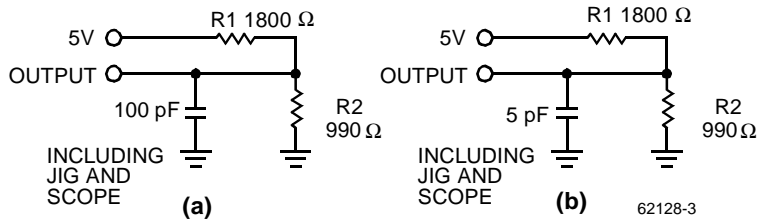
Parameter	Description	Test Conditions	62128-55			62128-70			Unit	
			Min.	Typ <sup>[3]</sup>	Max.	Min.	Typ <sup>[3]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.4			2.4			V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA			0.4			0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> + 0.3	2.2		V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3		0.8	-0.3		0.8	V	
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	+1		+1	+1		+1	μA	
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND			-300			-300	mA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com:l		40	115		40	110	mA
				L	30	70		30	60	mA
			Ind:l	LL	30	70		30	60	mA
					40	115		40	110	mA
				L	30	70		30	70	mA
				LL	30	70		30	70	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>IH</sub> or CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com:l		0.3	25		0.3	1	mA
				L	0.15	3		0.15	1	mA
			Ind:l	LL	0.1	2		0.1	1	mA
					0.3	25		0.3	1	mA
				L	0.15	3		0.15	1	mA
				LL	0.1	2		0.1	1	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, or CE <sub>2</sub> ≤ 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f=0	Com:l		0.4	500		0.4	500	μA
				L		100			100	μA
				LL		20			20	μA
			Ind		0.4	500		0.4	500	μA
				L		100			100	μA
				LL		40			40	μA

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	9	pF
C <sub>OUT</sub>	Output Capacitance		9	pF

**Notes:**

- Typical values are included for reference only and are not tested or guaranteed. Typical values are an average of the distribution across normal production variations as measured at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C, and t<sub>AA</sub> = 70ns
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT  
 OUTPUT  $\text{---} \frac{639\ \Omega}{\text{---}} \text{---} 1.77\text{V}$

 62128-3  
 62128-4

**Switching Characteristics<sup>[6]</sup> Over the Operating Range**

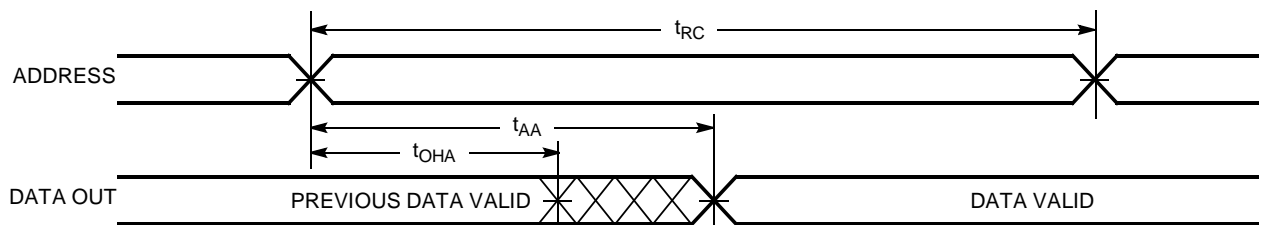
Parameter	Description	62128-55		62128-70		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	5		5		ns
$t_{ACE}$	$\overline{CE}_1$ LOW to Data Valid, $CE_2$ HIGH to Data Valid		55		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		20		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[7,8]</sup>		20		25	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW to Low Z, $CE_2$ HIGH to Low Z <sup>[8]</sup>	5		5		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH to High Z, $CE_2$ LOW to High Z <sup>[7,8]</sup>		20		25	ns
$t_{PU}$	$\overline{CE}_1$ LOW to Power-Up, $CE_2$ HIGH to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH to Power-Down, $CE_2$ LOW to Power-Down		55		70	ns
<b>WRITE CYCLE<sup>[9]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}_1$ LOW to Write End, $CE_2$ HIGH to Write End	45		60		ns
$t_{AW}$	Address Set-Up to Write End	45		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	45		50		ns
$t_{SD}$	Data Set-Up to Write End	25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[8]</sup>	5		5		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>		20		25	ns

**Notes:**

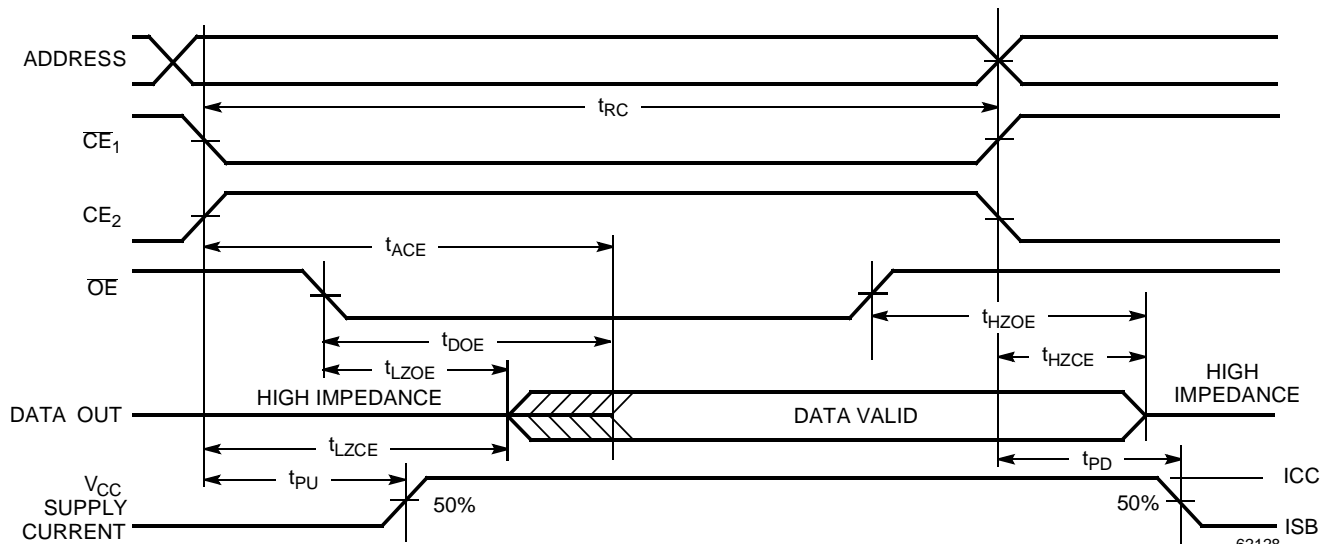
- Test conditions assume signal transition time of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 100pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $CE_2$  HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

**Data Retention Characteristics** (Over the Operating Range for “L” and “LL” version only)

Parameter	Description	Conditions <sup>[10]</sup>	Min.	Typ.	Max.	Unit	
$V_{DR}$	VCC for Data Retention		2.0			V	
$I_{CCDR}$	Data Retention Current	Coml.	L	$V_{CC}=V_{DR}=3.0V,$ $CE \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or, $V_{IN} \leq 0.3V$	0.4	100	$\mu A$
			LL			20	$\mu A$
		Incl.	L			100	$\mu A$
			LL			20	$\mu A$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns	
$t_R^{[3]}$	Operation Recovery Time		$t_{RC}$			ns	

**Switching Waveforms**
**Read Cycle No.1<sup>[11,12]</sup>**


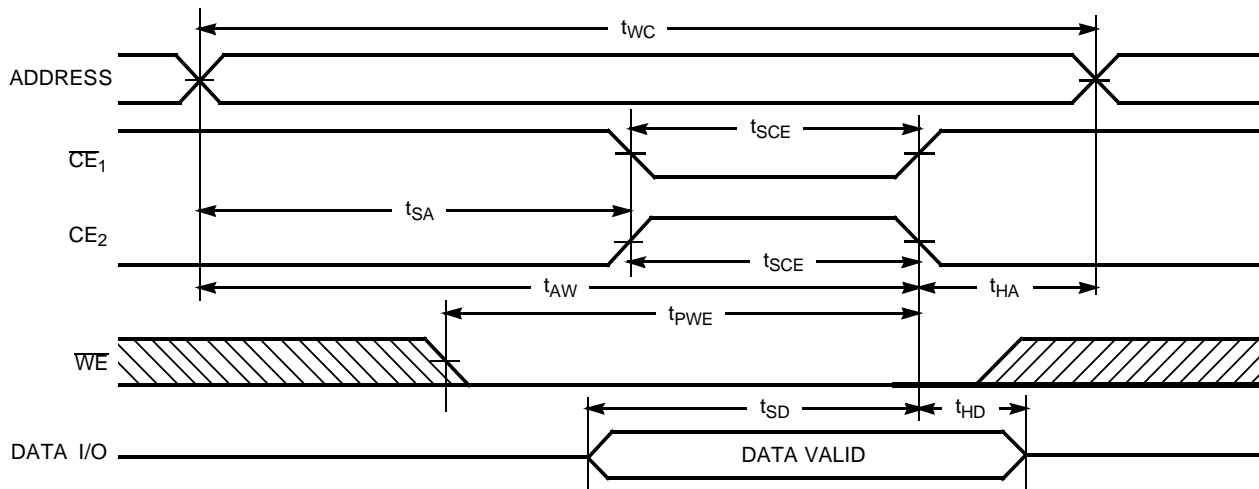
62128-5

**Read Cycle No. 2 (OE Controlled)<sup>[12,13]</sup>**


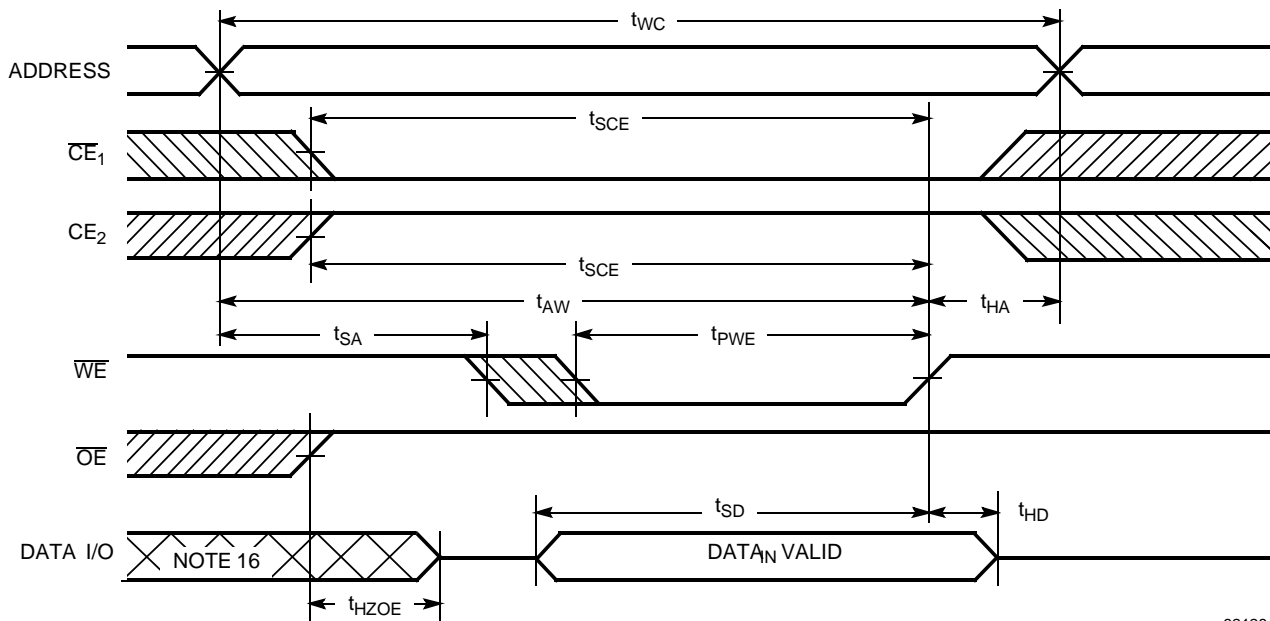
62128-6

**Notes:**

10. No input may exceed  $V_{CC} + 0.5V$ .
11. Device is continuously selected.  $\overline{OE}, CE_1 = V_{IL}, CE_2 = V_{IH}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[14,15]</sup>**


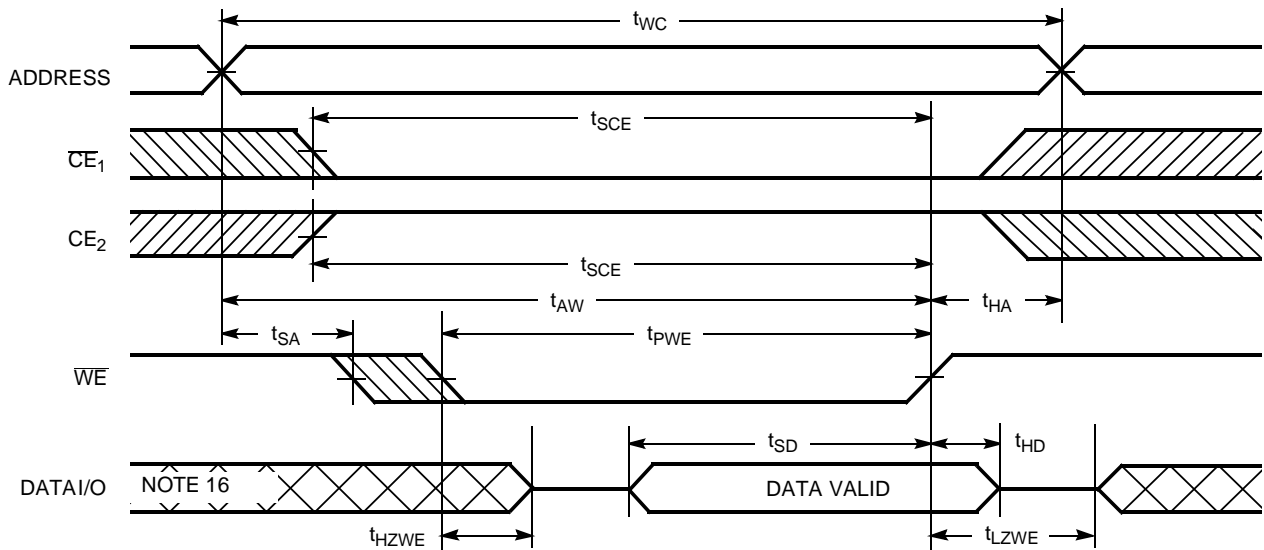
62128-7

**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[14,15]</sup>**


62128-8

**Notes:**

14. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
15. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[14,15]</sup>**


62128-9

**Truth Table**

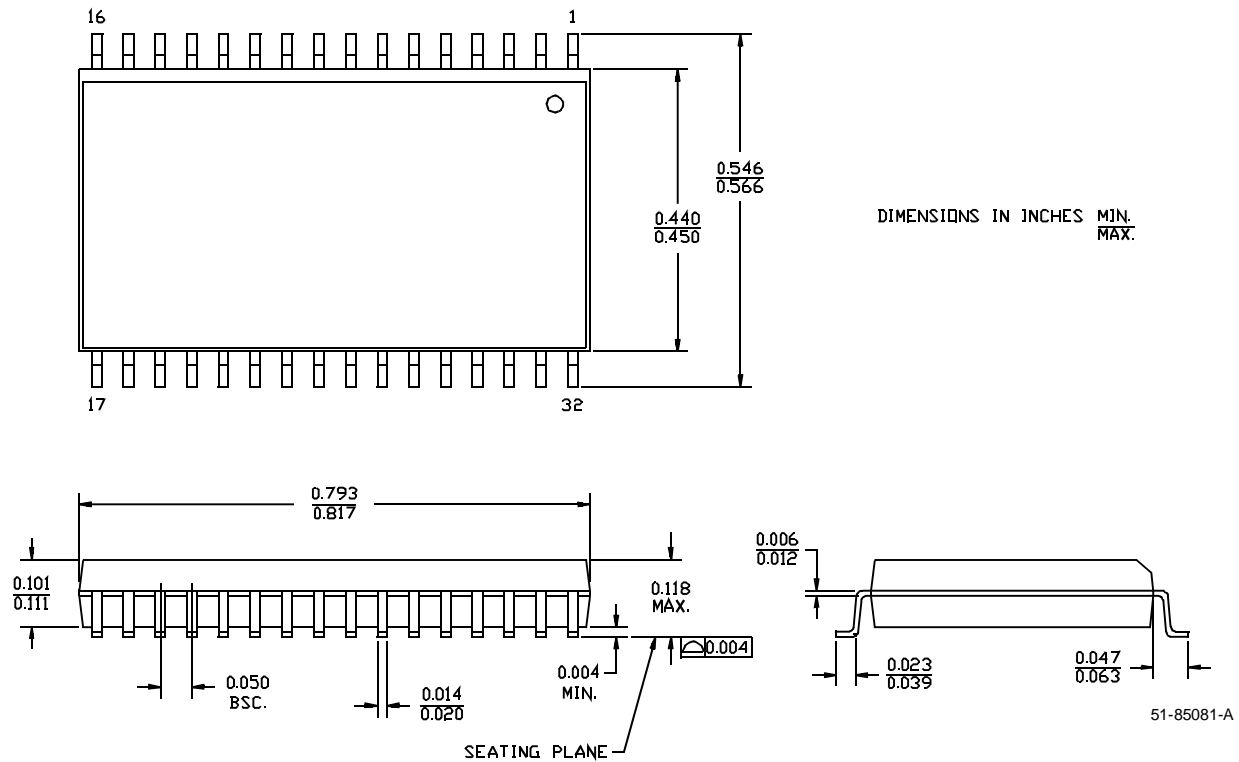
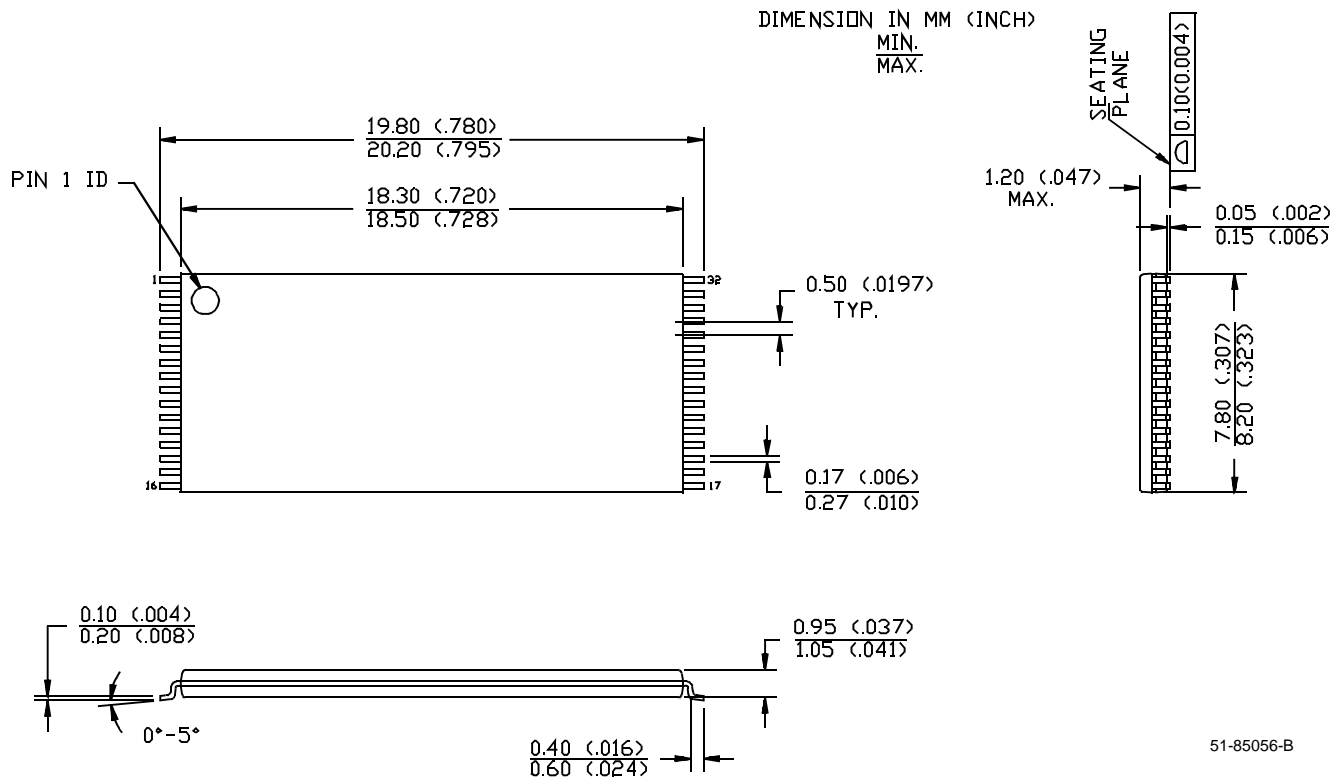
$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$	Mode	Power
H	X	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	H	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	H	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62128-55SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128-55ZC	Z32	32-Lead TSOP Type I	
	CY62128-55ZAC	ZA32	32-Lead STSOP Type I	
70	CY62128-70SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128-70ZC	Z32	32-Lead TSOP Type I	
	CY62128-70ZAC	ZA32	32-Lead STSOP Type I	
	CY62128-70ZRC	ZR32	32-Lead Reverse TSOP Type I	
	CY62128-70SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128-70ZI	Z32	32-Lead TSOP Type I	
	CY62128-70ZAI	ZA32	32-Lead STSOP Type I	
	CY62128-70ZRI	ZR32	32-Lead Reverse TSOP Type I	
	CY62128L-70SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128L-70ZC	Z32	32-Lead TSOP Type I	
	CY62128L-70ZAC	ZA32	32-Lead STSOP Type I	
	CY62128L-70ZRC	ZR32	32-Lead Reverse TSOP Type I	
	CY62128L-70SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128L-70ZI	Z32	32-Lead TSOP Type I	
	CY62128L-70ZAI	ZA32	32-Lead STSOP Type I	
	CY62128L-70ZRI	ZR32	32-Lead Reverse TSOP Type I	
	CY62128LL-70SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128LL-70ZC	Z32	32-Lead TSOP Type I	
	CY62128LL-70ZAC	ZA32	32-Lead STSOP Type I	
	CY62128LL-70ZRC	ZR32	32-Lead Reverse TSOP Type I	
CY62128LL-70SI	Z32	32-Lead 450-Mil Type I	Industrial	
CY62128LL-70ZI	Z32	32-Lead TSOP Type I		
CY62128LL-70ZAI	Z32	32-Lead STSOP Type I		
CY62128LL-70ZRI	ZR32	32-Lead Reverse TSOP Type I		

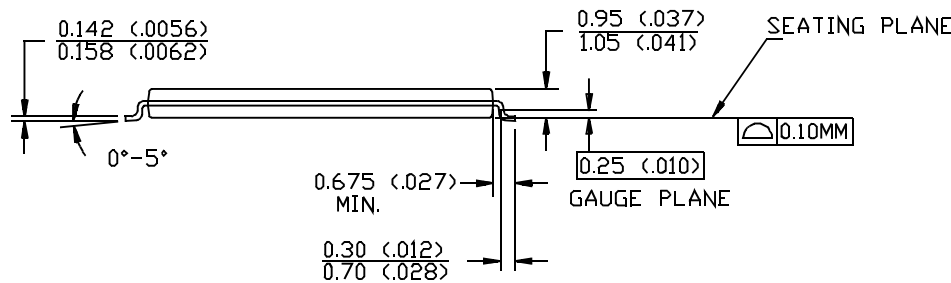
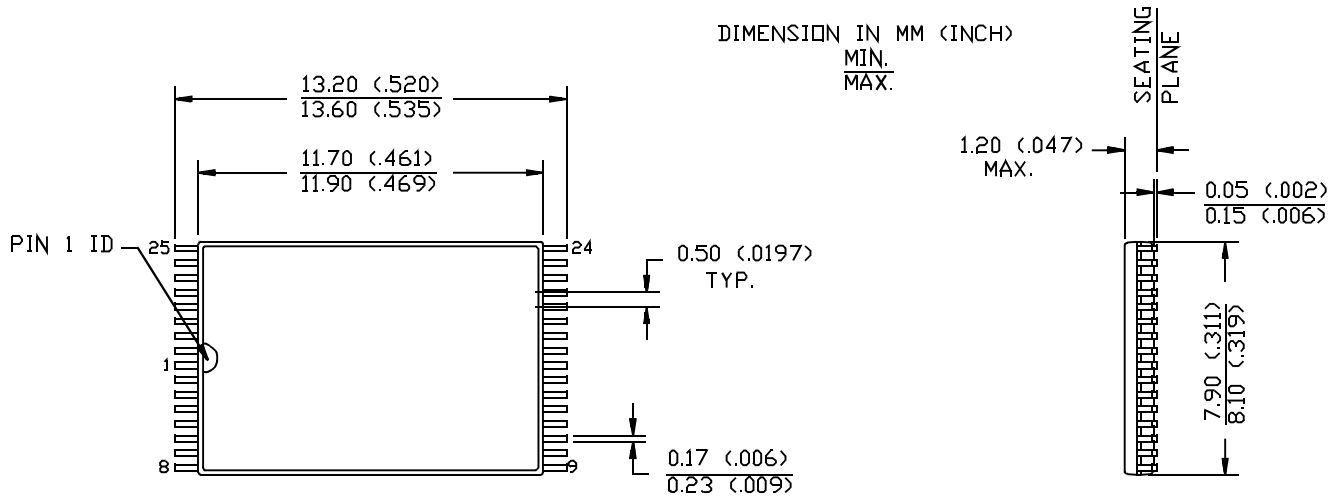
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**Package Diagrams**
**32-Lead (450 MIL) Molded SOIC S34**

**32-Lead Thin Small Outline Package Z32**


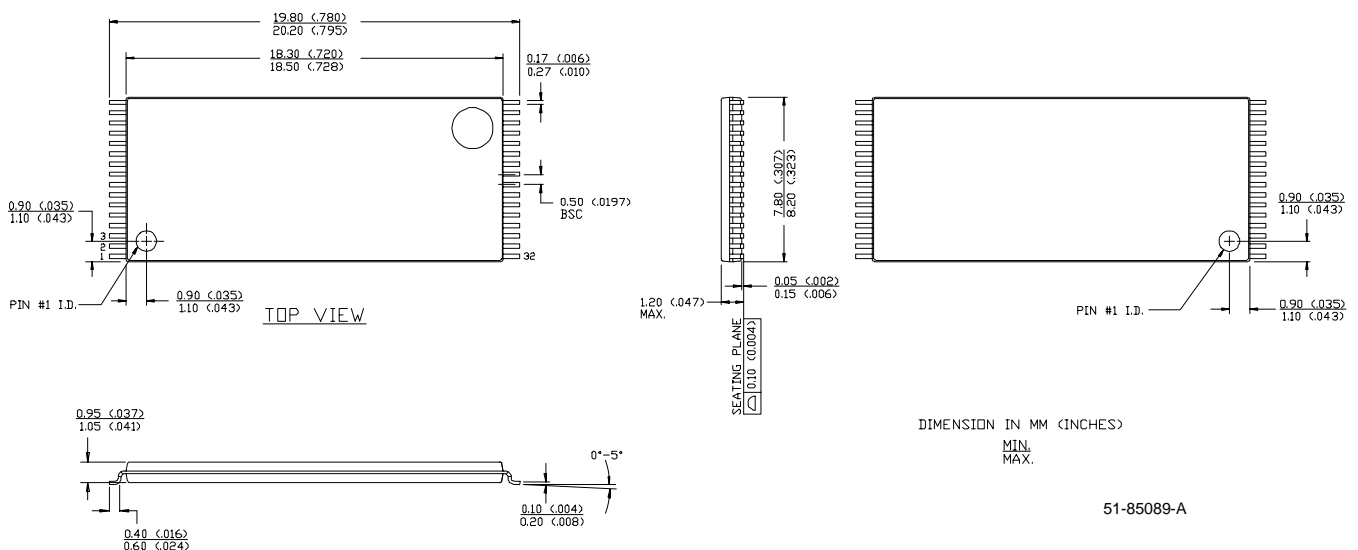
Package Diagrams (continued)

32-Lead Shrunken Thin Small Outline Package ZA32



51-85094

32-Lead Reverse Thin Small Outline Package ZR32



51-85089-A