Hex/Quad D-type Flip-Flops with Clear

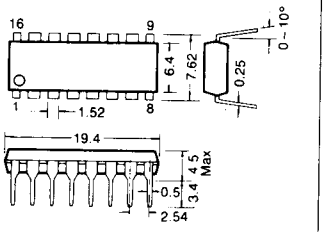
The '174 contains six, and the '175 contains four D-type filp-flops all sharing a common clock and a common clear. The '174 features single-rail outputs for every flip-flops whereas the '175 has complementary outputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

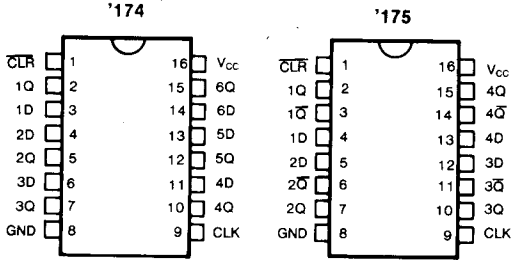
16 Dip Unit: mm



FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C

PIN CONFIGURATION



FUNCTION TABLE

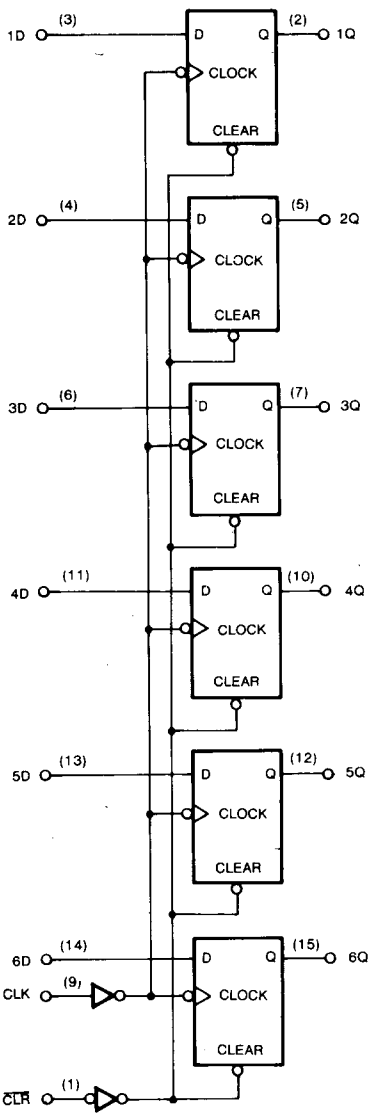
(Each Flip-Flop)

Inputs			Outputs	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

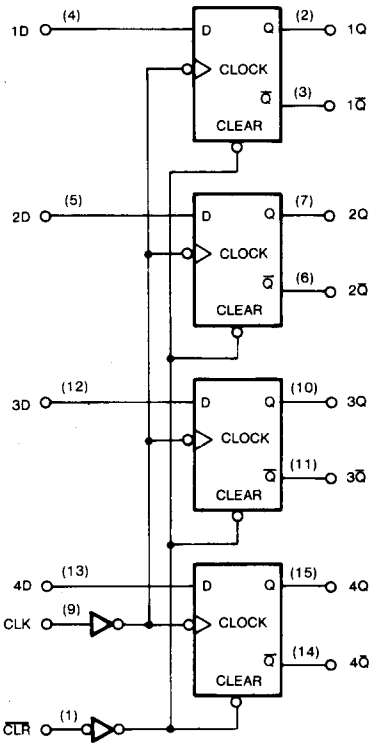
†='175 only

LOGIC DIAGRAM

'174



'175



ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Ratings	Unit
Supply Voltage Range	V_{CC}	−0.5 to +7.0	V
DC Input Diode Current (V_I<−0.5V or V_I>V_{CC} +0.5V)	I_{ik}	±20	mA
DC Output Diode Current (V_O<−0.5V or V_O>V_{CC} +0.5V)	I_{ok}	±20	mA
Continuous Output Current Per Pin (−0.5V<V_O<V_{CC} +0.5V)	I_o	±35	mA
Continuous Current Through V_{CC} or GND pins		±125	mA
Power Dissipation Per Package	P_d†	500	mW
Storage Temperature Range	T_{stg}	−65 to +150	°C

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristic		Symbol	Value			Unit
			Min	Typ	Max	
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
DC Input & Output Voltages*		V_{IN}, V_{OUT}	0		V_{CC}	V
Operating Tempesature Range	KS74HCTLS KS54HCTLS	T_A	−40 −55		+85 +125	°C °C
Input Rise & Fall Times		t_r, t_f			500	ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_A=25°C	KS74AHCT T_A=−40°C to +85°C	KS54AHCT T_A=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS174

Characteristic		Symbol	Conditions†	$T_A = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_A = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30		25	20	MHz
Maximum Propagation Delay, CLK to Q		t_{PLH}		22	30		37	45	ns
		t_{PHL}		22	30		37	45	
Maximum Propagation Delay, $\overline{CLR}$ to Q		t_{PHL}		26	35		43	52	ns
Minimum Setup Time before CLK↑	Data	t_{su}		10	13		17	20	ns
	$\overline{CLR}$ Inactive			12	16		20	25	
Minimum Hold Time, Data after CLK↑		t_h		0	0		0	0	ns
Minimum Pulse Width	CLK High or Low	t_w		10	13		17	20	ns
	$\overline{CLR}$ Low			10	13		17	20	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS175

Characteristic		Symbol	Conditions†	$T_A = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_A = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	30		25	20	MHz
Maximum Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		18	25		31	37	ns
		t_{PHL}		18	25		31	37	
Maximum Propagation Delay, $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		22	30		37	45	ns
		t_{PHL}		22	30		37	45	
Minimum Setup Time before CLK↑	Data	t_{su}		10	13		17	20	ns
	$\overline{CLR}$ Inactive			12	16		20	25	
Minimum Hold Time, Data after CLK↑		t_h		0	0		0	0	ns
Minimum Pulse Width	CLK High or Low	t_w		10	13		17	20	ns
	$\overline{CLR}$ Low			10	13		17	20	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

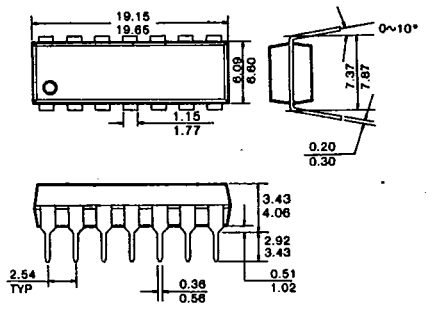
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

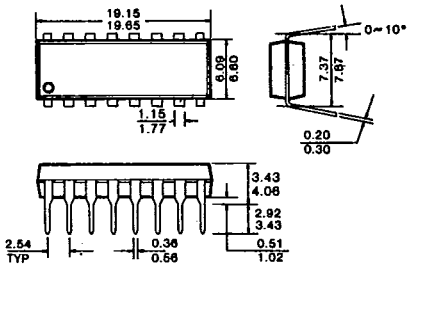
T-90-20

1. PLASTIC PACKAGES

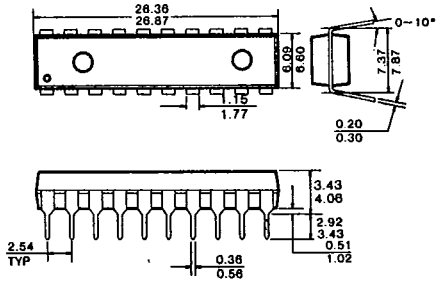
14-Pin Plastic DIP **Units: mm**



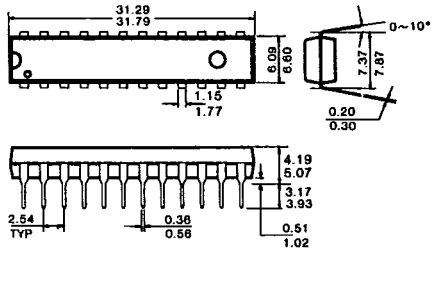
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



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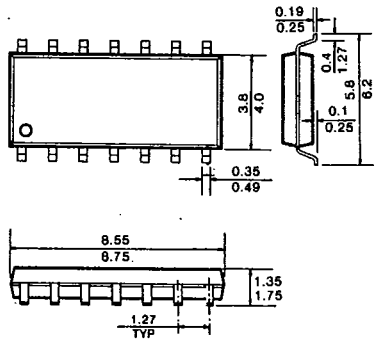
PACKAGE DIMENSIONS

T-90-20

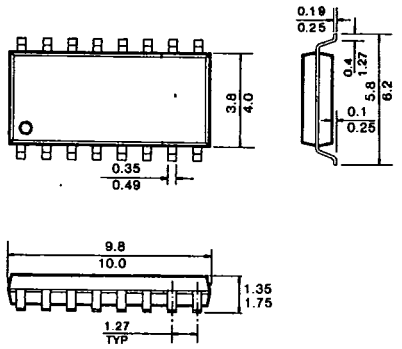
14-Pin SOP

Unit: mm



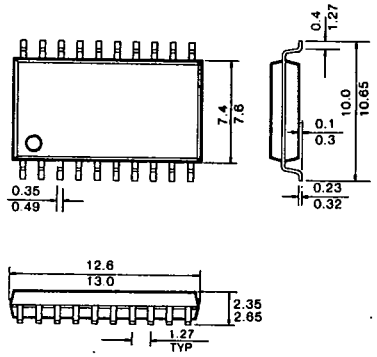
16-Pin SOP

Unit: mm



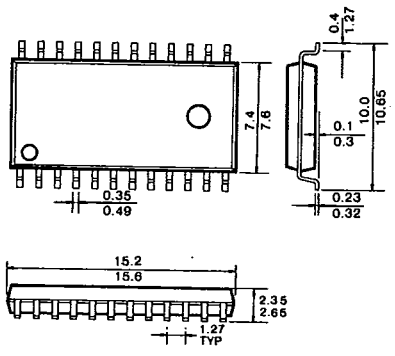
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm

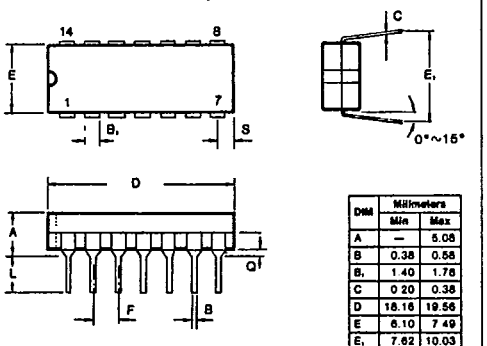


PACKAGE DIMENSIONS

T-90-20

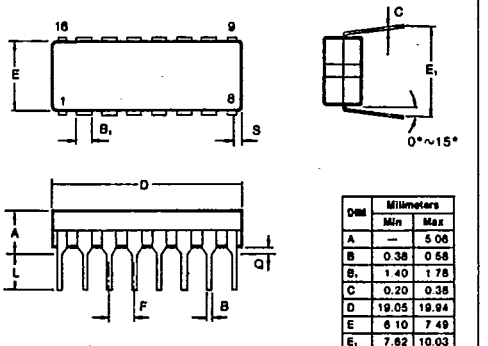
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



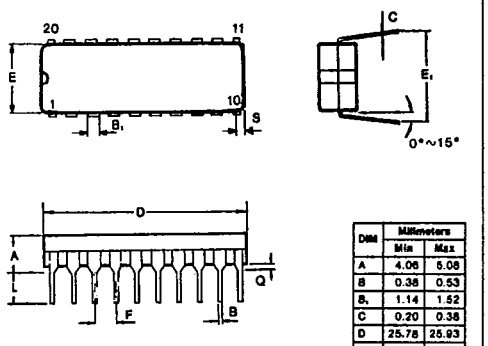
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



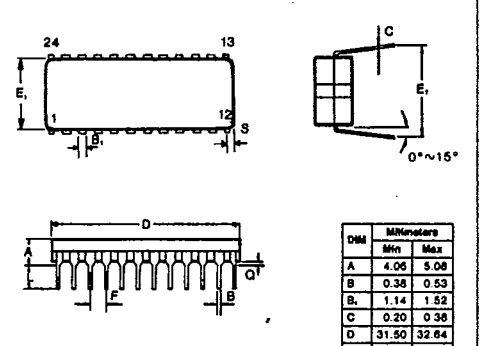
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

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