



**PRELIMINARY**

**CY37128**

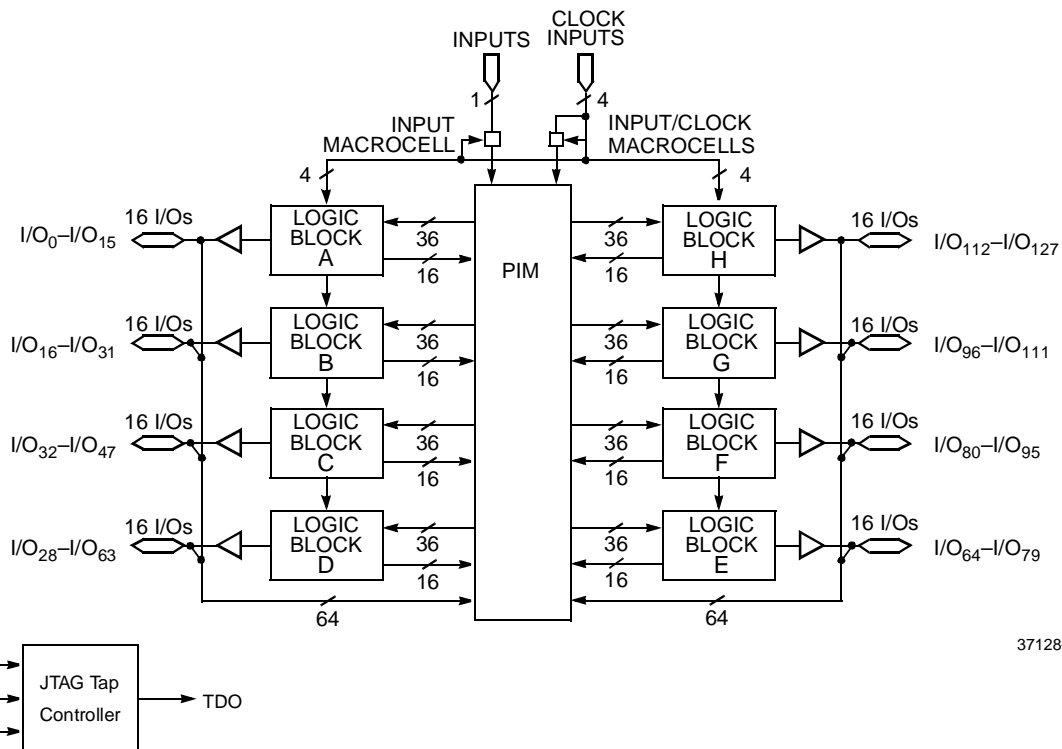
**UltraLogic™ 128-Macrocell ISR™ CPLD**

**Features**

- 128 macrocells in eight logic blocks
- In-System Reprogrammable (ISR™)
  - JTAG-compliant on-board programming
  - Design changes don't cause pinout changes
  - Design changes don't cause timing changes
- Up to 128 I/Os
  - plus 5 dedicated inputs including 4 clock inputs
- High speed
  - $f_{MAX} = 167$  MHz
  - $t_{PD} = 6.5$  ns
  - $t_S = 3.5$  ns

- $t_{CO} = 4.5$  ns
- Product-term clocking
- IEEE 1149.1 JTAG boundary scan
- Programmable slew rate control on individual I/Os
- Low power option on individual logic block basis
- 5V and 3.3V I/O capability
- User-Programmable Bus Hold capabilities on all I/Os
- Simple Timing Model
- PCI compliant
- 84-160 pins in TQFP, PLCC and CLCC packages
- Pinout compatible with the CY37064/37064V, CY37128V, CY37192/37192V, CY37256/37256V, CY7C373i, CY7C374i, CY7C375i

**Logic Block Diagram (160-pin TQFP)**



**Selection Guide**

	<b>CY37128-167</b>	<b>CY37128-125</b>	<b>CY37128-100</b>
Maximum Propagation Delay, $t_{PD}$ (ns)	6.5	10	12
Minimum Set-Up, $t_S$ (ns)	4	5.5	7.0
Maximum Clock to Output, $t_{CO}$ (ns)	4	6.5	6.5
Typical Supply Current, $I_{CC}$ (mA) in Low Power Mode	30	30	30

## Functional Description

The CY37128 is an In-System Reprogrammable (ISR) Complex Programmable Logic Device (CPLD) and is part of the Ultra37000™ family of high-density, high-speed CPLDs. Like all members of the Ultra37000 family, the CY37128 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

# of Pins	# Buried Macrocells	# I/O Macrocells	Package Types
84	64	64	PLCC/CLCC
100	64	64	TQFP
160	0	128	TQFP

For a more detailed description of the architecture and features of the CY37128 see the Ultra37000 family data sheet.

### Fully Routable with 100% Logic Utilization

The CY37128 is designed with a robust routing architecture which allows utilization of the entire device with a fixed pinout. This makes Ultra37000 optimal for implementing on-board design changes using ISR without changing pinouts.

### Simple Timing Model

The CY37128 features a very simple timing model with predictable delays. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. The timing model allows for design changes with ISR without causing changes to system performance.

### Low Power Operation

Each Logic Block of the CY37128 can be configured as either High-Speed (default) or Low-Power. In the Low-Power mode, the logic block consumes approximately 50% less power and slows down by  $t_{LP}$ .

### Output Slew Rate Control

Each output can be configured with either a fast edge rate (default) for high performance, or a slow edge rate for added

noise reduction. In the fast edge rate mode, outputs switch at 3V/ns max. and in the slow edge rate mode, outputs switch at 1V/ns max. There is a nominal delay for I/Os using the slow edge rate mode.

### 3.3V or 5V I/O Operation

The CY37128 operates with a 5V supply, and can support 5V or 3.3V I/O levels.  $V_{CCO}$  connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the  $V_{CCO}$  pins to 5V the user insures 5V TTL levels on the outputs. If  $V_{CCO}$  is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. A nominal timing delay is incurred on output buffers when  $V_{CCO}$  is set to 3.3V. This device requires 5V ISR programming.

### In System Reprogramming

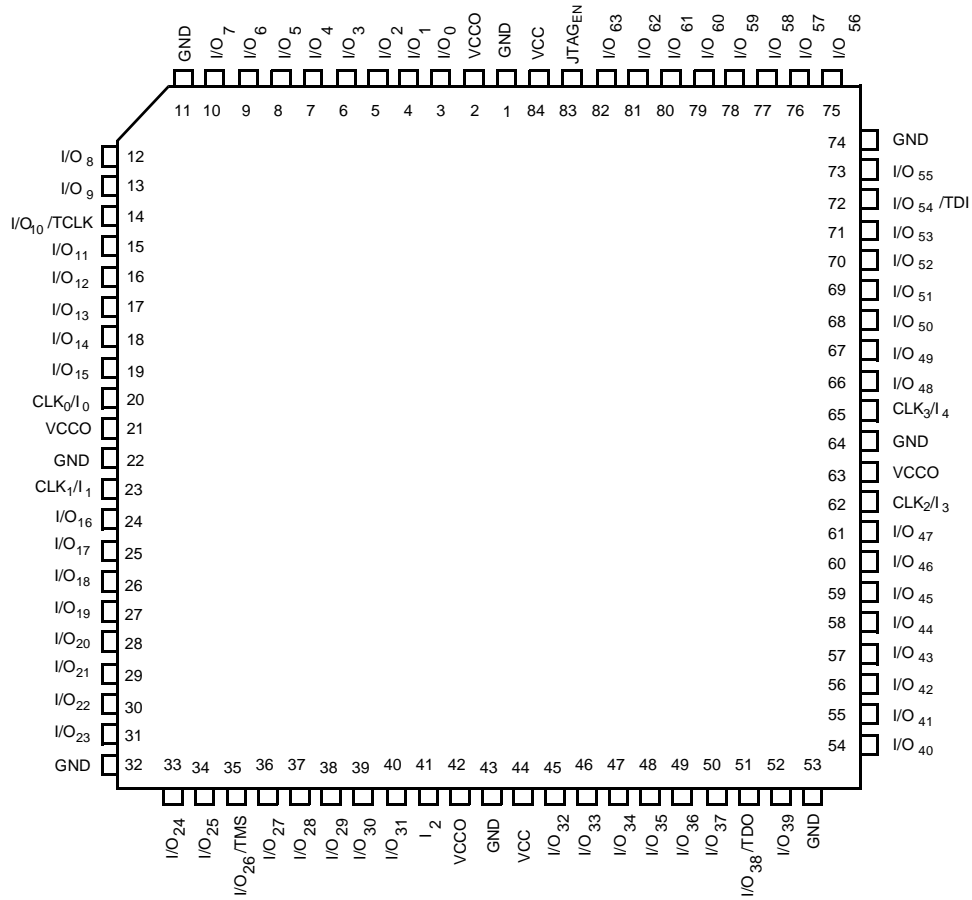
The CY37128 can be programmed in system using IEEE 1149.1 compliant JTAG programming protocol. The CY37128 can also be programmed on a number of traditional parallel programmers including Cypress's *Impulse3™* programmer and industry standard third-party programmers. For an overview of ISR programming, refer to the Ultra37000 Family data sheet and for UltraISR cable and software specifications, refer to InSRkit: ISR Programming data sheet (CY3600i).

### User-Programmable Bus Hold

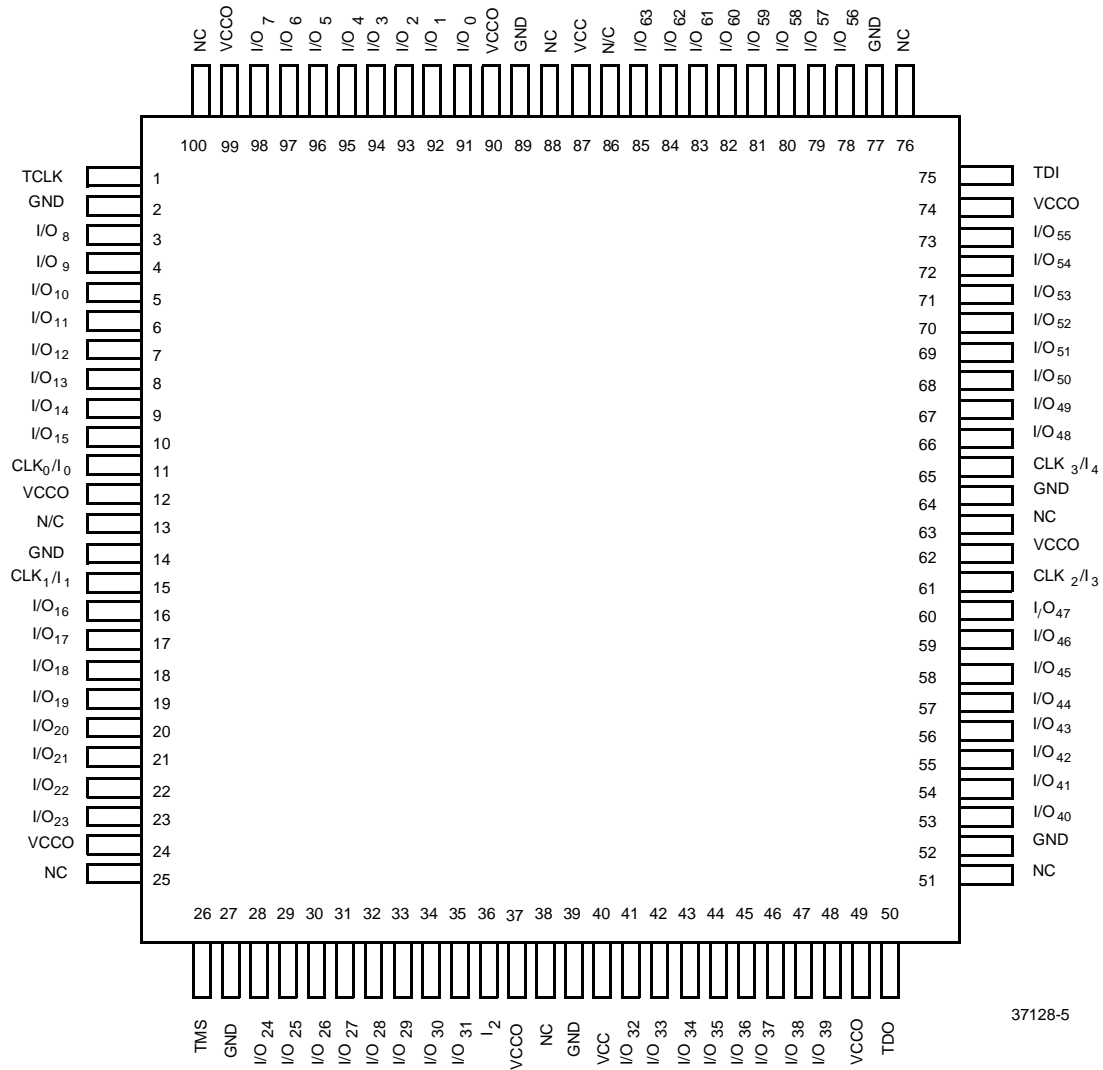
All outputs of the CY37128 can either be configured into bus hold mode or left floating. When in bus hold mode, the undriven outputs retain their last value with a weak latch. This feature allows the designer the flexibility of either eliminating or including external pull-up/pull-down resistors. Enabling this feature affects all I/Os simultaneously.

### Design Tools

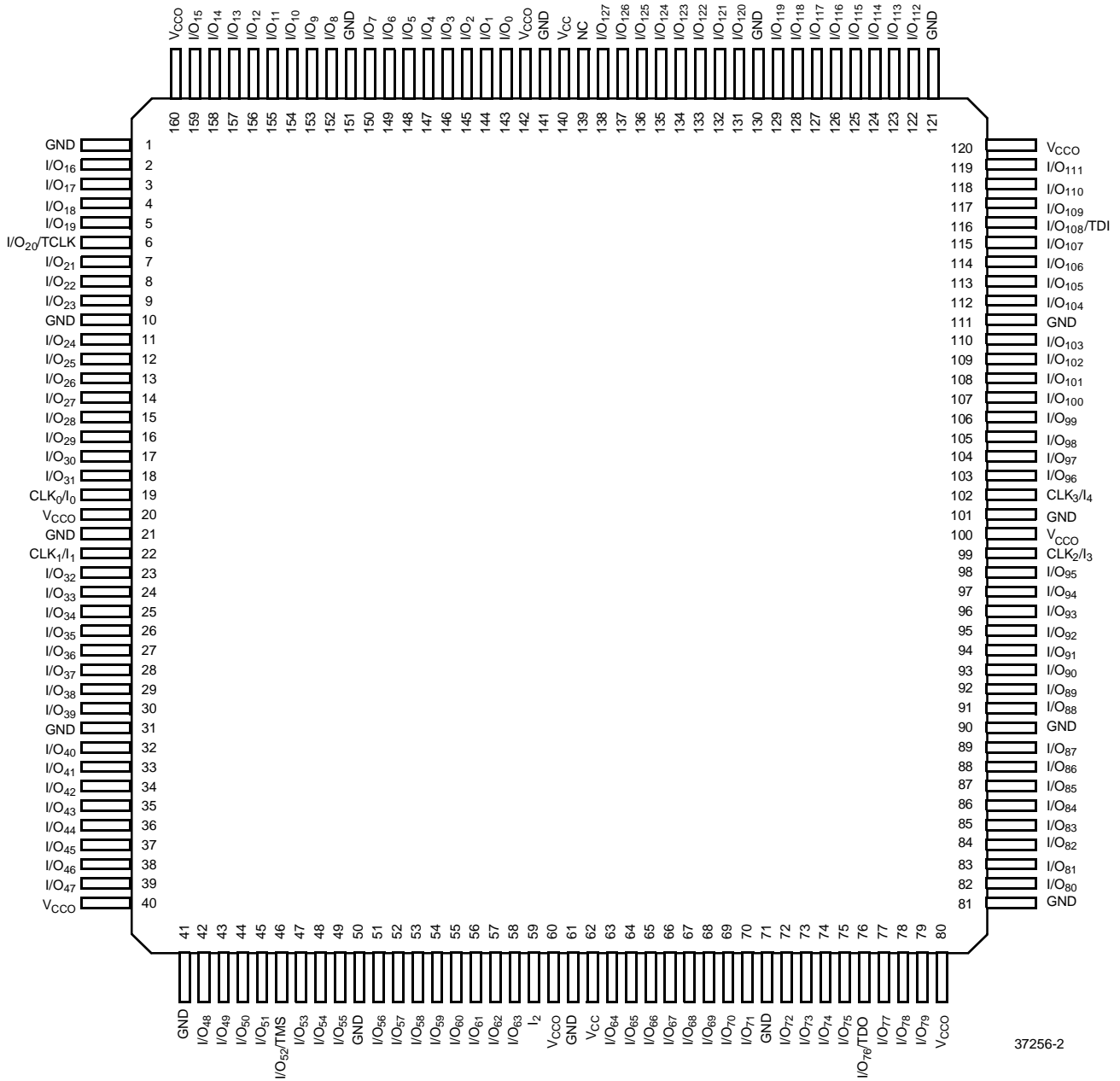
Development software for the CY37128 is available from Cypress's *Warp™* or third-party bolt-in software packages as well as a number of third-party development packages. Please refer to the *Warp* or third-party tool support data sheets for further information.

**Pin Configurations**
**84-pin PLCC/CLCC**
**Top View**


37128-4

**Pin Configurations (continued)**
**100-pin TQFP  
Top View**


37128-5

**Pin Configurations (continued)**
**160-pin TQFP  
Top View**




**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -0.5V to +7.0V  
 DC Program Voltage ..... 4.5 to 5.5V  
 Current into Outputs ..... 16 mA  
 Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

**Operating Range<sup>[1]</sup>**

Range	Ambient Temperature <sup>[1]</sup>	Junction Temperature	Output Condition	V <sub>CC</sub>	V <sub>CCO</sub>
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	-40°C to +85°C	-40°C to +125°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military <sup>[2]</sup>	-55°C to +125°C	-55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

Shaded areas contain advance information.

**Notes:**

1. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 family devices see the Ultra37000 family data sheet.
2. T<sub>A</sub> is the "instant on" case temperature.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min.	I <sub>OH</sub> = -3.2 mA (Com'I/Ind) <sup>[3]</sup>	2.4			V
			I <sub>OH</sub> = -2.0 mA (Mil) <sup>[3]</sup>	2.4			V
V <sub>OHZ</sub>	Output HIGH Voltage with Output Disabled <sup>[7]</sup>	V <sub>CC</sub> = Max.	I <sub>OH</sub> = 0 μA (Com'I/Ind) <sup>[4]</sup>			4.0	V
			I <sub>OH</sub> = -50 μA (Com'I/Ind) <sup>[4]</sup>			3.6	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min.	I <sub>OL</sub> = 16 mA (Com'I/Ind) <sup>[3]</sup>			0.5	V
			I <sub>OL</sub> = 12 mA (Mil) <sup>[3]</sup>			0.5	V
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs <sup>[5]</sup>		2.0		V <sub>CCmax</sub>	V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs <sup>[5]</sup>		-0.5		0.8	V
I <sub>IX</sub>	Input Load Current	V <sub>I</sub> = GND OR V <sub>CC</sub>		-10		10	μA
I <sub>OZ</sub>	Output Leakage Current	V <sub>O</sub> = GND or V <sub>CC</sub> , Output Disabled		-50		50	μA
		V <sub>CC</sub> = Max., V <sub>O</sub> = 3.3V, Output Disabled <sup>[4]</sup>		0	-70	-125	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[6, 7]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V		-30		-160	mA
I <sub>BHL</sub>	Input Bus Hold LOW Sustaining Current	V <sub>CC</sub> = Min., V <sub>IL</sub> = 0.8V		+75			μA
I <sub>BHH</sub>	Input Bus Hold HIGH Sustaining Current	V <sub>CC</sub> = Min., V <sub>IH</sub> = 2.0V		-75			μA
I <sub>BHLO</sub>	Input Bus Hold LOW Overdrive Current	V <sub>CC</sub> = Max.				+500	μA
I <sub>BHHO</sub>	Input Bus Hold HIGH Overdrive Current	V <sub>CC</sub> = Max.				-500	μA

**Inductance**<sup>[7]</sup>

Parameter	Description	Test Conditions	160-Pin TQFP	84-lead CLCC	84-lead PLCC	100-Pin TQFP	Unit
L	Maximum Pin Inductance	V <sub>IN</sub> = 5.0V at f = 1 MHz	9	5	8	8	nH

**Capacitance**<sup>[7]</sup>

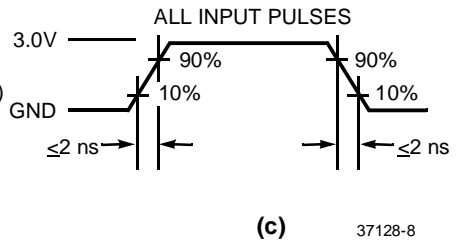
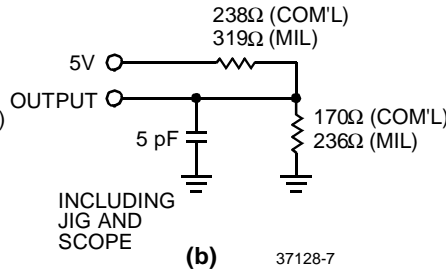
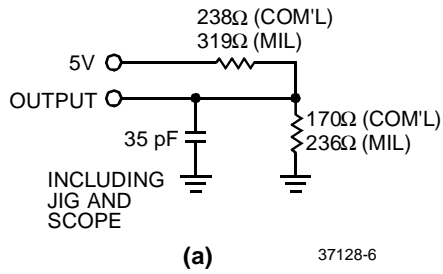
Parameter	Description	Test Conditions	Max.	Unit
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>IN</sub> = 5.0V at f = 1 MHz at T <sub>A</sub> = 25°C	8	pF
C <sub>CLK</sub>	Clock Signal Capacitance	V <sub>IN</sub> = 5.0V at f = 1 MHz at T <sub>A</sub> = 25°C	12	pF

**Endurance Characteristics**<sup>[7]</sup>

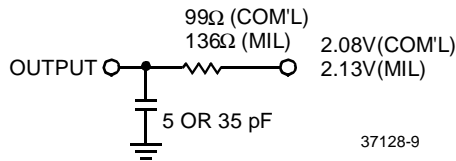
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions <sup>[1]</sup>	1,000	10,000	Cycles

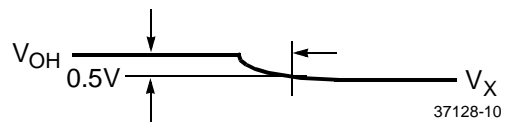
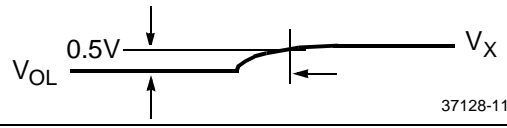
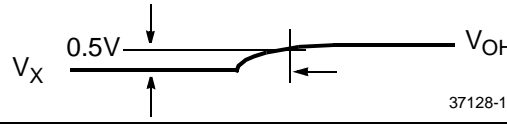
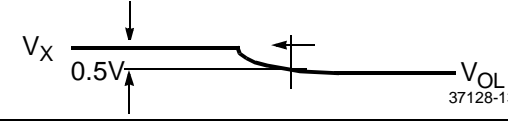
**Notes:**

- I<sub>OH</sub> = -2 mA, I<sub>OL</sub> = 2 mA for TDO.
- When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT



Parameter <sup>[8]</sup>	$V_X$	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	$V_{the}$	

**(d) Test Waveforms**
**Note:**

 8.  $t_{ER}$  measured with 5-pF AC Test Load and  $t_{EA}$  measured with 35-pF AC Test Load.



**Switching Characteristics** Over the Operating Range<sup>[9]</sup>

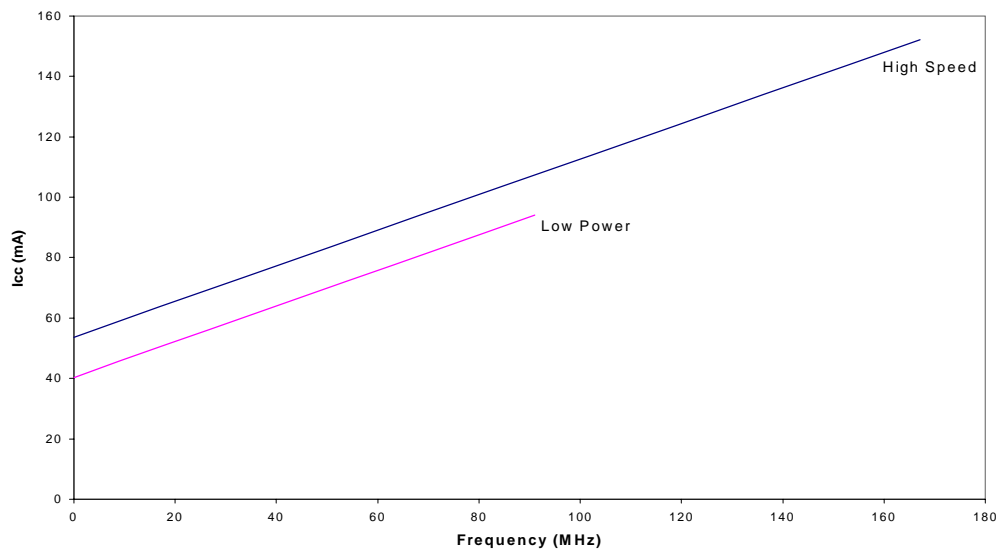
Parameter	Description	37128-167		37128-125		37128-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Combinatorial Mode Parameters</b>								
$t_{PD}^{[10, 11, 12]}$	Input to Combinatorial Output		6.5		10		12	ns
$t_{PDL}^{[10, 11, 12]}$	Input to Output Through Transparent Input or Output Latch		10		13		16.5	ns
$t_{PDLL}^{[10, 11, 12]}$	Input to Output Through Transparent Input and Output Latches		12		15		17	ns
$t_{EA}^{[10, 11, 12]}$	Input to Output Enable		10		14		16	ns
$t_{ER}^{[10]}$	Input to Output Disable		10		14		16	ns
<b>Input Register Parameters</b>								
$t_{WL}$	Clock or Latch Enable Input LOW Time <sup>[7]</sup>	2.5		3		3		ns
$t_{WH}$	Clock or Latch Enable Input HIGH Time <sup>[7]</sup>	2.5		3		3		ns
$t_{IS}$	Input Register or Latch Set-Up Time	2		2		2.5		ns
$t_{IH}$	Input Register or Latch Hold Time	2		2		2.5		ns
$t_{ICO}^{[10, 11, 12]}$	Input Register Clock or Latch Enable to Combinatorial Output		11		12.5		16	ns
$t_{ICOL}^{[10, 11, 12]}$	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		12		16		18	ns
<b>Synchronous Clocking Parameters</b>								
$t_{CO}^{[11, 12]}$	Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable to Output		4		6.5		6	ns
$t_S^{[10]}$	Set-Up Time from Input to Sync. Clk (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable	4		5.5		7		ns
$t_H$	Register or Latch Data Hold Time	0		0		0		ns
$t_{CO2}^{[10, 11, 12]}$	Output Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable to Combinatorial Output Delay (Through Logic Array)		10		14		16	ns
$t_{SCS}^{[10]}$	Output Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable to Output Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable (Through Logic Array)	6		8.0		10		ns
$t_{SL}^{[10]}$	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable	7.5		10		12		ns
$t_{HL}$	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable	0		0		0		ns
<b>Product Term Clocking Parameters</b>								
$t_{COPT}^{[10, 11, 12]}$	Product Term Clock or Latch Enable (PTCLK) to Output		10		13		13	ns
$t_{SPT}$	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	2.5		3		3		ns
$t_{HPT}$	Register or Latch Data Hold Time	2.5		3		3		ns
$t_{ISPT}^{[10]}$	Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)		-2		-2		-2	ns

**Notes:**

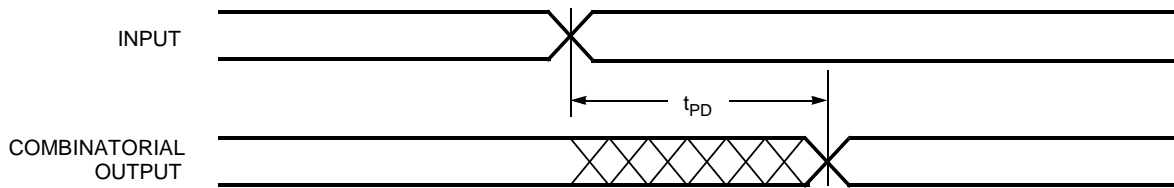
9. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
10. Logic Blocks operating in low power mode, add  $t_{LP}$  to this spec.
11. Outputs using Slow Output Slew Rate, add  $t_{SLEW}$  to this spec.
12. When  $V_{CC0} = 3.3V$ , add  $t_{3.3IO}$  to this spec.

**Switching Characteristics** Over the Operating Range<sup>[9]</sup> (continued)

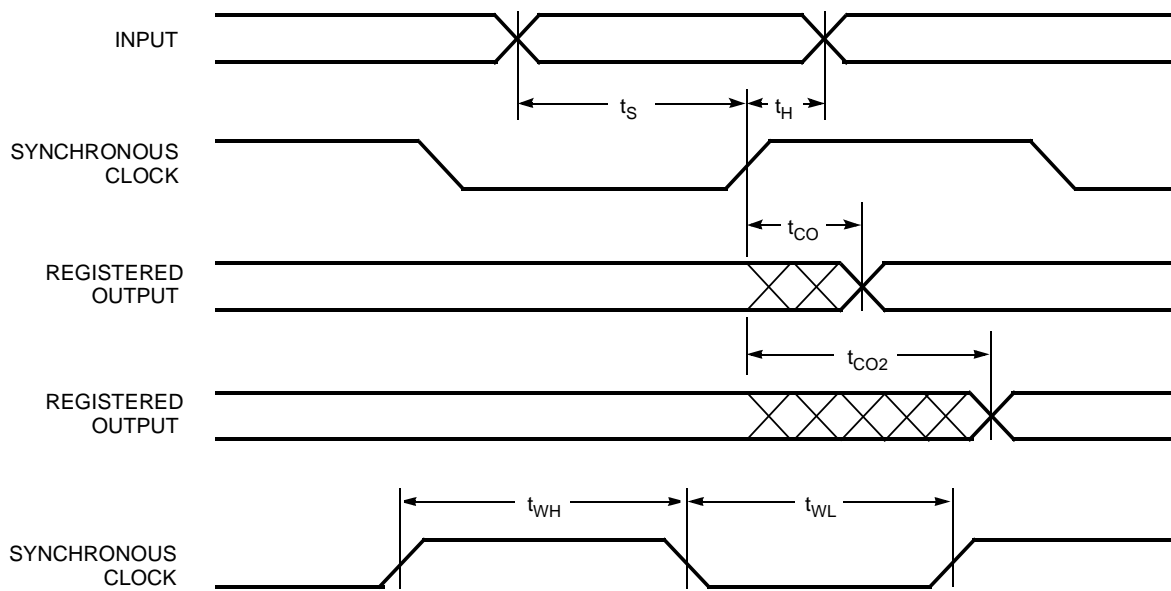
Parameter	Description	37128-167		37128-125		37128-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{IHPT}$	Buried Register Used as an Input Register or Latch Data Hold Time		6.5		9		11	ns
$t_{CO2PT}^{[10, 11, 12]}$	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)		14		19		21	ns
<b>Pipelined Mode Parameters</b>								
$t_{ICS}^{[10]}$	Input Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) to Output Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> )	6		8		10		ns
<b>Operating Frequency Parameters</b>								
$f_{MAX1}$	Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$ , $1/(t_S + t_H)$ , or $1/t_{CO}$ ) <sup>[7]</sup>	167		125		100		MHz
$f_{MAX2}$	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$ , $1/(t_S + t_H)$ , or $1/t_{CO}$ )	200		158		143		MHz
$f_{MAX3}$	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$ )	105		83		76.9		MHz
$f_{MAX4}$	Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_S)$ , $1/t_{ICS}$ , $1/(t_{WL} + t_{WH})$ , $1/(t_{IS} + t_H)$ , or $1/t_{SCS}$ )	143		125		100		MHz
<b>Reset/Preset Parameters</b>								
$t_{RW}$	Asynchronous Reset Width <sup>[7]</sup>	8		10		12		ns
$t_{RR}^{[10]}$	Asynchronous Reset Recovery Time <sup>[7]</sup>	10		12		14		ns
$t_{RO}^{[10, 11, 12]}$	Asynchronous Reset to Output		13		15		18	ns
$t_{PW}$	Asynchronous Preset Width <sup>[7]</sup>	8		10		12		ns
$t_{PR}^{[10]}$	Asynchronous Preset Recovery Time <sup>[7]</sup>	10		12		14		ns
$t_{PO}^{[10, 11, 12]}$	Asynchronous Preset to Output		13		15		18	ns
<b>User Option Parameters</b>								
$t_{LP}$	Low Power Adder		4		4		4	ns
$t_{SLEW}$	Slow Output Slew Rate Adder		2		2		2	ns
$t_{3.3IO}$	3.3V I/O Mode Timing Adder		0.1		0.1		0.1	ns
<b>JTAG Timing Parameters</b>								
$t_{S JTAG}$	Set-Up Time from TDI and TMS to TCK	0		0		0		ns
$t_{H JTAG}$	Hold Time on TDI and TMS	20		20		20		ns
$t_{CO JTAG}$	Falling Edge of TCK to TDO		20		20		20	ns
$f_{JTAG}$	Maximum JTAG Tap Controller Frequency		20		20		20	MHz

**Typical  $I_{CC}$  Characteristics**

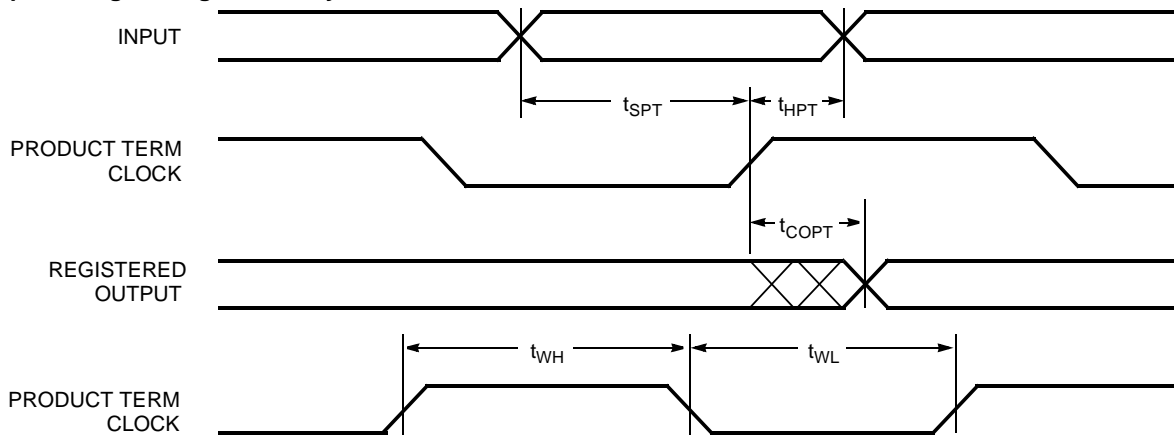
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 5.0V$ ,  $T_A = \text{Room Temperature}$

**Switching Waveforms**
**Combinatorial Output**


37128-14

**Registered Output with Synchronous Clocking**


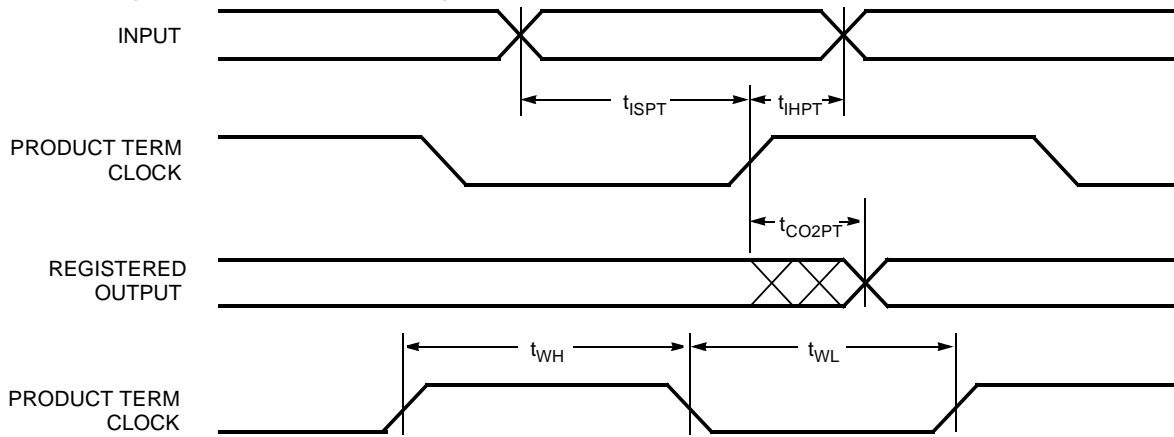
37128-15

**Registered Output with Product Term Clocking  
Input Going Through the Array**


37128-16

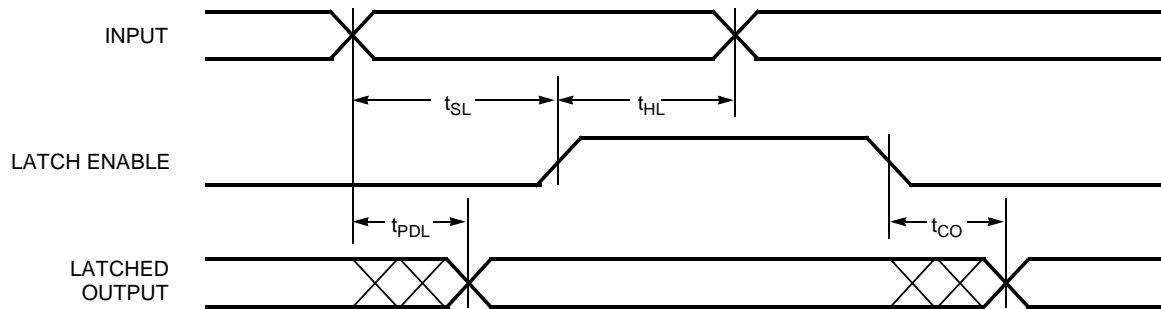
**Switching Waveforms (continued)**

**Registered Output with Product Term Clcking  
Input Coming From Adjacent Buried Register**



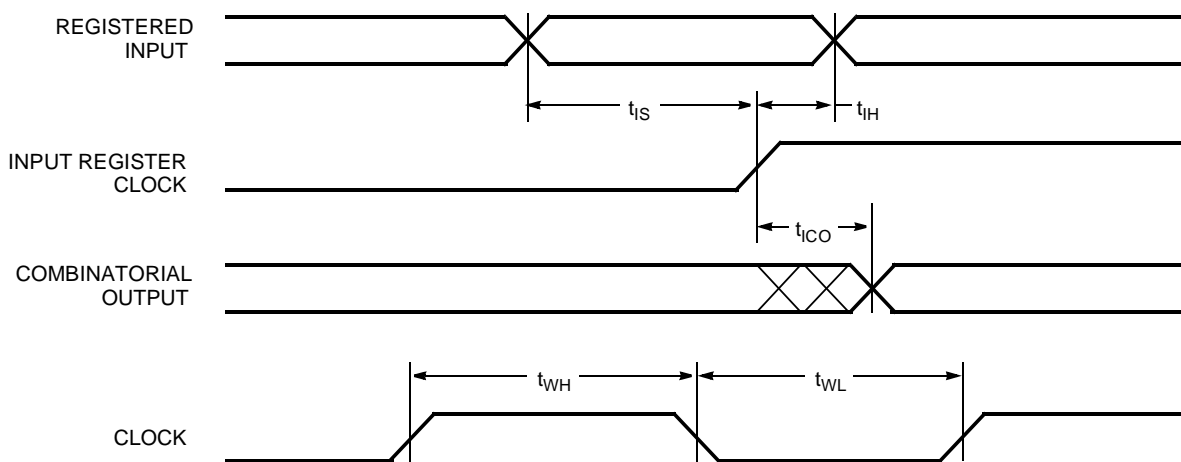
37128-17

**Latched Output**

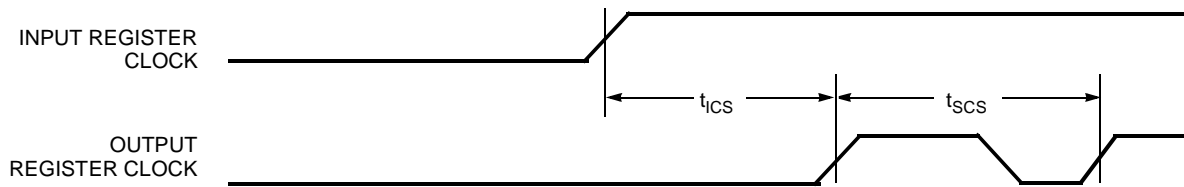


37128-18

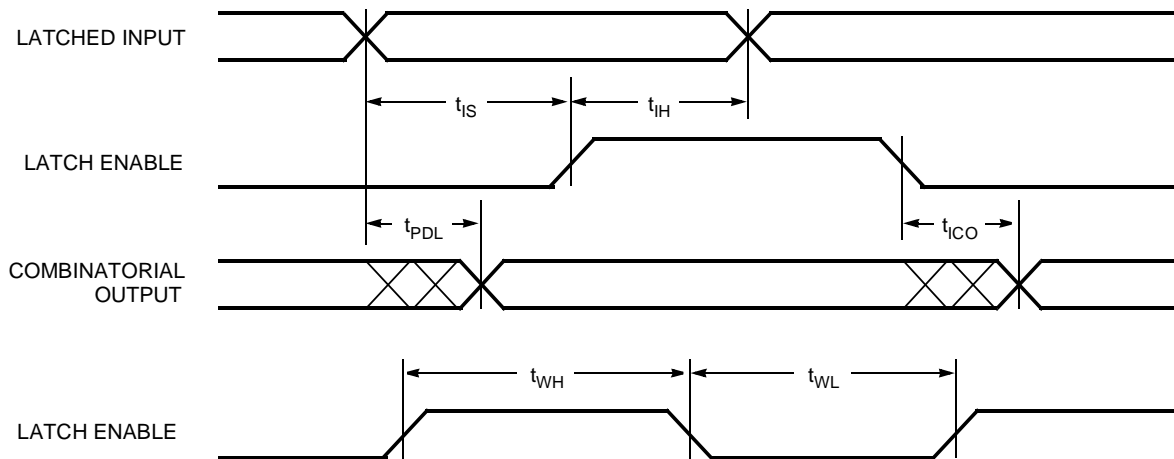
**Registered Input**



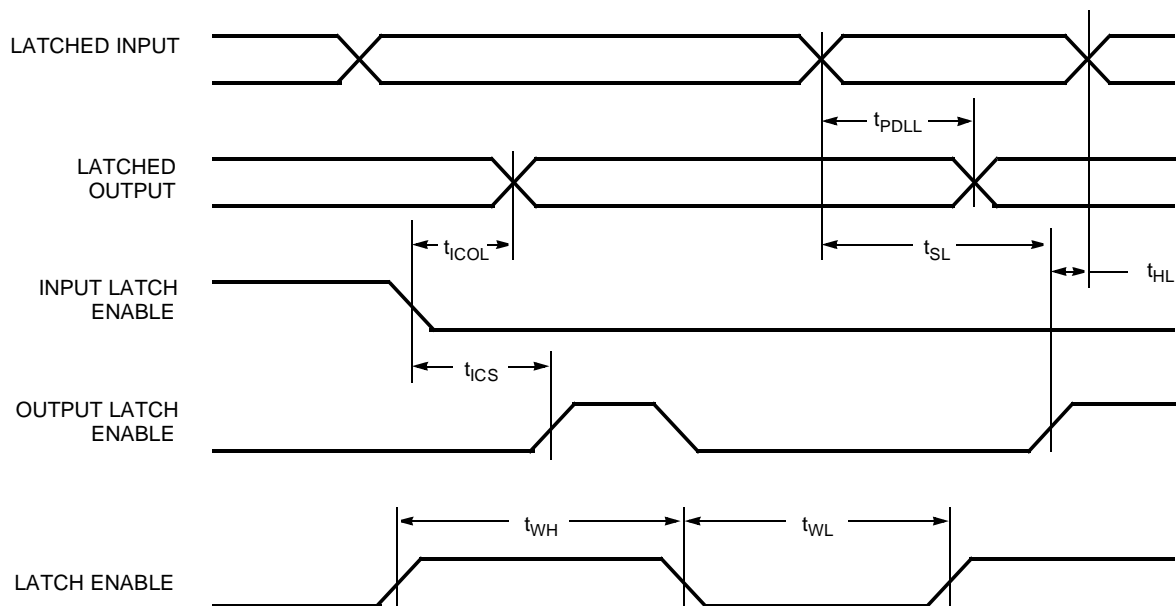
37128-19

**Switching Waveforms (continued)**
**Clock to Clock**


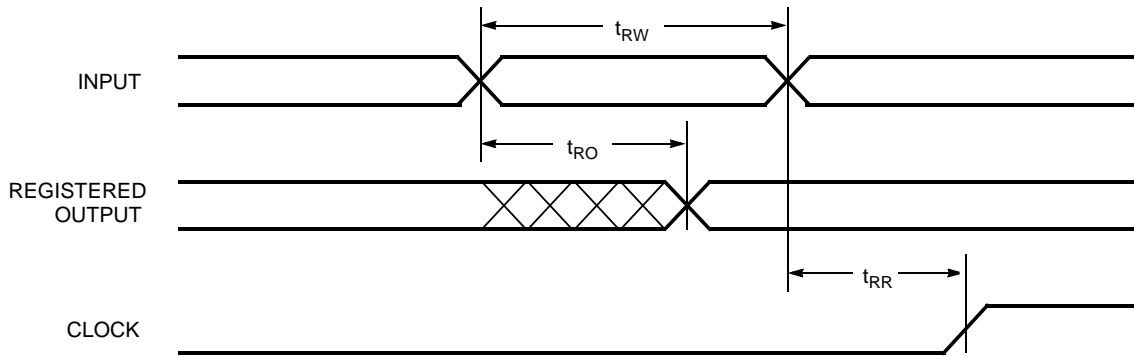
37128-20

**Latched Input**


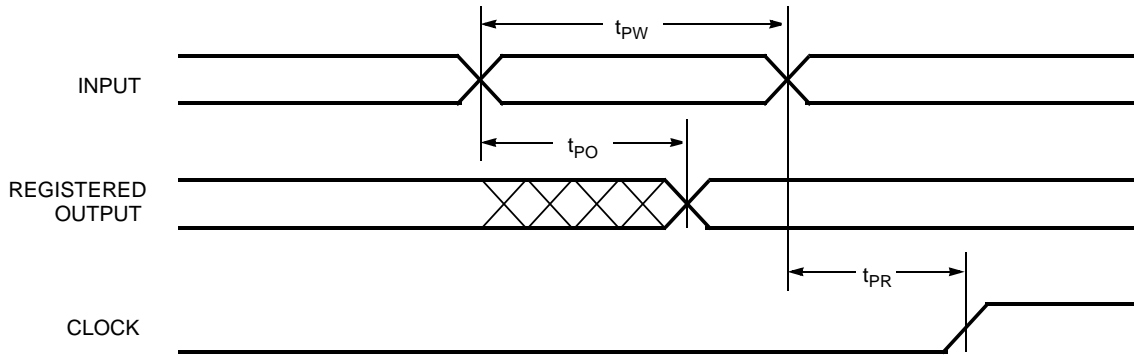
37128-21

**Latched Input and Output**


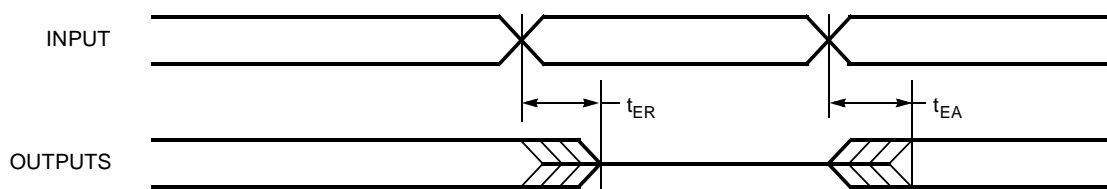
37128-22

**Switching Waveforms (continued)**
**Asynchronous Reset**


37128-23

**Asynchronous Preset**


37128-24

**Output Enable/Disable**


37128-25

**Ordering Information**

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
167	CY37128P84-167JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY37128P100-167AC	A100	100-Pin Thin Quad Flatpack	
	CY37128P160-167AC	A160	160-Pin Thin Quad Flatpack	
125	CY37128P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY37128P100-125AC	A100	100-Pin Thin Quad Flatpack	
	CY37128P160-125AC	A160	160-Pin Thin Quad Flatpack	
	CY37128P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
	CY37128P100-125AI	A100	100-Pin Thin Quad Flatpack	
	CY37128P160-125AI	A160	160-Pin Thin Quad Flatpack	
	CY37128P84-125YMB	Y84	84-Lead Ceramic Leaded Chip Carrier	
100	CY37128P84-100JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY37128P100-100AC	A100	100-Pin Thin Quad Flatpack	
	CY37128P160-100AC	A160	160-Pin Thin Quad Flatpack	
	CY37128P84-100JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
	CY37128P100-100AI	A100	100-Pin Thin Quad Flatpack	
	CY37128P160-100AI	A160	160-Pin Thin Quad Flatpack	
	CY37128P84-100YMB	Y84	84-Lead Ceramic Leaded Chip Carrier	
				Military

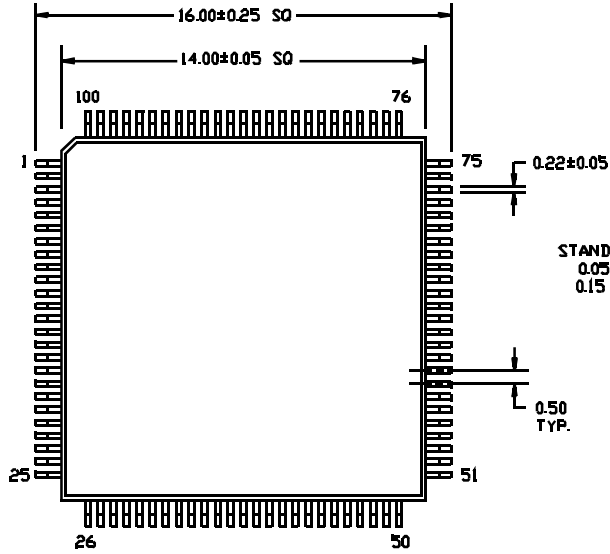
In-System Reprogrammable, ISR, UltraLogic, FLASH370, Ultra37000, InSRkit, *Impulse3*, and *Warp* are trademarks of Cypress Semiconductor Corporation.

*Warp2* and *Warp3* are registered trademarks of Cypress Semiconductor Corporation.

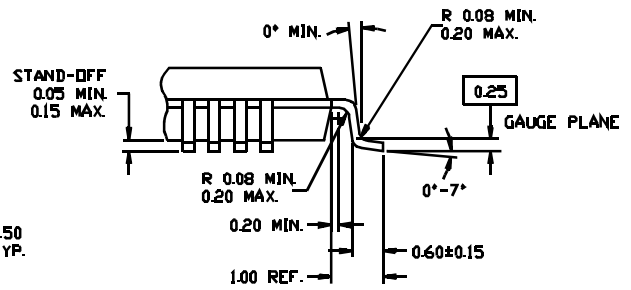


**Package Diagrams**

**100-Pin Thin Plastic Quad Flat Pack (TQFP) A100**

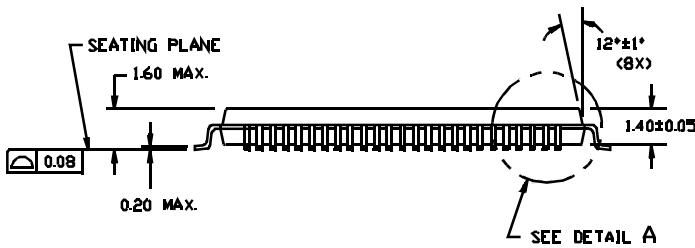


DIMENSIONS ARE IN MILLIMETERS.



51-85048-A

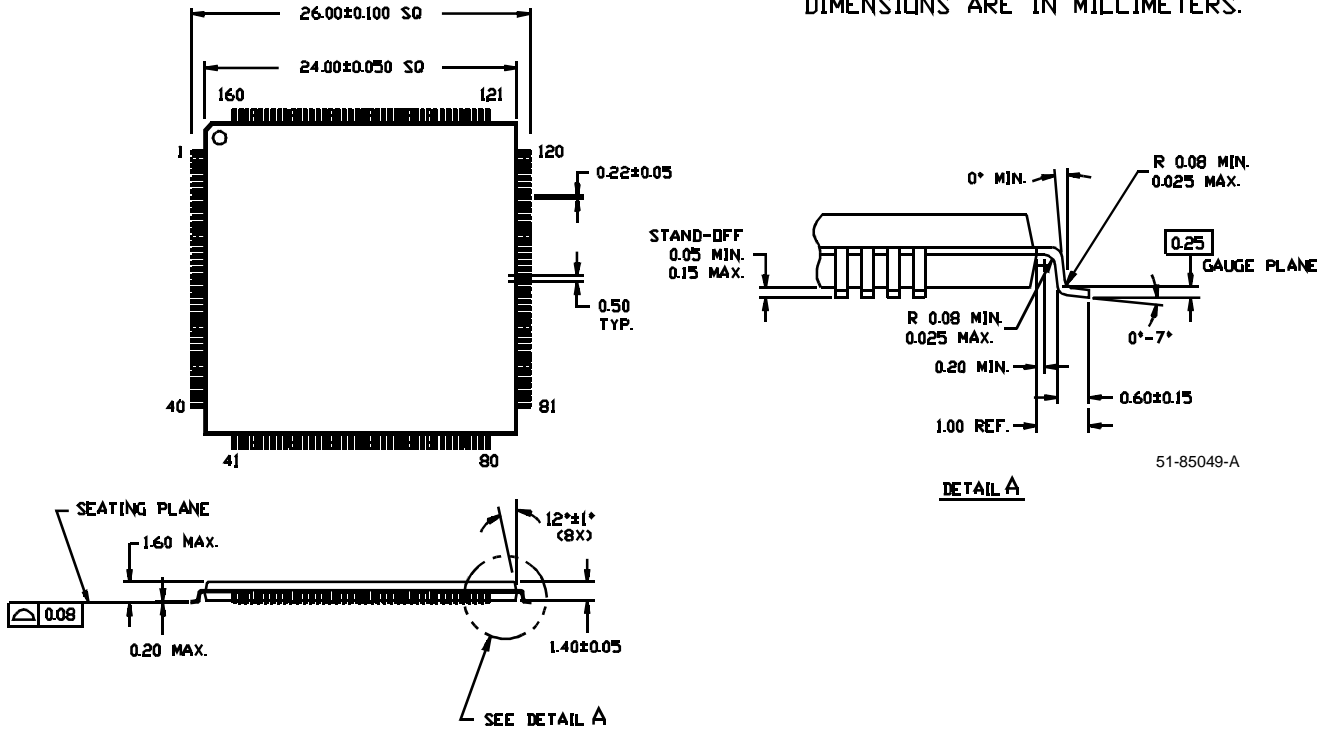
DETAIL A



Package Diagrams (continued)

**160-Pin Thin Plastic Quad Flat Pack (TQFP) A160**

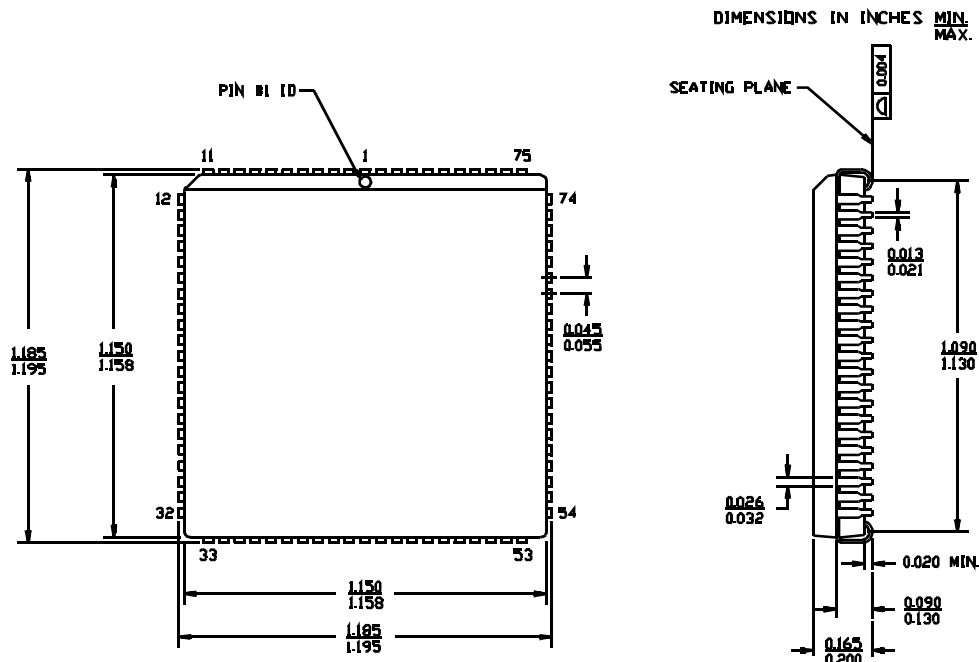
DIMENSIONS ARE IN MILLIMETERS.



51-85049-A

**84-Lead Plastic Leaded Chip Carrier J83**

DIMENSIONS IN INCHES MIN. MAX.



51-85006-A

**Package Diagrams (continued)**
**84-Pin Ceramic Leaded Chip Carrier Y84**
